

# SPECIFICATION

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**L2263**

**Current Mode PWM Controller**

**VERSION 1.1**

## Description

L2263 is highly integrated current mode PWM control IC optimized for high performance, low standby power and cost effective offline flyback converter applications in sub 30W range.

PWM switching frequency at normal operation is externally programmable to tight range. At no load or light load condition, the IC operates in extended 'burst mode' to minimize switching loss. Lower standby power and higher conversion efficiency in thus achieved.

VDD low startup current and low operating current contribute to a reliable power on startup design with L2263. A large value resistor could thus be used in the startup circuit to minimize the standby power.

L2263 offers complete protection coverage with automatic self-recovery feature including Cycle-by-Cycle current limiting (OCP), over temperature protection (OTP), VDD over voltage clamp and under voltage lockout (UVLO). The Gate output is clamped to maximum 18V to protect the power MOSFET.

### Features

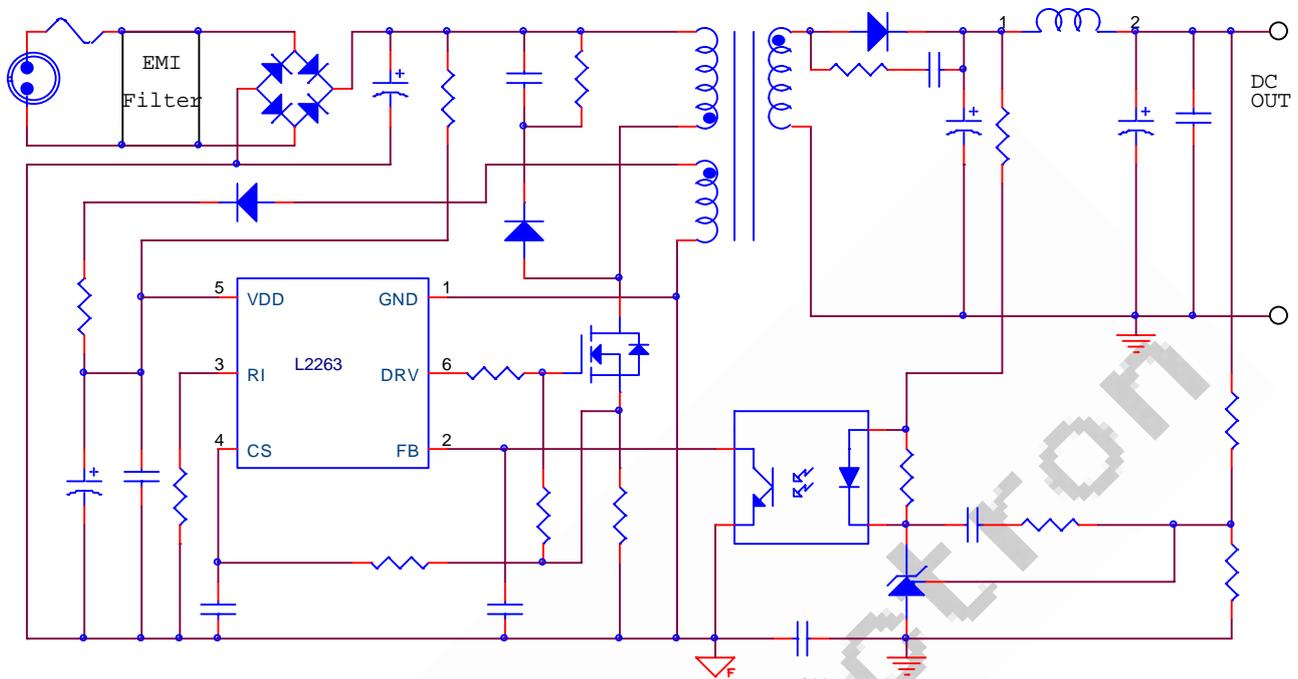
- Proprietary frequency shuffling technology for improved EMI performance.
- External programmable PWM switching frequency.

- Leading edge Blanking on current sense input.
- Internal synchronized slope compensation .
- Extended burst mode control for improved efficiency and minimum standby power design
- Low VDD startup current and low operating current.
- Gate output maximum voltage clamp
- Cycle-by-Cycle Current Limiting, Built-in Adaptive Current Peak Regulation
- Power on Soft-start, Programmable CV and CC Regulation
- VDD Under Voltage Lockout with Hysteresis (UVLO), VDD OVP, OLP, OTP, OCP, VDD Clamp
- Internal over temperature protection (OTP)

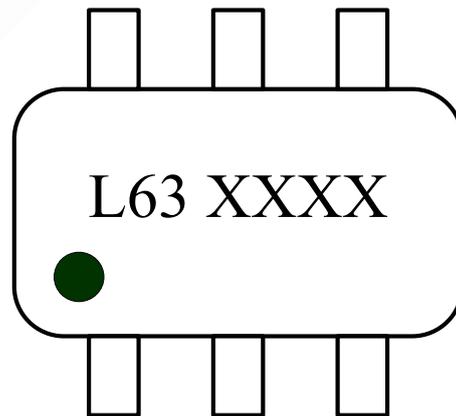
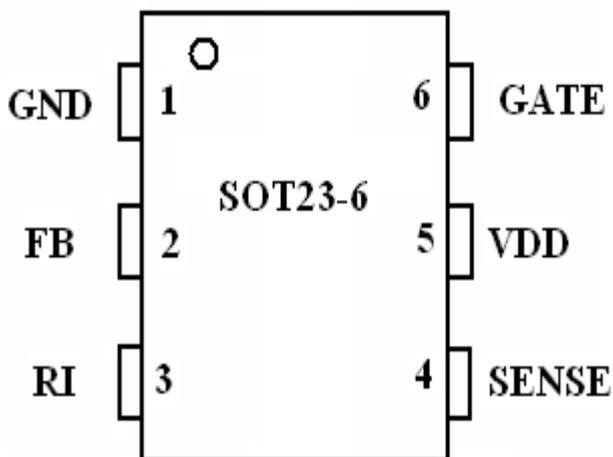
### Applications

- Cell Phone Charger
- Digital Cameras Charger
- Power adaptor
- Set\_top box power supplies
- Open\_frame SMPS
- Battery charger

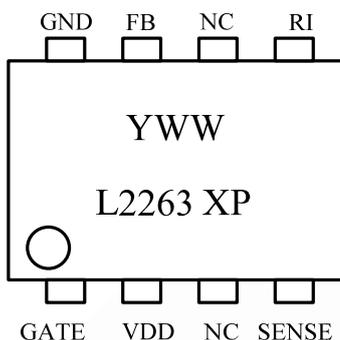
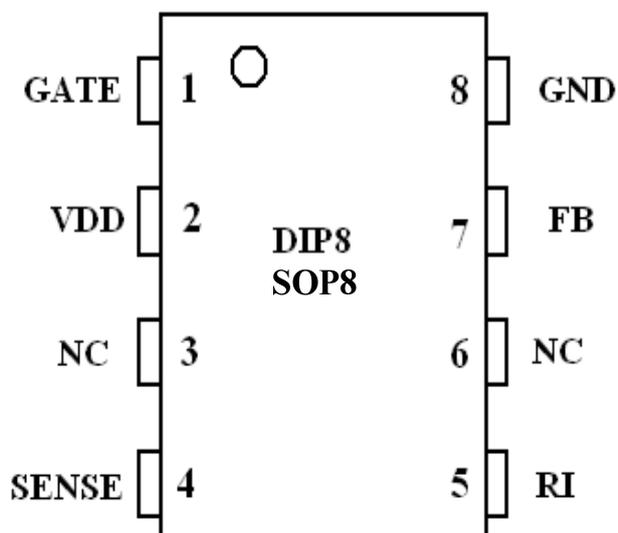
### Application Circuit



### Pin Assignment & Marking Information



XX:Year Code  
XX:WeekCode(1-52)



X:T for SOT23-6  
S for SOP-8  
D for DIP-8  
P:Pb-free Package  
Y:Year Code(0-9)  
WW:Week Code(01-52)

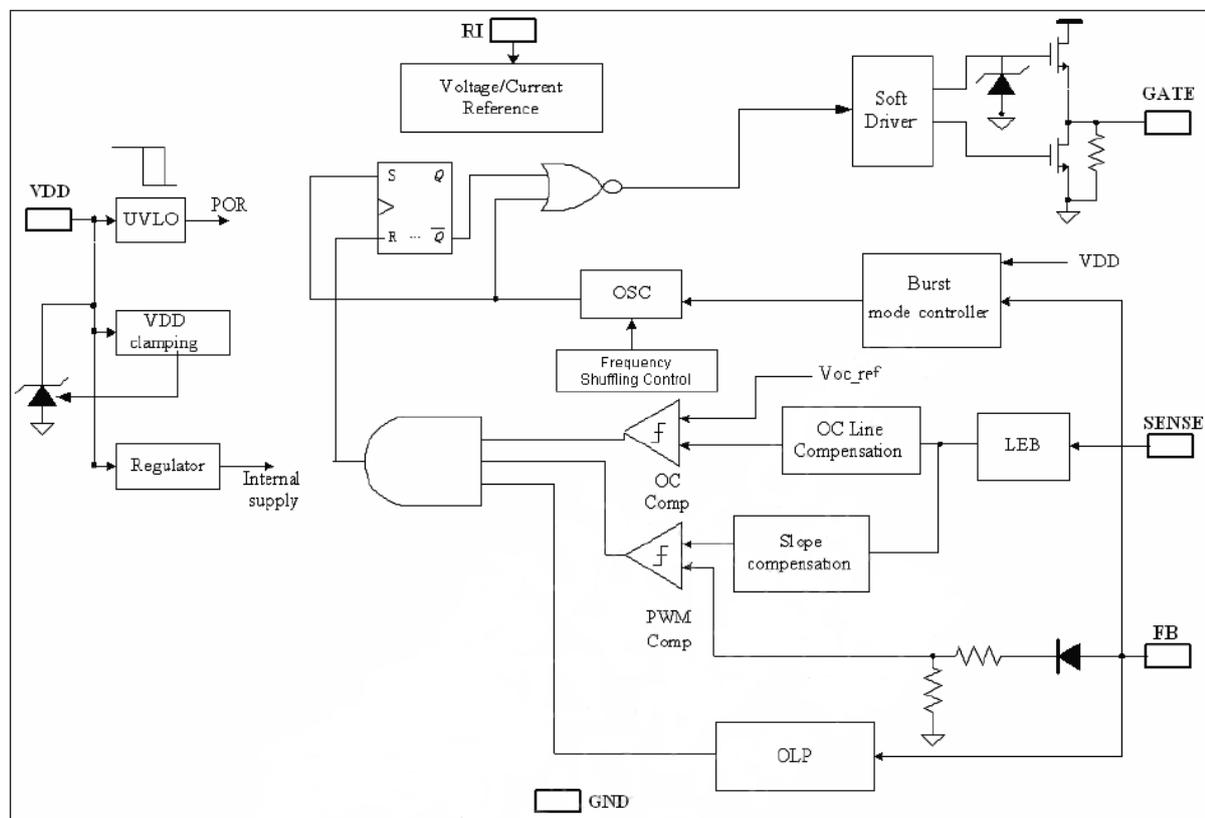
### Ordering Information

Part number	Package	version number
L2263TP	SOT23-6	
L2263SP	SOP-8	
L2263DP	DIP-8	

### Pin Description

Symbol	Type	Description
GATE	O	Totem-pole gate driver output for the power MOSFET
VDD	P	Chip DC power supply pin
SENSE	I	Current sense input pin. Connected to MOSFET current resistor node.
RI	I	Internal oscillator frequency setting pin.
FB	I	Feedback input pin. The PWM duty cycle is determined by voltage level into this pin and SENSE pin input.
Gnd	P	Ground.

## Block Diagram



## Absolute Maximum Rating

Parameter	Value	Unit
VDD supply voltage	30	V
VDD clamp voltage	32	V
VDD clamp current	10	mA
VFB input voltage	-0.3 to 7	V
VSENSE input voltage to SENSE pin	-0.3 to 7	V
VRI input voltage to RI Pin	-0.3 to 7	V
Min/Max operating junction temperature	-55 to 150	°C
Operating ambient temperature	-20 to 85	°C

### Recommended Operating Conditions

Symbol	Parameter	Min. Max.	Unit
VDD	Supply Voltage Vcc	10 to 30	V
RI	RI Resistor Value	100	Kohm
T <sub>OA</sub>	Operating Ambient Temperature	-20 to 85	°C

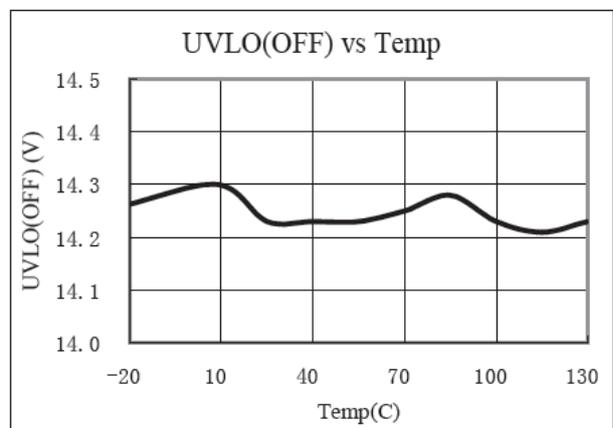
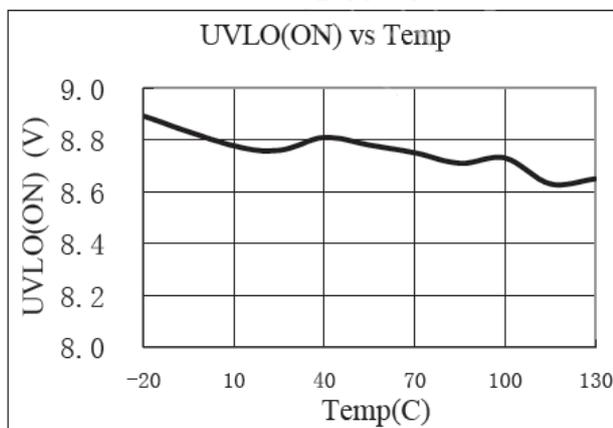
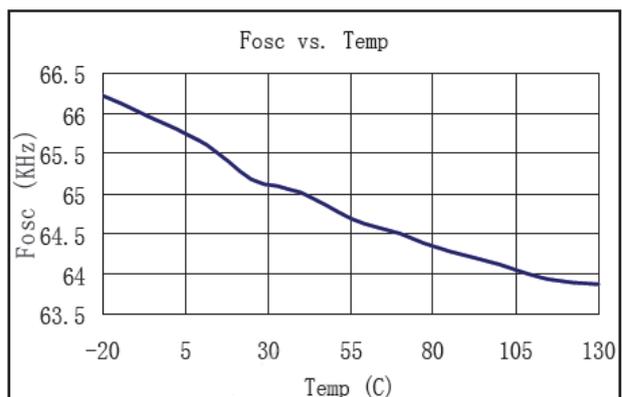
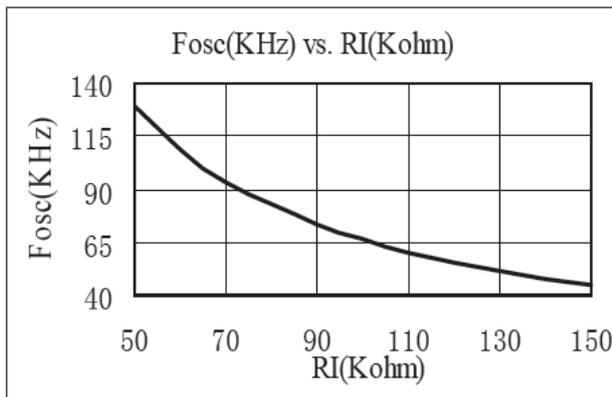
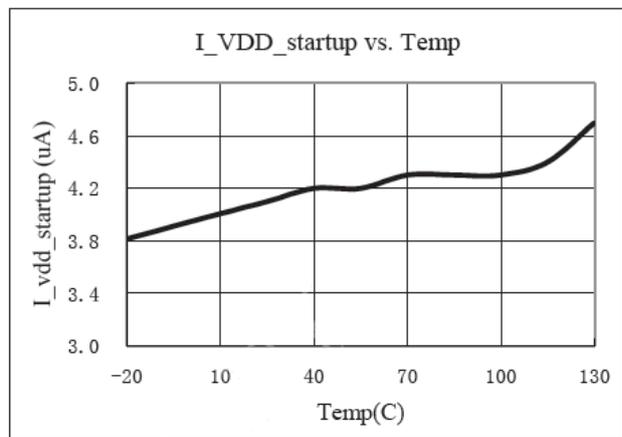
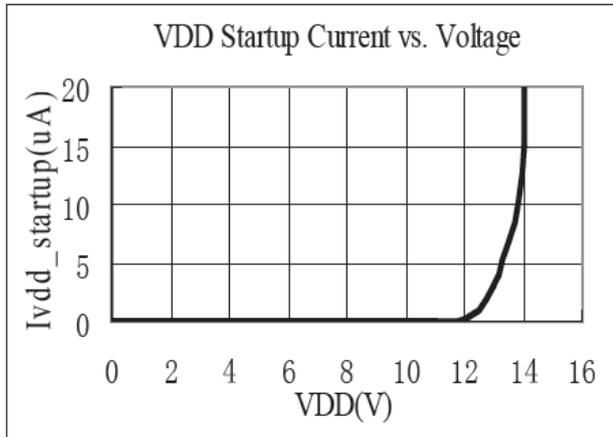
### Electrical Characteristics(T<sub>A</sub> = 25 °C, if not otherwise noted)

Symbol	Parameter	Conditions	Value			Unit
			Min.	Typ.	Max	
<b>Supply Voltage(V<sub>ad</sub> Pin)</b>						
I <sub>dd_startup</sub>	VDD start up current	VDD=12.5V,RI=100K		3	10	uA
I <sub>dd</sub>	VDD Operation current	VDD=16V RI=100K Ω , FB=3V		2.3		mA
UVLO(ON)	VDD under voltage lockout enter		7.7	8.8	9.8	V
UVLO(OFF)	VDD under voltage lockout exit		13	14	15	V
VDD_clamp	VDD zener clamp voltage	I <sub>dd</sub> =10mA	27	29	31	V
<b>Voltage Feedback (FB Pin)</b>						
AVCS	PWM input gain	Δ VFB/ Δ VSENSE		2		V/V
VFB_open	VFB open loop voltage			5.7		V
IFB_short	FB pin short current	Short FB pin to GND and measure current	0.75	0.865	0.98	mA
VFB_burst	Burst mode voltage			1.2		V
VTH_PL	Power limiting FB threshold voltage	I <sub>out</sub> =-10mA		3.7		V
TD_PL	Power limiting debounce time			32		mS

DC_MAX	Maximum duty cycle	VDD=18V,SENSE=0V RI=100K $\Omega$ ,FB=3V		75		%
<b>Current Sensing (SEN Pin)</b>						
T_blanking	Leading edge blanking time	RI=100K $\Omega$		250		nS
ZSENSE_IN	Input impedance			40		K $\Omega$
VTH_sense	Over current threshold voltage			0.9		V
<b>Oscillator</b>						
Fosc	Normal oscillation frequency	RI=100K $\Omega$	60	65	70	Khz
$\Delta f_{temp}$	Frequency temperature stability	VD TA -20 $^{\circ}$ C to 100 $^{\circ}$ C D=16V,RI=100K $\Omega$		5		%
$\Delta f_{VDD}$	Frequency voltage stability	VDD=12V to 25V RI=100K $\Omega$		5		%
RI_range	Operating RI range		50	100	150	K $\Omega$
VRI_open	RI open load voltage			2		V
Fosc_BM	Burst mode base frequency			25		Khz
$\Delta f_{OSC}$	Frequency modulation range /Base frequency	RI=100K $\Omega$	-5		+5	%
<b>Gate Drive Output</b>						
VOL	Output low level	VDD=16V,IO=-20mA			0.8	V
VOH	Output high level	VDD=16V,IO=20mA	10			V
V_Clamp	output clamp voltage level			18		V
T_r	Output rising time	VDD=16V,CL=1nF		220		nS
T_f	Output falling time	VDD=16V,CL=1nF		70		nS

### Characterization Plots

VDD = 16V, RI = 100 Kohm, TA = 25oC condition applies if not otherwise noted.



## Application Information

The L2263 is a highly integrated PWM controller IC optimized for offline flyback converter applications in sub 30W power range. The extended burst mode control greatly reduces the standby power consumption and helps the design easily meet the international power conservation requirements.

### Startup Current and Start up Control

Startup current of L2263 is designed to be very low so that VDD could be charged up above UVLO threshold level and device starts up quickly. A large value startup resistor can therefore be used to minimize the power loss yet provides reliable startup in application. For AC/DC adaptor with universal input range design, a 2 M $\Omega$ , 1/8 W startup resistor could be used together with a VDD capacitor to provide a fast startup and low power dissipation solution.

### Operating Current

The Operating current of L2263 is low at 2.3mA. Good efficiency is achieved with L2263 low operating current together with extended burst mode control features.

### Frequency shuffling for EMI improvement

The frequency Shuffling/jittering (switching frequency modulation) is implemented in L2263. The oscillation frequency is modulated with a random source so that the tone energy is spread out. The spread spectrum minimizes the conduction band EMI and therefore reduces system design challenge.

### ended Burst Mode Operation

At zero load or light load condition, majority of the power dissipation in a switching mode power supply is from switching loss on the MOSFET transistor, the core loss of the

transformer and the loss on the snubber circuit. The magnitude of power loss is in proportion to the number of switching events within a fixed period of time. Reducing switching events leads to the reduction on the power loss and thus conserves the energy. L2263 self adjusts the switching mode according to the loading condition. At from no load to light/medium load condition, the FB input drops below burst mode threshold level. Device enters Burst Mode control. The Gate drive output switches only when VDD voltage drops below a preset level and FB input is active to output an on state. Otherwise the gate drive remains at off state to minimize the switching loss and reduces the standby power consumption to the greatest extend. The frequency control also eliminates the audio noise at any loading conditions.

### Oscillator Operation

A resistor connected between RI and GND sets the constant current source to charge/discharge the internal cap and thus the PWM oscillator frequency is determined. The relationship between RI and switching frequency follows the below equation within the specified RI in Kohm range at nominal loading operational condition.

$$F_{osc} = 6500/RI(K\Omega) \quad (Khz)$$

### Current Sensing and Leading Edge Blanking

Cycle-by-Cycle current limiting is offered in L2263 current mode PWM control. The switch current is detected by a sense resistor into the sense pin. An internal leading edge blanking circuit chops off the sense voltage spike at initial MOSFET on state due to Snubber diode reverse recovery so that the external RC filtering on sense input is no longer required. The current limit comparator is disabled and

thus cannot turn off the external MOSFET during the blanking period. PWM duty cycle is determined by the current sense input voltage and the FB input voltage.

### **Internal Synchronized Slope Compensation**

Built-in slope compensation circuit adds voltage ramp onto the current sense input voltage for PWM generation. This greatly improves the close loop stability at CCM and prevents the sub-harmonic oscillation and thus reduces the output ripple voltage.

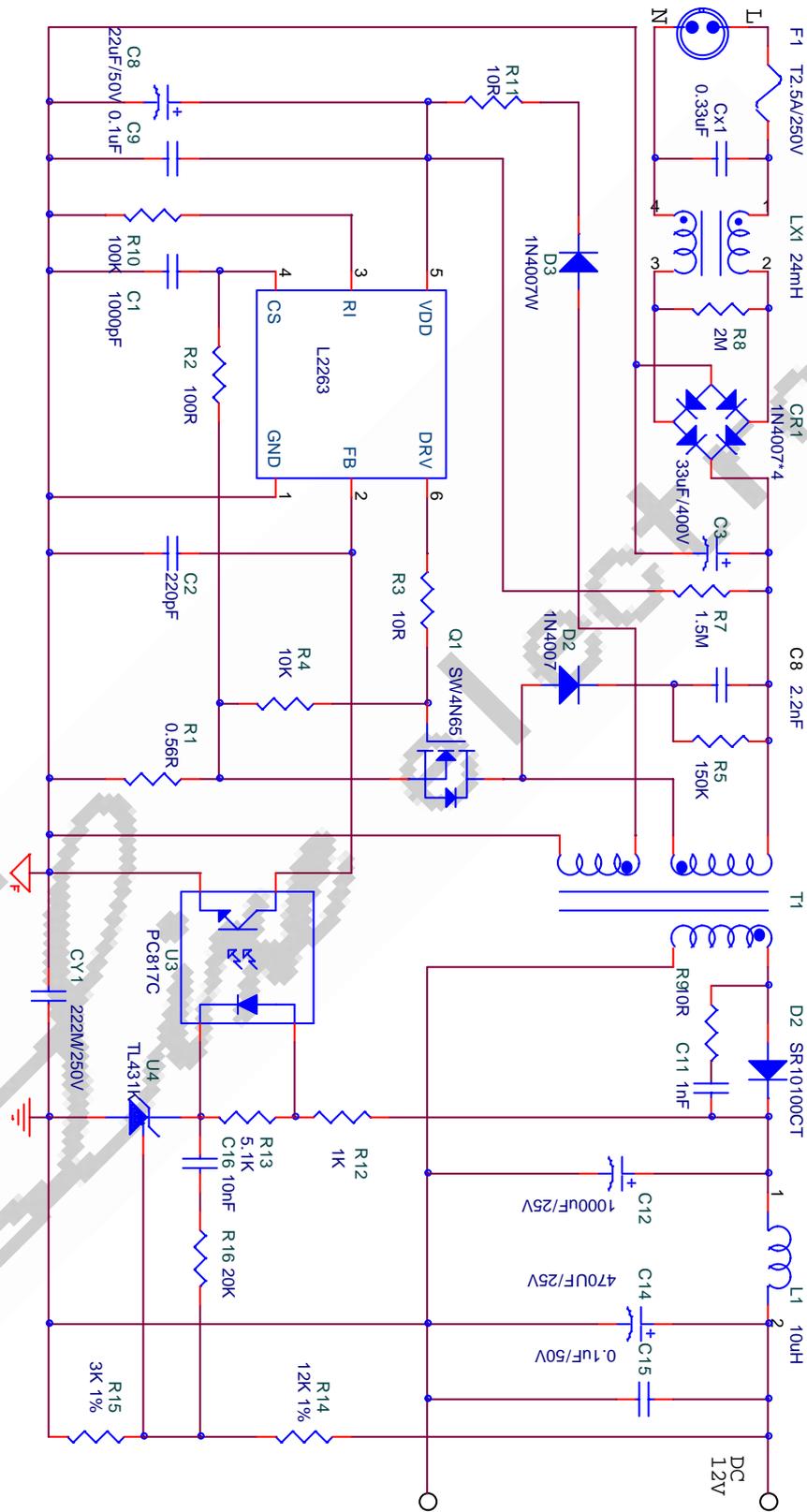
### **Gate Drive**

L2263 Gate is connected to an external MOSFET gate for power switch control. Too weak the gate drive strength results in higher conduction and switch loss of MOSFET while too strong gate drive output compromises the EMI. A good tradeoff is achieved through the built-in totem pole gate design with right output strength and dead time control. The low idle loss and good EMI system design is easier to achieve with this dedicated control scheme. An internal 18V clamp is added for MOSFET gate protection at higher than expected VDD input.

### **Protection Controls**

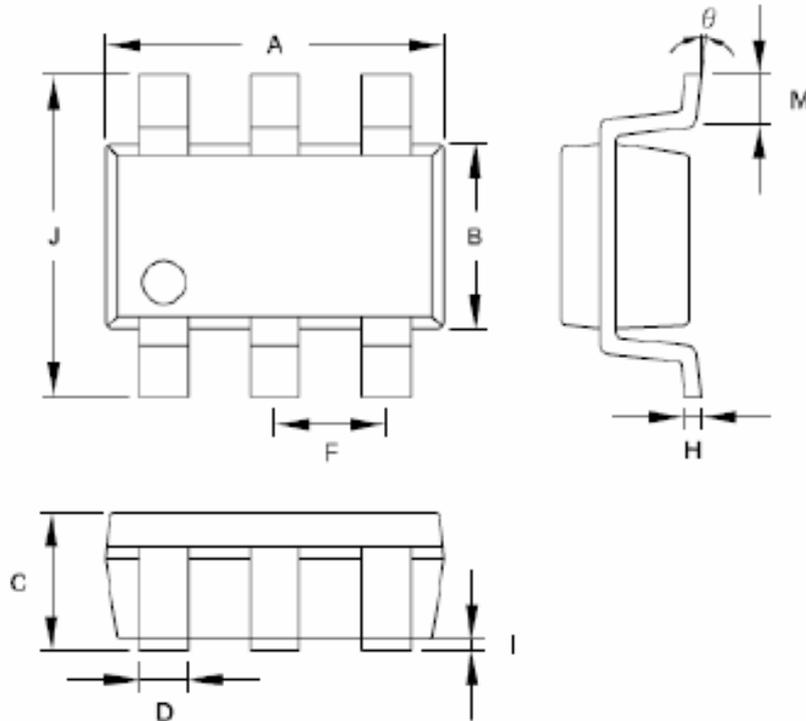
Good power supply system reliability is achieved with its rich protection features including Cycle-by-Cycle current limiting (OCP), Over Load Protection (OLP) and over voltage clamp, Under Voltage Lockout on VDD (UVLO). With On-Bright Proprietary technology, the OCP threshold tracks PWM Duty cycles and is line voltage compensated to achieve constant output power limit over the universal input voltage range with recommended reference design. At overload condition when FB input voltage exceeds power limit threshold value for more than TD\_PL, control circuit reacts to shut down the output power MOSFET. Device restarts when VDD voltage drops below UVLO limit. VDD is supplied by transformer auxiliary winding output. It is clamped when VDD is higher than threshold value. The power MOSFET is shut down when VDD drops below UVLO limit and device centers power on start-up sequence thereafter.

Typical Application Schematic



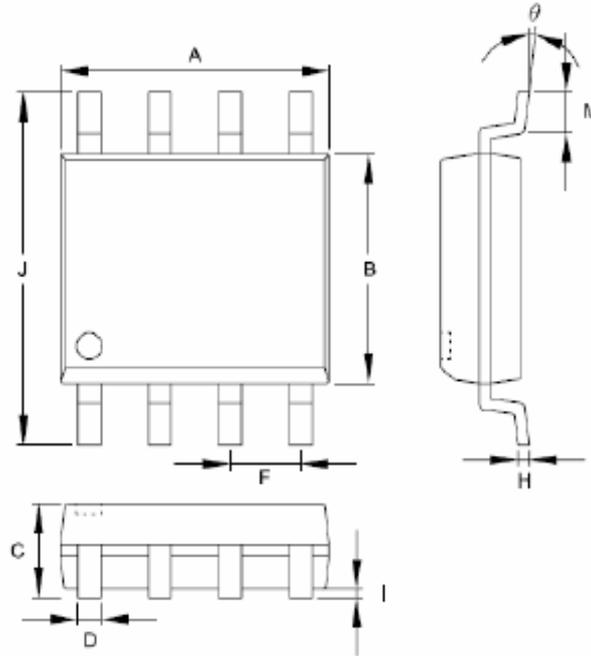
**Package Information**

SOT-23-6



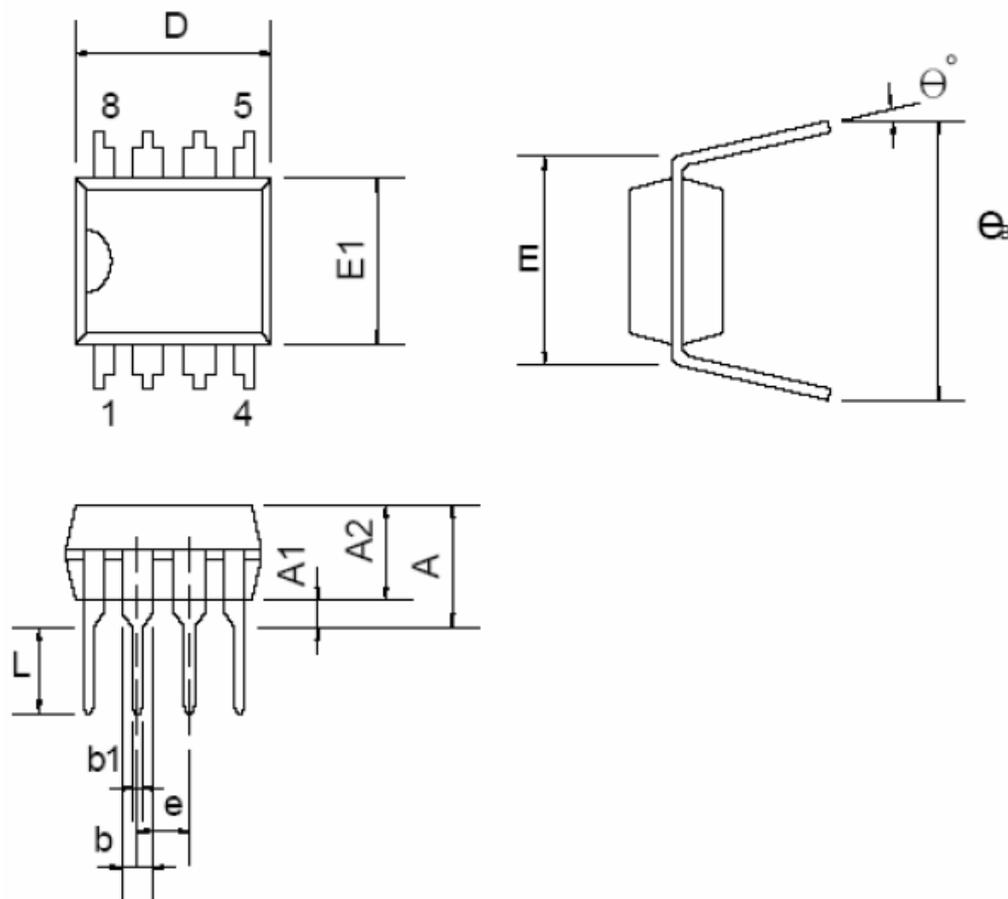
Symbol	Dimension in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	2.692	3.099	0.106	0.122
B	1.397	1.803	0.055	0.071
C	-----	1.450	-----	0.058
D	0.300	0.550	0.012	0.022
F	0.838	1.041	0.033	0.041
H	0.080	0.254	0.003	0.010
I	0.050	0.150	0.002	0.006
J	2.600	3.000	0.102	0.118
M	0.300	0.600	0.012	0.024
θ	0°	10°	0°	10°

SOP-8



Symbols	Dimensions in Millimeters		Dimensions in Inch	
	MIN	MAX	MIN	MAX
A	4.801	5.004	0.189	0.197
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.178	0.229	0.007	0.009
I	0.102	0.254	0.004	0.010
J	5.791	6.198	0.228	0.244
M	0.406	1.270	0.016	0.050
$\theta$	0°	8°	0°	8°

DIP-8



Dimensions

Symbol	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			5.334			0.210
A1	0.381			0.015		
A2	3.175	3.302	3.429	0.125	0.130	0.135
b		1.524			0.060	
b1		0.457			0.018	
D	9.017	9.271	10.160	0.355	0.365	0.400
E		7.620			0.300	
E1	6.223	6.350	6.477	0.245	0.250	0.255
e		2.540			0.100	
L	2.921	3.302	3.810	0.115	0.130	0.150
eB	8.509	9.017	9.525	0.335	0.355	0.375
θ°	0°	7°	15°	0°	7°	15°