

Power Supply

All power supplies described below are a black box for Service. When defective, a new board must be ordered and the defective one must be returned, unless the main fuse of the board is broken. Always replace a defective fuse with one with the correct specifications! This part is available in the regular market.

Consult the Service Spare Parts website for the order codes of the boards.

7.2.1 Specifications

Most sets in the TV543 platform use the Integrated Power Board (IPB) - incl. inverter. The 52" sets in this chassis have a conventional PSU - with separate inverter.

In this Service Manual, no detailed information is available because of design protection issues.

7.2.2 Diversity

Below find an overview of the different PSUs that are used:

Table 7-1 Supply diversity

Supplier	PSU	Model	Input Voltage Range
LGIT	PLHL-T826B	32PFL7404H/12	High Mains (198 to 265 V _{AC})
Delta	DPS-298CP-4 A	42PFL7404H/12	High Mains (198 to 265 V _{AC})
Delta	DPS-298CP-2 A	47PFL7404H/12	High Mains (198 to 265 V _{AC})
Delta	DPS-411AP-3 A	52PFL7404H/12	High Mains (198 to 265 V _{AC})
LGIT	PLHL-T826B	32PFL8404H/12	High Mains (198 to 265 V _{AC})
Delta	DPS-298CP A	37PFL8404H/12	High Mains (198 to 265 V _{AC})
Delta	DPS-298CP-4 A	42PFL8404H/12	High Mains (198 to 265 V _{AC})
Delta	DPS-298CP-2 A	47PFL8404H/12	High Mains (198 to 265 V _{AC})

7.2.3 Application

An application diagram can be found below:

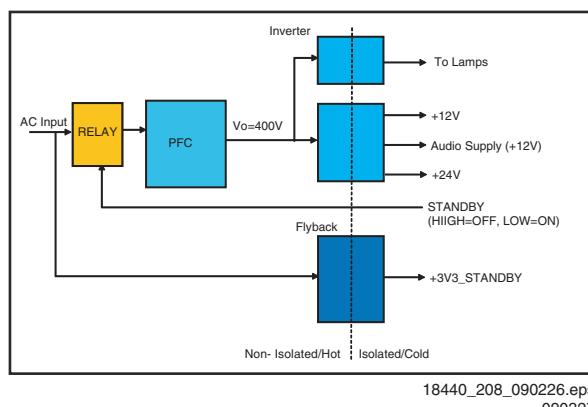


Figure 7-3 Application Integrated Power Board

7.2.4 Power Supply Timing

The STANDBY signal controls the on-mode voltages +12V, +V_{snd} and +24V. During chassis cold start from AC mains, +12V can be expected to be stable within 1.0 seconds, while for a warm start, i.e. wake up from stand-by power state, this timing becomes 0.5 seconds maximum. During AC switch off, stand-by power +3V3-STANDBY decay is at least 20 ms but not more than 5.0 seconds compared to +12V. Refer to [Figure 7-4](#):

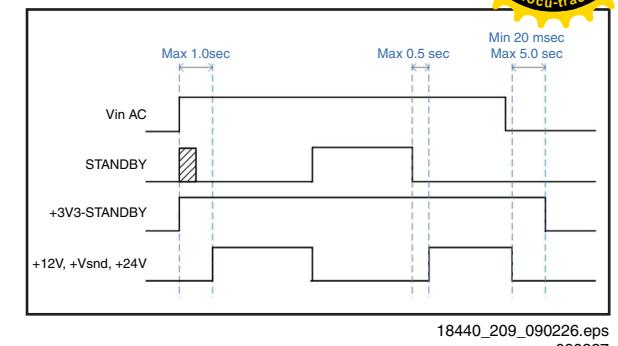


Figure 7-4 PSU Timing Diagram

7.2.5 Power Supply Protection

Power supply protection is implemented via the stand-by controller of the PNX8543 via the following signals:

- POWER-OK: signal from PSU to indicate if the supply output from the IPB is normal
- DETECT1: signal to indicate if the +5V, +3V3 and +1V2 voltages on the chassis are present
- DETECT2: signal to indicate if the +12V voltage on the chassis is present.

7.3 DC-DC Converter

Input power is obtained from the IPB module via the following voltages:

- +3V3-STANDBY (stand-by-mode only)
- +12V (on-mode)
- +V_{snd} (audio power) (on-mode)
- +24V (bolt-on power) (on-mode).

Control is achieved by the PNX8543 controller via the STANDBY signal.

Audio power is specifically for audio supply usage only and does not go through any DC conversion.

Below find a block diagram of the on-board DC-DC converters.

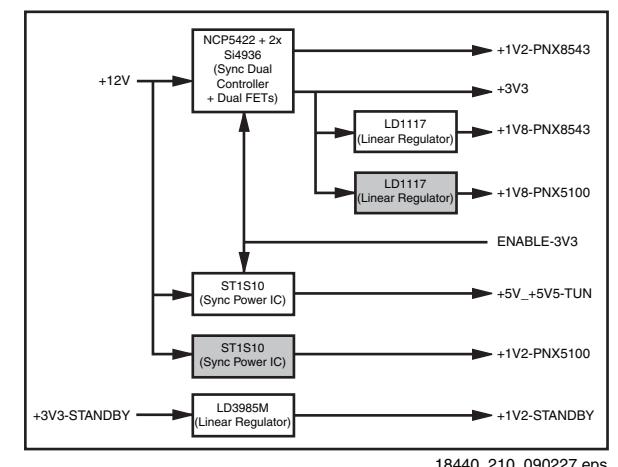


Figure 7-5 DC-DC converters

Front-End

The Front-End consist of the following key components:

- Tuner HD1816AF
- IF demodulator DRX3926K
- AGC amplifier UPC3221GV
- SAW filter 36M125.

Below find a block diagram of the front-end application.

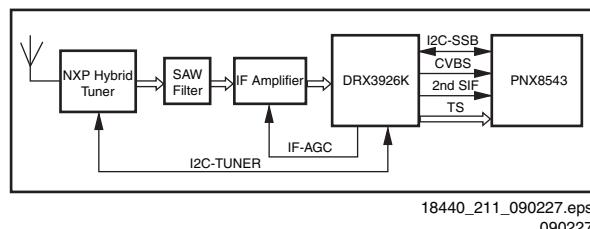


Figure 7-6 Front-End block diagram

The DRX3926K is a multi-standard demodulator supporting DVB-C, DVB-T and analogue standards. The demodulated digital stream is fed into the parallel transport stream data ports of the PNX8543. The demodulated analogue signal in the form of CVBS is connected to the analogue video CVBS/Y input channel, while the SIF is connected via the SSIF2 positive input port.

7.5 HDMI

In this platform, the TDA9996 HDMI multiplexer is implemented. The EDID contents are no longer stored in a separate EEPROM, but directly in the multiplexer. Each input has its own physical sub address: the first 253 bytes are common, where the last 3 bytes define the specific input. The EDID contents are, at +5V power-up, downloaded to RAM. The following figures show the HDMI input configuration and EDID control.

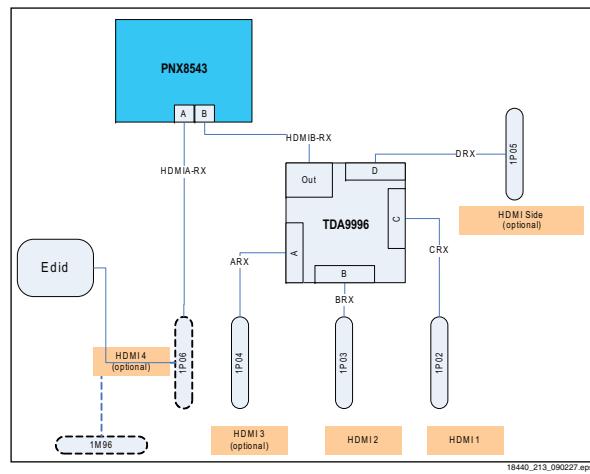


Figure 7-7 HDMI input configuration

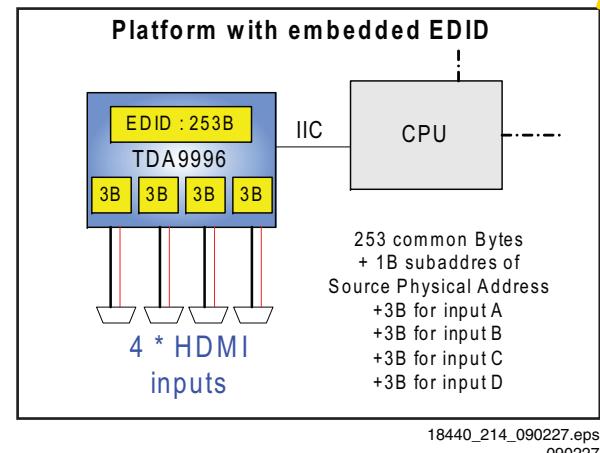


Figure 7-8 EDID control (embedded EDID)

Some delta's w.r.t. TDA9996 compared to earlier chassis/platforms are:

- +5V detection mechanism
- stable clock detection mechanism
- integrated EDID
- RT control
- HPD control
- TMDS output control
- CEC control
- new hot-plug control for PNX8543 for 5th HDMI input
- new EDID structure: EDID stored in TDA9996, therefore there are no EDID pins on the SSB. Only in the event of a 5th HDMI input, an additional EEPROM is foreseen, as was implemented in previous platforms.

Some delta's with respect to PNX8543 compared to earlier chassis/platforms are:

- 2 HDMI inputs (A & B)
- HDMI deep colour RGB/YCbCr 4:4:1 10/12 bit detection.

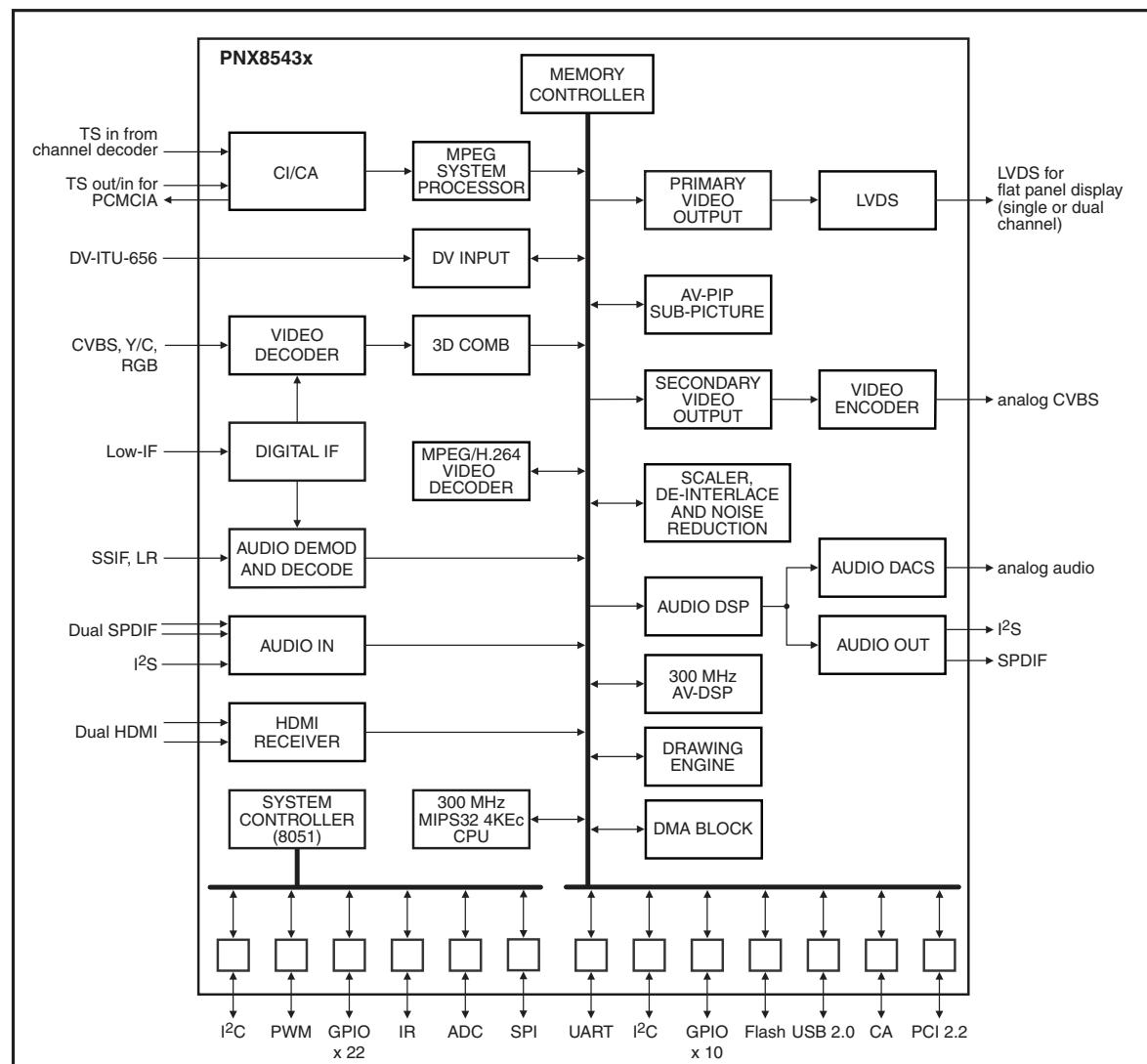
After replacement of the TDA9996 HDMI multiplexer, the default I₂C address should be reprogrammed from C0 to CE, and the HDMI EDIDs should be reprogrammed as well. Both actions should be executed via ComPair.

Video and Audio Processing - PNX8543

The PNX8543 is the main audio and video processor (or System-on-Chip) for this platform. It is a member of the PNX85xx SoC family (described in earlier chassis) with the addition of the MPEG4 functionality; the separate STi710x MPEG4 decoder is no longer implemented in this platform.

The PNX8543 handles the digital and analogue video decoding and processing. The processor is a 300 MHz general purpose CPU and a 8051-based TV controller for power management and user event handling.

- For a functional diagram of the PNX8543, refer to [Figure 7-9](#).

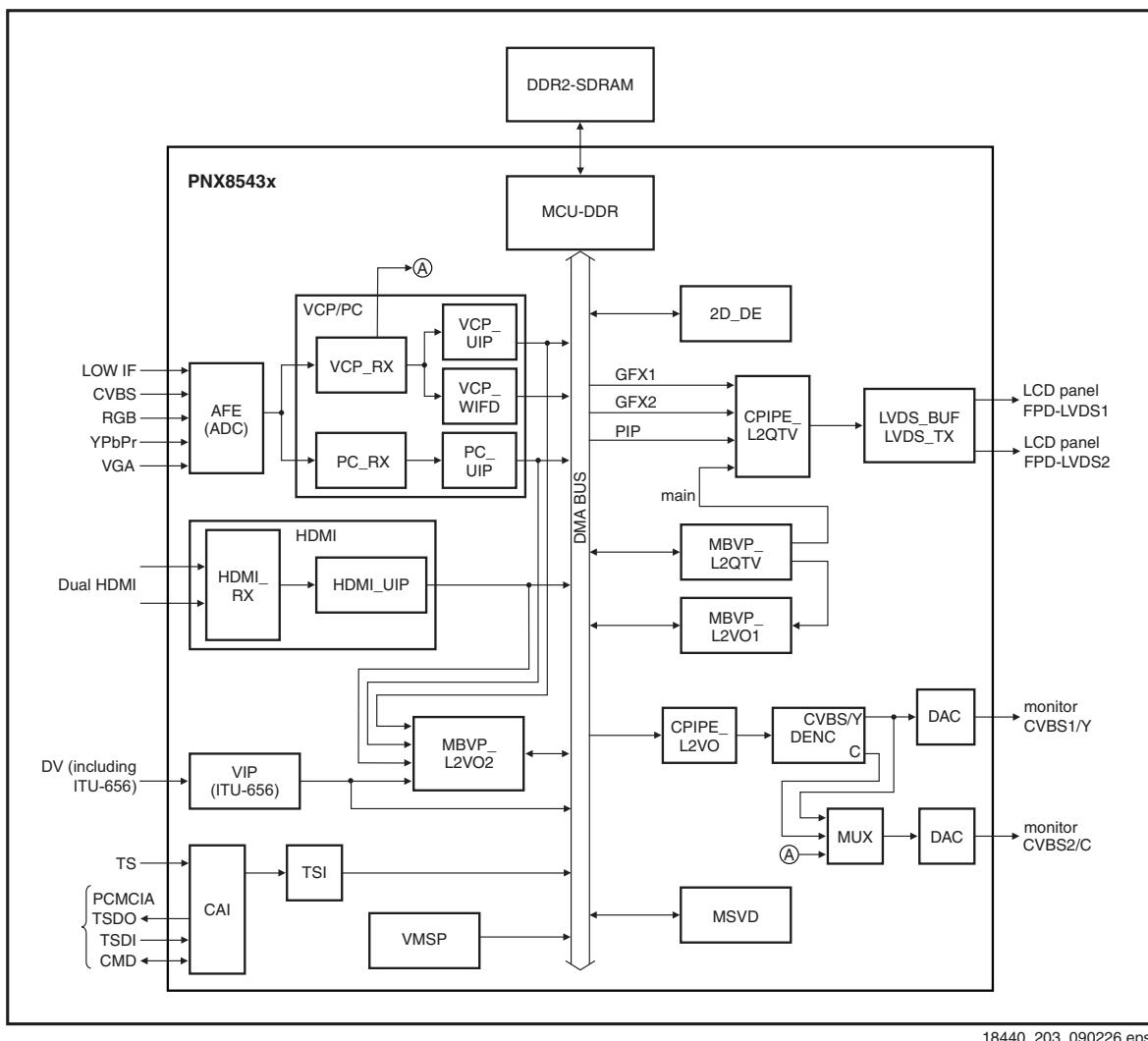


18440_202_090226.eps
090226

Figure 7-9 PNX8543 functional diagram

Subsystem

Refer to [Figure 7-10](#) for the main video interfaces for the PNX8543 and the video signal flow between blocks and memory.



18440_203_090226.eps
090226

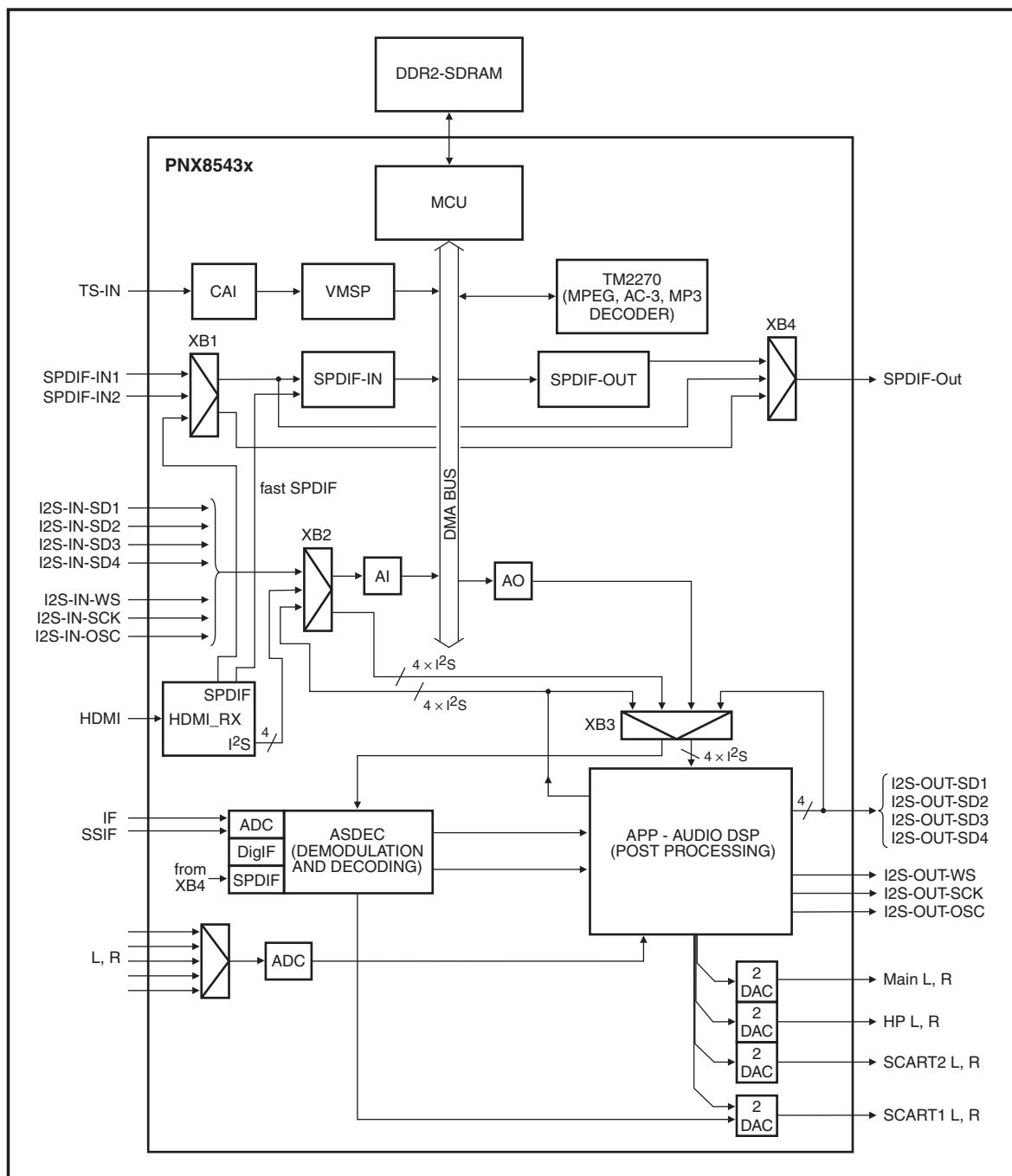
Figure 7-10 PNX8543 video flow diagram

The Video Subsystem consist of the following blocks:

- Analogue Front-End (AFE) block
- Video and PC Capture (VPC/PC) pipe
- HDMI Receiver interface
- Memory-Based Video Processor MBVP
- Video Composition Pipe (CPIPE)
- Memory Based Video Processor (MBVP) VO-1
- Memory Based Video Processor (MBVP) VO-2
- Video Composition Pipe (CPIPE)
- Dual Flat Panel Display-LVDS (FPD-LVDS)
- Digital Encoder (DENC)
- Digital Video VIP
- 2D graphics block.

3.2 Audio Subsystem

Refer to [Figure 7-11](#) for the main audio interfaces for the PNX8543 and the audio signal flow between blocks and memory.



18440_204_090226.eps
090226

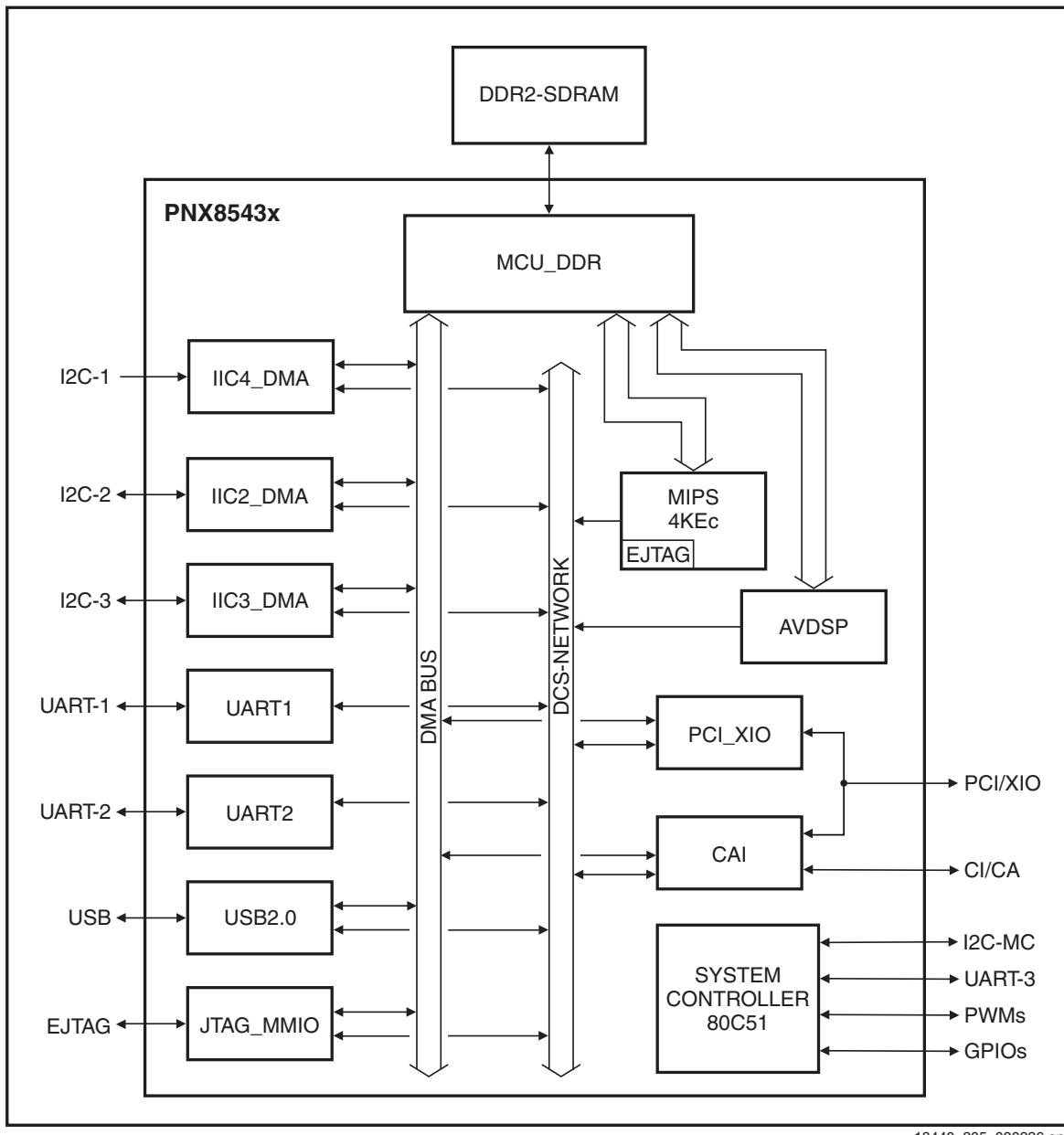
Figure 7-11 PNX8543 audio flow diagram

The Audio Subsystem consist of the following blocks:

- Analogue Audio Front End (AAFE) used to capture Baseband Audio Inputs and to sample Secondary Sound IF (SSIF) directly or via Low-IF input
- HDMI Receiver interface block
- SPDIF input block
- Audio Input (AI) block
- Audio Output (AO) block
- Demodulation & Decoding (ASDEC) DSP for decoding all analogue terrestrial TV sound standards
- Audio Post-Processing (APP) block
- Digital Audio decoder.

Connectivity and Compute Subsystem

Refer to [Figure 7-12](#) for the connectivity and compute subsystem.



18440_205_090226.eps
090226

Figure 7-12 PNX8543 connectivity and compute subsystem

The Connectivity Subsystem consists of:

- PCI/XIO interface
- USB2.0 interface
- Three 2-wire UARTs
- Four Master/Slave I²C interfaces
- Common Interface/Conditional Access Interface.

The Computing Subsystem consists of:

- 32-bit MIPS RISC core
- Enhanced JTAG (EJTAG) block inside the MIPS
- JTAG_MMIO blocks
- TV controller
- Audio/Video DSP (AV_DSP)
- Memory Control Unit (MCU).

7.6.4 Service Notice - FLASH RAM / PNX8543 exchange

The FLASH RAM (item 7M00) and/or PNX8543 (item 7600) can only be exchanged by an authorised central workshop with dedicated programming tools. Due to the presence of (Cl+) keys in the components, **unauthorised exchange of these components will always result in a defective board**.

7.7 Common Interface Cl+

Together with this platform, an extension to the Common Interface (CI) Conditional Access system is added, called CI+.

CI+ or Common Interface Plus is a specification that extends the Common Interface (DVB-CI) as described in the digital broadcasting standard DVB.

The weakness of the conventional CI module used in a Conditional Access system was the absence of a Copy Protection mechanism, as decrypted content could be sent over the PCMCIA interface unscrambled. With the CI+ extension, a form of copy protection is established between the Conditional Access Module (CAM) and the Integrated Digital Television (IDTV). The security mechanisms in CI+ are derived/copied from POD (with the exception of Out Of Band (OOB) used in US CA systems). For more information about conventional CA systems using a CI module, refer to the BJ3.0E L/PA or BL2.xU Service Manual.

The CI+ standard is downwards compatible with the existing CI standard.

The following figure shows the implementation of the CI+ Conditional Access system in the TV543 platform.

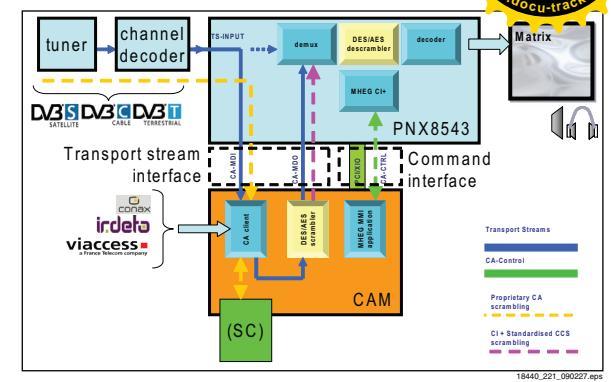


Figure 7-13 CI+ Conditional Access implementation

7.8 Ambi Light

The Ambi Light architecture in this platform has been entirely renewed. The characteristics are:

- Additional DC/DC board generating 12/16/24 V (optional)
- ARM processor (on DC/DC panel or AL board)
- Low-power LEDs
- SPI interface from ARM to LED drivers
- I²C upgradeable via USB
- Each AL module has a temperature sensor.

The use of the DC/DC board is optional. In case no DC/DC board is implemented, the ARM processor is located on one of the AL boards.

Refer to [Figure 7-14](#) for the Ambi Light architecture.

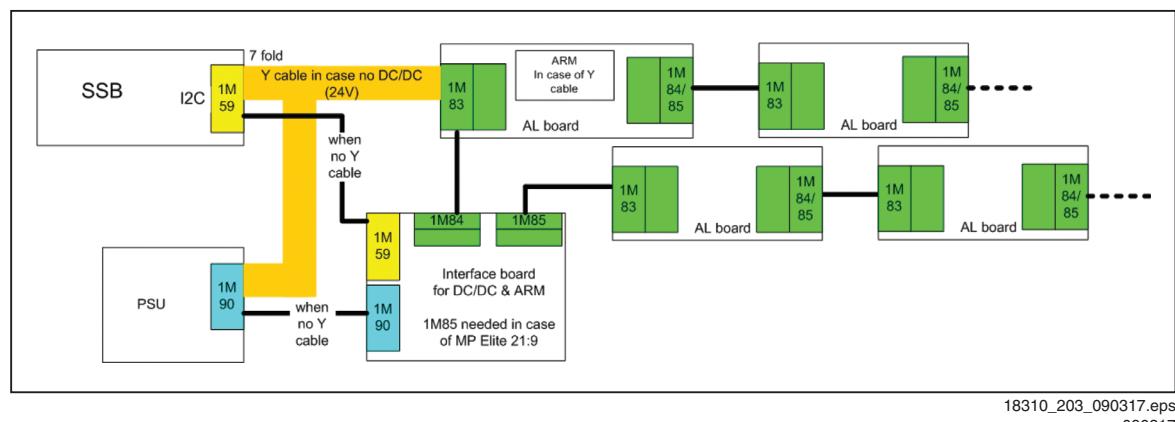


Figure 7-14 Interface between Ambi Light and SSB

7.8.1 ARM controller

Refer to [Figure 7-15](#) below for signal interfacing to and from the ARM controller. The ARM controller is located on the DC/DC board (item no. 7302) or AL panel (item no. 7102).

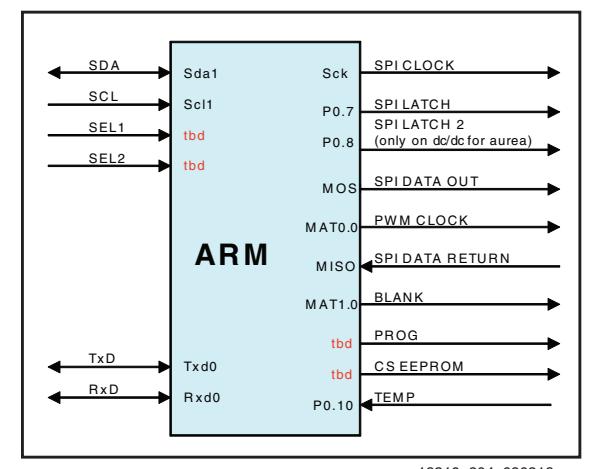


Figure 7-15 ARM controller interface

Data transfer between ARM processor and LED drivers is executed by a Serial Peripheral Interface (SPI) bus interface.

SPI bus is a synchronous serial data link standard that operates in full duplex mode.

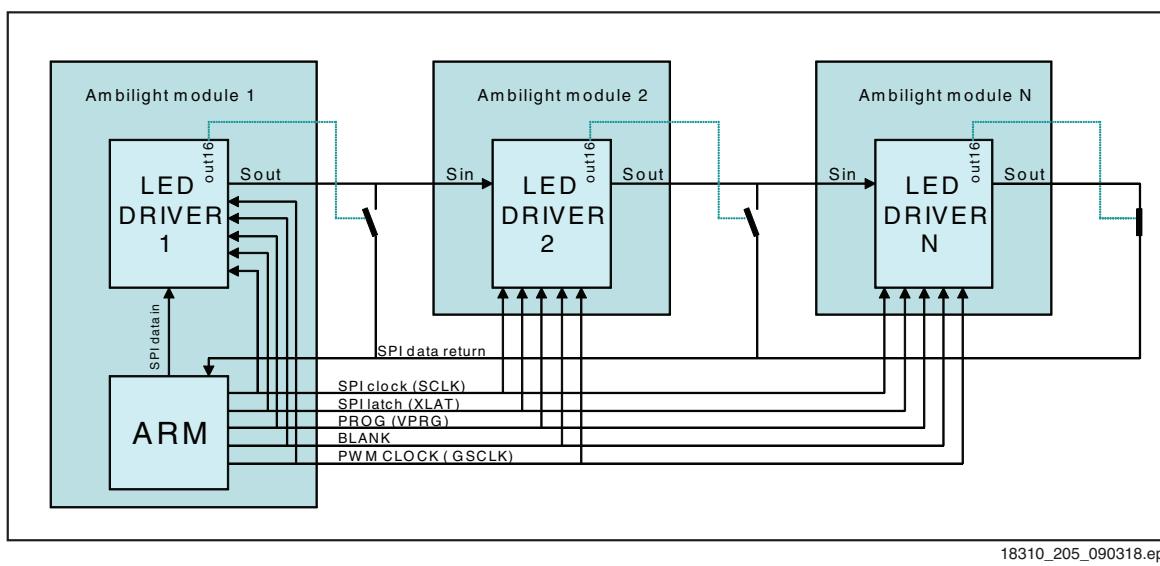
For debugging purposes, the working principle is given below:

- At startup the controller will read-out matrix data from the EEPROM devices (via SPI DATA RETURN)
- Before operation, the driver current is set via SPI, with driver in DC mode
- During normal operation the controller receives RGB-, configuration-, operation mode- and topology data via I²C
- The controller converts the I²C RGB data via the matrixes to SPI LED data
- Via data return the controller receives error data (if applicable).

Also PWM clock and BLANK signals are generated by the controller. The controller can be reprogrammed via I²C (via USB). The controller can receive matrix values via I²C, which will be stored in the EEPROM of each AL module via the SPI bus. The temperature sensor in each AL module controls the TEMP line; in case of a too high temperature the controller will reduce the overall brightness.

7.8.2 LED driver communication (via SPI bus)

Refer to [Figure 7-16](#) below for signal interfacing between the ARM controller and the LED drivers on the AL boards, and the LED drivers and the EEPROMs on the AL boards.



18310_205_090318.eps
090318

Figure 7-16 SPI communication between ARM controller and LED drivers

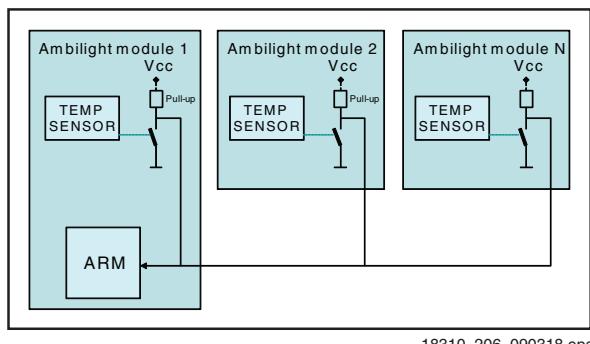
The ARM controller communicates with the LED drivers (on each AL module) via an SPI bus. For debugging purposes, the working principle is given below:

- Data from the ARM controller is linked through the drivers, which are connected in cascade
- SPI CLK, SPI LATCH, PROG, BLANK and PWM CLOCK are going directly from the controller to each driver
- SPI DATA RETURN is linked from the last driver to the controller: controller decides which driver returns data.

Each AL board is equipped with a temperature sensor. If one of the sensors detects a temperature over the threshold, the TEMP line is pulled LOW which results in brightness reduction.

7.8.3 Temperature Control

Refer to [Figure 7-17](#) for signal interfacing between the ARM controller and the temperature sensor on the AL boards.



18310_206_090318.eps
090318

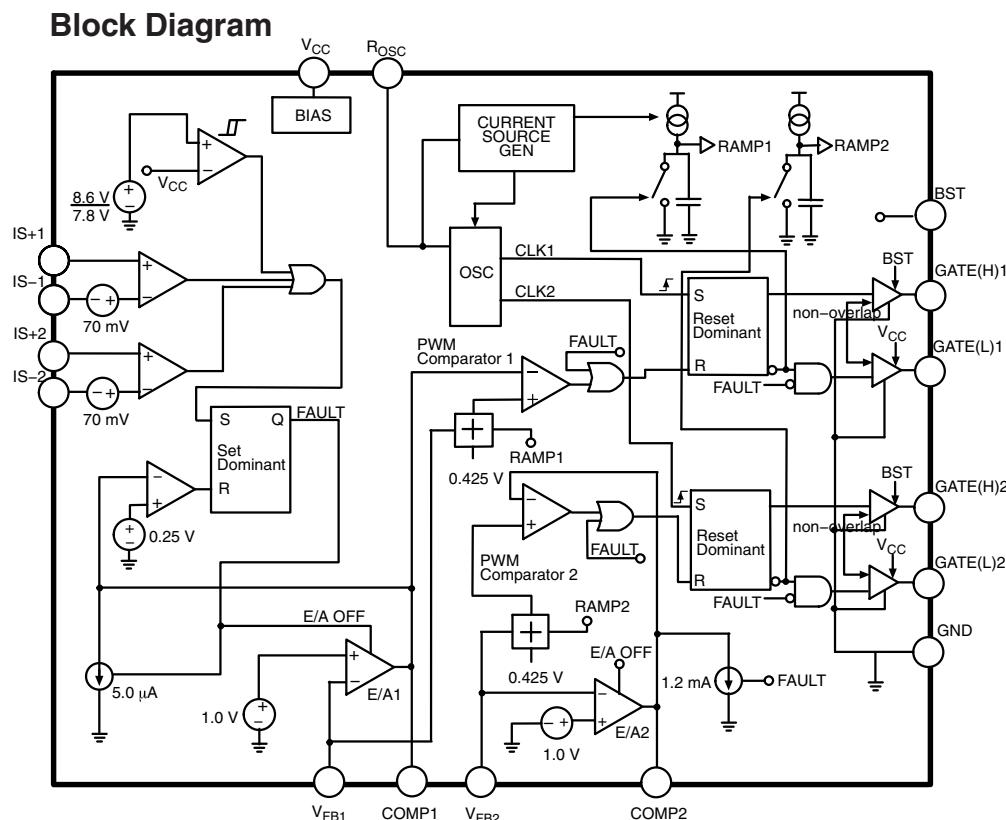
Figure 7-17 Communication between ARM controller and temperature sensor

5. IC Data Sheets

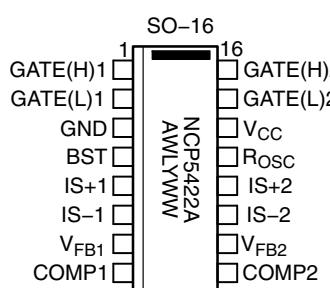
This chapter shows the internal block diagrams and pin configurations of ICs that are drawn as “black boxes” in the

electrical diagrams (with the exception of “memory” and “logic” ICs).

8.1 Diagram SSB: DC/DC +3V3 +1V2 B01A, NCP5422AD (IC 7103)



Pin Configuration



A = Assembly Location

WL = Wafer Lot

Y = Year

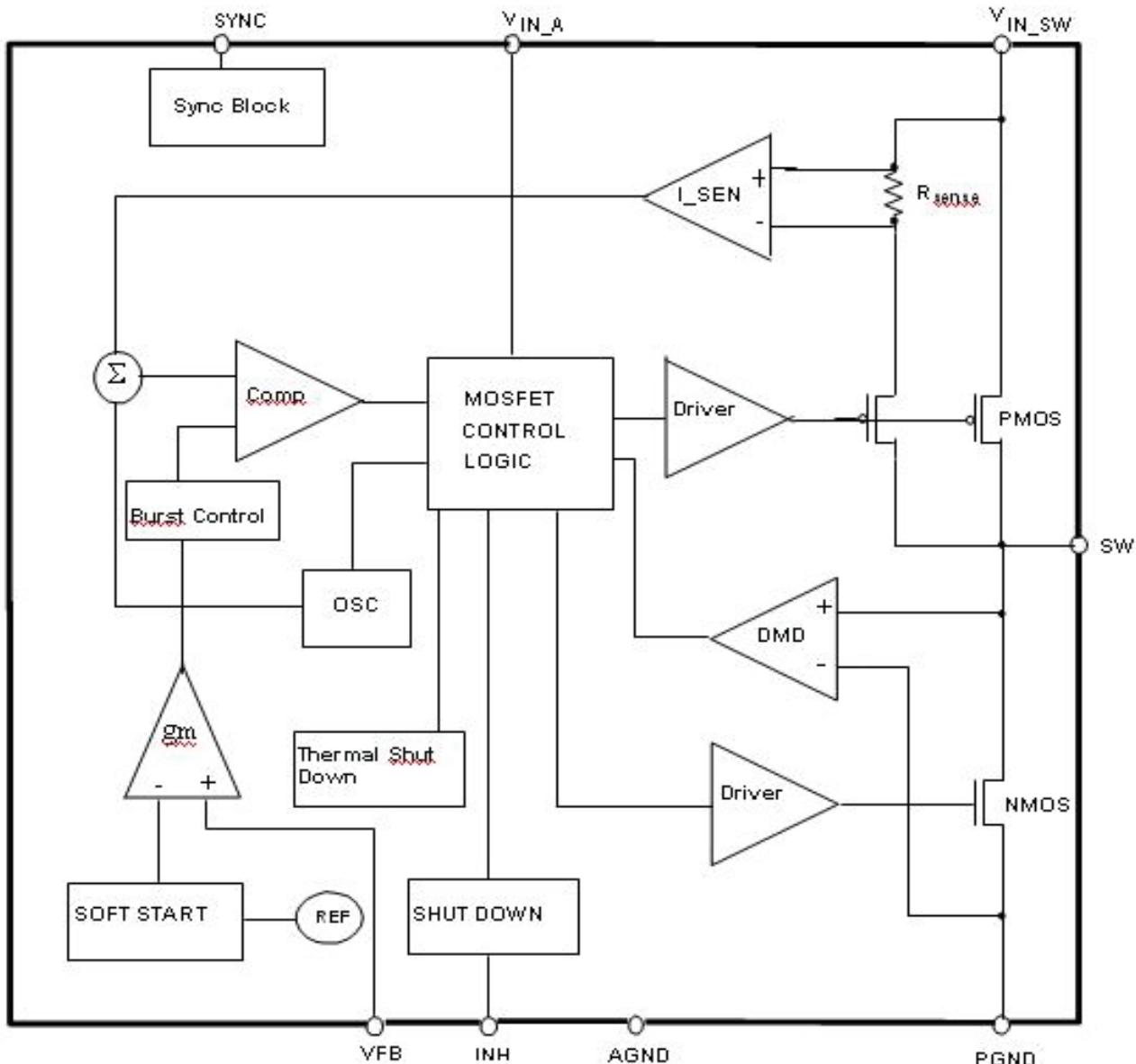
WW = Work Week

F_15400_129.eps
240505

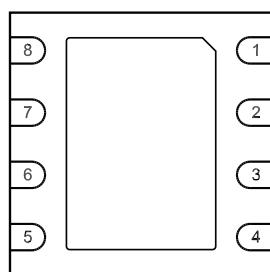
Figure 8-1 Internal block diagram and pin configuration

Program SSB: DC/DC +3V3 +1V2 Standby B01B, ST1S10PH (IC 7202/7222)

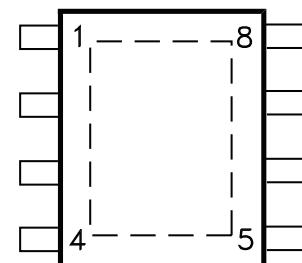
Block Diagram



Pin Configuration



DFN8 (4x4)



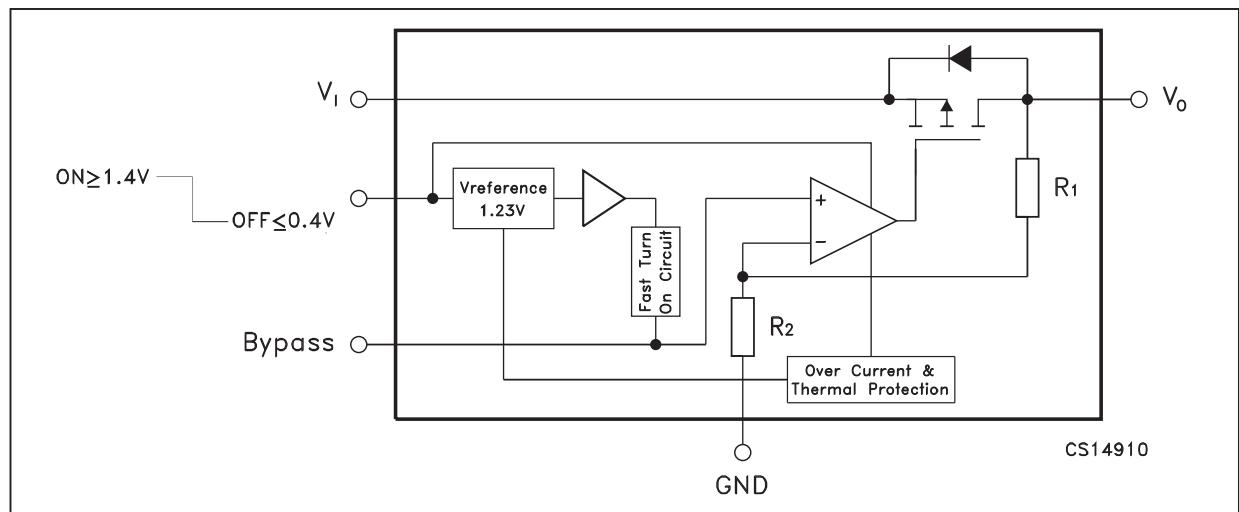
PowerSO-8

I_18010_083.eps
130608

Figure 8-2 Internal block diagram and pin configuration

Diagram SSB: DC/DC +3V3 +1V2 Standby B01B, LD3985M (IC 7201)

Block Diagram



Pin Configuration

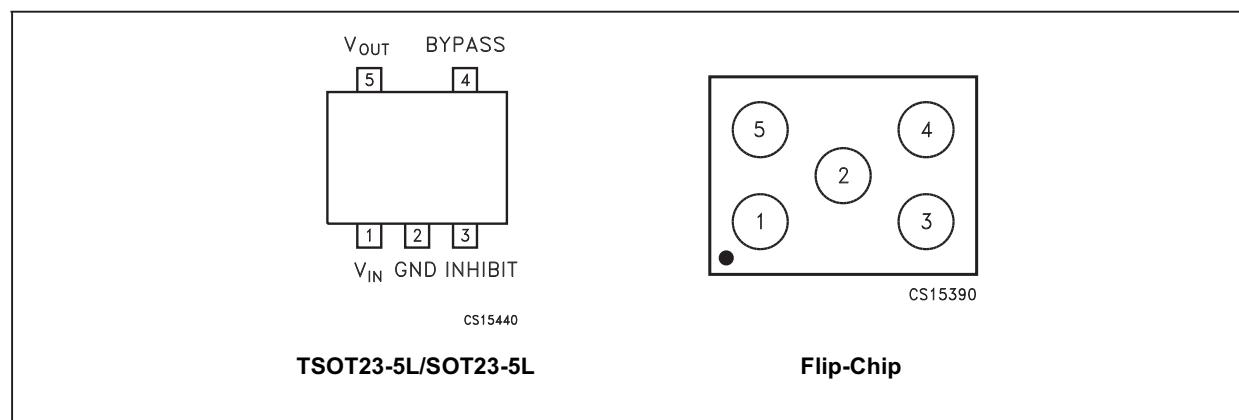
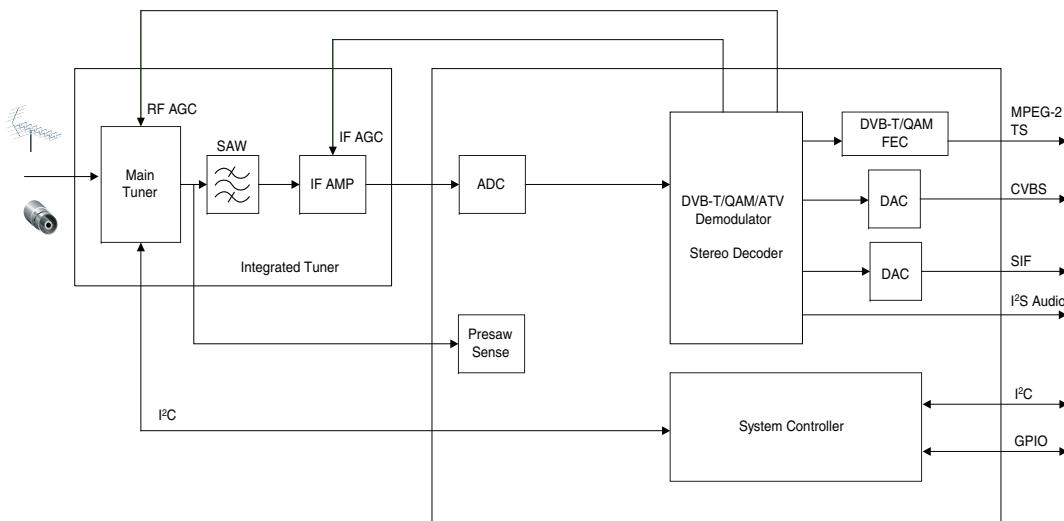
G_16290_084.eps
020206

Figure 8-3 Internal block diagram and pin configuration

Program SSB: Front End B02A, DRX3926K (IC 7303)

Block Diagram



Pin Configuration

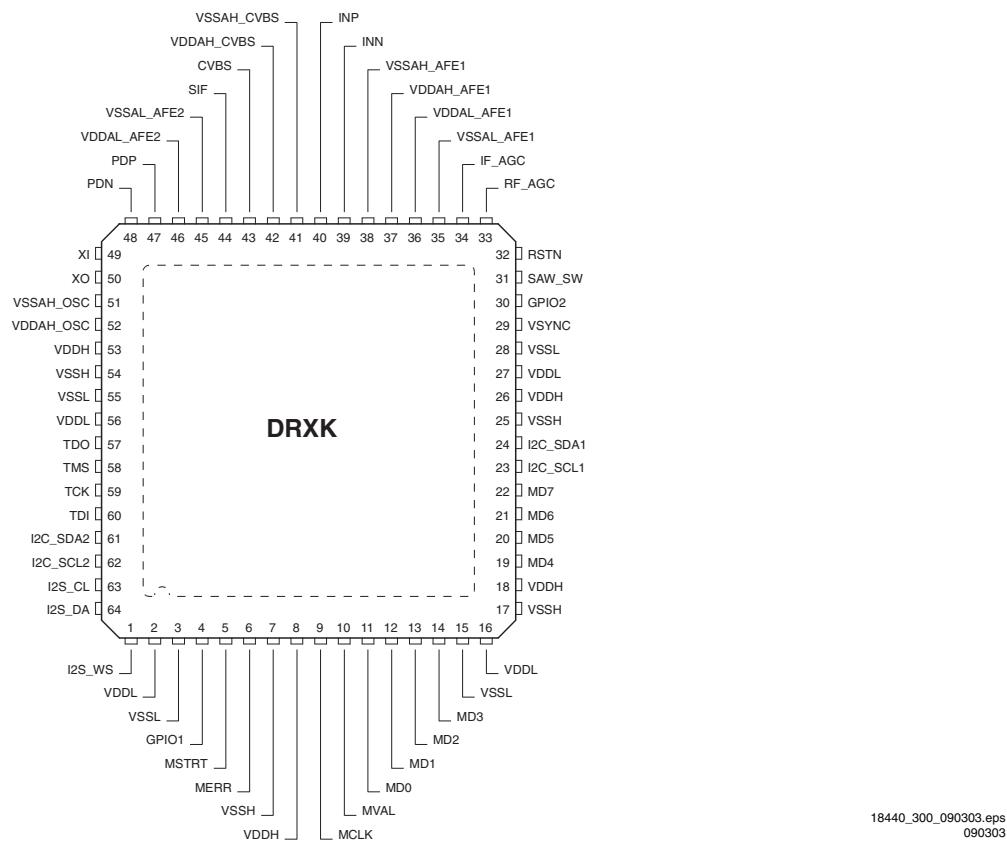
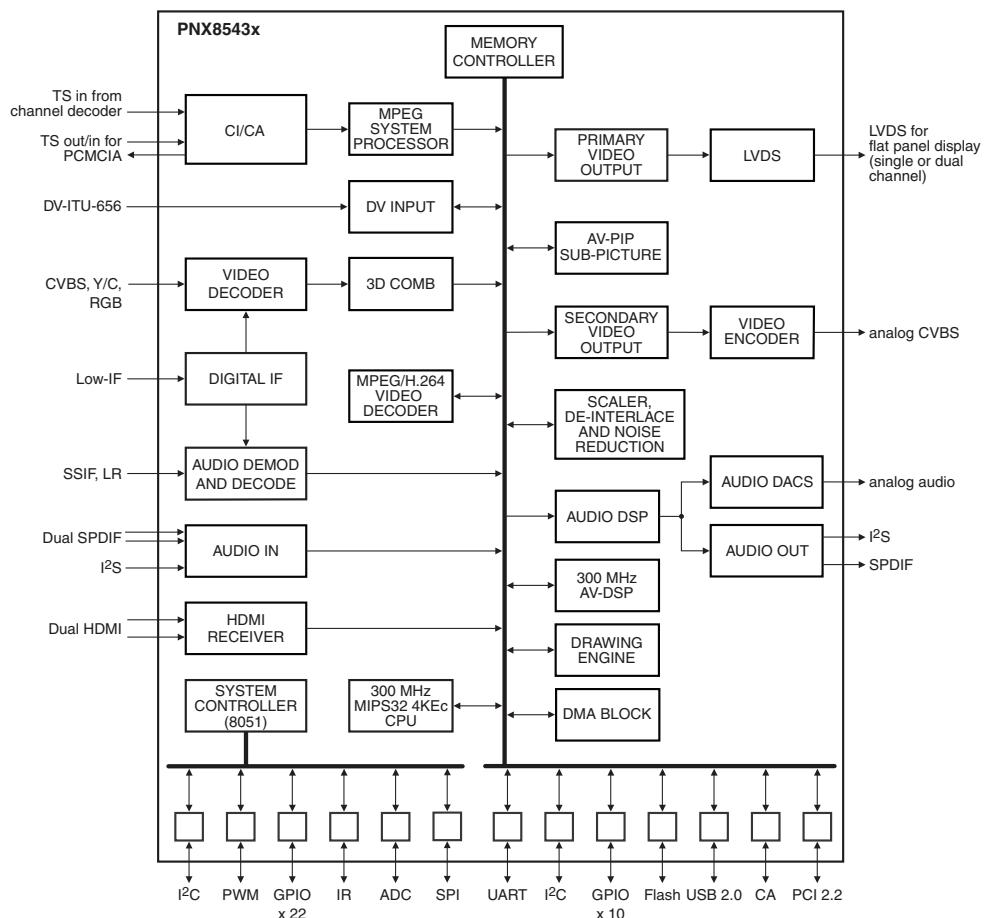


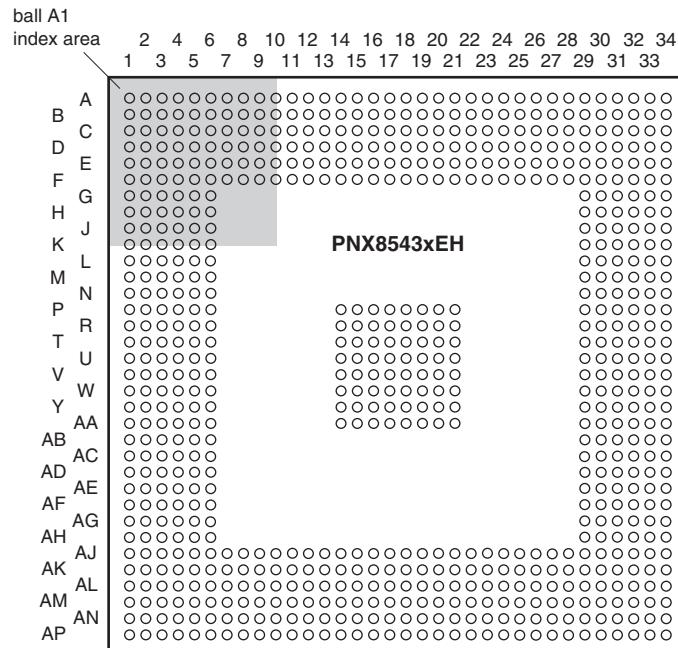
Figure 8-4 Pin configuration

Diagram SSB: PNX8543 - Power B03A-B03H, PNX8543 (IC7600)

Block Diagram



Pin Configuration

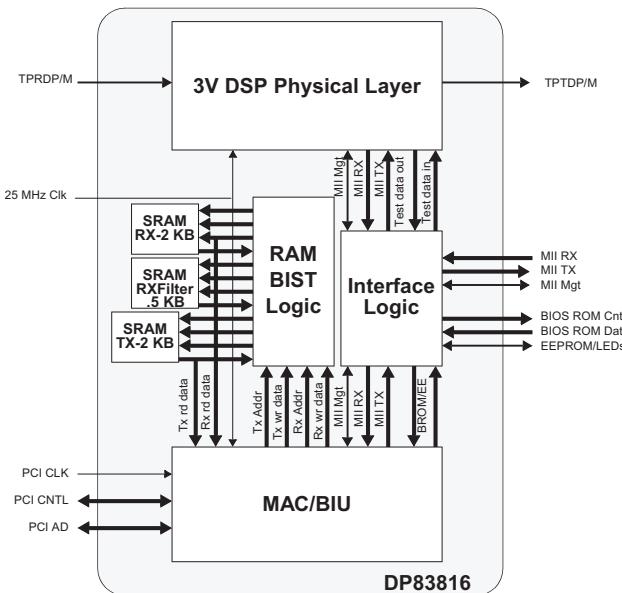


18440_301_090303.eps
090303

Figure 8-5 Internal block diagram and pin configuration

Program SSB: Ethernet B05B, DP83816 (IC7N04)

Block Diagram



Pin Configuration

Pin No.	Pin Name
36	NC
37	VSS
38	IAUXVDD
39	VREF
40	RESERVED
41	NC
42	NC
43	VSS
44	NC
45	TPRDIM
46	TPTDP
47	IAUXVDD
48	REGEN
49	VSS
50	RESERVED
51	VSS
52	TPTDM
53	TPTDP
54	VSS
55	AUXVDD
56	VSS
57	AUXVDD
58	PMEN/CCLKRUNN
59	PCICLK
60	INTA
61	RSTN
62	GNTN
63	REGDN
64	VSS
65	AD31
66	AD30
67	AD29
68	AD28
69	PCI/VDD
70	AD27
71	AD26
72	PCI AD
73	AD25
74	AD24
75	CBEIN3
76	IDSEL
77	IDSEL
78	AD23
79	AD22
80	PCI/VDD
81	AD21
82	AD20
83	AD19
84	NC
85	NC
86	AD18
87	AD17
88	AD16
89	CBEN2
90	VSS
91	FRAHEN
92	IRDYN
93	TCIN
94	PCI/VDD
95	DEVSLEN
96	STOPN
97	PEIRRN
98	SERIRN
99	CBEN1
100	AD15
101	AD14
102	AD13
103	AD12
104	AD11
105	AD10
106	PCI/VDD
107	AD10
108	AD9
144	MA2/LED100N
143	MA1/LED10N
142	MA1/LEDACTN
141	MD7
140	MD6
139	MD5
138	MD4/EEDO
137	MD3/ADXVDD
136	VSS
135	MD2
134	MD1/CFGDISN
133	MD1
132	MWRN
131	MRDN
130	MRCN
129	MCSN
128	EESL
127	RESERVED
126	NC
125	NC
124	PWRGOOD
123	AD2
122	AD1
121	AD0
120	AD1
119	AD2
118	AD3
117	PCI/VDD
116	AD4
115	AD5
114	VSS
113	AD6
112	AD7
111	CRBN0
110	AD8
109	AD9

DP83816

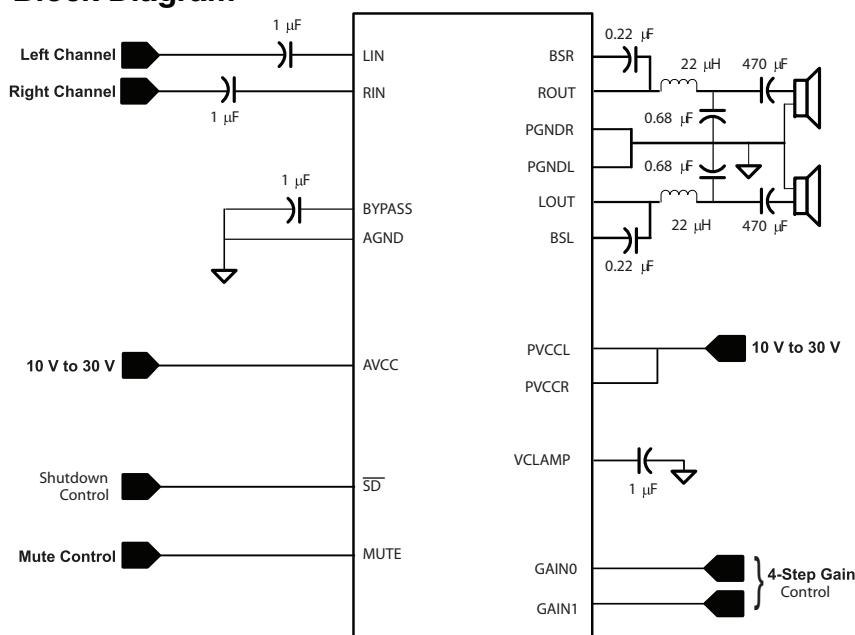
Pin Identification

F_15710_167.eps
230905

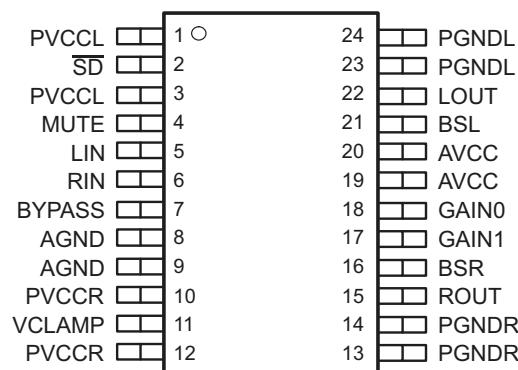
Figure 8-6 Internal block diagram and pin configuration

Diagram SSB: Class-D B06A, TPA3123D (IC 7L10)

Block Diagram



Pin Configuration

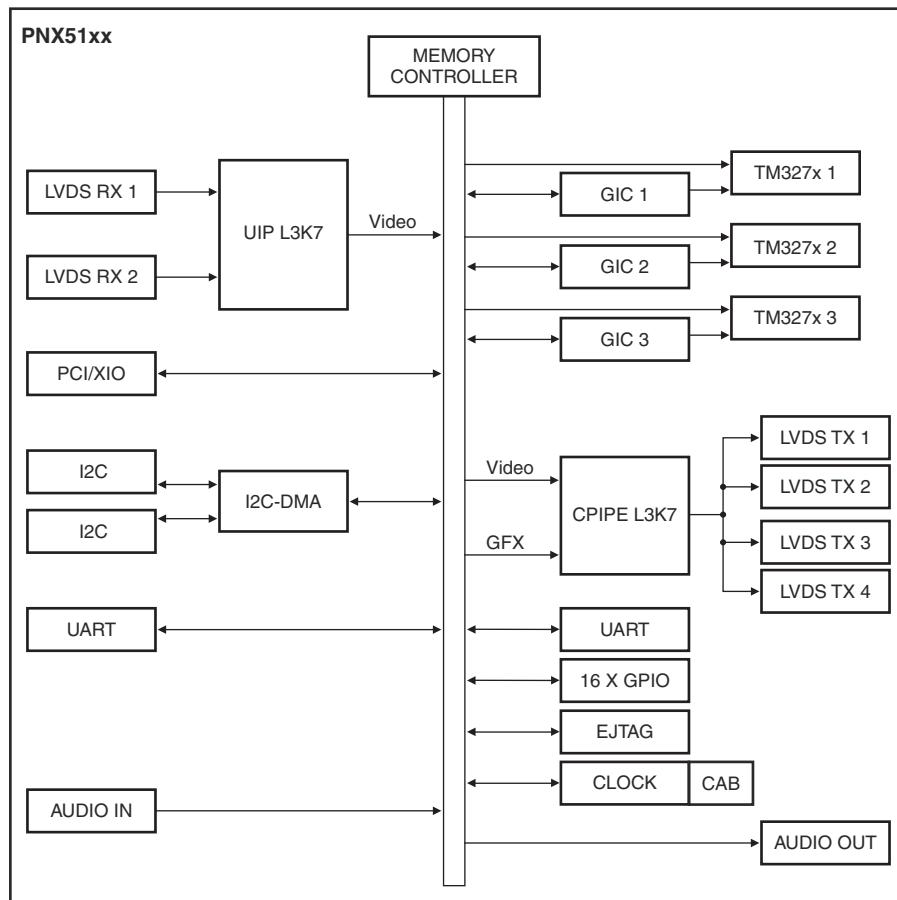


TERMINAL	NAME	24-PIN (PWP)	I/O/P	DESCRIPTION
	SD	2	I	Shutdown signal for IC (low = disabled, high = operational). TTL logic levels with compliance to AVCC
	RIN	6	I	Audio input for right channel
	LIN	5	I	Audio input for left channel
	GAIN0	18	I	Gain select least-significant bit. TTL logic levels with compliance to AVCC
	GAIN1	17	I	Gain select most-significant bit. TTL logic levels with compliance to AVCC
	MUTE	4	I	Mute signal for quick disable/enable of outputs (high = outputs switch at 50% duty cycle, low = outputs enabled). TTL logic levels with compliance to AVCC
	BSL	21	I/O	Bootstrap I/O for left channel
	PVCLL	1, 3	P	Power supply for left-channel H-bridge, not internally connected to PVCCR or AVCC
	LOUT	22	O	Class-D 1/2-H-bridge positive output for left channel
	PGNDL	23, 24	P	Power ground for left-channel H-bridge
	VCLAMP	11	P	Internally generated voltage supply for bootstrap capacitors
	BSR	16	I/O	Bootstrap I/O for right channel
	ROUT	15	O	Class-D 1/2-H-bridge negative output for right channel
	PGNDR	13, 14	P	Power ground for right-channel H-bridge.
	PVCCR	10, 12	P	Power supply for right-channel H-bridge, not connected to PVCLL or AVCC
	AGND	9	P	Analog ground for digital/analog cells in core
	AGND	8	P	Analog ground for analog cells in core
	BYPASS	7	O	Reference for preamplifier inputs. Nominally equal to AVCC/8. Also controls start-up time via external capacitor sizing.
	AVCC	19, 20	P	High-voltage analog power supply. Not internally connected to PVCCR or PVCLL
	Thermal pad	Die pad	P	Connect to ground. Thermal pad should be soldered down on all applications to properly secure device to printed wiring board.

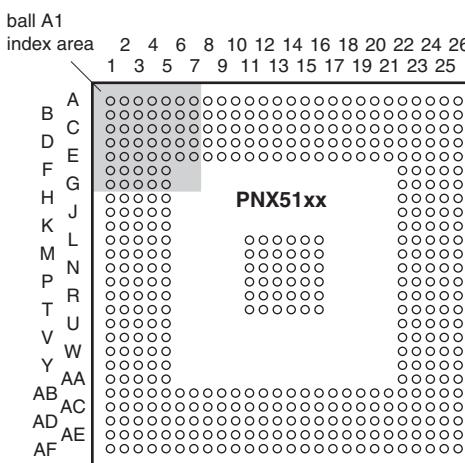
18440_302_090303.eps
090303

Figure 8-7 Internal block diagram and pin configuration

Block Diagram



Pin Configuration



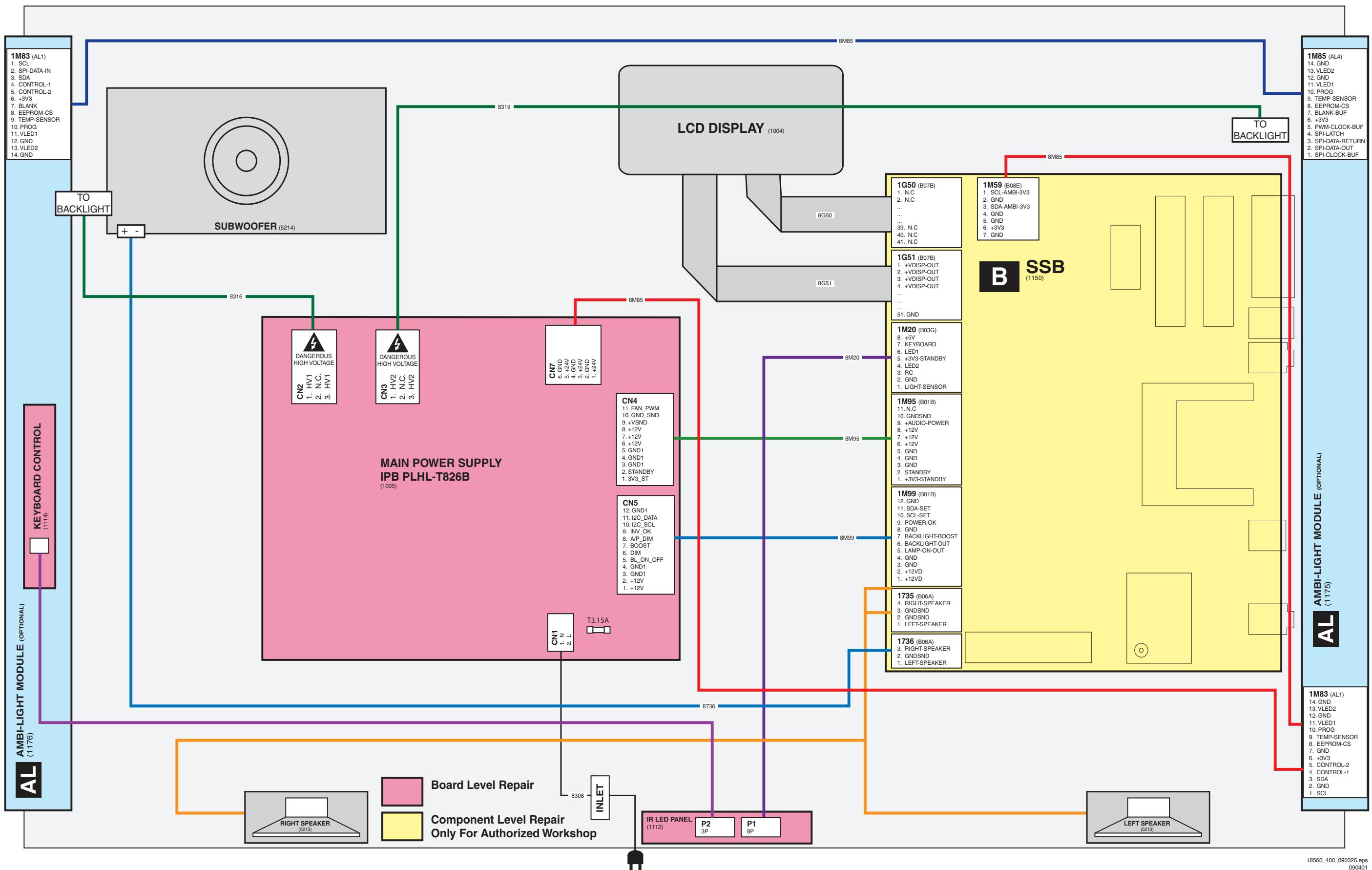
18560_300_090403.eps
090403

Figure 8-8 Internal block diagram and pin configuration

9. Block Diagrams

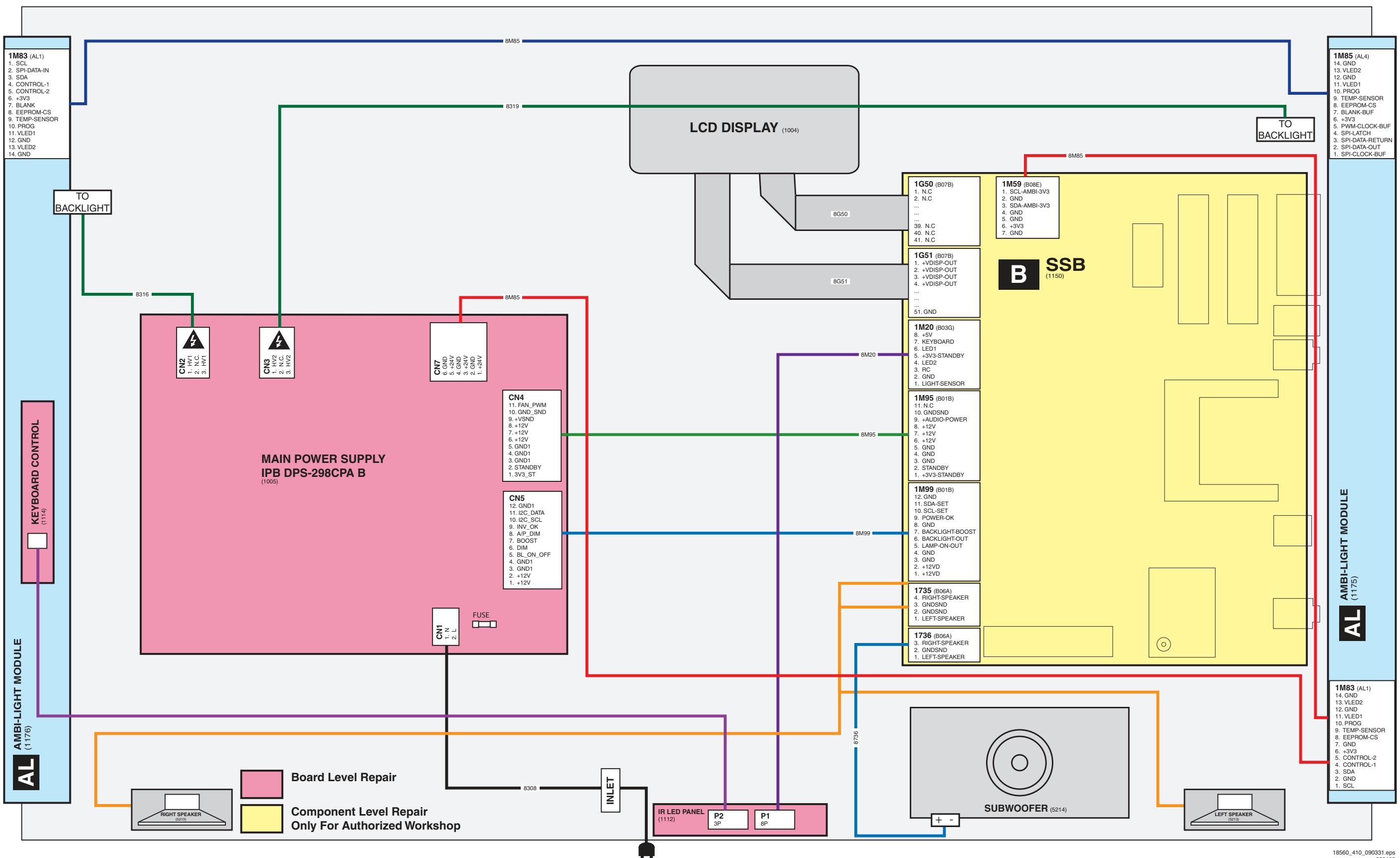
Wiring Diagram 32" (Frame)

WIRING DIAGRAM 32" (FRAME / ROADRUNNER)



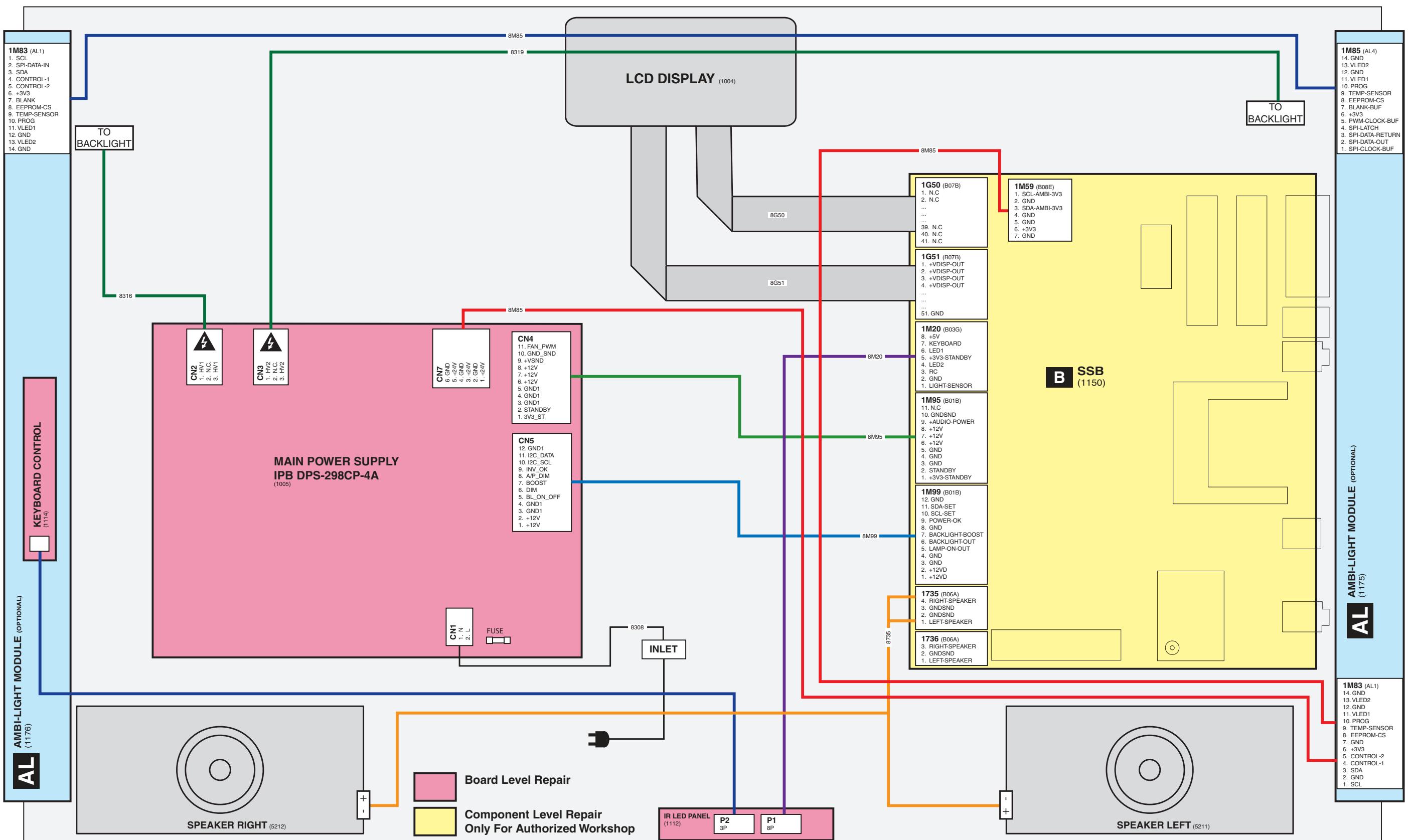
Wiring Diagram 37" (Roadrunner)

WIRING DIAGRAM 37" (ROADRUNNER)



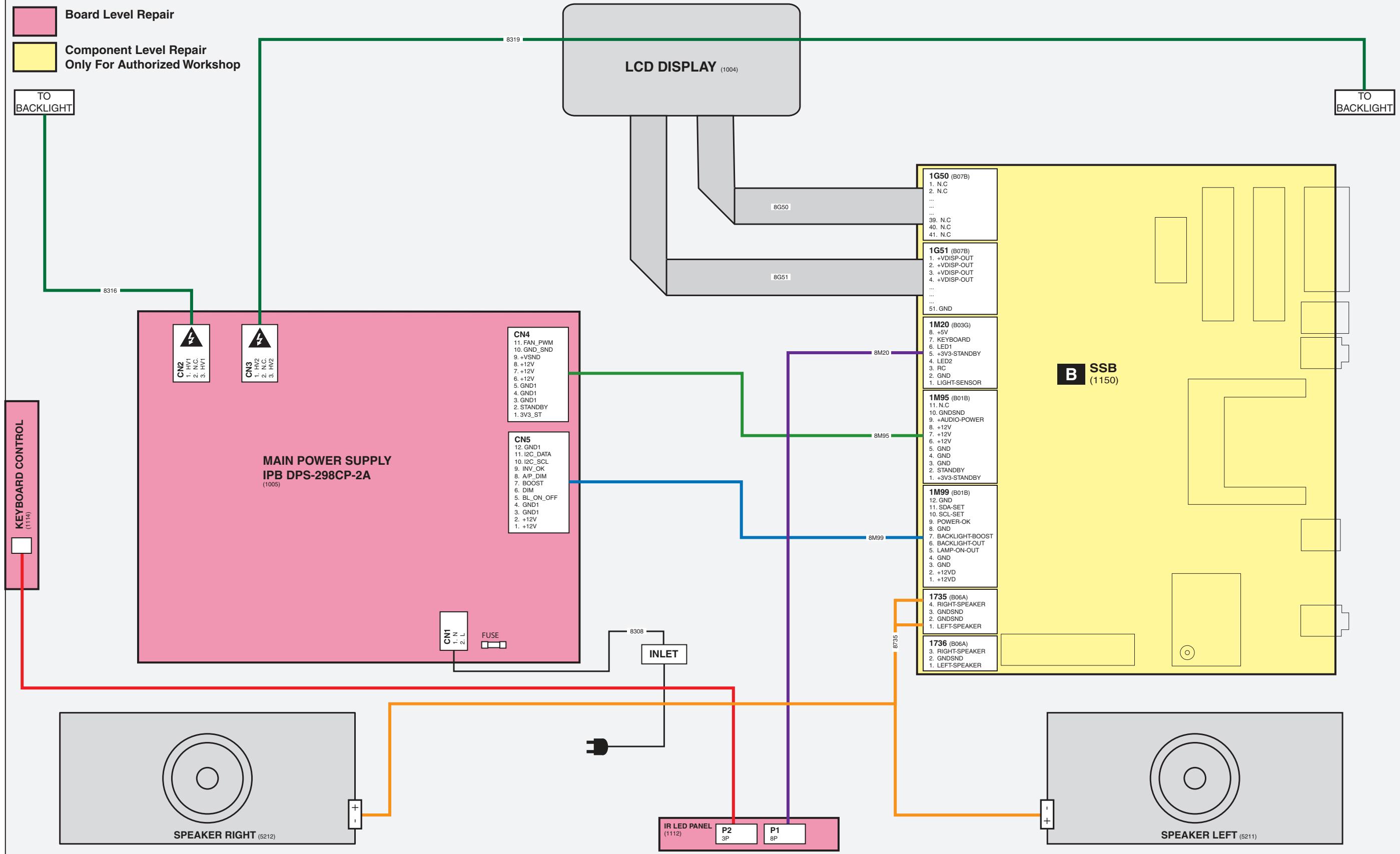
Wiring Diagram 42" (Frame/Roadrunner)

WIRING DIAGRAM 42" (FRAME / ROADRUNNER)



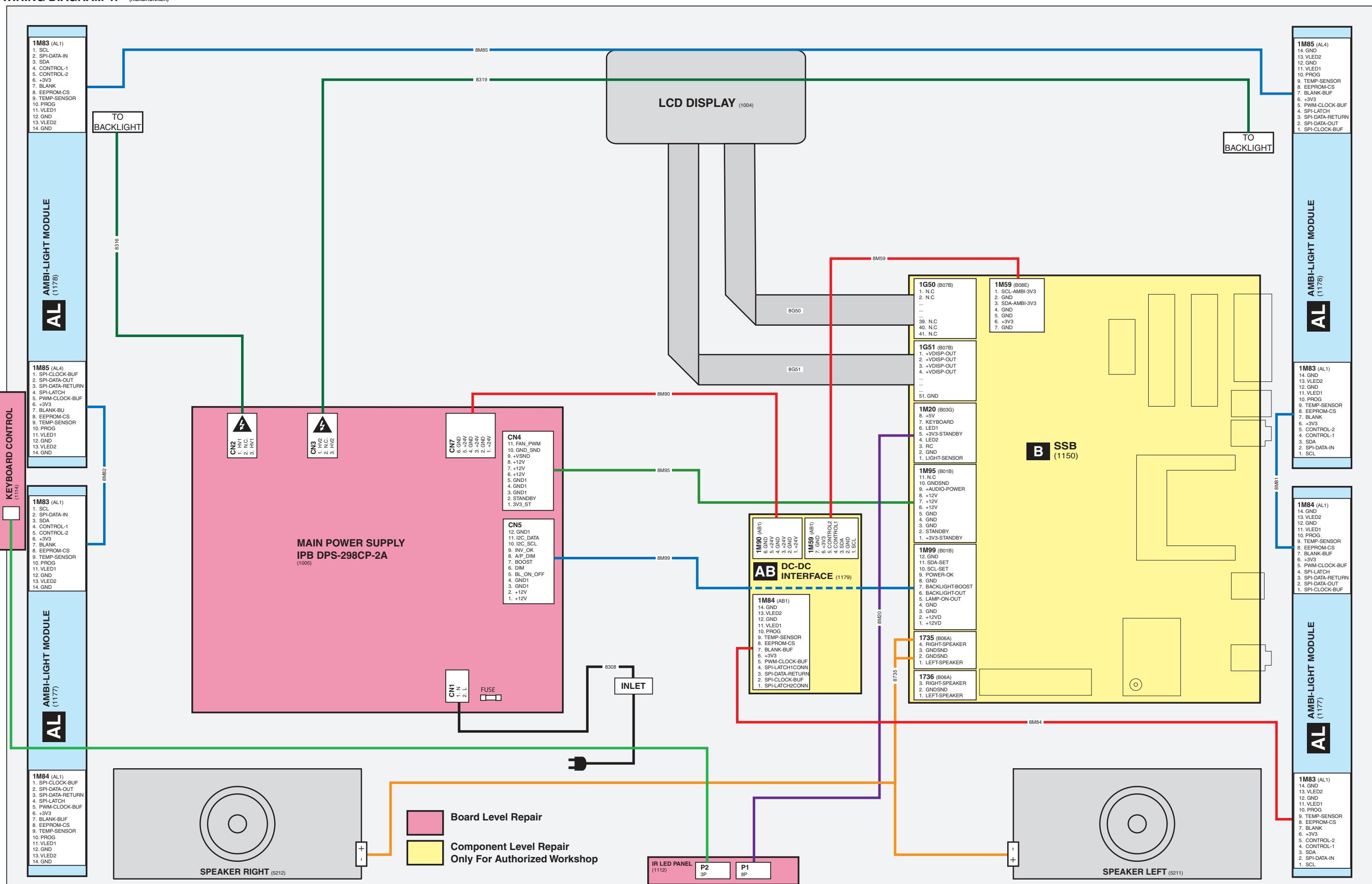
Wiring Diagram 47" (Frame)

WIRING DIAGRAM 47" (FRAME)



Wiring Diagram 47" (Roadrunner)

WIRING DIAGRAM 47" (ROADRUNNER)

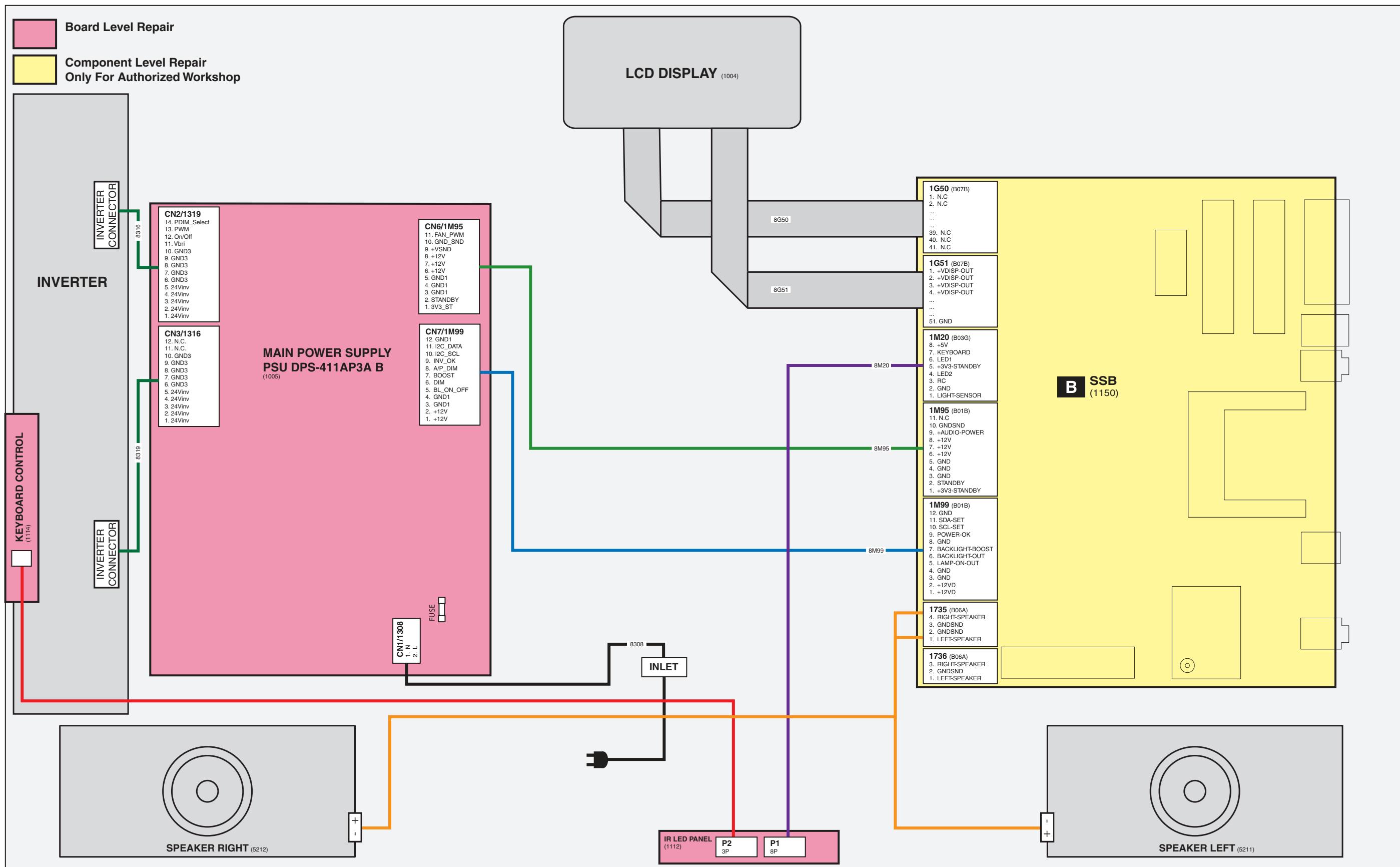


Wiring Diagram 52" (Frame)

WIRING DIAGRAM 52" (FRAME)

Board Level Repair

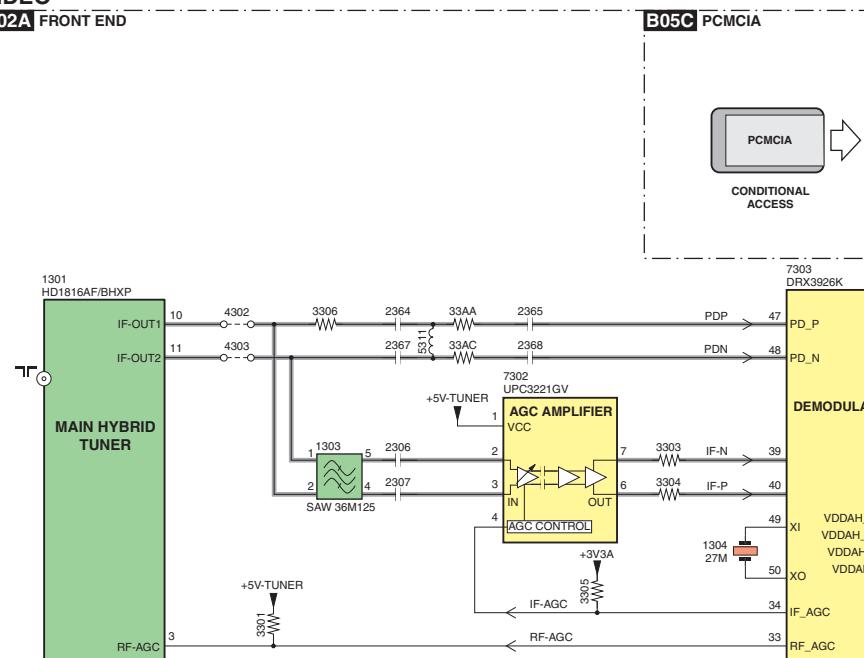
Component Level Repair
Only For Authorized Workshop



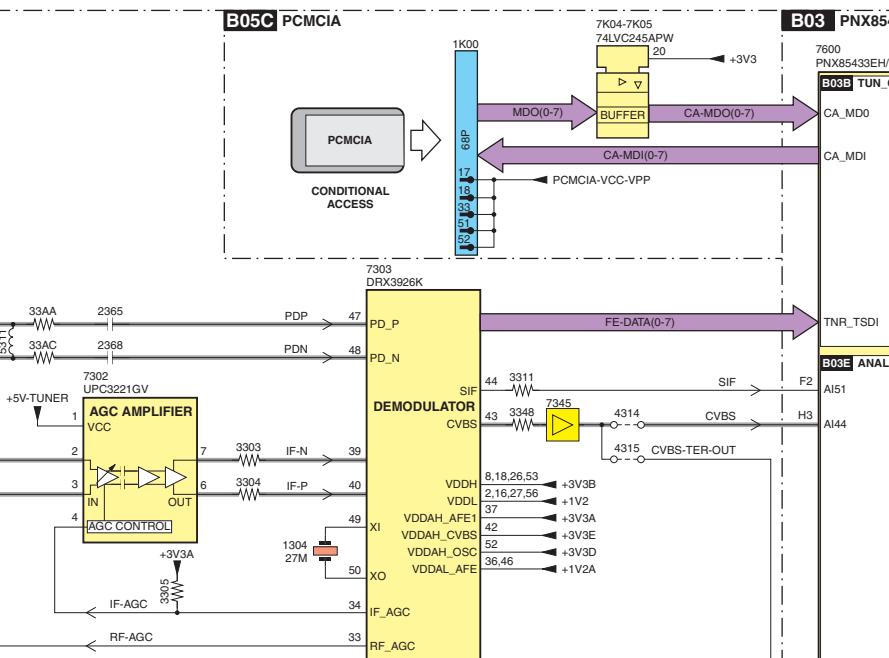
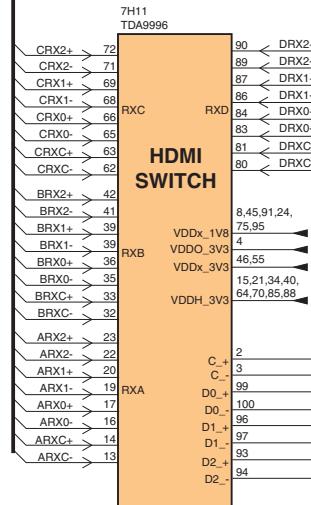
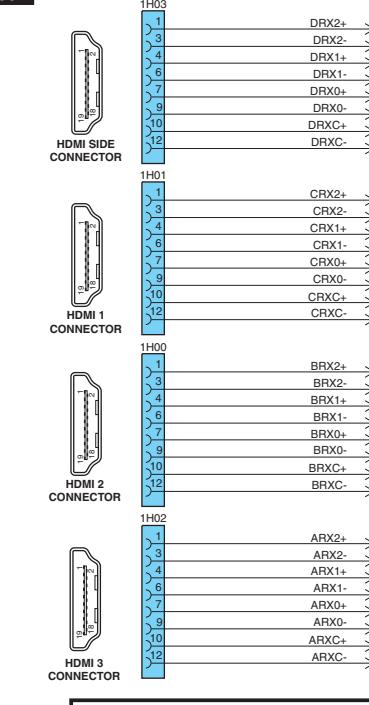
Block Diagram Video

VIDEO

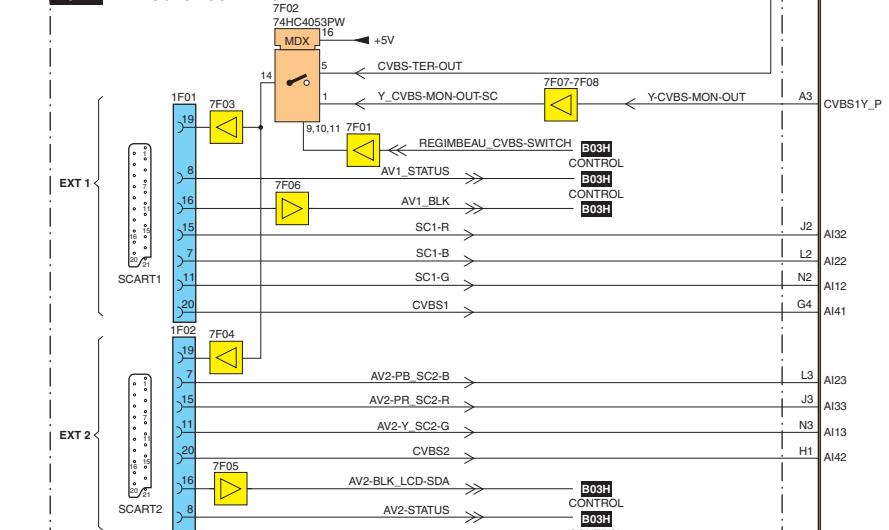
B02A FRONT END



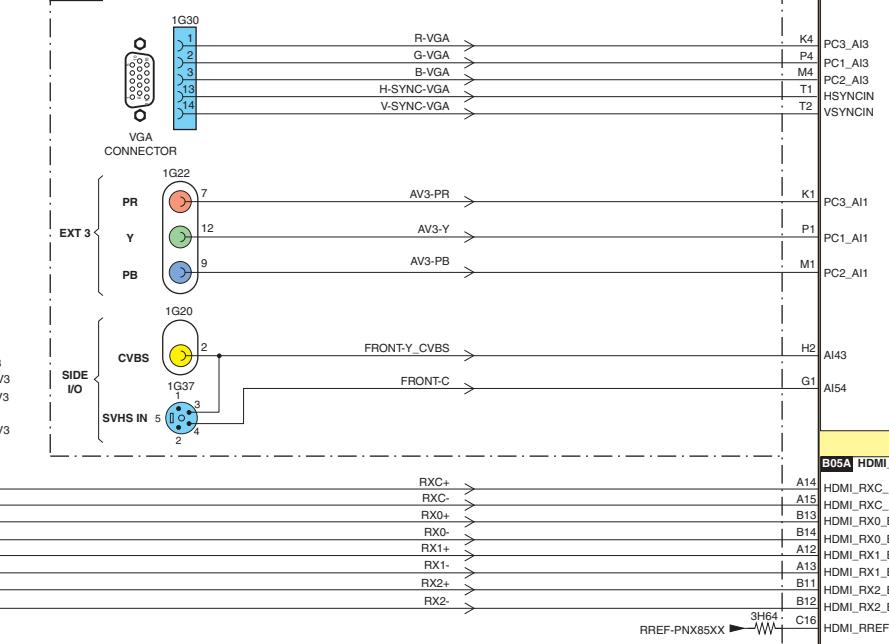
B05A HDMI



B04B ANALOG IO - SCART 1&2

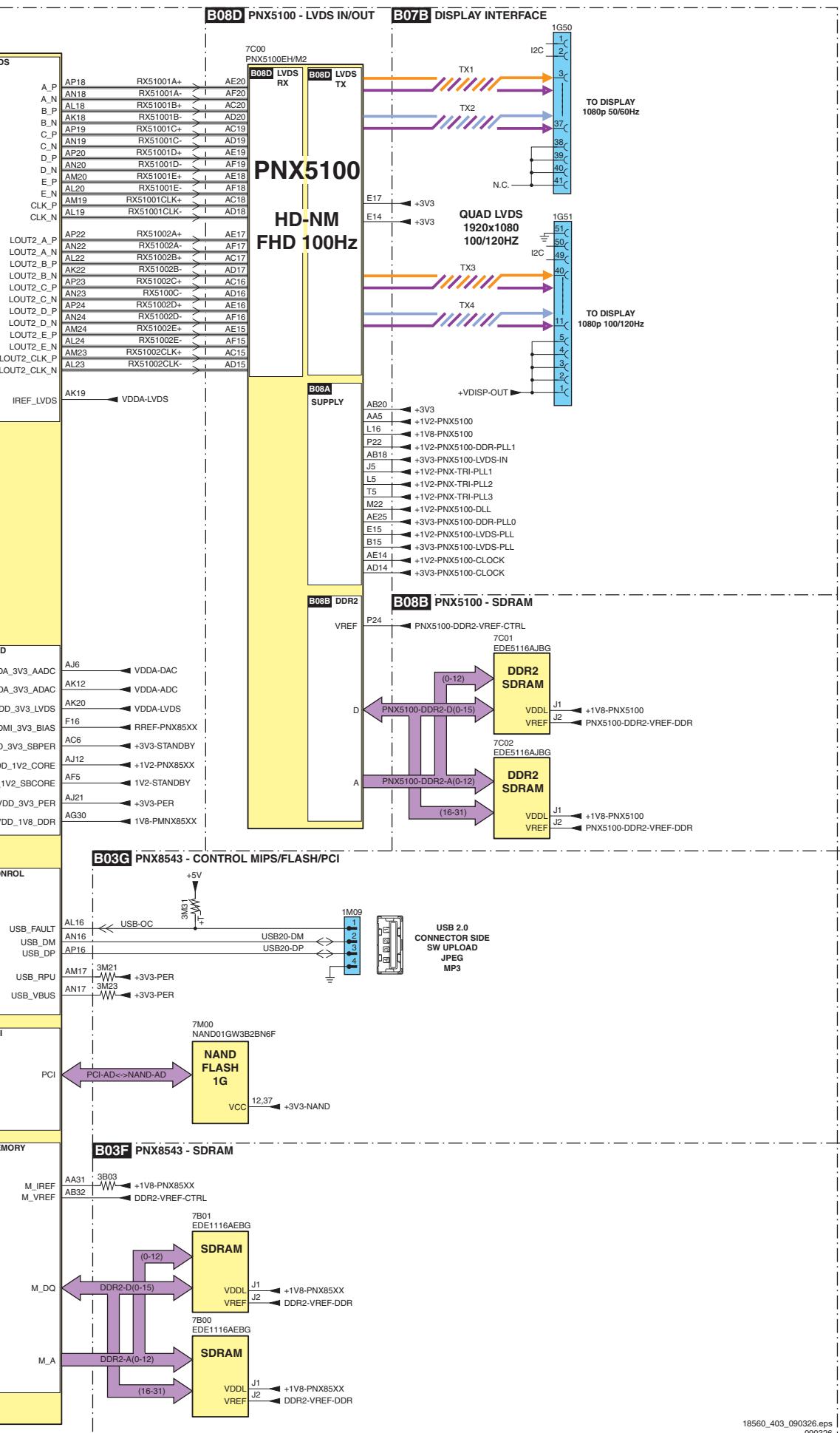
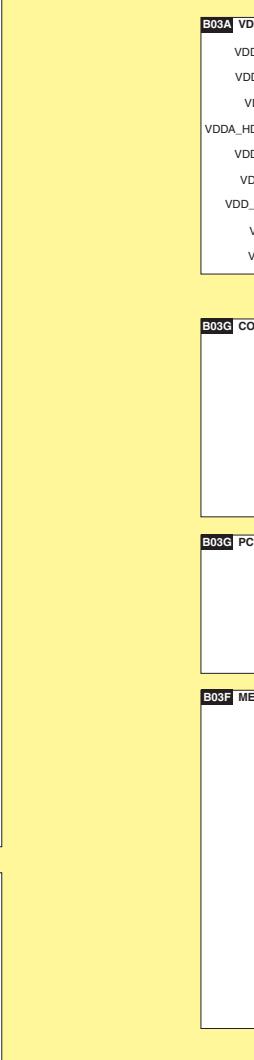


B04C YPBR / SIDE IO / S-VIDEO



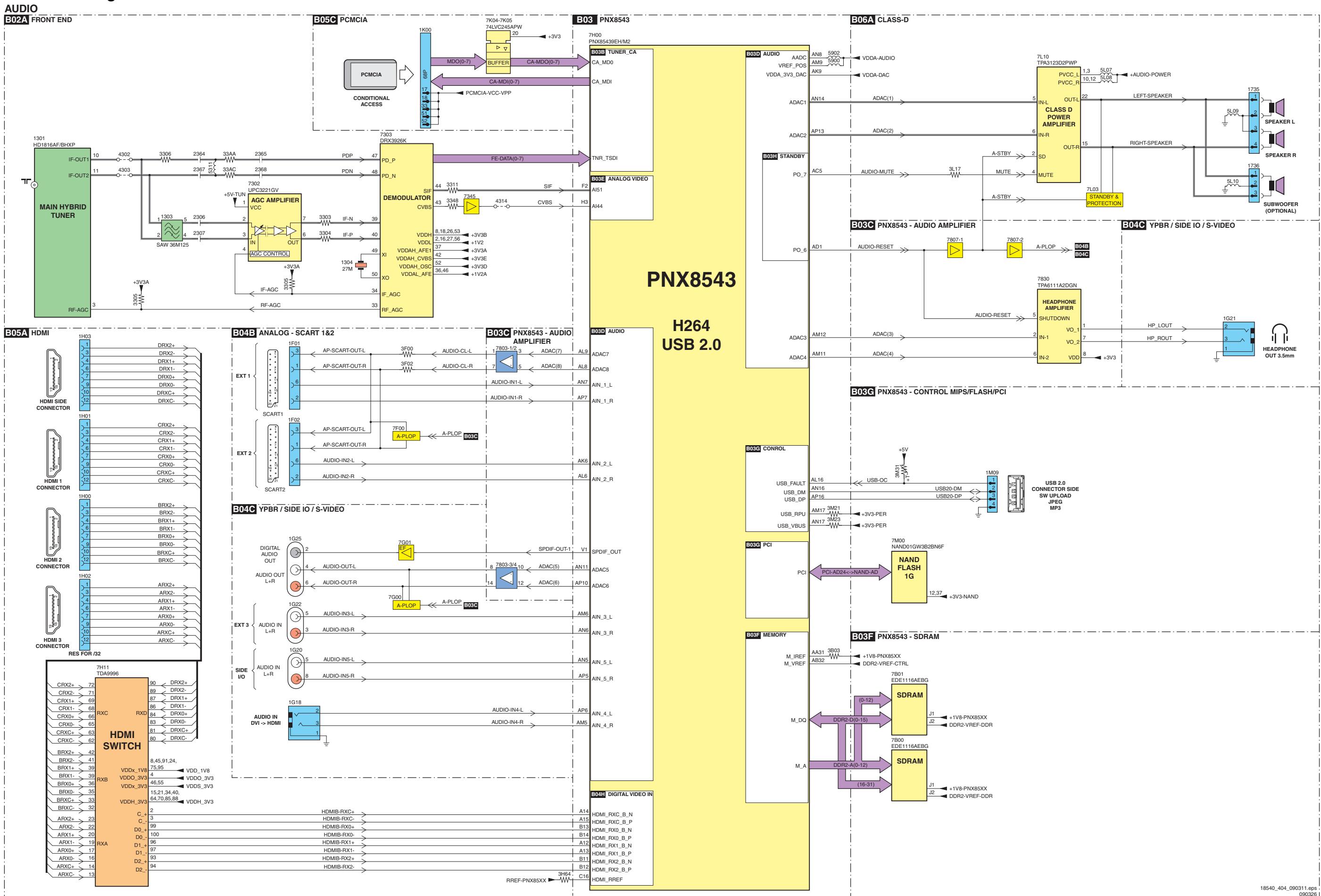
2009-Apr-03

PNX8543
H264
USB 2.0



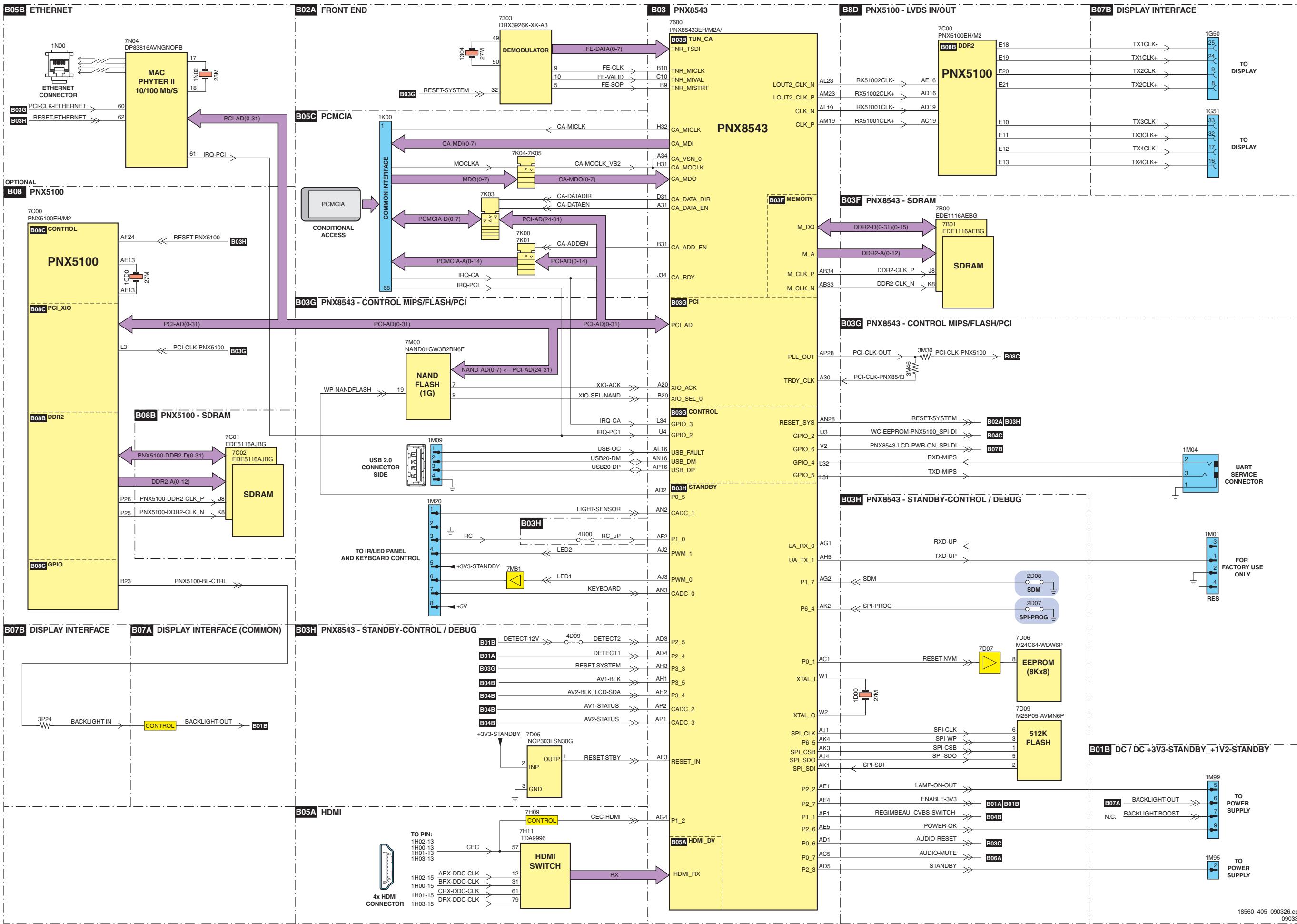
18560_403_090326.eps
090326

Block Diagram Audio

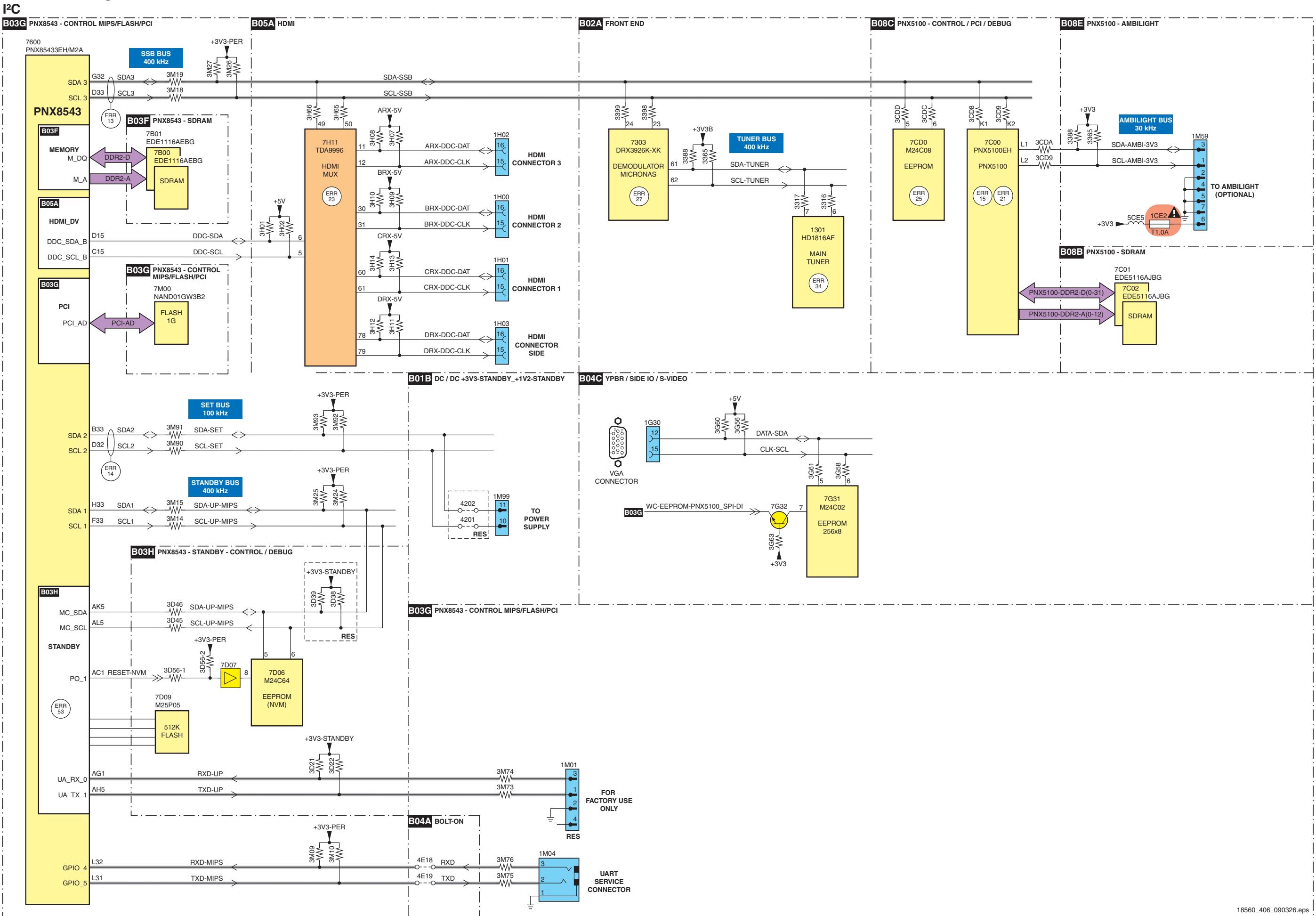


Block Diagram Control & Clock Signals

CONTROL + CLOCK SIGNALS

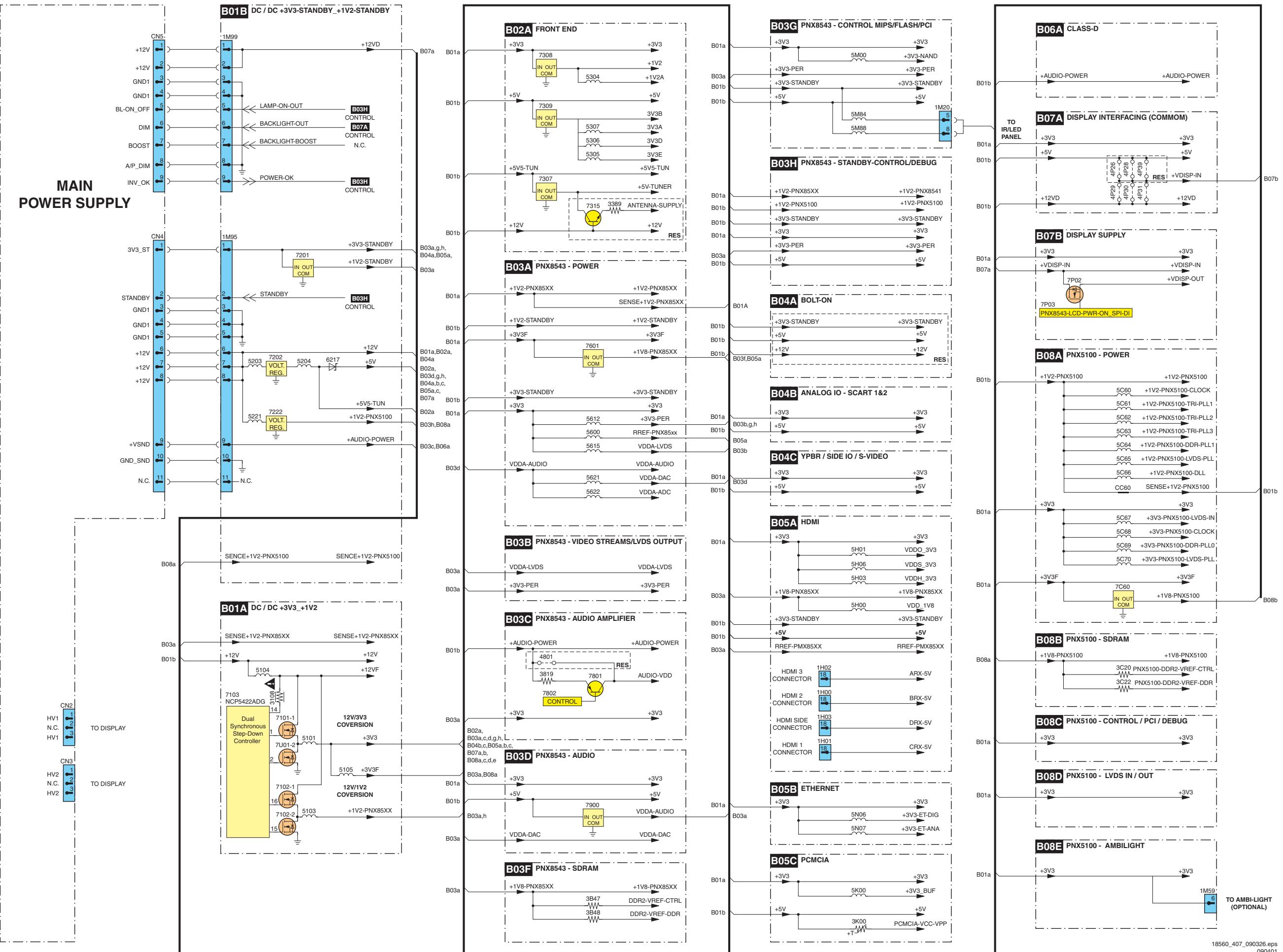


Block Diagram I²C



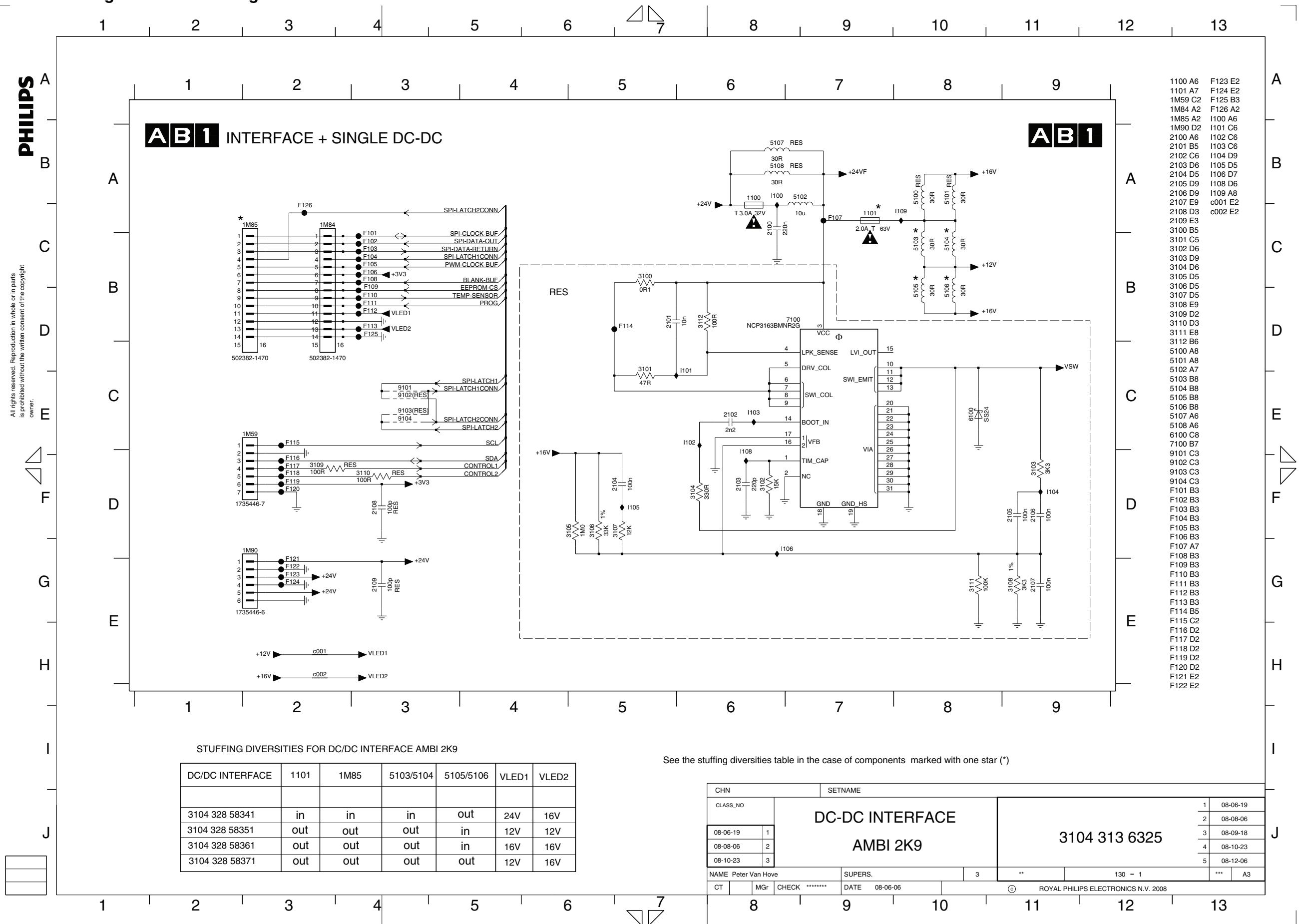
Supply Lines Overview

SUPPLY LINES OVERVIEW

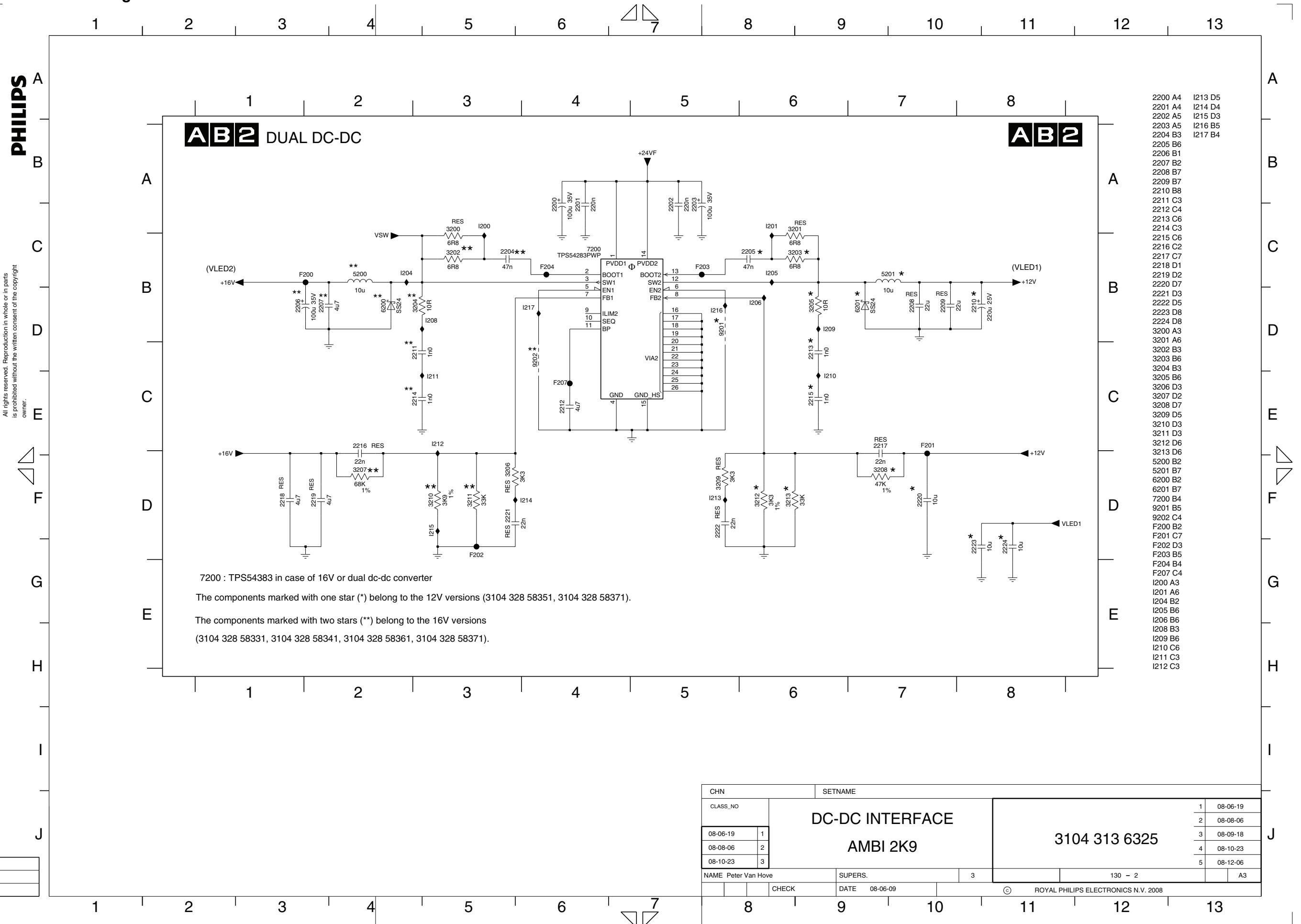


10. Circuit Diagrams and PWB Layouts

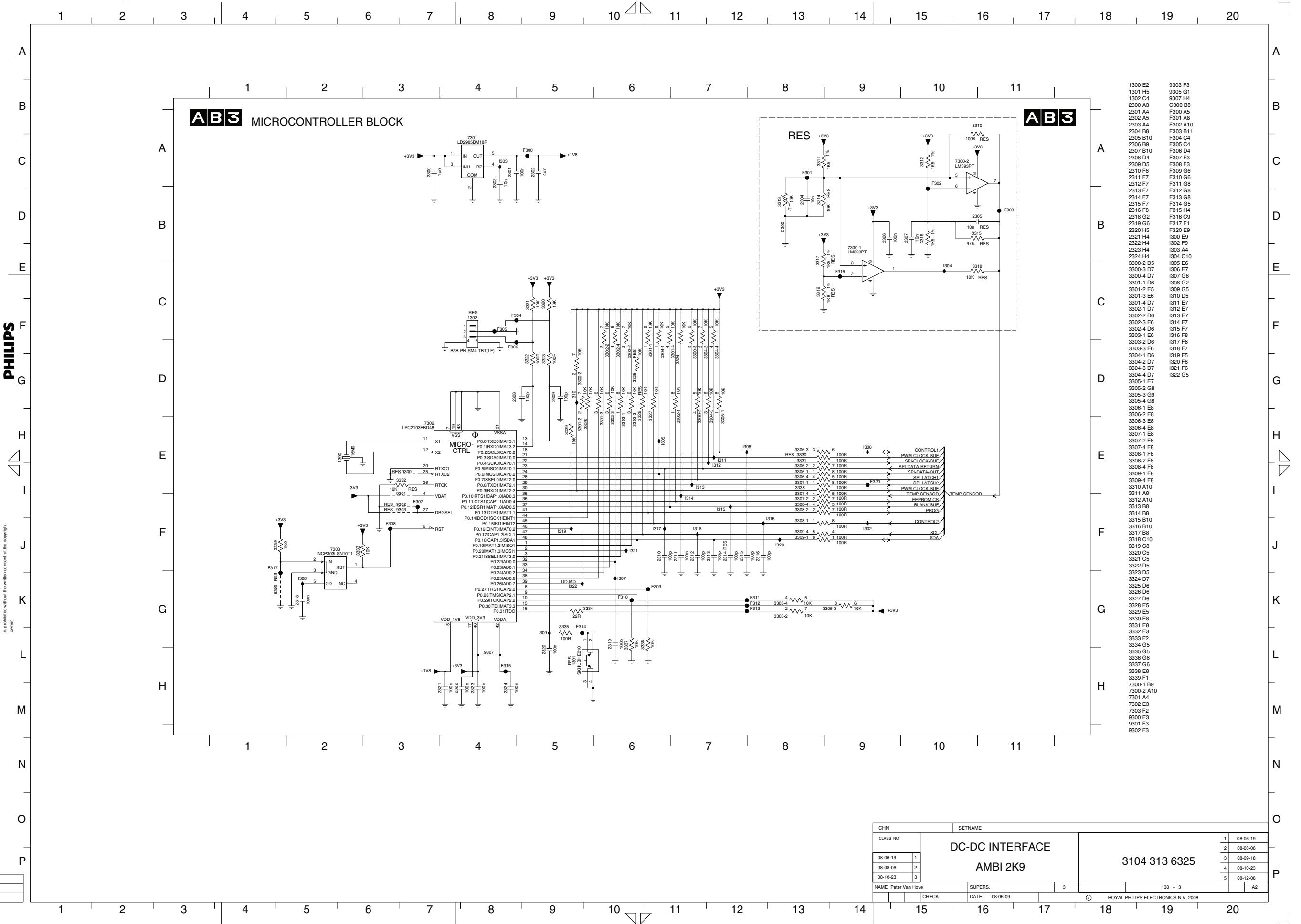
Interface Ambilight: Interface + Single DC-DC



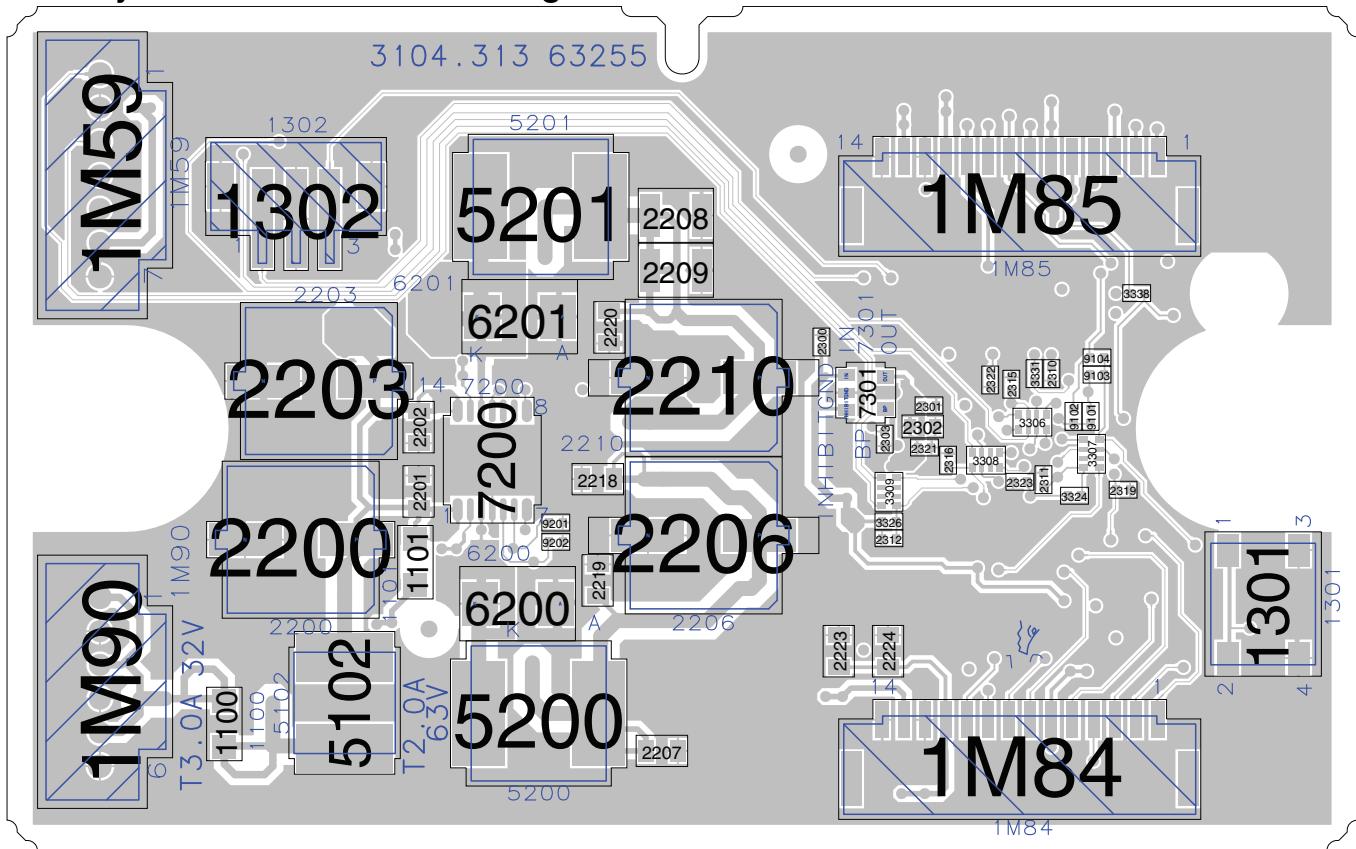
Interface Ambilight: Dual DC-DC



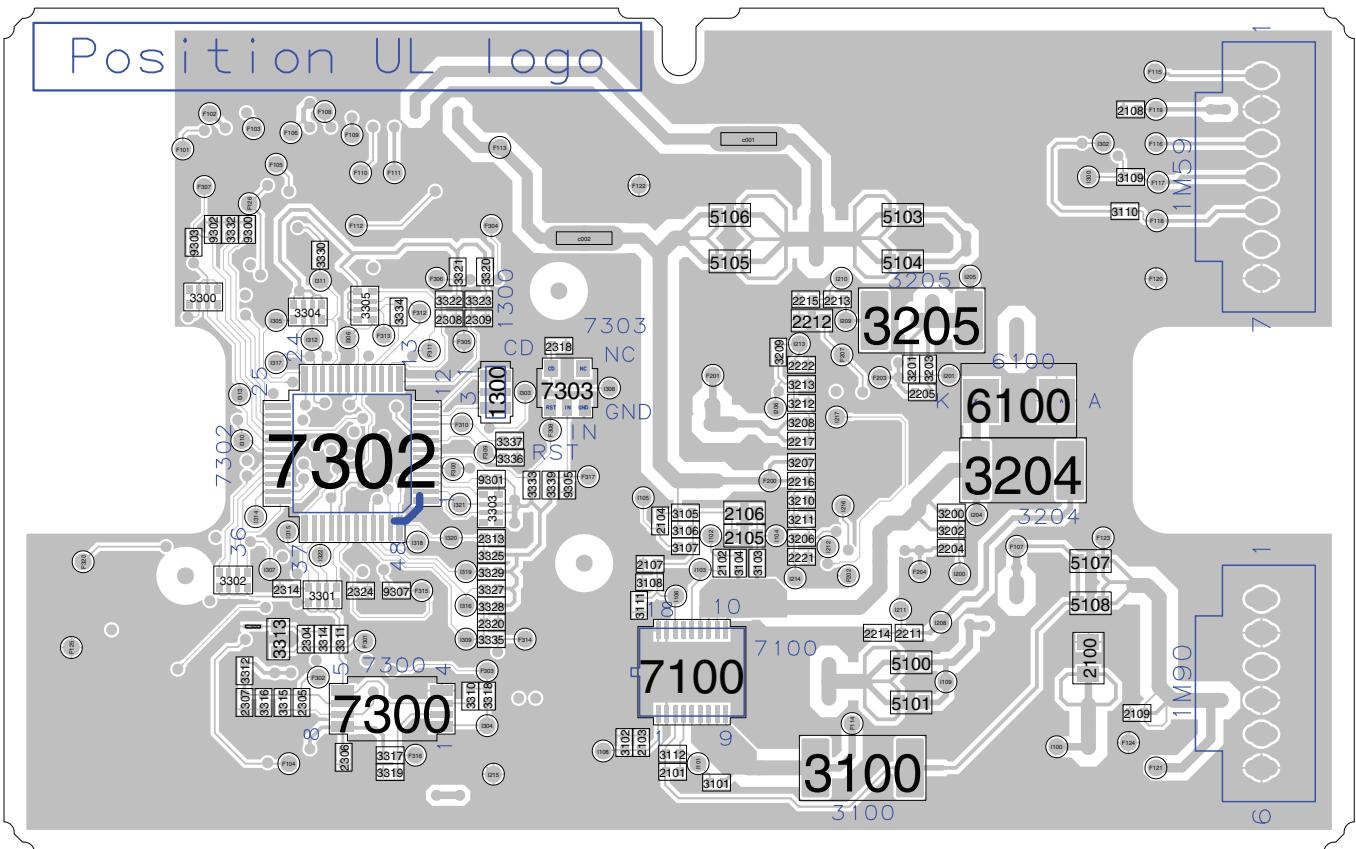
Interface Ambilight: Microcontrollerblock



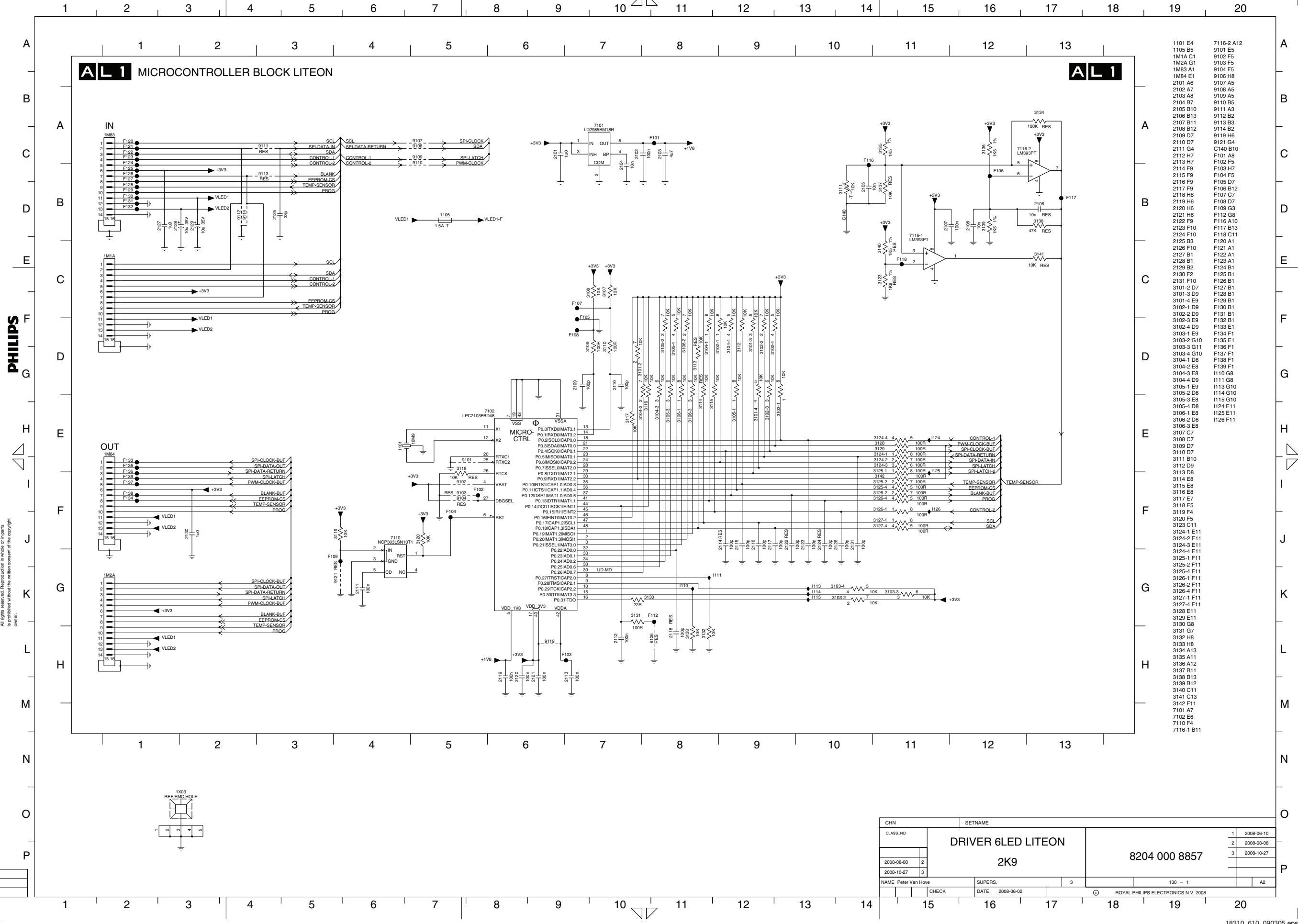
Layout DC/DC Interface Ambilight



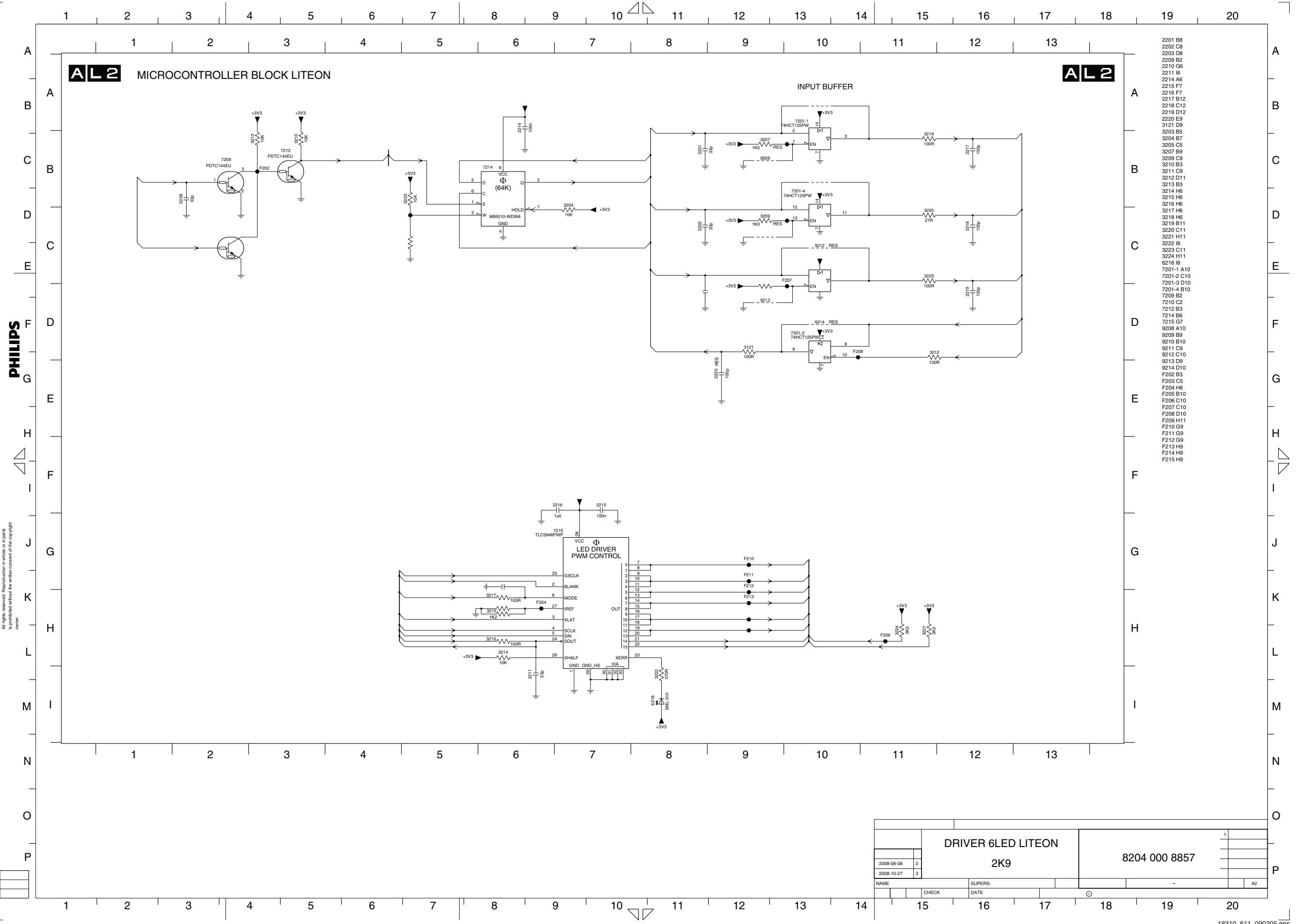
Personal Notes:

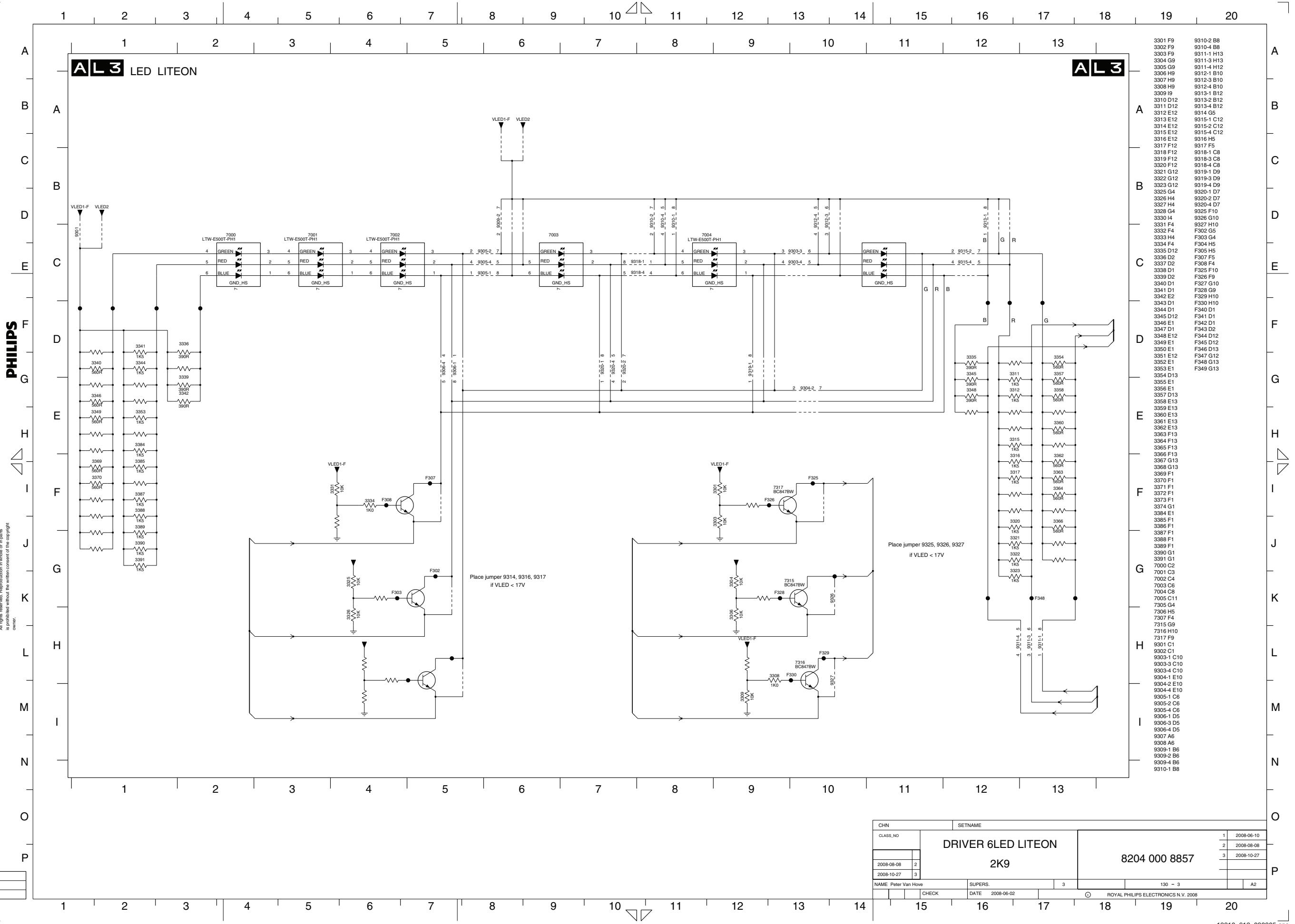


6 LED Low-Pow: Microcontroller Block Liteon

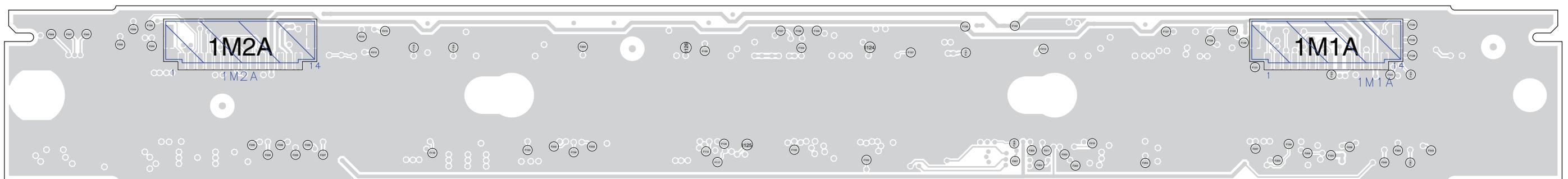
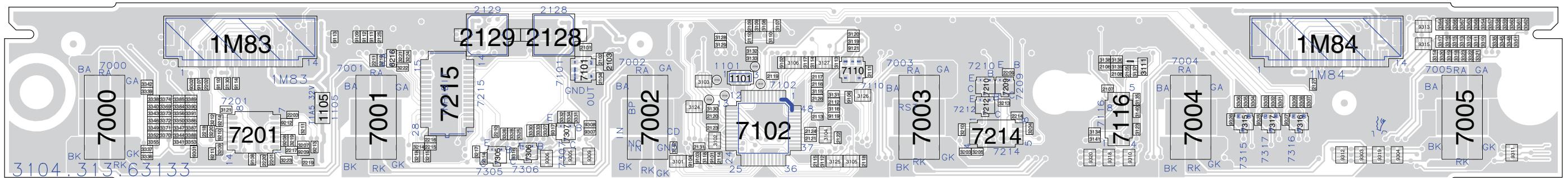


6 LED Low-Pow: Microcontroller Block Liteon



6 LED Low-Pow: LED Liteon

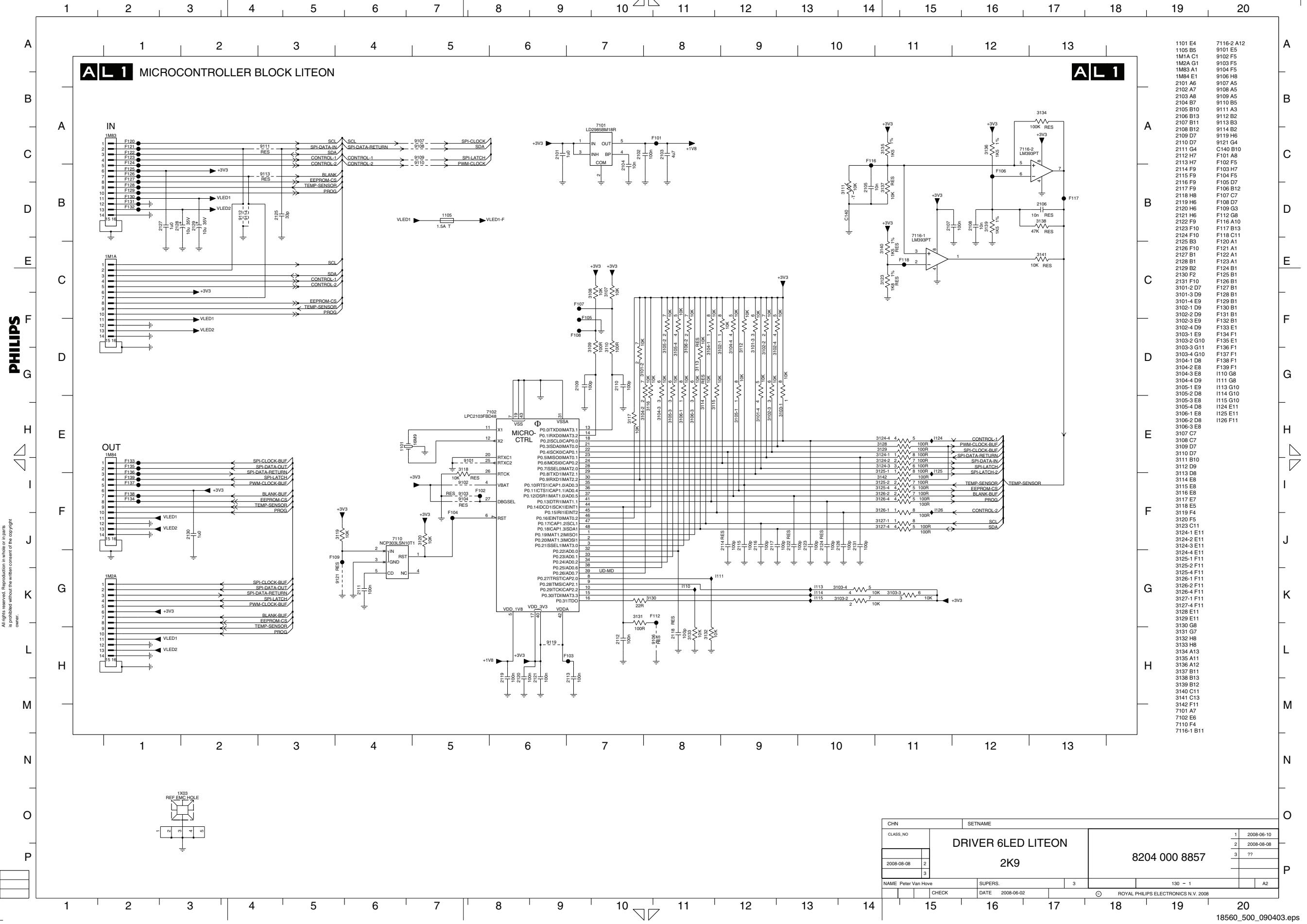
Layout 6 LED Low-Pow



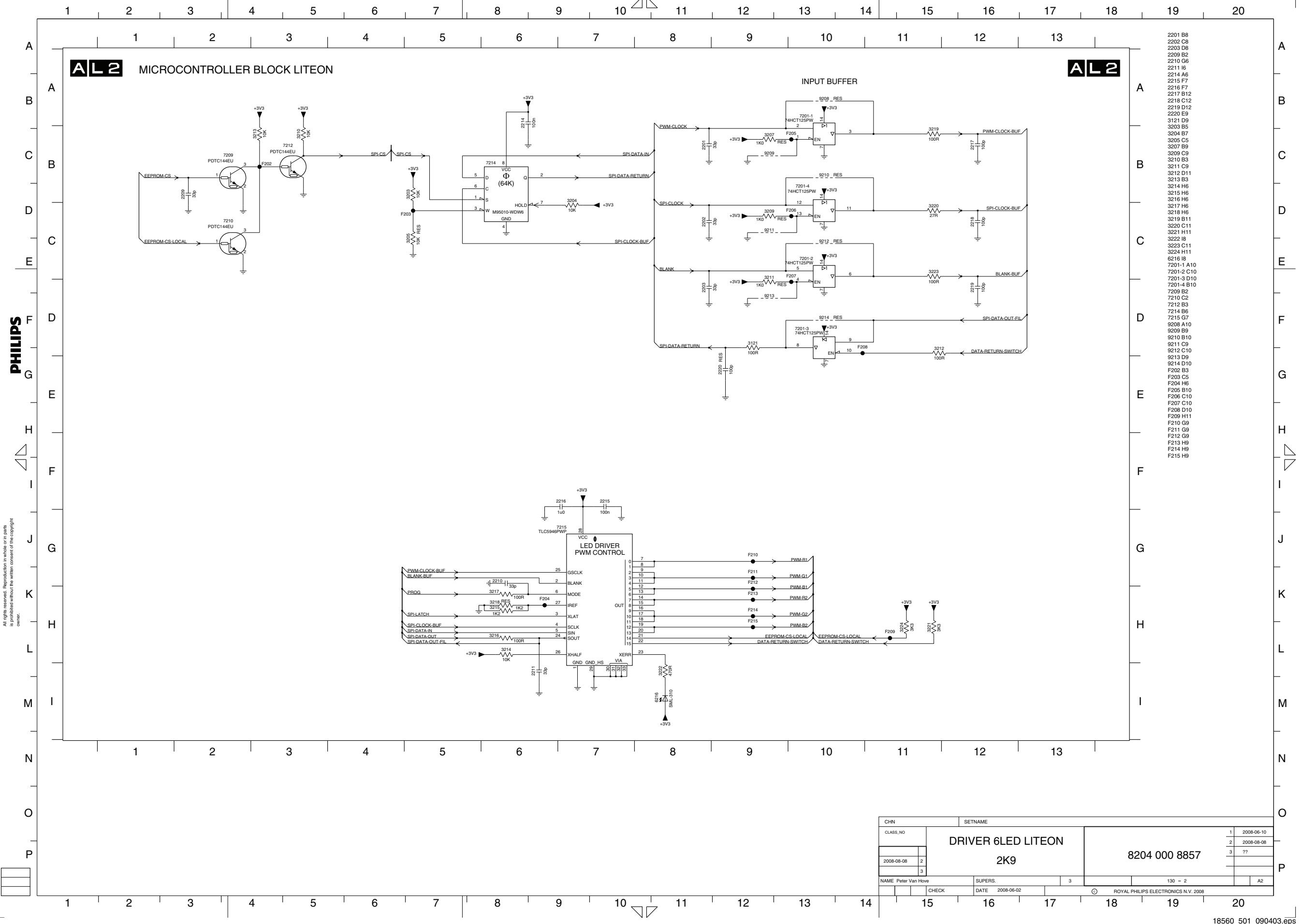
3104 313 6313.3

18310_551_090309
090309

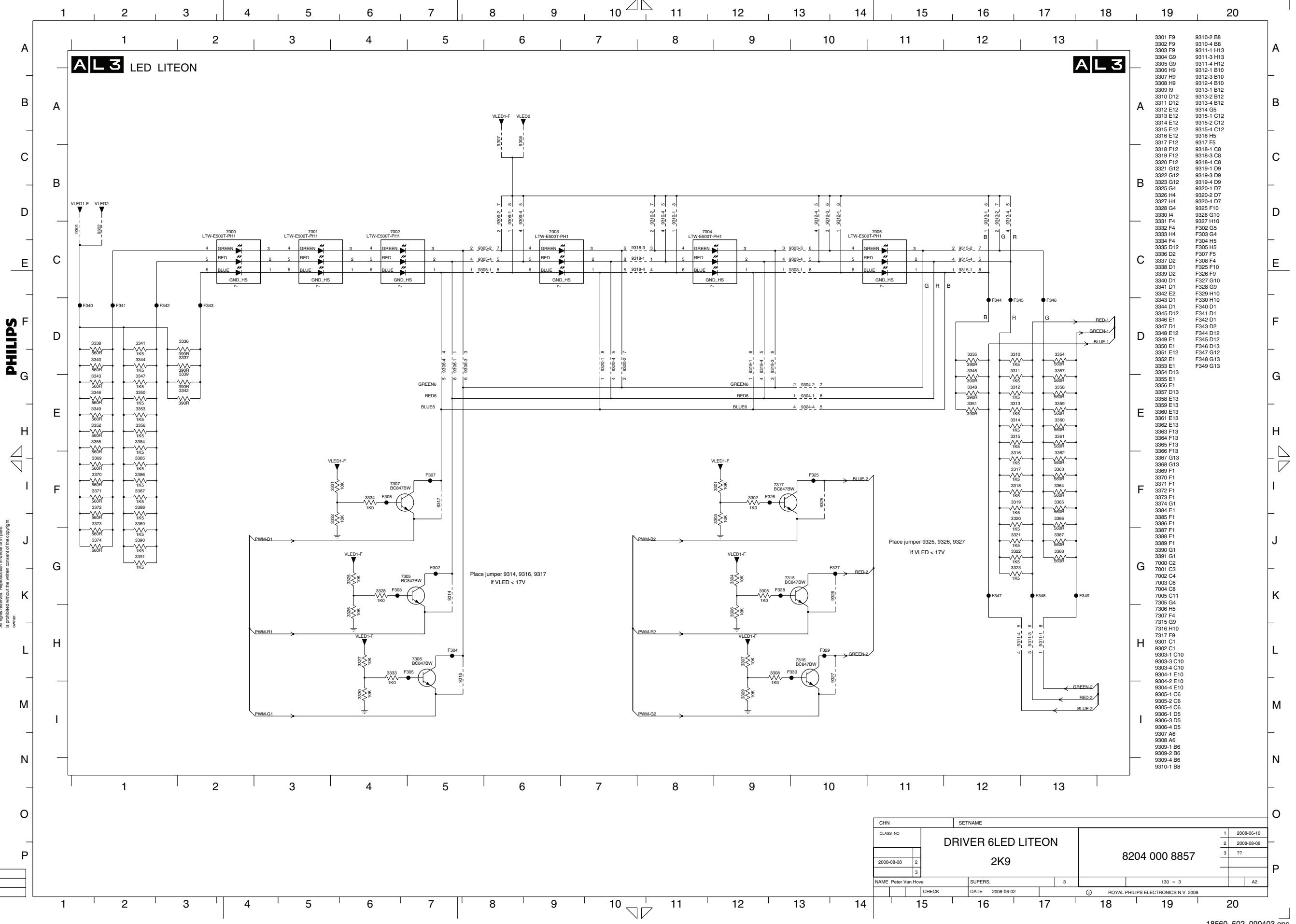
8 LED Low-Pow: Microcontroller Block Liteon



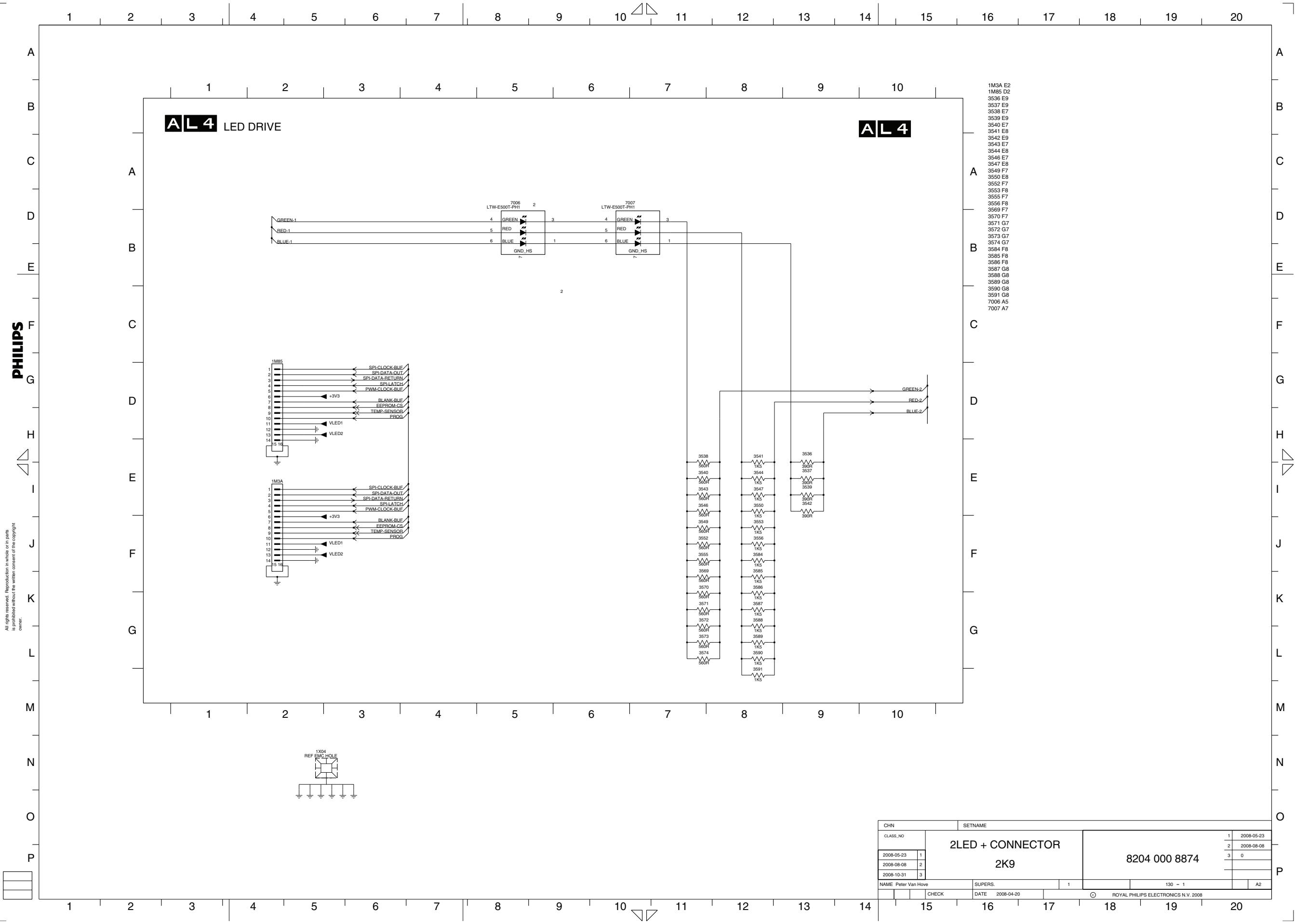
8 LED Low-Pow: Microcontroller Block Liteon



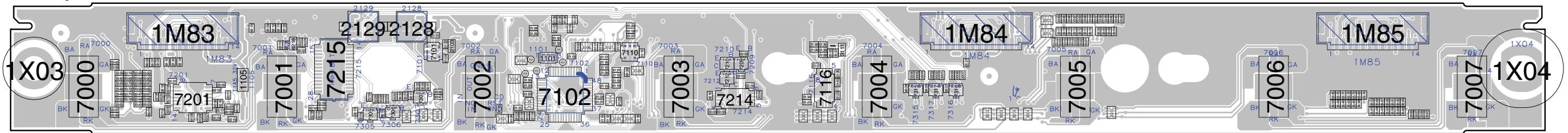
8 LED Low-Pow: LED Liteon



8 LED Low-Pow: LED Drive Liteon



Layout 8 LED Low-Pow

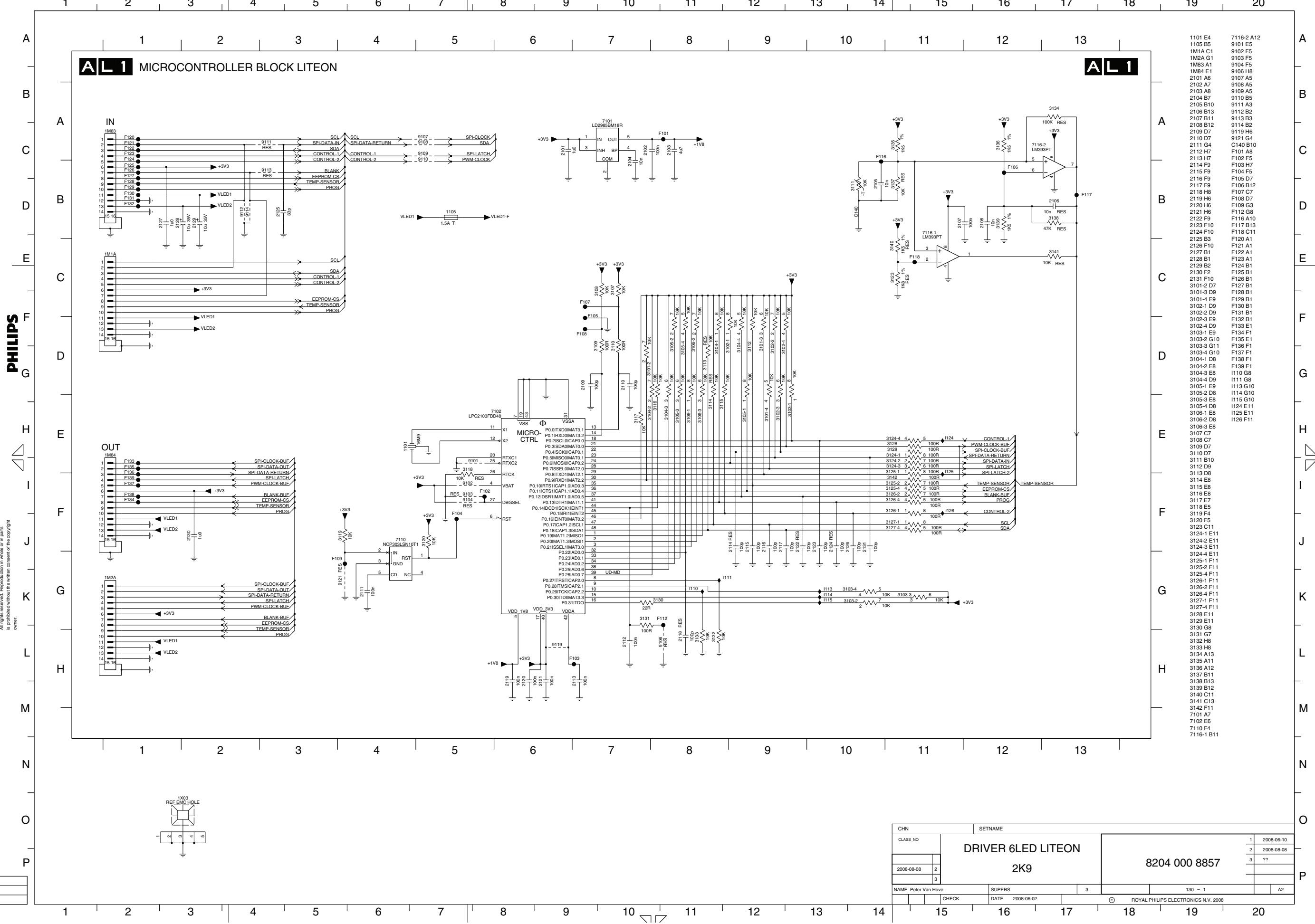


31043136314.3

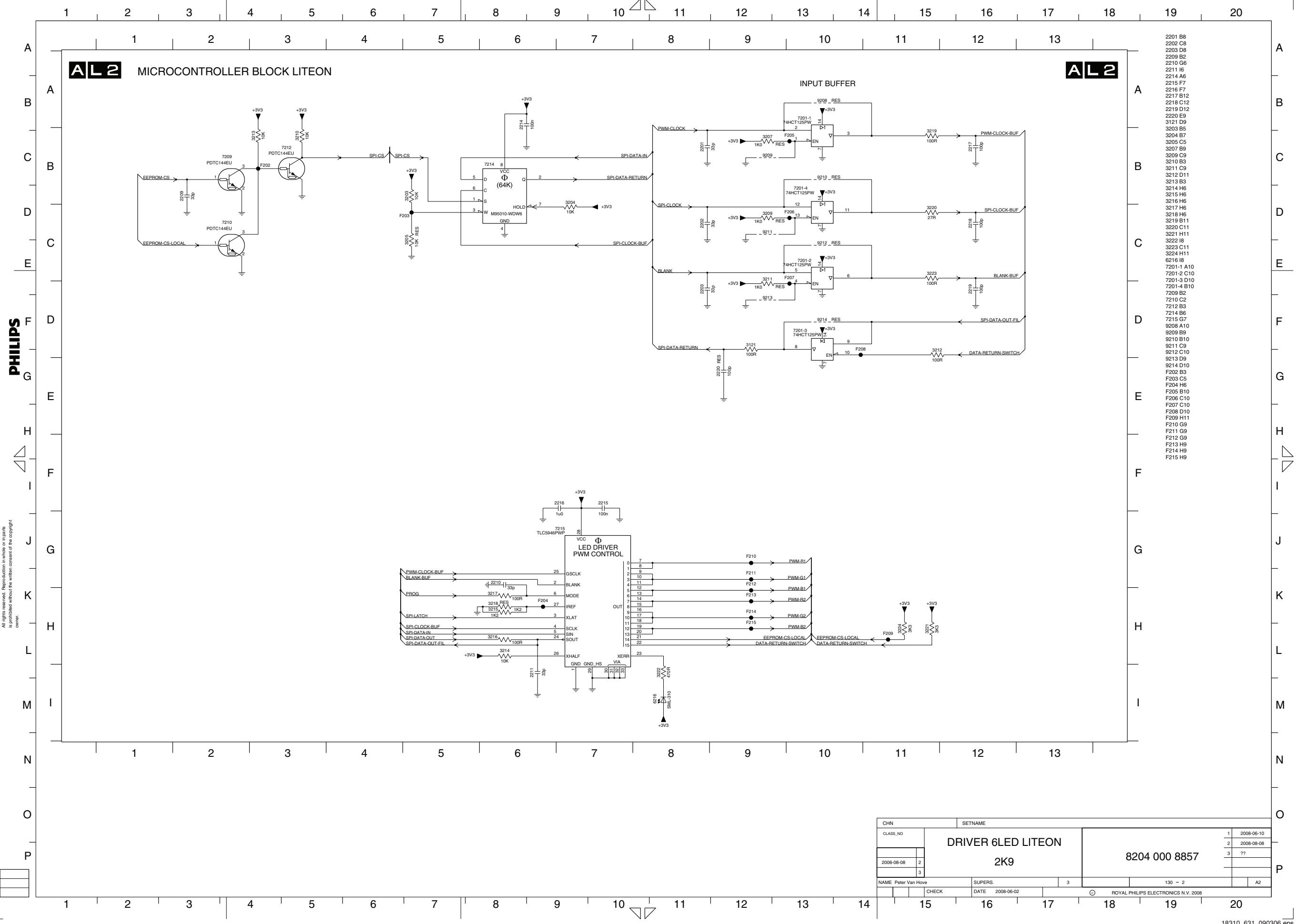
18490_550_090326.eps
090326



10 LED Low-Pow: Microcontroller Block Liteon

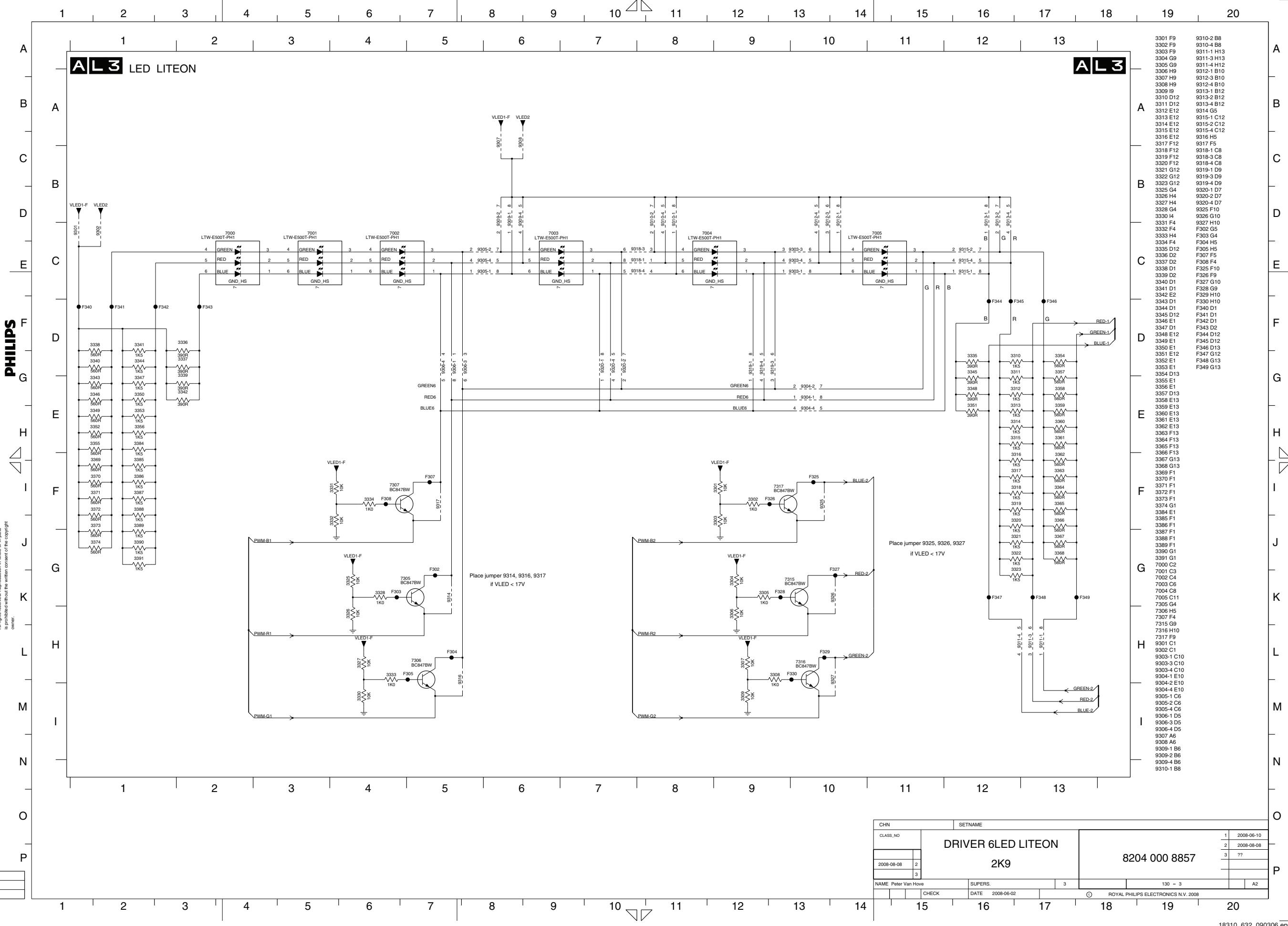


10 LED Low-Pow: Microcontroller Block Liteon

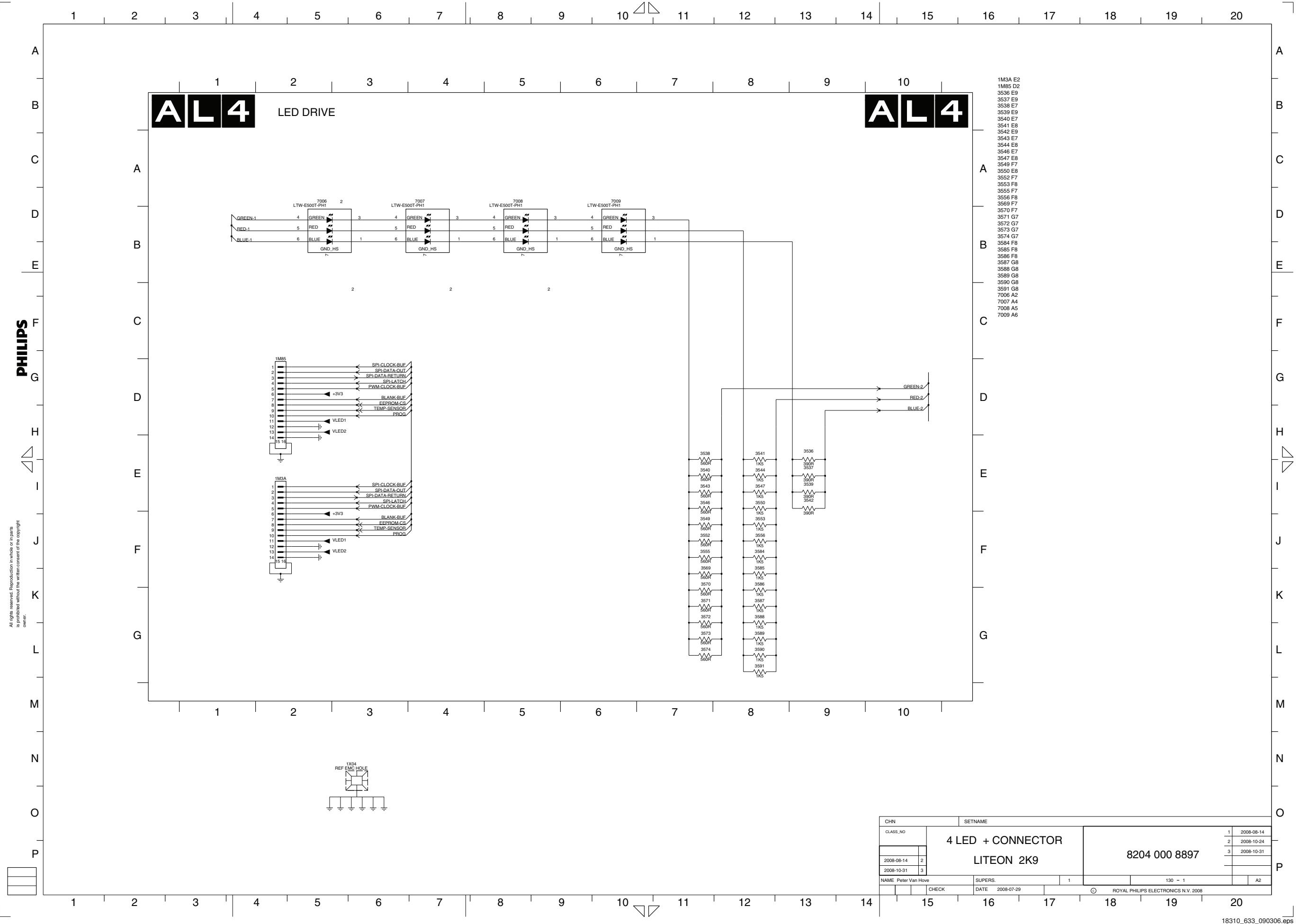




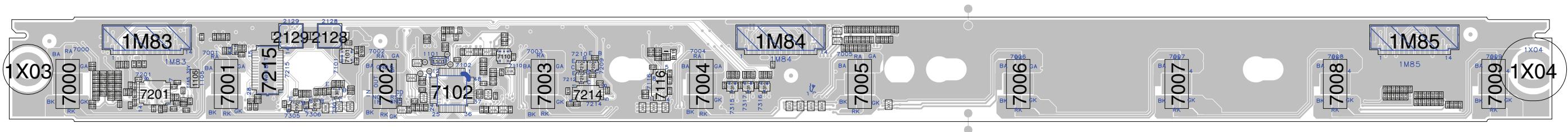
10 LED Low-Pow: LED Liteon



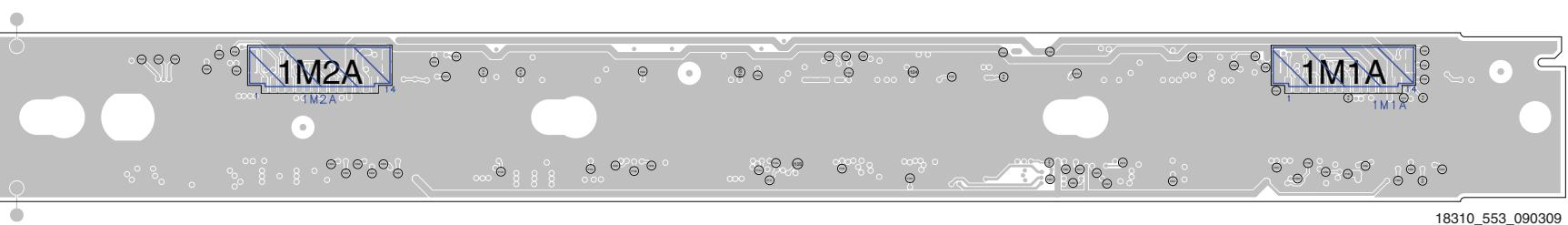
10 LED Low-Pow: LED Drive Liteon



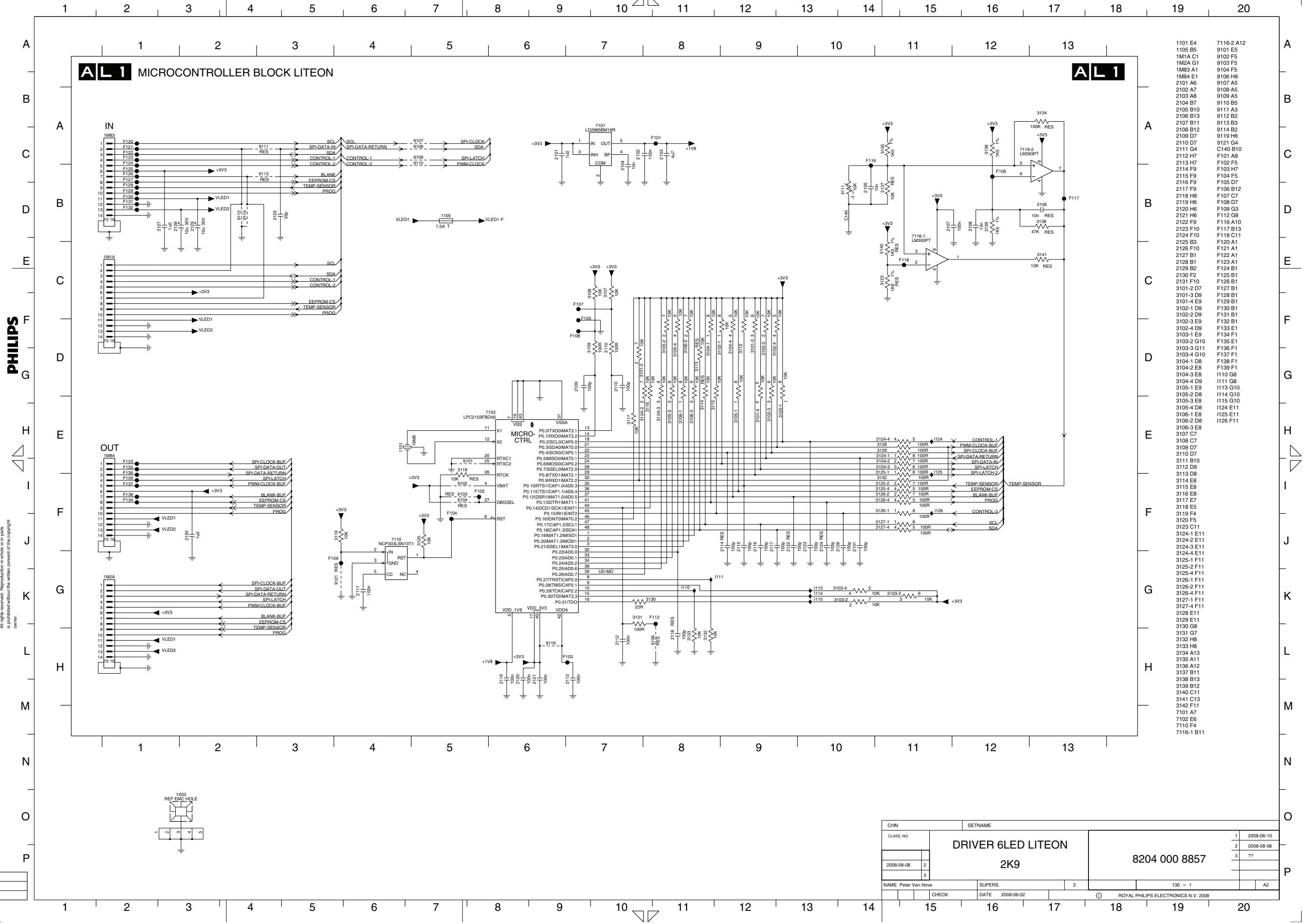
Layout 10 LED Low-Pow



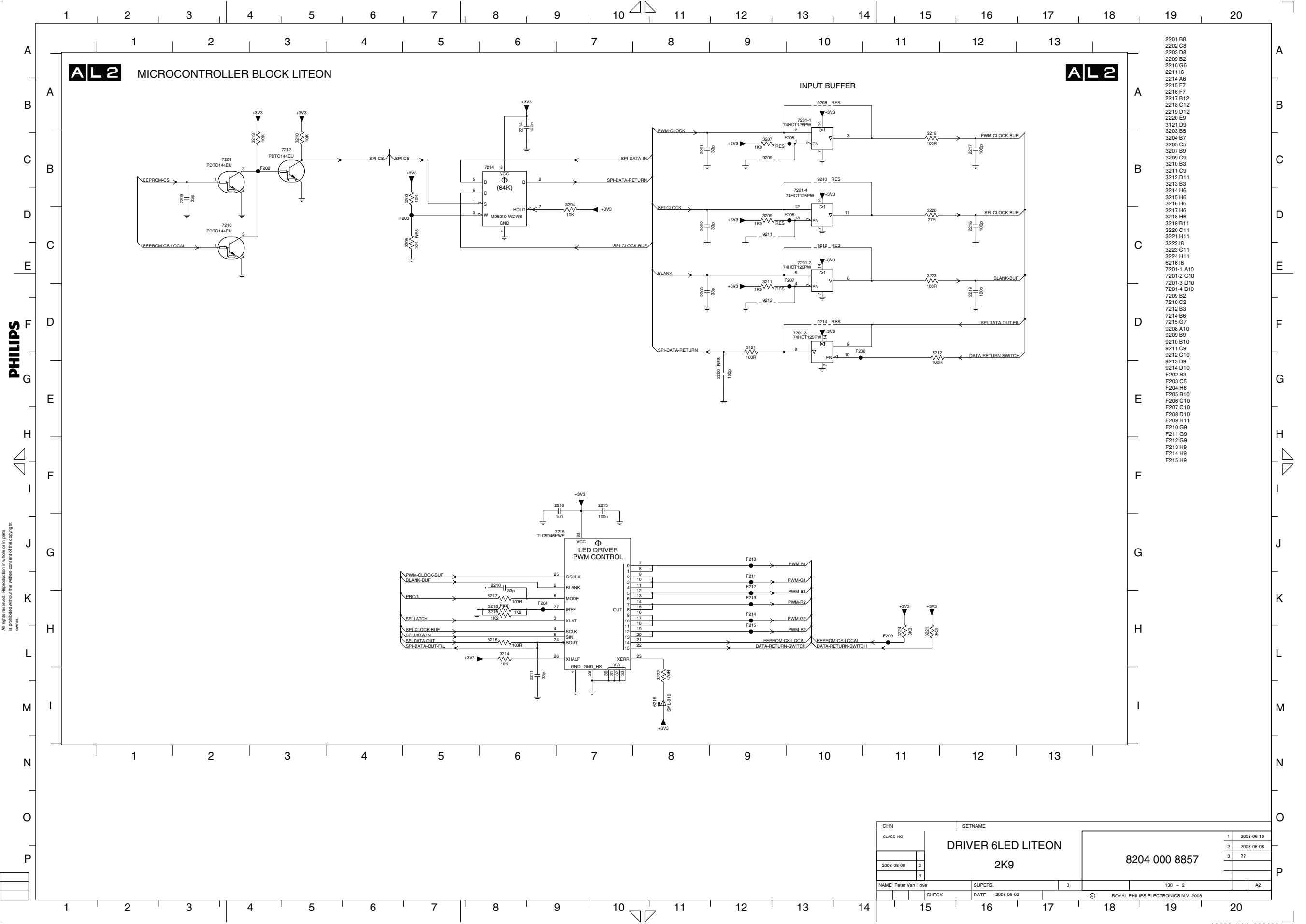
3104 313 6315.2

18310_553_090309
090309

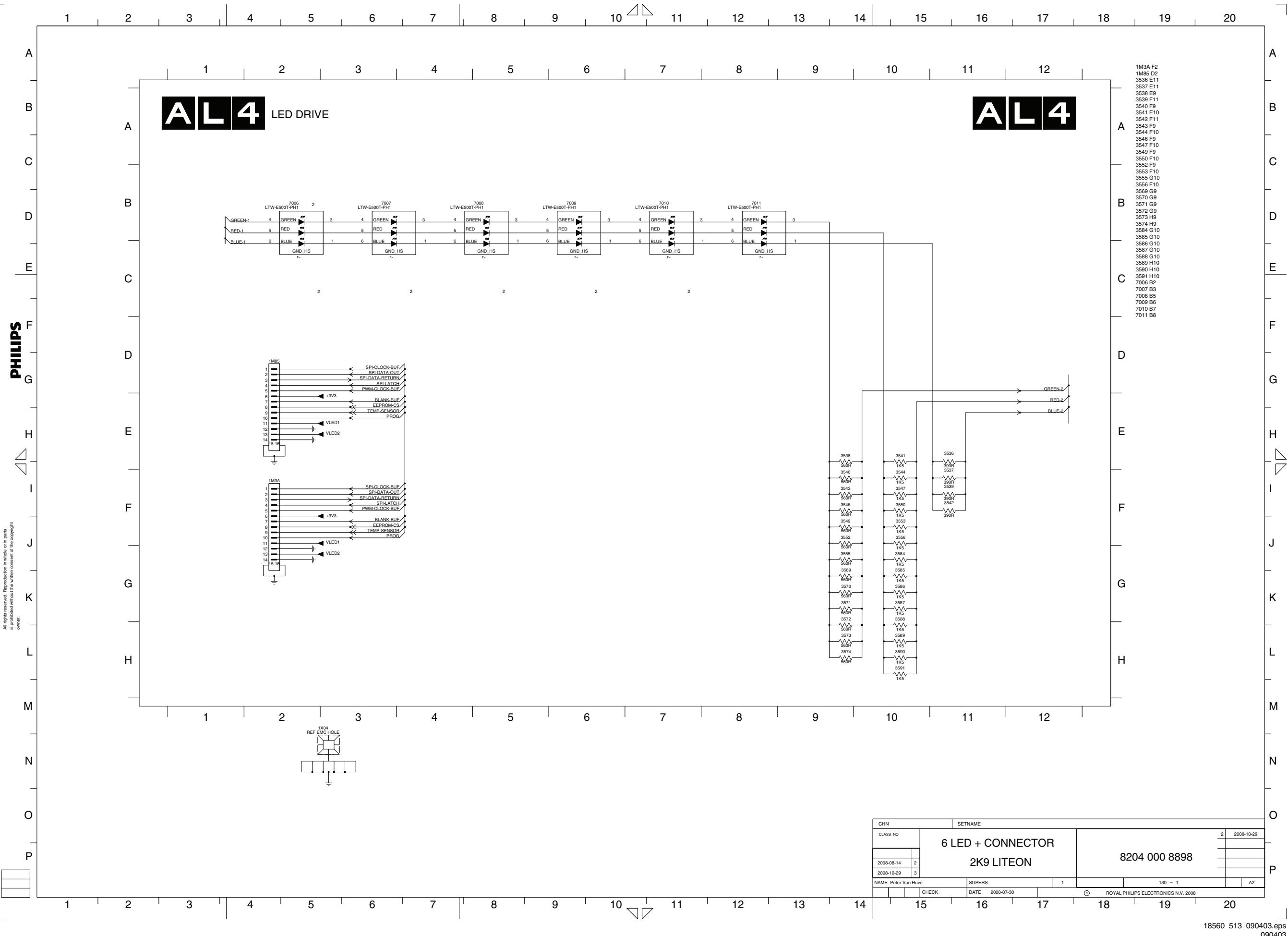
12 LED Low-Pow: Microcontroller Block Liteon



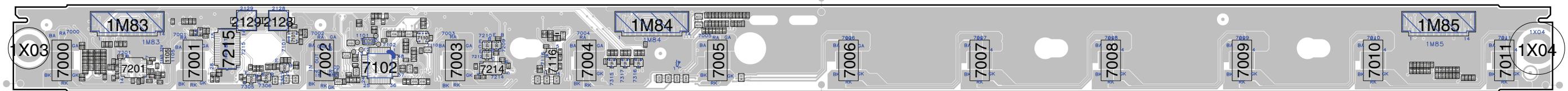
12 LED Low-Pow: Microcontroller Block Liteon



12 LED Low-Pow: LED Drive



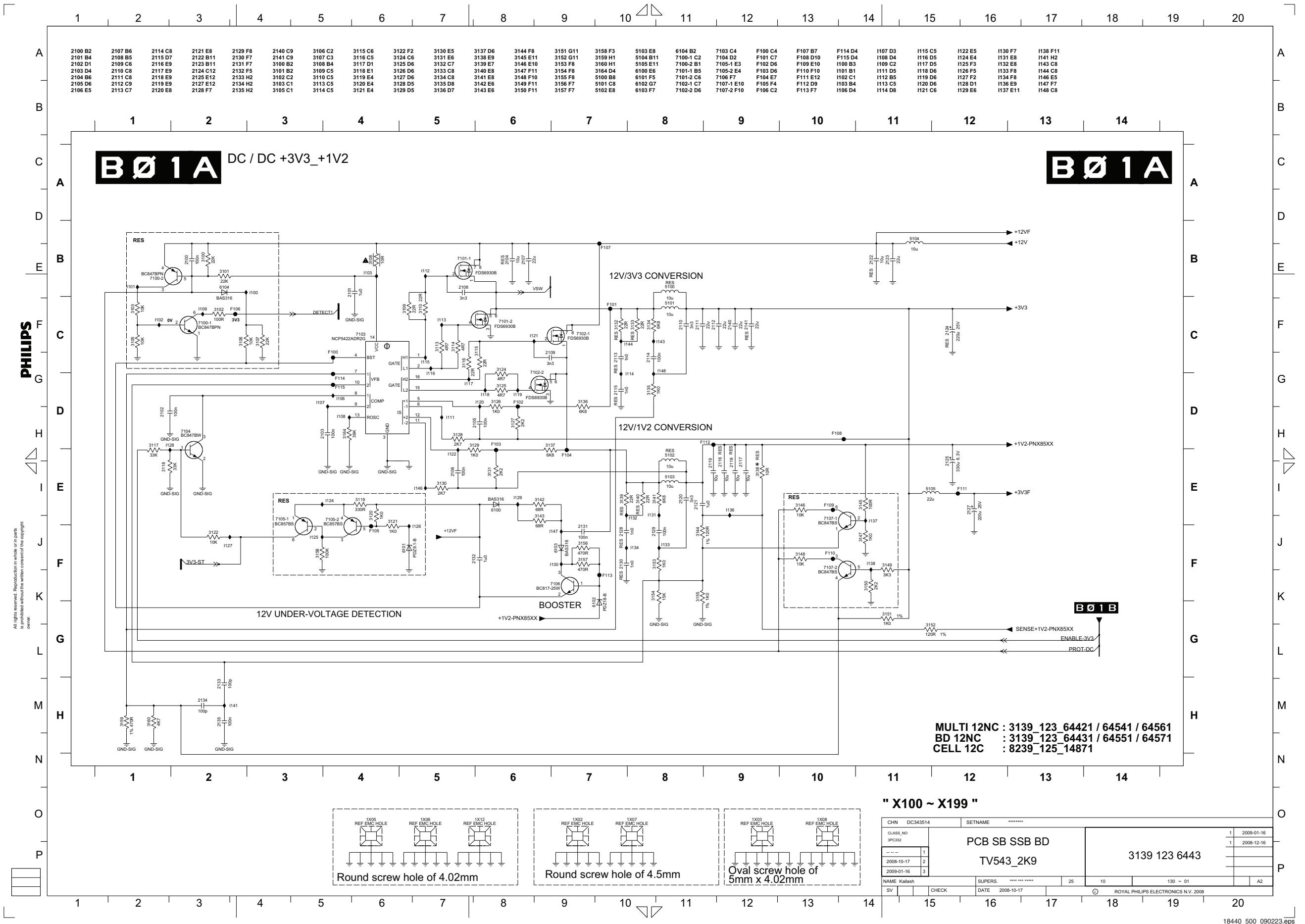
Layout 12 LED Low-Pow



31043136335.2

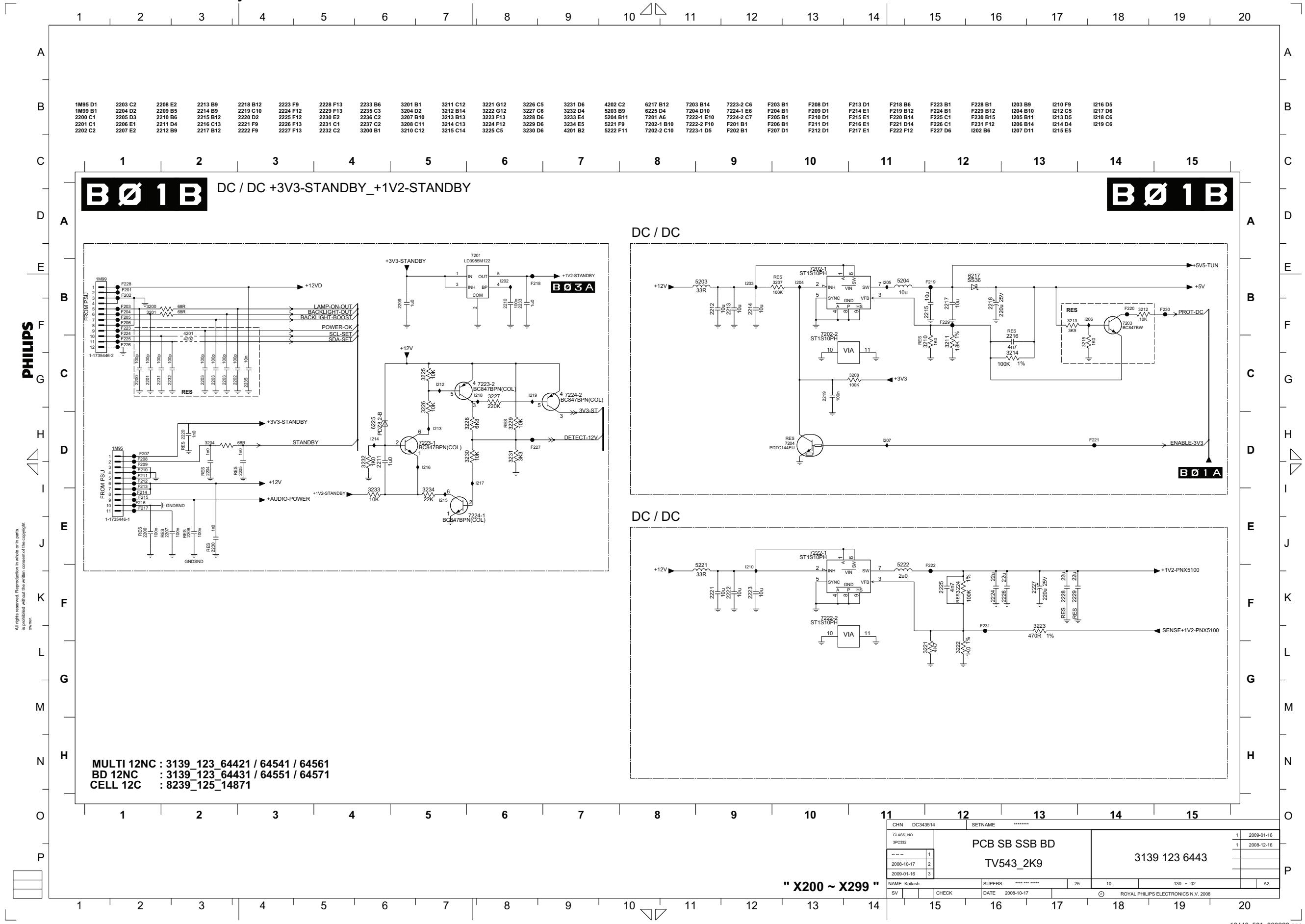
18490_551_090326.eps
090331

SSB: DC/DC +3V3 +1V2



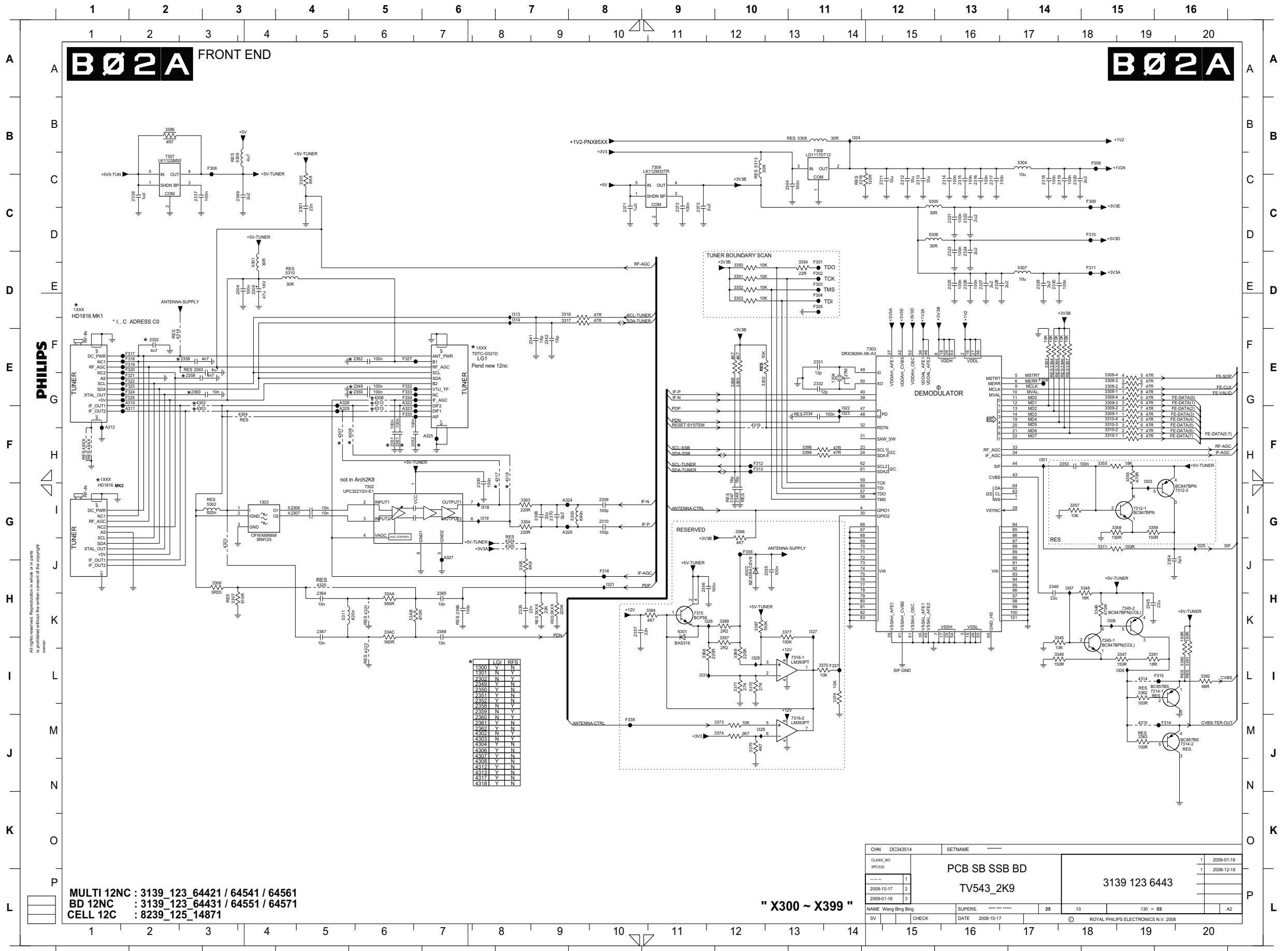


SSB: DC/DC +3V3 +1V2 Standby

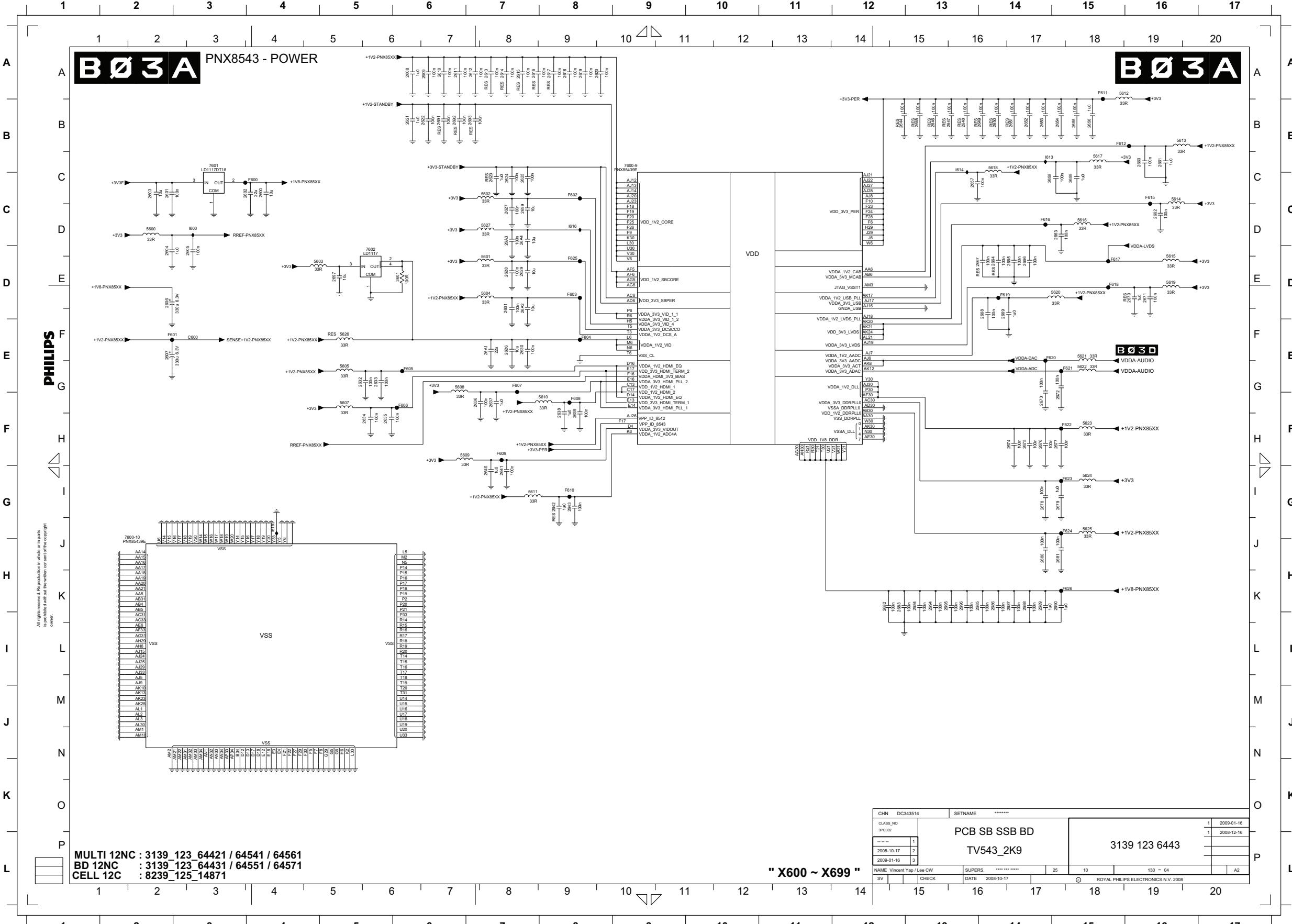




SSB: Front End

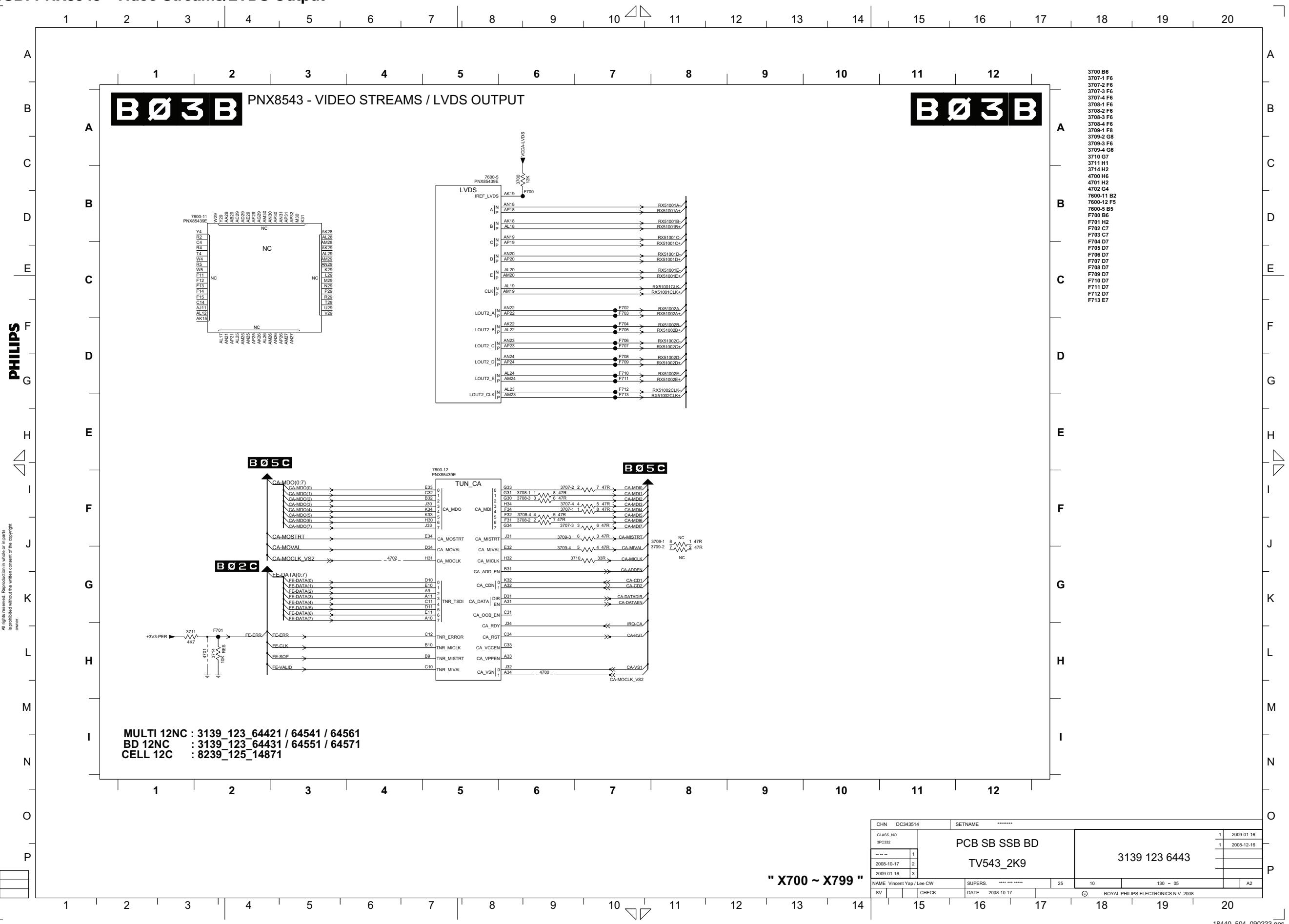


SSB: PNX8543 - Power

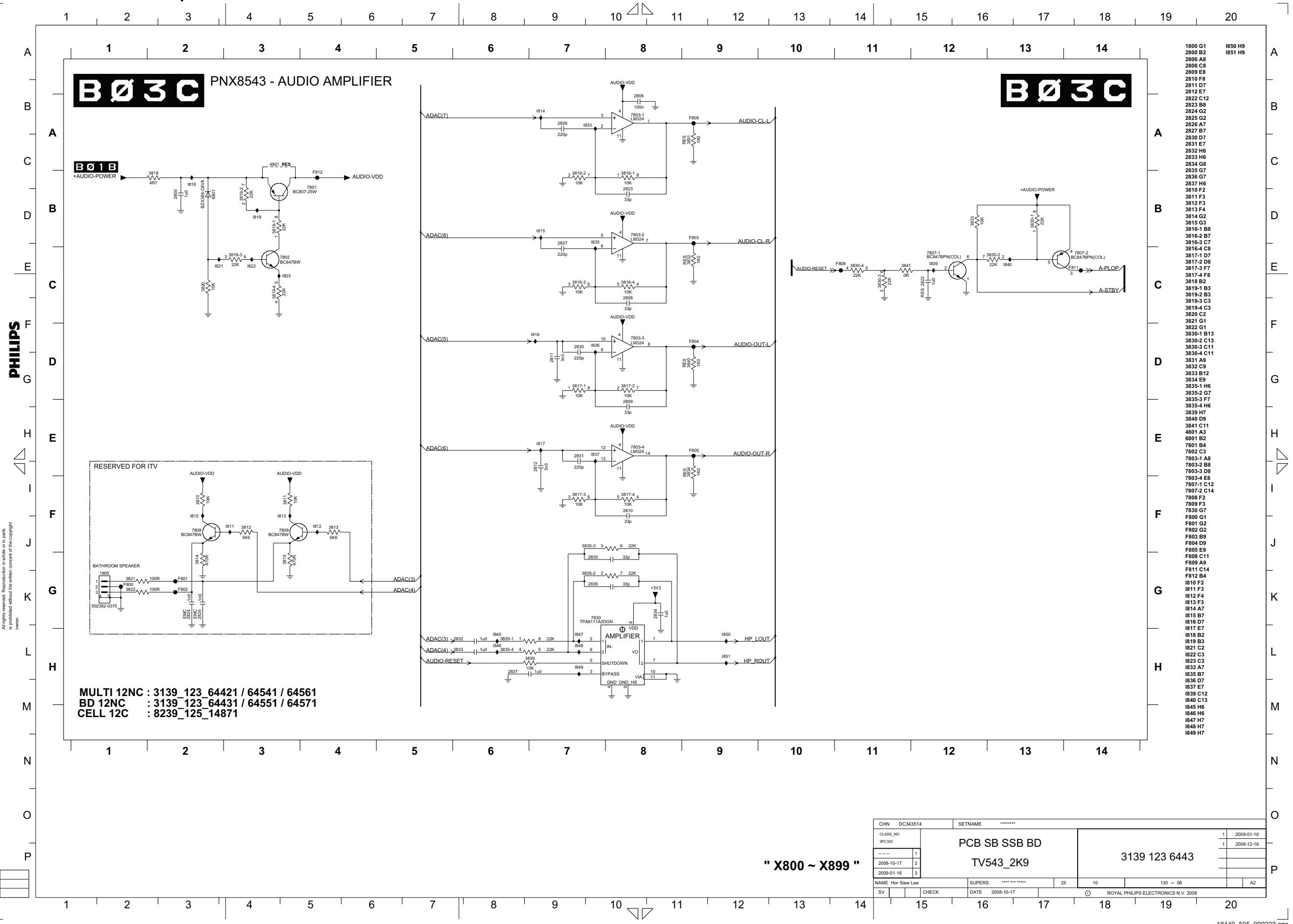


2600 C4	F609 F7
2601 C2	F610 G8
2602 E2	F611 A16
2602 C2	F612 P15
2604 D3	F615 C16
2605 D3	F616 C14
2606 D2	F617 D15
2606 E2	F618 D15
2609 A6	F620 E14
2610 A6	F621 E15
2611 A6	F622 F15
2612 A7	F623 G15
2614 A7	F625 G15
2614 A7	F625 D8
2615 A7	F626 H15
2616 A7	I600 C3
2617 A8	I611 B14
2617 A8	I612 I13
2619 A8	I615 G4
2620 A8	I616 C8
2621 B6	
2622 B6	
2623 C7	
2625 C7	
2626 E7	
2627 C7	
2629 D7	
2630 E7	
2631 D7	
2632 E5	
2633 E5	
2634 F5	
2635 F5	
2636 F7	
2637 F7	
2638 F9	
2639 F8	
2640 G7	
2641 G7	
2642 G8	
2643 G8	
2644 B12	
2645 B13	
2646 B13	
2647 B13	
2648 B13	
2649 B13	
2650 B14	
2651 B14	
2652 B14	
2653 B14	
2654 B15	
2655 B15	
2656 B15	
2657 C13	
2658 C14	
2659 C15	
2660 B16	
2661 B16	
2662 C15	
2664 D14	
2665 D14	
2666 D14	
2667 D14	
2668 E14	
2669 D14	
2670 D16	
2671 D16	
2672 F15	
2673 F14	
2675 F14	
2676 F14	
2677 F15	
2678 G14	
2679 G15	
2680 H14	
2681 H15	
2682 H12	
2683 H12	
2684 H13	
2685 H13	
2686 H14	
2687 H14	
2688 H14	
2689 H15	
2690 H15	
2691 B6	
2692 B6	
2693 B7	
2694 H13	
2695 H13	
2696 H13	
2697 D5	
2698 C7	
26A1 E7	
26A2 D7	
26A3 C7	
26A4 C7	
3610 D6	
5600 C2	
5601 D7	
5602 C7	
5603 D4	
5604 D7	
5605 E7	
5606 E5	
5607 F5	
5608 F6	
5609 F6	
5610 F5	
5611 E5	
5612 E5	
5613 E5	
5614 E5	
5615 E5	
5616 E5	
5617 E5	
5618 E5	
5619 E5	
5620 E5	
5621 E5	
5622 E5	
5623 E5	
5624 E5	
5625 E5	
5626 E5	
5627 C7	
7600-10 G2	
7600-9 B9	
7610 B3	
7620 D5	
C600 E3	
F600 C4	
F601 E2	
F602 C6	
F603 D8	
F604 E8	
F605 E6	
F606 F6	
F607 E7	
F608 F6	

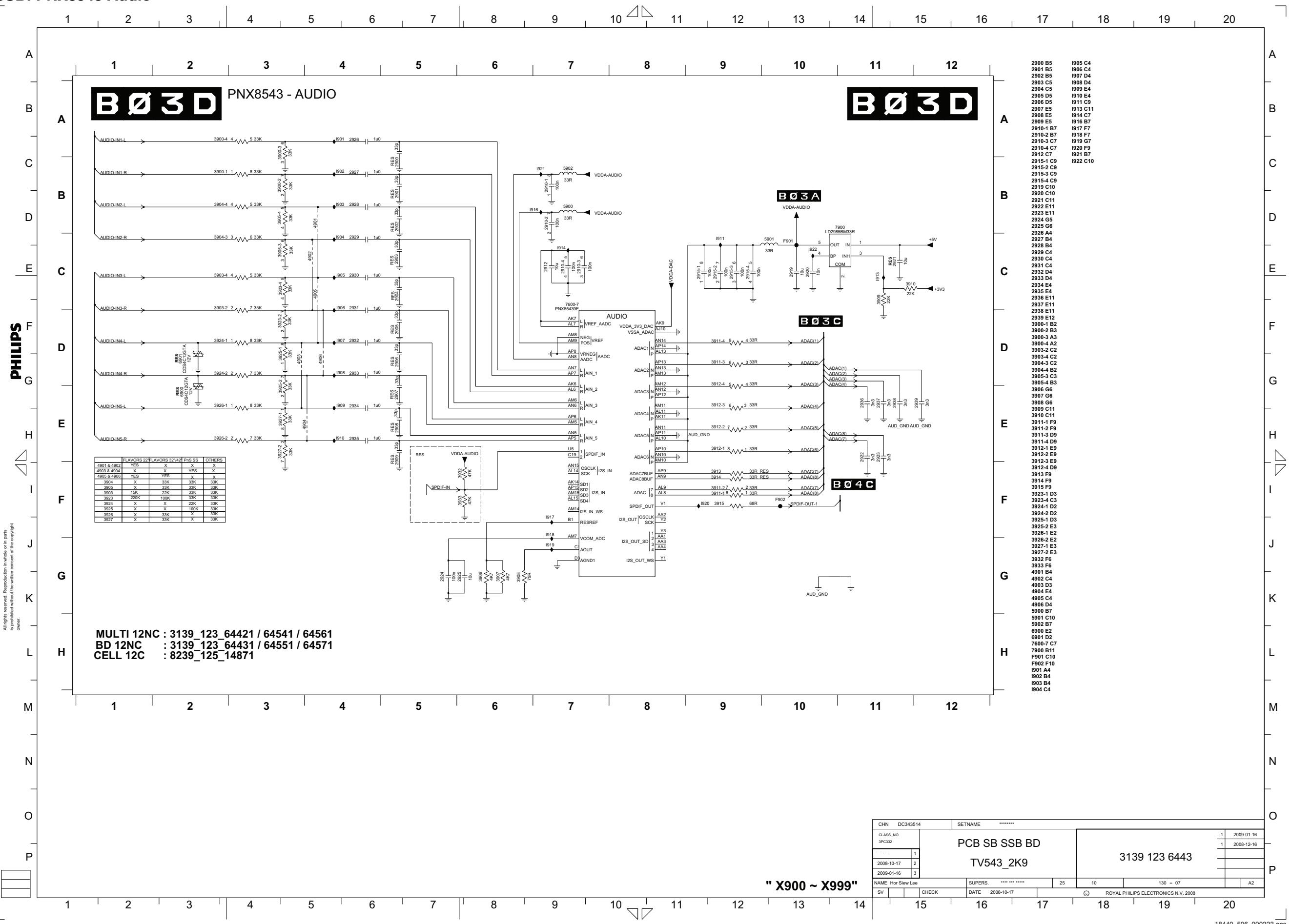
SSB: PNX8543 - Video Streams/LVDS Output



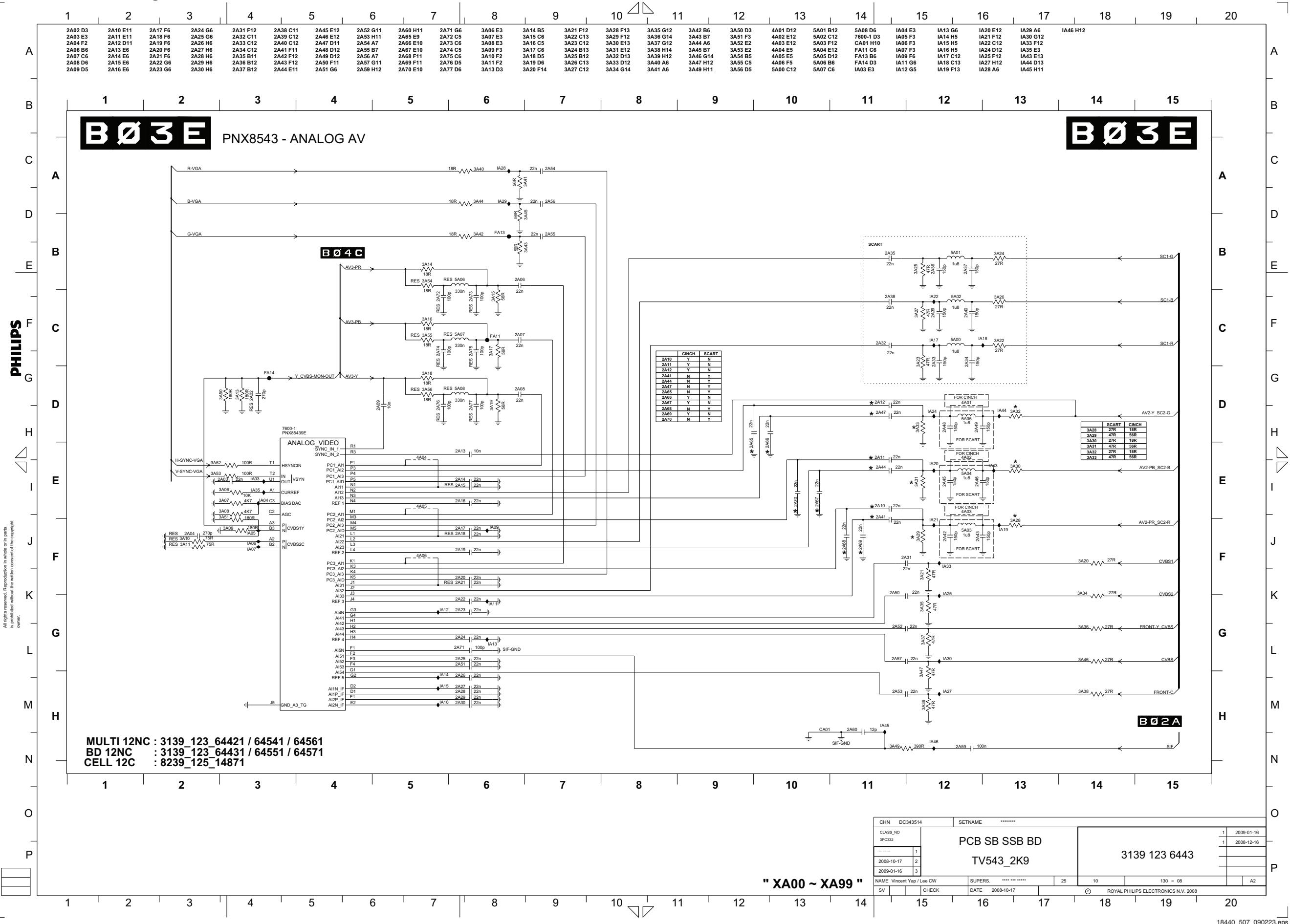
SSB: PNX8543 Audio Amplifier



SSB: PNX8543 Audio

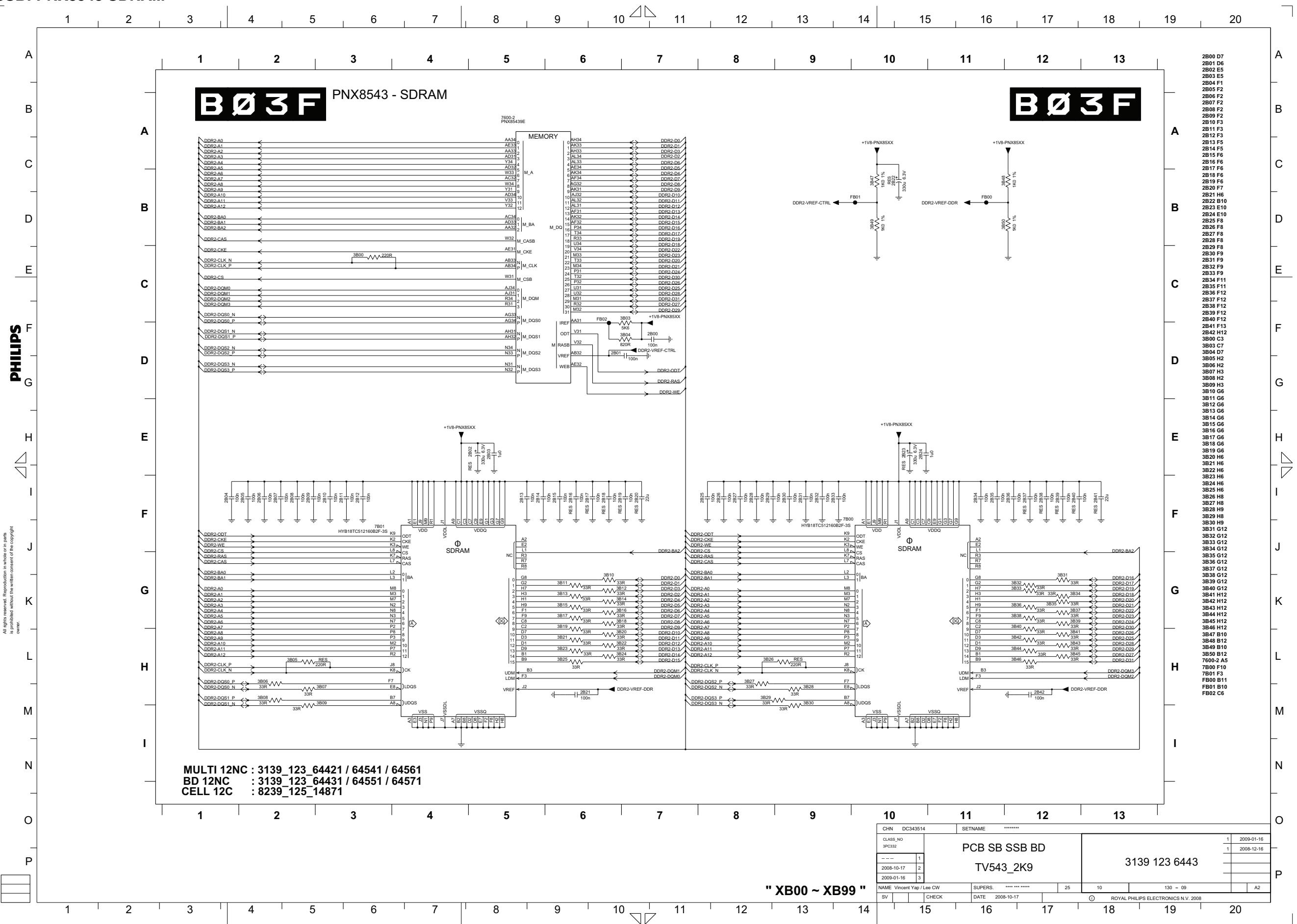


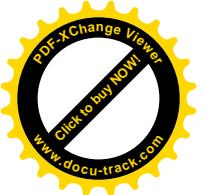
SSB: PNX8543 Analog AV



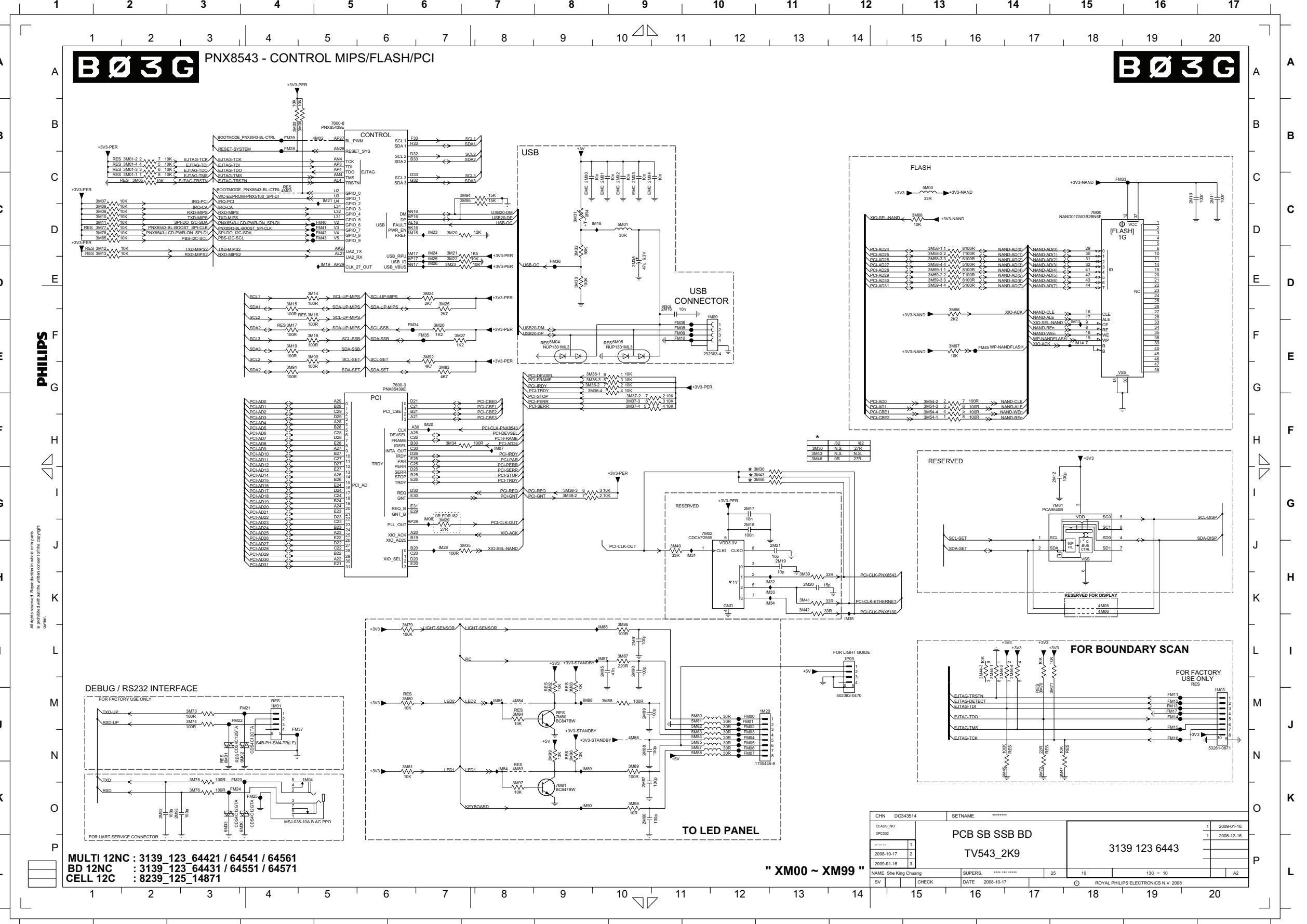


SSB: PNX8543 SDRAM



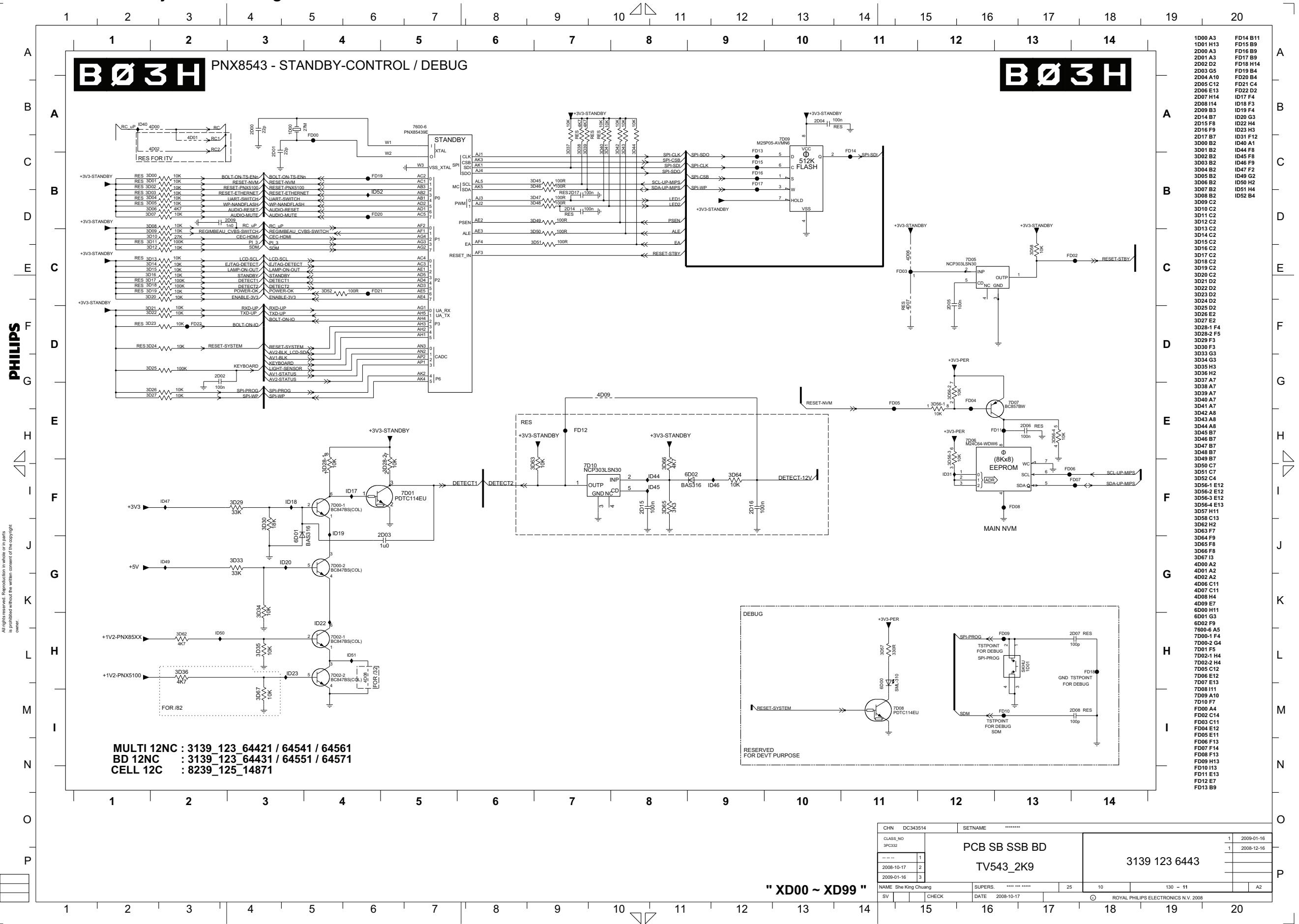


SSB: PNX8543 Control MIPS/Flash/PCI

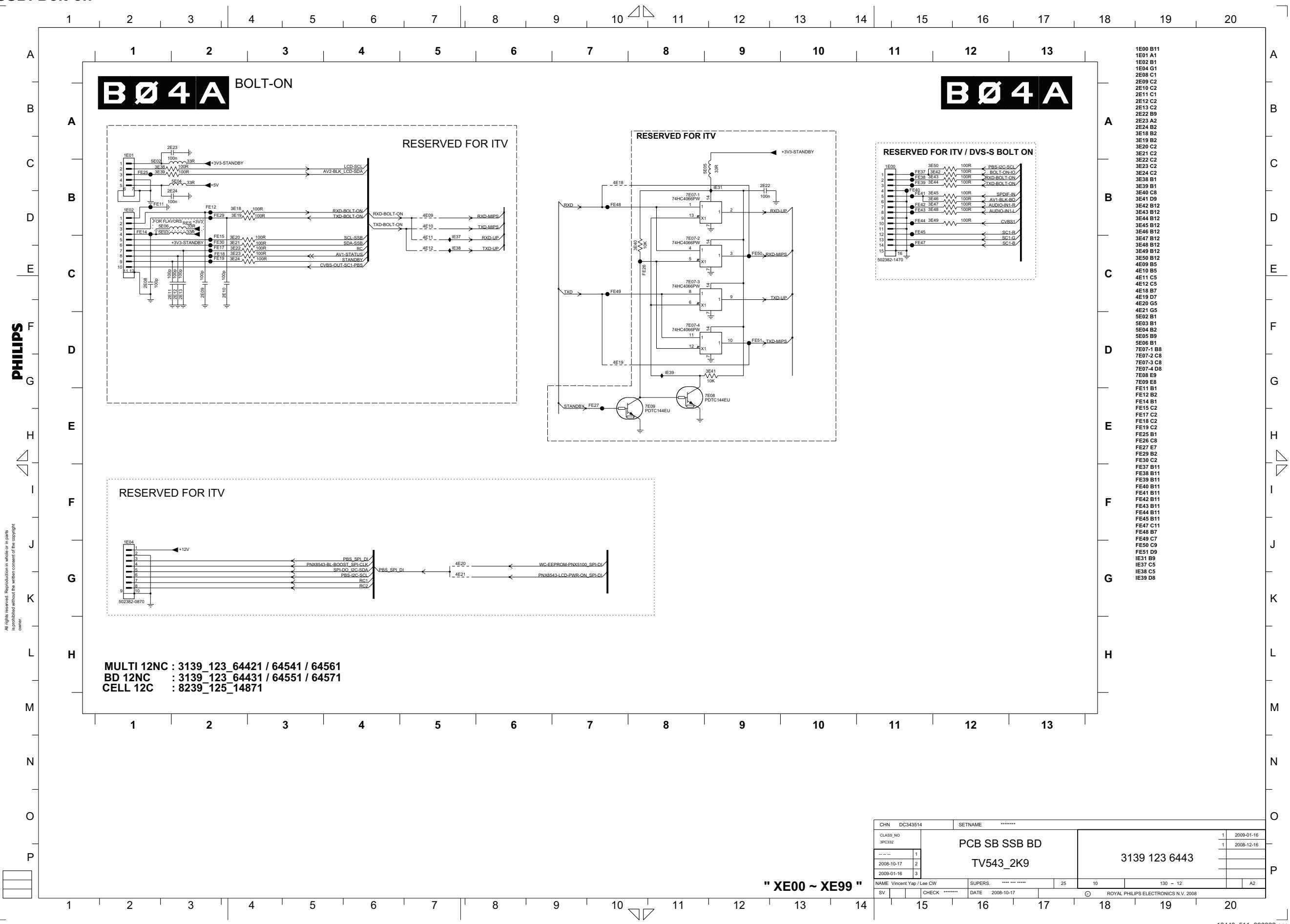




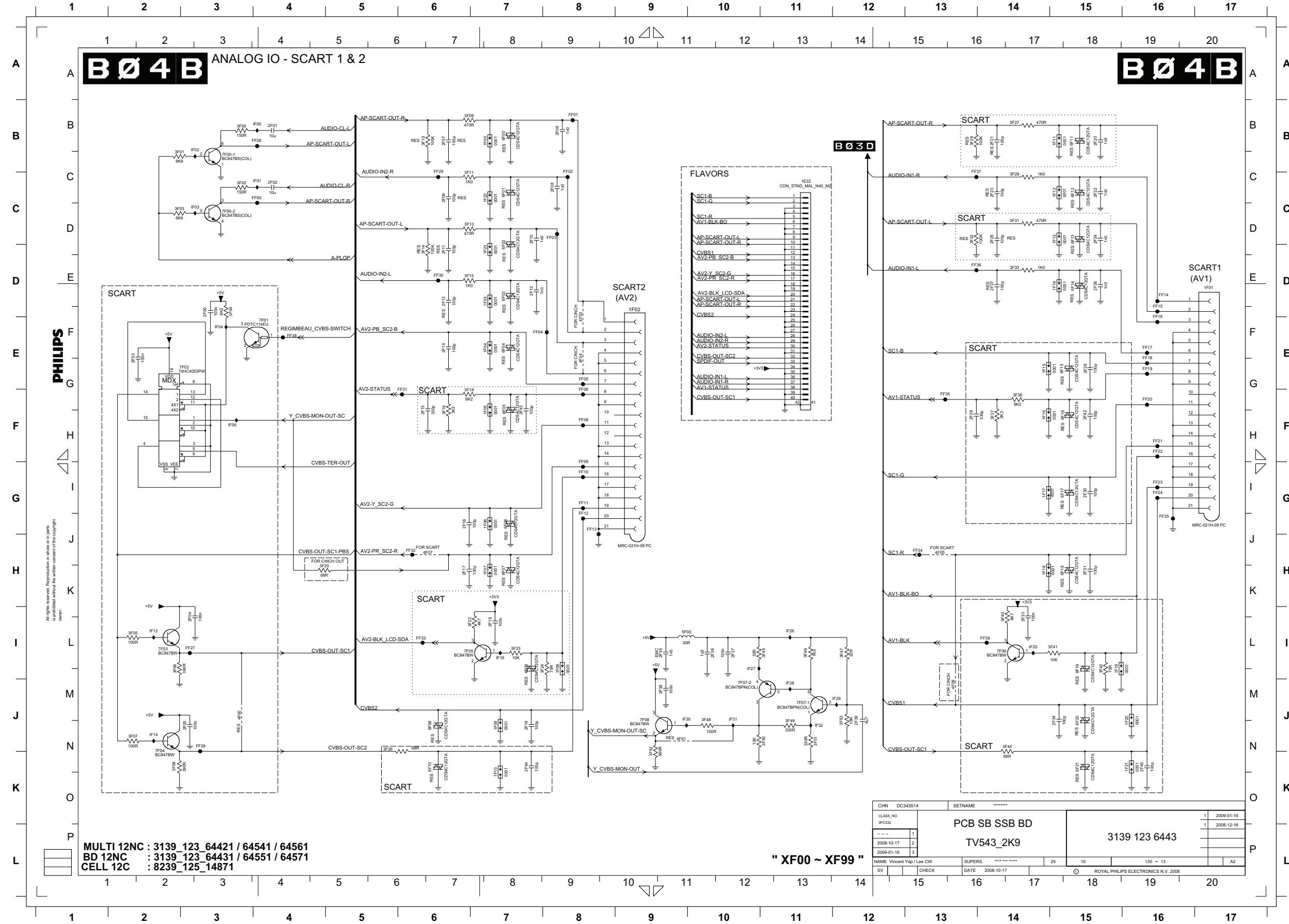
SSB: PNX8543 Standby Control/Debug



SSB: Bolt-on

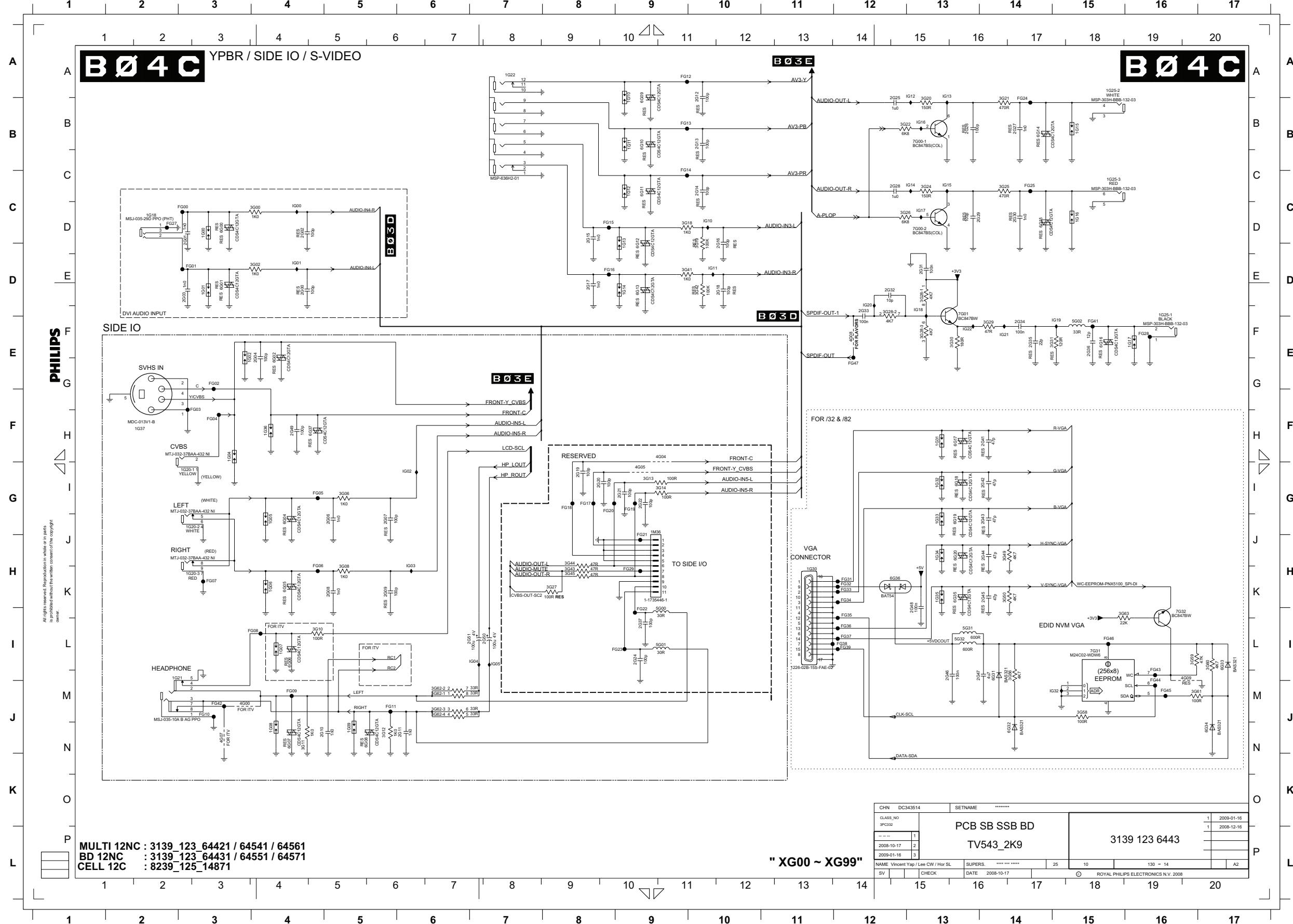


SSB: Analog IO - Scart 1 & 2



1E32 C11 7F04 I2
1F00 B7 7F04 K2
1F02 D1 7F05 J7
1F03 D1 7F07 H4
1F04 E7 7F07-2 J11
1F05 F7 7F08 J9
1F06 G7 4F04 H4
1F07 H8 FF02 E8
1F08 I8 FF03 C8
1F09 J7 FF03 C8
1F10 K7 FF04 E7
1F11 B15 FF04 E8
1F12 F15 FF04 E8
1F13 C15 FF04 F8
1F14 D15 FF05 G8
1F15 E14 FF11 G8
1F16 F14 FF11 G8
1F17 G15 4F04 G8
1F18 H14 FF11 G8
1F19 H15 FF14 D16
1F20 J15 FF15 D16
1F21 K16 FF16 E16
1F22 L16 FF17 F16
1F23 M17 FF18 G16
1F24 N18 FF20 B4
1F25 O19 FF20 G16
1F26 P19 FF20 B4
1F27 Q19 FF20 G16
1F28 R19 FF20 B4
1F29 S19 FF20 G16
1F30 T19 FF20 B4
1F31 U19 FF20 G16
1F32 V19 FF20 B4
1F33 W19 FF20 G16
1F34 X19 FF20 B4
1F35 Y19 FF20 G16
1F36 Z19 FF20 B4
1F37 A19 FF20 G16
1F38 B19 FF20 B4
1F39 C19 FF20 G16
1F40 D19 FF20 B4
1F41 E19 FF20 G16
1F42 F19 FF20 B4
1F43 G19 FF20 G16
1F44 H19 FF20 B4
1F45 I19 FF20 G16
1F46 J19 FF20 B4
1F47 K19 FF20 G16
1F48 L19 FF20 B4
1F49 M19 FF20 G16
1F50 N19 FF20 B4
1F51 O19 FF20 G16
1F52 P19 FF20 B4
1F53 Q19 FF20 G16
1F54 R19 FF20 B4
1F55 S19 FF20 G16
1F56 T19 FF20 B4
1F57 U19 FF20 G16
1F58 V19 FF20 B4
1F59 W19 FF20 G16
1F60 X19 FF20 B4
1F61 Y19 FF20 G16
1F62 Z19 FF20 B4
1F63 A19 FF20 G16
1F64 B19 FF20 B4
1F65 C19 FF20 G16
1F66 D19 FF20 B4
1F67 E19 FF20 G16
1F68 F19 FF20 B4
1F69 G19 FF20 G16
1F70 H19 FF20 B4
1F71 I19 FF20 G16
1F72 J19 FF20 B4
1F73 K19 FF20 G16
1F74 L19 FF20 B4
1F75 M19 FF20 G16
1F76 N19 FF20 B4
1F77 O19 FF20 G16
1F78 P19 FF20 B4
1F79 Q19 FF20 G16
1F80 R19 FF20 B4
1F81 S19 FF20 G16
1F82 T19 FF20 B4
1F83 U19 FF20 G16
1F84 V19 FF20 B4
1F85 W19 FF20 G16
1F86 X19 FF20 B4
1F87 Y19 FF20 G16
1F88 Z19 FF20 B4
1F89 A19 FF20 G16
1F90 B19 FF20 B4
1F91 C19 FF20 G16
1F92 D19 FF20 B4
1F93 E19 FF20 G16
1F94 F19 FF20 B4
1F95 G19 FF20 G16
1F96 H19 FF20 B4
1F97 I19 FF20 G16
1F98 J19 FF20 B4
1F99 K19 FF20 G16

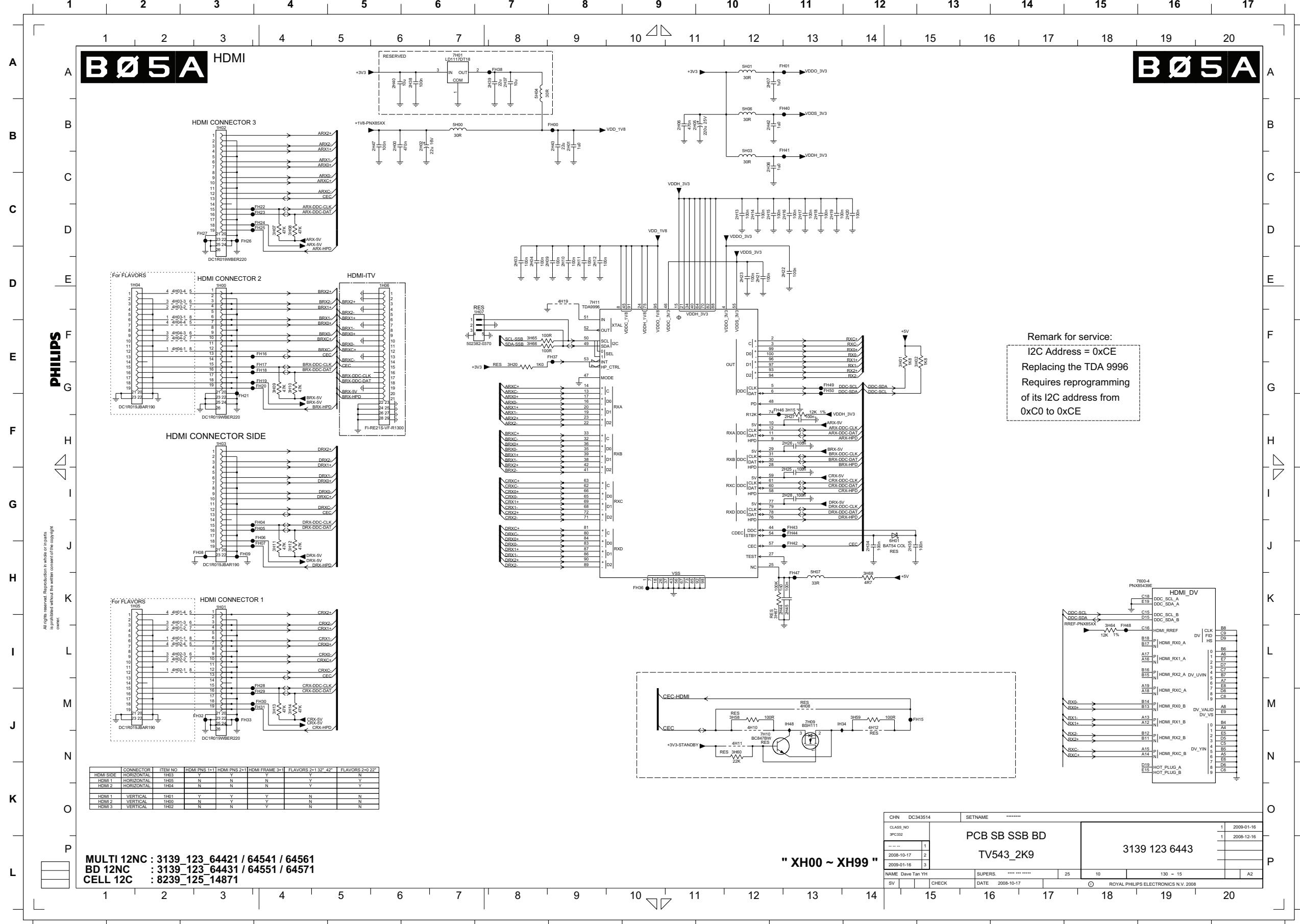
SSB: YPbPr / Side I/O / S-video



1G00 C3 6G12 C9
1G01 D3 6G13 D9
1G02 E3 6G14 B14
1G03 F3 6G15 C14
1G05 G4 6G16 E15
1G06 H4 6G17 F15
1G07 I4 6G18 G13
1G09 J5 6G19 H13
1G10 A9 6G21 I14
1G11 B9 6G22 J14
1G12 C9 6G31 H17
1G13 D9 6G32 H13
1G15 H15 6G33 H12
1G16 E15 6G37 F4
1G17 E16 7G00-1 B13
1G18 C2 7G01-1 C13
1G20-2 G3 7G31 H15
1G20-3 H3 7G32 H16
1G21 I2 FG00 C3
1G22 A7 FG01 D3
1G23 B7 FG02 E3
1G25-2 WHITE MSP-303H-BBB-132-03
1G25-3 RED MSP-303H-BBB-132-03
1G25-1 BLACK MSP-303H-BBB-132-03
1G26-1 10K 1G26-2 10K
1G27-1 10K 1G27-2 10K
1G28-1 10K 1G28-2 10K
1G29-1 10K 1G29-2 10K
1G30-1 10K 1G30-2 10K
1G31-1 10K 1G31-2 10K
1G32-1 10K 1G32-2 10K
1G33-1 10K 1G33-2 10K
1G34-1 10K 1G34-2 10K
1G35-1 10K 1G35-2 10K
1G36-1 10K 1G36-2 10K
1G37-1 10K 1G37-2 10K
1G38-1 10K 1G38-2 10K
1G39-1 10K 1G39-2 10K
1G40-1 10K 1G40-2 10K
1G41-1 10K 1G41-2 10K
1G42-1 10K 1G42-2 10K
1G43-1 10K 1G43-2 10K
1G44-1 10K 1G44-2 10K
1G45-1 10K 1G45-2 10K
1G46-1 10K 1G46-2 10K
1G47-1 10K 1G47-2 10K
1G48-1 10K 1G48-2 10K
1G49-1 10K 1G49-2 10K
1G50-1 10K 1G50-2 10K
1G51-1 10K 1G51-2 10K
1G52-1 10K 1G52-2 10K
1G53-1 10K 1G53-2 10K
1G54-1 10K 1G54-2 10K
1G55-1 10K 1G55-2 10K
1G56-1 10K 1G56-2 10K
1G57-1 10K 1G57-2 10K
1G58-1 10K 1G58-2 10K
1G59-1 10K 1G59-2 10K
1G60-1 10K 1G60-2 10K
1G61-1 10K 1G61-2 10K
1G62-1 10K 1G62-2 10K
1G63-1 10K 1G63-2 10K
1G64-1 10K 1G64-2 10K
1G65-1 10K 1G65-2 10K
1G66-1 10K 1G66-2 10K
1G67-1 10K 1G67-2 10K
1G68-1 10K 1G68-2 10K
1G69-1 10K 1G69-2 10K
1G70-1 10K 1G70-2 10K
1G71-1 10K 1G71-2 10K
1G72-1 10K 1G72-2 10K
1G73-1 10K 1G73-2 10K
1G74-1 10K 1G74-2 10K
1G75-1 10K 1G75-2 10K
1G76-1 10K 1G76-2 10K
1G77-1 10K 1G77-2 10K
1G78-1 10K 1G78-2 10K
1G79-1 10K 1G79-2 10K
1G80-1 10K 1G80-2 10K
1G81-1 10K 1G81-2 10K
1G82-1 10K 1G82-2 10K
1G83-1 10K 1G83-2 10K
1G84-1 10K 1G84-2 10K
1G85-1 10K 1G85-2 10K
1G86-1 10K 1G86-2 10K
1G87-1 10K 1G87-2 10K
1G88-1 10K 1G88-2 10K
1G89-1 10K 1G89-2 10K
1G90-1 10K 1G90-2 10K
1G91-1 10K 1G91-2 10K
1G92-1 10K 1G92-2 10K
1G93-1 10K 1G93-2 10K
1G94-1 10K 1G94-2 10K
1G95-1 10K 1G95-2 10K
1G96-1 10K 1G96-2 10K
1G97-1 10K 1G97-2 10K
1G98-1 10K 1G98-2 10K
1G99-1 10K 1G99-2 10K

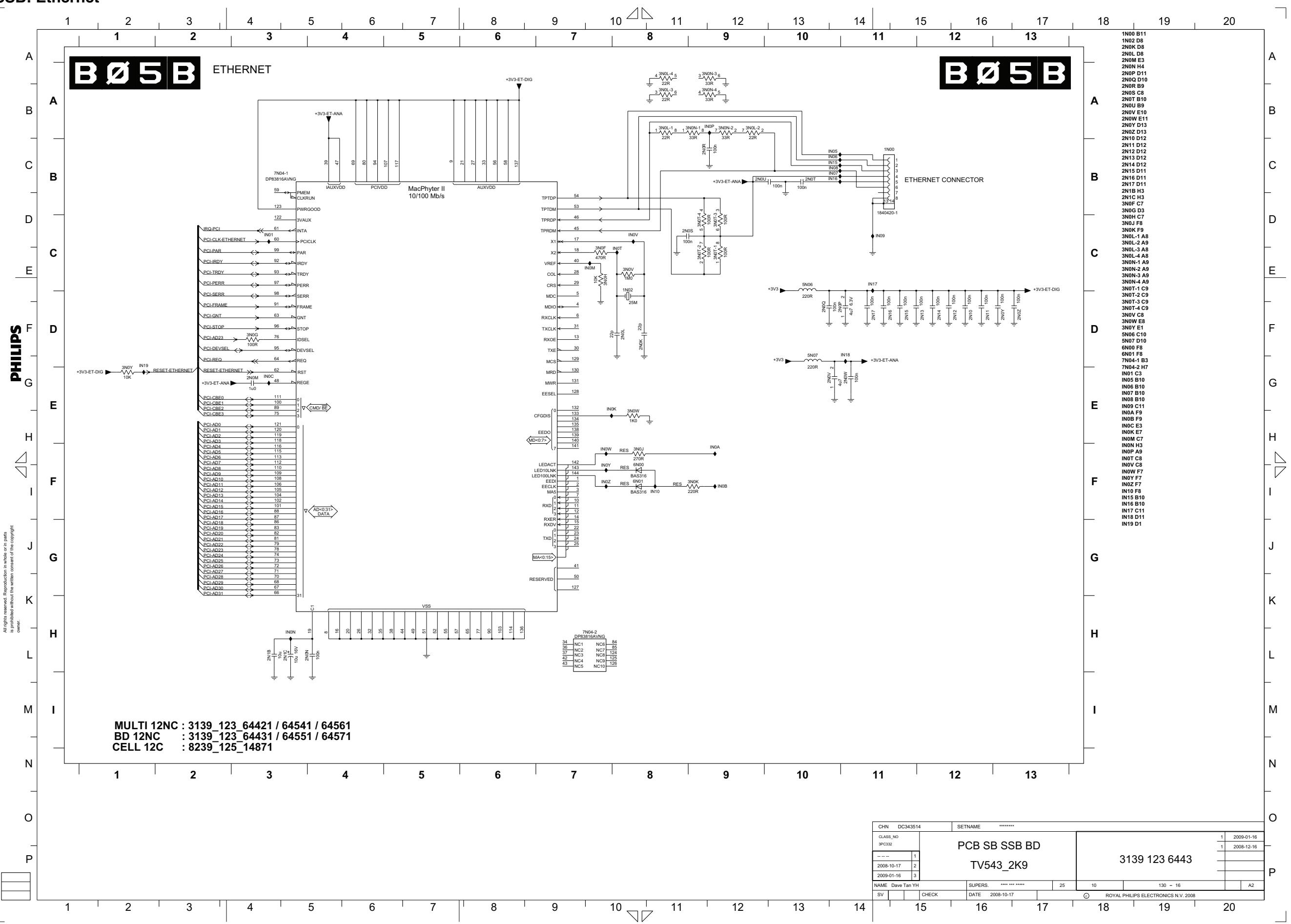
CHN DC343514		SETNAME	
CLASS_NO	3PC32		
-----	1		
2008-10-17	2		
2009-01-16	3		
		PCB SB SSB BD	
		TV543_2K9	
		3139 123 6443	
NAME	Vincent Yap / Lee CW / Hor SL	SUPERS	
SV	CHECK	DATE	2008-10-17
			ROYAL PHILIPS ELECTRONICS N.V. 2008
			A2

SSB: HDMI



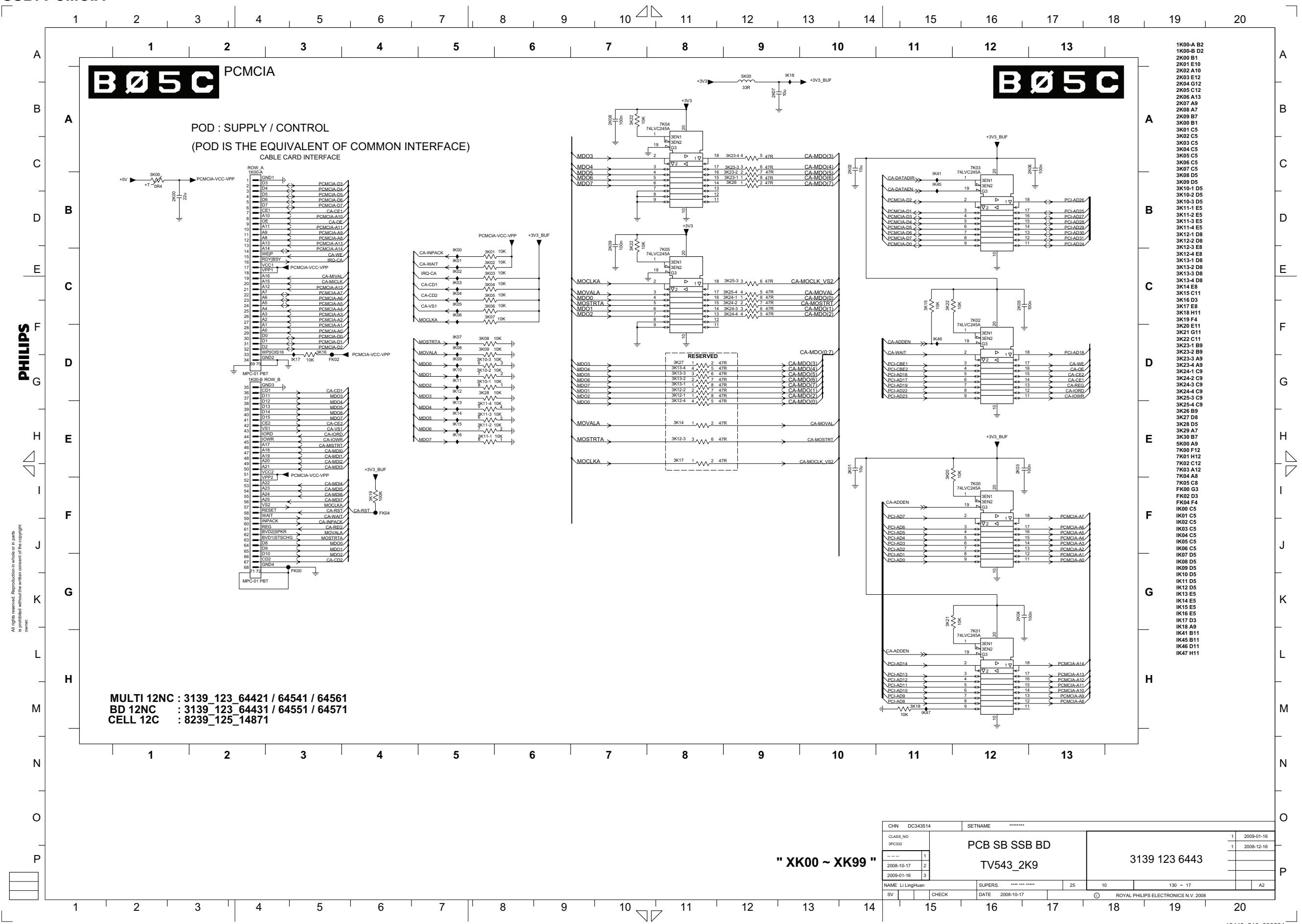
1H00_D3
1H01_H3
1H02_A3
1H03_F3
1H04_L2
1H05_H2
1H06_D5
1H07_D7
1H08_S5
1H09_B6
2H03_D7
2H04_D7
2H05_B10
2H06_B5
2H07_A11
2H08_D8
2H10_D8
2H11_D8
2H12_D8
2H13_C10
2H14_C10
2H15_C11
2H16_C11
2H17_C11
2H18_C11
2H19_C11
2H20_C12
2H21_D10
2H22_D11
2H23_G11
2H24_F11
2H25_G11
2H26_H12
2H27_B11
2H28_A7
2H29_A6
2H30_B11
2H31_G15
2H32_H11
2H33_B5
3H01_E12
3H02_E13
3H03_E4
3H04_C4
3H05_E4
3H10_E4
3H11_G4
3H12_G4
3H13_H4
3H14_I4
3H15_F11
3H20_E7
3H58_J10
3H62_J12
3H63_J10
3H64_I15
3H65_E7
3H66_E7
3H67_H11
3H68_I12
4H01_I2_H2
4H01_I2_H3
4H01_I2_H4
4H02_I2_I2
4H03_I2_H2
4H03_I2_D2
4H03_S2
4H04_I2_H2
4H04_I2_D2
4H04_I3_D2
4H04_I4_D2
4H04_I5_D2
4H05_I1
4H10_I10
5H04_A7
5H05_B10
5H07_H11
6H01_G12
7H00_H16
7H01_A5
7H09_J11
7H10_J10
7H11_D8
FH09_B8
FH10_H11
FH04_G4
FH05_G4
FH07_G4
FH08_G3
FH09_G3
FH11_J13
FH12_D4
FH17_E4
FH18_E4
FH19_E4
FH20_E4
FH21_E3
FH22_B4
FH23_C4
FH24_C4
FH25_C3
FH26_C3
FH27_C3
FH28_I4
FH29_I4
FH30_I4
FH31_I4
FH32_I3
FH33_I3
FH34_H9
FH35_A7
FH41_B11
FH42_H11
FH43_G11
FH44_G11
FH45_H11
FH46_H11
FH47_E11
FH48_E11
FH50_E11
IH34_J11
IH48_J11

SSB: Ethernet

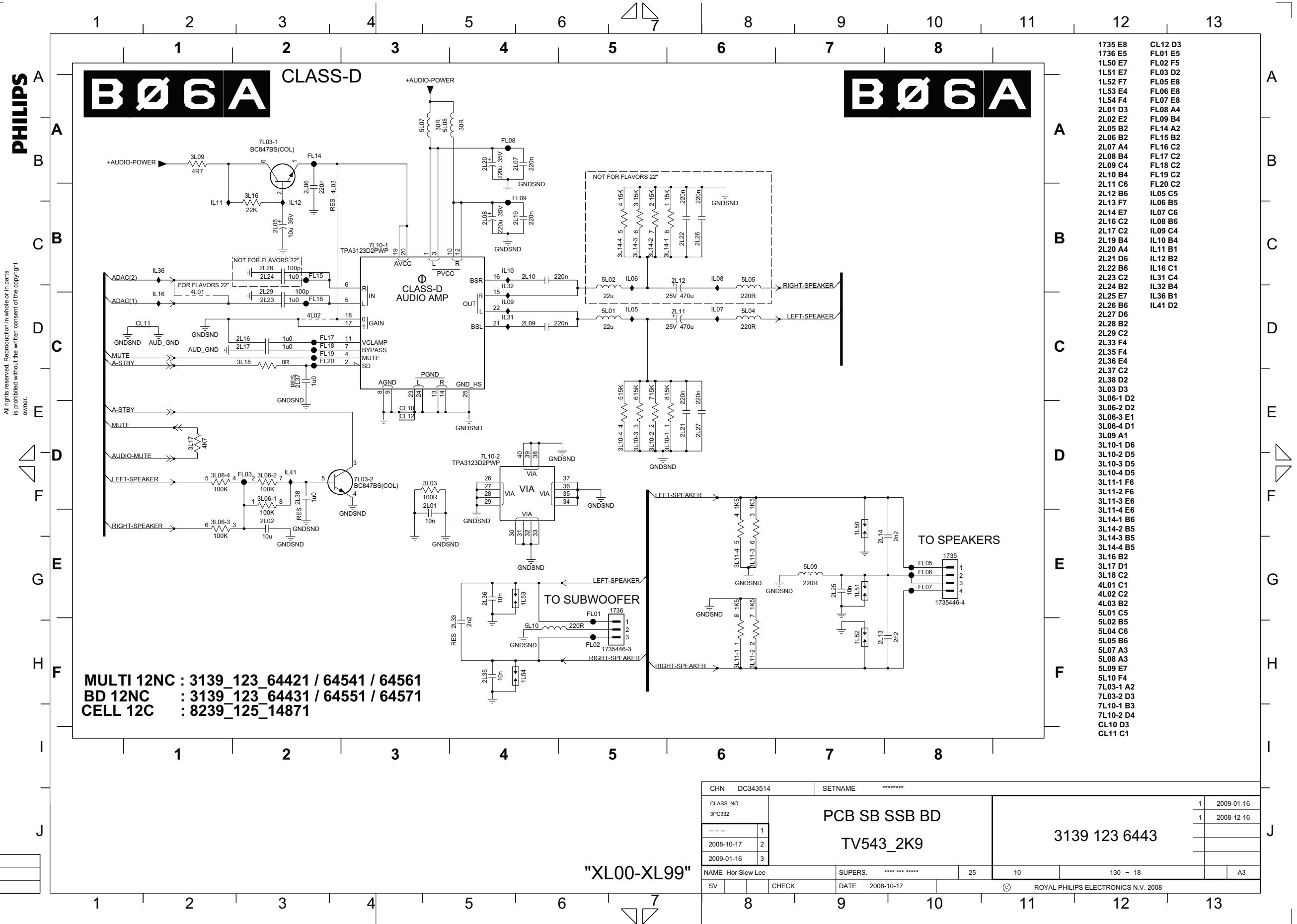




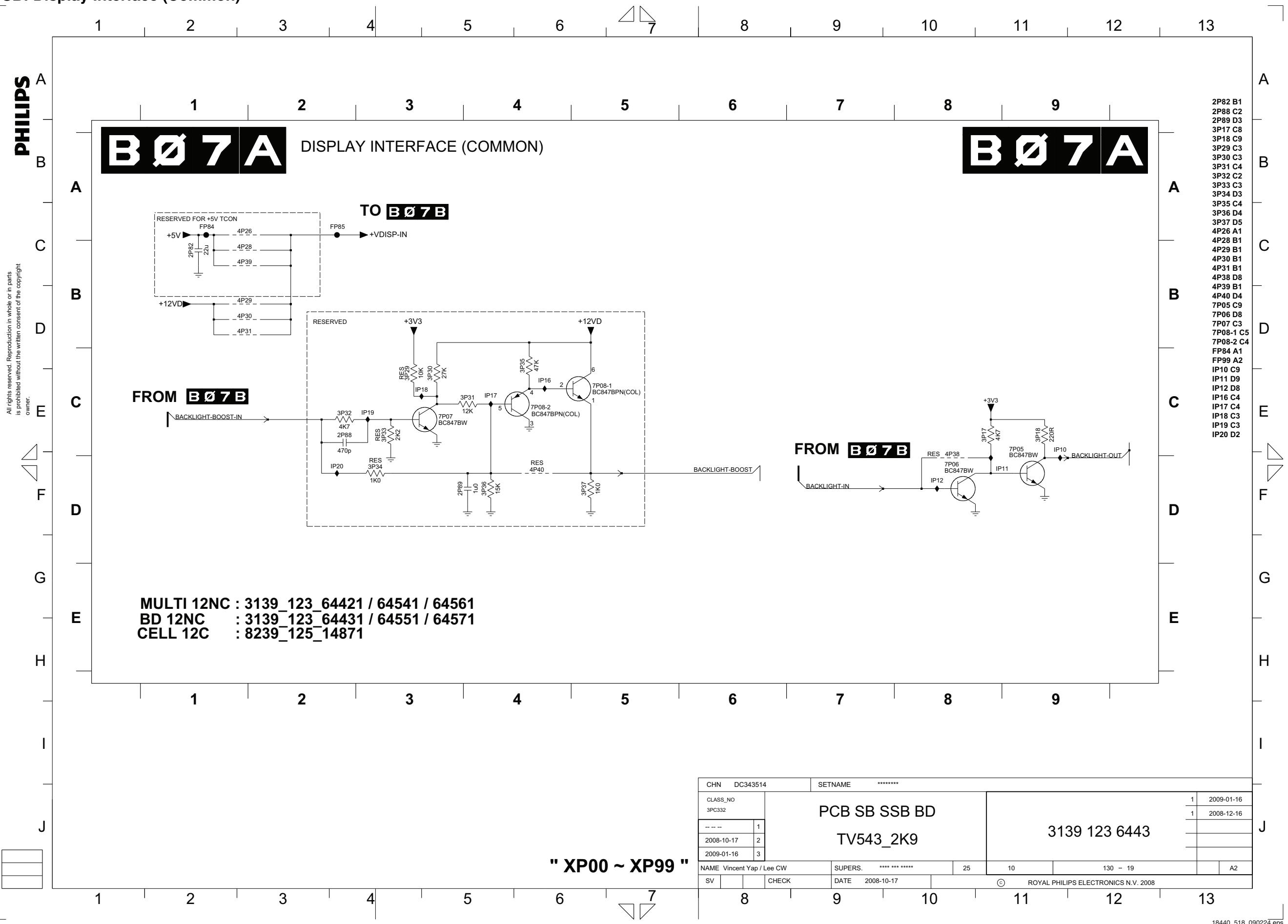
SSB: PCMCIA



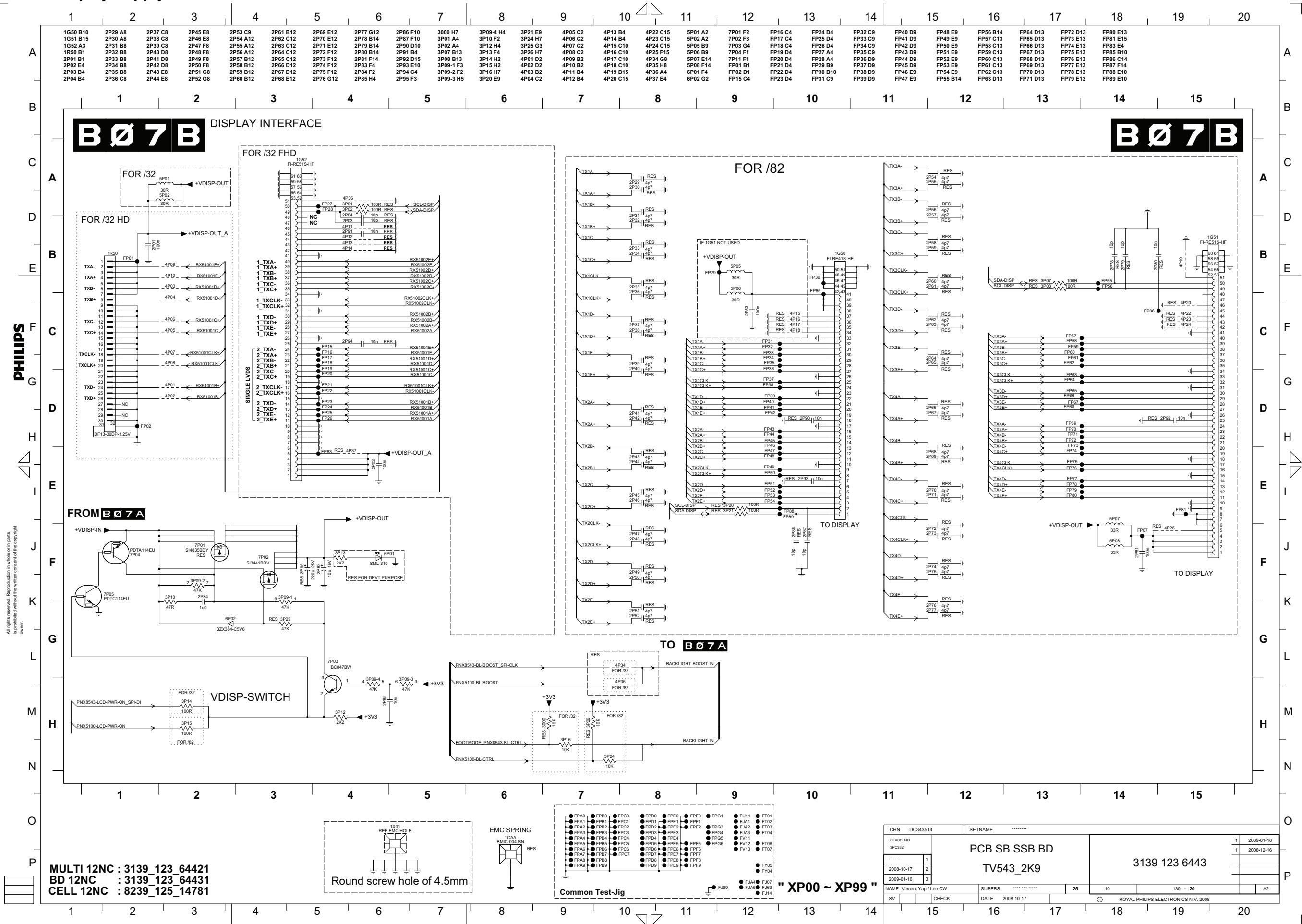
SSB: Class-D



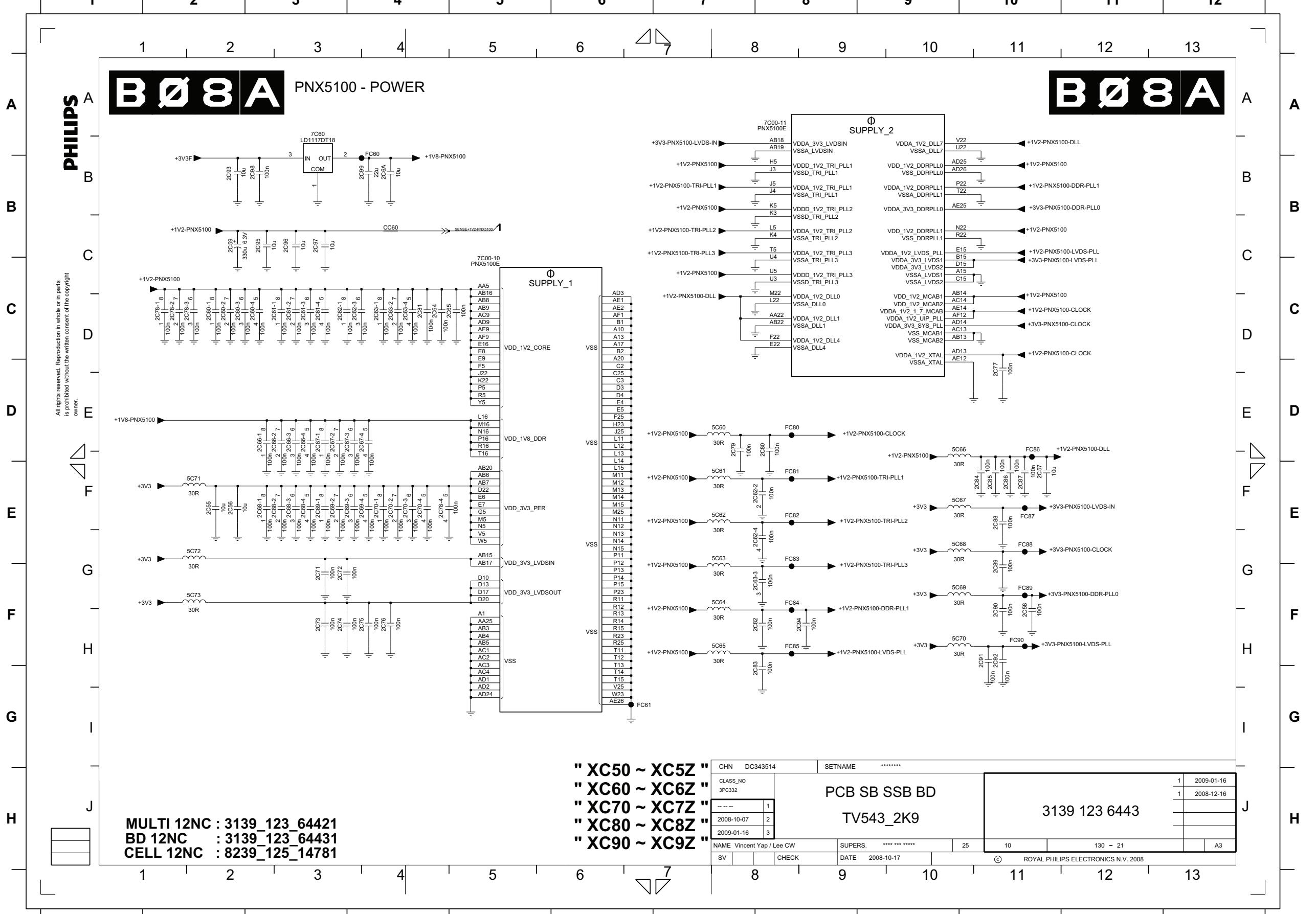
SSB: Display Interface (Common)



SSB: Display Supply

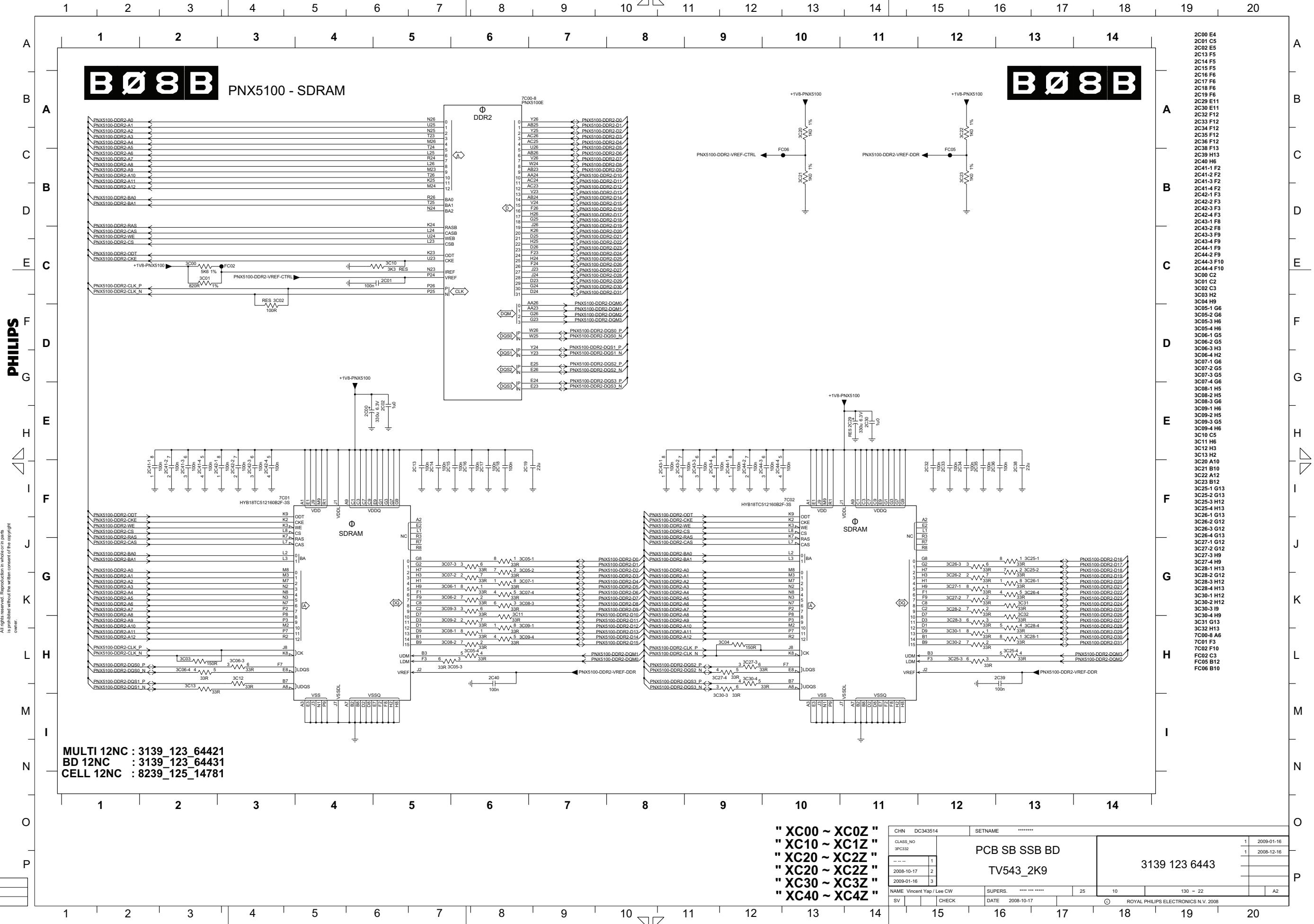


SSB: PNX5100 - Power

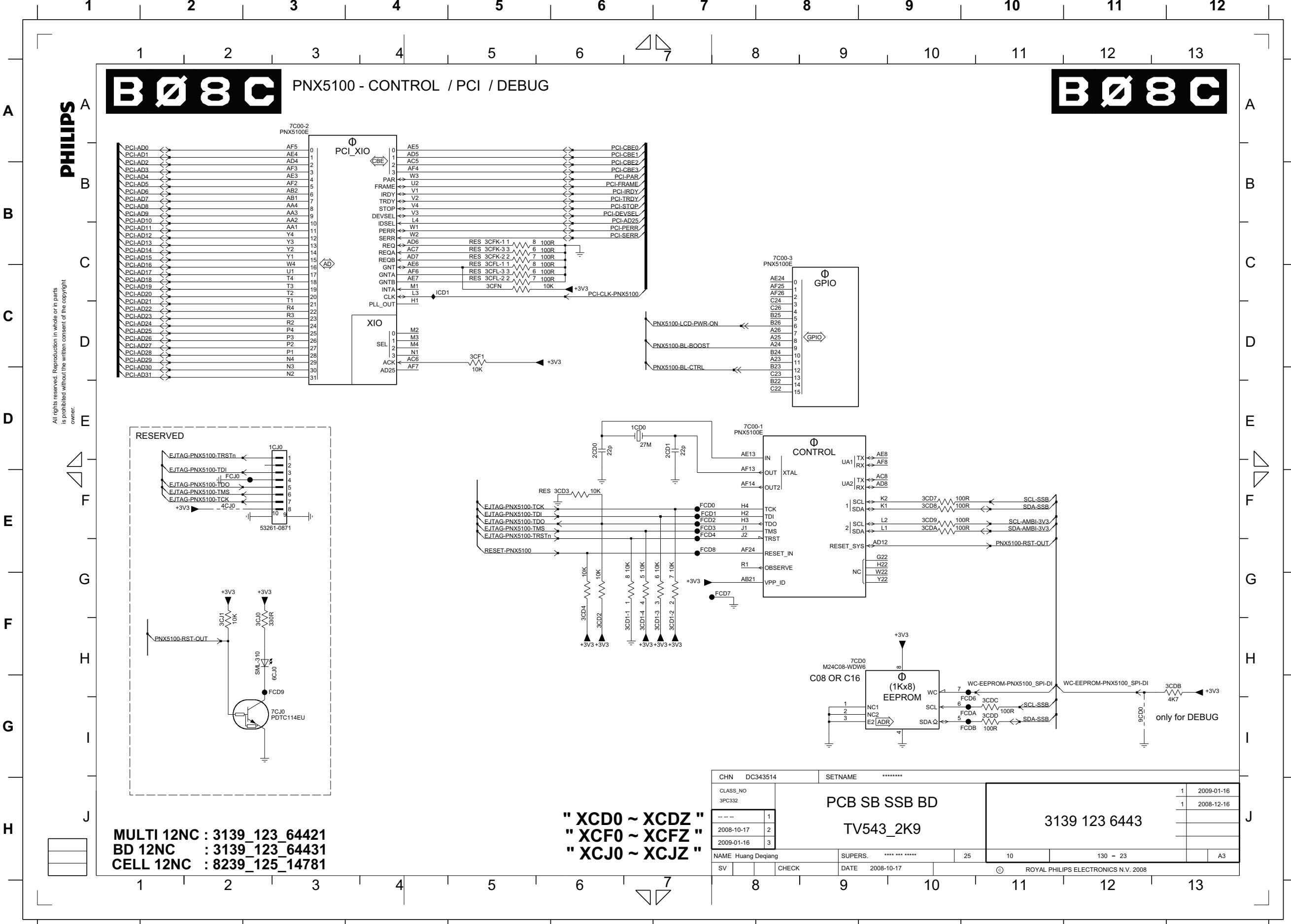


2C55 E2
2C56 E2
2C57 E10
2C58 F10
2C59 B2
2C60-1 C2
2C60-2 C2
2C60-3 C2
2C60-4 C3
2C61-1 C3
2C61-2 C3
2C61-3 C3
2C61-4 C3
2C62-1 C3
2C62-2 E8
2C62-3 C4
2C62-4 E8
2C63-1 C4
2C63-2 C4
2C63-3 F8
2C63-4 C4
2C64 C4
2C65 C5
2C66-1 D3
2C66-2 D3
2C66-3 D3
2C66-4 D3
2C67-1 D3
2C67-2 D3
2C67-3 D4
2C67-4 D4
2C68-1 E3
2C68-2 E3
2C68-3 E3
2C68-4 E3
2C69-1 E3
2C69-2 E3
2C69-3 E4
2C69-4 E4
2C6A B4
2C70-1 E4
2C70-2 E4
2C70-3 E4
2C70-4 E4
2C71 F3
2C72 F3
2C73 F3
2C74 F3
2C75 F4
2C76 F4
2C77 D10
2C78-1 C2
2C78-2 C2
2C78-3 C2
2C78-4 E4
2C79 D7
2C80 D8
2C81 C4
2C82 F8
2C83 G8
2C84 E10
2C85 E10
2C86 E10
2C87 E10
2C88 E10
2C89 F10
2C90 F10
2C91 F10
2C92 F10
2C93 B2
2C94 F8
2C95 B3
2C96 B3
2C97 B3
2C98 B3
2C99 B4
5C60 D7
5C61 E7
5C62 E7
5C63 E7
5C64 F7
5C65 F7
5C66 D10
5C67 E10
5C68 E10
5C69 F10
5C70 F10
5C71 E2
5C72 E2
5C73 F2
7C00-10 C5
7C00-11 A8
7C60 A3
CC60 B4
FC60 B4
FC61 G6
FC80 D8
FC81 E8
FC82 E8
FC83 E8
FC84 F8
FC85 F8
FC86 D10
FC87 E10

SSB: PNX5100 - SDRAM

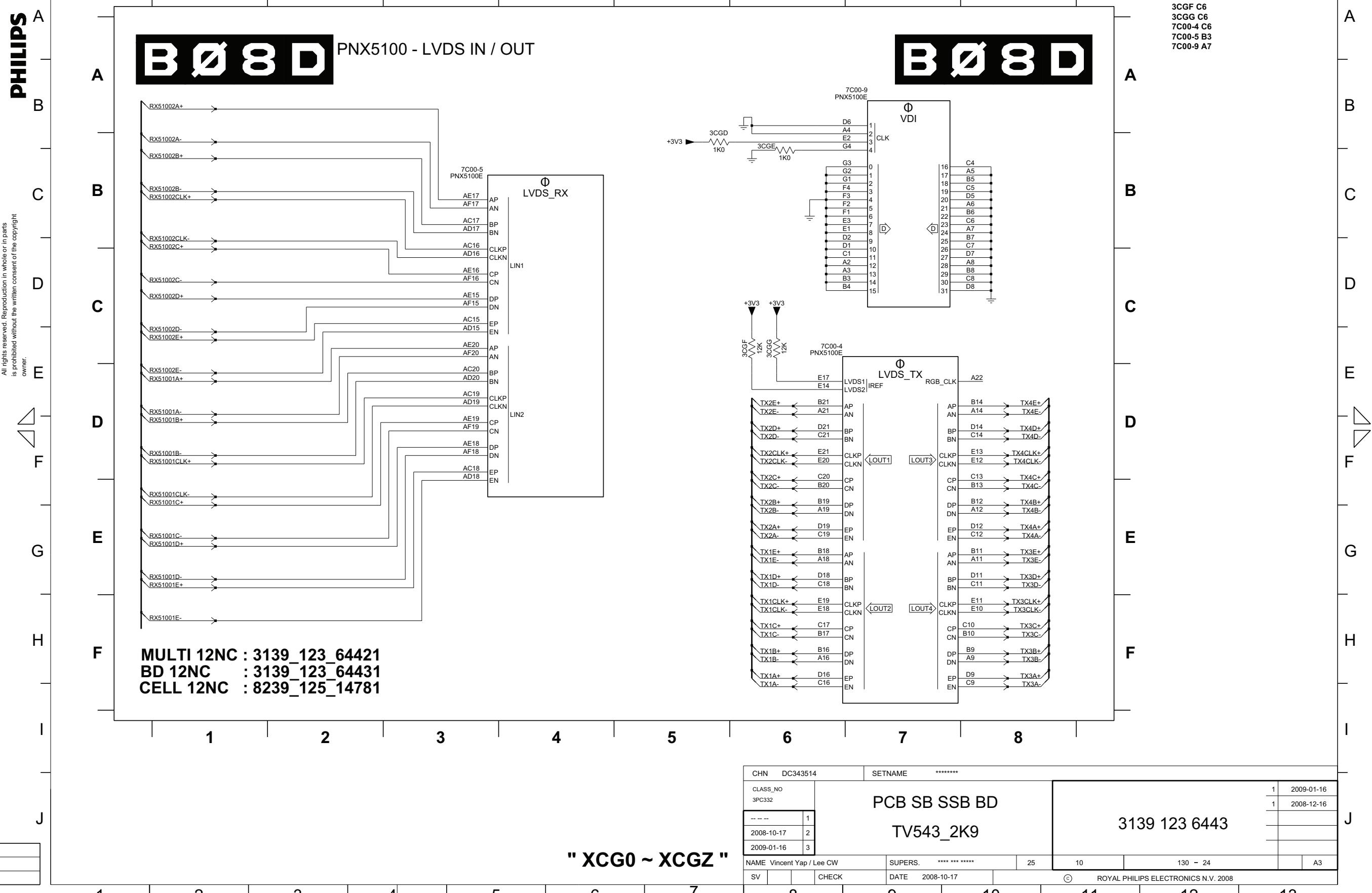


SSB: PNX5100 - Control / PCI / Debug

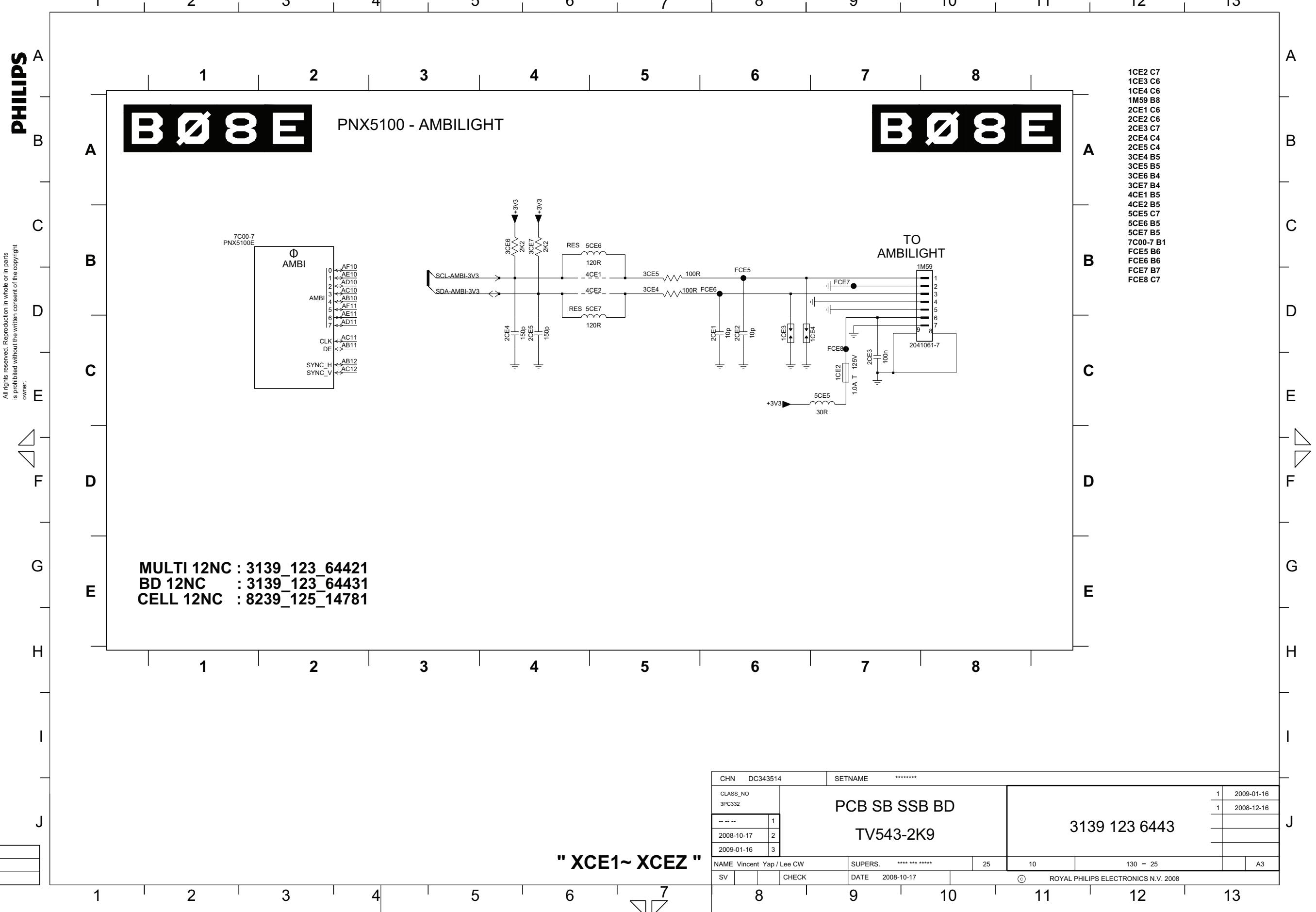


1CD0 D6
1CJ0 D3
2CD0 D6
2CD1 D7
3CD1-2 F7
3CD1-3 F7
3CD1-4 F6
3CD2 F6
3CD3 E6
3CD4 F6
3CD7 E9
3CD8 E9
3CD9 E9
3CDA E9
3CDB G12
3CDC G10
3CDD G10
3CF1 C5
3CFK-1 B5
3CFK-2 B5
3CFK-3 B5
3CFL-1 C5
3CFL-2 C5
3CFL-3 C5
3CJ0 F3
3CJ1 F2
4CJ0 E2
6CJ0 F3
7C00-1 D8
7C00-2 A3
7C00-3 B8
7CD0 F9
7CJ0 G3
9CD0 G11
FCD0 E7
FCD1 E7
FCD2 E7
FCD3 E7
FCD4 E7
FCD6 G10
FCD7 F7
FCD8 E7
FCDA G3
FCDB G10
FCJ0 E2
ICD1 C4

SSB: PNX5100 - LVDS In/Out



SSB: PNX5100 - AmbiLight



SSB: SRP List Explanation

Example

Net Name	Diagram
+12-15V	AP1 (4x)
+12-15V	AP4 (4x)
+12-15V	AP5 (12x)
+12-15V	AP6 (4x)
+12-15V	AP7 (8x)
+12V	AP1 (4x)
+12V_NF	AP1 (2x)
+12V_AL	AP1 (2x)
+25VLP	AP1 (4x)
+3VS-STANDBY	AP2 (1x)
+400V-F	AP5 (3x)
+400V-F	AP1 (2x)
+400V-F	AP3 (2x)
+5V2	AP1 (6x)
+5V2	AP2 (1x)
+5V2-NF	AP1 (1x)
+5V2-NF	AP2 (1x)
+5V-SW	AP1 (6x)
+5V-SW	AP2 (1x)
+8V6	AP1 (3x)
+AUX	AP1 (2x)
+AUX	AP2 (1x)
+DC-F	AP1 (2x)
+DC-F	AP3 (2x)
+SUB-SPEAKER	AP5 (1x)
+SUB-SPEAKER	AP6 (2x)
-12-15V	AP1 (4x)
-12-15V	AP4 (6x)
-12-15V	AP5 (14x)
-12-15V	AP6 (6x)
-12-15V	AP7 (6x)
-AL-GND	AP1 (2x)
AUDIO-L	AP4 (1x)
AUDIO-L	AP5 (1x)
AUDIO-PROT	AP5 (3x)
AUDIO-R	AP4 (1x)
AUDIO-R	AP5 (1x)
AUDIO-SW	AP5 (1x)
AUDIO-SW	AP7 (1x)
BOOST	AP1 (2x)
C-PROT	AP4 (2x)
C-PROT	AP5 (1x)
C-PROT-SW	AP5 (1x)
C-PROT-SW	AP6 (2x)
-DC-F	AP1 (2x)
-DC-F	AP3 (2x)
-DC-PROT	AP1 (1x)
-DC-PROT	AP5 (2x)
DIM-CONTROL	AP1 (2x)
FEEDBACK+SW	AP6 (2x)
FEEDBACK-L	AP4 (2x)
FEEDBACK-R	AP4 (2x)
FEEDBACK-SW	AP6 (2x)
GND-FA	AP1 (2x)
GND-HA	AP1 (40x)
GND-HA	AP2 (20x)
GND-HA	AP3 (2x)
GND-LOT	AP1 (2x)
GND-L	AP4 (2x)
GND-L	AP5 (4x)
GND-L	AP5 (34x)
GND-LL	AP4 (7x)
GND-LL	AP5 (1x)
GND-LR	AP4 (7x)
GND-LR	AP5 (1x)
GND-LSW	AP5 (1x)
GND-LSW	AP6 (15x)
GND-S	AP1 (11x)
GND-SA	AP4 (8x)
GND-SA	AP5 (2x)
GND-SA	AP6 (8x)
GND-SA	AP7 (6x)
GND-screw	AP3 (2x)
GNDscrew	AP5 (2x)
GND-SSB	AP5 (3x)
GND-SSB	AP1 (51x)
GND-SSB	AP2 (15x)
IN-SW	AP6 (2x)
IN-R	AP2 (2x)
IN-SW	AP4 (2x)
IN-R	AP6 (2x)
INV-MUTE	AP4 (1x)
INV-MUTE	AP5 (1x)
INV-MUTE	AP6 (1x)
LEFT-SPEAKER	AP4 (1x)
LEFT-SPEAKER	AP5 (1x)
MUTE	AP4 (2x)
MUTE	AP5 (1x)
MUTE	AP6 (2x)
ON-OFF	AP1 (3x)
OUT	AP6 (1x)
OUT	AP7 (2x)
OUTN	AP6 (1x)
OUTN	AP7 (1x)
POWER-GOOD	AP1 (2x)
POWER-OK-PLATFORM	AP1 (2x)
RIGHT-SPEAKER	AP4 (1x)
RIGHT-SPEAKER	AP5 (1x)
SOUND-ENABLE	AP5 (3x)
STANDBY	AP1 (5x)
STANDBY	AP2 (1x)
-SUB-SPEAKER	AP5 (1x)
-SUB-SPEAKER	AP6 (2x)
V-CLAMP	AP1 (1x)
V-CLAMP	AP3 (2x)

1.1. Introduction

SRP (Service Reference Protocol) is a software tool that creates a list with all references to signal lines. The list contains references to the signals within all schematics of a PWB. It replaces the text references currently printed next to the signal names in the schematics. These printed references are created manually and are therefore not guaranteed to be 100% correct. In addition, in the current crowded schematics there is often none or very little place for these references. Some of the PWB schematics will use SRP while others will still use the manual references. Either there will be an SRP reference list for a schematic, or there will be printed references in the schematic.

1.2. Non-SRP Schematics

There are several different signals available in a schematic:

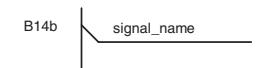
1.2.1. Power Supply Lines

All power supply lines are available in the supply line overview (see chapter 6). In the schematics (see chapter 7) is not indicated where supplies are coming from or going to. It is however indicated if a supply is incoming (created elsewhere), or outgoing (created or adapted in the current schematic).



1.2.2. Normal Signals

For normal signals, a schematic reference (e.g. B14b) is placed next to the signals.

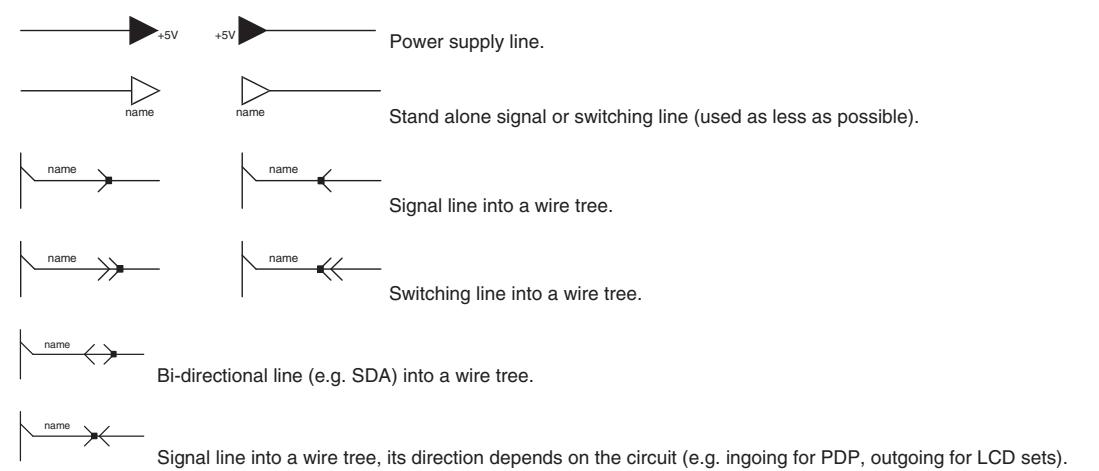


1.2.3. Grounds

For normal and special grounds (e.g. GNDHOT or GND3V3 etc.), nothing is indicated.

1.3. SRP Schematics

SRP is a tool, which automatically creates a list with signal references, indicating on which schematic the signals are used. A reference is created for all signals indicated with an SRP symbol, these symbols are:



Remarks:

- When there is a black dot on the "signal direction arrow" it is an SRP symbol, so there will be a reference to the signal name in the SRP list.
- All references to normal grounds (Ground symbols without additional text) are not listed in the reference list, this to keep it concise.
- Signals that are not used in multiple schematics, but only once or several times in the same schematic, are included in the SRP reference list, but only with one reference.

Additional Tip:

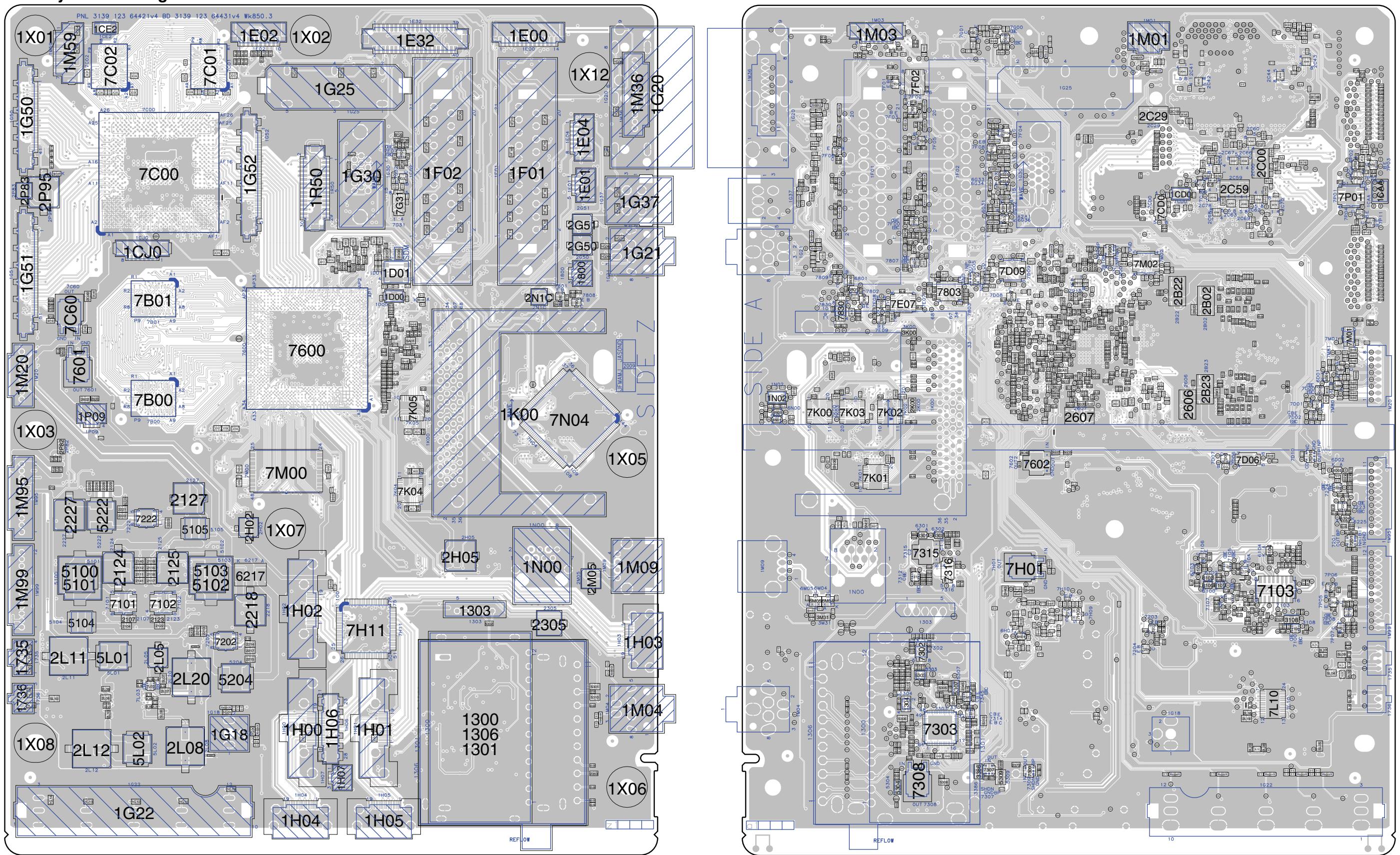
When using the PDF service manual file, you can very easily search for signal names and follow the signal over all the schematics. In Adobe PDF reader:

- Select the signal name you want to search for, with the "Select text" tool.
- Copy and paste the signal name in the "Search PDF" tool.
- Search for all occurrences of the signal name.
- Now you can quickly jump between the different occurrences and follow the signal over all schematics. It is advised to "zoom in" to e.g. 150% to see clearly, which text is selected. Then you can zoom out, to get an overview of the complete schematic.

PS. It is recommended to use at least Adobe PDF (reader) version 6.x, due to better search possibilities in this version.

Personal Notes:

Layout Small Signal Board



31391236443.1

18540_550_090311.eps
090320