KEY FEATURES

- ■ DVB-S / DIRECTV™ system
- ■ Fast channel acquisition
- ■ Up to 60 Msps operation

INTERFACES

- ■ DVB common interface compliant transport stream (12 bit)
- ■ I²C serial bus interface, including private repeater

- ■ DiSEqC 2.0 22 kHz to 100 kHz interface
- ■ Flexible GPIOs and interrupts
- ■ Monitoring through I2C serial interface

TECHNOLOGY

- ■ 90nm CMOS process
- ■ Multi supply: 1.0 V core, 2.5 V analog, 3.3 V interfaces
- ■ Power saving features
- ■ 1.0 V DC regulator integrated
- ■ TQFP 64 package with no exposed pad

Figure 1: STV0288 block diagram
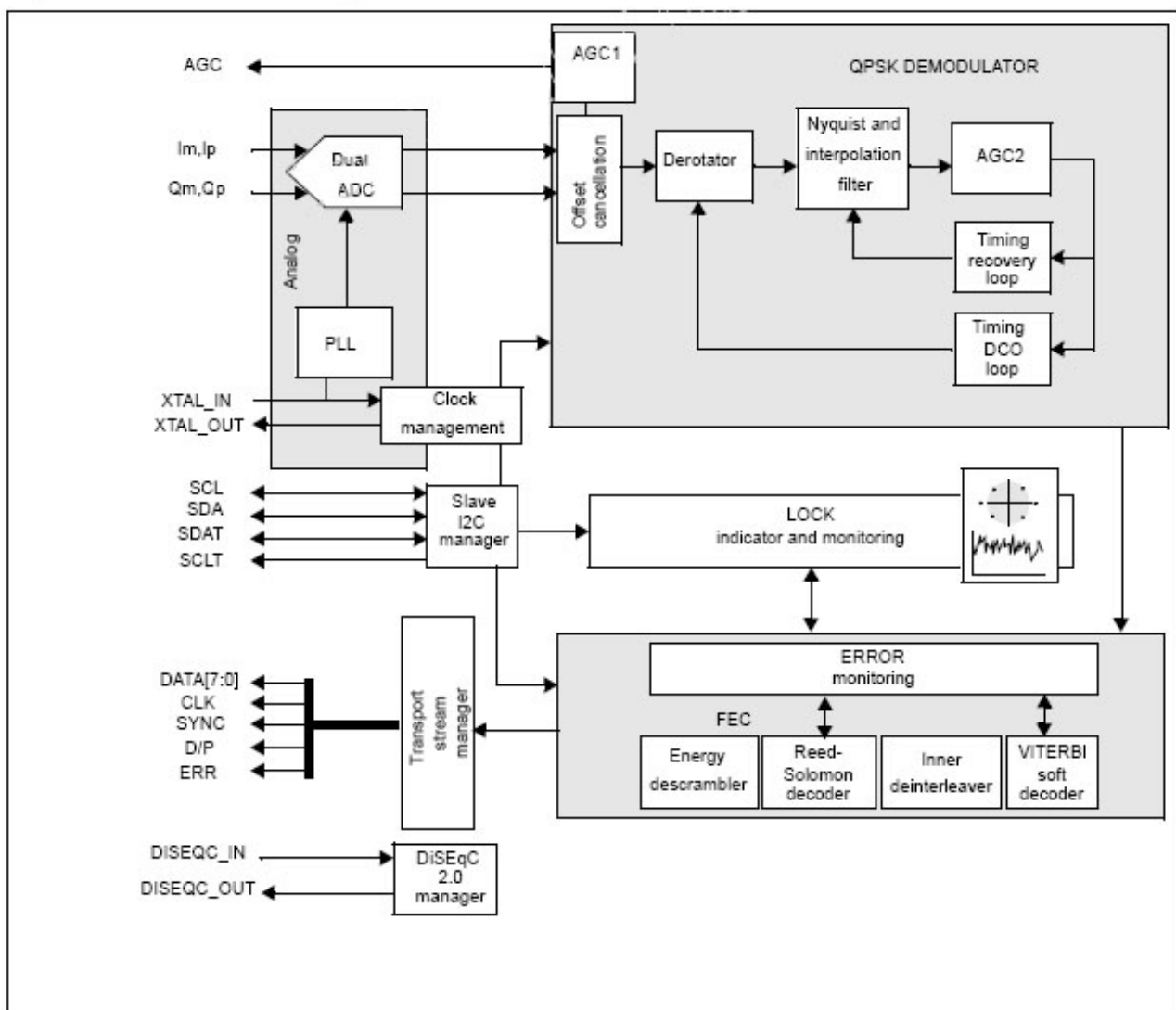
FAST CHANNEL ACQUISITION

- ■ High speed scanning mode for blind symbol rate acquisition
- ■ Full satellite transponders scanning in seconds

DiSEqC™ 2.0

- ■ Receive and transmit for full control of LNB and switchers

MULTISTANDARD DEMODULATION

- ■ Compatible with direct conversion tuners
  - ● dual 8-bit analog to digital converters
  - ● wide range carrier tracking loop for frequency offset recovery
  - ● flexible clock generation to operate with 4 MHz to 30 MHz external reference
- ■ Digital carrier and timing recovery loops
  - ● full digital timing and phase recovery loops
- ■ Up to 60 Msps operation
- ■ Automatic spectral inversion ambiguity resolution
- ■ Digital carrier and timing recovery loops
  - ● full digital timing and phase recovery loops
- ■ Up to 60 Msps operation
- ■ Automatic spectral inversion ambiguity resolution
- ■ Digital cancellation of A/D offset
- ■ Digital Nyquist root filter
  - ● 0.20, 0.35 roll-off factors

MULTISTANDARD DECODING

- ■ DIRECTV™ system / DVB-S
  - ● VITERBI soft decoder rate 1/2
  - ● puncture rates are 1/2, 2/3, 3/4, 5/6, 6/7, 7/8
  - ● outer Reed-Solomon decoder as per DVB-S and DIRECTV™ system
  - ● energy dispersal descrambler

INTERFACES

- ■ Data to transport decoder
  - ● DVB common interface compliant
  - ● 12-bit parallel and 5-bit serial data interface with data on DATA_0 ... DATA7 (packet error private line)
  - ● transport bit rate automatic regulation with regard to transport clock
- ■ I^2C serial bus interface
  - ● fast I^2C up to 4 Mbit/s slave interface
  - ● 4 possible slave addresses
  - ● up to 400 Kbit/s private repeater for tuner isolation
- ■ DiSEqC™ 2.0
  - ● 22 kHz to 100 kHz interface
- ■ GPIOs and interruption line
  - ● lock indicators: AGC carrier, timing, VITERBI-decoder
- ■ Monitoring through I^2C serial interface
  - ● C/N estimator - signal strength indicator
  - ● IQ constellation display
  - ● BER and PER estimator
  - ● bit and packet error count
- ■ Monitoring through I^2C serial interface
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  - ● BER and PER estimator
  - ● bit and packet error count

TECHNOLOGY

- ■ 90nm CMOS process
- ■ Multi supply: 1.0 V core, 2.5 V analog, 3.3 V interfaces
- ■ Power saving features
  - ● active < 200 mW, (internal clock 100 MHz, puncture 7/8, rate 30 Mbit/s)
  - ● stand-by < 50mW
- ■ Low-noise active slew rate buffers
- ■ TQFP 64 package with no exposed pad
  - ● Rth = 20° C/W
- ■ Integrated 1.0 V DC regulator

Contents

1 Overview

The STV0288 is a single-chip channel receiver for satellite television reception.

The device contains two 8-bit analog to digital converters for I-input and Q-input, a QPSK demodulator, and a forward error correction (FEC) unit with both an inner (Viterbi) and a outer (Reed-Solomon) decoder.

The device accepts baseband differential signals as I and Q inputs. An external reference generates the high performance clock. Analog to digital conversion is performed by two 8-bit ADCs.The FEC unit is compliant with the DIRECTV and DSS specifications. All processing is digital. The Reed-Solomon decoder corrects up to eight erroneous bytes per packets.

A derotator, located before the Nyquist root filter, allows a wide range of offset tracking.

The high sampling rate facilitates the implementation of low-cost, direct conversion tuners.

The STV0288 is controlled through an I^2C interface. The device operates up to 120 MHz and can process variable modulation rates up to 60 Msps. The chip outputs MPEG transport streams and interfaces to the packet demultiplexers embedded in the ST Omega chip family.

The multistandard capability associated with a broad range of input frequency operations makes it easy to use. Its low power consumption, small package and low bill of material makes it perfect for all satellite applications.

2 Pin assignments

Figure 2: STV0288 TQFP64 pin connections
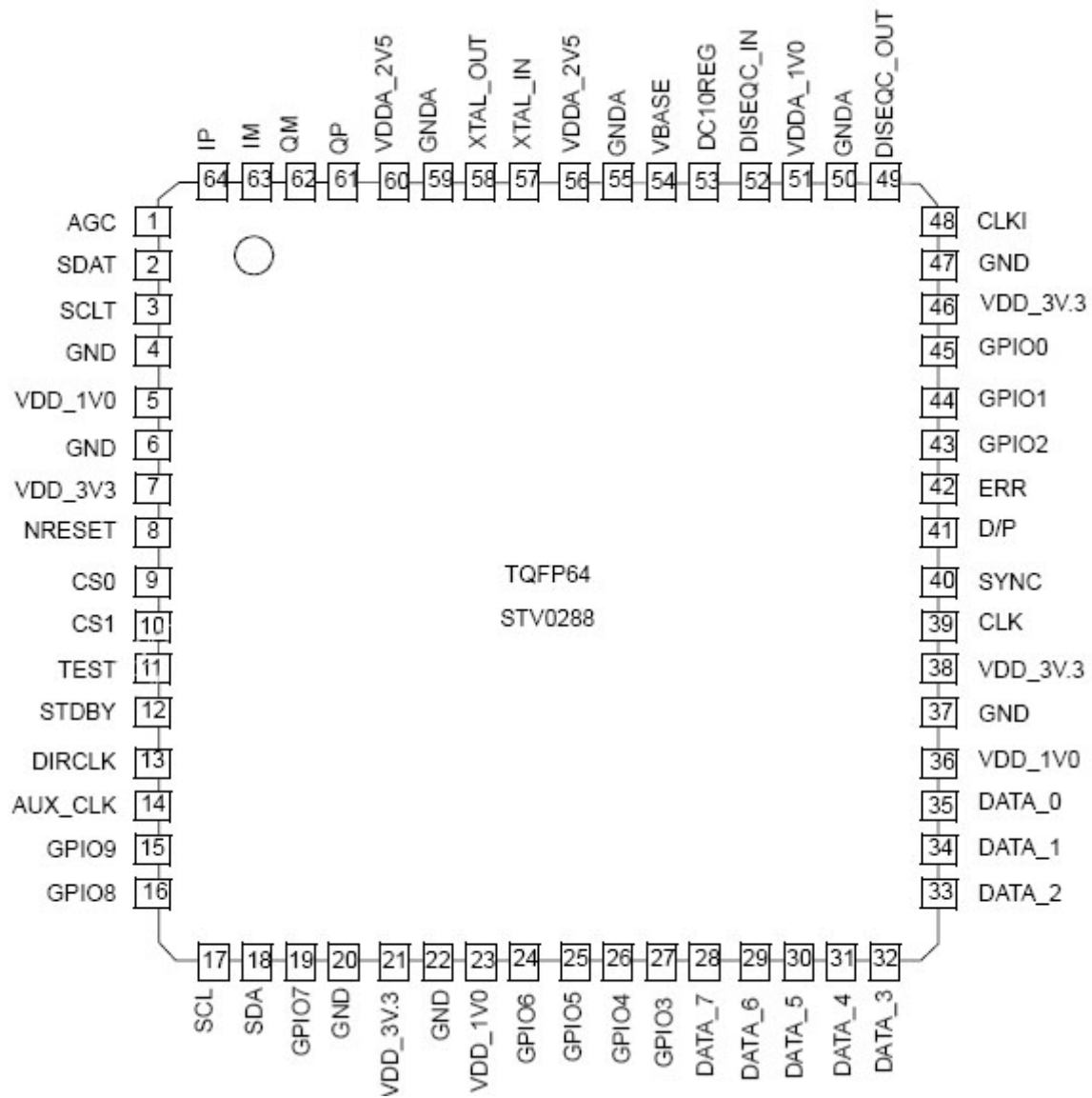
2.1 Pin description

Table 1: STV0288 pin list

Pin	Symbol	Type	Voltage	Description/comment
01	AGC	I/O	3.3	AGC control signal or general purpose I/O
02	SDAT	I/O	3.3	I²C isolated repeater data or general purpose I/O
03	SCLT	I/O	3.3	I²C isolated repeater clock or general purpose I/O
04	GND	Ground	0	Digital ground
05	VDD_1V0	Supply	1.0	Digital core supply
06	GND	Ground	0	Digital ground
07	VDD_3V3	Supply	3.3	Digital buffer supply
08	NRESET	I/O	3.3	Reset signal active low
09	CS0	I/O	3.3	Chip select for address selection or general purpose I/O
10	CS1	I/O	3.3	Chip select for address selection or general purpose I/O
11	TEST	I/O	3.3	For test purposes
12	STDBY	I/O	3.3	Standby mode or general purpose I/O
13	DIRCLK	I/O	3.3	Clock path selection or general purpose I/O
14	AUX_CLK	I/O	3.3	Programmable output clock or general purpose I/O
15	GPIO9	I/O	3.3	General purpose I/O
16	GPIO8	I/O	3.3	General purpose I/O
17	SCL	I/O	3.3	Serial interface input clock (I²C bus)
18	SDA	I/O	3.3	Serial interface I/O data (I²C bus)
19	GPIO7	I/O	3.3	General purpose I/O
20	GND	Ground	0	Digital ground
21	VDD_3V3	Supply	3.3	Digital buffer supply
22	GND	Ground	0	Digital ground
23	VDD_1V0	Supply	1.0	Digital core supply
24	GPIO6	I/O	3.3	General purpose I/O
25	GPIO5	I/O	3.3	General purpose I/O
26	GPIO4	I/O	3.3	General purpose I/O
27	GPIO3	I/O	3.3	General purpose I/O
28	DATA_7	I/O	3.3	Transport stream parallel data MSB or data out in serial data
29	DATA_6	I/O	3.3	Transport stream parallel data
30	DATA_5	I/O	3.3	Transport stream parallel data
31	DATA_4	I/O	3.3	Transport stream parallel data
32	DATA_3	I/O	3.3	Transport stream parallel data
33	DATA_2	I/O	3.3	Transport stream parallel data

Pin	Symbol	Type	Voltage	Description/comment
34	DATA_1	I/O	3.3	Transport stream parallel data
35	DATA_0	I/O	3.3	Transport stream parallel data LSB or data_out in serial data
36	VDD_1V0	Supply	1.0	Digital core supply
37	GND	Ground	0	Digital ground
38	VDD_3V3	Supply	3.3	Digital buffer supply
39	CLK	I/O	3.3	Transport stream byte or bit clock
40	SYNC	I/O	3.3	Transport stream sync bit
41	D/P	I/O	3.3	Transport stream data valid signal
42	ERR	I/O	3.3	Transport stream packet error signal
43	GPIO2	I/O	3.3	General purpose I/O
44	GPIO1	I/O	3.3	General purpose I/O
45	GPIO0	I/O	3.3	General purpose I/O
46	VDD_3V3	Supply	3.3	Digital buffer supply
47	GND	Ground	0	Digital ground
48	CLKI	I/O	3.3	Optional clock input
49	DISEQC_OUT	I/O	3.3	Digital satellite equipment control output or general purpose I/O
50	GNDA	Ground	0	Analog ground (DISEqC, PLL, OSC)
51	VDDA_1V0	I/O	1.0	Analog supply 1.0v (DISEqC, PLL, OSC)
52	DISEQC_IN	Supply	3.3	Digital satellite equipment control input
53	VDD10REG	Supply	1.0	VDD 1.0 V regulated
54	VBASE	I/O	3.3	Control of bipolar base for regulator
55	GNDA	Ground	0	Analog ground (DISEqC, PLL, OSC)
56	VDDA_2V5	Supply	2.5	Analog supply 2.5 V
57	XTAL_IN	I/O	3.3	Oscillator input
58	XTAL_OUT	I/O	3.3	Oscillator output
59	GNDA	Ground	0	Analog ground (AD, regulator)
60	VDDA_2V5	Supply	2.5	Analog supply 2.5 V (AD, regulator)
61	QP	I/O	3.3	Positive quadrature-phase baseband input
62	QM	I/O	3.3	Negative quadrature-phase baseband input
63	IM	I/O	3.3	Negative in-phase baseband input
64	IP	I/O	3.3	Positive in-phase baseband input

3 General purpose I/O (GPIO)

The flexible GPIO implementation facilitates debug, and allows digital signals to be routed to the most convenient pin for board layout and test. The general-purpose I/O pins are named GPIO0 to GPIO9. Their function is defined by programming the GPIOXCFG registers, where X is the GPIO pin number [0:9]. The register programming is detailed below.

7	6	5	4	3	2	1	0
OPEN_DRAIN	CONFIGURATION VALUE						XOR

Bit 7: OPEN_DRAIN: when high, configures the pin in open-drain; when low, configures the pin as push-pull.

Bit [6:1]: CONFIGURATION VALUE: refer to Table 6: *General-purpose input and output configuration on page 57*.

Bit 0: XOR: Invert the signal selected (by applying an XOR operation with the value XOR).

All the GPIO pins are configured by default to 0x82 which means they are set to open drain, logic 1 (that is, high impedance).

Refer to the GPIOXCFG register to configure these pins for application-specific requirements. The following pins may also be configured as GPIO pins by accessing the appropriate registers.

- SDAT: See register *SDATCFG on page 58*.
- SCLT: See register *SCLTCFG on page 58*.
- AGC: See register *AGCCFG on page 58*
- DIRCLK: See register *DIRCLKCFG on page 58*.
- AUX_CLK: See register *AUXCKCFG on page 58*.
- STDBY: See register *STDBYCFG on page 59*.
- CS0: See register *CS0CFG on page 59*.
- CS1: See register *CS1CFG on page 59*.
- DISEQC_OUT: See register *DISEQCOCFG on page 59*.

These pins are identical to the GPIO pins except that they are programmed with default values at power up, or after a reset. It is not recommended that these pins are reprogrammed but, if necessary, it is possible to do so.

Registers GPIOVAL0, GPIOVAL1 and GPIOVAL2 (0x6A, 0x6B and 0x6C) can be used to read the values present on GPIOs.

4 I²C interface

The I²C interface uses the standard I²C protocol, where the first byte is 0xD0 (0xD2, 0xD4, or 0xD6) for a write operation, or 0xD1 (0xD3, 0xD5, or 0xD7) for a read operation. The I²C interface supports I²C fast mode (I²C 400 kHz).

4.1 I²C chip addresses

The I²C chip addresses are shown in Table 2. The address is initiated at power-on, or on the rising edge of the hard reset. The address (7 bits) is given by 11010, CS1 and CS0. The address value is kept in register IOCFG2 until the next hard reset.

Table 2: I²C chip addresses

Pin	Value				
CS1 pin 10	0	0	1	1	MSB
CS0 pin 9	0	1	0	1	LSB
I²C chip address	0xD0	0xD2	0xD4	0xD6	

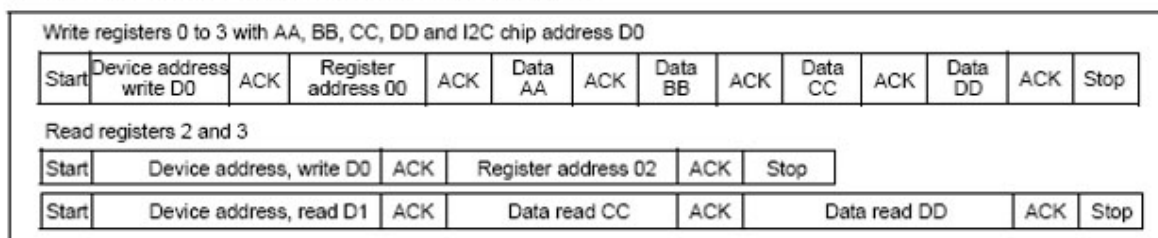## 4.2 Write operation (normal mode)

The byte sequence is as follows:

1. The first byte gives the device address plus the direction bit (R/W = 0).
2. The second byte contains the internal address of the first register to be accessed.
3. The next byte is written in the internal register. Following bytes (if any) are written in successive internal registers.
4. The transfer lasts until stop conditions are encountered.
5. The STV0288 acknowledges every byte transfer.

4.3 Read operation (normal mode)

The address of the first register to read is programmed in a write operation without data, and terminated by the stop condition. Then, another start is followed by the device address, and R/W = 1. All following bytes are data to be read at successive positions, starting from the initial address. Figure 3 shows the I²C read and write mode.

Figure 3: Example of I²C read and write operations

Write registers 0 to 3 with AA, BB, CC, DD and I2C chip address D0													
Start	Device address write D0	ACK	Register address 00	ACK	Data AA	ACK	Data BB	ACK	Data CC	ACK	Data DD	ACK	Stop

Read registers 2 and 3					
Start	Device address, write D0	ACK	Register address 02	ACK	Stop
Start	Device address, read D1	ACK	Data read CC	ACK	Data read DD	ACK	Stop

4.4   I²C interface in standby mode

The standby mode bit is at address 0x41 (register SYNTCTRL bit STANDBY). Only registers marked with an asterisk (*) in the register map can be addressed in standby mode.

4.5   Identification register

Register ID (at address 0x00) gives the release number of the circuit.

The content of this register at reset (currently 0x10), will be modified for any new release. In this case, the register at reset will become 0x11.

The register is first read, then the value obtained is compared with the value required by the software, for example:

- Release 1: read address 0x00: value = 0x10,
- Release 2: read address 0x00: value = 0x11.

4.6   I²C bus repeater

Signal pollution, generated by the SDA/SCL lines of the I²C bus, can dramatically worsen tuner performance. To avoid this, the STV0288 has a dedicated I²C bus repeater so that SDAT and SCLT are active only when necessary, and become muted once the tuner configuration has settled.

Pins SDAT and SCLT are set high at reset. When the microprocessor writes a 1 into register I2CRPT, bit I2CT_ON, the next I²C message on SDA and SCL is repeated on pins SDAT and SCLT respectively, until stop conditions are detected.

To write to the tuner, the external microprocessor must, for each tuner message:

1. Program 1 in bit I2CT_ON (register I2CRPT).
2. Send the message to the tuner.

Any size of byte transfer is allowed, regardless of the address, until the stop conditions are detected. Transfers are fully bidirectional. Bit I2CT_ON is automatically reset at a stop condition.

The maximum operating frequency of the I²C bus repeater is 400 kHz. The I²CT speed is programmable through bits ENARPT_LEVEL[2:0] of register I2CRPT.

4.7   General purpose DAC

A DAC is available to control external analog devices. It is built as a sigma-delta first-order loop, and has a 12-bit resolution. It only requires an external low-pass filter (simple RC filter). The clock frequency is derived from the main clock by programmable division. The converter is controlled by two registers at addresses 0x1B (DACR1) and 0x1C (DACR2).

If the DAC is needed, the DAC output can be used by setting a GPIO. See Chapter 3: General purpose I/O (GPIO) on page 9.

5 Clock generation

5.1 Crystal oscillator and control

The STV0288 uses two types of clock signal. The clock signal is generated either by a crystal connected to pins XTAL_IN and XTAL_OUT, or by an external clock, connected to pin CLK_I.

The DIRCLK pin, sampled during hard reset, determines whether or not the crystal oscillator is defaulted active. Active means that the XTAL_IN and XTAL_OUT pins are able to drive an external quartz. When a logical one is sampled at DIRCLK, the clock is taken from CLK_I pin.

The oscillator cell in the STV0288 is a 30 MHz low phase noise oscillator and operates with a 27 MHz crystal oscillator. The oscillator can operate from 4 MHz up to 33 MHz. CLK_I pin can operate with an external clock from 4 MHz to 30 MHz.

5.1.1 Internal clock generation

An analog PLL generates the following clocks by division:

- the master clock (M_CLK), which corresponds to the sampling frequency,
- an auxiliary clock (AUX_CLK), which can be in MHz, or in the range 25 Hz to 1500 Hz. Frequencies in this range, for example, 60 Hz, are used for LNB control,
- two lower frequencies, F22FR and F22RX, from 22 kHz to 88 kHz, are needed for LNB control or DiSEqCTM control transmission and reception.

The PLL is based upon the charge pump principle and consists of the phase frequency detector, charge pump, filter, VCO, bandgap current reference and programmable dividers.

The PLL takes its reference from either the internal oscillator or the CLK_I pin. The frequency for this reference must be in the range 4 MHz to 30 MHz.

The PLL operating frequency is given by the equation:

$f_{pll} = f_{xtal} \times (PLL\_DIV)/4$ or $f_{pll} = f_{clk\_i} \times (PLL\_DIV)/4$ when PLL_SELRATIO = 1

$f_{pll} = f_{xtal} \times (PLL\_DIV)/6$ or $f_{pll} = f_{clk\_i} \times (PLL\_DIV)/6$ when PLL_SELRATIO = 0

The PLL has a power down mode, see bit PLL_STOP in the register *SYNTCTRL on page 55*. When this mode is active, the bandgap reference circuits are disabled, and the PLL consumes almost zero power.
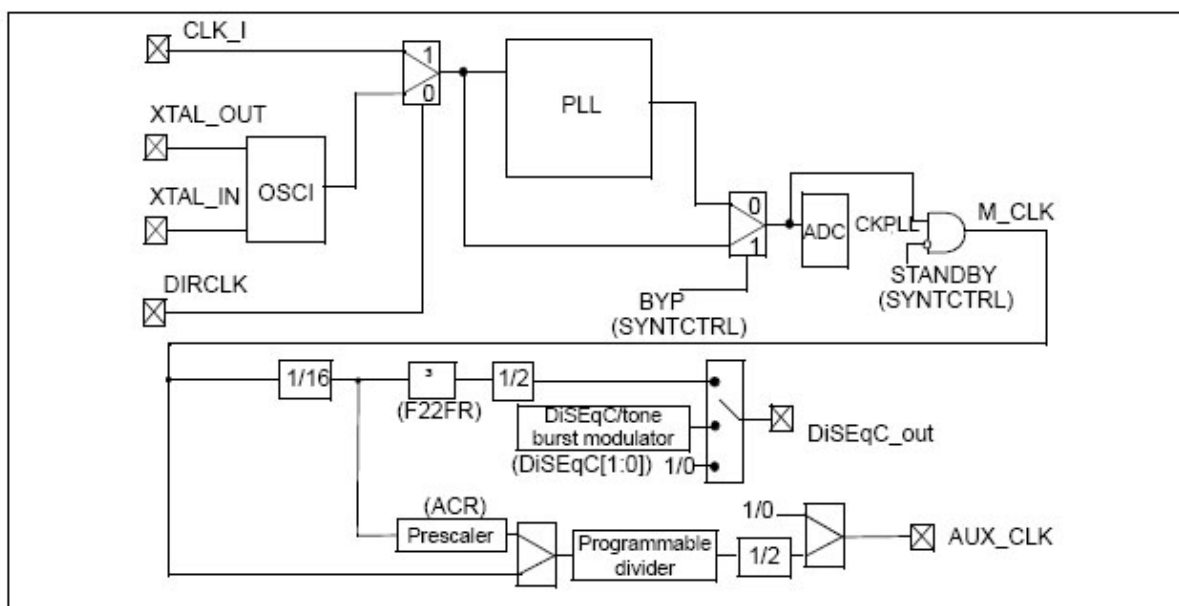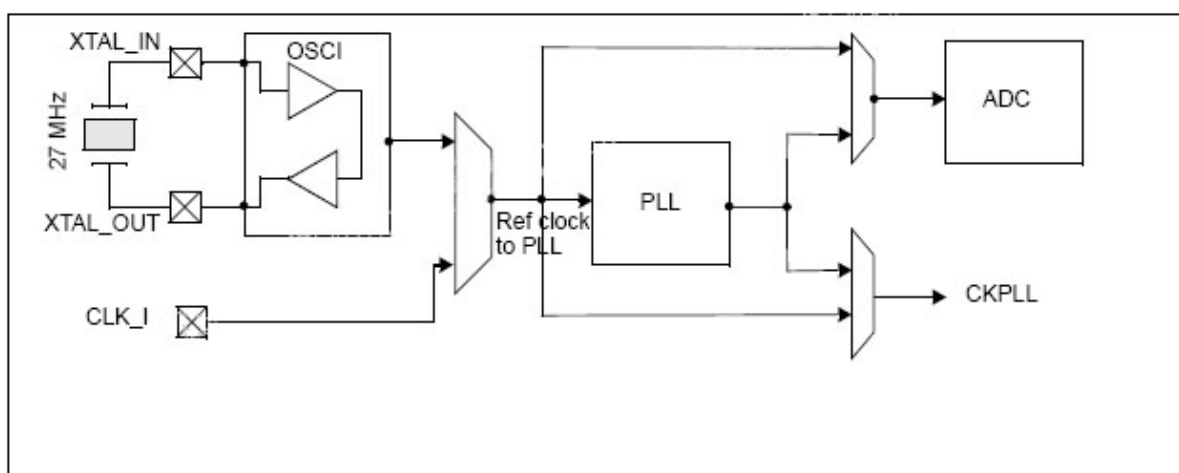
Figure 4: Clock signal generation

Figure 5: Master clock generation

The master clock frequency is programmed using PLL_DIV, see *PLLCTRL on page 55*.

Clock registers

The auxiliary clock and F22 frequency registers are at addresses 0x02 (ACR), 0x03 (F22FR) and 0x04 (F22RX).

Standby mode

A low-power consumption mode (standby) is available. In standby mode, the I^{2}C decoder still operates, but with some restrictions.

Standby mode can be initiated or stopped by I^{2}C bus commands as described in *SYNTCTRL on page 55*, (address 0x41).

At power-on, the circuit starts to operate in standby mode when pin STDBY (pin 12) is tied to V$_{DD}$ This guarantees low power consumption for the stand-alone modules (PCMCIA size front-end modules) before any command is initiated. After the power-on sequence, the standby mode is entirely controlled through register SYNTCTRL.
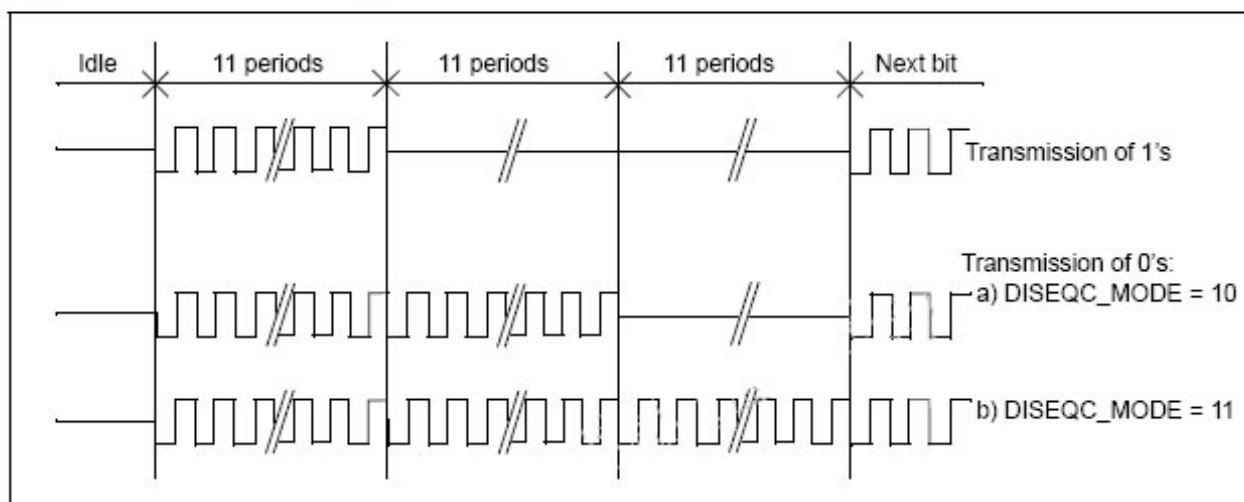
6 DiSEqC interface

DiSEqC transmit interface

The transmit DiSEqC interface simplifies the real-time dialog between the microprocessor and the LNB. Using the I^2C bus, the microprocessor fills a 16-bytes FIFO, and then transmits the data by modulating the F22FR clock (F22FR is set to 22 kHz).

Modulation

Figure 6: Schematic showing bit transmission

The output is a gated 22 kHz square signal. In idle state, modulation is permanently inactive.

In byte transmission, the byte is sent (MSB first) and is followed by an odd parity bit. A byte transmission is therefore a serial 9-bit transmission with an odd number of 1's. Each bit lasts 33 F22 periods and the transmission is PWM-modulated.

Transmission of 0's

There are two submodes controlled by the I^2C bus:

- modulation is active for 22 pulses, then inactive for 11 pulses (2/3 PWM),
- modulation is active for 33 pulses (3/3 PWM).

Transmission of 1's

During transmission of 1's, modulation is active for 11 pulses, then inactive for 22 pulses (1/3 PWM). This is compatible with tone burst in older LNB protocols.

For the modulated tone burst, only one byte (with value 0xFF) is written to the FIFO. The parity bit is 1. As a result, the output signal is nine 0.5 ms bursts, separated by eight 1 ms intervals.

For the unmodulated tone burst, DISEQC_MODE = 11 and only one byte of value 0x00 is sent. The parity bit is still 1. As a result, the signal is a continuous series of 12.5 ms.

When the modulation is active, the DiSEqC output is forced alternatively to V_{DD} and V_{SS} levels.

6.1.2 Envelope mode

In envelope mode, a 22-kHz envelope output is generated instead of a modulated signal output. It controls the on/off switch of an external 22-kHz oscillator.

The backward compatibility of DiSEqC requires a 15-ms gap after a tone burst sequence. This information is delivered by a flag in a status register. This flag is set at the beginning of the transmission, and is reset after a time that includes both the transmission, and a period defined by the I^{2}C bus.

Figure 7: Gap between bursts
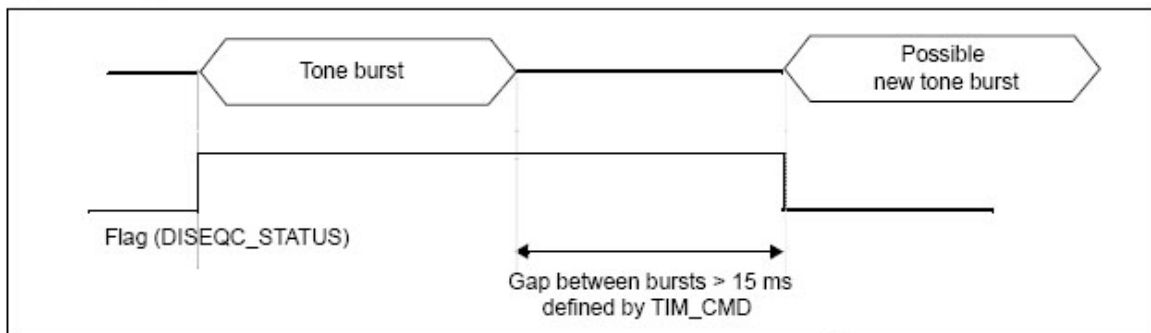
6.2 DiSEqC receive interface

The DiSEqC receive interface is composed of three parts, one analog and two digital as follows:
- analog: bypassable 1-bit analog-to-digital conversion,
- digital filtering: envelop detection.
- digital treatment: received byte extraction and stacking in FIFO, status management.

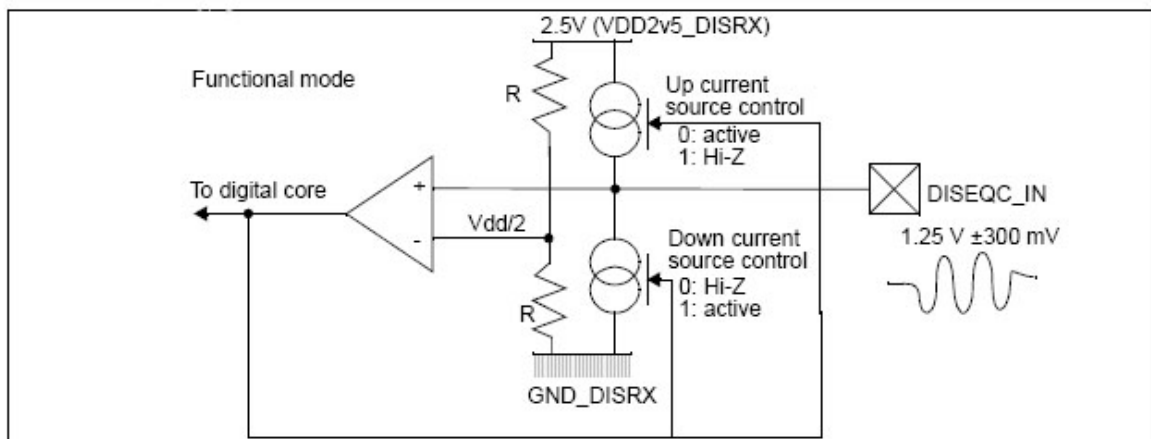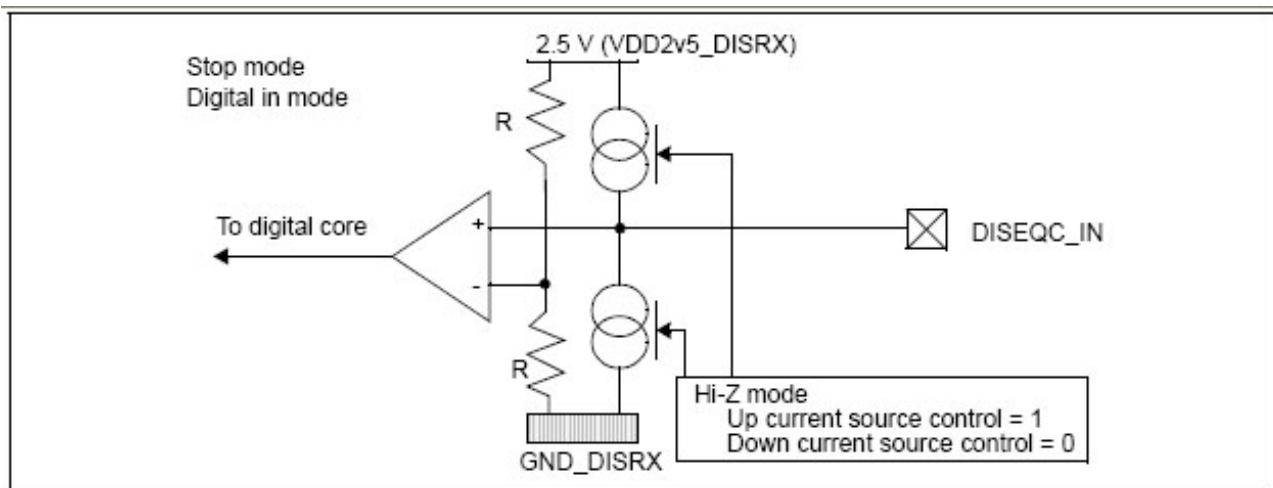Figure 8: DiSEqC receive analog part, running mode

Figure 9: DiSEqC receive analog part, stopped mode

General cell characteristics are as follows:

- 16-byte FIFO,
- bypass mode for analog cell: the signal can be provided by a pin other than DISEQC_IN (or inverted DISEQC_IN),
- envelope mode: bypass of digital filtering,
- IRQ signals: eighth byte stacked in the FIFO and end of reception,
- 16-bit status register,
- FIFO and parity output registers: a nonnull value in PARITY_FAIL BIT in DISRX_ST1 register indicates a transmission error in the remaining data still stacked in the FIFO,
- ignore short 22-kHz mode: does not consider pulses composed of less than seven 22-kHz waves,
- one-chip test mode: DISEqC Tx signal is injected into the DiSEqC Rx cell so the decoder understands the encoder,
- continuous tone detection,
- decoding fail detection and alert,

22-kHz frequency generation register: F22RX. The digital construction of the analog cell enables the standard 22 kHz to be increased up to 100 kHz.

7 Signal processing

In general the STV0288 is programmed using scripts and low level application (LLA) drivers supplied by STMicroelectronics. The following description provides an aid to understanding the register settings but does not replace the need to reference the application notes, LLA drivers and scripts.

7.1 Demodulation

The demodulator block performs QPSK demodulation according to DIRECTV and DVBS specifications. This implementation is based on the STv0299B demodulator core, and has the following functions:

- automatic gain correction (AGC1),
- IQ DC offset corrections,
- carrier frequency and phase acquisition and tracking,
- symbol timing acquisition and tracking,
- Nyquist filtering (alpha = 0.2, 0.35),
- symbol demapping and soft bit decisions.
- supports channel symbol rates up to 60 MSPS: maximum QPSK 60 MSPS @ 120 MHz fsamp.

The following sections provide a description of each block within the DVB-S/DIRECTV demodulator.

7.1.1 I and Q output

The STV0288 contains dual 8-bit A/D converters. The elementary ADC preforms an 8-bit conversion within 10 cycles (minimum) of the master clock. Maximum input is 120 MHz.

An internal voltage reference block generates all necessary voltage references or common mode voltage.

The inputs are differential inputs. In case of single-ended applications, I and Q signals from the tuner are fed to the respective IP and QP inputs through a capacitor. The IN and QN pins are DC biased.

7.1.2 AGC1

The modulus of the I and Q input is compared to a programmable threshold, m1, and the difference is integrated. This signal is then converted into a pulse density modulation by a first order $\Sigma\Delta$ DAC to drive the AGC output. This output signal is provided to control the signal levels in the tuner section of the receiver and ensure the signal level fed to the STV0288 is set at an optimal value under all reception conditions.

The output is a 3.3 V tolerant open drain or push pull stage, configurable through the bit AGC_OPDRAIN.

The time constant of the AGC is given by

$$Tagc = \frac{2^{26-\beta agc}}{m1} xTmclk$$

The coefficient beta is programmable through the AGC1C register (AGCIQ_BETA field). The reset value of beta allows an initial settling time of less than 100 k master clock periods. T_{mclk} represents the period of the master clock (MCLK).

Figure 10: AGC signal generation
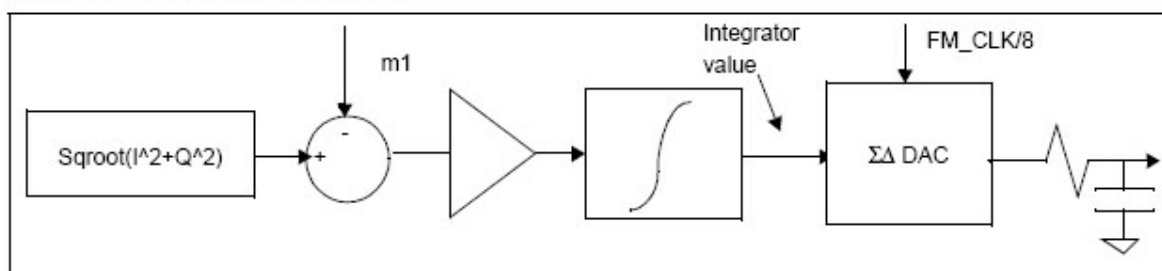
7.1.3 Offset cancellation

This device suppresses the residual DC component on I and Q. The compensation may be frozen to its last value by resetting the DC offset compensation bit in AGC control register AGC1C at address 0x0E (bit AVERAGE_ON).

7.1.4 Nyquist root and interpolation filters

Two roll off values are available: 0.35 and 0.20. They are selected in ROLLOFF register bit MODE_COEFF.

After Nyquist filtering, the signal amplitude is adjusted using a second AGC (AGC2). This AGC is controlled using register AGC2REF. Through the action of the AGC. the modulus of the output IQ signals is constant and equal to AGC2REF.

The RMS value of I and Q is measured after the Nyquist filter and compared to a programmable value, m2, as for the analog AGCs. The integrated error signal is applied to a multiplier on each I and Q path. m2 is compared to $\sqrt{(I^2 + Q^2)}$

The AGC2 control register AGC2COEF is at address 0x12. Bits [2:0] give the AGC2 coefficient, and this sets BETA_AGC2 the gain of the integrator. Table 3 shows how BETA_AGC2 is programmed with the AGC2 coefficient (which is related to the time constant of the AGC).

Table 3: AGC2 coefficients

AGC2 coefficient	BETA_AGC2
000	0
001	1
010	4
011	16
100	64
101	256
110	-
111	-

If the AGC2 coefficient = 0, the gain remains unchanged from its last value.

The time constant is independent of the symbol frequency, however it does depend on the modulus, m1, of the input signal, programmed in AGC1, with the following approximate relation:

$$T_{AGC2} = \{60 \times 10^3 \times T_{M\_CLK}\} / \{m1 \times BETA\_AGC2\}$$