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1. INTRODUCTION

17MB95 main board is driven by MStar SOC. This IC is a single chip iDTV solution that supports channel decoding, MPEG decoding, and media-center functionality enabled by a high performance AV CODEC and CPU.

Key features includes,

- Combo Front-End Demodulator
- A multi standart A/V format decoder
- The MACEpro video processor
- Home theatre sound processor
- Internet and Variety of Connectivity Support
- Dual-stream decoder for 3D contents
- Multi-purpose CPU for OS and multimedia
- Peripheral and power management

Supported peripherals are:

- 1 RF input VHF I, VHF III, UHF
- 1 Satellite input
- 1 Side AV (CVBS, R/L_Audio)
- 1 SCART socket(Common)
- 1 Side YPbPr
- 1 Side S-Video(Common)
- 1 PC input(Common)
- 3 HDMI input
- 1 Common interface(Common)
- 1 S/PDIF output
- 1 Headphone(Common)
- 2 USB
- 1 Ethernet-RJ45
- 1 External Touchpad(Common)
2. TUNER

A. **SI2156 Terrestrial and Cable TV Tuner:**

A.1. Description:

The Si2156 integrates a complete hybrid TV tuner supporting all worldwide terrestrial and cable TV standards. Leveraging Silicon Labs’ field proven digital low-IF architecture, the Si2156 maintains the unmatched performance and design simplicity of the Si2153 while further reducing footprint size and bill of materials cost. No external LNAs, tracking filters, wirewound inductors, or SAW filters are used.

Compared with competing silicon tuners and discrete MOPLL-based tuners, the Si2156 delivers superior picture quality and a higher number of received stations in crowded and near/far real-world reception conditions. The high linearity and low noise RF front-end delivers superior blocking performance and higher sensitivity in the presence of strong undesired channels and interference.

The Si2156 integrates the complete signal path from antenna input to IF outputs for both analog and digital transmission standards. Compared to traditional discrete MOPLL-based tuners, the Si2156 eliminates hundreds of external components including external LNAs, tracking filter varactors and inductors (unlike competing silicon tuners), and SAW filters, resulting in the simplest, lowest-cost BOM for a hybrid TV tuner.

Interfacing the Si2156 seamlessly with the Si2165 DVB-T/C demodulator creates a complete terrestrial and cable DVB-T/C receiver plus PAL/SECAM tuner.

A.2. Features:

- Worldwide hybrid TV tuner
- Analog TV: NTSC, PAL/SECAM
- Digital TV: ATSC/QAM, DVB-T/T2/C, ISDB-T/C, DTMB
- 42-1002 MHz frequency range
- Compliance to A/74, NorDig, D-Book, C-Book, ARIB, EN55020, OpenCable™ specifications
- Best-in-class real-world reception
- Exceeds discrete MOPLL-based tuners
- Highly integrated, lowest BOM
- No SAW filters or wirewound inductors required
- Integrated LNAs and complete tracking filters
- No alignment, tuning or calibration required
- Digital low-IF architecture
- Integrated channel select filters
- Flexible output interface
- ALIF to analog TV demodulator or SoC
- DLIF to digital TV demodulator or SoC
- 3.3 and 1.8 V power supplies
- Standard CMOS process technology
- 5 x 5 mm, 32-pin QFN package
- RoHS compliant

Figure 1: Pin description
<table>
<thead>
<tr>
<th>Pin Number(s)</th>
<th>Name</th>
<th>I/O</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>VDD_S</td>
<td>S</td>
<td>Interface supply voltage (I²C), 1.8 to 5.0 V</td>
</tr>
<tr>
<td>2</td>
<td>SCL</td>
<td>I</td>
<td>I²C clock input</td>
</tr>
<tr>
<td>3</td>
<td>SDA</td>
<td>I/O</td>
<td>I²C data input/output</td>
</tr>
<tr>
<td>4</td>
<td>VDD_D</td>
<td>S</td>
<td>Digital supply voltage, 1.8 V</td>
</tr>
<tr>
<td>5</td>
<td>GND</td>
<td>S</td>
<td>Ground. Connect GND pins to GND_PAD.</td>
</tr>
<tr>
<td>6</td>
<td>ADDR</td>
<td>I</td>
<td>I²C address select</td>
</tr>
<tr>
<td>7*</td>
<td>ALIF_AG C</td>
<td>I</td>
<td>ALIF output amplitude control input (optional)</td>
</tr>
<tr>
<td>8*</td>
<td>DLIF_AG C</td>
<td>I</td>
<td>DLIF output amplitude control input (optional)</td>
</tr>
<tr>
<td>9*</td>
<td>ALIF_N</td>
<td>O</td>
<td>ALIF differential output to ATV demodulator (negative)</td>
</tr>
<tr>
<td>10</td>
<td>VDD_H</td>
<td>S</td>
<td>Analog high supply voltage, 3.3 V</td>
</tr>
<tr>
<td>11*</td>
<td>ALIF_P</td>
<td>O</td>
<td>ALIF differential output to ATV demodulator (positive)</td>
</tr>
<tr>
<td>12*</td>
<td>DLIF_N</td>
<td>O</td>
<td>DLIF differential output to DTV demodulator (negative)</td>
</tr>
<tr>
<td>13*</td>
<td>DLIF_P</td>
<td>O</td>
<td>DLIF differential output to DTV demodulator (positive)</td>
</tr>
<tr>
<td>14</td>
<td>VDD_L</td>
<td>S</td>
<td>Analog low supply voltage, 1.8 V</td>
</tr>
<tr>
<td>15*</td>
<td>BCLK</td>
<td>O</td>
<td>Buffered clock output</td>
</tr>
<tr>
<td>16*</td>
<td>XOUT</td>
<td>O</td>
<td>Output reference clock to secondary tuner or receiver</td>
</tr>
<tr>
<td>17</td>
<td>XTAL_O</td>
<td>S</td>
<td>Crystal pin 2 (leave floating if XTAL_I is driven by XOUT of another tuner or receiver)</td>
</tr>
<tr>
<td>18</td>
<td>XTAL_I</td>
<td>I</td>
<td>Crystal pin 1 (or RCLK input driven by XOUT of another tuner or receiver)</td>
</tr>
<tr>
<td>19</td>
<td>VDD_H</td>
<td>S</td>
<td>Analog high supply voltage, 3.3 V</td>
</tr>
<tr>
<td>20</td>
<td>VDD_H</td>
<td>S</td>
<td>Analog high supply voltage, 3.3 V</td>
</tr>
<tr>
<td>21</td>
<td>RF_SHLD</td>
<td>S</td>
<td>RF input shield</td>
</tr>
<tr>
<td>22</td>
<td>RF_IN</td>
<td>I</td>
<td>RF balanced input from balun (negative)</td>
</tr>
<tr>
<td>23</td>
<td>RF_IP</td>
<td>I</td>
<td>RF balanced input from balun (positive)</td>
</tr>
<tr>
<td>24</td>
<td>RF_SHLD</td>
<td>S</td>
<td>RF input shield</td>
</tr>
<tr>
<td>25</td>
<td>GND</td>
<td>S</td>
<td>Ground. Connect GND pins to GND_PAD.</td>
</tr>
<tr>
<td>26</td>
<td>GND</td>
<td>S</td>
<td>Ground. Connect GND pins to GND_PAD.</td>
</tr>
<tr>
<td>27</td>
<td>GND</td>
<td>S</td>
<td>Ground. Connect GND pins to GND_PAD.</td>
</tr>
<tr>
<td>28*</td>
<td>GPIO</td>
<td>I/O</td>
<td>General purpose input/output</td>
</tr>
<tr>
<td>29*</td>
<td>INTB</td>
<td>O</td>
<td>Interrupt request output</td>
</tr>
<tr>
<td>30</td>
<td>RSTB</td>
<td>I</td>
<td>Hardware reset (active low)</td>
</tr>
<tr>
<td>31</td>
<td>GND</td>
<td>S</td>
<td>Ground. Connect GND pins to GND_PAD.</td>
</tr>
<tr>
<td>32</td>
<td>VDD_IO</td>
<td>S</td>
<td>I/O supply voltage, 1.8 to 3.3 V</td>
</tr>
<tr>
<td></td>
<td>GND_PAD</td>
<td>S</td>
<td>Ground. Connect GND pins to GND_PAD.</td>
</tr>
</tbody>
</table>

*Note:* Pin should be left floating if unused.

Table 1: Pin functions
B. **M88TS2022 Satellite Tuner**

B.1. Features and General Description

<table>
<thead>
<tr>
<th>Features</th>
<th>Applications</th>
</tr>
</thead>
<tbody>
<tr>
<td>Single-chip tuner</td>
<td>Digital satellite receiver front-end for DVB-S2 and ABS-S applications</td>
</tr>
<tr>
<td>Compliant with DVB-S2 and ABS-S standards</td>
<td></td>
</tr>
<tr>
<td>Support QPSK, 8PSK and 10APSK</td>
<td></td>
</tr>
<tr>
<td>Direct-conversion from L-band to baseband</td>
<td></td>
</tr>
<tr>
<td>Symbol rate: 1 to 45 Msymbols/s</td>
<td></td>
</tr>
<tr>
<td>Integrated VCOs and PLL, with on-chip inductors, varactors and loop filter</td>
<td></td>
</tr>
<tr>
<td>Integrated baseband filters: 4 MHz to 40 MHz bandwidth</td>
<td></td>
</tr>
<tr>
<td>Integrated RF AGC for optimal performance</td>
<td></td>
</tr>
<tr>
<td>Integrated baseband DC offset cancellation (patent-pending) removes external loop filters</td>
<td></td>
</tr>
<tr>
<td>Excellent immunity to strong adjacent undesired channels</td>
<td></td>
</tr>
<tr>
<td>Integrated clock driver provides auxiliary divided clock output for other devices</td>
<td></td>
</tr>
<tr>
<td>Selectable RF bypass</td>
<td></td>
</tr>
<tr>
<td>Support sleep mode</td>
<td></td>
</tr>
<tr>
<td>2-wire serial bus with 3.3 V compatible logic levels</td>
<td></td>
</tr>
<tr>
<td>Power supply: +3.3 V</td>
<td></td>
</tr>
<tr>
<td>28-pin QFN (Quad Flat No-lead) package</td>
<td></td>
</tr>
<tr>
<td>RoHS compliant</td>
<td></td>
</tr>
</tbody>
</table>

**General Description**

The M88TS2022 is a single-chip, direct-conversion tuner for digital satellite receiver applications. It offers the industry’s most integrated solution to a satellite tuner function, simplifying the front-end designs. The device also provides an RF bypass output for driving a second tuner module.

This device incorporates the following functional blocks on a single chip: an LNA, quadrature down-converting mixers, a low phase noise and fast locking frequency synthesizer with on-chip loop filters, a DC offset cancellation loop with integrated loop filters, self-calibrated programmable baseband channel filters, an integrated RF AGC loop, and crystal oscillators with an integrated auxiliary clock output.

As a result of integrating all these blocks, the M88TS2022 has the least number of pins compared with other conventional solutions, and requires the least external components. In typical applications, the M88TS2022 requires only one crystal, one bypass capacitor, one matching network, and a few external resistors. The device also has the industry’s smallest latency, as it uses a fast locking PLL and a fast settling DC offset cancellation architecture.

The M88TS2022 can be configured via a 2-wire serial bus. The chip is available in a 28-pin QFN package.

B.2. Pin Assignment

![Diagram of M88TS2022 pinout](image)
B.3. Absolute Maximum Ratings and Recommended Operating Conditions

### Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min.</th>
<th>Max.</th>
<th>Unit</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDDA</td>
<td>Analog power supply</td>
<td>-0.6</td>
<td>5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>VDD_DIG</td>
<td>Digital power supply</td>
<td>-0.6</td>
<td>5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( V_{2\text{-wire}} )</td>
<td>Voltage on 2-wire bus pins</td>
<td>-0.6</td>
<td>5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( V_{IN} )</td>
<td>Voltage on other input pins</td>
<td>-0.6</td>
<td>2.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( V_{OUT} )</td>
<td>Output voltage</td>
<td>-0.6</td>
<td>VDDA + 0.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( T_{STG} )</td>
<td>Storage temperature</td>
<td>-55</td>
<td>150</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>( T_{OP} )</td>
<td>Operating ambient temperature</td>
<td>0</td>
<td>70</td>
<td>°C</td>
<td></td>
</tr>
</tbody>
</table>

*Note: Stresses above the Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended period may affect device reliability.*

### Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDDA, VDD_DIG</td>
<td>Analog power supply</td>
<td>3.0</td>
<td>3.3</td>
<td>3.6</td>
<td>V</td>
<td>With respect to VSS</td>
</tr>
<tr>
<td>( T_{OP} )</td>
<td>Operating ambient temperature</td>
<td>0</td>
<td></td>
<td>70</td>
<td>°C</td>
<td></td>
</tr>
</tbody>
</table>

*Note: Device functionality is not guaranteed at any conditions beyond the recommended operating conditions.*

### 3. AUDIO AMPLIFIER STAGES

#### A. MAIN AMPLIFIER (TAS5719)(6-8 W option)

##### a. General Description

The TAS5717/TAS5719 is a 10-W/15-W, efficient, digital audio-power amplifier for driving stereo bridge-tied speakers. One serial data input allows processing of up to two discrete audio channels and seamless integration to most digital audio processors and MPEG decoders. The device accepts a wide of input data and data rates. A fully programmable data path routes these channels to the internal speaker drivers.

The TAS5717/9 is a slave-only device receiving all clocks from external sources. The TAS5717/TAS5719 operates with a PWM carrier between a 384-kHz switching rate and a 352-KHz switching rate, depending on the input sample rate. Oversampling combined with a fourth-order noise shaper provides a flat noise floor and excellent dynamic range from 20 Hz to 20 kHz.
b. Features

• Audio Input/Output
  – TAS5717 Supports 2×10 W and TAS5719 Supports 2×15 W Output
  – Wide PVDD Range, From 4.5 V to 26 V
  – Efficient Class-D Operation Eliminates Need for Heatsinks
  – Requires Only 3.3 V and PVDD
  – One Serial Audio Input (Two Audio Channels)
  – I2C Address Selection via PIN (Chip Select)
  – Supports 8-kHz to 48-kHz Sample Rate (LI/RJ/I2S)
  – External Headphone-Amplifier Shutdown Signal
  – Integrated CAP-Free Headphone Amplifier
  – Stereo Headphone (Stereo 2-V RMS Line Driver) Outputs

• Audio/PWM Processing
  – Independent Channel Volume Controls With 24-dB to Mute
  – Programmable Two-Band Dynamic Range Control
  – 14 Programmable Biquads for Speaker EQ
  – Programmable Coefficients for DRC Filters
  – DC Blocking Filters
  – 0.125-dB Fine Volume Support

• General Features
  – Serial Control Interface Operational Without MCLK
  – Factory-Trimmed Internal Oscillator for Automatic Rate Detection
  – Surface Mount, 48-Pin, 7-mm × 7-mm HTQFP Package
  – AD, BD, and Ternary PWM-Mode Support
  – Thermal and Short-Circuit Protection
• Benefits
  – EQ: Speaker Equalization Improves Audio Performance
  – DRC: Dynamic Range Compression. Can Be Used As Power Limiter. Enables Speaker Protection, Easy Listening, Night-Mode Listening
  – DirectPath Technology: Eliminates Bulky DC Blocking Capacitors
  – Stereo Headphone/Stereo Line Drivers: Adjust Gain via External Resistors, Dedicated Active Headphone Mute Pin, High Signal-to-Noise Ratio
  – Two-Band DRC: Set Two Different Thresholds for Low- and High-Frequency Content

c. Pin descriptions and functions:

![Figure 2: Pin description](image-url)
<table>
<thead>
<tr>
<th>PIN</th>
<th>TYPE(1)</th>
<th>V TOLERANT</th>
<th>TERMINATION(2)</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>NAME</td>
<td>NO.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>AGND</td>
<td>30</td>
<td>P</td>
<td></td>
<td>Analog ground for power stage</td>
</tr>
<tr>
<td>A_SEL</td>
<td>14</td>
<td>DIO</td>
<td></td>
<td></td>
</tr>
<tr>
<td>A2</td>
<td>13</td>
<td>P</td>
<td></td>
<td>3.3-V analog power supply</td>
</tr>
<tr>
<td>AVSS</td>
<td>9</td>
<td>P</td>
<td></td>
<td>Analog 3.3-V supply ground</td>
</tr>
<tr>
<td>BST_A</td>
<td>45</td>
<td>P</td>
<td></td>
<td>High-side bootstrap supply for half-bridge A</td>
</tr>
<tr>
<td>BST_B</td>
<td>41</td>
<td>P</td>
<td></td>
<td>High-side bootstrap supply for half-bridge B</td>
</tr>
<tr>
<td>BST_C</td>
<td>40</td>
<td>P</td>
<td></td>
<td>High-side bootstrap supply for half-bridge C</td>
</tr>
<tr>
<td>BST_D</td>
<td>36</td>
<td>P</td>
<td></td>
<td>High-side bootstrap supply for half-bridge D</td>
</tr>
<tr>
<td>CPN</td>
<td>6</td>
<td>IO</td>
<td></td>
<td>Charge-pump flying-capacitor negative connection</td>
</tr>
<tr>
<td>CPP</td>
<td>7</td>
<td>IO</td>
<td></td>
<td>Charge-pump flying-capacitor positive connection</td>
</tr>
<tr>
<td>DVDD</td>
<td>27</td>
<td>P</td>
<td></td>
<td>3.3-V digital power supply</td>
</tr>
<tr>
<td>DVSS</td>
<td>28</td>
<td>P</td>
<td></td>
<td>Digital ground</td>
</tr>
<tr>
<td>DVSSO</td>
<td>17</td>
<td>P</td>
<td></td>
<td>Oscillator ground</td>
</tr>
<tr>
<td>GND</td>
<td>29</td>
<td>P</td>
<td></td>
<td>Analog ground for power stage</td>
</tr>
<tr>
<td>GYDD_OUT</td>
<td>34</td>
<td>P</td>
<td></td>
<td>Gate drive internal regulator output</td>
</tr>
<tr>
<td>HPL_IN</td>
<td>1</td>
<td>AI</td>
<td></td>
<td>Headphone left IN (single-ended, analog IN)</td>
</tr>
<tr>
<td>HPL_OUT</td>
<td>2</td>
<td>AO</td>
<td></td>
<td>Headphone left OUT (single-ended, analog OUT)</td>
</tr>
<tr>
<td>HP_PWML</td>
<td>48</td>
<td>DO</td>
<td></td>
<td>PWM left-channel headphone out</td>
</tr>
<tr>
<td>HP_PWMRR</td>
<td>47</td>
<td>DO</td>
<td></td>
<td>PWM right-channel headphone out</td>
</tr>
<tr>
<td>HPR_IN</td>
<td>4</td>
<td>AI</td>
<td></td>
<td>Headphone right IN (single-ended, analog IN)</td>
</tr>
<tr>
<td>HPR_OUT</td>
<td>3</td>
<td>AO</td>
<td></td>
<td>Headphone right OUT (single-ended, analog OUT)</td>
</tr>
<tr>
<td>HP_SD</td>
<td>33</td>
<td>AI</td>
<td></td>
<td>Headphone shutdown (active-low)</td>
</tr>
<tr>
<td>HPVDD</td>
<td>8</td>
<td>P</td>
<td></td>
<td>Headphone supply</td>
</tr>
<tr>
<td>HPVSS</td>
<td>5</td>
<td>P</td>
<td></td>
<td>Headphone ground</td>
</tr>
<tr>
<td>LRCLK</td>
<td>20</td>
<td>DI</td>
<td>5-V Pulldown</td>
<td>input serial audio data left/right clock (sample rate clock)</td>
</tr>
<tr>
<td>MCLK</td>
<td>15</td>
<td>DI</td>
<td>5-V Pulldown</td>
<td>Master clock input</td>
</tr>
<tr>
<td>OSC_RES</td>
<td>16</td>
<td>AO</td>
<td></td>
<td>Oscillator trim resistor. Connect an 19-kΩ 1% resistor to DVSSO.</td>
</tr>
<tr>
<td>OUT_A</td>
<td>44</td>
<td>O</td>
<td></td>
<td>Output, half-bridge A</td>
</tr>
<tr>
<td>OUT_B</td>
<td>42</td>
<td>O</td>
<td></td>
<td>Output, half-bridge B</td>
</tr>
<tr>
<td>OUT_C</td>
<td>39</td>
<td>O</td>
<td></td>
<td>Output, half-bridge C</td>
</tr>
<tr>
<td>OUT_D</td>
<td>37</td>
<td>O</td>
<td></td>
<td>Output, half-bridge D</td>
</tr>
<tr>
<td>PDN</td>
<td>19</td>
<td>DI</td>
<td>5-V Pulldown</td>
<td>Power down, active-low. PDN prepares the device for loss of power supplies by shutting down the noise shaper and initiating the PWM stop sequence. Power ground for half-bridges A and B</td>
</tr>
<tr>
<td>PDND_AB</td>
<td>43</td>
<td>P</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PGND_CD</td>
<td>38</td>
<td>P</td>
<td></td>
<td>Power ground for half-bridges C and D</td>
</tr>
<tr>
<td>PLL_FLM</td>
<td>10</td>
<td>AO</td>
<td></td>
<td>PLL negative loop-filter terminal</td>
</tr>
<tr>
<td>PLL_FLTP</td>
<td>11</td>
<td>AO</td>
<td></td>
<td>PLL positive loop-filter terminal</td>
</tr>
<tr>
<td>PVDD_AB</td>
<td>46</td>
<td>P</td>
<td></td>
<td>Power-supply input for half-bridge output A</td>
</tr>
<tr>
<td>PVDD_CD</td>
<td>35</td>
<td>P</td>
<td></td>
<td>Power-supply input for half-bridge output C</td>
</tr>
<tr>
<td>RESET</td>
<td>25</td>
<td>DI</td>
<td>5-V Pulldown</td>
<td>Reset, active-low. A system reset is generated by applying a logic low to this pin. RESET is an asynchronous control signal that restores the DAP to its default conditions, and places the PWM in the hard-mute (high-impedance) state.</td>
</tr>
<tr>
<td>SCL</td>
<td>24</td>
<td>DI</td>
<td>5-V</td>
<td>PC serial control clock input</td>
</tr>
<tr>
<td>SCLK</td>
<td>21</td>
<td>DI</td>
<td>5-V Pulldown</td>
<td>Serial audio data clock (shift clock). SCLK is the serial audio port input data bit clock.</td>
</tr>
<tr>
<td>SDA</td>
<td>23</td>
<td>DIO</td>
<td>5-V</td>
<td>PC serial control data interface input/output.</td>
</tr>
<tr>
<td>SDIN</td>
<td>22</td>
<td>DI</td>
<td>5-V Pulldown</td>
<td>Serial analog audio input. SDIN supports three discrete (stereo) data formats.</td>
</tr>
<tr>
<td>SSTIMMER</td>
<td>32</td>
<td>AI</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TEST</td>
<td>26</td>
<td>DI</td>
<td></td>
<td>Factory test pin. Connect directly to DVSS.</td>
</tr>
<tr>
<td>VR_ANA</td>
<td>12</td>
<td>P</td>
<td></td>
<td>Internally regulated 1.8-V analog supply voltage. This pin must not be used to power external devices.</td>
</tr>
<tr>
<td>VR_DIG</td>
<td>18</td>
<td>P</td>
<td></td>
<td>Internally regulated 1.8-V digital supply voltage. This pin must not be used to power external devices.</td>
</tr>
<tr>
<td>VREG</td>
<td>31</td>
<td>P</td>
<td></td>
<td>Digital regulator output. Not to be used for powering external circuits.</td>
</tr>
</tbody>
</table>

Table 2: Pin functions
Table 3: Recommended operating conditions

### B. MAIN AMPLIFIER (TS4962M)(2.5 W option)

#### a. General Description

The TS4962M is a differential Class-D BTL power amplifier. It is able to drive up to 2.3W into a 4Ω load and 1.4W into an 8Ω load at 5V. It achieves outstanding efficiency (88%typ.) compared to classical Class-AB audio amps. The gain of the device can be controlled via two external gain-setting resistors. Pop & click reduction circuitry provides low on/off switch noise while allowing the device to start within 5ms. A standby function (active low) allows the reduction of current consumption to 10nA typ.

#### b. Features

- Operating from VCC = 2.4V to 5.5V
- Standby mode active low
- Output power: 3W into 4Ω and 1.75W into 8Ω
- with 10% THD+N max and 5V power supply.
- Output power: 2.3W @5V or 0.75W @ 3.0V
- into 4Ω with 1% THD+N max.
- Output power: 1.4W @5V or 0.45W @ 3.0V
- into 8Ω with 1% THD+N max.
- Adjustable gain via external resistors
- Low current consumption 2mA @ 3V
- Efficiency: 88% typ.
- Signal to noise ratio: 85dB typ.
- PSRR: 63dB typ. @217Hz with 6dB gain
- PWM base frequency: 250kHz
- Low pop & click noise
- Thermal shutdown protection
- Available in flip-chip 9 x 300μm (Pb-free)

c. Pin descriptions and functions:

![Figure 3: Pin description](image)

IN+: positive differential input
IN-: negative differential input
VDD: analog power supply
GND: power supply ground
STBY: standby pin (active low)
OUT+: positive differential output
OUT-: negative differential output
Table 4: Recommended operating conditions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{CC}$</td>
<td>Supply voltage(^{(1)})</td>
<td>2.4 to 5.5</td>
<td>V</td>
</tr>
<tr>
<td>$V_{IC}$</td>
<td>Common mode input voltage range(^{(2)})</td>
<td>0.5 to $V_{CC} - 0.8$</td>
<td>V</td>
</tr>
<tr>
<td>$V_{STBY}$</td>
<td>Standby voltage input: (^{(3)}) Device ON Device OFF</td>
<td>$1.4 \leq V_{STBY} \leq V_{CC}$ GND $\leq V_{STBY} \leq 0.4$ (^{(4)})</td>
<td>V</td>
</tr>
<tr>
<td>$R_L$</td>
<td>Load resistor</td>
<td>$\geq 4$</td>
<td>$\Omega$</td>
</tr>
<tr>
<td>$R_{thja}$</td>
<td>Thermal resistance junction to ambient (^{(5)})</td>
<td>90</td>
<td>$^\circ C/W$</td>
</tr>
</tbody>
</table>

1. For $V_{CC}$ from 2.4V to 2.5V, the operating temperature range is reduced to $0^\circ C \leq T_{amb} \leq 70^\circ C$.
2. For $V_{CC}$ from 2.4V to 2.5V, the common mode input range must be set at $V_{CC}/2$.
3. Without any signal on $V_{STBY}$, the device will be in standby.
4. Minimum current consumption is obtained when $V_{STBY} = $ GND.
5. With heat sink surface $= 125mm^2$.

C. HEADPHONE AMPLIFIER STAGE

Headphone is a SoC (single on chip) configuration in mainboard, design scheme is shown in figure 4.
4. POWER STAGE

Power socket is used for taking voltages which are 3.3V, 12V, 5V and 24V(VDD_Audio). These voltages are produced in power card. Also socket is used for giving dimming, backlight and standby signals with power card. It is shown in figure 5.

24V(VDD_Audio) goes directly to the audio side, through power socket other incoming voltages from power card are converted several voltages.
General Description and Features

**Single P-Channel 2.5V Specified PowerTrench® MOSFET**
-20 V, -4.0 A, 65 mΩ

**Features**
- Max rD(on) = 65 mΩ at VDS = -4.5 V, ID = -4.0 A
- Max rD(on) = 100 mΩ at VDS = -2.5 V, ID = -3.2 A
- Fast switching speed
- Low gate charge (11nC typical)
- High performance trench technology for extremely low rD(on)
- SuperSO™-8 package; small footprint (72% smaller than standard SO-8), low profile (1 mm thick)
- Termination is Lead-free and RoHS Compliant

**General Description**
This P-Channel 2.5V specified MOSFET is produced using Fairchild's advanced PowerTrench® process that has been especially tailored to minimize on-state resistance and yet maintain low gate charge for superior switching performance. These devices have been designed to offer exceptional power dissipation in a very small footprint for applications where the larger packages are impractical.

**Applications**
- Lead switch
- Battery protection
- Power management

---

**TPS65251**

a) **General Description**

The TPS65251 features three synchronous wide input range high efficiency buck converters. The converters are designed to simplify its application while giving the designer the option to optimize their usage according to the target application.

The converters can operate in 5-, 9-, 12- or 15-V systems and have integrated power transistors. The output voltage can be set externally using a resistor divider to any value between 0.8 V and close to the input supply. Each converter features enable pin that allows a delayed start-up for sequencing purposes, soft start pin that allows adjustable soft-start time by choosing the soft-start capacitor, and a current limit (RLIMx) pin that enables designer to adjust current limit by selecting an external resistor and optimize the choice of inductor. The current mode control allows a simple RC compensation.

The switching frequency of the converters can either be set with an external resistor connected to ROSC pin or can be synchronized to an external clock connected to SYNC pin if needed. The switching regulators are designed to operate from 300 kHz to 2.2 MHz. 180° out of phase operation between Buck 1 and Buck 2, 3 (Buck 2 and 3 run in phase) minimizes the input filter requirements.
TPS65251 features a supervisor circuit that monitors each converter output. The PGOOD pin is asserted once sequencing is done, all PG signals are reported and a selectable end of reset time lapses. The polarity of the PGOOD signal is active high.

TPS65251 also features a light load pulse skipping mode (PSM) by allowing the LOW_P pin tied to V3V. The PSM mode allows for a reduction on the input power supplied to the system when the host processor is in stand-by (low activity) mode.

b) Features

• Wide Input Supply Voltage Range (4.5 V - 18 V)
• 0.8 V, 1% Accuracy Reference
• Continuous Loading: 3 A (Buck 1), 2 A (Buck 2 and 3)
• Maximum Current: 3.5 A (Buck 1), 2.5 A (Buck 2 and 3)
• Adjustable Switching Frequency 300 kHz - 2.2 MHz Set By External Resistor
• Dedicated Enable for Each Buck
• External Synchronization Pin for Oscillator
• External Enable/Sequencing and Soft Start Pins
• Adjustable Current Limit Set By External Resistor
• Soft Start Pins
• Current-Mode Control With Simple Compensation Circuit
• Power Good
• Optional Low Power Mode Operation for Light Loads
• QFN Package, 40-Pin 6 mm x 6 mm RHA

APPLICATIONS

• Set Top Boxes
• Blu-ray DVD
• Security Camera
• Car Audio/Video
• DTV
• DVR
Table 5: Recommended operating conditions

<table>
<thead>
<tr>
<th>NAME</th>
<th>NO.</th>
<th>I/O</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>RLIM3</td>
<td>1</td>
<td>I</td>
<td>Current limit setting for Buck 3. Fit a resistor from this pin to ground to set the peak current limit on the output inductor.</td>
</tr>
<tr>
<td>SS3</td>
<td>2</td>
<td>I</td>
<td>Soft start pin for Buck 3. Fit a small ceramic capacitor to this pin to set the converter soft start time.</td>
</tr>
<tr>
<td>COMP3</td>
<td>3</td>
<td>O</td>
<td>Compensation for Buck 3. Fit a series RC circuit to this pin to complete the compensation circuit of this converter.</td>
</tr>
<tr>
<td>FB3</td>
<td>4</td>
<td>I</td>
<td>Feedback input for Buck 3. Connect a divider set to 0.8V from the output of the converter to ground.</td>
</tr>
<tr>
<td>SYNC</td>
<td>5</td>
<td>I</td>
<td>Synchronous clock input. If there is a sync clock in the system, connect to the pin. When not used connect to GND.</td>
</tr>
<tr>
<td>ROGC</td>
<td>6</td>
<td>I</td>
<td>Oscillator set. This resistor sets the frequency of internal autonomous clock. If external synchronization is used resistor should be fitted and set to ~70% of external clock frequency.</td>
</tr>
<tr>
<td>FB1</td>
<td>7</td>
<td>I</td>
<td>Feedback pin for Buck 1. Connect a divider set to 0.6 V from the output of the converter to ground.</td>
</tr>
<tr>
<td>COMP1</td>
<td>8</td>
<td>O</td>
<td>Compensation pin for Buck 1. Fit a series RC circuit to this pin to complete the compensation circuit of this converter.</td>
</tr>
<tr>
<td>SS1</td>
<td>9</td>
<td>I</td>
<td>Soft start pin for Buck 1. Fit a small ceramic capacitor to this pin to set the converter soft start time.</td>
</tr>
<tr>
<td>RLIM1</td>
<td>10</td>
<td>I</td>
<td>Current limit setting pin for Buck 1. Fit a resistor from this pin to ground to set the peak current limit on the output inductor.</td>
</tr>
<tr>
<td>EN1</td>
<td>11</td>
<td>I</td>
<td>Enable pin for Buck 1. A low level signal on this pin enables it. If pin is left open a weak internal pull-up to 3V will allow for automatic enable. For a delayed start-up add a small ceramic capacitor from this pin to ground.</td>
</tr>
<tr>
<td>BST1</td>
<td>12</td>
<td>I</td>
<td>Bootstrap capacitor for Buck 1. Fit a 47-nF ceramic capacitor from this pin to the switching node.</td>
</tr>
<tr>
<td>VIN1</td>
<td>13</td>
<td>I</td>
<td>Input supply for Buck 1. Fit a 10-µF ceramic capacitor close to this pin.</td>
</tr>
<tr>
<td>LX1</td>
<td>14, 15</td>
<td>O</td>
<td>Switching node for Buck 1</td>
</tr>
<tr>
<td>LX2</td>
<td>16, 17</td>
<td>O</td>
<td>Switching node for Buck 2</td>
</tr>
<tr>
<td>VIN2</td>
<td>18</td>
<td>I</td>
<td>Input supply for Buck 2. Fit a 10-µF ceramic capacitor close to this pin.</td>
</tr>
<tr>
<td>BST2</td>
<td>19</td>
<td>I</td>
<td>Bootstrap capacitor for Buck 2. Fit a 47-nF ceramic capacitor from this pin to the switching node.</td>
</tr>
</tbody>
</table>
MP1484

a) General Description

The MP1484 is a monolithic synchronous buck regulator. The device integrates top and bottom 85mΩ MOSFETS that provide 3A of continuous load current over a wide operating input voltage of 4.75V to 18V. Current mode control provides fast transient response and cycle-by-cycle current limit.

An adjustable soft-start prevents inrush current at turn-on and in shutdown mode, the supply current drops below 1μA.

The MP1484 is PIN compatible to the MP1482 2A/18V/Synchronous Step-Down Converter.

b) Features

• 3A Continuous Output Current
• Wide 4.75V to 18V Operating Input Range
• Integrated 85mΩ Power MOSFET Switches
- Output Adjustable from 0.925V to 20V
- Up to 95% Efficiency
- Programmable Soft-Start
- Stable with Low ESR Ceramic Output Capacitors
- Fixed 340KHz Frequency
- Cycle-by-Cycle Over Current Protection
- Input Under Voltage Lockout
- Thermally Enhanced 8-Pin SOIC Package

APPLICATIONS
- FPGA, ASIC, DSP Power Supplies
- LCD TV
- Green Electronics/Appliances
- Notebook Computers

Figure 8: General description

<table>
<thead>
<tr>
<th>PACKAGE REFERENCE</th>
</tr>
</thead>
<tbody>
<tr>
<td>TOP VIEW</td>
</tr>
<tr>
<td>BS 1</td>
</tr>
<tr>
<td>8 SS</td>
</tr>
<tr>
<td>EXPOSED PAD ON BACKSIDE CONNECT TO GND PIN</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Part Number*</th>
<th>Package</th>
<th>Temperature</th>
</tr>
</thead>
<tbody>
<tr>
<td>MP1484EN</td>
<td>SOIC8N (Exposed Pad)</td>
<td>-20°C to +85°C</td>
</tr>
</tbody>
</table>

* For Tape & Reel, add suffix -Z (e.g. MP1484EN-Z)
For Lead Free, add suffix -LF (e.g. MP1484EN-LF-Z)

**ABSOLUTE MAXIMUM RATINGS**
- Supply Voltage $V_{IN}$: $-0.3V$ to $+24V$
- Switch Voltage $V_{SW}$: $-1V$ to $V_{IN} + 0.3V$
- Boost Voltage $V_{BS}$: $V_{SW} - 0.3V$ to $V_{SW} + 6V$
- All Other Pins: $-0.3V$ to $+6V$
- Junction Temperature: $-150°C$
- Lead Temperature: $260°C$
- Storage Temperature: $-65°C$ to $+150°C$

**Recommended Operating Conditions**
- Input Voltage $V_{IN}$: $4.75V$ to $18V$
- Output Voltage $V_{OUT}$: $0.925V$ to $20V$
- Ambient Operating Temp: $-20°C$ to $+85°C$

**Thermal Resistance**
- $\theta_{JA}$ and $\theta_{JC}$
- SOIC8N (Exposed Pad): $50\ldots10\ldots°C/W$

**Notes:**
1) Exceeding these ratings may damage the device.
2) The device is not guaranteed to function outside of its operating conditions.
3) Measured on approximately 1" square of 1 oz copper.
Table 7: Pin functions

<table>
<thead>
<tr>
<th>Pin #</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>BS</td>
<td>High-Side Gate Drive Boost Input. BS supplies the drive for the high-side N-Channel MOSFET switch. Connect a 0.01μF capacitor from SW to BS to power the high side switch.</td>
</tr>
<tr>
<td>2</td>
<td>IN</td>
<td>Power Input. IN supplies the power to the IC, as well as the step-down converter switches. Drive IN with a 4.7V to 18V power source. See Input Capacitor.</td>
</tr>
<tr>
<td>3</td>
<td>SW</td>
<td>Power Switching Output. SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load. Note that a capacitor is required from SW to BS to power the high side switch.</td>
</tr>
<tr>
<td>4</td>
<td>GND</td>
<td>Ground (Connect the exposed pad to Pin 4).</td>
</tr>
<tr>
<td>5</td>
<td>FB</td>
<td>Feedback Input. FB senses the output voltage and regulates it. Drive FB with a resistive voltage divider connected to it from the output voltage. The feedback threshold is 0.925V. See Setting the Output Voltage.</td>
</tr>
<tr>
<td>6</td>
<td>COMP</td>
<td>Compensation Node. COMP is used to compensate the regulation control loop. Connect a series RC network from COMP to GND. In some cases, an additional capacitor from COMP to GND is required. See Compensation Components.</td>
</tr>
<tr>
<td>7</td>
<td>EN</td>
<td>Enable Input. EN is a digital input that turns the regulator on or off. Drive EN high to turn on the regulator; low to turn it off. Attach to IN with a 100kΩ pull up resistor for automatic startup.</td>
</tr>
<tr>
<td>8</td>
<td>SS</td>
<td>Soft-Start Control Input. SS controls the soft-start period. Connect a capacitor from SS to GND to set the soft-start period. A 0.1μF capacitor sets the soft-start period to 15ms. To disable the soft-start feature, leave SS unconnected.</td>
</tr>
</tbody>
</table>

**APL5910**

**a) General Description**

The APL5910 is a 1A ultra low dropout linear regulator. The IC needs two supply voltages, one is a control voltage (VCNTL) for the control circuitry, the other is a main supply voltage (VIN) for power conversion, to reduce power dissipation and provide extremely low dropout voltage. The APL5910 integrates many functions. A Power-On-Reset (POR) circuit monitors both supply voltages on VCNTL and VIN pins to prevent erroneous operations. The functions of thermal shutdown and current-limit protect the device against thermal and current over-loads. A POK indicates that the output voltage status with a delay time set internally. It can control other converter for power sequence. The APL5910 can be enabled by other power systems. Pulling and holding the EN voltage below 0.4V shuts off the output.

The APL5910 is available in a SOP-8P package which features small size as SOP-8 and an Exposed Pad to reduce the junction-to-case resistance to extend power range of applications.

**b) Features**

- Ultra Low Dropout
  - 0.12V (Typical) at 1A Output Current
- 0.8V Reference Voltage
- High Output Accuracy
  - ±1.5% over Line, Load, and Temperature Range
- Fast Transient Response
- Adjustable Output Voltage
- Power-On-Reset Monitoring on Both VCNTL and VIN Pins
- Internal Soft-Start
- Current-Limit and Short Current-Limit Protections
- Thermal Shutdown with Hysteresis
- Open-Drain VOUT Voltage Indicator (POK)
- Low Shutdown Quiescent Current (< 30mA)
- Shutdown/Enable Control Function
- Simple SOP-8P Package with Exposed Pad
- Lead Free and Green Devices Available (RoHS Compliant)

**APPLICATIONS**
- Motherboards, VGA Cards
- Notebook PCs
- Add-in Cards

![Figure 9: Pin configuration](image)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Range</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCMN</td>
<td>VCNTL Supply Voltage</td>
<td>3.0 ~ 6.5</td>
<td>V</td>
</tr>
<tr>
<td>VIN</td>
<td>VIN Supply Voltage</td>
<td>1.0 ~ 5.5</td>
<td>V</td>
</tr>
<tr>
<td>VOUT</td>
<td>VOUT Output Voltage (when VCMN=VOUT&gt;1.4V)</td>
<td>0.8 ~ VOUT - VCMN</td>
<td>V</td>
</tr>
<tr>
<td>IOUT</td>
<td>VOUT Output Current</td>
<td>0 ~ 1</td>
<td>A</td>
</tr>
<tr>
<td>R2</td>
<td>FB to GND</td>
<td>1k ~ 34k</td>
<td>Ω</td>
</tr>
<tr>
<td>COUT</td>
<td>VOUT Output Capacitance</td>
<td></td>
<td>μF</td>
</tr>
<tr>
<td>ESROUT</td>
<td>ESR of VOUT Output Capacitor</td>
<td></td>
<td>mΩ</td>
</tr>
<tr>
<td>TA</td>
<td>Ambient Temperature</td>
<td>-40 ~ 65</td>
<td>°C</td>
</tr>
<tr>
<td>TJ</td>
<td>Junction Temperature</td>
<td>-40 ~ 125</td>
<td>°C</td>
</tr>
</tbody>
</table>

Table 8: Recommended operating conditions
**LM1117**

**a) General Description**

The LM1117 is a series of low dropout voltage regulators with a dropout of 1.2V at 800mA of load current. It has the same pin-out as National Semiconductor’s industry standard LM317.

The LM1117 is available in an adjustable version, which can set the output voltage from 1.25V to 13.8V with only two external resistors. In addition, it is also available in five fixed voltages, 1.8V, 2.5V, 2.85V, 3.3V, and 5V.

The LM1117 offers current limiting and thermal shutdown. Its circuit includes a zener trimmed bandgap reference to assure output voltage accuracy to within ±1%.

The LM1117 series is available in LLP, TO-263, SOT-223, TO-220, and TO-252 D-PAK packages. A minimum of 10µF tantalum capacitor is required at the output to improve the transient response and stability.

**b) Features**

- Available in 1.8V, 2.5V, 2.85V, 3.3V, 5V, and Adjustable Versions
- Space Saving SOT-223 and LLP Packages
- Current Limiting and Thermal Protection
- Output Current 800mA
- Line Regulation 0.2% (Max)
- Load Regulation 0.4% (Max)
- Temperature Range:

### Table 9: Pin description

<table>
<thead>
<tr>
<th>PIN</th>
<th>NO.</th>
<th>NAME</th>
<th>FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>P0K</td>
<td>Power-OK signal output pin. This pin is an open-drain output used to indicate the status of output voltage by sensing FB voltage. This pin is pulled low when output voltage is not within the Power-OK voltage window.</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>EN</td>
<td>Active-high enable control pin. Applying and holding the voltage on this pin below the enable voltage threshold shuts down the output. When re-enabled, the IC undergoes a new soft-start process. When left this pin open, an internal pull-up current (5µA typical) pulls the EN voltage and enables the regulator.</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>VIN</td>
<td>Main supply input pin for voltage conversions. A decoupling capacitor (≥10µF recommended) is usually connected near this pin to filter the voltage noise and improve transient response. The voltage on this pin is monitored for Power-On/Reset purpose.</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>VCTRL</td>
<td>Bias voltage input pin for internal control circuitry. Connect this pin to a voltage source (+5V recommended). A decoupling capacitor (1µF typical) is usually connected near this pin to filter the voltage noise. The voltage at this pin is monitored for Power-On/Reset purpose.</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>NC</td>
<td>No Connection</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>VOUT</td>
<td>Output pin of the regulator. Connecting this pin to load and output capacitors (10µF at least) is required for stability and improving transient response. The output voltage is programmed by the resistor-divider connected to FB pin. The VOUT can provide 1A (max.) load current to loads. During shutdown, the output voltage is quickly discharged by an internal pull-down MOSFET.</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>FB</td>
<td>Voltage Feedback Pin. Connecting this pin to an external resistor divider receives the feedback voltage of the regulator.</td>
<td></td>
</tr>
</tbody>
</table>
- LM1117 0˚C to 125˚C
- LM1117I −40˚C to 125˚C

- **Applications**
  - 2.85V Model for SCSI-2 Active Termination
  - Post Regulator for Switching DC/DC Converter
  - High Efficiency Linear Regulators
  - Battery Charger
  - Battery Powered Instrumentation

5. **MICROCONTROLLER (MSTAR MSD8WB9BX)**

  a) **General Description**

The MSD8WB9BX is MStar’s most up-to-date system-on-chip flagship for flat panel integrated digital television products. Building on the success of MStar’s current solutions, the MSD8WB9BX hosts the most advanced picture processing engine, **MStarACE<sup>Pro</sup>**, for all the Experts in various fields of TV video quality tuning to develop the state-of-the-art TV and DTV system.

**MStarACE<sup>Pro</sup>**, the Professional Edition of MStar color processor, includes all MStar’s successful color-tuning tools and a newly added multi-dimensional color/sharpening/NR formula that can quickly reflect subtle or sudden changes in even darker, brighter or mixture scenes. With this ultimate color processor, a specially designed color remapping system for modern wider gamut displays and an easy-to-use color-tool UI, developers can quickly and easily identify PQ characteristic from the most high-end panel models to the most conventional panel models.

The MSD8WB9BX integrates DTV/multi-media all-purpose AV decoder, DVB-T/DVB-C demodulator, VIF demodulator and Sound/Video processor into a single device. This allows the overall BOM to be reduced significantly making the MSD8WB9BX a very cost effective multi-media DTV solution.

The MSD8WB9BX enables feature rich products that bring differentiation to the DTV market. By the use of AV decoder capable of decoding a plethora of high definition content with Ethernet, USB 2.0 connectivity and a powerful CPU/GPU, an MSD8WB9BX based system can provide a high quality networking application and media-center experience.

For standard users, the MSD8WB9BX provides multi-standard analog TV support with adaptive 3D video decoding and YBI data extraction. The build-in audio decoder is capable of decoding FM, AM, NICAM, A2, BTSC and EIA-J sound standards. The MSD8WB9BX supplies all the necessary A/V inputs and outputs to complete a receiver design including a multi-port HDMI receiver and component video ADC. All input selection multiplexed for video and audio are integrated, including full SCART support with CVBS output.

To meet the increasingly popular energy legislative requirements without the use of additional hardware, the MSD8WB9BX has an ultra low power standby mode during which an embedded MCU can act upon standby events and wake up the system as required.
b) Features

**MSD8W89BX**, a single chip iDTV solution that supports channel decoding, MPEG decoding, and media-center functionality enabled by a high performance AV CODEC and CPU. Key features include:

1. **DVB-T/C Front-End Demodulator**
2. **A Multi-Standard A/V Format Decoder**
3. **The MACE™ Video Processor**
4. **Home Theater Sound Processor**
5. **Internet and Variety of Connectivity Support**
6. **Dual-stream decoder for 3D contents**
7. **Multi-Purpose CPU for OS and Multimedia**
8. **Peripheral and Power Management**

**High Performance Micro-processor**
- Ultra high speed/performance 32-bit RISC CPU
- Memory Management Unit for Linux support
- Three full duplex UARTs
- Supports USB and ISP programming
- DMA Engine

**Transport Stream De-multiplexer**
- Supports two parallel TS interfaces, with or without sync signal
- Supports TS input and output for external CI module
- Supports external demodulator of ISDB, DTMBS, or DVD-T2/S2
- Maximum TS data rate is 16 MB/sec
- 32 general purpose PID filters and section filters for each transport stream de-multiplexer
- Supports additional audio/video/PCR filters
- Supports TS DMA channel for time-shifting PVR
- Supports 3DES/DES and AES encryption/decryption

**MPEG-2 Video Decoder**
- ISO/IEC 13818-2 MPEG-2 video MP@HL
- Automatic frame rate conversion
- Supports resolution up to HDTV (1080i, 720p) and SDTV

**MPEG-4 Video Decoder**
- ISO/IEC 14496-2 MPEG-4 ASP video decoding
- Supports resolutions up to HDTV (1080p@30fps)
- Supports DivX® Home Theater & HD profiles
- Optional Plus HD
- Supports VC-1 Optional, FLV video format decoding

**H.264 Decoder**
- ITU-T H.264, ISO/IEC 14496-10 video decoding
- Main and high profile up to level 4.1, MVC video decoding
- Supports dual-stream decoding
- Supports resolutions for all DVB, ATSC, HDTV, DVD and VCD
- Supports resolution up to 1080p@30fps
- Supports CABAC and CAVLC stream types
- Processing of ES and PES streams, extraction and provision of time stamps
- Up to 40 Mbits bitrate (Blu-ray spec.)

**AVS Decoder**
- Supports Jihun profile, level 6.0
- Supports resolution up to 1920x1088 @30fps
- Supports bit-rate up to 20Mbps
- Supports dual-stream decoding for 3D content

**RealMedia Decoder**
- Supports maximum resolution up to 1080p@30fps
- Supports RV8, RV9, RV10, RA8-LBR and HE-AAC decoders
- Supports file formats with RM and RMVB
- Supports Picture Re-sampling
- Supports in-loop de-block for B-frame
Hardware MPEG
- Supports sequential mode, single scan
- Supports both color and grayscale pictures
- Following the file header scan the hardware decoder fully handles the decode process
- Supports programmable Region of Interest (ROI)
- Supports formats: 422/411/420/444/422T
- Supports scaling down ratios: 1/2, 1/4, 1/8
- Supports picture rotation

NTSC/PAL/SECAM Video Decoder
- Supports NTSC-M, NTSC-I, NTSC-4.43, PAL (B, D, G, H, M, N, I, Ne), and SECAM standards
- Automatic standard detection
- Motion adaptive 3D comb filter
- Four configurable CVBS & Y/C S-video inputs
- Supports Teletext, Closed Caption (analog CC 608/ analog CC 708/digital CC 608/digital CC 708), V-chip and SCTE

Multi-Standard TY Sound Processor
- SIF audio decoding
- Supports BTSC/A2/EIA-3 demodulation
- Supports NICAM/PWM demodulation
- Supports MTS Mono/Stereo/SAP in BTSC/ EIA-3 mode
- Supports Mono/Stereo/Dual in A2/NICAM mode
- Built-in audio sampling rate conversion (SRC)
- Audio processing for loudspeaker channel, including volume, balance, mute, tone, EQ, virtual stereo/surround and treble/bass controls
- Advanced sound processing options available, for example: Dolby*, SRS*, BBE*, QSound®, Audyssey®
- Supports digital audio format decoding:
  - MPEG-1, MPEG-2 (Layer 1/II), MP3, Dolby Digital (AC-3)™, AAC-LC, HE-AAC, WMA, and WMA9 Pro
  - Supports Optional Dolby Digital Plus, Dolby

Dolby, and MS16 multistream decoder, including Dolby Digital Encoder for transcoding streams to Dolby Digital 5.1 (DDCO)
- Supports MPEG Audio, Dolby Digital, Dolby Digital Plus, HE-AAC format AD (Audio Description)
- Supports MPEG audio encoding
- Supports time-shifting PVR

Audio Interface
- One SIF audio input interface with minimal external saw filters
- Six L/R audio line-inputs
- Three L/R outputs for main speakers and additional TV line-output
- One embedded stereo headphone driver
- L2S digital audio output
- SPI/P&D digital audio output & input
- HDMI™ audio channel processing
- Programmable delay for audio/video synchronization

Analog RGB Compliant Input Ports
- Three analog ports support up to 1080P
- Supports PC RGB input up to SXGA@75Hz
- Supports HDTV RGB/YPrPb/YPbPr
- Supports Composite Sync and S0G
- Sync-on-Green
- Automatic color calibration

Analog RGB Auto-Configuration & Detection
- Auto input signal format and mode detection
- Auto-tuning function including phasing, positioning, offset, gain, and jitter detection
- Sync Detection for H/V Sync

DVI/HDCP HDMI Compliant Input Ports
- Four HDMI/DVI input ports
- HDMI 1.3/1.4 Compliant
- MStar Switch for fast HDMI switching
- HDCP 1.1/1.3 Compliant
- 215MHz @ 1080P 60Hz input with 12-bit Deep-color support
- Supports HDMI CEC
- Supports HDMI 1.4a 3D format input
- Supports HDMI 4K@2K input
- Supports HDMI ARC
- Single link DVI 1.0 compliant

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*® Registered trademark of SRS Labs, Inc.
*® Registered trademark of QSound Labs, Inc.
*® Registered trademark of Audyssey Laboratories, Inc.
© Please see Ordering Guide for details.
© Registered trademark of HDMI Licensing LLC.
- Robust receiver with excellent long-cable support
- **MStar Advanced Color Engine - Professional Edition (MStarACE™)**
  - 10/12-bit internal data processing
  - High hips and fully programmable multi-function scaling engine
    - Nonlinear video scaling supports various modes including Panorama
    - Supports dynamic scaling for RM, VC-1/LHDC
  - High-Quality DTV video processor
    - 3D motion video deinterlace with motion object stabilizer
    - Edge-oriented denoiser with edge detection and repair
    - 3D multi-purpose noise reduction for DTV or low rate input
    - MPEG artifact removal including de-blocking and mosquito noise reduction
    - Arbitrary frame rate conversion
  - Automatic picture enhancement:
    - Includes all features in MACE 24/4 engine
    - 3D adaptive color control enabling vivid visual reception in the true world from most dark to most bright scenes
    - 3D adaptive sharpening control enabling crystal clear visual reception without distorting scene reality
    - Supports sRGB and wYCC color processing
    - Supports HDMI 1.3 deep color format
    - Supports enhanced and seamless color mapping for wider gamut panels
    - Programmable 12-bit RGB gamut CCLUT
    - Supports 2D to 3D conversion

- **Output Interface**
  - Single/dual link 8/10-bit LVDS output
  - Supports panel resolution up to Full-HD (1920×1080) @ 60Hz
  - Supports dithering options
  - Spurious spectrum output frequency for EMI suppression

- **CVBS Video Encoder**
  - Supports all NTSC/PAL TV Standard
  - Stand-alone scaling engine
  - Programmable Hue, Contract, Brightness
  - Supports TTX/OCW/ISDB output

- **CVBS Video Outputs**
  - Allows CVBS output from CVBS encoder
  - Supports CVBS bypass output

- **3D-like Graphics Engine**
  - Hardware Graphics Engine for responsive interactive applications
    - Supports point draw, line draw, rectangle draw/fill, text draw and textured draw
    - Bilinear, bi-linear, trapezoidal Bilinear, mirror Bilinear and rotate Bilinear
    - Supports alpha and destination alpha compare
    - Raster Operation (ROP)
    - Supports Porter-Duff

- **VIF Demodulator**
  - Compliant with NTSC, M/N, PAL B, G/H, I, D/K, SECAM I/L standards
  - Digital low IF architecture
  - Audio/Video dual-path processor
  - Stepped-gain PGA with 25 dB tuning range and 1 dB tuning resolution
  - Maximum IF gain of 37 dB
  - Programmable TLP to accommodate different tuner gain and SAW filter insertion loss to optimize noise and linearity performance
  - Multi-standard processing with single SAW
  - Supports silicon tuner low IF output architecture

- **DVB-T/DVB-C Demodulator**
  - Digital carrier frequency offset correction: ±500KHz
  - Optimized for SFN channels with pre/post-cursive echoes inside/outside the guard
  - Acquisition range ±857KHz includes up to 3× 24/6 MHz transmitter offset
  - Meets Nordic unified 1.0.3, D-Book 5.0, EICTA E-Book/C-Book test requirement
  - ITU 6.3 Annex A/C, DVB-C (EN 300 429) compliant
  - Supports DVB-C 0.7-7MHz simulcast symbol rate
  - ±100KHz internal carrier offset recovery range
  - 6.8 μsues echo cancellation at 7 Maysyn’s
  - Supports IF, low-IF inputs
  - Ultra-fast automatic blind UHF/VHF channel scan (constellations and symbol rate)

- **Connectivity**
  - Two USB 2.0 host ports
  - USB architecture designed for efficient support of external storage devices in conjunction with off-air broadcasting
  - Built-in 10/100Mbit Ethernet PHY and MAC
  - MStar proprietary 1F for Wi-Fi and Bluetooth companion chips

- **Miscellaneous**
  - DRAM interface supporting up to two 16-bit DDR3 @ 1.6GHz
  - Supports RTC
  - Supports Common Interface for conditional access support
  - Bootable SPI interface with serial flash support
  - Parallel interface for NAND flash support
  - Power control module with ultra low power MGU available in standby mode
  - 560-ball LFPGA package
  - Operating Voltage: 1.2V (core), 1.5V (DDR3), 2.6V and 3.3V (IO and analog)
6. 1Gb DDR3 SDRAM

**Hynix H5TQ1G630FA**

**a) Description**

The H5TQ1G6(8)3DFR-xxx series are a 1,073,741,824-bit CMOS Double Data Rate III (DDR3) Synchronous DRAM, ideally suited for the main memory applications which requires large memory density and high bandwidth. Hynix 1Gb DDR3 SDRAMs offer fully synchronous operations referenced to both rising and falling edges of the clock. While all addresses and control inputs are latched on the rising edges of the CK (falling edges of the CK), Data, Data strobes and Write data masks inputs are sampled on both rising and falling edges of it. The data paths are internally pipelined and 8-bit prefetched to achieve very high bandwidth.

**b) Features**

- DQ Power & Power supply : VDD & VDDQ = 1.5V +/- 0.075V
- DQ Ground supply : VSSQ = Ground
- Fully differential clock inputs (CK, CK) operation
- Differential Data Strobe (DQS, DQS)
- On chip DLL align DQ, DQS and DQS transition with CK transition
- DM masks write data-in at the both rising and falling edges of the data strobe
- All addresses and control inputs except data, data strobes and data masks latched on the rising edges of the clock
- Programmable CAS latency 6, 7, 8, 9, 10, 11, 12, 13 and 14 supported
- Programmable additive latency 0, CL-1, and CL-2 supported
- Programmable CAS Write latency (CWL) = 5, 6, 7, 8, 9, 10
- Programmable burst length 4/8 with both nibble sequential and interleave mode
- Programmable PASR(Partial Array Self-Refresh) for Digital consumer Applications.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.3V Supply Voltages</td>
<td>V&lt;sub&gt;DD&lt;/sub&gt; 3</td>
<td>3.14</td>
<td>3.46</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>2.5V Supply Voltages</td>
<td>V&lt;sub&gt;DD&lt;/sub&gt; 25</td>
<td>2.38</td>
<td>2.62</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>1.8V Supply Voltages</td>
<td>V&lt;sub&gt;DD&lt;/sub&gt; 18</td>
<td>1.70</td>
<td>1.90</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>1.5V Supply Voltages</td>
<td>V&lt;sub&gt;DD&lt;/sub&gt; 15</td>
<td>1.43</td>
<td>1.57</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>1.2V Supply Voltages</td>
<td>V&lt;sub&gt;DD&lt;/sub&gt; 12</td>
<td>1.16</td>
<td>1.20</td>
<td>1.24</td>
<td>V</td>
</tr>
<tr>
<td>Junction Temperature</td>
<td>T&lt;sub&gt;j&lt;/sub&gt;</td>
<td></td>
<td></td>
<td>125</td>
<td>°C</td>
</tr>
<tr>
<td>Case Temperature</td>
<td>T&lt;sub&gt;c&lt;/sub&gt;</td>
<td></td>
<td></td>
<td>100</td>
<td>°C</td>
</tr>
</tbody>
</table>

Table 10: Recommended operating conditions
• Programmable BL=4 supported (tCCD=2CLK) for Digital consumer Applications.
• Programmable ZQ calibration supported
• BL switch on the fly
• 8 banks
• Average Refresh Cycle (Tease of 0 oC~ 95 oC)
  - 7.8 µs at -40oC ~ 85 oC
  - 3.9 µs at 85oC ~ 95 oC
  - Commercial Temperature (0oC ~ 85 oC)
  - Industrial Temperature (-40oC ~ 85 oC)
• Auto Self Refresh supported
• JEDEC standard 78ball FBGA(x8), 96ball FBGA(x16)
• Driver strength selected by EMRS
• Dynamic On Die Termination supported
• Asynchronous RESET pin supported
• TDQS (Termination Data Strobe) supported (x8 only)
• Write Levelization supported
• On Die Thermal Sensor supported
• 8 bit pre-fetch

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Rating</th>
<th>Units</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD</td>
<td>Supply Voltage</td>
<td>1.425</td>
<td>1.500</td>
<td>V</td>
</tr>
<tr>
<td>VDDQ</td>
<td>Supply Voltage for Output</td>
<td>1.425</td>
<td>1.500</td>
<td>V</td>
</tr>
</tbody>
</table>

**Notes:**
1. Under all conditions, VDDQ must be less than or equal to VDD.
2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.

**Table 11: Recommended operating conditions**

### 7. 1Gb G-die DDR3 SDRAM

**Samsung K4B1G1646G**

a) **Key Features**

• JEDEC standard 1.5V ± 0.075V Power Supply
• VDDQ = 1.5V ± 0.075V
• 400 MHz fCK for 800Mb/sec/pin, 533MHz fCK for 1066Mb/sec/pin, 667MHz fCK for 1333Mb/sec/pin, 800MHz fCK for 1600Mb/sec/pin 900MHz fCK for 1866Mb/sec/pin
• 8 Banks
• Programmable CAS Latency (posted CAS): 5, 6, 7, 8, 9, 10, 11, 13
• Programmable Additive Latency: 0, CL-2 or CL-1 clock
• Programmable CAS Write Latency (CWL) = 5 (DDR3-800), 6 (DDR3-1066), 7 (DDR3-1333), 8 (DDR3-1600) and 9 (DDR3-1866)
• 8-bit pre-fetch
• Burst Length: 8 (Interleave without any limit, sequential with starting address “000” only), 4 with tCCD = 4 which does not allow seamless read or write [either On the fly using A12 or MRS]
• Bi-directional Differential Data-Strobe
• Internal (self) calibration: Internal self calibration through ZQ pin (RZQ : 240 ohm ± 1%)
• On Die Termination using ODT pin
• Average Refresh Period 7.8us at lower than TCASE 85°C, 3.9us at 85°C < TCASE < 95 °C
• Asynchronous Reset
• Package: 78 balls FBGA - x4/x8
• All of Lead-Free products are compliant for RoHS
• All of products are Halogen-free

<table>
<thead>
<tr>
<th>Speed</th>
<th>DDR3-800</th>
<th>DDR3-1066</th>
<th>DDR3-1333</th>
<th>DDR3-1600</th>
<th>DDR3-1866</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>tCK(min)</td>
<td>2.5</td>
<td>1.875</td>
<td>1.5</td>
<td>1.25</td>
<td>1.07</td>
<td>ns</td>
</tr>
<tr>
<td>CAS Latency</td>
<td>6</td>
<td>7</td>
<td>9</td>
<td>11</td>
<td>13</td>
<td>nCK</td>
</tr>
<tr>
<td>tRCD(min)</td>
<td>15</td>
<td>13.125</td>
<td>13.5</td>
<td>13.75</td>
<td>13.91</td>
<td>ns</td>
</tr>
<tr>
<td>tRP(min)</td>
<td>15</td>
<td>13.125</td>
<td>13.5</td>
<td>13.75</td>
<td>13.91</td>
<td>ns</td>
</tr>
<tr>
<td>tRAS(min)</td>
<td>37.5</td>
<td>37.5</td>
<td>38</td>
<td>39</td>
<td>34</td>
<td>ns</td>
</tr>
<tr>
<td>tRC(min)</td>
<td>52.5</td>
<td>50.025</td>
<td>48.5</td>
<td>48.75</td>
<td>47.91</td>
<td>ns</td>
</tr>
</tbody>
</table>

Table 12: 1Gb DDR3 G-die Speed bins

b) Description

The 1Gb DDR3 SDRAM G-die is organized as a 32Mbit x 4 I/Os x 8banks, 16Mbit x 8 I/Os x 8banks device. This synchronous device achieves high speed double-data-rate transfer rates of up to 1866Mb/sec/pin (DDR3-1866) for general applications.

The chip is designed to comply with the following key DDR3 SDRAM features such as posted CAS, Programmable CWL, Internal (Self) Calibration, On Die Termination using ODT pin and Asynchronous Reset.

All of the control and address inputs are synchronized with a pair of externally supplied differential clocks. Inputs are latched at the crosspoint of differential clocks (CK rising and
CK falling). All I/Os are synchronized with a pair of bidirectional strobes (DQS and DQS) in a source synchronous fashion. The address bus is used to convey row, column, and bank address information in a RAS/CAS multiplexing style. The DDR3 device operates with a single 1.5V ± 0.075V power supply and 1.5V ± 0.075V VDDQ. The 1Gb DDR3 G-die device is available in 78ball FBGAs(x4/x8).

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Rating</th>
<th>Units</th>
<th>NOTE</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD</td>
<td>Voltage on VDD pin relative to VSS</td>
<td>-0.4 V – 1.975 V</td>
<td>V</td>
<td>1.3</td>
</tr>
<tr>
<td>VDDQ</td>
<td>Voltage on VDDQ pin relative to VSS</td>
<td>-0.4 V – 1.975 V</td>
<td>V</td>
<td>1.3</td>
</tr>
<tr>
<td>VIN, VOUT</td>
<td>Voltage on any pin relative to VSS</td>
<td>-0.4 V – 1.975 V</td>
<td>V</td>
<td>1</td>
</tr>
<tr>
<td>TSTO</td>
<td>Storage Temperature</td>
<td>-65 to +100</td>
<td>°C</td>
<td>1, 2</td>
</tr>
</tbody>
</table>

Table 13: Absolute Maximum DC Ratings

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Rating</th>
<th>Units</th>
<th>NOTE</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD</td>
<td>Supply Voltage</td>
<td>1.425</td>
<td>V</td>
<td>1.2</td>
</tr>
<tr>
<td>VDDQ</td>
<td>Supply Voltage for Output</td>
<td>1.425</td>
<td>V</td>
<td>1.2</td>
</tr>
</tbody>
</table>

NOTE:
1. Under all conditions $V_{DDQ}$ must be less than or equal to $V_{DD}$.
2. $V_{DDQ}$ tracks with $V_{DD}$. AC parameters are measured with $V_{DD}$ and $V_{DDQ}$ tied together.

Table 14: Recommended operating conditions

8. 2Gbit (256M x 8 bit) NAND Flash Memory

**H27U2G8F2CTR-BC**

a) **Key Features**

**DENSITY**
- 2Gbit: 2048 blocks

**NAND FLASH INTERFACE**
- NAND Interface
- ADDRESS / DATA Multiplexing

**SUPPLY VOLTAGE**
- $V_{cc} = 3.0/1.3 V$ Volt core supply voltage for Program, Erase and Read operations.

**MEMORY CELL ARRAY**
- X8: (2K + 64) bytes x 64 pages x 2048 blocks
- X16: (1k+32) words x 64 pages x 2048 blocks

**PAGE SIZE**
- X8: (2048 + 64 spare) bytes
- X16:(1024 + 32spare) Words

Block SIZE
- X8: (128K + 4K spare) bytes
- X16:(64K + 2K spare) Words

PAGE READ / PROGRAM
- Random access: 25us (Max)
- Sequential access: 25ns / 45ns (3.0V/1.8V, min.)
- Program time(3.0V/1.8V): 200us / 250us (Typ)
- Multi-page program time (2 pages):
  200us / 250us (3.0V/1.8V, Typ.)

BLOCK ERASE / MULTIPLE BLOCK ERASE
- Block erase time: 3.5 ms (Typ)
- Multi-block erase time (2 blocks):
  3.5ms / 3.5ms (3.0V/1.8V, Typ.)

SEURITY
- OTP area
- Serial number (unique ID)
- Hardware program/erase disabled during Power transition
- Multiplane Architecture:
  Array is split into two independent planes.
  Parallel operations on both planes are available, having program and erase time.
- Single and multiplane copy back program with automatic EDC (error detection code)
- Single and multiplane page re-program
- Single and multiplane cache program
- Cache read
- Multiplane block erase

Reliability
- 100,000 Program / Erase cycles (with 1bit /528Byte ECC)
- 10 Year Data retention

ONFI 1.0 COMPLIANT COMMAND SET

ELECTRONICAL SIGNATURE
- Maunufacture ID: ADh
- Device ID
- PACKAGE
  - Lead/Halogen Free
  - TSOP48 12 x 20 x 1.2 mm
  - FBGA63 9 x 11 x 1.0 mm

b) Description

H27(U_S)2G8_6F2C series is a 256Mx8bit with spare 8Mx8 bit capacity. The device is offered in 3.0/1.8 Vcc Power Supply, and with x8 and x16 I/O interface Its NAND cell provides the most cost-effective solution for the solid state mass storage market. The memory is divided into blocks that can be erased independently so it is possible to preserve valid data while old data is erased.

The device contains 2048 blocks, composed by 64 pages. Memory array is split into 2 planes, each of them consisting of 1024 blocks. Like all other 2KB - page NAND Flash devices, a program operation allows to write the 2112-byte page in typical 200us(3.3V) and an erase operation can be performed in typical 3.5ms on a 128K-byte block.

In addition to this, thanks to multi-plane architecture, it is possible to program 2 pages at a time (one per each plane) or to erase 2 blocks at a time (again, one per each plane). As a consequence, multi-plane architecture allows program time to be reduced by 40% and erase time to be reduction by 50%. In case of multi-plane operation, there is small degradation at 1.8V application in terms of program/erase time.

The multiplane operations are supported both with traditional and ONFI 1.0 protocols. Data in the page can be read out at 25ns (3V version) and 45ns (1.8V version) cycle time per byte. The I/O pins serve as the ports for address and data input/output as well as command input. This interface allows a reduced pin count and easy migration towards different densities, without any rearrangement of footprint. Commands, Data and Addresses are synchronously introduced using CE#, WE#, ALE and CLE input pin. The on-chip Program/Erase Controller automates all read, program and erase functions including pulse repetition, where required, and internal verification and margining of data.

A WP# pin is available to provide hardware protection against program and erase operations.

The output pin RB# (open drain buffer) signals the status of the device during each operation. In a system with multiple memories the RB# pins can be connected all together to provide a global status signal. Each block can be programmed and erased up to 100,000 cycles with ECC (error correction code) on. To extend the lifetime of Nand Flash devices, the
implementation of an ECC is mandatory. The chip supports CE# don't care function. This function allows the direct download of the code from the NAND Flash memory device by a microcontroller, since the CE# transitions do not stop the read operation. In addition, device supports ONFI 1.0 specification.

The copy back function allows the optimization of defective blocks management: when a page program operation fails the data can be directly programmed in another page inside the same array section without the time consuming serial data insertion phase. Copy back operation automatically executes embedded error detection operation: 1 bit error out of every 528-byte (x8) or 1 bit error out of every 264-word (x16) can be detected. With this feature it is no longer necessary to use an external to detect copy back operation errors. Multiplane copy back is also supported, both with traditional and ONFI 1.0 protocols. Data read out after copy back read (both for single and multiplane cases) is allowed. In addition, Cache program and multi cache program operations improve the programing throughput by programming data using the cache register.

The devices provide two innovative features: page re-program and multiplane page re-program. The page re-program allows to re-program one page. Normally, this operation is performed after a previously failed page program operation. Similarly, the multiplane page re-program allows to re-program two pages in parallel, one per each plane. The first page must be in the first plane while the second page must be in the second plane; the multiplane page re-program operation is performed after a previously failed multiplane page program operation. The page re-program and multiplane page re-program guarantee improve performance, since data insertion can be omitted during re-program operations, and save ram buffer at the host in the case of program failure. The devices, available in the TSOP48 (12X20mm) package, support the ONFI1.0 specification and come with four security features:

- OTP (one time programmable) area, which is a restricted access area where sensitive data/code can be stored permanently.
- Serial number (unique identifier), which allows the devices to be uniquely indentified.
- Read ID2 extension

These security features are subject to an NDA (non-disclosure agreement) and are, therefore, no described in the datasheet. For more details about them, contact your nearest Hynix sales office.
Table 15: DC and operating characteristic

9. 16M-BIT [16M x 1] CMOS SERIAL FLASH EEPROM

**MX25L1602 Mstar SPI Flash**

_a) Key Features_

- **HIGH DENSITY NAND FLASH MEMORIES**
  
  **GENERAL**
  
  - 16,777,216 x 1 bit structure
  - 256 Equal Sectors with 8K-byte each
    - Any sector can be erased
  - 4096 Equal Segments with 512-byte each
    - Provides sequential output within any segment
  - Single Power Supply Operation
    - 3.0 to 3.6 volt for read, erase, and program operations
  - Latch-up protected to 100mA from -1V to Vcc +1V
  - Low Vcc write inhibit is equal to or less than 2.5V
PERFORMANCE

• High Performance
  - Fast access time: 20MHz serial clock (50pF + 1TTL Load)
  - Fast program time: 5ms/page (typical, 128-byte per page)
  - Fast erase time: 300ms/sector (typical, 8K-byte per sector)

• Low Power Consumption
  - Low active read current: 10mA (typical) at 17MHz
  - Low active programming current: 10mA (typical)
  - Low active erase current: 10mA (typical)
  - Low standby current: 30uA (typical, CMOS)

• Minimum 100,000 erase/program cycle

SOFTWARE FEATURES

• Input Data Format
  - 1-byte Command code, 3-byte address, 1-byte byte address

• 512-byte Sequential Read Operation
• Built in 9-bit (A0 to A8) pre-settable address counter to support the 512-byte sequential read operation

• Auto Erase and Auto Program Algorithm
  - Automatically erases and verifies data at selected sector
  - Automatically programs and verifies data at selected page by an internal algorithm that automatically times the program pulse widths (Any page to be programmed should have page in the erased state first)

• Status Register Feature
  - Provides detection of program and erase operation completion.
  - Provides auto erase/program error report

HARDWARE FEATURES

• SCLK Input
  - Serial clock input

• SI Input
  - Serial Data Input

• SO Output
  - Serial Data Output
b) General Description

The MX25L1602 is a CMOS 16,777,216 bit serial Flash EEPROM, which is configured as 2,097,152 x 8 internally. The MX25L1602 features a serial peripheral interface and software protocol allowing operation on a simple 3-wire bus. The three bus signals are a clock input (SCLK), a serial data input (SI), and a serial data output (SO). SPI access to the device is enabled by CS input.

The MX25L1602 provide sequential read operation on whole chip. The sequential read operation is executed on a segment (512 byte) basis. User may start to read from any byte of the segment. While the end of the segment is reached, the device will wrap around to the beginning of the segment and continuously outputs data until CS goes high.

After program/erase command is issued, auto program/erase algorithms which program/erase and verify the specified page locations will be executed. Program command is executed on a page (128 bytes) basis, and erase command is executed on both chip and sector (8K bytes) basis.

To provide user with ease of interface, a status register is included to indicate the status of the chip. The status read command can be issued to detect completion and error flag status of a program or erase operation.

When the device is not in operation and CS is high, it is put in standby mode and draws less than 30μA DC current.

The MX25L1602 utilizes MXIC's proprietary memory cell which reliably stores memory contents even after 100,000 program and erase cycles.
10. USB Interface

Mstar IC has two input port for USB, therefore air mouse, internal wi-fi interface and USB2 are combined with HUB. This property is optional. If air mouse and wi-fi interfaces are not aligned, two USB are connected directly to main IC.
**USB2512B**

a) General Description
The SMSC USB251xB/xBi hub is a family of low-power, configurable, MTT (multi transaction translator) hub controller IC products for embedded USB solutions. The $x$ in the part number indicates the number of downstream ports available, while the $B$ indicates battery charging support. The SMSC hub supports low-speed, full-speed, and hi-speed (if operating as a hi-speed hub) downstream devices on all of the enabled downstream ports.

b) Features
- USB251xB/xBi products are fully footprint compatible with USB251x/xi/xA/xAi products as direct drop-in replacements
  - Cost savings include using the same PCB components and application of USB-IF Compliance by Similarity
- Full power management with individual or ganged power control of each downstream port
- Fully integrated USB termination and pull-up/pulldown resistors
- Supports a single external 3.3 V supply source; internal regulators provide 1.2 V internal core voltage
- Onboard 24 MHz crystal driver, ceramic resonator, or external 24/48 MHz clock input
- Customizable vendor ID, product ID, and device ID
- 4 kilovolts of HBM JESD22-A114F ESD protection (powered and unpowered)
- Supports self- or bus-powered operation
- Supports the USB Battery Charging specification Rev. 1.1 for Charging Downstream Ports (CDP)
- 36-pin QFN (6x6 mm) Lead-free RoHS compliant package
- USB251xBi products support the industrial temperature range of -40°C to +85°C
- USB251xB products support the extended commercial temperature range of 0°C to +85°C

c) Applications
- LCD monitors and TVs
- Multi-function USB peripherals
- PC motherboards
- Set-top boxes, DVD players, DVR/PVR
- Printers and scanners
- PC media drive bay
- Portable hub boxes
- Mobile PC docking
- Embedded systems

Figure 11: Pin configurations
11. CI Interface

17MB95 Digital CI ve Smart Card Interface Block diagram:

![Block Diagram](image)

Figure 12: CI interface

12. Demodulator Stage

A. MSB1231 DVB-T2

a) Key Features

- Integrated DVB-T/T2 Receiver
  - Compliant with DVB-T (ETSI EN 300 744)
  - Compliant with DVB-T2 (ETSI EN 302 755)
  - Supports all guard intervals (1/128 to 1/4)
  - Supports all FFT modes from 1K to 32K
  - Supports all long and short block code rates (1/2, 3/5, 2/3, 3/4, 4/5, 5/6)
  - Supports all constellations (QPSK, 16-QAM, 64-QAM, 256-QAM)
  - Transmit diversity (MISO) support
  - Supports all scattered pilot patterns (PP1 to PP8)
  - Supports rotated and non-rotated constellations
  - Supports single and multiple PLPs
  - Nordic Unified, D-Book, E-Book compliant
  - Automatic co-channel and adjacent channel interference suppression
  - All digital demodulation and timing recovery loops for tracking frequency and clock offset

- DVB-C Demodulator
  - Compliant with DVB-C (EN300429) and ITU-T J.133 Annex A/C
  - Supports symbol rates up to 7 M Baud
  - Blind acquisition of QAM constellations
  - Single IF filter bandwidth for all symbol rates

- Miscellaneous
  - Accept IF, low IF, zero-IF inputs in 1.7, 5, 6, 7, 8MHz channel bandwidths
  - Configurable parallel/serial MPEG-2 transport stream interface
  - Fast channel acquisition and auto-scan time
  - Clock generation from a single crystal
  - On chip MCU to reduce host control overhead
  - Support single or dual AGC control loops
  - Supports I2C interface with bypass mode
  - 64-pin LQFP package
b) General Description

The MSB1231 is a single chip demodulator supporting DVB-T2, DVB-T, and DVB-C standards. The MSB1231 enables the design of ETSI EN302755 compliant receivers with performance exceeding DTG Dbook 6.1 requirements. The device integrates a house keeping microcontroller that takes care of all real time and algorithmic tasks simplifying the host control interface.

The MSB1231 front end can accept tuners that provide IF, low IF or ZIF output. A high rejection channel filter has been included easing the channel filtering requirement of the tuner whilst still meeting the stringent requirements for adjacent channel interference. The MSB1231 may be clocked directly using a crystal, typically 24MHz or may take a reference clock from another stable source such as the tuner.

The MSB1231 is capable of blind acquisition of DVB-T and T2 signals. All parameters may be detected in this mode enabling fast and accurate auto scanning. Its frequency recovery circuit is capable of compensating for all typical tuner and broadcast frequency errors.

For DVB-T, a novel impulsive interference filter has been implemented to remove impulsive interference without affecting normal operation thus reducing the effects of transient interference known to affect the quality of OFDM digital TV reception.

The development platform may be supplied as a complete system solution for STB and iDTV applications including a silicon tuner and source decoder.

c) Block Diagram
d) Pinning
c) Absolute Maximum Ratings and Recommended Operating Conditions

### Recommended Operating Power Conditions

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.3V Supply Voltages</td>
<td>V_{CC0,31}</td>
<td>3.14</td>
<td>3.3</td>
<td>3.46</td>
<td>V</td>
</tr>
<tr>
<td>2.5V Supply Voltages</td>
<td>V_{CC0,25}</td>
<td>2.38</td>
<td>2.5</td>
<td>2.62</td>
<td>V</td>
</tr>
<tr>
<td>1.2V Supply Voltages</td>
<td>V_{CC0,12}</td>
<td>1.14</td>
<td>1.2</td>
<td>1.26</td>
<td>V</td>
</tr>
</tbody>
</table>

### Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.3V Supply Voltages</td>
<td>V_{CC0,31}</td>
<td>3.6</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>2.5V Supply Voltages</td>
<td>V_{CC0,25}</td>
<td>2.75</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>1.2V Supply Voltages</td>
<td>V_{CC0,12}</td>
<td>1.32</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Input Voltage (5V tolerant inputs)</td>
<td>V_{IN}</td>
<td>5.0</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Input Voltage (non 5V tolerant inputs)</td>
<td>V_{IN}</td>
<td>V_{CCO,23}</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Ambient Operating Temperature</td>
<td>T_a</td>
<td>0</td>
<td>70</td>
<td>°C</td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>T_{STG}</td>
<td>-40</td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>Junction Temperature</td>
<td>T_{J}</td>
<td>150</td>
<td>°C</td>
<td></td>
</tr>
</tbody>
</table>

**Note:** Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and does not imply functional operation of the device. Exposure to absolute maximum ratings for extended periods may affect device reliability.
B. **M88DS3002 DVB-S/S2 Demodulator**

a) Key Features and General Description

**Features**
- **Multi-standard demodulation**
  - Compliant with DVB-S/S2 specification
  - QPSK, 8PSK, 16APSK and 32APSK demodulation schemes
  - Maximum channel bit rate is 130 Mbps
  - Maximum symbol rate are: 45 Mps for QPSK and 6PSK, 36 Mps for 16APSK and 26 Mps for 32APSK
- **DSP features**
  - Symbol rate sweeping
  - IQ impairment cancellation
  - Automatic spectrum inversion
  - Adaptive equalizer for RF reflection removal
  - Roll-off factor automatic identification
  - Blind scan for programming search
  - High performance on-chip micro-controller
  - Multi-error monitor
  - Accurate SNR estimation
  - Multi-lock indicators
  - Clipping rate reporter
  - DC removal
  - Automatic frequency correction (AFC)
  - Fast timing loop acquisition
  - Robust frame synchronization scheme
  - Phase noise indicator
  - Fast system recovery from fading or other abnormal conditions
  - Co-channel interference cancellation
  - Constellation monitor
- **Interface**
  - DVB-S/S2 common, parallel and serial MPEG output interface compliant
  - 2-wire serial bus to configure the device
  - 2-wire bus repeater for tuner configuration
  - DiSEqC™ 2.X compliant interface
  - General purpose output (GPO)
  - Dedicated reference clocks (13.5MHz/27MHz) generation
- **System**
  - On-chip 8-bit ADC
  - On-chip PLL for master clock from a 27 MHz external clock or quartz crystal
  - Sleep mode supported

**Applications**
- Digital satellite set-top boxes
- Digital satellite receivers

**General Description**
The M88DS3002 is an advanced single-chip demodulator for digital satellite television broadcasting. It is fully compliant with the DVB-S/S2 standard and can support QPSK, 8PSK, 16APSK and 32APSK demodulation schemes. The chip provides a fast, easy-to-apply and cost-effective front-end solution for digital satellite receiver.

The M88DS3002 accepts baseband differential or single-ended I and Q signals from a tuner, then digitizes, demodulates and decodes the signals, and finally outputs an MPEG transport stream.

The M88DS3002 supports symbol rate from 1 Mps up to 45 Mps, and code rate from 1/4 to 9/10. Its features cover blind scan, fade detection, timing and carrier recovery, performance monitoring, co-channel interference cancellation, command interface, and DiSEqC™ 2X interface, etc. The device is controlled via a 2-wire serial bus.

The M88DS3002 works properly with 1.25 V and 3.3 V voltage supplies. Typically, the power consumption is around 390 mW. The chip is available in a 64-pin QFN package and is RoHS compliant.
b) Block Diagram

![Block Diagram](image1)

M88DS3002

Carrier Recovery, SNR Estimation & Soft-decision

DVB-S Mode FEC

DVB-S2 Mode FEC

Error Monitor & Output Formatter

Micro-controller

Power & Supply

c) Pin Information

![Pin Information](image2)

M88DS3002 QFN 64-Pin

Ground – An exposed pad at the bottom of the package.
a) Absolute Maximum Ratings and Recommended Operating Conditions

**Absolute Maximum Ratings**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DDA}, V_{DDD}$</td>
<td>3.3 V Power Supply for the Analog Part and the I/O Pad</td>
<td>-0.3</td>
<td>3.8</td>
<td>V</td>
</tr>
<tr>
<td>$V_{CC}$</td>
<td>1.25 V Power Supply for the Digital Core</td>
<td>-0.2</td>
<td>1.44</td>
<td>V</td>
</tr>
<tr>
<td>$V_{SVT}$</td>
<td>Voltage on 5V Tolerant Pins</td>
<td>-0.5</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>$V_{IN}$</td>
<td>Voltage on Input Pins</td>
<td>-0.3</td>
<td>$V_{DDD} + 0.3$</td>
<td>V</td>
</tr>
<tr>
<td>$T_{STG}$</td>
<td>Storage Temperature</td>
<td>-40</td>
<td>+150</td>
<td>°C</td>
</tr>
</tbody>
</table>

Note: Stresses above the Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended period may affect device reliability.

**Recommended Operating Conditions**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DDA}, V_{DDD}$</td>
<td>3.3 V Power Supply for the Analog Part and the I/O Pad</td>
<td>2.97</td>
<td>3.3</td>
<td>3.63</td>
<td>V</td>
</tr>
<tr>
<td>$V_{CC}$</td>
<td>1.25 V Power Supply for the Digital Core</td>
<td>1.2</td>
<td>1.25</td>
<td>1.375</td>
<td>V</td>
</tr>
<tr>
<td>$T_{A}$</td>
<td>Operating Ambient Temperature</td>
<td>0</td>
<td>-</td>
<td>70</td>
<td>°C</td>
</tr>
</tbody>
</table>

Note: Device functionality is not guaranteed at any conditions beyond the recommended operating conditions.

13. **LNB supply and control IC**

**MP8125**

a) **General Description**

The MP8125 is a voltage regulator designed to provide efficient, low noise power to the Satellite receiver’s RF LNB (Low Noise Block) converter via coaxial cable through a DiSEqC 1.x compatible link that receives instructions from a dedicated controller.

The MP8125 integrates a current mode boost regulator followed by a tracking linear regulator. The boost regulator provides a clean and quiet power source that will not contaminate the low noise RF signal down converted to the receiver. The tracking linear regulator protects the output against overload or short.

The MP8125 provides a number of features described in the European EUTELSAT specification (DiSEqC) including: voltage selection of horizontal or vertical polarization directions of LNB and a selectable VOUT compensation for voltage drop on the long coaxial cable. In accordance with DiSEqC standard, a tone signal of 22kHz is generated by an internal oscillator and can be activated or deactivated onto output by EXTM pin.

The MP8125 is available in thermally enhanced TSSOP16 package.
b) Key Features
• DiSEqC 1.x Compatibility
• Up to 550mA Output Current
• 8V to 14V Input Voltage
• Boost Converter with Internal Switch
• Low Noise LDO Output
• Built-in 22kHz Tone Signal Generator
• Programmable Current Limit
• 1V Line Drop Compensation
• Adjustable Soft-start Time
• POK Indicator
• Short Circuit Protection
• Over Temperature Protection
• TSSOP16 Exposed Pad Package

APPLICATIONS
• LNB Power Supply and Control for Satellite Set Top Boxes

c) Package Reference
a) Absolute Maximum Ratings and Recommended Operating Conditions

**Absolute Maximum Ratings**

- **VDD**: −0.3V to 18V
- **VOUT, SW, VBOOST**: −0.3V to 25V
- **BST**: −0.3V to 7V
- **All Other Pins**: −0.3V to 6.5V
- **Continuous Power Dissipation (T2=25°C)**: 2.8W
- **TSSOP-16**: 2.8W
- **Junction Temperature**: 150°C
- **Lead Temperature**: 260°C
- **Storage Temperature**: −65°C to 150°C

**Recommended Operating Conditions**

- **Supply Voltage V_IN**: 8V to 14V
- **Output Voltage V_OUT**: 13V/14V/18V/19V
- **Operating Junct. Temp (Tj)**: −20°C to +125°C

14. Software Update

14.1 Main SW update

In MB95 project there is only one software. From following steps software update procedure can be seen:

1. MB90_en.bin, mboot.bin and usb_auto_update_A1.txt documents should copy directly inside of a flash memory(not in a folder).
2. Insert flash memory to the tv when tv is powered off.
3. While pushing the OK button in remote control, power on the and wait. TV will power-up itself.
4. If First Time Installation screen comes, it means software update procedure is successful.

15. Troubleshooting

A. No Backlight Problem

**Problem**: If TV is working, led is normal and there is no picture and backlight on the panel.

**Possible causes**: Backlight pin, dimming pin, backlight supply, stby on/off pin

BACKLIGHT_ON/OFF pin should be high when the backlight is ON. R119 must be low when the backlight is OFF. If it is a problem, please check Q10 and the panel cables. Also it can be tested in TP50 in main board.
Dimming pin should be high or square wave in open position. If it is low, please check S60 for Mstar side and panel or power cables, connectors.

Backlight power supply should be in panel specs. Please check Q33, shown below; also it can be checked TP53.
STBY_ON/OFF_NOT should be low for TV on condition, please check Q11’s collector.

B. CI Module Problem

**Problem:** CI is not working when CI module inserted.

**Possible causes:** Supply, supply control pin, detect pins, mechanical positions of pins.

- CI supply should be 5V when CI module inserted. If it is not 5V please check CI_PWR_CTRL, this pin should be low.
- Please check mechanical position of CI module. Is it inserted properly or not?
- Detect ports should be low. If it is not low please check CI connector pins, CI module pins.
C. Staying in Stand-by Mode

**Problem:** Staying in stand-by mode, no other operation

This problem indicates a short on Vcc voltages. Protect pin should be logic high while normal operation. When there is a short circuit protect pin will be logic low. If you detect logic low on protect pin, unplug the TV set and control voltage points with a multimeter to find the shorted voltage to ground.
D. IR Problem

Problem: LED or IR not working
Check LED card supply on MB95 chassis.

E. Keypad Touchpad Problems

Problem: Keypad or Touchpad is not working
Check keypad supply on MB95.
F. USB Problems

**Problem:** USB is not working or no USB Detection.

Check USB Supply, It should be nearly 5V. Also USB Enable should be logic high.
G. No Sound Problem

**Problem:** No audio at main TV speaker outputs.
Check supply voltages of 24V VDD_AUDIO, 3.3V AUDIO_AVDD and AUDIO_DVDD with a voltage-meter. There may be a problem in headphone connector or headphone detect circuit (when headphone is connected, speakers are automatically muted). Measure voltage at HP_DETECT pin, it should be 3.3v.

H. Standby On/Off Problem

**Problem:** Device can not boot, TV hangs in standby mode.
There may be a problem about power supply. Check main supplies with a voltage-meter. Also there may be a problem about SW. Try to update TV with latest SW. Additionally it is good to check SW printouts via Teraterm. These printouts may give a clue about the problem. You can use Scart-1 for terraterm connection.
I. No Signal Problem

**Problem:** No signal in TV mode.

Check tuner supply voltage; 5V_VCC, 3V3_TUNER and 1V8_TUNER. Check tuner options are correctly set in Service menu. Check AGC voltage at IF_AG pin of tuner.

16. Service Menu Settings

In order to reach service menu, first Press “MENU” button, then write “4725” by using remote controller.

You can see the service menu main screen below. You can check SW releases by using this menu. In addition, you can make changes on video, audio etc. by using video settings, audio settings titles.
Service Menu Main Screen

Video Settings
Audio Settings

Options-1 Menu
Tuner Settings Menu

Source Settings Menu
Diagnostic Menu
17. General Block Diagram