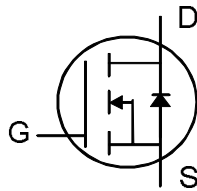


## N-CHANNEL ENHANCEMENT-MODE POWER MOSFET

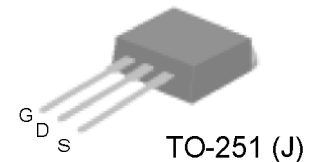
Low gate-charge  
Simple drive requirement  
Fast switching



$BV_{DSS}$  30V  
 $R_{DS(ON)}$  9m $\Omega$   
 $I_D$  60A

### Description

The SSM70T03H is in a TO-252 package, which is widely used for commercial and industrial surface-mount applications, and is well suited for low voltage applications such as DC/DC converters. The through-hole version, the SSM70T03J in TO-251, is available for low-footprint vertical mounting. These devices are manufactured with an advanced process, providing improved on-resistance and switching performance. The devices have a maximum junction temperature rating of 175°C for improved thermal margin and reliability.



### Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	30	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V
$I_D @ T_A=25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	60	A
$I_D @ T_A=100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	43	A
$I_{DM}$	Pulsed Drain Current <sup>1</sup>	195	A
$P_D @ T_A=25^\circ\text{C}$	Total Power Dissipation	53	W
	Linear Derating Factor	0.36	W/ $^\circ\text{C}$
$E_{AS}$	Single Pulse Avalanche Energy <sup>3</sup>	29	mJ
$T_{STG}$	Storage Temperature Range	-55 to 175	$^\circ\text{C}$
$T_J$	Operating Junction Temperature Range	-55 to 175	$^\circ\text{C}$

### Thermal Data

Symbol	Parameter	Value	Units
Rthj-c	Thermal Resistance Junction-case	Max. 2.8	$^\circ\text{C}/\text{W}$
Rthj-a	Thermal Resistance Junction-ambient	Max. 110	$^\circ\text{C}/\text{W}$

**Electrical Characteristics@T<sub>j</sub>=25°C(unless otherwise specified)**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	30	-	-	V
$\Delta BV_{DSS}/\Delta T_j$	Breakdown Voltage Temperature Coefficient	Reference to 25°C, $I_D=1mA$	-	0.032	-	V/°C
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS}=10V, I_D=33A$	-	-	9	mΩ
		$V_{GS}=4.5V, I_D=20A$	-	-	18	mΩ
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	1	-	3	V
$g_{fs}$		$V_{DS}=10V, I_D=33A$	-	35	-	S
$I_{DSS}$	Drain-Source Leakage Current (T <sub>j</sub> =25°C)	$V_{DS}=30V, V_{GS}=0V$	-	-	1	μA
	Drain-Source Leakage Current (T <sub>j</sub> =175°C)	$V_{DS}=24V, V_{GS}=0V$	-	-	250	μA
$I_{GSS}$	Gate-Source Leakage	$V_{GS}= \pm 20V$	-	-	±100	nA
$Q_g$	Total Gate Charge <sup>2</sup>	$I_D=33A$	-	16.5	-	nC
$Q_{gs}$	Gate-Source Charge	$V_{DS}=20V$	-	5	-	nC
$Q_{gd}$	Gate-Drain ("Miller") Charge	$V_{GS}=4.5V$	-	10.3	-	nC
$t_{d(on)}$	Turn-on Delay Time <sup>2</sup>	$V_{DS}=15V$	-	8.2	-	ns
$t_r$	Rise Time	$I_D=33A$	-	105	-	ns
$t_{d(off)}$	Turn-off Delay Time	$R_G=3.3\Omega, V_{GS}=10V$	-	21.4	-	ns
$t_f$	Fall Time	$R_D=0.45\Omega$	-	8.5	-	ns
$C_{iss}$	Input Capacitance	$V_{GS}=0V$	-	1485	-	pF
$C_{oss}$	Output Capacitance	$V_{DS}=25V$	-	245	-	pF
$C_{rss}$	Reverse Transfer Capacitance	$f=1.0MHz$	-	170	-	pF

**Source-Drain Diode**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$V_{SD}$	Forward On Voltage <sup>2</sup>	$I_S=60A, V_{GS}=0V$	-	-	1.3	V
$t_{rr}$	Reverse Recovery Time <sup>2</sup>	$I_S=30A, V_{GS}=0V,$	-	29	-	ns
$Q_{rr}$	Reverse Recovery Charge	$dI/dt=100A/\mu s$	-	12	-	nC

**Notes:**

1. Pulse width limited by safe operating area.
2. Pulse width  $\leq 300\mu s$ , duty cycle  $\leq 2\%$ .
3.  $V_{DD}=25V, L=100\mu H, R_G=25\Omega, I_{AS}=24A$ .

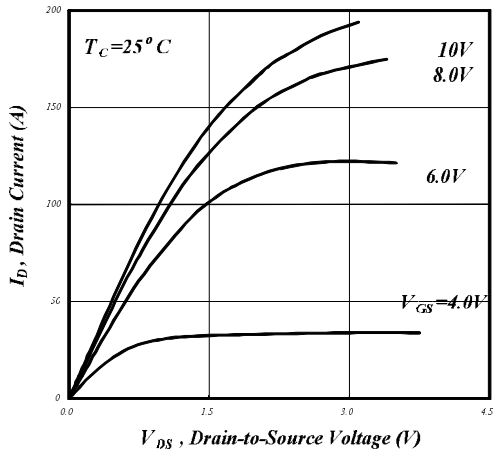


Fig 1. Typical Output Characteristics

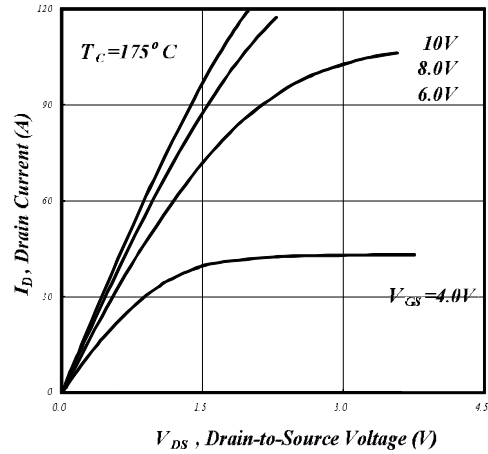


Fig 2. Typical Output Characteristics

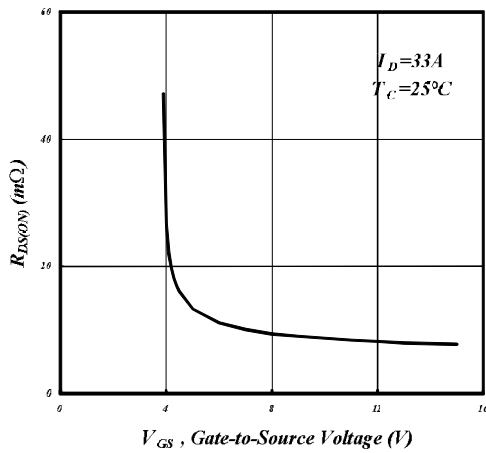


Fig 3. On-Resistance vs. Gate Voltage

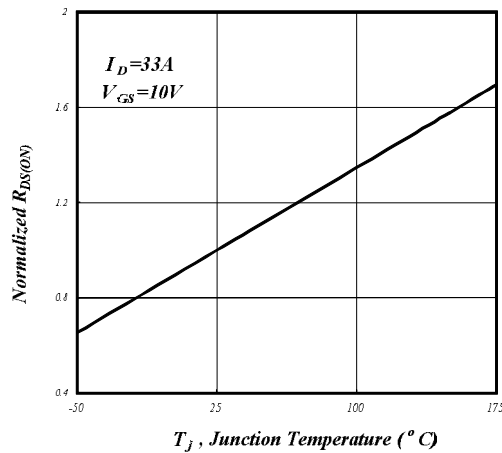


Fig 4. Normalized On-Resistance vs. Junction Temperature

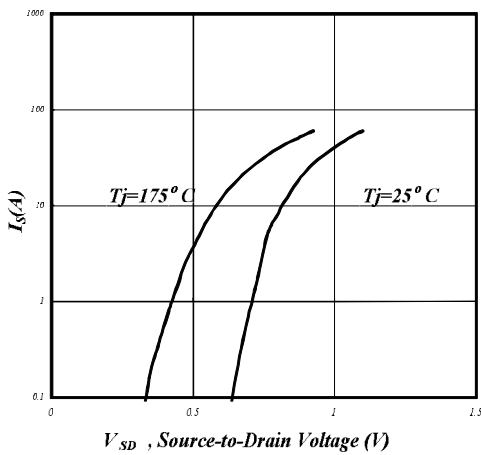


Fig 5. Forward Characteristic of Reverse Diode

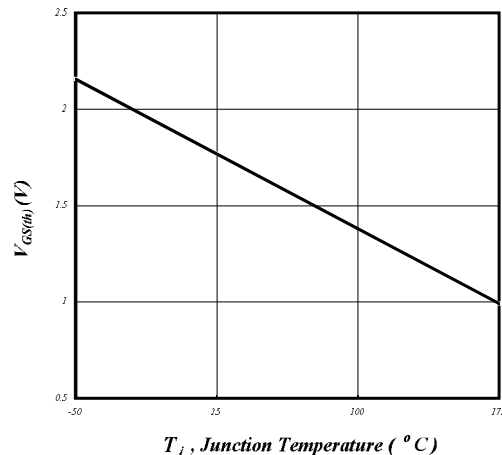


Fig 6. Gate Threshold Voltage vs. Junction Temperature

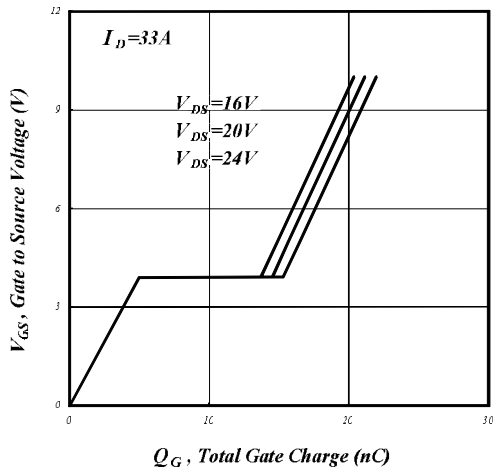


Fig 7. Gate Charge Characteristics

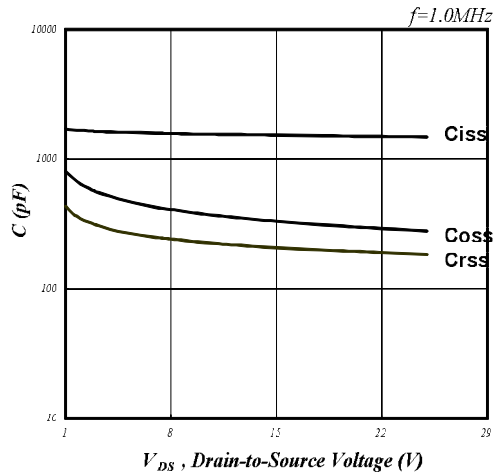


Fig 8. Typical Capacitance Characteristics

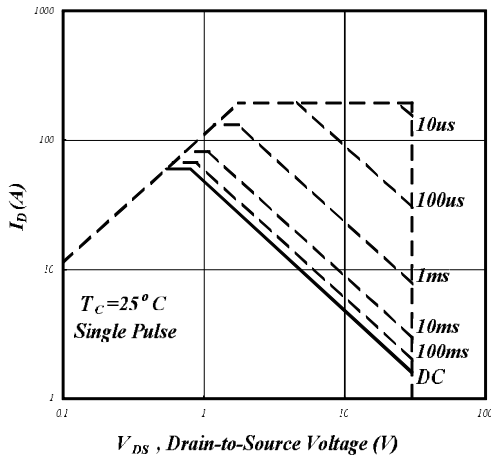


Fig 9. Maximum Safe Operating Area

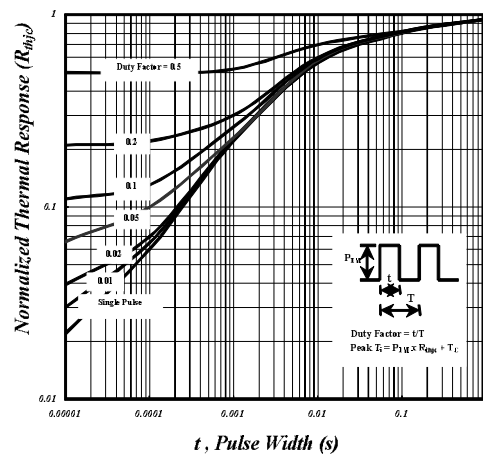


Fig 10. Effective Transient Thermal Impedance

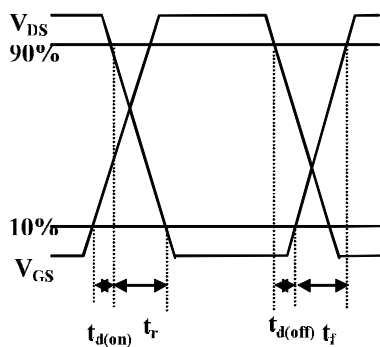


Fig 11. Switching Time Waveform

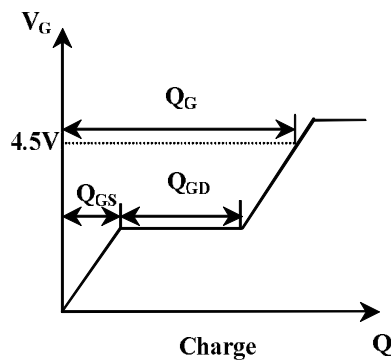


Fig 12. Gate Charge Waveform

Information furnished by Silicon Standard Corporation is believed to be accurate and reliable. However, Silicon Standard Corporation makes no guarantee or warranty, express or implied, as to the reliability, accuracy, timeliness or completeness of such information and assumes no responsibility for its use, or for infringement of any patent or other intellectual property rights of third parties that may result from its use. Silicon Standard reserves the right to make changes as it deems necessary to any products described herein for any reason, including without limitation enhancement in reliability, functionality or design. No license is granted, whether expressly or by implication, in relation to the use of any products described herein or to the use of any information provided herein, under any patent or other intellectual property rights of Silicon Standard Corporation or any third parties.