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Phison Electronics Corporation

USB 2.0 Flash Controller Specification
PS2251-33

Version 1.2

Document Number : S-09003

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Revision History

Revision	History	Date
1.0	New Release	14-Jan-2009

A. General Description

The PHISON's PS2251-33 micro-controller supports USB 2.0 & 1.1 and interface to NAND Flash Memory. This chip is specially designed for portable storage device or build-in to the PC / Notebook / IA system. It is pin-to-pin compatible to previous controllers. (eg : PS2136 & PS2231 & PS2232…..etc)

PS2251-33 controller implements with PRAM (program RAM) architecture, which can upgrade firmware code anytime if required. This is very helpful for time-to-market & Mass Production solution.

By using this single chip solution, it will reduce a lot of efforts which was needed from R/D to production, as well as simplifying the RMA problems. With the USB plug & play function and driver-less solution with most of the operating systems, this solution provides not only easy to install, but also fast, easy to use and low cost way for user.

B. Controller Features

- **Support Host Interfaces :** USB 2.0 & 1.1 Interface
  - Fully compatible with USB Specification Version 2.0 & 1.1
  - High speed 480Mbit/second supporting
  - Full speed 12Mbit/second supporting
  - Support one CONTROL transfer, one INTERRUPT transfer and two BULK transfer
  - Support four Endpoints :
    - Endpoint 0 : 64 Bytes CONTROL transfer
    - Endpoint 1 : 512 Bytes BULK transfer for IN transaction
    - Endpoint 2 : 512 Bytes BULK transfer for OUT transaction
    - Endpoint 3 : 64 Bytes INTERRUPT transfer for IN transaction
  - Support Data Payload
    - Endpoint 0 : max 64 bytes
    - Endpoint 1 : max 512 bytes
    - Endpoint 2 : max 512 bytes
    - Endpoint 3 : max 64 bytes
  - Support USB power saving mode

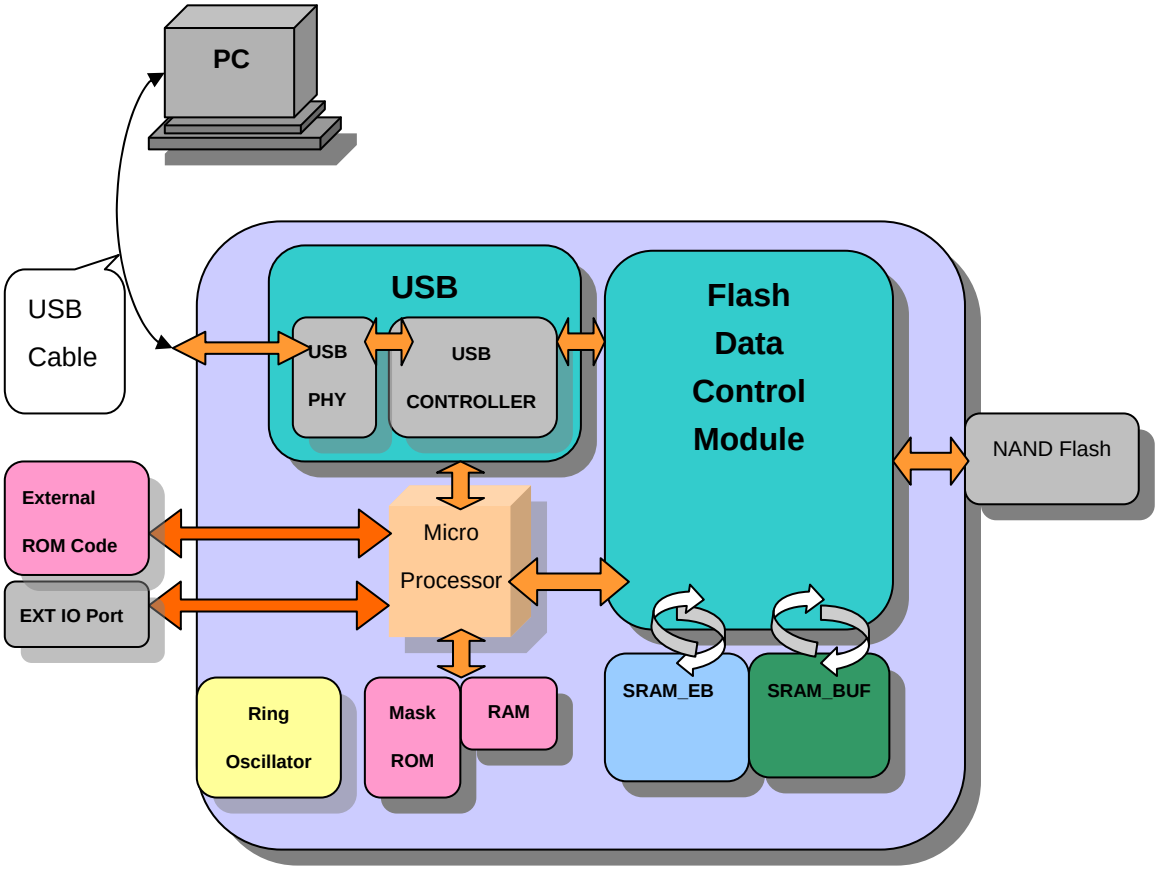
- **Build-In NAND Flash Memory Interface**
  - Build-in hardware ECC circuit.
  - Support SLC (Single level cell) 2k-page large block NAND Flash.
  - Support SLC (Single level cell) 4k-page large block NAND Flash.
  - Support MLC (Multi level cell) 2k-page Large Block NAND flash.
  - Support MLC (Multi level cell) 4k-page Large Block NAND flash.
  - Support MLC (Multi level cell) 8k-page Large Block NAND flash.

- **Support 3.3V Flash I/O:**
  Internal 3.3V regulator can supply current for controller analog circuit, controller I/O and Flash.

- **Support 1.8V Flash I/O:**
  Internal 1.8V regulator can supply the current for controller core, controller I/O and Flash.

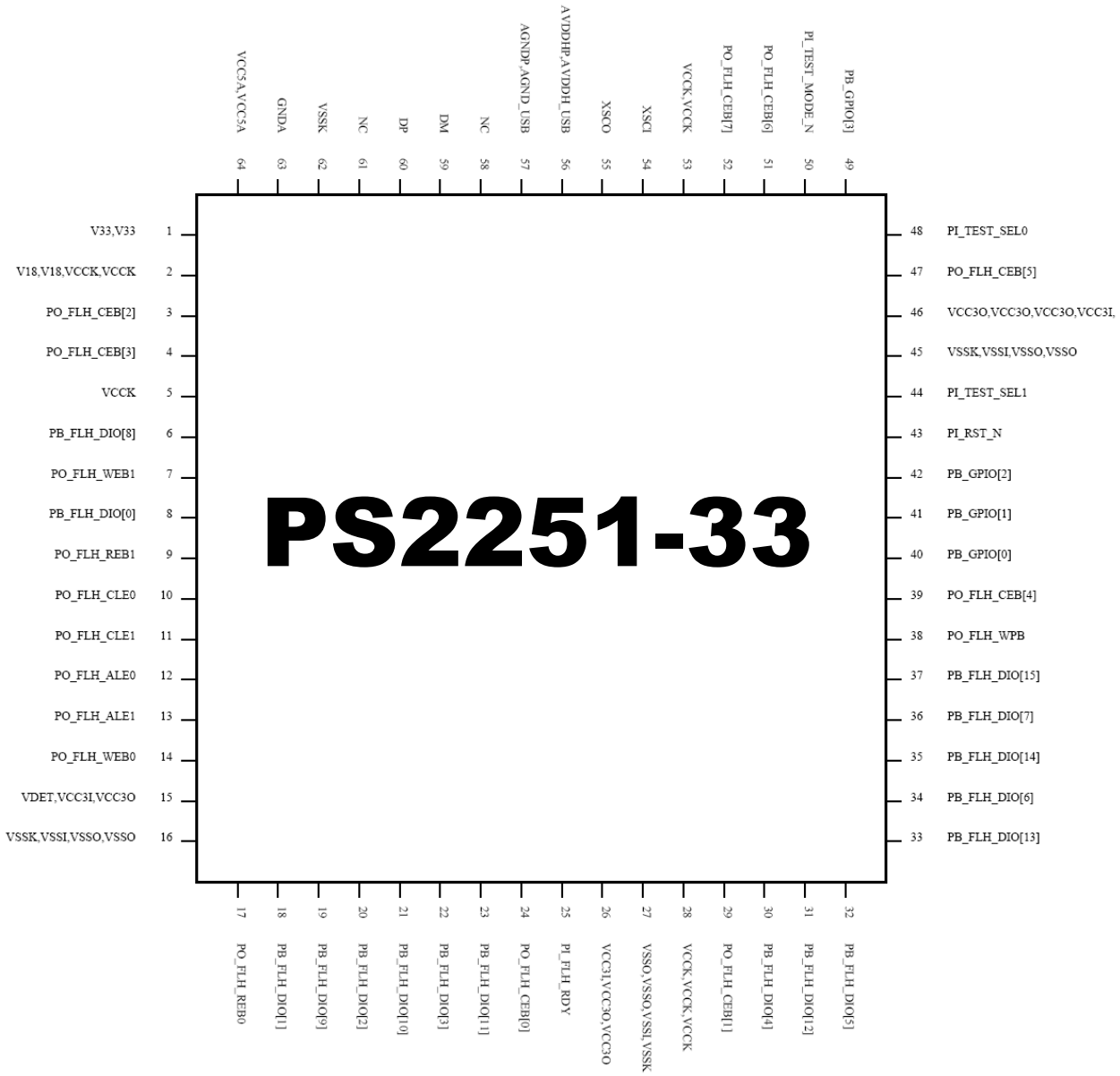
- **Support In-System Programming through USB Port**
- **Buffer SRAM :** 16 buffers for performance improvement
- **Build-in regulator**
- **48-pins / 64-pins QFP Package**
- **Operating Voltage:** 4.5V ~ 5.5V.
- **USB bus-powered capability.**
- **Power Saving implemented.**
- **Working Frequency: 12MHz.**

C. BLOCK DIAGRAM



D. Pin Assignment and Description

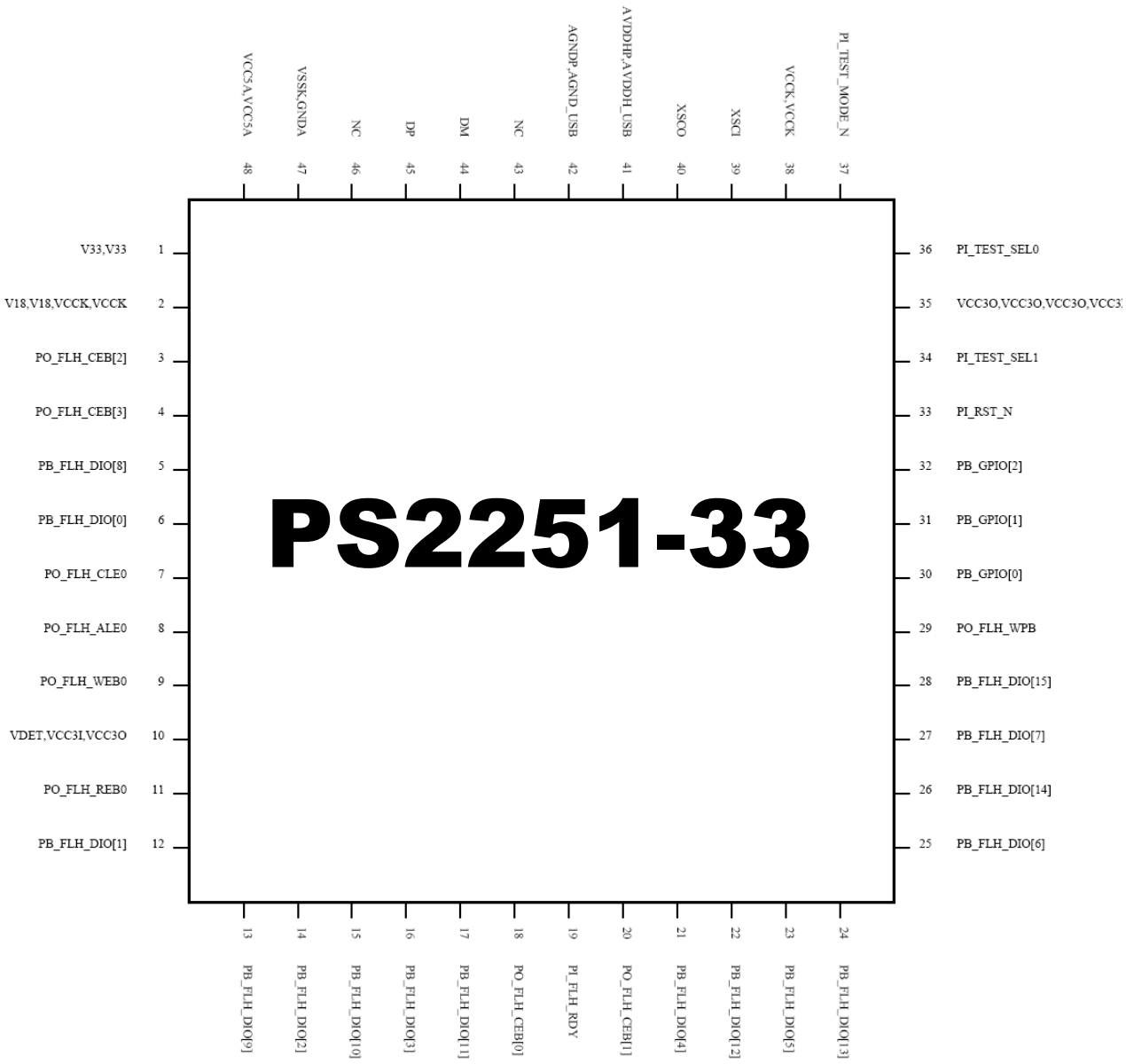
D1. Pin Assignment - 64pins



D2. Pins Listed in Numeric Order – 64pins

Pin	Signal	Pin	Signal	Pin	Signal
1	V33	23	PB_FLH_DIO[11]	45	VSSK,VSSIO
2	V18,VCCK	24	PO_FLH_CEB[0]	46	VCC3IO
3	PO_FLH_CEB[2]	25	PI_FLH_RDY	47	PO_FLH_CEB[5]
4	PO_FLH_CEB[3]	26	VCC3IO	48	PI_TEST_SEL0
5	VCCK	27	VSSIO,VSSK	49	PB_GPIO[3]
6	PB_FLH_DIO[8]	28	VCCK	50	PI_TEST_MODE_N
7	PO_FLH_WEB1	29	PO_FLH_CEB[1]	51	PO_FLH_CEB[6]
8	PB_FLH_DIO[0]	30	PB_FLH_DIO[4]	52	PO_FLH_CEB[7]
9	PO_FLH_REB1	31	PB_FLH_DIO[12]	53	VCCK
10	PO_FLH_CLE0	32	PB_FLH_DIO[5]	54	XSCI
11	PO_FLH_CLE1	33	PB_FLH_DIO[13]	55	XSCO
12	PO_FLH_ALE0	34	PB_FLH_DIO[6]	56	AVDDHP,AVDDH_USB
13	PO_FLH_ALE1	35	PB_FLH_DIO[14]	57	AGNDP,AGND_USB
14	PO_FLH_WEB0	36	PB_FLH_DIO[7]	58	NC
15	VDET,VCC3IO	37	PB_FLH_DIO[15]	59	DM
16	VSSK,VSSIO	38	PO_FLH_WPB	60	DP
17	PO_FLH_REB0	39	PO_FLH_CEB[4]	61	NC
18	PB_FLH_DIO[1]	40	PB_GPIO[0]	62	VSSK
19	PB_FLH_DIO[9]	41	PB_GPIO[1]	63	GNDA
20	PB_FLH_DIO[2]	42	PB_GPIO[2]	64	VCC5A
21	PB_FLH_DIO[10]	43	PI_RST_N		
22	PB_FLH_DIO[3]	44	PI_TEST_SEL1		

D3. Pin Assignment - 48pins



D4. Pins Listed in Numeric Order – 48pins

Pin	Signal	Pin	Signal	Pin	Signal
1	V33	17	PB_FLH_DIO[11]	33	PI_RST_N
2	V18,VCCK	18	PO_FLH_CEB[0]	34	PI_TEST_SEL1
3	PO_FLH_CEB[2]	19	PI_FLH_RDY	35	VCC3IO
4	PO_FLH_CEB[3]	20	PO_FLH_CEB[1]	36	PI_TEST_SEL0
5	PB_FLH_DIO[8]	21	PB_FLH_DIO[4]	37	PI_TEST_MODE_N
6	PB_FLH_DIO[0]	22	PB_FLH_DIO[12]	38	VCCK
7	PO_FLH_CLE0	23	PB_FLH_DIO[5]	39	XSCI
8	PO_FLH_ALE0	24	PB_FLH_DIO[13]	40	XSCO
9	PO_FLH_WEB0	25	PB_FLH_DIO[6]	41	AVDDHP,AVDDH_USB
10	VDET,VCC3IO	26	PB_FLH_DIO[14]	42	AGNDP,AGND_USB
11	PO_FLH_REB0	27	PB_FLH_DIO[7]	43	NC
12	PB_FLH_DIO[1]	28	PB_FLH_DIO[15]	44	DM
13	PB_FLH_DIO[9]	29	PO_FLH_WPB	45	DP
14	PB_FLH_DIO[2]	30	PB_GPIO[0]	46	NC
15	PB_FLH_DIO[10]	31	PB_GPIO[1]	47	VSSK,GNDA
16	PB_FLH_DIO[3]	32	PB_GPIO[2]	48	VCC5A

D5. Pin Description

USB + Regulator Interface		
Pin Name	**Dir.**	**Pin Description**
V18	VCC18	1.8V regulator power supply
V33	VCC33	3.3V regulator power supply
VCC5A	VCC5	5.0V regulator power input
GNDA	GND	0V regulator ground reference input
DP	I/O	USB 2.0 data in positive pin terminal.
DM	I/O	USB 2.0 data in negative pin terminal.
AVDDHP,AVDDH_USB	VCC33	USB 2.0 PHY power (3.3V)
AGNDP,AGND_USB	GND	USB 2.0 PHY ground reference (0V)
VSSK	VCC33	USB 2.0 PLL ground (0V)
XSCO	O	Crystal oscillator output
XSCI	I	Crystal oscillator input
VCCK	I	USB 2.0 core power (1.8V)
NC		No Connection

FLASH Interface		
Pin Name	**Dir.**	**Pin Description**
PO_FLH_CEB [7:0]	O	Flash chip enable, low active.
PB_FLH_DIO [15:0]	I/O	Flash data bus
PO_FLH_ALE0, PO_FLH_ALE1	O	Flash address latch enable, high active.
PO_FLH_CLE0, PO_FLH_CLE1	O	Flash command latch enable, high active.
PO_FLH_REB0, PO_FLH_REB1	O	Flash read control signal, low active.
PO_FLH_WEB0, PO_FLH_WEB1	O	Flash write control signal, low active.
PO_FLH_WPB	O	Flash write protect control signal, low active.
PI_FLH_RDY	I	Flash ready/busy signal input

Global Signal		
Pin Name	**Dir.**	**Pin Description**
PI_RST_N	I	Reset Signal
PI_TEST_SEL0	I	Test Mode Signal.
PI_TEST_SEL1	I	EAMODE Select Signal.
PI_TEST_MODE_N	I	USB VBUS input
PB_GPIO[0:3]	I/O	4-bit GPIO
VCC3IO	VCC33	3.3V IO power
VCCK	VCC18	1.8V digital core power
VSSIO	GND	0V IO ground reference
VSSK	GND	0V digital core ground reference

E. System Power Consumption

Item	Power Consumption (mA)	
	1 * Flash	2 * Flash
Normal	61.07	62.28
Suspend	0.356	0.402
Sleep	0.361	0.387
Read	106.90	121.98
Write	155.80	181.99

The above values are for reference only, it may change according to the flash memory used.

F. Electrical Specifications

Absolute Maximum Rating

Item	Symbol	Parameter	MIN	MAX	Unit
1	V_{DD}-V_{SS}	DC Power Supply	-0.3	+5.5	V
2	V_{IN}	Input Voltage	V_{SS}-0.3	V_{DD}+0.3	V
3	Ta	Operating Temperature (Commercial)	0	+70	℃
4	Ta	Operating Temperature (Industrial)	-40	+85	℃
5	Tst	Storage Temperature (Commercial)	-40	+85	℃
6	Tst	Storage Temperature (Industrial)	-50	+125	℃

Parameter	Symbol	Min	Typ	MAX	Unit
Operating Temperature (Commercial)	T_a	0	+25	+70	℃
Operating Temperature (Industrial)	T_a	-40	+25	+85	℃
V_{DD} Voltage	V_{DD}	3.0	3.3	3.6	V
		4.5	5.0	5.5	V

G. DC Characters

DC characteristics of 3.3V I/O Cells

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
VCCK	Core Power Supply	Core Area	1.62	1.8	1.98	V
VCC3IO	Power Supply	3.3V I/O	3.0	3.3	3.6	V
Temp	Junction Temperature		0	25	115	℃
Vt	Switching threshold	LVTTL		1.5		V
Vt-	Schmitt Trigger Negative Going threshold voltage	LVTTL	0.8	1.1		V
Vt+	Schmitt Trigger Positive Going threshold voltage			1.6	2.0	V
Vol	Output Low voltage	|Iol| = 2 ~ 16 mA			0.4	V
Voh	Output High voltage	|Ioh| = 2 ~ 16 mA	VCC3IO - 0.4			V
Rpu	Input Pull-Up Resistance	PU=high, PD=low	40	75	190	KΩ
Rpd	Input Pull-Down Resistance	PU=high, PD=low	40	75	190	KΩ
Iin	Input Leakage Current	Vin = VCC3I or 0			1	μA
Ioz	Tri-state Output Leakage Current		-10	±1	10	μA

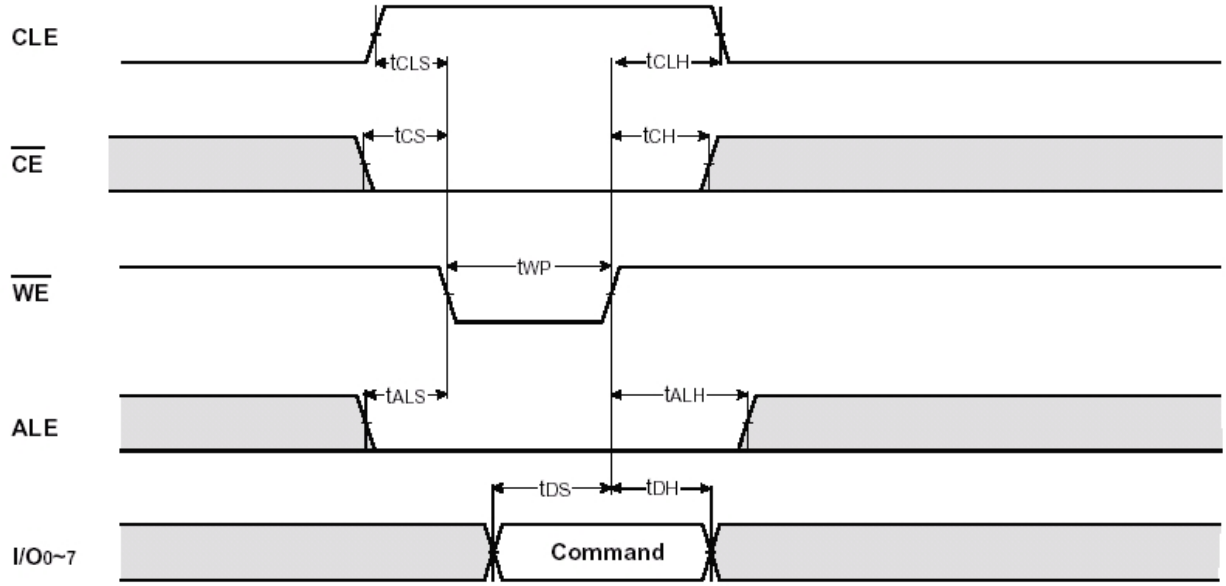
H. AC Characters

H1. Flash Memory Interface Timing

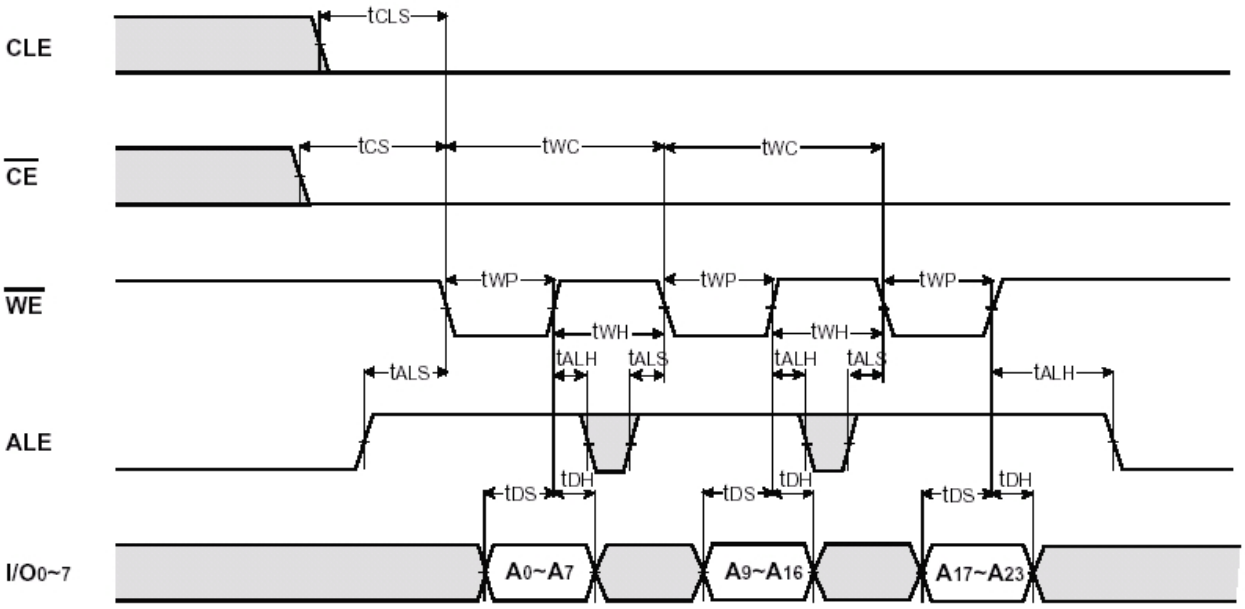
NAND Flash Memory Interface Timing

Parameter	Symbol	Min	Max	Unit
CLE Set-up Time	t_{CLS}	0	-	ns
CLE Hold Time	t_{CLH}	10	-	ns
CE Setup Time	t_{CS}	0	-	ns
CE Hold Time	t_{CH}	10	-	ns
WE Pulse Width	t_{WP}	25	-	ns
ALE Setup Time	t_{ALS}	0	-	ns
ALE Hold Time	t_{ALH}	10	-	ns
Data Setup Time	t_{DS}	20	-	ns
Data Hold Time	t_{DH}	10	-	ns
Write Cycle Time	t_{WC}	45	-	ns
WE High Hold Time	t_{WH}	15	-	ns
Read Cycle Time	t_{RC}	50	-	ns
/RE Pulse Width	t_{RP}	25	-	ns
/RE High Hold Time	t_{REH}	15	-	ns
Ready to /RE Low	t_{RR}	60	-	ns

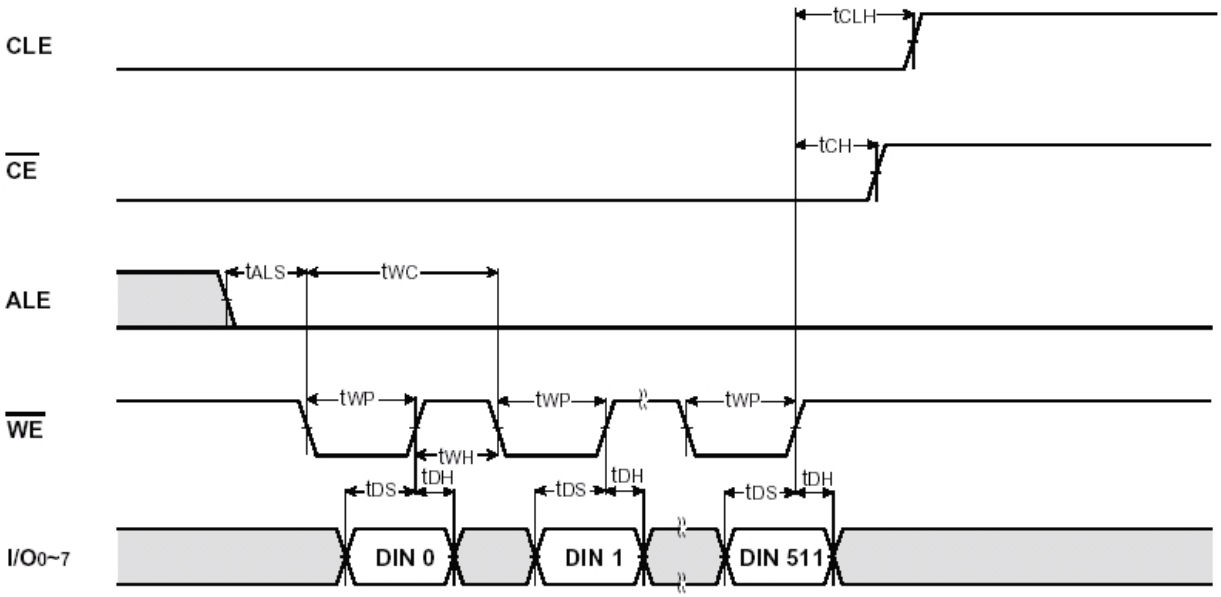
H1.1 Command Latch Cycle



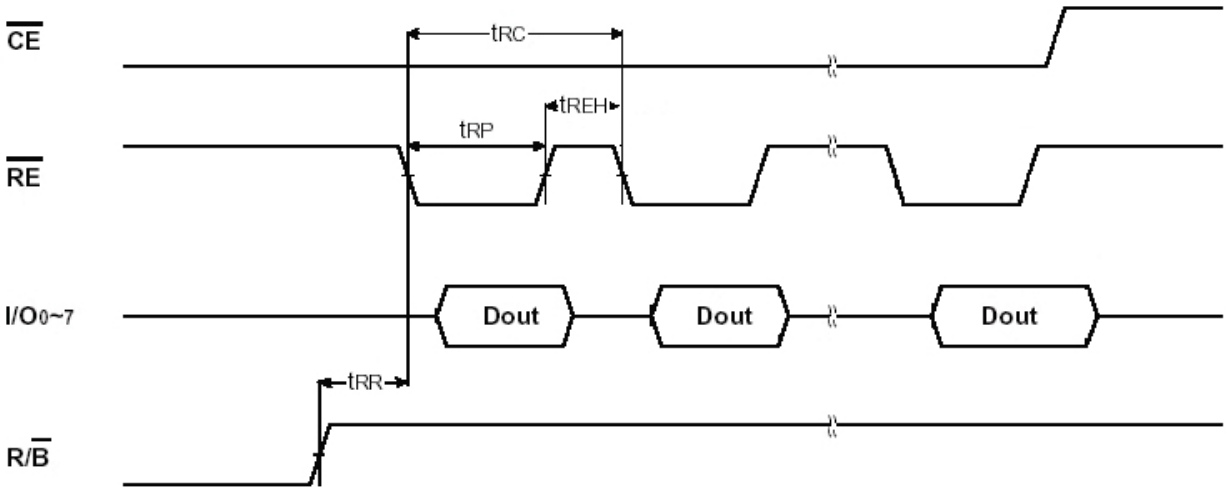
H1.2 Address Latch Cycle



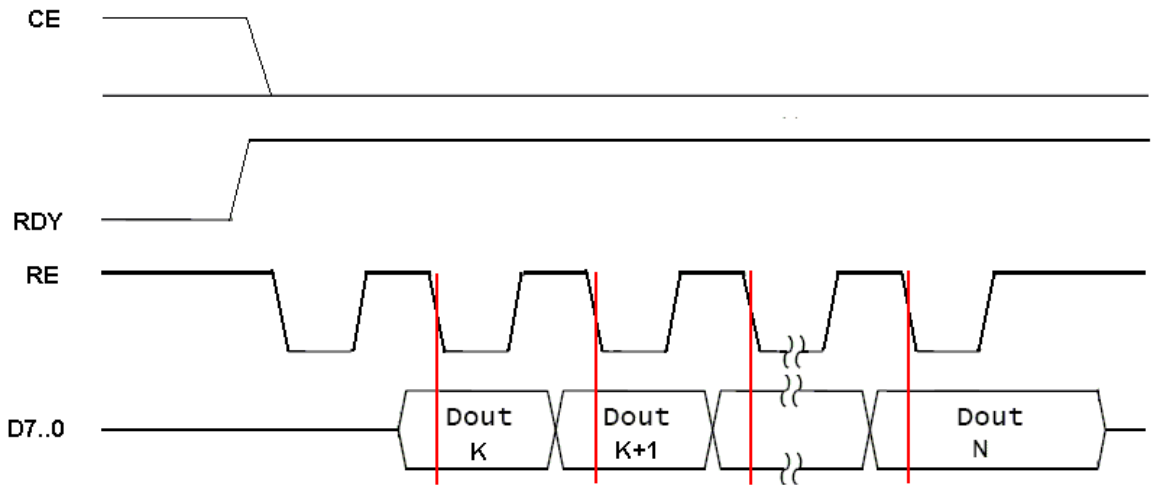
H1.3 Input Data Latch Cycle



H1.4 Sequential Out Cycle after Read (CLE=L, /WE=H, ALE=L)



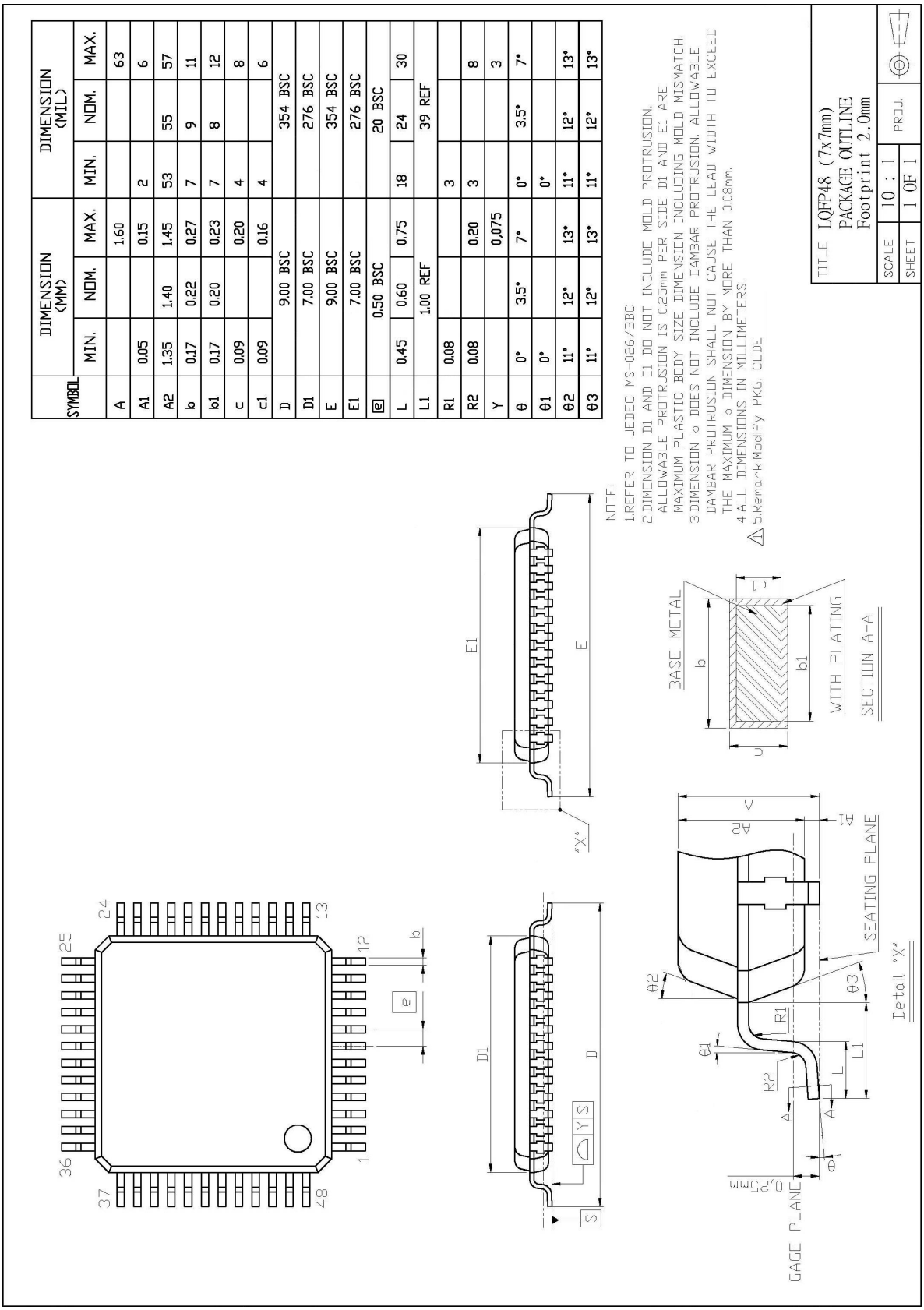
H1.5 EDO mode for data latch



EDO mode to latch the data at the negative edge of RE.

I. Package Information

I1. 48 Pins



SYMBOL	DIMENSION (MM) MIN.	NOM.	MAX.	DIMENSION (MIL.) MIN.	NOM.	MAX.
A			1.60			63
A1	0.05		0.15	2		6
A2	1.35	1.40	1.45	53	55	57
b	0.17	0.22	0.27	7	9	11
b1	0.17	0.20	0.23	7	8	12
c	0.09		0.20	4		8
c1	0.09		0.16	4		6
D		9.00 BSC			354 BSC	
D1		7.00 BSC			276 BSC	
E		9.00 BSC			354 BSC	
E1		7.00 BSC			276 BSC	
e		0.50 BSC			20 BSC	
L	0.45	0.60	0.75	18	24	30
L1		1.00 REF			39 REF	
R1	0.08			3		
R2	0.08		0.20	3		8
Y			0.075			3
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°			0°		
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°

I2. 64 Pins

SYMBOL	DIMENSION (MM) MIN.	NOM.	MAX.	DIMENSION (MIL) MIN.	NOM.	MAX.
A			1.60			63
A1	0.05		0.15	2		6
A2	1.35	1.40	1.45	53	55	57
b	0.13	0.18	0.23	5	7	9
b1	0.13	0.16	0.19	5	6	8
c	0.09		0.20	4		8
c1	0.09		0.16	4		6
D		9.00 BSC			354 BSC	
D1		7.00 BSC			276 BSC	
E		9.00 BSC			354 BSC	
E1		7.00 BSC			276 BSC	
e		0.40 BSC			15.8 BSC	
L	0.45	0.60	0.75	18	24	30
L1		1.00 REF			39 REF	
R1	0.08			3		
R2	0.08		0.20	3		8
Y			0.10			4
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°			0°		
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°

NOTE:
1.REFER TO JEDEC MS-026(ISSUE C)/BBD
2.DIMENSION D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.
3.DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.
4.ALL DIMENSIONS IN MILLIMETERS.

TITLE LQFP64 (7x7x1.4mm)
PACKAGE OUTLINE
Footprint 2.0mm
SCALE 10 : 1
SHEET 1 OF 1
PROJ.