

HS-C²MOSTM INTEGRATED CIRCUITS

046614(54-1)
046615(541)

M54HC540/541
M74HC540/541

PRELIMINARY DATA

HC540 OCTAL BUS BUFFER (INVERTING) (3-STATE)

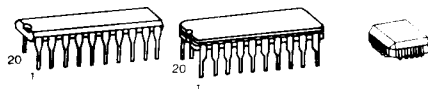
HC541 OCTAL BUS BUFFER (3-STATE)

DESCRIPTION

The M54/74HC540/541 are high speed CMOS OCTAL BUS BUFFERS (3-STATE) fabricated in silicon gate C²MOS technology. They have the same high speed performance of LSTTL combined with true CMOS low power consumption. The M54/74HC540 is an inverting buffer and the M54/74HC541 is a non-inverting buffer. The 3-STATE control gate operates as a two-input AND such that if either G1 or G2 are high, all eight outputs are in the high-impedance state.

In order to enhance PC board layout, the 'HC540 and 'HC541 offers a pinout having inputs and outputs on opposite sides of the package.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.



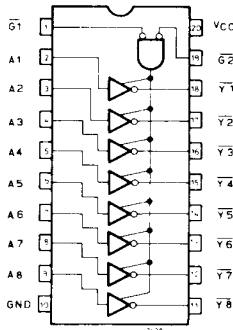
B1 Plastic Package **F1** Ceramic Package **C1** Chip Carrier

ORDERING NUMBERS: M54HCXXX F1
M74HCXXX B1
M74HCXXX F1
M74HCXXX C1

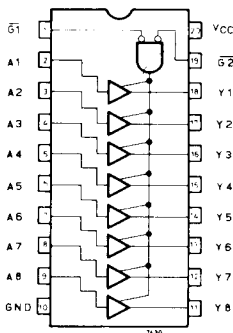
FEATURES

- High Speed
 $t_{PD} = 13 \text{ ns (Typ.) at } V_{CC} = 5V$
- Low Power Dissipation
 $I_{CC} = 4 \mu A \text{ (Max.) at } T_A = 25^\circ C$
- High Noise Immunity
 $V_{NIH} = V_{NIL} = 28\% V_{CC} \text{ (Min.)}$
- Output Drive Capability
15 LSTTL Loads
- Symmetrical Output Impedance
 $|I_{OH}| = I_{OL} = 6 \text{ mA (Min.)}$
- Balanced Propagation Delays
 $t_{PLH} = t_{PHL}$
- Wide Operating Voltage Range
 $V_{CC} \text{ (opr)} = 2V \text{ to } 6V$
- Pin and Function compatible with 54/74LS540/541

PIN CONNECTIONS (top view) HC540

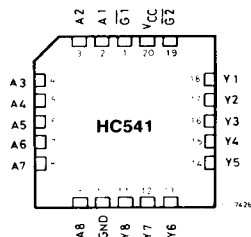
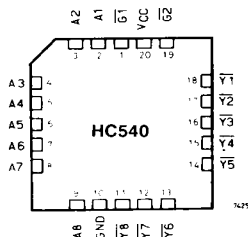


HC541



M54HC540/541 M74HC540/541

CHIP CARRIER



TRUTH TABLE HC540

OUTPUT INPUTS		
\bar{G}	A	\bar{Y}
H	*	Z
L	L	H
L	H	L

Z: High impedance

*: Don't care

TRUTH TABLE HC541

OUTPUT INPUTS		
\bar{G}	A	Y
H	*	Z
L	L	L
L	H	H

Z: High impedance

*: Don't care

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	- 0.5 to 7	V
V_I	DC Input Voltage	- 0.5 to $V_{CC} + 0.5$	V
V_O	DC Output Voltage	- 0.5 to $V_{CC} + 0.5$	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 35	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	- 65 to 150	$^{\circ}C$

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: $\cong 65^{\circ}C$ derate to 300 mW by 10 mW/ $^{\circ}C$: $65^{\circ}C$ to $85^{\circ}C$.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limit	Unit
V_{CC}	Supply Voltage	2 to 6	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_A	Operating Temperature 74HC Series 54HC Series	– 40 to 85 – 55 to 125	°C
t_r, t_f	Input Rise and Fall Time	$V_{CC} \begin{cases} 2 \text{ V} \\ 4.5 \text{ V} \\ 6 \text{ V} \end{cases} \begin{matrix} 0 \text{ to } 1000 \\ 0 \text{ to } 500 \\ 0 \text{ to } 400 \end{matrix}$	ns

DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25^\circ\text{C}$ 54HC and 74HC			– 40 to 85°C 74HC		– 55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0 4.5 6.0		1.5 3.15 4.2	— — —	— — —	1.5 3.15 4.2	— — —	1.5 3.15 4.2		V
V_{IL}	Low Level Input Voltage	2.0 4.5 6.0		— — —	— — —	0.5 1.35 1.8	— — —	0.5 1.35 1.8		0.5 1.35 1.8	V
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	V
		4.5	V_{IH} or	– 20 μA	4.4	4.5	—	4.4	—	4.4	
		6.0	V_{IL}	– 6.0 mA	5.9	6.0	—	5.9	—	5.9	
		4.5 6.0	V_{IL}	– 7.8 mA	4.18 5.68	4.31 5.8	— —	4.13 5.63	— —	4.10 5.60	
V_{OL}	Low Level Output Voltage	2.0	V_{IH} or	20 μA	—	0	0.1	—	0.1	0.1	V
		4.5	V_{IL}	6.0 mA	—	0.17	0.26	—	0.33	0.40	
		6.0	V_{IL}	7.8 mA	—	0.18	0.26	—	0.33	0.40	
		4.5 6.0	V_{IL}	7.8 mA	—	0.18	0.26	—	0.33	0.40	
I_I	Input Leakage Current	6.0	$V_I = V_{CC}$ or GND		—	—	± 0.1	—	± 1	± 1	μA
I_{OZ}	3-State Output Off-State Current	6.0	$V_I = V_{IH}$ or V_{IL} $V_O = V_{CC}$ or GND		—	—	± 0.5	—	± 5.0	± 10	μA
I_{CC}	Quiescent Supply Current	6.0	$V_I = V_{CC}$ or GND $I_O = 0$		—	—	4	—	40	80	μA

M54HC540/541 **M74HC540/541**

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V$, $T_A = 25^\circ C$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	CL (pF)	54HC and 74HC			Unit
			MIN.	TYP.	MAX.	
t_{TLH} t_{THL}	Output Transition Time	50		7	11	ns
t_{PLH} t_{PHL}	Propagation Delay Time	50		12	20	ns
t_{PZL} t_{PZH}	3-State Output Enable Time	50		17	27	ns
t_{PLH} t_{PLZ}	3-State Output Disable Time	50		16	26	ns

AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	V_{CC}	Test Condition	$T_A = 25^\circ C$ 54HC and 74HC			- 40 to 85°C 74HC		- 55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0 4.5 6.0		— — —	22 8 7	60 12 10	— — —	75 15 13			ns
t_{PLH} t_{PHL}	Propagation Delay Time	2.0 4.5 6.0		— — —	60 13 11	105 21 18	— — —	130 26 22			ns
t_{PZL} t_{PZH}	3-State Output Enable	2.0 4.5 6.0	$R_L = 1K\Omega$	— — —	65 18 16	145 29 25	— — —	175 35 130			ns
t_{PLZ} t_{PHZ}	3-State Output Disable Time	2.0 4.5 6.0	$R_L = 1K\Omega$	— — —	49 22 20	136 32 28	— — —	166 38 34			ns
C_{IN}	Input Capacitance			—	5	10	—	10			pF
$C_{PD} (*)$	Power Dissipation Capacitance										pF

Note (*) C_{PD} is defined as the value the IC's of internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the following equation.

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8 \text{ (per Circuit).}$$