FUJITSU SEMICONDUCTOR
DATA SHEET

DS07-16501-1E

32-Bit Proprietary Microcontroller

CMOS

FR65E Series

MB91340/MB91V340

■ DESCRIPTION

The MB91340/MB91V340 are standard microcontrollers that feature a 32-bit high-performance RISC CPU and a variety of built-in I/O resources and bus control mechanisms suitable for embedded control applications requiring high-capability, high-speed CPU processing. The large address space supported by the 32-bit CPU addressing means that operation is primarily based on external bus access although a large internal RAM area is included for high-speed execution of CPU instructions.
The MB91340 and MB91V340 are FR65E series products based on the FR30/40 series CPU with enhanced bus access for higher speed operation. The device specifications include a D/A converter to facilitate motor control and are ideal for use in DVD players that support fly-by transfer.

■ FEATURES

1. FR CPU

- 32-bit RISC, load/store architecture, 5-stage pipeline
- 66MHz operating frequency [when using PLL with base frequency = 16.5 MHz]
- 16-bit fixed length instructions (basic instructions), 1 instruction per cycle
- Instruction set optimized for embedded applications: Memory-to-memory transfer, bit manipulation, barrel shift etc.

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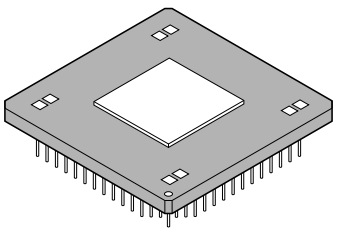
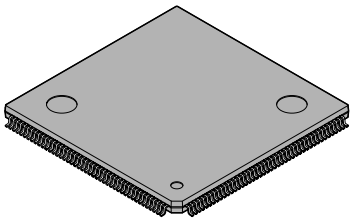
■ PACKAGE

361-pin, Ceramic PGA



(PGA-361C-A01)

176-pin, Plastic LQFP



(FPT-176P-M02)

FUJITSU

- Instructions adapted for high-level languages: Function entry/exit instructions, multiple-register load/store instructions
- Easier assembler coding: Register interlock function
- Internal multiplier with instruction-level support
  Signed 32-bit multiplication : 5 cycles
  Signed 16-bit multiplication : 3 cycles
- Interrupt (PC, PS save) : 6 cycles, 16 priority levels
- Harvard architecture for simultaneous program and data access
- Linear access to large 4 GB memory space
- Instructions compatible with FR series

2. Bus interface

- Operating frequency : Max 33MHz
- Full 24-bit address output (16MB memory space)
- 8-bit or 16-bit data input/output (The MB91V340 supports 32-bit data input/output)
- Built-in pre-fetch buffer
- Unused data and address pins can be used as general-purpose input/output ports
- Eight fully independent chip select outputs, can be set in minimum 64 KB units
- Supports the following memory interfaces
  SRAM, ROM/Flash
  Page mode flash ROM, page mode ROM interface
  Burst mode flash ROM (selectable burst length = 1, 2, 4, or 8)
- Basic bus cycle : 2 cycles
- Automatic wait cycle generation function can insert wait cycles, independently programmable for each memory area
- RDY input for external wait cycles
- DMA supports fly-by transfer with independent I/O wait control

3. Internal memory

- 64 KB mask ROM
- 4 KB data RAM
- 112 KB RAM. In addition to use as data RAM, this RAM area can also be used for reading and writing of instruction codes. (128 KB on the MB91V340)

4. Instruction cache (MB91V340 only)

- Size : 4 KB
- 2-way set associative
- 4 words (16 bytes) per set
- Lock function enables program code to be made cache-resident
- Areas not used for instruction cache can be used as instruction RAM

5. DMAC (DMA Controller)

- 5-channel (3-channel external-to-external)
- 3 transfer triggers : External pin, internal peripheral, software
- Addressing using 32-bit full addressing mode (increment, decrement, fixed)
- Transfer modes : Demand transfer, burst transfer, step transfer, or block transfer
- Supports fly-by transfer (between external I/O and memory)
- Selectable transfer data size : 8, 16, or 32-bit

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6. Bit search module (for REALOS)
- Searches words from MSB for position of first 1/0 bit value change

7. Timers
- 16-bit reload timer : 4 channels (1 channel used by REALOS)
  Selectable clock : Internal clock divided by 2, 8, or 32 (divided by 64 or 128 also available for channel 3 only)
- 16-bit freerun timer : 1 channel, output compare: 8 channels,
  input capture : 4 channels
- 8-bit up counter : 1 channel
- 8/16-bit up/down timer/counter : 8-bit x 4 channels or 16-bit x 2 channels

8. UART
- Full duplex, double buffer UART
- 3 channels
- Parity/no parity selection
- Asynchronous (start-stop synchronized) or CLK-synchronous communications selectable
- Internal dedicated baud rate timer
- External clock can be used as transfer clock
- Variety of error detection functions (parity, frame, overrun)

9. Interrupt controller
- Total of 9 external interrupts : 1 non-maskable interrupt pin and 8 normal interrupt pins
- Interrupts from internal peripheral devices
- Programmable priorities (16 levels) for all interrupts except the non-maskable interrupt
- Can be used to wake-up from stop mode

10. D/A converter
- 8-bit resolution, 3 channels

11. A/D converter
- 10-bit resolution, 8 channels
- Successive approximation type, conversion time : 5.4 μs
- Conversion modes : Single conversion mode, continuous conversion mode
- Conversion triggers : Software, external trigger, peripheral interrupt
- 8-bit result register

12. Other interval timers
- 16-bit timer : 3 channels (U-TIMER)
- Watchdog timer

13. I^2C bus interface
- 1 channel, master/slave sending and receiving
- Arbitration function
- “Standard mode” or “terminal split mode” external interface

14. I/O ports
- Maximum 107 ports (Maximum 125 ports on MB91V340)

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15. Other features

- Internal version register (3-bit) allows chip version to be detected
- Built-in oscillator circuit for clock source, selectable PLL multiplier
- $\overline{\text{INIT}}$ reset pin
- Resets can also be triggered by a watchdog timer reset or software reset
- Power-saving modes : Stop mode, sleep mode
- Gear function
- Internal timebase timer
- Package : LQFP-176
- CMOS technology MB91V340/MB91340 (0.25 µm)
- Supply voltage 3.3 V ± 0.3 V , 2.5 V ± 0.2 V

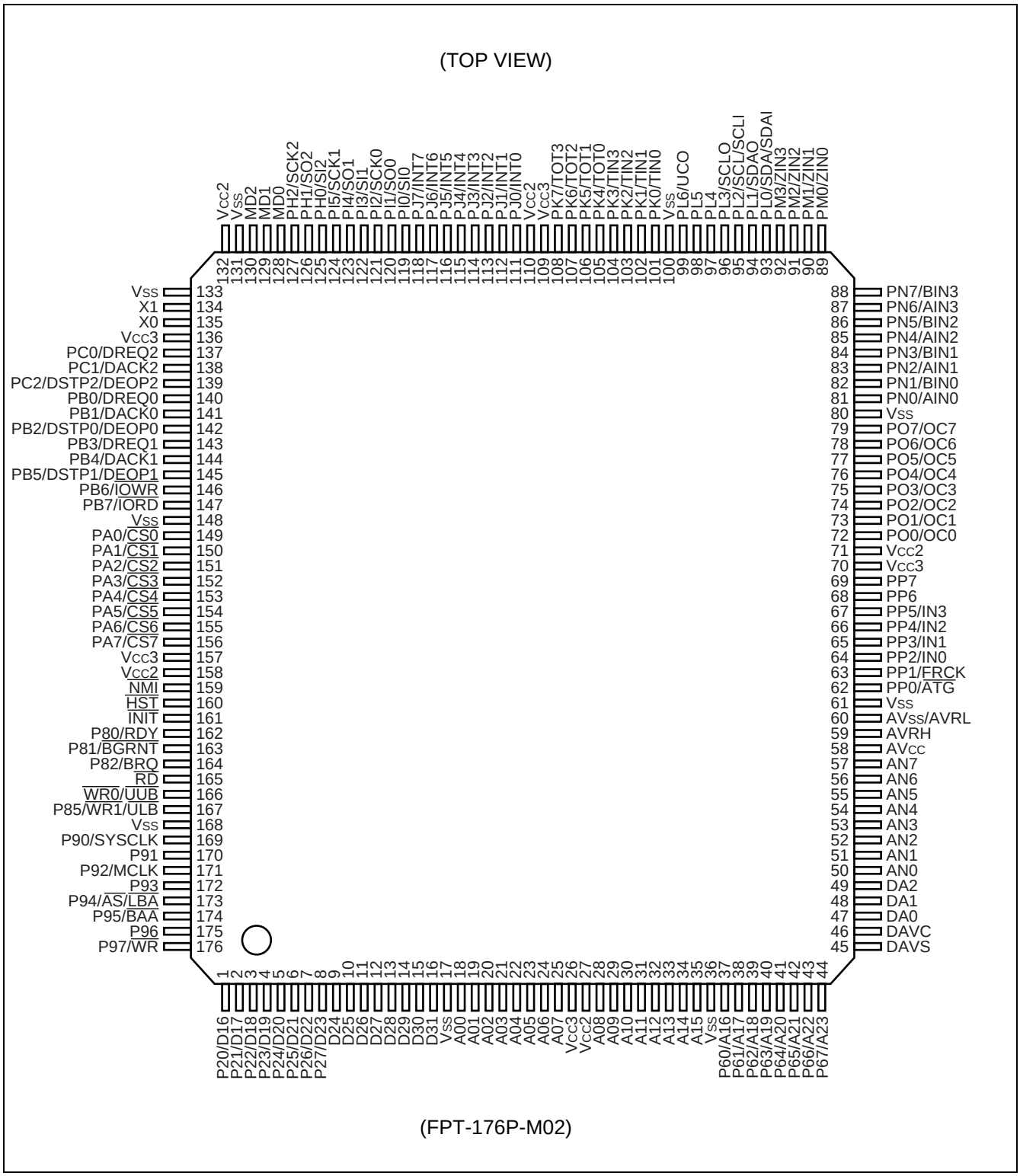
Note : I^2C license
Purchase of Fujitsu I^2C components conveys a license under the Philips I^2C Patent rights to use these components in an I^2C system provided that the system conforms to the I^2C Standard Specification as defined by Philips.

■ PRODUCT LINEUP

	MB91340	MB91V340
Type	MASK ROM version (for volume production)	Evaluation version (For evaluation and development)
Max external bus width	16-bit	32-bit
Max no. of ports	107	125 (additional ports are P00 to P07, P10 to P17, P86, P87)
Write strobe	$\overline{\text{WR0}}$ to $\overline{\text{WR1}}$	$\overline{\text{WR0}}$ to $\overline{\text{WR3}}$
RAM	112 KB	128 KB
ROM	64 KB mask ROM	64 KB emulation RAM
Instruction cache	None	4 KB
Package	LQFP-176	PGA-361
Other	Currently in production	Currently available

■ PIN ASSIGNMENTS

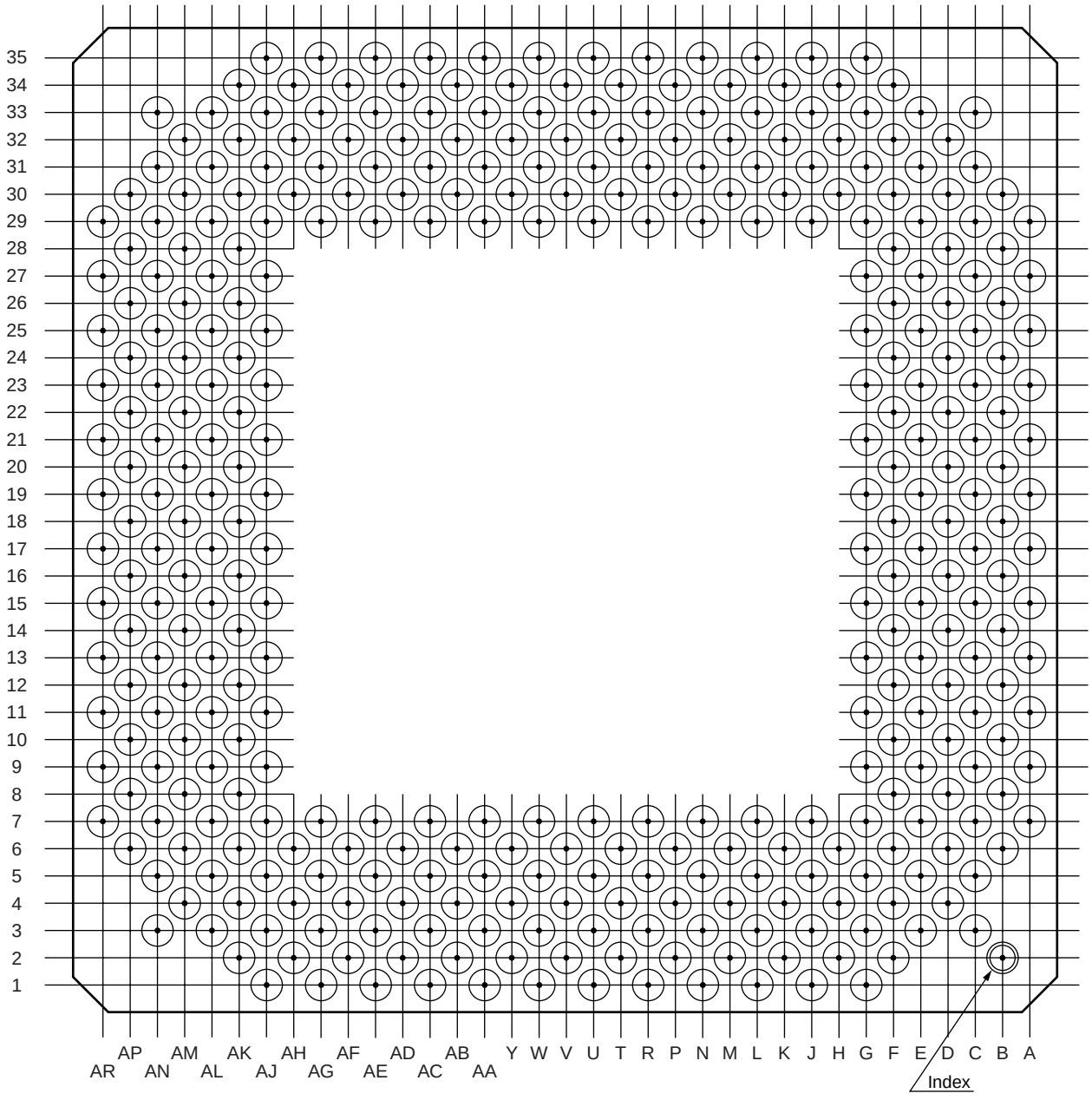
- MB91340



(FPT-176P-M02)

- MB91V340

(BOTTOM VIEW)



(PGA-361C-A01)

Note : Operation of 32-bit bus pins P00/D00 to P17/D15, P86/$\overline{WR2}$ and P87/$\overline{WR3}$ is not currently guaranteed.

■ PIN NO. TABLE

• Device : MB91V340 Package : PGA-361C-A01

No.	PIN	Pin Name	Remarks	No.	PIN	Pin Name	Remarks
1	F6	P13/D11	V340	36	G17	$V_{CC}2$	
2	C5	P14/D12	V340	37	A15	A08	
3	E7	P15/D13	V340	38	D16	A09	
4	G7	V_{SS}		39	E17	A10	
5	F8	P16/D14	V340	40	B16	A11	
6	D6	P17/D15	V340	41	F18	A12	
7	G9	$V_{CC}2$		42	D18	A13	
8	B6	P20/D16		43	C17	A14	
9	C7	P21/D17		44	G19	V_{SS}	
10	F10	P22/D18		45	A17	A15	
11	E9	P23/D19		46	E19	P60/A16	
12	D8	P24/D20		47	B20	P61/A17	
13	G11	V_{SS}		48	B18	P62/A18	
14	A9	P25/D21		49	D20	P63/A19	
15	F12	P26/D22		50	C19	P64/A20	
16	B8	P27/D23		51	F20	$V_{CC}3$	
17	C11	D24		52	A19	P65/A21	
18	C9	D25		53	E21	P66/A22	
19	A11	D26		54	G21	V_{SS}	
20	E11	D27		55	C21	P67/A23	
21	F14	$V_{CC}3$		56	A21	EX_A23	V340
22	E13	D28		57	F22	DAVS	
23	G13	V_{SS}		58	D22	DAVC	
24	D12	D29		59	B22	DA0	
25	D10	D30		60	B24	DA1	
26	C13	D31		61	C23	DA2	
27	B10	A00		62	D24	AN0	
28	E15	A01		63	E23	AN1	
29	B12	A02		64	G23	V_{SS}	
30	D14	A03		65	A23	AN2	
31	B14	A04		66	G25	$V_{CC}2$	
32	A13	A05		67	A25	AN3	
33	G15	V_{SS}		68	B26	AN4	
34	F16	A06		69	F24	AN5	
35	C15	A07		70	D26	AN6	

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No.	PIN	Pin Name	Remarks	No.	PIN	Pin Name	Remarks
71	C25	AN7		106	L33	PM1/ZIN1	
72	B28	AV_{CC}		107	M30	$V_{CC}3$	
73	E25	AVRH		108	L35	PM2/ZIN2	
74	G27	V_{SS}		109	N29	V_{SS}	
75	A27	$AVRL/AV_{SS}$		110	M32	PM3/ZIN3	
76	C27	PP0/$\overline{ATG}$		111	M34	PL0/SDA/SDAI	
77	E27	PP1/FRCK		112	N31	PL1/SDAO	
78	D28	PP2/IN0		113	P32	PL2/SCL/SCLI	
79	C29	PP3/IN1		114	N33	PL3/SCLO	
80	F26	$V_{CC}3$		115	P34	PL4	
81	D30	PP4/IN2		116	P30	PL5	
82	B30	PP5/IN3		117	T32	PL6/UCO	
83	F28	V_{SS}		118	N35	PK0/TIN0	
84	E29	PP6		119	R29	V_{SS}	
85	C31	PP7		120	R31	PK1/TIN1	
86	E31	PO0/OC0		121	R33	PK2/TIN2	
87	F30	PO1/OC1		122	U29	$V_{CC}2$	
88	E33	PO2/OC2		123	T30	PK3/TIN3	
89	G31	PO3/OC3		124	T34	PK4/TOT0	
90	G29	V_{SS}		125	R35	PK5/TOT1	
91	H30	PO4/OC4		126	V34	PK6/TOT2	
92	F32	PO5/OC5		127	U33	PK7/TOT3	
93	J29	$V_{CC}2$		128	V32	PJ0/INT0	
94	F34	PO6/OC6		129	U31	PJ1/INT1	
95	H32	PO7/OC7		130	W29	V_{SS}	
96	J31	PN0/AIN0		131	U35	PJ2/INT2	
97	H34	PN1/BIN0		132	V30	PJ3/INT3	
98	K30	PN2/AIN1		133	Y34	PJ4/INT4	
99	L29	V_{SS}		134	W35	PJ5/INT5	
100	G33	PN3/BIN1		135	Y32	PJ6/INT6	
101	J33	PN4/AIN2		136	W33	PJ7/INT7	
102	K32	PN5/BIN2		137	Y30	$V_{CC}3$	
103	L31	PN6/AIN3		138	W31	PI0/SI0	
104	K34	PN7/BIN3		139	AA35	PI1/SO0	
105	J35	PM0/ZIN0		140	AA29	V_{SS}	

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No.	PIN	Pin Name	Remarks	No.	PIN	Pin Name	Remarks
141	AA33	PI2/SCK0		176	AJ29	V_{SS}	
142	AB34	PI3/SI1		177	AK28	TDT45	V340
143	AC35	PI4/SO1		178	AM30	TDT44	V340
144	AB32	PI5/SCK1		179	AJ27	$V_{CC}2$	
145	AA31	PH0/SI2		180	AP30	TDT43	V340
146	AD34	PH1/SO2		181	AN29	TDT42	V340
147	AC33	PH2/SCK2		182	AK26	TDT41	V340
148	AD32	TDT68	V340	183	AL27	TDT40	V340
149	AE35	TDT67	V340	184	AM28	TDT39	V340
150	AC29	V_{SS}		185	AJ25	V_{SS}	
151	AB30	TDT66	V340	186	AR27	TDT38	V340
152	AD30	$V_{CC}2$		187	AK24	TDT37	V340
153	AC31	TDT65	V340	188	AP28	TDT36	V340
154	AF34	TDT64	V340	189	AN25	TDT35	V340
155	AE33	TDT63	V340	190	AN27	TDT34	V340
156	AF32	TDT62	V340	191	AR25	TDT33	V340
157	AG35	TDT61	V340	192	AL25	TDT32	V340
158	AH34	TDT60	V340	193	AK22	$V_{CC}3$	
159	AE31	TDT59	V340	194	AL23	TDT31	V340
160	AG29	V_{SS}		195	AJ23	V_{SS}	
161	AG33	TDT58	V340	196	AM24	TDT30	V340
162	AH32	TDT57	V340	197	AM26	TDT29	V340
163	AG31	TDT56	V340	198	AN23	TDT28	V340
164	AF30	TDT55	V340	199	AP26	TDT27	V340
165	AJ33	TDT54	V340	200	AL21	TDT26	V340
166	AE29	$V_{CC}3$		201	AP24	TDT25	V340
167	AK32	TDT53	V340	202	AM22	TDT24	V340
168	AK34	TDT52	V340	203	AP22	TDT23	V340
169	AH30	V_{SS}		204	AR23	TDT22	V340
170	AJ31	TDT51	V340	205	AJ21	V_{SS}	
171	AL33	TDT50	V340	206	AK20	TDT21	V340
172	AL31	TDT49	V340	207	AN21	TDT20	V340
173	AK30	TDT48	V340	208	AJ19	$V_{CC}2$	
174	AN31	TDT47	V340	209	AR21	TDT19	V340
175	AL29	TDT46	V340	210	AM20	TDT18	V340

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No.	PIN	Pin Name	Remarks	No.	PIN	Pin Name	Remarks
211	AL19	TDT17	V340	246	AJ9	V_{SS}	
212	AP20	TDT16	V340	247	AR9	TAD08	V340
213	AK18	TDT15	V340	248	AN9	TAD07	V340
214	AM18	TDT14	V340	249	AL9	TAD06	V340
215	AN19	TDT13	V340	250	AM8	TAD05	V340
216	AJ17	V_{SS}		251	AN7	TAD04	V340
217	AR19	TDT12	V340	252	AK10	$V_{CC}3$	
218	AL17	TDT11	V340	253	AM6	TAD03	V340
219	AP16	TDT10	V340	254	AP6	TAD02	V340
220	AP18	TDT09	V340	255	AK8	V_{SS}	
221	AM16	TDT08	V340	256	AL7	TAD01	V340
222	AN17	TDT07	V340	257	AN5	TAD00	V340
223	AK16	$V_{CC}3$		258	AL5	EXRAM	V340
224	AR17	TDT06	V340	259	AK6	BREAK	
225	AL15	TDT05	V340	260	AL3	ICD3	V340
226	AJ15	V_{SS}		261	AJ5	ICD2	V340
227	AN15	TDT04	V340	262	AJ7	V_{SS}	
228	AR15	TDT03	V340	263	AH6	ICD1	V340
229	AK14	TDT02	V340	264	AK4	ICD0	V340
230	AM14	TDT01	V340	265	AG7	$V_{CC}2$	
231	AP14	TDT00	V340	266	AK2	ICS2	V340
232	AP12	$\overline{TWR}$	V340	267	AH4	ICS1	V340
233	AN13	$\overline{TADSC}$	V340	268	AG5	ICS0	V340
234	AM12	$\overline{TCE1}$	V340	269	AH2	ICLK	V340
235	AL13	$\overline{TOE}$	V340	270	AF6	$\overline{RST}$	V340
236	AJ13	V_{SS}		271	AE7	V_{SS}	
237	AR13	TCLK	V340	272	AJ3	MD0	
238	AJ11	$V_{CC}2$		273	AG3	MD1	
239	AR11	TAD15	V340	274	AF4	MD2	
240	AP10	TAD14	V340	275	AE5	$V_{CC}2$	V340
241	AK12	TAD13	V340	276	AF2	OPEN	V340
242	AM10	TAD12	V340	277	AG1	OPEN	V340
243	AN11	TAD11	V340	278	AE3	OPEN	V340
244	AP8	TAD10	V340	279	AD6	$V_{CC}3$	
245	AL11	TAD09	V340	280	AE1	X0	

(Continued)

No.	PIN	Pin Name	Remarks	No.	PIN	Pin Name	Remarks
281	AC7	V_{SS}		316	P4	$\overline{RD}$	
282	AD4	X1		317	R5	$\overline{WR0}/\overline{UUB}$	
283	AD2	PC0/DREQ2		318	M2	P85/$\overline{WR1}/\overline{ULB}$	
284	AC5	$V_{CC}2$	V340	319	N3	P86/$\overline{WR2}/\overline{LUB}$	V340
285	AB4	PC1/DACK2		320	M4	P87/$\overline{WR3}/\overline{LLB}$	V340
286	AC3	PC2/DSTP2/ DEOP2		321	L1	P90/SYSCLK	
287	AB2	PB0/DREQ0		322	N7	V_{SS}	
288	AB6	PB1/DACK0		323	P6	P91	
289	Y4	PB2/DSTP0/ DEOP0		324	M6	$V_{CC}2$	
290	AC1	PB3/DREQ1		325	N5	P92/MCLK	
291	AA7	V_{SS}		326	K2	P93	
292	AA5	PB4/DACK1		327	L3	P94/$\overline{AS}/\overline{LBA}$	
293	AA3	PB5/DSTP1/ DEOP1		328	K4	P95/$\overline{BAA}$	
294	W7	$V_{CC}2$		329	J1	P96	
295	Y6	PB6/$\overline{IOWR}$		330	H2	P97/$\overline{WR}$	
296	Y2	PB7/$\overline{IORD}$		331	L5	P00/D00	V340
297	AA1	PA0/$\overline{CS0}$		332	J7	V_{SS}	
298	V2	PA1/$\overline{CS1}$		333	J3	P01/D01	V340
299	W3	PA2/$\overline{CS2}$		334	H4	P02/D02	V340
300	V4	PA3/$\overline{CS3}$		335	J5	P03/D03	V340
301	W5	PA4/$\overline{CS4}$		336	K6	P04/D04	V340
302	U7	V_{SS}		337	G3	P05/D05	V340
303	W1	PA5/$\overline{CS5}$		338	L7	$V_{CC}3$	
304	V6	PA6/$\overline{CS6}$		339	F4	P06/D06	V340
305	T2	PA7/$\overline{CS7}$		340	F2	P07/D07	V340
306	U1	$\overline{NMI}$		341	H6	V_{SS}	
307	T4	$\overline{HST}$		342	G5	P10/D08	V340
308	U3	$\overline{INIT}$		343	E3	P11/D09	V340
309	T6	$V_{CC}3$		344	E5	P12/D10	V340
310	U5	$\overline{EX\_BGRNT}$	V340	345	A7	OPEN	V340
311	R1	EX_BRQ	V340	346	A29	OPEN	V340
312	R7	V_{SS}		347	B2	OPEN	V340
313	R3	P80/RDY		348	C3	OPEN	V340
314	P2	P81/$\overline{BGRNT}$		349	C33	OPEN	V340
315	N1	P82/BRQ		350	D4	OPEN	V340

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No.	PIN	Pin Name	Remarks	No.	PIN	Pin Name	Remarks
351	D32	OPEN	V340	357	AM32	OPEN	V340
352	G1	OPEN	V340	358	AN3	OPEN	V340
353	G35	OPEN	V340	359	AN33	OPEN	V340
354	AJ1	OPEN	V340	360	AR7	OPEN	V340
355	AJ35	OPEN	V340	361	AR29	OPEN	V340
356	AM4	OPEN	V340				

Note : Pins with “V340” in the “Remarks” column are present on the MB91V340 only. They are not present on the MB91340 mask ROM version.

■ PIN DESCRIPTIONS

Refer to the Pin Assignment diagram. Pins used by the MB91V340 evaluation tools are not included in these pin descriptions.

Pin no.		Pin name	I/O circuit type	Function
MB91340	MB91V340			
—	331, 333 to 337, 339 to 340	D00 to D07	C	External data bus bits 0 to 7 *
		P00 to P07		Can be used as ports in 8-bit or 16-bit external bus mode. *
—	342 to 344, 1 to 3, 5 to 6	D08 to D15	C	External data bus bits 08 to 15 *
		P10 to P17		Can be used as ports in 8-bit or 16-bit external bus mode. *
1 to 8	8 to 12, 14 to 16	D16 to D23	C	External data bus bits 16 to 23
		P20 to P27		Can be used as ports in 8-bit external bus mode.
9 to 16	17 to 20, 22, 24 to 26	D24 to D31	C	External data bus bits 24 to 31
18 to 25	27 to 32, 34 to 35	A00 to A07	C	External address bus bits 0 to 7
28 to 35	37 to 43, 45	A08 to A15	C	External address bus bits 8 to 15
37 to 44	46 to 50, 52 to 53, 55	A16 to A23	C	External address bus bits 16 to 23
		P60 to P67		Can be used as ports when external address bus not used.
—	56	EX_A23	J	External address bus bit 23. This outputs the status of the internal bus. *
47 to 49	59 to 61	DA0 to DA2	—	D/A converter output pins
50 to 57	62 to 63, 65, 67 to 71	AN0 to AN7	D	Analog input pins
62	76	$\overline{ATG}$	C	[$\overline{ATG}$] External trigger input for A/D converter. This input is used continuously when selected as the A/D converter start trigger. In this case, do not output to this port unless doing so intentionally.
		PP0		[PP0] General purpose input/output port.
63	77	FRCK	C	[FRCK] External clock input pin for freerun timer. This input is used continuously when selected as the external clock input pin for the freerun timer. In this case, do not output to this port unless doing so intentionally.
		PP1		[PP1] General purpose input/output pin.
64 to 67	78 to 79, 81 to 82	IN0 to IN3	C	[IN0-IN3] Input capture input pin. These inputs are used continuously when selected as input capture inputs. In this case, do not output to these ports unless doing so intentionally.
		PP2 to PP5		[PP2-PP5] General purpose input/output ports.
68 to 69	84 to 85	PP6 to PP7	C	[PP6-PP7] General purpose input/output ports.

* : Shaded pins are only present on the MB91V340.

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Pin no.		Pin name	I/O circuit type	Function
MB91340	MB91V340			
72 to 79	86 to 89, 91 to 92, 94 to 95	OC0 to OC7	C	[OC0-OC7] Output compare output pins.
		PO0 to PO7		[PO0-PO7] General purpose input/output ports. These pins can be used as ports when the output from the output compare unit is not used.
81 to 88	96 to 98, 100 to 104	AIN0, BIN0, AIN1, BIN1, AIN2, BIN2, AIN3, BIN3	C	[AIN0, BIN0, AIN1, BIN1, AIN2, BIN2, AIN3, BIN3] Up/down timer inputs. These inputs are used continuously when input is enabled. In this case, do not output to these ports unless doing so intentionally.
		PN0 to PN7		[PN0-PN7] General purpose input/output ports.
89 to 92	105 to 106, 108, 110	ZIN0 to ZIN3	C	[ZIN0-ZIN3] Up/down timer inputs. These inputs are used continuously when input is enabled. In this case, do not output to these ports unless doing so intentionally.
		PM0 to PM3		[PM0-PM3] General purpose input/output ports.
93	111	SDA	C	[SDA] Data input/output pin for the I²C bus. The pin has this function when I²C is enabled in standard mode. In this case, do not output to this port unless doing so intentionally. (Open drain output)
		SDAI		[SDAI] Data input pin for the I²C bus. The pin has this function when I²C is enabled in terminal split mode. In this case, do not output to this port unless doing so intentionally.
		PL0		[PL0] General purpose input/output port. The pin operates as a port when I²C operation is disabled.
94	112	SDAO	C	[SDAO] Data output pin for the I²C bus. The pin operates as a dedicated data output when I²C is enabled in terminal split mode.
		PL1		[PL1] General purpose input/output port. The pin operates as a port when I²C terminal split mode operation is disabled.
95	113	SCL	C	[SCL] Clock input/output pin for the I²C bus. The pin has this function when I²C is enabled in standard mode. In this case, do not output to this port unless doing so intentionally. (Open drain output)
		SCLI		[SCLI] Clock input pin for the I²C bus. The pin has this function when I²C is enabled in terminal split mode. In this case, do not output to this port unless doing so intentionally.
		PL2		[PL2] General purpose input/output port. The pin operates as a port when I²C operation is disabled.
96	114	SCLO	C	[SCLO] Clock output pin for the I²C bus. The pin is used as the clock output when I²C is enabled in terminal split mode.
		PL3		[PL3] General purpose input/output port. The pin operates as a port when I²C terminal split mode operation is disabled.

* : Shaded pins are only present on the MB91V340.

(Continued)

Pin no.		Pin name	I/O circuit type	Function
MB91340	MB91V340			
97 to 98	115 to 116	PL4 to PL5	C	[PL4-PL5] General purpose input/output ports.
99	117	UCO	C	[UCO] Pulse output for 8-bit up counter. The pin outputs pulses when pulse output is enabled for the 8-bit up counter.
		PL6		[PL6] General purpose input/output port. The pin operates as a port when output is disabled for the 8-bit up counter.
101 to 104	118, 120 to 121, 123	TIN0 to TIN3	C	[TIN0-TIN3] Reload timer inputs. These inputs are used continuously when the corresponding timer input is enabled. In this case, do not output to these ports unless doing so intentionally.
		PK0 to PK3		[PK0-PK3] General purpose input/output ports.
105 to 108	124 to 127	TOT0 to TOT3	C	[TOT0-TOT3] Reload timer output ports. The pins operate as reload timer output ports when timer output is enabled.
		PK4 to PK7		[PK4-PK7] General purpose input/output ports. The pins operate as ports when timer output is disabled.
111 to 118	128 to 129, 131 to 136	INT0 to INT7	I	[INT0-INT7] External interrupt inputs. These inputs are used continuously when the corresponding external interrupt is enabled. In this case, do not output to these ports unless doing so intentionally.
		PJ0 to PJ7		[PJ0-PJ7] General purpose input/output ports.
119	138	SI0	C	[SI0] UART0 data input pin. This input is used continuously when UART0 is performing input. In this case, do not output to this port unless doing so intentionally.
		PI0		[PI0] General purpose input/output port.
120	139	SO0	C	[SO0] UART0 data output pin. The pin has this function when UART0 data output is enabled.
		PI1		[PI1] General purpose input/output port. The pin has this function when UART0 data output is disabled.
121	141	SCK0	C	[SCK0] UART0 clock input/output pin. The pin has this function when UART0 clock output is enabled.
		PI2		[PI2] General purpose input/output port. The pin has this function when UART0 clock output is disabled.
122	142	SI1	C	[SI1] UART1 data input pin. This input is used continuously when UART1 is performing input. In this case, do not output to this port unless doing so intentionally.
		PI3	C	[PI3] General purpose input/output port.
123	143	SO1	C	[SO1] UART1 data output pin. The pin has this function when UART1 data output is enabled.
		PI4		[PI4] General purpose input/output port. The pin has this function when UART1 data output is disabled.

* : Shaded pins are only present on the MB91V340.

(Continued)

Pin no.		Pin name	I/O circuit type	Function
MB91340	MB91V340			
124	144	SCK1	C	[SCK1] UART1 clock input/output pin. The pin has this function when UART1 clock output is enabled.
		PI5		[PI5] General purpose input/output port. The pin has this function when UART1 clock output is disabled.
125	145	SI2	C	[SI2] UART2 data input pin. This input is used continuously when UART2 is performing input. In this case, do not output to this port unless doing so intentionally.
		PH0		[PH0] General purpose input/output port.
126	146	SO2	C	[SO2] UART1 data output pin. The pin has this function when UART2 data output is enabled.
		PH1		[PH1] General purpose input/output port. The pin has this function when UART2 data output is disabled.
127	147	SCK2	C	[SCK2] UART2 clock input/output pin. The pin has this function when UART2 clock output is enabled.
		PH2		[PH2] General purpose input/output port. The pin has this function when UART2 clock output is disabled.
128 to 130	272 to 274	MD0 to MD2	G	[MD0-MD2] Mode pins 0 to 2. The levels applied to these pins set the basic operating mode. Connect to VCC or VSS.
134	282	X1	A	Clock (oscillation) output
135	280	X0	A	Clock (oscillation) input
137	283	DREQ2	C	[DREQ2] External input for DMA transfer requests. This input is used continuously when selected as a DMA activation trigger. In this case, do not output to this port unless doing so intentionally.
		PC0		[PC0] General purpose input/output port.
138	285	DACK2	C	[DACK2] External acknowledge output for DMA transfer requests. The pin has this function when outputting DMA transfer request acknowledgement is enabled.
		PC1		[PC1] General purpose input/output port. The pin has this function when outputting DMA transfer request acknowledgement is disabled.
139	286	DEOP2	C	[DEOP2] Completion output for DMA external transfer. The pin has this function when outputting DMA transfer completion is enabled.
		DSTP2		[DSTP2] Stop input for DMA external transfer. The pin has this function when the stop input is enabled for DMA transfer.
		PC2		[PC2] General purpose input/output port. The pin has this function when completion output and stop input are disabled for DMA transfer.

* : Shaded pins are only present on the MB91V340.

(Continued)

Pin no.		Pin name	I/O circuit type	Function
MB91340	MB91V340			
140	287	DREQ0	C	[DREQ0] External input for DMA transfer requests. This input is used continuously when selected as a DMA activation trigger. In this case, do not output to this port unless doing so intentionally.
		PB0		[PB0] General purpose input/output port.
141	288	DACK0	C	[DACK0] External acknowledge output for DMA transfer requests. The pin has this function when outputting DMA transfer request acknowledgement is enabled.
		PB1		[PB1] General purpose input/output port. The pin has this function when outputting DMA transfer request acknowledgement is disabled.
142	289	DEOP0	C	[DEOP0] Completion output for DMA external transfer. The pin has this function when outputting DMA transfer completion is enabled.
		DSTP0		[DSTP0] Stop input for DMA external transfer. The pin has this function when the stop input is enabled for DMA transfer.
		PB2		[PB2] General purpose input/output port. The pin has this function when completion output and stop input are disabled for DMA transfer.
143	290	DREQ1	C	[DREQ1] DMA External input for DMA transfer requests. This input is used continuously when selected as a DMA activation trigger. In this case, do not output to this port unless doing so intentionally.
		PB3		[PB3] General purpose input/output port.
144	292	DACK1	C	[DACK1] External acknowledge output for DMA transfer requests. The pin has this function when outputting DMA transfer request acknowledgement is enabled.
		PB4		[PB4] General purpose input/output port. The pin has this function when outputting DMA transfer request acknowledgement is disabled.
145	293	DEOP1	C	[DEOP1] Completion output for DMA external transfer. The pin has this function when outputting DMA transfer completion is enabled.
		DSTP1		[DSTP1] Stop input for DMA external transfer. The pin has this function when the stop input is enabled for DMA transfer.
		PB5		[PB5] General purpose input/output port. The pin has this function when completion output and stop input are disabled for DMA transfer.
146	295	$\overline{\text{IOWR}}$	C	[$\overline{\text{IOWR}}$] Write strobe output for DMA fly-by transfer. The pin has this function when outputting a write strobe for DMA fly-by transfer is enabled.
		PB6		[PB6] General purpose input/output port. The pin has this function when outputting a write strobe for DMA fly-by transfer is disabled.

* : Shaded pins are only present on the MB91V340.

(Continued)

Pin no.		Pin name	I/O circuit type	Function
MB91340	MB91V340			
147	296	$\overline{\text{IORD}}$	C	[$\overline{\text{IORD}}$] Read strobe output for DMA fly-by transfer. The pin has this function when outputting a read strobe for DMA fly-by transfer is enabled.
		PB7		[PB7] General purpose input/output port. The pin has this function when outputting a read strobe for DMA fly-by transfer is disabled.
149	297	$\overline{\text{CS0}}$	C	[$\overline{\text{CS0}}$] Chip select 0 output. The pin has this function when chip select 0 output is enabled.
		PA0		[PA0] General purpose input/output port. The pin has this function when chip select 0 output is disabled.
150	298	$\overline{\text{CS1}}$	C	[$\overline{\text{CS1}}$] Chip select 1 output. The pin has this function when chip select 1 output is enabled.
		PA1		[PA1] General purpose input/output port. The pin has this function when chip select 1 output is disabled.
151	299	$\overline{\text{CS2}}$	C	[$\overline{\text{CS2}}$] Chip select 2 output. The pin has this function when chip select 2 output is enabled.
		PA2		[PA2] General purpose input/output port. The pin has this function when chip select 2 output is disabled.
152	300	$\overline{\text{CS3}}$	C	[$\overline{\text{CS3}}$] Chip select 3 output. The pin has this function when chip select 3 output is enabled.
		PA3		[PA3] General purpose input/output port. The pin has this function when chip select 3 output is disabled.
153	301	$\overline{\text{CS4}}$	C	[$\overline{\text{CS4}}$] Chip select 4 output. The pin has this function when chip select 4 output is enabled.
		PA4		[PA4] General purpose input/output port. The pin has this function when chip select 4 output is disabled.
154	303	$\overline{\text{CS5}}$	C	[$\overline{\text{CS5}}$] Chip select 5 output. The pin has this function when chip select 5 output is enabled.
		PA5		[PA5] General purpose input/output port. The pin has this function when chip select 5 output is disabled.
155	304	$\overline{\text{CS6}}$	C	[$\overline{\text{CS6}}$] Chip select 6 output. The pin has this function when chip select 6 output is enabled.
		PA6		[PA6] General purpose input/output port. The pin has this function when chip select 6 output is disabled.
156	305	$\overline{\text{CS7}}$	C	[$\overline{\text{CS7}}$] Chip select 7 output. The pin has this function when chip select 7 output is enabled.
		PA7		[PA7] General purpose input/output port. The pin has this function when chip select 7 output is disabled.
159	306	$\overline{\text{NMI}}$	G	NMI (Non Maskable Interrupt) input
160	307	$\overline{\text{HST}}$	G	Hardware standby input

* : Shaded pins are only present on the MB91V340.

(Continued)

Pin no.		Pin name	I/O circuit type	Function	
MB91340	MB91V340				
161	308	$\overline{\text{INIT}}$	B	External reset input (Reset to initialize settings)	
—	270	$\overline{\text{RST}}$	B	External reset input (Reset to initialize operation)	*
162	313	RDY	C	[RDY] External ready input. The pin has this function when external ready input is enabled.	
		P80		[P80] General purpose input/output port. The pin has this function when external ready input is disabled.	
163	314	$\overline{\text{BGRNT}}$	C	[$\overline{\text{BGRNT}}$] Acknowledge output for external bus release. Outputs "L" when the external bus is released. The pin has this function when output is enabled.	
		P81		[P81] General purpose input/output port. The pin has this function when output is disabled for external bus release acknowledge.	
164	315	BRQ	C	[BRQ] External bus release request input. Input "1" to request release of the external bus. The pin has this function when input is enabled.	
		P82		[P82] General purpose input/output port. The pin has this function when the external bus release request input is disabled.	
—	310	$\overline{\text{EX\_BGRNT}}$	J	Acknowledge output for external bus release. Outputs "L" when the external bus is released.	*
—	311	EX_BRQ	K	External bus release request input. Input "1" to request release of the external bus. The pin has this function when input is enabled.	*
165	316	$\overline{\text{RD}}$	C	[$\overline{\text{RD}}$] External bus read strobe output.	
166	317	$\overline{\text{WR0}}$/$\overline{\text{UUB}}$	C	[$\overline{\text{WR0}}$] External bus write strobe output. When $\overline{\text{WR}}$ is used as the write strobe, this becomes the byte-enable pin ($\overline{\text{UUB}}$).	
167	318	$\overline{\text{WR1}}$/$\overline{\text{ULB}}$	C	[$\overline{\text{WR1}}$] External bus write strobe output. The pin has this function when $\overline{\text{WR1}}$ output is enabled. When $\overline{\text{WR}}$ is used as the write strobe, this becomes the byte-enable pin ($\overline{\text{ULB}}$).	
		P85		[P85] General purpose input/output port. The pin has this function when the external bus write-enable output is disabled.	
—	319	$\overline{\text{WR2}}$/$\overline{\text{LUB}}$	C	[$\overline{\text{WR2}}$] External bus write strobe output. The pin has this function when $\overline{\text{WR2}}$ output is enabled. When $\overline{\text{WR}}$ is used as the write strobe, this becomes the byte-enable pin ($\overline{\text{LUB}}$).	*
		P86		[P86] General purpose input/output port. The pin has this function when the external bus write-enable output is disabled.	*
—	320	$\overline{\text{WR3}}$/$\overline{\text{LLB}}$	C	[$\overline{\text{WR3}}$] External bus write strobe output. The pin has this function when $\overline{\text{WR3}}$ output is enabled. When $\overline{\text{WR}}$ is used as the write strobe, this becomes the byte-enable pin ($\overline{\text{LLB}}$).	*
		P87		[P87] General purpose input/output port. The pin has this function when the external bus write-enable output is disabled.	*

* : Shaded pins are only present on the MB91V340.

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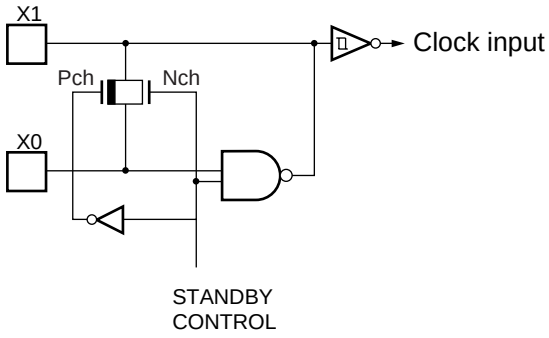
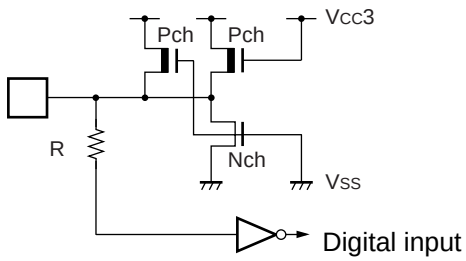
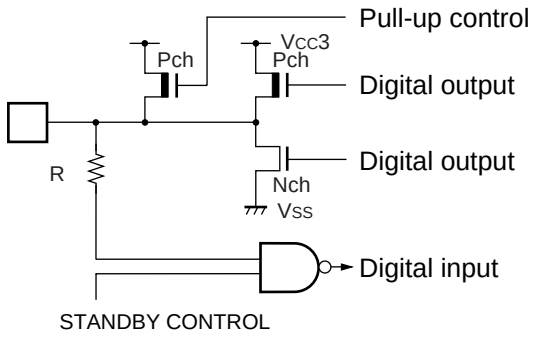
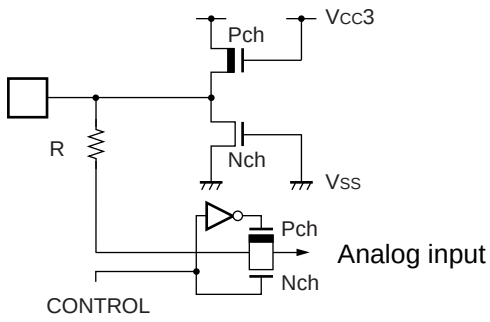
Pin no.		Pin name	I/O circuit type	Function
MB91340	MB91V340			
169	321	SYSCLK	C	[SYSCLK] System clock output. The pin has this function when system clock output is enabled. This outputs the same clock as the external bus operating frequency. (Output halts in stop mode.)
		P90		[P90] General purpose input/output port. The pin has this function when system clock output is disabled.
170	323	P91	C	[P91] General purpose input/output port.
171	325	MCLK	C	[MCLK] Memory clock output. The pin has this function when memory clock output is enabled. This outputs the same clock as the external bus operating frequency. (Output halts in sleep mode.)
		P92		[P92] General purpose input/output port. The pin has this function when memory clock output is disabled.
172	326	P93	C	[P93] General purpose input/output port.
173	327	$\overline{AS}$	C	[$\overline{AS}$] Address strobe output. The pin has this function when address strobe output is enabled.
		$\overline{LBA}$		[$\overline{LBA}$] Address strobe output for burst flash ROM. The pin has this function when address strobe output is enabled.
		P94		[P94] General purpose input/output port. The pin has this function when address strobe output is disabled.
174	328	$\overline{BAA}$	C	[$\overline{BAA}$] Address advance output for burst Flash ROM. The pin has this function when address advance output is enabled.
		P95		[P95] General purpose input/output port. The pin has this function when address advance output is disabled.
175	329	P96	C	[P96] General purpose input/output port.
176	330	$\overline{WR}$	C	[$\overline{WR}$] Memory write strobe output. The pin has this function when write strobe output is enabled.
		P97		[P97] General purpose input/output port. The pin has this function when write strobe output is disabled.

* : Shaded pins are only present on the MB91V340.

[Power supply and GND pins]

Pin no.		Pin name	Function
MB91340	**MB91V340**		
17, 36, 61, 80, 100, 131, 133, 148, 168	4, 23, 33, 44, 54, 64, 74, 83, 90, 99, 109, 119, 130, 140, 150, 160, 169, 176, 185, 195, 205, 216, 226, 236, 246, 255, 262, 271, 281, 291, 302, 312, 322, 332, 341	V_{SS}	GND pins. Connect all pins at the same potential.
27, 71, 110, 132, 158	7, 36, 66, 93, 122, 179, 208, 238, 265, 275, 284, 294, 324	$V_{CC}2$	2V power supply pins. Connect all pins at the same potential.
26, 70, 109, 136, 157	21, 80, 107, 137, 166, 193, 223, 252, 279, 309, 338	$V_{CC}3$	3V power supply pins. Connect all pins at the same potential.
45	57	DAVS	GND pin for D/A converter
46	58	DAVC	Power supply pin for D/A converter
58	72	AV_{CC}	Analog power supply pin for A/D converter
59	73	AVRH	Reference power supply pin for A/D converter
60	75	AV_{SS}/AVRL	Analog GND pin for A/D converter
—	276, 277, 278, 345 to 361	OPEN	Open pins. Leave these pins open circuit.

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		• Oscillation feedback resistance approx. 1 MΩ
B		• CMOS level input with pull-up resistor Pull-up resistor = 25 KΩ approx. (Typ)
C		• CMOS level I/O with pull-up control with standby control Pull-up resistor = 25KΩ approx. (Typ) * : In I²C standard mode, the P-type digital output is disabled and the pin becomes an open drain output.
D		• Analog input With switch

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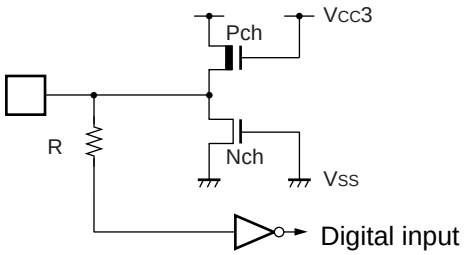
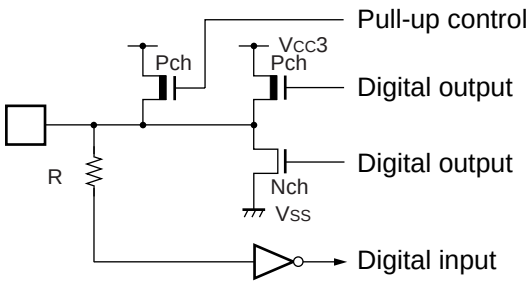
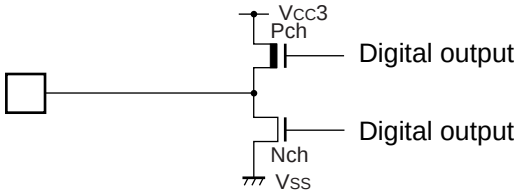
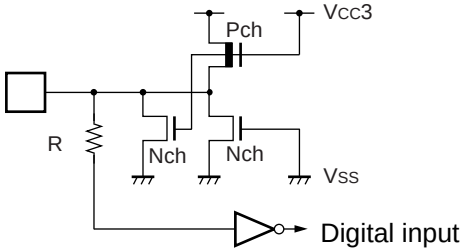
Type	Circuit	Remarks
G		• CMOS level input No standby control
I		• CMOS level I/O with pull-up control No standby control Pull-up resistor = 25 KΩ approx. (Typ)
J		• CMOS level output
K		• CMOS level input with pull-down Pull-down resistor = 25 KΩ approx. (Typ)

■ HANDLING DEVICES

• Preventing Latchup

When CMOS integrated circuit devices are subjected to applied voltages higher than $V_{CC}3$ at input and output pins, or to voltages lower than V_{SS}, as well as when voltages in excess of rated levels are applied between $V_{CC}3$, $V_{CC}2$ and V_{SS}, a phenomenon known as latchup can occur. When a latchup condition occurs, the supply current can increase dramatically and may destroy semiconductor elements. In using semiconductor devices, always take sufficient care to avoid exceeding maximum ratings.

• Treatment of unused input pins

If unused input pins are left open, abnormal operation may result. Any unused input pins should be connected to pull-up or pull-down resistors.

• Power supply pins

Devices with multiple $V_{CC}3$, $V_{CC}2$ and V_{SS} supply pins are designed to prevent problems such as latchup occurring by providing internal connections between pins at the same potential. However, in order to reduce unwanted radiation, prevent abnormal operation of strobe signals due to a rise in ground level, and to maintain the total output current ratings, all such pins should always be connected externally to power supply or ground. Also, ensure that the impedance of the $V_{CC}3$, $V_{CC}2$ and V_{SS} connections to the power supply are as low as possible.
In addition, it is recommended that a bypass capacitor of approximately 0.1µF be connected between V_{CC} and V_{SS}. Connect the capacitor close to the V_{CC} and V_{SS} pins.

• Crystal oscillators

Noise in proximity to the X0 and X1 pins can cause abnormal operation in this device. Printed circuit boards should be designed so that the X0 and X1 pins, crystal (or ceramic) oscillator, and bypass capacitor connected to ground are placed as close together as possible.
Also, to ensure stable operation, it is strongly recommended that the printed circuit board art work be designed such that the X0 and X1 pins are surrounded by ground.

• Treatment of NC and OPEN pins

Pins marked as "NC" or "OPEN" must be left open-circuit.

• Mode pins (MD0 to MD2)

These pins should be connected directly to $V_{CC}3$ or V_{SS}. To prevent the device erroneously switching to test mode due to noise, design the printed circuit board such that the distance between the mode pins and $V_{CC}3$ or V_{SS} is as short as possible and the connection impedance is low.

• Operation at startup

Always apply a settings initialization (INIT) to the $\overline{\text{INIT}}$ pin immediately after turning on the power.
Also, in order to provide a delay while the oscillator circuits stabilize immediately after startup, maintain the "L" level input to the INIT pin for the required stabilization delay time. (The initialization processing (INIT) triggered by the $\overline{\text{INIT}}$ pin initializes the oscillation stabilization delay time to the minimum setting.)

• Source oscillation input at startup

At power-on startup, always input a clock signal until the oscillation stabilization delay time is ended.

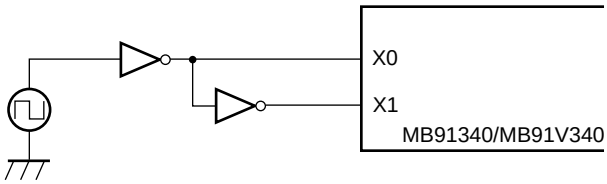
- **Hardware standby at power-on startup**

  If a hardware standby request occurs immediately after turning on the power, the settings initialization reset (INIT) triggered by the $\overline{\text{INIT}}$ pin has priority. However, the device goes to the hardware standby state after the settings initialization reset (INIT) triggered by the $\overline{\text{INIT}}$ pin completes. At this time, the oscillation stabilization delay time is initialized to the maximum value and accordingly, this time is used for the oscillation stabilization delay that occurs after hardware standby is released.

- **Remarks for External Clock Operation**

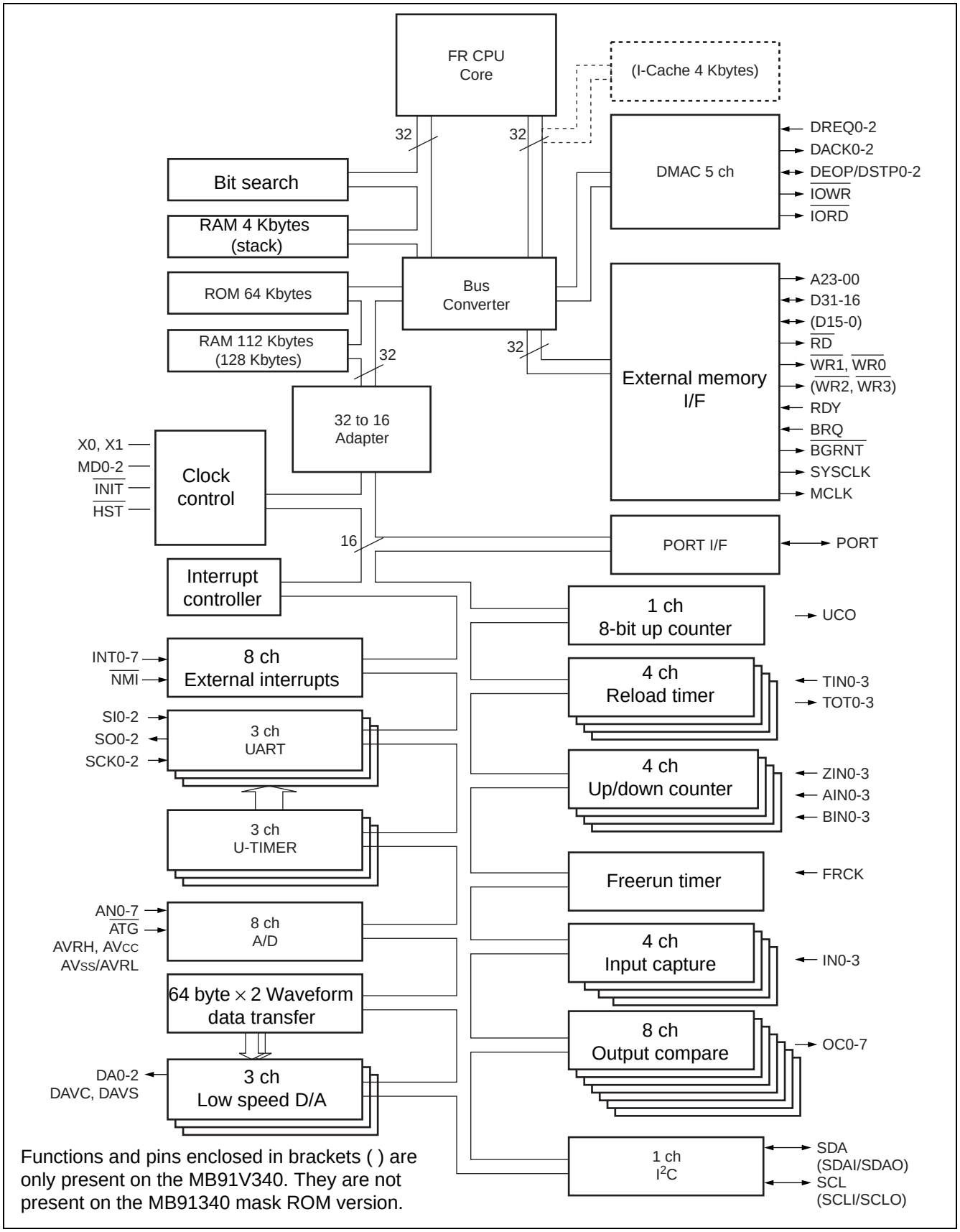
  When external clock is selected, supply it to X0 pin generally, and simultaneously the opposite phase clock to X0 must be supplied to X1 pin. However, in this case the stop mode must not be used (because X1 pin stops at “H” output in stop mode) .

● Using an external clock (normal)



Note: Stop mode (oscillation stop mode) can not be used.

■ BLOCK DIAGRAM



Functions and pins enclosed in brackets ( ) are only present on the MB91V340. They are not present on the MB91340 mask ROM version.

■ CPU

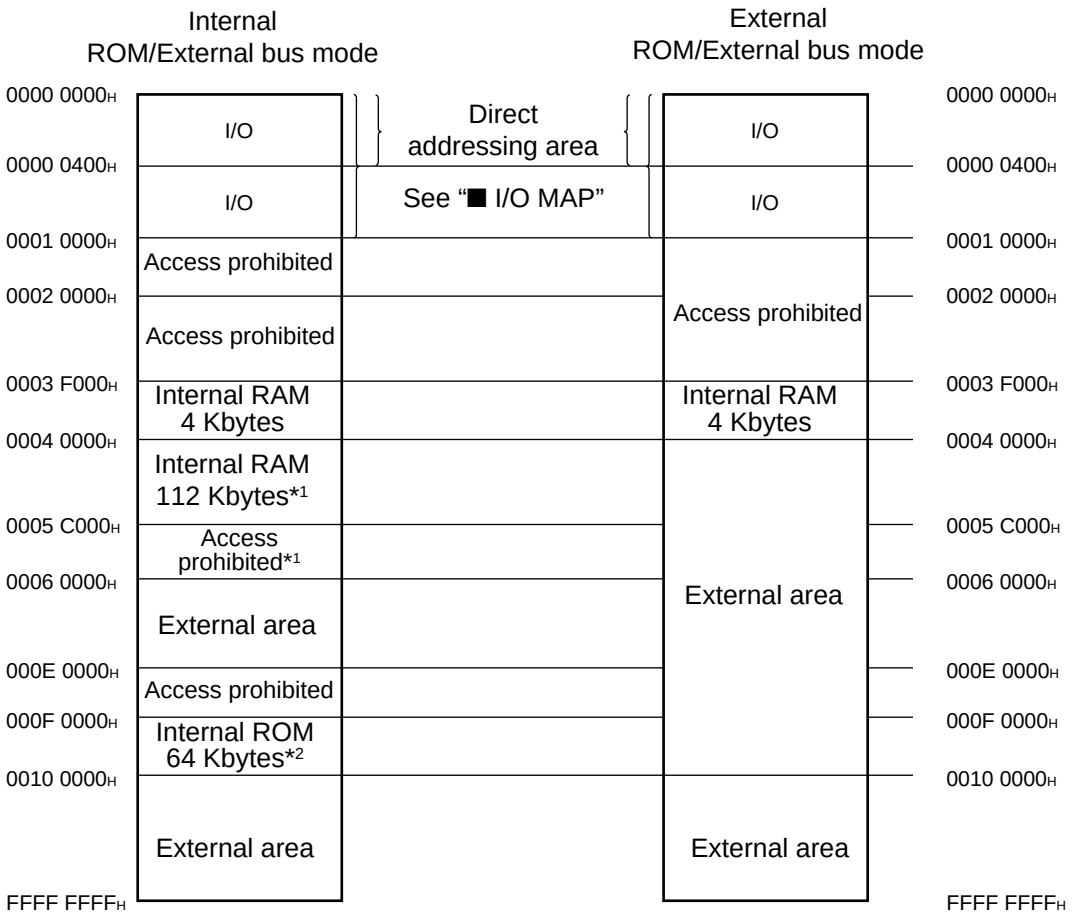
1. Memory Space

The FR series has a 4Gbytes (2^{32} bytes) logical address space and the CPU performs linear access.

• Memory map

The figure below shows the memory map for this device.

The various mode settings are determined by the mode vector fetch performed after $\overline{\text{INIT}}$ is negated.
(See "■ MODE SETTINGS" for details of the mode settings.)



*1 : On the MB91V340, the prohibited access area and 112Kbytes RAM area are combined into a 128Kbytes RAM area.

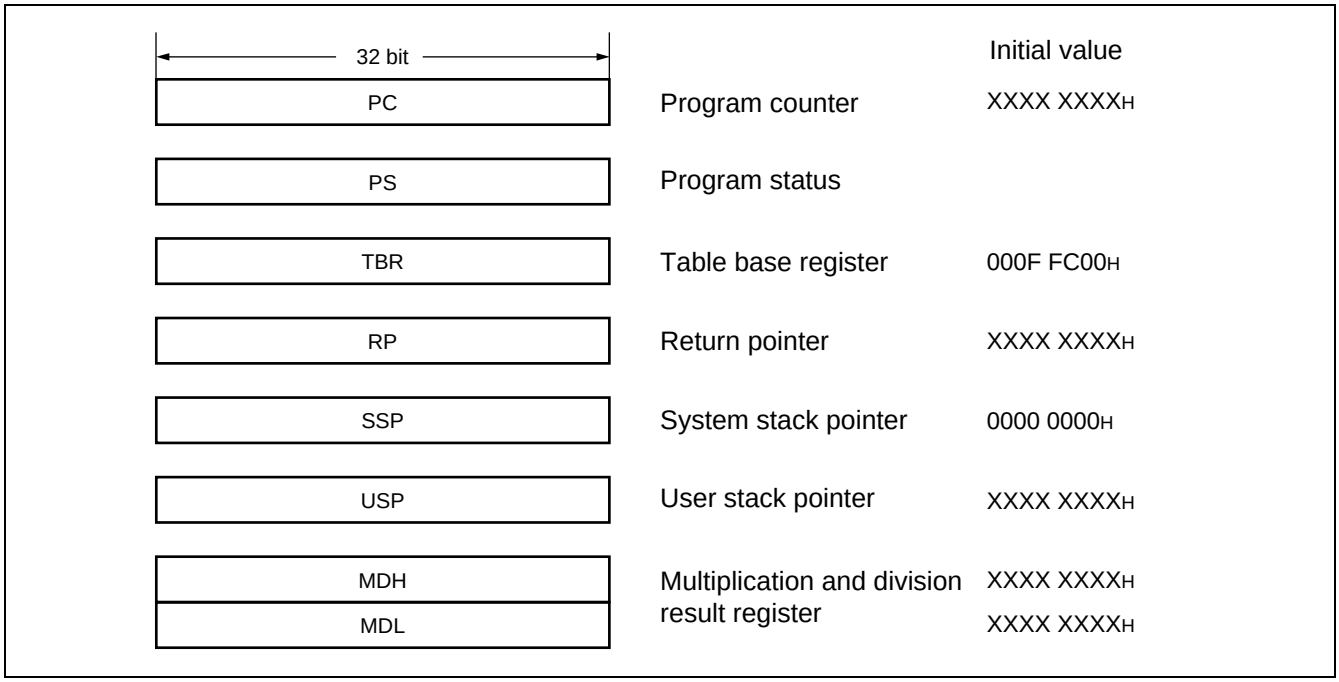
*2 : On the MB91V340, the 64Kbytes ROM area contains emulation RAM.

2. Registers

The FR series has two types of registers: application-specific registers in the CPU and general purpose registers in memory.

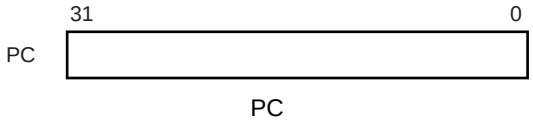
- Dedicated registers

Program counter (PC)	:	32-bit register. Stores the current instruction address.
Program status (PS)	:	32-bit register. Contains the register pointer and condition code.
Table base register (TBR)	:	Stores the top address of the vector table used by the EIT (exception/interrupt/ trap) function.
Return pointer (RP)	:	Stores the subroutine return address.
System stack pointer (SSP)	:	Points to the system stack area.
User stack pointer (USP)	:	Points to the user stack area.
Multiplication and division result register (MDH/MDL)	:	32-bit registers used for multiplication and division.



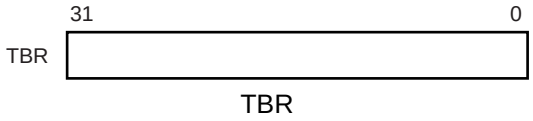
- PC (Program Counter)

The PC is the program counter and stores the address of the currently executing instruction.



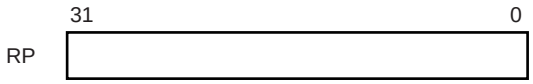
- Table base register (TBR)

The TBR is the table base register and stores the top address of the vector table used by the EIT function.



- Return pointer (RP)

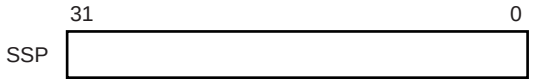
  The RP is the return pointer and stores the subroutine return address.



RP

- System stack pointer (SSP)

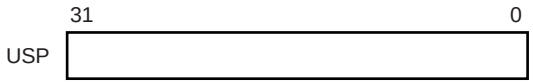
  The SSP is the system stack pointer and functions as R15 when the S flag is “0”.



SSP

- User stack pointer (USP)

  The USP is the user stack pointer and functions as R15 when the S flag is “1”.



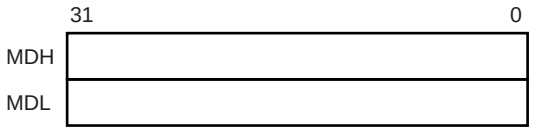
USP

- Multiplication and division result register (MDH/MDL)

  MDH/MDL : 32-bit registers used for multiplication and division.

  MDH : Remainder

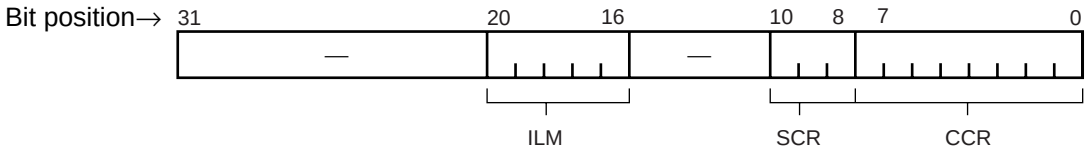
  MDL : Quotient



Multiplication and division result register

• Program status (PS)

This register holds the program status and is divided into the ILM, SCR, and CCR.



PS

• Condition code register (CCR)

S flag : Specifies which stack pointer to use as R15.

I flag : Enables or disables user interrupt requests.

N flag : Indicates the sign when an operation result is represented as a 2's complement integer.

Z flag : Indicates whether an operation result is zero.

V flag : Indicates whether an overflow occurred for an operation result when the operation operand is represented as a 2's complement integer.

C flag : Indicates whether an operation resulted in a borrow or a carry from the most significant bit.

7	6	5	4	3	2	1	0	Initial Value
—	—	S	I	N	Z	V	C	- - 00XXXX$_B$

CCR

• System condition code register (SCR)

D1, D0 flags : Stores intermediate data for stepwise multiplication operations.

T flags : A flag specifying whether the step trace trap function is enabled or not.

10	9	8	Initial Value
D1	D0	T	XX0$_B$

SCR

• Interrupt level mask register(ILM)

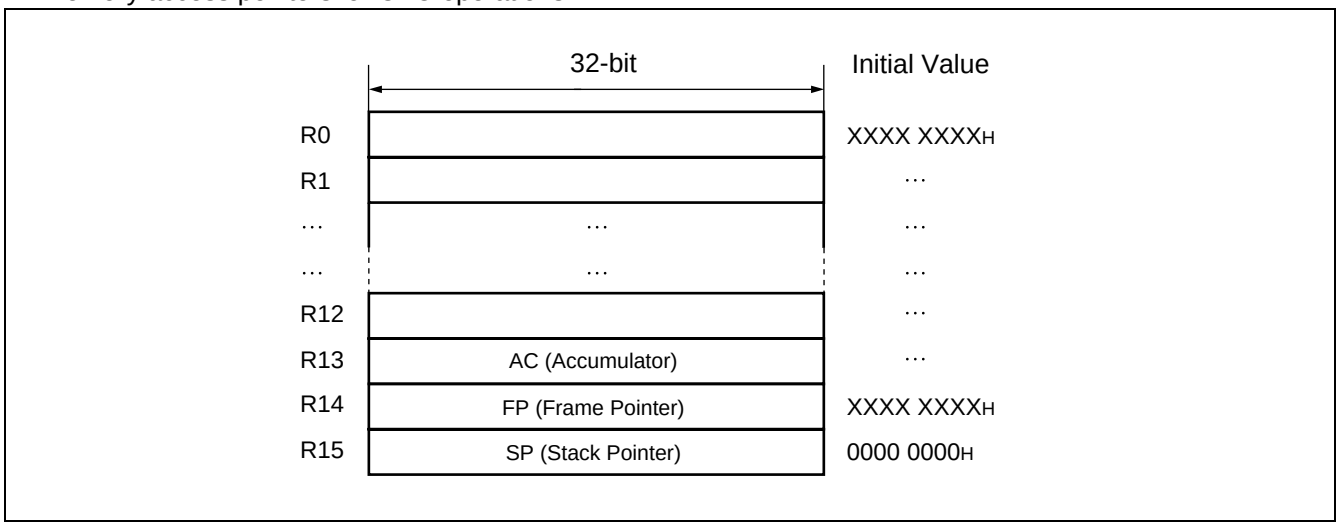
ILM4 to ILM0 : his register stores the interrupt level mask value. The value in the ILM register is used as the level mask. Only interrupt requests to the CPU that have an interrupt level that is higher than the level specified in ILM are accepted.

20	19	18	17	16			Initial Value
ILM4	ILM3	ILM2	ILM1	ILM0	Interrupt Level		01111$_B$
0	0	0	0	0	0	High	
		• • •			• • •	↑	
0	1	0	0	0	15	(Medium)	
		• • •			• • •	↓	
1	1	1	1	1	31	Low	

ILM

■ GENERAL PURPOSE REGISTERS

General purpose registers R0 to R15 are used by the CPU. The registers are used as the accumulator and memory access pointers for CPU operations.



The following three registers are treated as having special meanings to enhance the operation of some instructions.

R13 : Virtual accumulator (AC)

R14 : Frame pointer (FP)

R15 : Stack pointer (SP)

The values of R0 to R14 after a reset are undefined. R15 is initialized to 0000 0000H (SSP value) .

■ MODE SETTINGS

In the FR series, the mode is set by the mode pins (MD2, 1, 0) and mode register (MODR).

1. Pins

The MD2, MD1, and MD0 pins specify how the mode vector fetch is performed.

Mode Pins			Mode name	Reset vector access area	Remarks
MD2	MD1	MD0			
0	0	0	Internal ROM vector mode	Internal	
0	0	1	External ROM vector mode	External	The bus width is specified by the mode register.

Values other than those listed in the table are prohibited.

2. Register

• Mode register (MODR) and setting mode

The data written to the mode register by the mode vector fetch operation is called the mode data.

After the data is set to the mode register (MODR), the device operates with the operating mode specified by this data.

The mode register is set by all types of reset. The register cannot be written to by user programs.

Note: The address used by the mode register (0000 07FF$_H$) was unused by previous FR series devices.

The register can be modified in emulator mode. In this case, use an 8-bit data transfer instruction. No data is written by 16 or 32-bit transfer instructions.

<Register details>

MODR	7	6	5	4	3	2	1	0	Initial Value	Access
	0	0	0	0	0	ROMA	WTH1	WTH0	XXXXXXXX$_B$	W

Operation mode setting bits

W : Write-only
X : Undefined

bit 7 to 3 : Always set “00000$_B$”.

ROMA : Specifies whether the internal Fbus RAM and Fbus ROM areas are enabled.

ROMA	Function	Remarks
0	External ROM mode	The internal Fbus area (4 0000$_H$ to 10 0000$_H$) becomes an external area.
1	Internal ROM mode	The internal 112Kbytes of Fbus RAM (128Kbytes on the MB91V340) and 64Kbytes Fbus ROM are enabled.

WTH1, WTH0 (Bus width setting bits) :

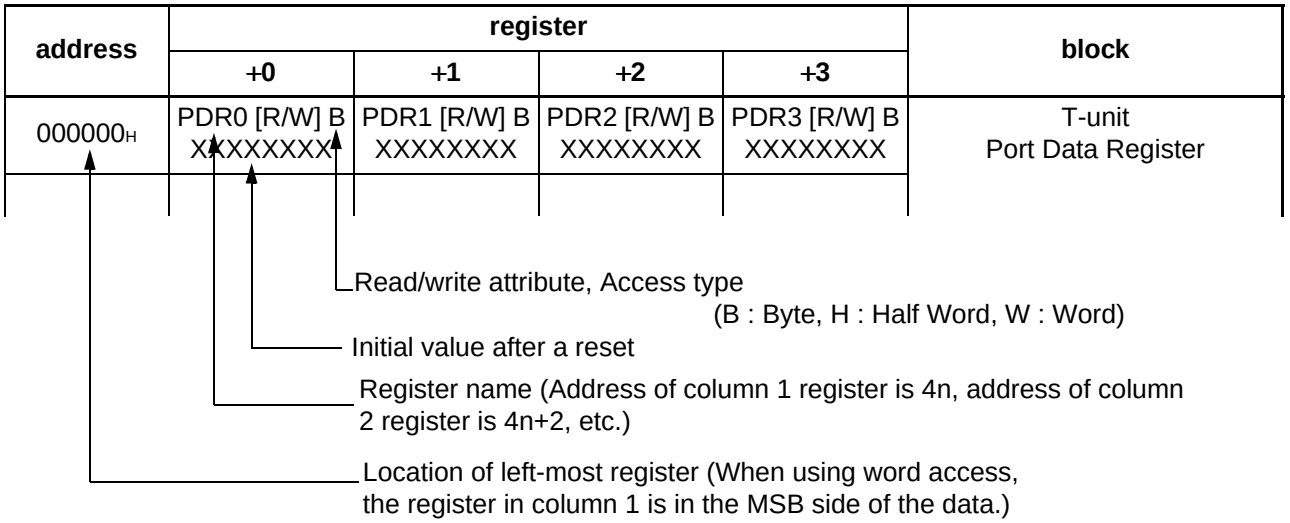
This sets the bus width in external bus mode. In external bus mode, the values of bits DBW1 and DBW0 in ACR0 (CS0 area) are set in these bits.

WTH1	WTH0	Function	Remarks
0	0	8-bit bus width	External bus mode
0	1	16-bit bus width	External bus mode
1	0	32-bit bus width	External bus mode (only available on the MB91V340)
1	1	Single chip mode	Prohibited setting on this device.

■ I/O MAP

This shows the location of the various peripheral resource registers in the memory space.

[How to read the table]



Note : Initial values of register bits are represented as follows :

"1" : Initial value"1"
"0" : Initial value"0"
"X" : Initial value"X"
"-" : No physical register at this location

address	register				block
	+0	+1	+2	+3	
000000H	PDR0 [R/W] B*1 XXXXXXXX	PDR1 [R/W] B*1 XXXXXXXX	PDR2 [R/W] B XXXXXXXX	—	T-unit Port Data Register
000004H	—	—	PDR6 [R/W] B XXXXXXXX	—	
000008H	PDR8 [R/W] B*2 --XXXXXX	PDR9 [R/W] B XXXXXXX-	PDRA [R/W] B XXXXXXXX	PDRB [R/W] B XXXXXXXX	
00000CH	PDRC [R/W] B -----XXX	—			
000010H	—	PDRH [R/W] B -----XXX	PDRI [R/W] B --XXXXXX	PDRJ [R/W] B XXXXXXXX	R-bus Port Data Register
000014H	PDRK [R/W] B XXXXXXXX	PDRL [R/W] B -XXXXXXX	PDRM [R/W] B ----XXXX	PDRN [R/W] B XXXXXXXX	
000018H	PDRO [R/W] B XXXXXXXX	PDRP [R/W] B XXXXXXXX	—	—	
00001CH	—				

(Continued)

address	register				block
	+0	+1	+2	+3	
000020H to 00003CH	—				Reserved
000040H	EIRR [R/W] B, H, W 00000000	ENIR [R/W] B, H, W 00000000	ELVR [R/W] B, H, W 00000000		Ext int
000044H	DICR [R/W] B, H, W -------0	HRCL [R/W] B, H, W 0--11111	—		DLYI/I-unit
000048H	TMRLR0 [W] H, W XXXXXXXX XXXXXXXX		TMR0 [R] H, W XXXXXXXX XXXXXXXX		Reload Timer 0
00004CH	—		TMCSR0 [R/W] B, H, W ----0000 00000000		
000050H	TMRLR1 [W] H, W XXXXXXXX XXXXXXXX		TMR1 [R] H, W XXXXXXXX XXXXXXXX		Reload Timer 1
000054H	—		TMCSR1 [R/W] B, H, W ----0000 00000000		
000058H	TMRLR2 [W] H, W XXXXXXXX XXXXXXXX		TMR2 [R] H, W XXXXXXXX XXXXXXXX		Reload Timer 2
00005CH	—		TMCSR2 [R/W] B, H, W ----0000 00000000		
000060H	SSR0 [R/W] B, H, W 00001000	SIDR0 [R/W] B, H, W XXXXXXXX	SCR0 [R/W] B, H, W 00000100	SMR0 [R/W] B, H, W 00--0-0-	UART0
000064H	UTIM0 [R] H (UTIMR0 [W] H) 00000000 00000000		DRCL0 [W] B --------	UTIMC0 [R/W] B 0--00001	U-TIMER 0
000068H	SSR1 [R/W] B, H, W 00001000	SIDR1 [R/W] B, H, W XXXXXXXX	SCR1 [R/W] B, H, W 00000100	SMR1 [R/W] B, H, W 00--0-0-	UART1
00006CH	UTIM1 [R] H (UTIMR1 [W] H) 00000000 00000000		DRCL1 [W] B --------	UTIMC1 [R/W] B 0--00001	U-TIMER 1
000070H	SSR2 [R/W] B, H, W 00001000	SIDR2 [R/W] B, H, W XXXXXXXX	SCR2 [R/W] B, H, W 00000100	SMR2 [R/W] B, H, W 00--0-0-	UART2
000074H	UTIM2 [R] H (UTIMR2 [W] H) 00000000 00000000		DRCL2 [W] B --------	UTIMC2 [R/W] B 0--00001	U-TIMER 2
000078H	ADCR [R] B, H, W 000000XX XXXXXXXX		ADCS [R/W] B, H, W 00000000 00000000		A/D Converter Sequential Compara-tor
00007CH	ADCR0 [R] B, H, W XXXXXXXX	ADCR1 [R] B, H, W XXXXXXXX	ADCR2 [R] B, H, W XXXXXXXX	ADCR3 [R] B, H, W XXXXXXXX	
000080H	ADCR4 [R] B, H, W XXXXXXXX	ADCR5 [R] B, H, W XXXXXXXX	ADCR6 [R] B, H, W XXXXXXXX	ADCR7 [R] B, H, W XXXXXXXX	
000084H	—	DACR2 [R/W] B, H, W -------0	DACR1 [R/W] B, H, W -------0	DACR0 [R/W] B, H, W -------0	D/A Converter
000088H	—	DADR2 [R/W] B, H, W XXXXXXXX	DADR1 [R/W] B, H, W XXXXXXXX	DADR0 [R/W] B, H, W XXXXXXXX	

(Continued)

address	register				block
	+0	+1	+2	+3	
00008C$_H$	WCR [R/W] B, H, W 00111111	APR [R/W] B, H, W -0000000	WDR1 [R/W] B, H, W XXXXXXXX	WDR0 [R/W] B, H, W XXXXXXXX	D/A DATA Transmitter
000090$_H$	—	—	—	VERR [R] B, H, W ----XXXX	Version Register
000094$_H$	IBCR [R/W] B, H, W 00000000	IBSR [R] B, H, W 00000000	ITBA [R/W] B, H, W ------00 00000000		I^2C interface
000098$_H$	ITMK [R/W] B, H, W 00----11 11111111		ISMK [R/W] B, H, W 01111111	ISBA [R/W] B, H, W -0000000	
00009C$_H$	—	IDAR [R/W] B, H, W 00000000	ICCR [R/W] B, H, W 0-011111	IDBL [R/W] B, H, W -------0	
0000A0$_H$	—	—	—	—	Reserved
0000A4$_H$	—	—	—	—	
0000A8$_H$	TMRLR3 [W] H, W XXXXXXXX XXXXXXXX		TMR3 [R] H, W XXXXXXXX XXXXXXXX		Reload Timer 3
0000AC$_H$	—		TMCSR3 [R/W] B, H, W ----0000 00000000		
0000B0$_H$	RCR1 [W] B, H, W 00000000	RCR0 [W] B, H, W 00000000	UDCR1 [R] B, H, W 00000000	UDCR0 [R] B, H, W 00000000	8/16 Bit U/D Counter0, 1
0000B4$_H$	CCRH0 [R/W] B, H, W 00001000	CCRL0 [R/W] B, H, W 00001000	—	CSR0 [R/W] B, H, W 00000000	
0000B8$_H$	CCRH1 [R/W] B, H, W 00001000	CCRL1 [R/W] B, H, W 00001000	—	CSR1 [R/W] B, H, W 00000000	
0000BC$_H$	RCR3 [W] B, H, W 00000000	RCR2 [W] B, H, W 00000000	UDCR3 [R] B, H, W 00000000	UDCR2 [R] B, H, W 00000000	8/16 Bit U/D Counter2, 3
0000C0$_H$	CCRH2 [R/W] B, H, W 00001000	CCRL2 [R/W] B, H, W 00001000	—	CSR2 [R/W] B, H, W 00000000	
0000C4$_H$	CCRH3 [R/W] B, H, W 00001000	CCRL3 [R/W] B, H, W 00001000	—	CSR3 [R/W] B, H, W 00000000	
0000C8$_H$	—	—	—	—	Reserved
0000CC$_H$	—	—	—	—	
0000D0$_H$	CCR [R/W] B, H, W 00001000	COMPR [R/W] B, H, W 00001000	CSR [R/W] B, H, W 00000000	UCR [R/W] B, H, W 00000000	8 Bit UP Counter
0000D4$_H$	TCDT [R/W] H, W 00000000 00000000		—	TCCS [R/W] B, H, W 00000000	16 bit Free run Timer
0000D8$_H$	IPCP1 [R] H, W XXXXXXXX XXXXXXXX		IPCP0 [R] H, W XXXXXXXX XXXXXXXX		16 bit ICU
0000DC$_H$	IPCP3 [R] H, W XXXXXXXX XXXXXXXX		IPCP2 [R] H, W XXXXXXXX XXXXXXXX		
0000E0$_H$	—	ICS23 [R/W] B, H, W 00000000	—	ICS01 [R/W] B, H, W 00000000	

(Continued)

address	register				block
	+0	+1	+2	+3	
0000E4H	OCCP1 [R/W] H, W XXXXXXXX XXXXXXXX		OCCP0 [R/W] H, W XXXXXXXX XXXXXXXX		16 bit OCU
0000E8H	OCCP3 [R/W] H, W XXXXXXXX XXXXXXXX		OCCP2 [R/W] H, W XXXXXXXX XXXXXXXX		
0000ECH	OCCP5 [R/W] H, W XXXXXXXX XXXXXXXX		OCCP4 [R/W] H, W XXXXXXXX XXXXXXXX		
0000F0H	OCCP7 [R/W] H, W XXXXXXXX XXXXXXXX		OCCP6 [R/W] H, W XXXXXXXX XXXXXXXX		
0000F4H	OCS23 [R/W] B, H, W 1110110 00001100		OCS01 [R/W] B, H, W 1110110 00001100		
0000F8H	OCS67 [R/W] B, H, W 1110110 00001100		OCS45 [R/W] B, H, W 1110110 00001100		
0000FCH to 0001FCH	—				Reserved
000200H	DMACA0 [R/W] B, H, W*3 00000000 0000XXXX XXXXXXXX XXXXXXXX				DMAC
000204H	DMACB0 [R/W] B, H, W 00000000 00000000 XXXXXXXX XXXXXXXX				
000208H	DMACA1 [R/W] B, H, W*3 00000000 0000XXXX XXXXXXXX XXXXXXXX				
00020CH	DMACB1 [R/W] B, H, W 00000000 00000000 XXXXXXXX XXXXXXXX				
000210H	DMACA2 [R/W] B, H, W*3 00000000 0000XXXX XXXXXXXX XXXXXXXX				
000214H	DMACB2 [R/W] B, H, W 00000000 00000000 XXXXXXXX XXXXXXXX				
000218H	DMACA3 [R/W] B, H, W*3 00000000 0000XXXX XXXXXXXX XXXXXXXX				
00021CH	DMACB3 [R/W] B, H, W 00000000 00000000 XXXXXXXX XXXXXXXX				
000220H	DMACA4 [R/W] B, H, W*3 00000000 0000XXXX XXXXXXXX XXXXXXXX				
000224H	DMACB4 [R/W] B, H, W 00000000 00000000 XXXXXXXX XXXXXXXX				
000228H	—				
00022CH to 00023CH	—				Reserved
000240H	DMACR [R/W] B 0XX00000 XXXXXXXX XXXXXXXX XXXXXXXX				DMAC

(Continued)

address	register				block
	+0	+1	+2	+3	
000244H to 000300H	—				Reserved
000304H	—	—	—	ISIZE [R/W] B, H, W ------11	I-Cache (MB91V340 only)
000308H to 0003E0H	—	—	—	—	Reserved
0003E4H	—	—	—	ICHCR [R/W] B, H, W 0-000000	I-Cache (MB91V340 only)
0003E8H	—				Reserved
0003ECH					
0003F0H	BSD0 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Bit Search Module
0003F4H	BSD1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0003F8H	BSDC [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0003FCH	BSRR [R] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000400H	—	DDRH [R/W] B -----000	DDRI [R/W] B --000000	DDRJ [R/W] B 00000000	R-bus Data Direction Register
000404H	DDRK [R/W] B 00000000	DDRL [R/W] B -0000000	DDRM [R/W] B ----0000	DDRN [R/W] B 00000000	
000408H	DDRO [R/W] B 00000000	DDRP [R/W] B 00000000	—		
00040CH	—				
000410H	—	PFRH [R/W] B -----00-	PFRI [R/W] B --00-00-	—	R-bus Port Function Register
000414H	PFRK [R/W] B 0000----	PFRL [R/W] B 00---000	—	—	
000418H	PFRO [R/W] 00000000	—	—		
00041CH	—				Reserved
000420H	—	PCRH [R/W] B -----000	PCRI [R/W] B --000000	PCRJ [R/W] B 00000000	R-bus Pull-up Control Register

(Continued)

address	register				block
	+0	+1	+2	+3	
000424H	PCRK [R/W] B 00000000	PCRL [R/W] B -0000000	PCRM [R/W] B ----000	PCRN [R/W] B 00000000	R-bus Pull-up Control Register
000428H	PCRO [R/W] B 00000000	PCRP [R/W] B 00000000	—	—	
00042CH to 00043CH	—				Reserved
000440H	ICR00 [R/W] B, H, W ---11111	ICR01 [R/W] B, H, W ---11111	ICR02 [R/W] B, H, W ---11111	ICR03 [R/W] B, H, W ---11111	Interrupt Control unit
000444H	ICR04 [R/W] B, H, W ---11111	ICR05 [R/W] B, H, W ---11111	ICR06 [R/W] B, H, W ---11111	ICR07 [R/W] B, H, W ---11111	
000448H	ICR08 [R/W] B, H, W ---11111	ICR09 [R/W] B, H, W ---11111	ICR10 [R/W] B, H, W ---11111	ICR11 [R/W] B, H, W ---11111	
00044CH	ICR12 [R/W] B, H, W ---11111	ICR13 [R/W] B, H, W ---11111	ICR14 [R/W] B, H, W ---11111	ICR15 [R/W] B, H, W ---11111	
000450H	ICR16 [R/W] B, H, W ---11111	ICR17 [R/W] B, H, W ---11111	ICR18 [R/W] B, H, W ---11111	ICR19 [R/W] B, H, W ---11111	
000454H	ICR20 [R/W] B, H, W ---11111	ICR21 [R/W] B, H, W ---11111	ICR22 [R/W] B, H, W ---11111	ICR23 [R/W] B, H, W ---11111	
000458H	ICR24 [R/W] B, H, W ---11111	ICR25 [R/W] B, H, W ---11111	ICR26 [R/W] B, H, W ---11111	ICR27 [R/W] B, H, W ---11111	
00045CH	ICR28 [R/W] B, H, W ---11111	ICR29 [R/W] B, H, W ---11111	ICR30 [R/W] B, H, W ---11111	ICR31 [R/W] B, H, W ---11111	
000460H	ICR32 [R/W] B, H, W ---11111	ICR33 [R/W] B, H, W ---11111	ICR34 [R/W] B, H, W ---11111	ICR35 [R/W] B, H, W ---11111	
000464H	ICR36 [R/W] B, H, W ---11111	ICR37 [R/W] B, H, W ---11111	ICR38 [R/W] B, H, W ---11111	ICR39 [R/W] B, H, W ---11111	
000468H	ICR40 [R/W] B, H, W ---11111	ICR41 [R/W] B, H, W ---11111	ICR42 [R/W] B, H, W ---11111	ICR43 [R/W] B, H, W ---11111	
00046CH	ICR44 [R/W] B, H, W ---11111	ICR45 [R/W] B, H, W ---11111	ICR46 [R/W] B, H, W ---11111	ICR47 [R/W] B, H, W ---11111	
000470H to 00047CH	—				
000480H	RSRR [R/W] B, H, W 10000000	STCR [R/W] B, H, W 00110011	TBCR [R/W] B, H, W 00XXXX00	CTBR [W] B, H, W XXXXXXXX	Clock Control unit
000484H	CLKR [R/W] B, H, W 00000000	WPR [W] B, H, W XXXXXXXX	DIVR0 [R/W] B, H, W 00000011	DIVR1 [R/W] B, H, W 00000000	
000488H	—				

(Continued)

address	register				block
	+0	+1	+2	+3	
00048CH to 0005FCH	—				Reserved
000600H	DDR0 [R/W] B*1 00000000	DDR1 [R/W] B*1 00000000	DDR2 [R/W] B 00000000	—	T-unit Data Direction Register
000604H	—	—	DDR6 [R/W] B 00000000	—	
000608H	DDR8 [R/W] B*4 --000000	DDR9 [R/W] B 00000000	DDRA [R/W] B 00000000	DDRB [R/W] B 00000000	
00060CH	DDRC [R/W] B -----000		—		
000610H	—	—	—	—	T-unit Port Function Register
000614H	—	—	PFR6 [R/W] B 11111111	—	
000618H	PFR8 [R/W] B*5 --1--0--	PFR9 [R/W] B 0-001001	PFRA [R/W] B 11111111	PFRB1 [R/W] B 00000000	
00061CH	PFRB2 [R/W] B 00----00	PFRC [R/W] B ---00000	—	—	
000620H	PCR0 [R/W] B*1 00000000	PCR1 [R/W] B*1 00000000	PCR2 [R/W] B 00000000	—	T-unit Pull-up Control Register
000624H	—	—	PCR6 [R/W] B 00000000	—	
000628H	PCR8 [R/W] B*4 --000000	PCR9 [R/W] B 00000000	PCRA [R/W] B 00000000	PCRB [R/W] B 00000000	
00062CH	PCRC [R/W] B -----000	—	—	—	
000630H to 00063CH	—				Reserved
000640H	ASR0 [R/W] H, W 00000000 00000000		ACR0 [R/W] B, H, W 1111XX00 00000000		T-unit
000644H	ASR1 [R/W] H, W 00000000 00000000		ACR1 [R/W] B, H, W XXXXXXXX XXXXXXXX		
000648H	ASR2 [R/W] H, W 00000000 00000000		ACR2 [R/W] B, H, W XXXXXXXX XXXXXXXX		
00064CH	ASR3 [R/W] H, W 00000000 00000000		ACR3 [R/W] B, H, W XXXXXXXX XXXXXXXX		
000650H	ASR4 [R/W] H, W 00000000 00000000		ACR4 [R/W] B, H, W XXXXXXXX XXXXXXXX		T-unit
000654H	ASR5 [R/W] H, W 00000000 00000000		ACR5 [R/W] B, H, W XXXXXXXX XXXXXXXX		

(Continued)

address	register				block
	+0	+1	+2	+3	
000658H	ASR6 [R/W] H, W 00000000 00000000		ACR6 [R/W] B, H, W XXXXXXXX XXXXXXXX		T-unit
00065CH	ASR7 [R/W] H, W 00000000 00000000		ACR7 [R/W] B, H, W XXXXXXXX XXXXXXXX		
000660H	AWR0 [R/W] B, H, W 01111111 11111111		AWR1 [R/W] B, H, W XXXXXXXX XXXXXXXX		
000664H	AWR2 [R/W] B, H, W XXXXXXXX XXXXXXXX		AWR3 [R/W] B, H, W XXXXXXXX XXXXXXXX		
000668H	AWR4 [R/W] B, H, W XXXXXXXX XXXXXXXX		AWR5 [R/W] B, H, W XXXXXXXX XXXXXXXX		
00066CH	AWR6 [R/W] B, H, W XXXXXXXX XXXXXXXX		AWR7 [R/W] B, H, W XXXXXXXX XXXXXXXX		
000670H	—				
000674H	—				
000678H	IOWR0 [R/W] B, H, W XXXXXXXX	IOWR1 [R/W] B, H, W XXXXXXXX	IOWR2 [R/W] B, H, W XXXXXXXX	—	
00067CH	—				
000680H	CSER [R/W] B, H, W 00000001	CheR [R/W] B, H, W*1 11111111	—	TCR [W] B, H, W 0000XXXX	
000684H	—				
000684H to 0007F8H	—				Reserved
0007FCH	—	MODR [W]*6 XXXXXXXX	—	—	
000800H to 000AFCH	—				Reserved
000B00H	ESTS0 [R/W] X0000000	ESTS1 [R/W] XXXXXXXX	ESTS2 [R] 1XXXXXXX	—	DSU (MB91V340 only)
000B04H	ECTL0 [R/W] 0X000000	ECTL1 [R/W] 00000000	ECTL2 [W] 000X0000	ECTL3 [R/W] 00X00X11	
000B08H	ECNT0 [W] XXXXXXXX	ECNT1 [W] XXXXXXXX	EUSA [W] XXX00000	EDTC [W] 0000XXXX	
000B0CH	EWPT [R] 00000000 00000000		—		
000B10H	EDTR0 [W] XXXXXXXX XXXXXXXX		EDTR1 [W] XXXXXXXX XXXXXXXX		

(Continued)

address	register				block
	+0	+1	+2	+3	
000B14H to 000B1CH	—				DSU (MB91V340 only)
000B20H	EIA0 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B24H	EIA1 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B28H	EIA2 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B2CH	EIA3 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B30H	EIA4 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B34H	EIA5 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B38H	EIA6 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B3CH	EIA7 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B40H	EDTA [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B44H	EDTM [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B48H	EOA0 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B4CH	EOA1 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B50H	EPCR [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B54H	EPSR [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B58H	EIAM0 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B5CH	EIAM1 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B60H	EOAM0/EODM0 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B64H	EOAM1/EODM1 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B68H	EOD0 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

(Continued)

(Continued)

address	register				block
	+0	+1	+2	+3	
000B6C$_H$	EOD1 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				DSU (MB91V340)
000B70$_H$ to 000FFC$_H$	—				Reserved
001000$_H$	DMASA0 [R/W] W XXXXXXXX_XXXXXXXX_XXXXXXXX_XXXXXXXX				DMAC
001004$_H$	DMADA0 [R/W] W XXXXXXXX_XXXXXXXX_XXXXXXXX_XXXXXXXX				
001008$_H$	DMASA1 [R/W] W XXXXXXXX_XXXXXXXX_XXXXXXXX_XXXXXXXX				
00100C$_H$	DMADA1 [R/W] W XXXXXXXX_XXXXXXXX_XXXXXXXX_XXXXXXXX				
001010$_H$	DMASA2 [R/W] W XXXXXXXX_XXXXXXXX_XXXXXXXX_XXXXXXXX				
001014$_H$	DMADA2 [R/W] W XXXXXXXX_XXXXXXXX_XXXXXXXX_XXXXXXXX				
001018$_H$	DMASA3 [R/W] W XXXXXXXX_XXXXXXXX_XXXXXXXX_XXXXXXXX				
00101C$_H$	DMADA3 [R/W] W XXXXXXXX_XXXXXXXX_XXXXXXXX_XXXXXXXX				
001020$_H$	DMASA4 [R/W] W XXXXXXXX_XXXXXXXX_XXXXXXXX_XXXXXXXX				
001024$_H$	DMADA4 [R/W] W XXXXXXXX_XXXXXXXX_XXXXXXXX_XXXXXXXX				
001028$_H$ to 001FFC$_H$	—				Reserved

*1 : This register is only present on the MB91V340.

*2 : The Initial value of this register on the MB91V340 is [XXXXXXXX].

*3 : Byte access is not permitted for the lower 16 bits of DMAC0 to 4 (DTC[15:0])

*4: The default value of this register on the MB91V340 is [00000000].

*5: The default value of this register on the MB91V340 is [111--0--].

*6 : This register is accessed through mode vector fetch; it cannot be accessed in normal mode.

■ INTERRUPT VECTORS

Interrupt	Interrupt No.		Interrupt level	Offset	TBR default address	RN
	Number					
Reset	#0	00H	—	3FCH	000FFFFCH	—
Mode vector	#1	01H	—	3F8H	000FFFF8H	—
System reserved	#2	02H	—	3F4H	000FFFF4H	—
System reserved	#3	03H	—	3F0H	000FFFF0H	—
System reserved	#4	04H	—	3ECH	000FFFECH	—
System reserved	#5	05H	—	3E8H	000FFFE8H	—
System reserved	#6	06H	—	3E4H	000FFFE4H	—
Coprocessor absent trap	#7	07H	—	3E0H	000FFFE0H	—
Coprocessor error trap	#8	08H	—	3DCH	000FFFDCH	—
INTE instruction	#9	09H	—	3D8H	000FFFD8H	—
Instruction break exception	#10	0AH	—	3D4H	000FFFD4H	—
Operand break trap	#11	0BH	—	3D0H	000FFFD0H	—
Step trace trap	#12	0CH	—	3CCH	000FFFCCH	—
NMI request (tool)	#13	0DH	—	3C8H	000FFFC8H	—
Undefined instruction exception	#14	0EH	—	3C4H	000FFFC4H	—
NMI request	#15	0FH	15 (FH) fixed	3C0H	000FFFC0H	—
External interrupt 0	#16	10H	ICR00	3BCH	000FFFBCH	6
External interrupt 1	#17	11H	ICR01	3B8H	000FFFB8H	7
External interrupt 2	#18	12H	ICR02	3B4H	000FFFB4H	11
External interrupt 3	#19	13H	ICR03	3B0H	000FFFB0H	12
External interrupt 4	#20	14H	ICR04	3ACH	000FFFACH	—
External interrupt 5	#21	15H	ICR05	3A8H	000FFFA8H	—
External interrupt 6	#22	16H	ICR06	3A4H	000FFFA4H	—
External interrupt 7	#23	17H	ICR07	3A0H	000FFFA0H	—
Reload timer 0	#24	18H	ICR08	39CH	000FFF9CH	8
Reload timer 1	#25	19H	ICR09	398H	000FFF98H	9
Reload timer 2	#26	1AH	ICR10	394H	000FFF94H	10
UART0 (RX completed)	#27	1BH	ICR11	390H	000FFF90H	0
UART1 (RX completed)	#28	1CH	ICR12	38CH	000FFF8CH	1
UART2 (RX completed)	#29	1DH	ICR13	388H	000FFF88H	2
UART0 (TX completed)	#30	1EH	ICR14	384H	000FFF84H	3
UART1 (TX completed)	#31	1FH	ICR15	380H	000FFF80H	4
UART2 (TX completed)	#32	20H	ICR16	37CH	000FFF7CH	5

(Continued)

Interrupt	Interrupt No. Number		Interrupt level	Offset	TBR default address	RN
DMAC0 (end, error)	#33	21_H	ICR17	378_H	$000FFF78_H$	—
DMAC1 (end, error)	#34	22_H	ICR18	374_H	$000FFF74_H$	—
DMAC2 (end, error)	#35	23_H	ICR19	370_H	$000FFF70_H$	—
DMAC3 (end, error)	#36	24_H	ICR20	$36C_H$	$000FFF6C_H$	—
DMAC4 (end, error)	#37	25_H	ICR21	368_H	$000FFF68_H$	—
A/D	#38	26_H	ICR22	364_H	$000FFF64_H$	15
I^2C	#39	27_H	ICR23	360_H	$000FFF60_H$	—
U/D counter 0	#40	28_H	ICR24	$35C_H$	$000FFF5C_H$	—
U/D counter 1	#41	29_H	ICR25	358_H	$000FFF58_H$	—
U/D counter 2	#42	$2A_H$	ICR26	354_H	$000FFF54_H$	—
U/D counter 3	#43	$2B_H$	ICR27	350_H	$000FFF50_H$	—
U-TIMER0	#44	$2C_H$	ICR28	$34C_H$	$000FFF4C_H$	—
U-TIMER1	#45	$2D_H$	ICR29	348_H	$000FFF48_H$	—
U-TIMER2	#46	$2E_H$	ICR30	344_H	$000FFF44_H$	—
Time base timer overflow	#47	$2F_H$	ICR31	340_H	$000FFF40_H$	—
Reload timer 3	#48	30_H	ICR32	$33C_H$	$000FFF3C_H$	13
UP counter	#49	31_H	ICR33	338_H	$000FFF38_H$	14
System reserved	#50	32_H	ICR34	334_H	$000FFF34_H$	—
System reserved	#51	33_H	ICR35	330_H	$000FFF30_H$	—
16 bit freerun timer	#52	34_H	ICR36	$32C_H$	$000FFF2C_H$	—
ICU0 (capture)	#53	35_H	ICR37	328_H	$000FFF28_H$	—
ICU1 (capture)	#54	36_H	ICR38	324_H	$000FFF24_H$	—
ICU2 (capture)	#55	37_H	ICR39	320_H	$000FFF20_H$	—
ICU3 (capture)	#56	38_H	ICR40	$31C_H$	$000FFF1C_H$	—
OCU0 (match)	#57	39_H	ICR41	318_H	$000FFF18_H$	—
OCU1 (match)	#58	$3A_H$	ICR42	314_H	$000FFF14_H$	—
OCU2 (match)	#59	$3B_H$	ICR43	310_H	$000FFF10_H$	—
OCU3 (match)	#60	$3C_H$	ICR44	$30C_H$	$000FFF0C_H$	—
OCU4/5 (match)	#61	$3D_H$	ICR45	308_H	$000FFF08_H$	—
OCU6/7 (match)	#62	$3E_H$	ICR46	304_H	$000FFF04_H$	—
Delay interrupt bit	#63	$3F_H$	ICR47	300_H	$000FFF00_H$	—
System reserved (Used by REALOS)	#64	40_H	—	$2FC_H$	$000FFEFC_H$	—
System reserved (Used by REALOS)	#65	41_H	—	$2F8_H$	$000FFEF8_H$	—
System reserved	#66	42_H	—	$2F4_H$	$000FFEF4_H$	—

(Continued)

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Interrupt	Interrupt No. Number		Interrupt level	Offset	TBR default address	RN
System reserved	#67	43_H	—	$2F0_H$	$000FFEF0_H$	—
System reserved	#68	44_H	—	$2EC_H$	$000FFEEC_H$	—
System reserved	#69	45_H	—	$2E8_H$	$000FFEE8_H$	—
System reserved	#70	46_H	—	$2E4_H$	$000FFEE4_H$	—
System reserved	#71	47_H	—	$2E0_H$	$000FFEE0_H$	—
System reserved	#72	48_H	—	$2DC_H$	$000FFEDC_H$	—
System reserved	#73	49_H	—	$2D8_H$	$000FFED8_H$	—
System reserved	#74	$4A_H$	—	$2D4_H$	$000FFED4_H$	—
System reserved	#75	$4B_H$	—	$2D0_H$	$000FFED0_H$	—
System reserved	#76	$4C_H$	—	$2CC_H$	$000FFECC_H$	—
System reserved	#77	$4D_H$	—	$2C8_H$	$000FFEC8_H$	—
System reserved	#78	$4E_H$	—	$2C4_H$	$000FFEC4_H$	—
System reserved	#79	$4F_H$	—	$2C0_H$	$000FFEC0_H$	—
Used by INT instruction	#80 to #255	50_H to FF_H	—	$2BC_H$ to 000_H	$000FFEBC_H$ to $000FFC00_H$	—

■ PERIPHERAL RESOURCES

This section describes the location of each peripheral resource register in the memory space.

1. External Bus Interface Controller

The external bus interface controller controls the interface between the LSI's internal bus and external memory and I/O devices.

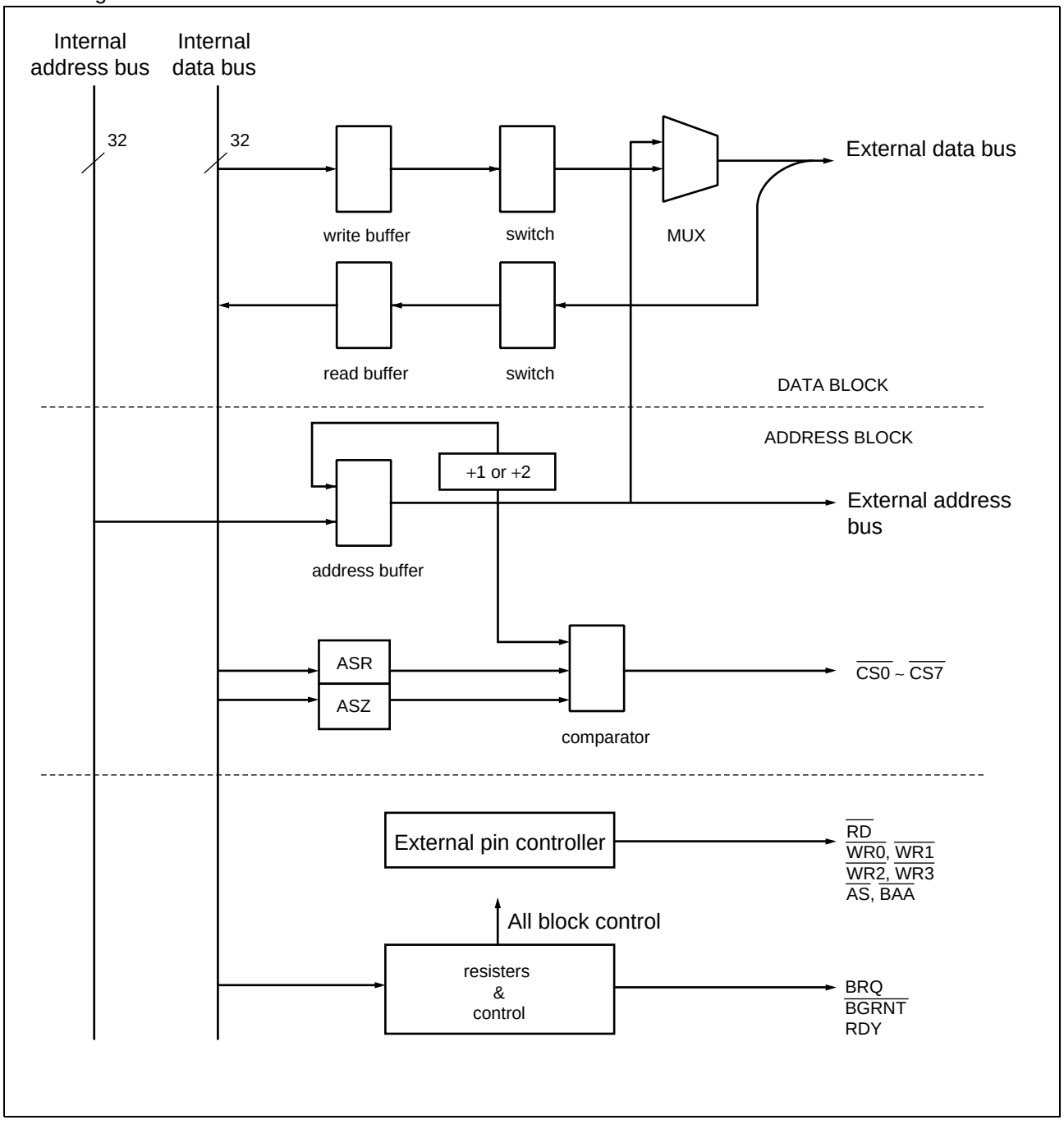
• External Bus Interface Controller Features

- Maximum output address width = 32-bit (4GB memory space)
- Various different types of external memory (8-bit, 16-bit, or 32-bit devices) can be directly connected and the controller can support multiple devices with different access timings.
  Asynchronous SRAM, asynchronous ROM/FLASH memory (supports multiple write strobe access or byte-enable access)
  Page mode ROM/FLASH memory (2, 4, or 8 page size)
  Burst mode ROM/FLASH memory (MBM29BL160D/161D/162D or equivalent)
  Address/data multiplexed bus (8-bit or 16-bit width only)
  Synchronous memory (ASIC internal memory, etc.)
  Note: Synchronous SRAM cannot be directly connected.
- Memory can be divided into eight independent banks (chip select areas) with a separate chip select output for each bank.
  The size of each area can be set in 64Kbyte increments (the size of each chip select area can range from 64Kbyte to 2Gbyte)
  Each area can be located anywhere in the physical address space (subject to boundary limitations based on the area size)
- The following functions can be set independently for each chip select area :
  Chip select area enable/disable (Access is not performed to disabled areas)
  Access timing type settings to suit the type of memory used
  Detailed access timing settings (wait cycles and similar settings for each access type)
  Data bus width (8-bit, 16-bit, 32-bit)
  Byte-ordering setting (big or little endian)
  Note: The CS0 area must be big endian.
  Write-prohibit setting (read-only areas)
  Enable or disable loading into internal cache
  Enable or disable prefetch function
  Maximum burst length setting (1, 2, 4, 8)
- Different detailed timing settings can be set for each timing type
  Even for the same type, different settings can be used for each chip select area.
  Up to 15 auto-wait cycles can be specified. (For asynchronous SRAM, ROM, Flash, and I/O areas)
  The bus cycle can be extended by the external RDY input. (For asynchronous SRAM, ROM, Flash, and I/O areas)
  Fast access wait and page wait settings are supported (For burst/page mode ROM and Flash areas)
  Idle cycles, recovery cycles, setup delays, and similar can be inserted.
- DMA supports fly-by transfer
  Transfer between memory and I/O can be performed by a single access.
  Memory wait cycles can be synchronized with the I/O wait period during fly-by transfer.
  Hold times can be maintained by extending access to the data source only.
  Separate idle and recovery cycle settings can be specified for use in fly-by transfer.
- Supports external bus arbitration using BRQ and $\overline{\text{BGRNT}}$.
- Pins not used by the external interface can be set as general purpose I/O ports.

- **Chip select areas**

The external bus interface supports up to eight separate chip select area settings.
The address range for each area can be set anywhere in the 4Gbyte memory space in 64Kbyte increments. The address settings for each area are set in ASR0 to ASR7 (Area Select Register) and ACR0 to ACR7 (Area Configuration Register).
When bus access is performed to one of the areas specified in these registers, the corresponding chip select signal ($\overline{CS0}$ to $\overline{CS7}$) is asserted (outputs "L") for the duration of the access cycle.
After a reset and until a value is written to ACR0, address range 00000000_H to $FFFFFFFF_H$ is assigned to chip select area 0.

- Block Diagram



• Register List

Address	31 24	23 16	15 08	07 00
00000640H	ASR0		ACR0	
00000644H	ASR1		ACR1	
00000648H	ASR2		ACR2	
0000064CH	ASR3		ACR3	
00000650H	ASR4		ACR4	
00000654H	ASR5		ACR5	
00000658H	ASR6		ACR6	
0000065CH	ASR7		ACR7	
00000660H	AWR0		AWR1	
00000664H	AWR2		AWR3	
00000668H	AWR4		AWR5	
0000066CH	AWR6		AWR7	
00000670H	Reserved	Reserved	Reserved	Reserved
00000674H	Reserved	Reserved	Reserved	Reserved
00000678H	IOWR0	IOWR1	IOWR2	Reserved
0000067CH	Reserved	Reserved	Reserved	Reserved
00000680H	CSER	CHER	Reserved	Reserved
00000684H	Reserved	Reserved	Reserved	Reserved
00000688H	Reserved	Reserved	Reserved	Reserved
0000068CH	Reserved	Reserved	Reserved	Reserved
	—	—	—	—
000007F8H	Reserved	Reserved	Reserved	Reserved
000007FCH	Reserved	(MODR)	Reserved	Reserved

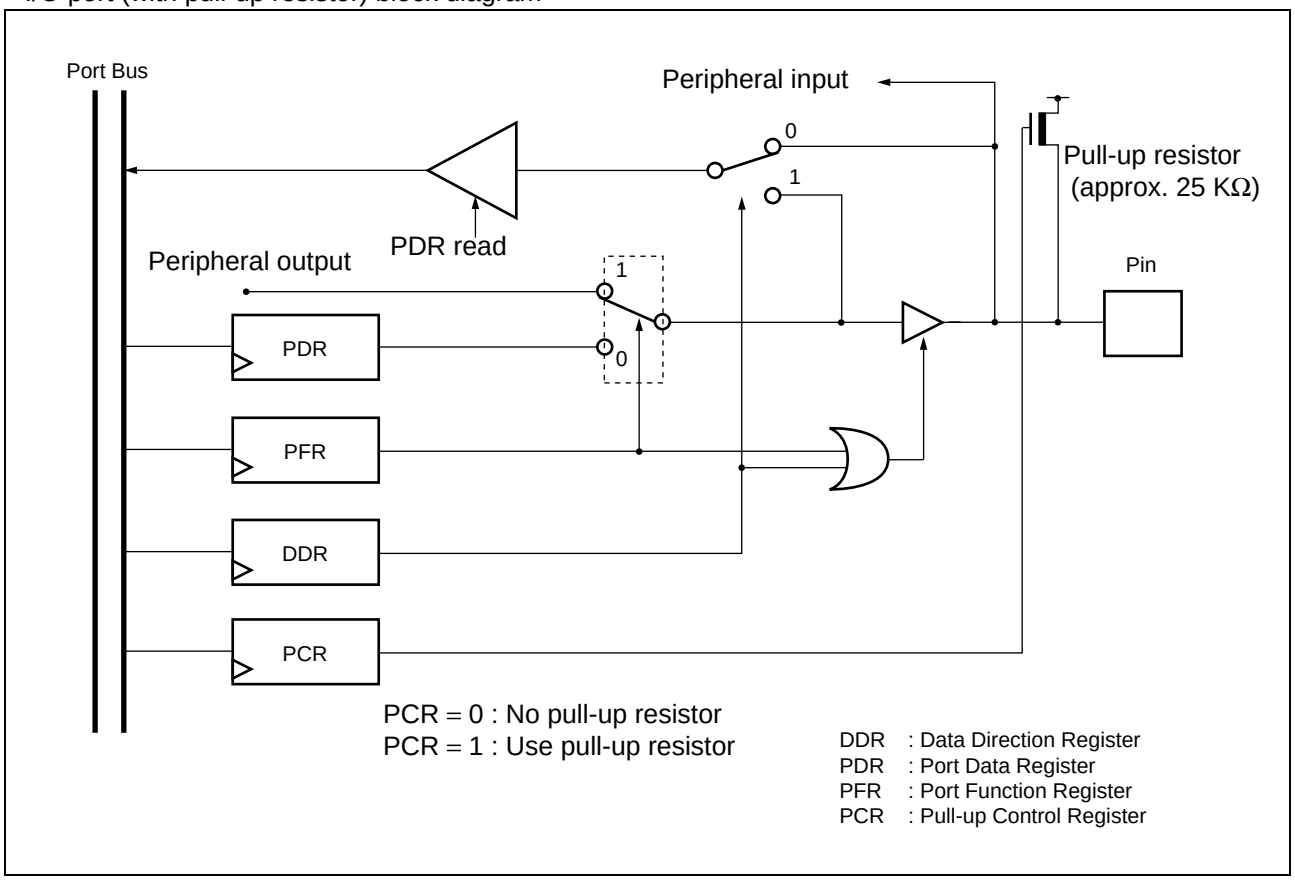
Reserved : Indicates a reserved register. When writing, always set to “0”.

The MODR register cannot be accessed by the user program.

2. I/O Ports

MB91340/MB91V340 pins can be used as I/O ports when not set for use by the external bus interface or the various peripheral I/O functions.

• I/O port (with pull-up resistor) block diagram



• I/O port registers

I/O ports with pull-up resistors have the following registers :

- PDR (Port Data Register)
- DDR (Data Direction Register)
- PFR (Port Function Register)
- PCR (Pull-up Control Register)

- When port is in input mode (PFR = “0” & DDR = “0”)
  PDR read : Reads the level of the corresponding external pin.
  PDR write : PDRWrites the value to the PDR.
- When port is in output mode (PFR = “0” & DDR = “1”)
  PDR read : Reads the PDR value.
  PDR write : Outputs the PDR value to the corresponding external pin.
- When port is in peripheral output mode (PFR = “1” & DDR = “X”)
  PDR : Reads the value of the corresponding peripheral output.
  PDR write : Writes the value to the PDR.

Notes :
- Use byte access to access ports.
- The external bus function has priority for port 0 to port A when these are used as external bus pins. Accordingly, writing to the DDR has no effect on the pin input/output setting while the pins are operating as external bus pins. The value set in the DDR becomes meaningful when the PFR register is modified to set the pins as general purpose ports.
- In stop mode (HiZ = 0), the pull-up resistor control register setting is used.
- In stop mode (HiZ = 1), the pull-up resistor control register setting is ignored during hardware standby.
- Using pull-up resistors is prohibited when these pins are used as external bus pins. In this case, do not write ’1" to the corresponding bit in the pull-up control register (PCR).

• Port Data Register (PDR)

	7	6	5	4	3	2	1	0	Initial value	Access
PDR0 Address : 00000000H	P07	P06	P05	P04	P03	P02	P01	P00	XXXXXXXXB	R/W
PDR1 Address : 00000001H	P17	P16	P15	P14	P13	P12	P11	P10	XXXXXXXXB	R/W
PDR2 Address : 00000002H	P27	P26	P25	P24	P23	P22	P21	P20	XXXXXXXXB	R/W
PDR6 Address : 00000006H	P67	P66	P65	P64	P63	P62	P61	P60	XXXXXXXXB	R/W
PDR8 Address : 00000008H	— (P87)	— (P86)	P85	—	—	P82	P81	P80	- - XXXXXXB (XXXXXXXXB)	R/W
PDR9 Address : 00000009H	P97	P96	P95	P94	P93	P92	P91	P90	XXXXXXXXB	R/W
PDRA Address : 0000000AH	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	XXXXXXXXB	R/W
PDRB Address : 0000000BH	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0	XXXXXXXXB	R/W
PDRC Address : 0000000CH	—	—	—	—	—	PC2	PC1	PC0	- - - - - XXXB	R/W
PDRH Address : 00000011H	—	—	—	—	—	PH2	PH1	PH0	- - - - - XXXB	R/W
PDRI Address : 00000012H	—	—	PI5	PI4	PI3	PI2	PI1	PI0	- - XXXXXXB	R/W
PDRJ Address : 00000013H	PJ7	PJ6	PJ5	PJ4	PJ3	PJ2	PJ1	PJ0	XXXXXXXXB	R/W
PDRK Address : 00000014H	PK7	PK6	PK5	PK4	PK3	PK2	PK1	PK0	XXXXXXXXB	R/W
PDRL Address : 00000015H	—	PL6	PL5	PL4	PL3	PL2	PL1	PL0	- XXXXXXXB	R/W

(Continued)

(Continued)

		7	6	5	4	3	2	1	0	Initial value	Access
PDRM	Address: 00000016H	—	—	—	—	PM3	PM2	PM1	PM0	- - - - XXXXB	R/W
PDRN	Address: 00000017H	PN7	PN6	PN5	PN4	PN3	PN2	PN1	PN0	XXXXXXXXB	R/W
PDRO	Address: 00000018H	PO7	PO6	PO5	PO4	PO3	PO2	PO1	PO0	XXXXXXXXB	R/W
PDRP	Address: 00000019H	PP7	PP6	PP5	PP4	PP3	PP2	PP1	PP0	XXXXXXXXB	R/W

PDR0 to PDRP are the I/O data registers for the I/O pots. The corresponding DDR0 to DDRP and PFR6 to PFRO registers control input and output operation.
P00 to P07, P10 to P17, P20 to P27, PJ0 to PJ7, PM0 to PM7, PN0 to PN7, and PP0 to PP7 do not have a PFR (port function register).

Note: PDR0 to PDR1 only exist on the MB91V340. The values enclosed in brackets ( ) for PDR8 indicate the functions and default values for the MB91V340.

• Data Direction Register (DDR)

DDR0
Address: 00000600H

7	6	5	4	3	2	1	0	Initial value	Access
P07	P06	P05	P04	P03	P02	P01	P00	00000000B	R/W

DDR1
Address: 00000601H

7	6	5	4	3	2	1	0	Initial value	Access
P17	P16	P15	P14	P13	P12	P11	P10	00000000B	R/W

DDR2
Address: 00000602H

7	6	5	4	3	2	1	0	Initial value	Access
P27	P26	P25	P24	P23	P22	P21	P20	00000000B	R/W

DDR6
Address: 00000606H

7	6	5	4	3	2	1	0	Initial value	Access
P67	P66	P65	P64	P63	P62	P61	P60	00000000B	R/W

DDR8
Address: 00000608H

7	6	5	4	3	2	1	0	Initial value	Access
— (P87)	— (P86)	P85	—	—	P82	P81	P80	- - 000000B (00000000B)	R/W

DDR9
Address: 00000609H

7	6	5	4	3	2	1	0	Initial value	Access
P97	P96	P95	P94	P93	P92	P91	P90	00000000B	R/W

DDRA
Address: 0000060AH

7	6	5	4	3	2	1	0	Initial value	Access
PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	00000000B	R/W

DDRB
Address: 0000060BH

7	6	5	4	3	2	1	0	Initial value	Access
PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0	00000000B	R/W

DDRC
Address: 0000060CH

7	6	5	4	3	2	1	0	Initial value	Access
—	—	—	—	—	PC2	PC1	PC0	- - - - - 000B	R/W

DDRH
Address: 00000401H

7	6	5	4	3	2	1	0	Initial value	Access
—	—	—	—	—	PH2	PH1	PH0	- - - - - 000B	R/W

DDRI
Address: 00000402H

7	6	5	4	3	2	1	0	Initial value	Access
—	—	PI5	PI4	PI3	PI2	PI1	PI0	- - 000000B	R/W

DDRJ
Address: 00000403H

7	6	5	4	3	2	1	0	Initial value	Access
PJ7	PJ6	PJ5	PJ4	PJ3	PJ2	PJ1	PJ0	00000000B	R/W

DDRK
Address: 00000404H

7	6	5	4	3	2	1	0	Initial value	Access
PK7	PK6	PK5	PK4	PK3	PK2	PK1	PK0	00000000B	R/W

DDRL
Address: 00000405H

7	6	5	4	3	2	1	0	Initial value	Access
—	PL6	PL5	PL4	PL3	PL2	PL1	PL0	- 0000000B	R/W

(Continued)

(Continued)

DDRM

Address: 00000406H

7	6	5	4	3	2	1	0	Initial value	Access
—	—	—	—	PM3	PM2	PM1	PM0	- - - - 0000B	R/W

DDRN

Address: 00000407H

7	6	5	4	3	2	1	0	Initial value	Access
PN7	PN6	PN5	PN4	PN3	PN2	PN1	PN0	00000000B	R/W

DDRO

Address: 00000408H

7	6	5	4	3	2	1	0	Initial value	Access
PO7	PO6	PO5	PO4	PO3	PO2	PO1	PO0	00000000B	R/W

DDRP

Address: 00000409H

7	6	5	4	3	2	1	0	Initial value	Access
PP7	PP6	PP5	PP4	PP3	PP2	PP1	PP0	00000000B	R/W

DDR0 to DDRP control the direction (input or output) of each bit in the corresponding port.

When PFR = 0 DDR = 0 : Port input

DDR = 1 : Port output

When PFR = 1 DDR = 0 : Peripheral input

DDR = 1 : Peripheral output

Note: DDR0 to DDR1 only exist on the MB91V340. The values enclosed in brackets ( ) for DDR8 indicate the functions and default values for the MB91V340.

• Pull-up Control Register (PCR)

	7	6	5	4	3	2	1	0	Initial value	Access
PCR0 Address: 00000620H	P07	P06	P05	P04	P03	P02	P01	P00	00000000B	R/W
PCR1 Address: 00000621H	P17	P16	P15	P14	P13	P12	P11	P10	00000000B	R/W
PCR2 Address: 00000622H	P27	P26	P25	P24	P23	P22	P21	P20	00000000B	R/W
PCR6 Address: 00000626H	P67	P66	P65	P64	P63	P62	P61	P60	00000000B	R/W
PCR8 Address: 00000628H	— (P87)	— (P86)	P85	— *1	— *1	P82	P81	P80	- - 000000B (00000000B)	R/W
PCR9 Address: 00000629H	P97	P96	P95	P94	P93	P92	P91	P90	00000000B	R/W
PCRA Address: 0000062AH	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	00000000B	R/W
PCRB Address: 0000062BH	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0	00000000B	R/W
PCRC Address: 0000062CH	—	—	—	—	—	PC2	PC1	PC0	- - - - - 000B	R/W
PCRH Address: 00000421H	—	—	—	—	—	PH2	PH1	PH0	- - - - - 000B	R/W
PCRI Address: 00000422H	—	—	PI5	PI4	PI3	PI2	PI1	PI0	- - 000000B	R/W
PCRJ Address: 00000423H	PJ7	PJ6	PJ5	PJ4	PJ3	PJ2	PJ1	PJ0	00000000B	R/W
PCRK Address: 00000424H	PK7	PK6	PK5	PK4	PK3	PK2	PK1	PK0	00000000B	R/W
PCRL Address: 00000425H	—	PL6	PL5	PL4	PL3	PL2	PL1	PL0	- 0000000B	R/W

(Continued)

(Continued)

	7	6	5	4	3	2	1	0	Initial value	Access
PCRM Address: 00000426H	—	—	—	—	PM3	PM2	PM1	PM0	- - - - 0000B	R/W
PCRN Address: 00000427H	PN7	PN6	PN5	PN4	PN3	PN2	PN1	PN0	00000000B	R/W
PCRO Address: 00000428H	PO7	PO6	PO5	PO4	PO3	PO2	PO1	PO0	00000000B	R/W
PCRP Address: 00000429H	PP7	PP6	PP5	PP4	PP3	PP2	PP1	PP0	00000000B	R/W

PCR0 to PCRP control the pull-up resistors for the corresponding port.

PCR = 0 : No pull-up resistor

PCR = 1 : Use pull-up resistor

Notes:
- PCR0 to PCR1 only exist on the MB91V340. The values enclosed in brackets ( ) for PCR8 indicate the functions and default values for the MB91V340.
- Always write "0" to bits indicated by "*1".
- Always write "0" to the bits for general purpose ports corresponding to pins used as external bus pins.

• Port Function Register (PFR)

PFR6
Address: 00000616H

7	6	5	4	3	2	1	0	Initial value	Access
A23E	A22E	A21E	A20E	A19E	A18E	A17E	A16E	11111111B	R/W

PFR8
Address: 00000618H

7	6	5	4	3	2	1	0	Initial value	Access
— (WR3XE)	— (WR2XE)	WR1XE	—	—	BRQE	—	—	- - 1 - - 0 - -B (111 - - 0 - -B)	R/W

PFR9
Address: 00000619H

7	6	5	4	3	2	1	0	Initial value	Access
WEXE	—	BAAE	ASXE	*1	MCKE	—	SYSE	0 - 001001B	R/W

PFRA
Address: 0000061AH

7	6	5	4	3	2	1	0	Initial value	Access
CS7XE	CS6XE	CS5XE	CS4XE	CS3XE	CS2XE	CS1XE	CS0XE	11111111B	R/W

PFRB1
Address: 0000061BH

7	6	5	4	3	2	1	0	Initial value	Access
DES1	AK12	AK11	AK10	DES0	AK02	AK01	AK00	00000000B	R/W

PFRB2
Address: 0000061CH

7	6	5	4	3	2	1	0	Initial value	Access
DRDE	DWRE	—	—	—	—	AKH1	AKH0	00 - - - - 00B	R/W

PFRC
Address: 0000061DH

7	6	5	4	3	2	1	0	Initial value	Access
—	—	—	AKH2	DES2	AK22	AK21	AK00	- - - 00000B	R/W

PFRH
Address: 00000411H

7	6	5	4	3	2	1	0	Initial value	Access
—	—	—	—	—	SCE2	SOE2	—	- - - - - 00 -B	R/W

PFRI
Address: 00000412H

7	6	5	4	3	2	1	0	Initial value	Access
—	—	SCE1	SOE1	—	SCE0	SOE0	—	- - 00 - 00 -B	R/W

PFRK
Address: 00000414H

7	6	5	4	3	2	1	0	Initial value	Access
TOE3	TOE2	TOE1	TOE0	—	—	—	—	0000 - - - -B	R/W

PFRL
Address: 00000415H

7	6	5	4	3	2	1	0	Initial value	Access
UDE1	UDE0	—	—	—	I2CD	TEST	I2CE	00 - - - 000B	R/W

PFRO
Address: 00000418H

7	6	5	4	3	2	1	0	Initial value	Access
OTE7	OTE6	OTE5	OTE4	OTE3	OTE2	OTE1	OTE0	00000000B	R/W

PFR6 to PFRO control the output for the corresponding external bus interface or peripheral output bit.
Always write "0" to unused bits in the PFR. (However, always write "1" to bits indicated by "*1")

Note: The values enclosed in brackets ( ) for PFR8 indicate the functions and default values for the MB91V340.

3. Interrupt Controller

The interrupt controller receives and processes interrupts.

• Hardware Configuration

The interrupt controller consists of the following :

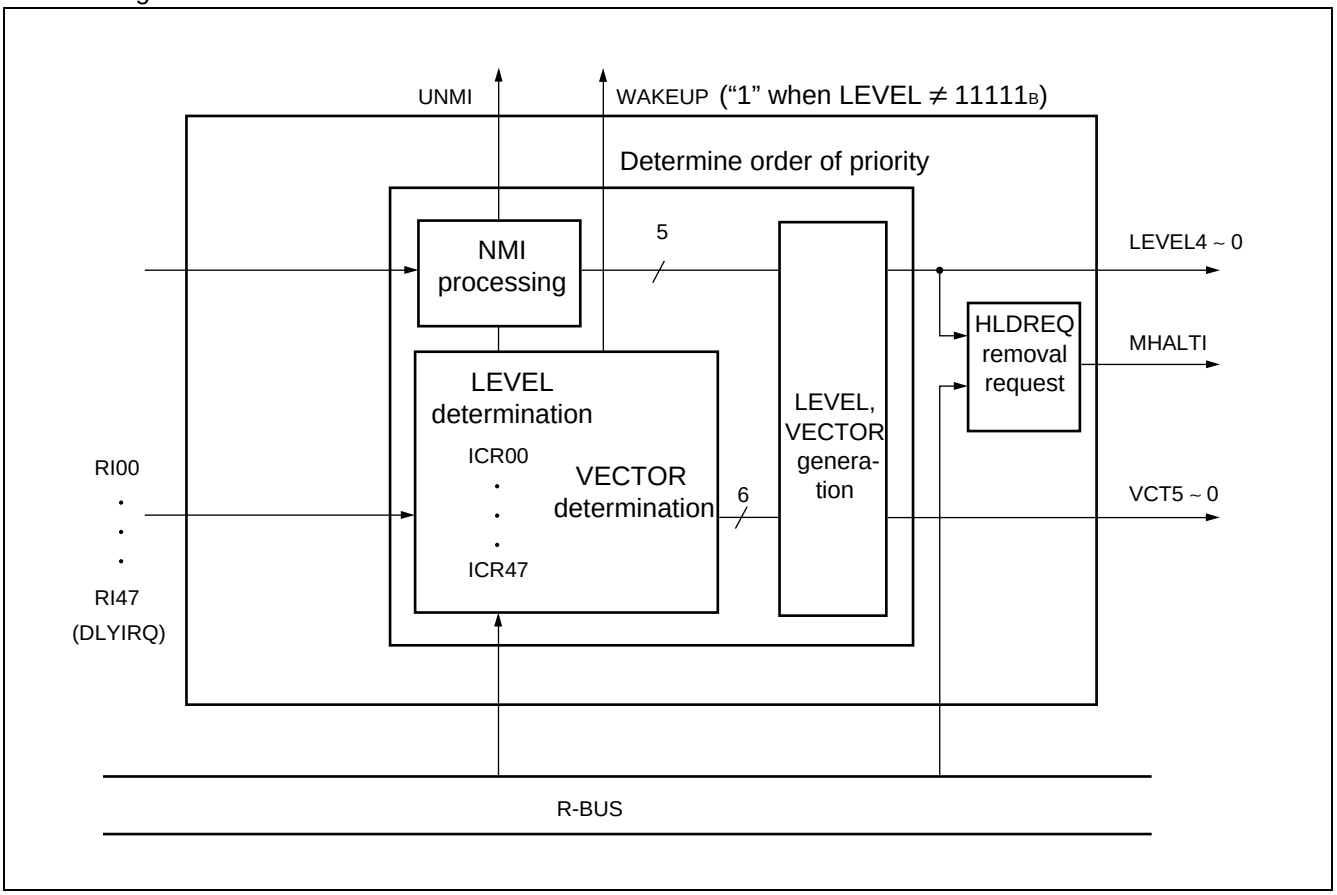
- ICR register
- Interrupt priority determination circuit
- Interrupt level and interrupt number (vector) generator
- Hold request removal request generator

• Principal Functions

The main functions of the interrupt controller are as follows :

- Detect NMI and interrupt requests
- Prioritize interrupts (according to level and number)
- Notify interrupt level of selected interrupt request (to CPU)
- Notify interrupt number of selected interrupt request (to CPU)
  If an NMI or interrupt request with an interrupt level other than "11111_B" occurs, notify recovery from stop mode (to CPU)
- Generate hold request removal requests to the bus master

• Block Diagram



• Register List

Bit	7	6	5	4	3	2	1	0	
Address: 00000440H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR00
Address: 00000441H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR01
Address: 00000442H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR02
Address: 00000443H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR03
Address: 00000444H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR04
Address: 00000445H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR05
Address: 00000446H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR06
Address: 00000447H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR07
Address: 00000448H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR08
Address: 00000449H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR09
Address: 0000044AH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR10
Address: 0000044BH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR11
Address: 0000044CH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR12
Address: 0000044DH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR13
Address: 0000044EH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR14
Address: 0000044FH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR15
Address: 00000450H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR16
Address: 00000451H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR17
Address: 00000452H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR18
Address: 00000453H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR19
Address: 00000454H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR20
Address: 00000455H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR21
Address: 00000456H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR22
Address: 00000457H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR23
Address: 00000458H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR24
Address: 00000459H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR25
Address: 0000045AH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR26
Address: 0000045BH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR27
Address: 0000045CH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR28
Address: 0000045DH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR29
Address: 0000045EH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR30
Address: 0000045FH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR31
				R	R/W	R/W	R/W	R/W	

(Continued)

(Continued)

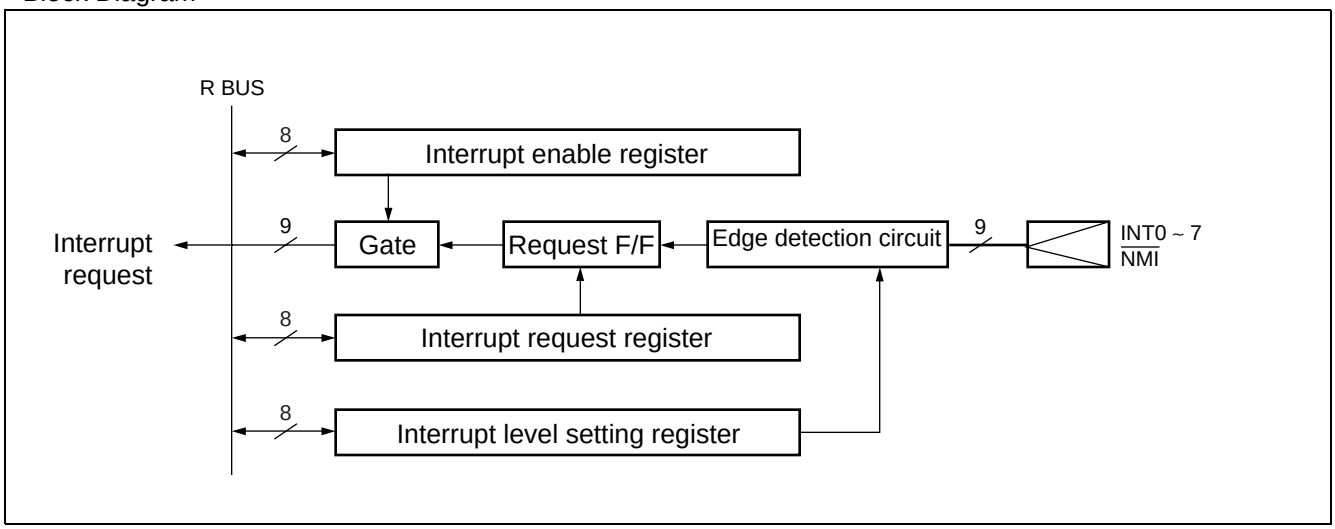
Bit	7	6	5	4	3	2	1	0	
Address: 00000460H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR32
Address: 00000461H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR33
Address: 00000462H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR34
Address: 00000463H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR35
Address: 00000464H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR36
Address: 00000465H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR37
Address: 00000466H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR38
Address: 00000467H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR39
Address: 00000468H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR40
Address: 00000469H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR41
Address: 0000046AH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR42
Address: 0000046BH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR43
Address: 0000046CH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR44
Address: 0000046DH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR45
Address: 0000046EH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR46
Address: 0000046FH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR47
				R	R/W	R/W	R/W	R/W	

Address: 00000045H	MHALTI	—	—	LVL4	LVL3	LVL2	LVL1	LVL0	HRCL
	R/W			R	R/W	R/W	R/W	R/W	

4. External Interrupt/NMI Control Block

The external interrupt control block controls external interrupt requests input to the NMIX and INT0-7 pins. The interrupt trigger level can be selected from "H", "L", "rising edge", or "falling edge" (except for NMI).

• Block Diagram



• Register List

External interrupt enable register (ENIR)

bit

7	6	5	4	3	2	1	0
EN7	EN6	EN5	EN4	EN3	EN2	EN1	EN0

External interrupt request register (EIRR)

bit

15	14	13	12	11	10	9	8
ER7	ER6	ER5	ER4	ER3	ER2	ER1	ER0

Request level setting register (ELVR)

bit

15	14	13	12	11	10	9	8
LB7	LA7	LB6	LA6	LB5	LA5	LB4	LA4

bit

7	6	5	4	3	2	1	0
LB3	LA3	LB2	LA2	LB1	LA1	LB0	LA0

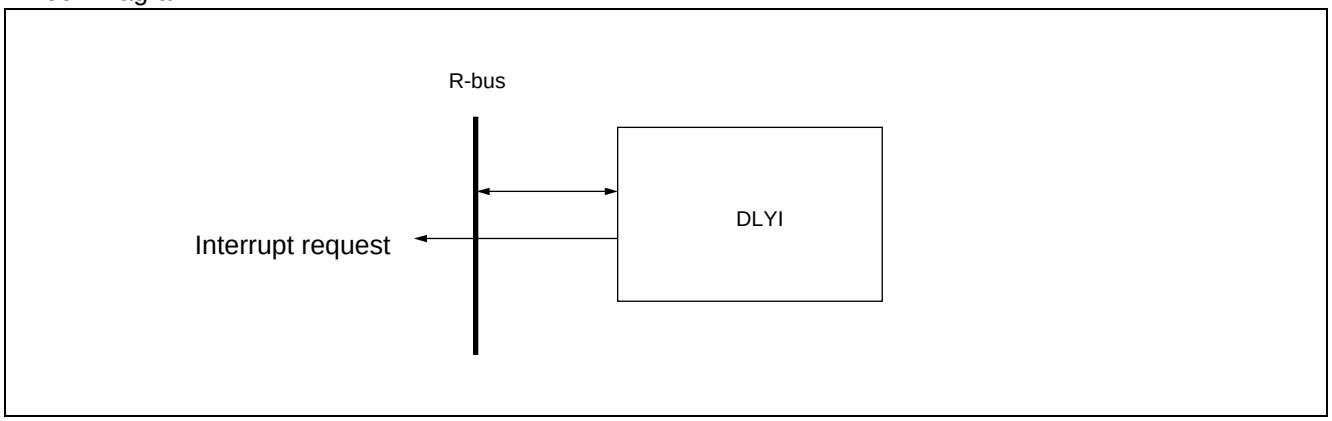
5. REALOS Related Hardware

The REALOS hardware is used by the realtime operating system. Accordingly, these resources are not available to the user program when REALOS is used.

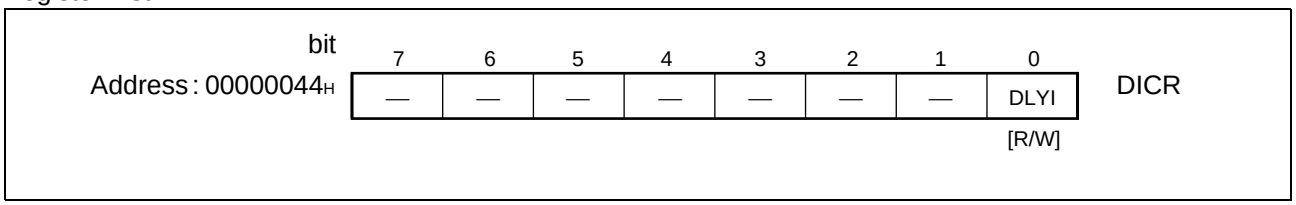
5.1 Delay Interrupt Module

The delay interrupt module is used to generate interrupts for task switching.
This module can be used to generate and cancel interrupts to the CPU via software.

- Block Diagram



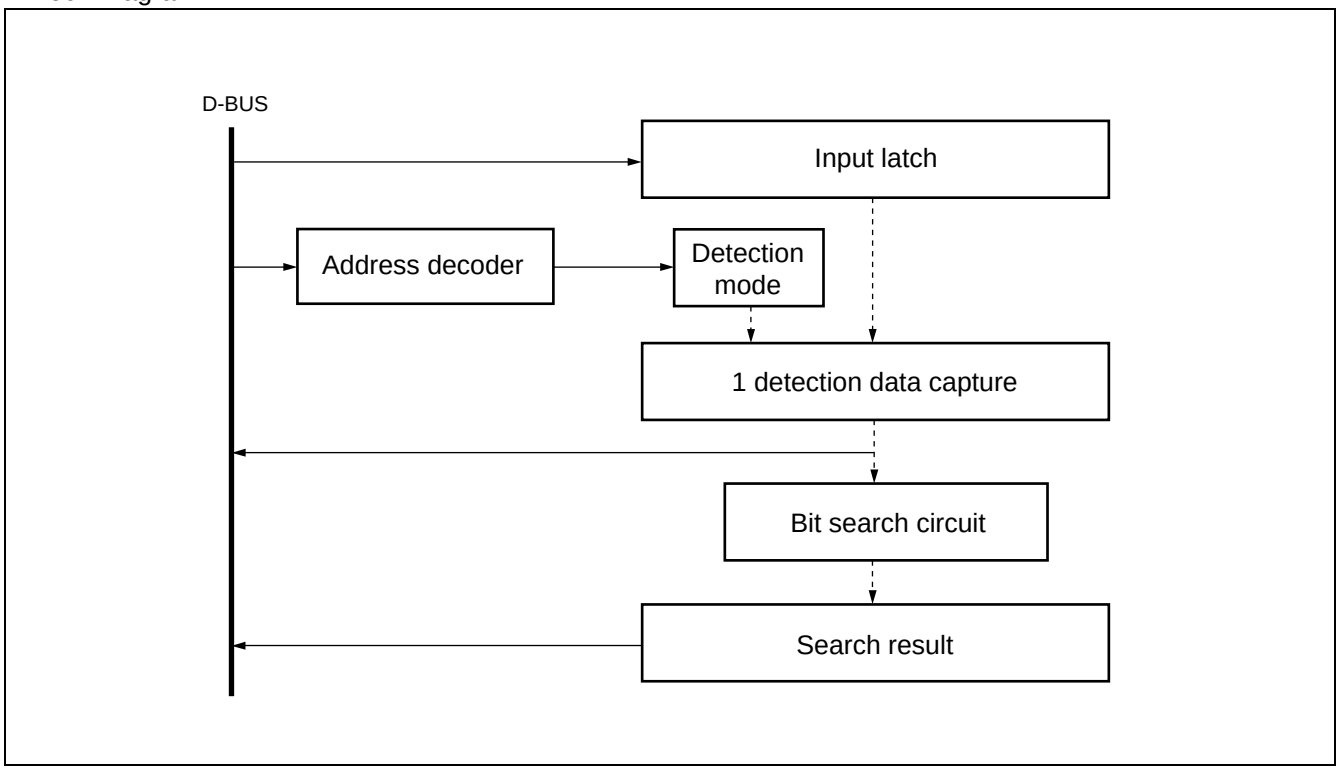
- Register List



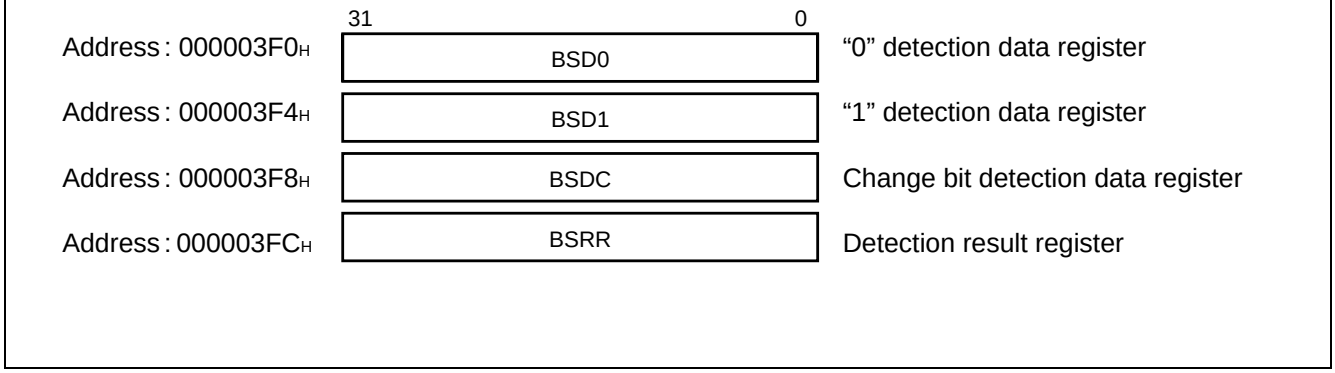
5.2 Bit Search Module

Searches the data written to the input register for the first bit containing "0", "1", or a change in value. The module returns the position of the detected bit.

• Block Diagram



• Register List



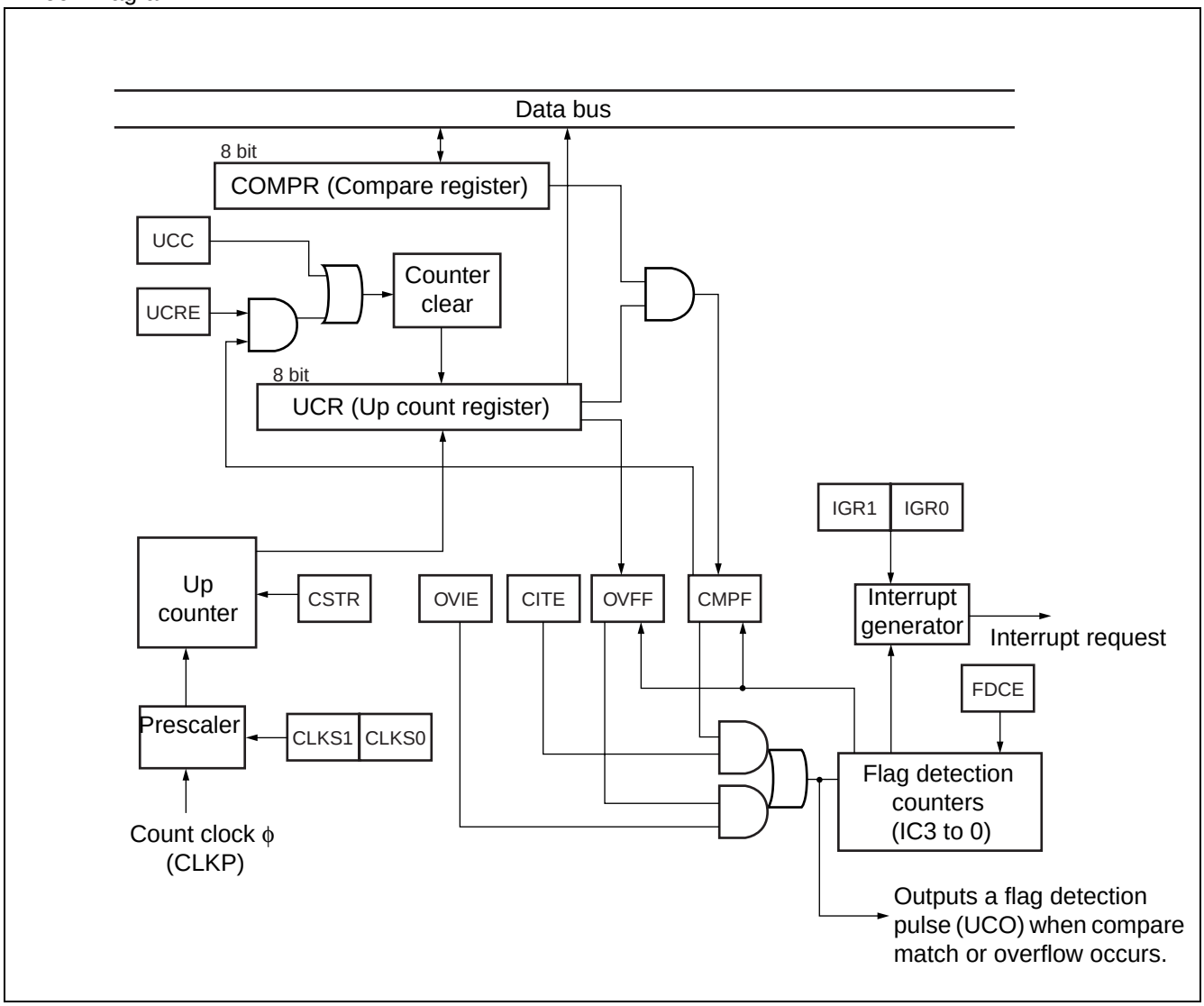
6. 8-Bit Up Counter

The 8-bit up counter unit consists of an 8-bit up counter, 8-bit compare register, and their respective control circuits.
The MB91340/MB91V340 has one 8-bit up counter channel.

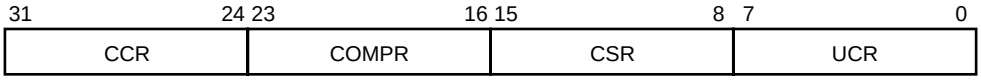
• 8-Bit Up Counter Features

- The 8-bit count register can count in the range (0)d to (256)d.
- The count clock can be selected from four internal clocks (counts on the rising edge).
- Includes a compare function for performing up-counting.
- The interrupt generation frequency for compare match and overflow can be controlled.
- The compare match and overflow interrupt can be enabled and disabled independently.
- A clock can be generated by detecting the flag when a compare match or overflow occurs.

• Block Diagram



• Register List



Up count register (UCR)

bit

	7	6	5	4	3	2	1	0
Address : 0000D3H	D07	D06	D05	D04	D03	D02	D01	D00

Compare register (COMPR)

bit

	7	6	5	4	3	2	1	0
Address : 0000D1H	D07	D06	D05	D04	D03	D02	D01	D00

Counter status register (CSR)

bit

	7	6	5	4	3	2	1	0
Address : 0000D2H	CITE	OVIE	CMPF	OVFF	IC3	IC2	IC1	IC0

Counter control register (CCR)

bit

	7	6	5	4	3	2	1	0
Address : 0000D0H	CSTR	CLKS1	CLKS0	UCRE	UCC	FDCE	IGR1	IGR0

7. 8/16-Bit Up/Down Counter/Timer

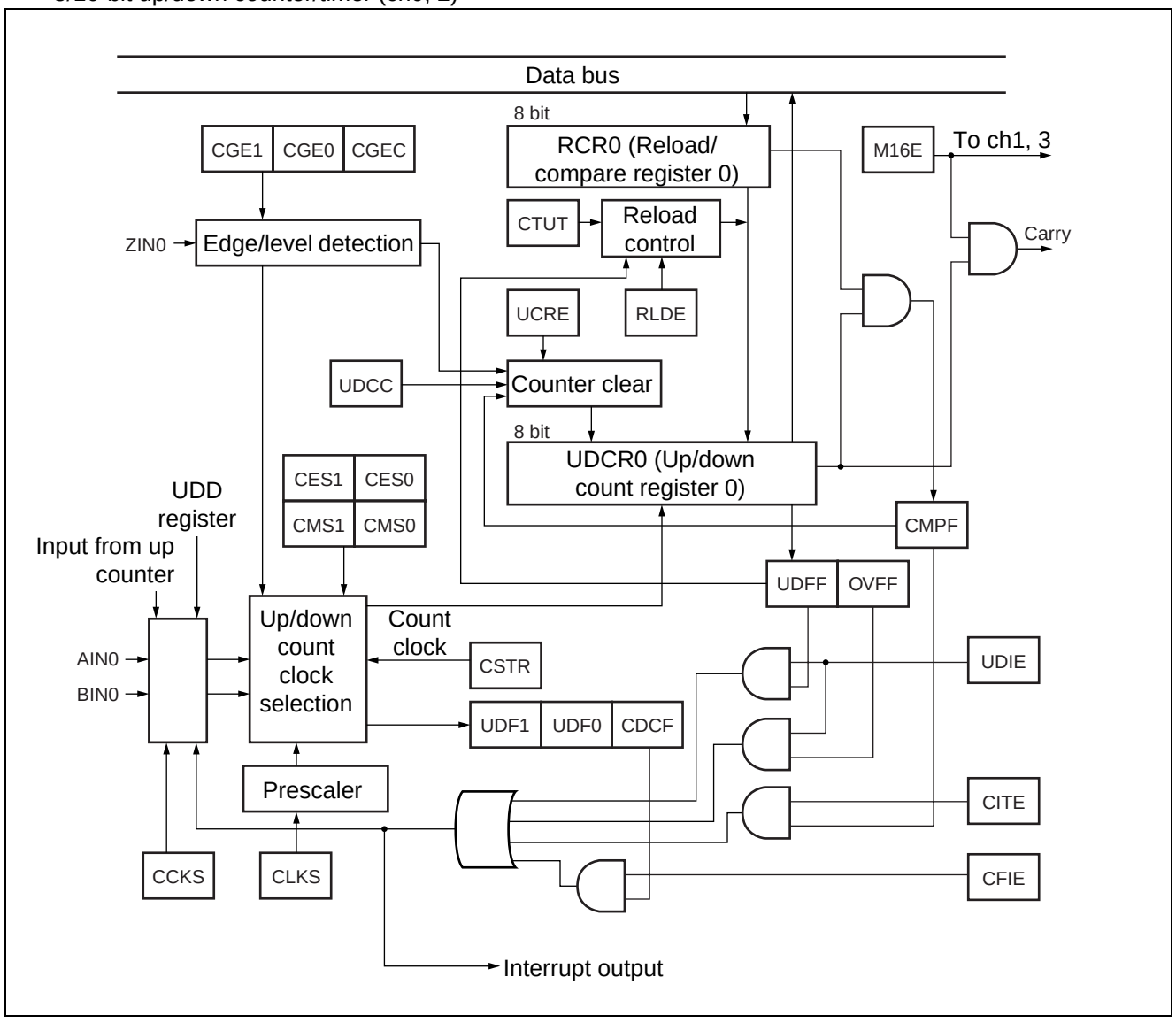
The 8/16-bit up/down counter/timer consists of an six event inputs, two 8-bit up/down counters, two 8-bit reload/compare registers, and their various control circuits.
The MB91340/MB91V340 have four 8-bit up/down counter/timer channels.

• 8-Bit Up/Down Counter/Timer Features

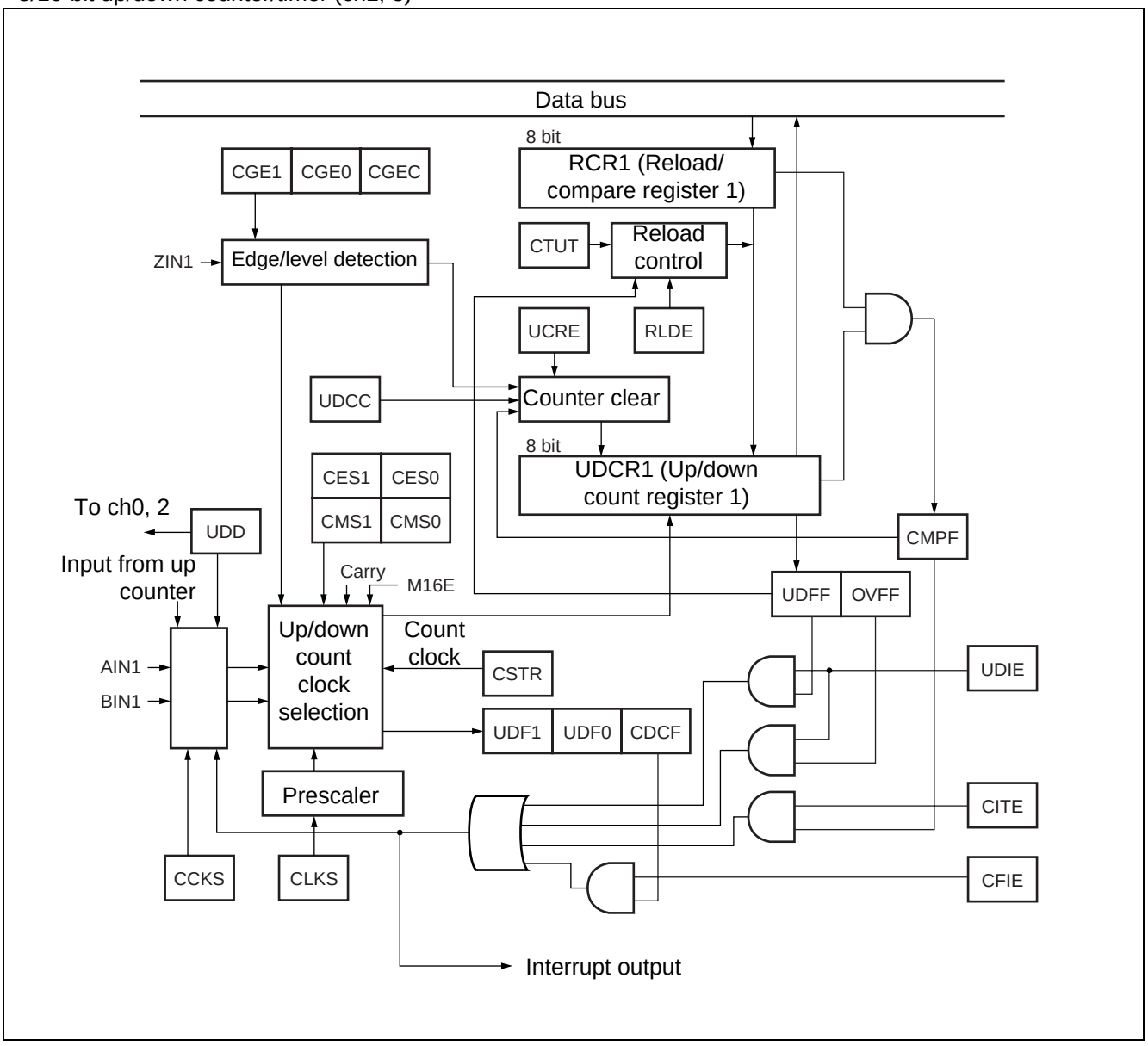
Parameter	Function
Operation mode	• 8-bit 2 channel modes • 16-bit 1 channel mode
Count mode	Can select four different count modes. • Timer mode • Up/down count mode • Phase difference count mode (multiply by 2) • Phase difference count mode (multiply by 4)
Count clock (In timer mode)	Can select two different count modes. • ϕ/2 (ϕ : Machine clock frequency) • ϕ/8
Edge selection for detection (In up/down count mode)	Can select which edge to detect on the external pin input signal. • Edge detection disabled • Detect falling edge • Detect rising edge • Detect both rising and falling edges
Function of ZIN pin	Can select two different functions. • Counter clear function • Gate function
Compare/reload function	Compare and reload functions are provided and these can be used individually or together. • Compare function (Interrupt request generation and counter clear by compare match) • Reload function (Interrupt request generation and reload by underflow) • Compare/reload function (Interrupt request generation and counter clear by compare match, interrupt request generation and reload by underflow) • Compare/reload disabled
Count derection	• The direction of the most recent count operation can be determined from the count direction flag.
Interrupt request	Can generate interrupt request • Compare match • Underflow or overflow • Count direction change

Note : Phase difference count mode is suitable for use as a motor or similar encorder counter. High precision rotational position and speed counters can be implemented easily by inputting the A, B and Z phase outputs from the encoder.

- Block Diagram
  - 8/16-bit up/down counter/timer (ch0, 2)



• 8/16-bit up/down counter/timer (ch1, 3)



• Register List

31 24	23 16	15 8	7 0
RCR1	RCR0	UDCR1	UDCR0
CCRH0	CCRL0	—	CSR0
CCRH1	CCRL1	—	CSR1
RCR3	RCR2	UDCR3	UDCR2
CCRH2	CCRL2	—	CSR2
CCRH3	CCRL3	—	CSR3

Up/down count register (UDCR)

• Up/down count register ch0 (UDCR0)

Address : 0000B3H

bit	7	6	5	4	3	2	1	0
	D07	D06	D05	D04	D03	D02	D01	D00

• Up/down count register ch1 (UDCR1)

Address : 0000B2H

bit	15	14	13	12	11	10	9	8
	D15	D14	D13	D12	D11	D10	D09	D08

• Up/down count register ch2 (UDCR2)

Address : 0000BFH

bit	7	6	5	4	3	2	1	0
	D07	D06	D05	D04	D03	D02	D01	D00

• Up/down count register ch3 (UDCR3)

Address : 0000BEH

bit	15	14	13	12	11	10	9	8
	D15	D14	D13	D12	D11	D10	D09	D08

Reload/compare register (RCR)

• Reload/compare register ch0 (RCR0)

Address : 0000B1H

bit	7	6	5	4	3	2	1	0
	D07	D06	D05	D04	D03	D02	D01	D00

• Reload/compare register ch1 (RCR1)

Address : 0000B0H

bit	15	14	13	12	11	10	9	8
	D15	D14	D13	D12	D11	D10	D09	D08

• Reload/compare register ch2 (RCR2)

Address : 0000BDH

bit	7	6	5	4	3	2	1	0
	D07	D06	D05	D04	D03	D02	D01	D00

• Reload/compare register ch3 (RCR3)

Address : 0000BCH

bit	15	14	13	12	11	10	9	8
	D15	D14	D13	D12	D11	D10	D09	D08

(Continued)

(Continued)

Counter status register (CSR)

- Counter status register ch0, 1 (CSR0, 1)

Address : 0000B7H / 0000BBH

bit	7	6	5	4	3	2	1	0
	CSTR	CITE	UDIE	CMPF	OVFF	UDFF	UDF1	UDF0

- Counter status register ch2, 3 (CSR2, 3)

Address : 0000C3H / 0000C7H

bit	7	6	5	4	3	2	1	0
	CSTR	CITE	UDIE	CMPF	OVFF	UDFF	UDF1	UDF0

Counter control register (CCRL)

- Counter control register ch0, 1 (CCRL0, 1)

Address : 0000B5H / 0000B9H

bit	7	6	5	4	3	2	1	0
	CCKS	CTUT	UCRE	RLDE	UDCC	CGSC	CGE1	CGE0

- Counter control register ch2, 3 (CCRL2, 3)

Address : 0000C1H / 0000C5H

bit	7	6	5	4	3	2	1	0
	CCKS	CTUT	UCRE	RLDE	UDCC	CGSC	CGE1	CGE0

Counter control register (CCRH)

- Counter control register ch0 (CCRH0)

Address : 0000B4H

bit	15	14	13	12	11	10	9	8
	M16E	CDCF	CFIE	CLKS	CMS1	CMS0	CES1	CES0

- Counter control register ch1 (CCRH1)

Address : 0000B8H

bit	15	14	13	12	11	10	9	8
	UDD	CDCF	CFIE	CLKS	CMS1	CMS0	CES1	CES0

- Counter control register ch2 (CCRH2)

Address : 0000C0H

bit	15	14	13	12	11	10	9	8
	M16E	CDCF	CFIE	CLKS	CMS1	CMS0	CES1	CES0

- Counter control register ch3 (CCRH3)

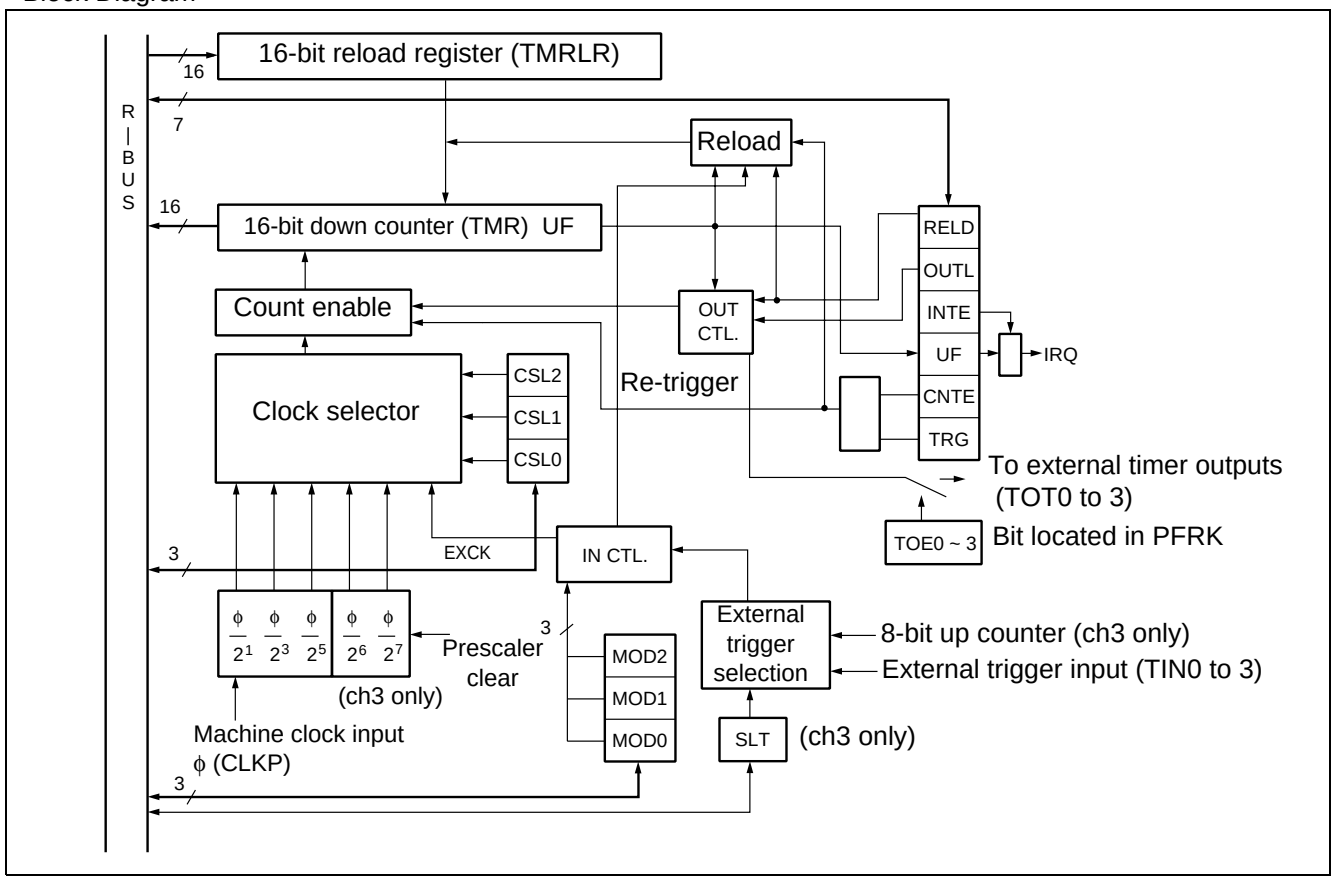
Address : 0000C4H

bit	15	14	13	12	11	10	9	8
	UDD	CDCF	CFIE	CLKS	CMS1	CMS0	CES1	CES0

8. 16-Bit Reload Timer

The 16-bit timer consists of a 16-bit down-counter, 16-bit reload register, prescaler for generating the internal count clock, and a control register.
The clock source can be selected from three internal clock signals (machine clock divided by 2, 8, or 32 - ch3 also supports machine clock divided by 64 or 128) or the external event input.
The interrupt can be used to initiate DMA transfer.
The MB91340/MB91V340 has four 16-bit reload timer channels.

• Block Diagram



• Register List

• Control status register (TMCSR)

15	14	13	12	11	10	9	8
—	—	SLT	CSL2	CSL1	CSL0	MOD2	MOD1

7	6	5	4	3	2	1	0
MOD0	—	OUTL	RELD	INTE	UF	CNTE	TRG

• 16-bit timer register (TMR)

15	0

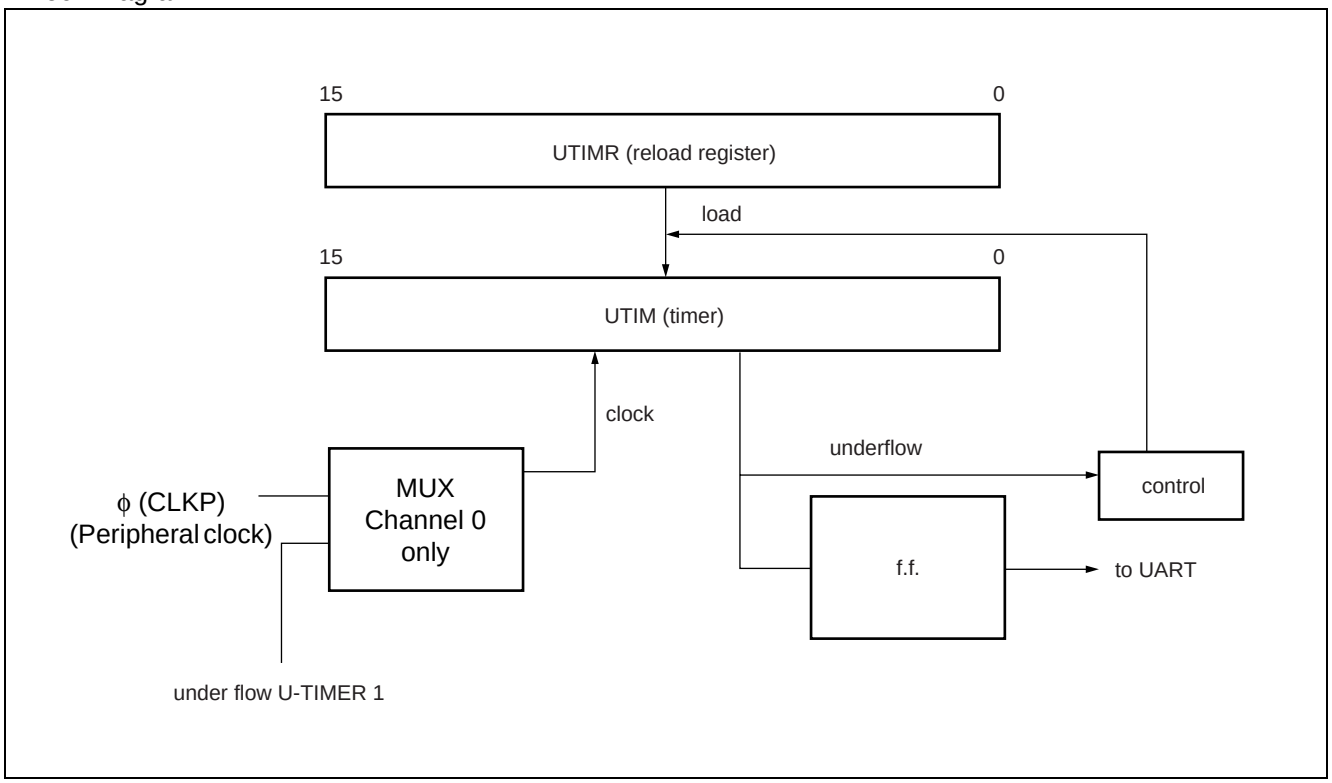
• 16-bit reload register (TMRLR)

15	0

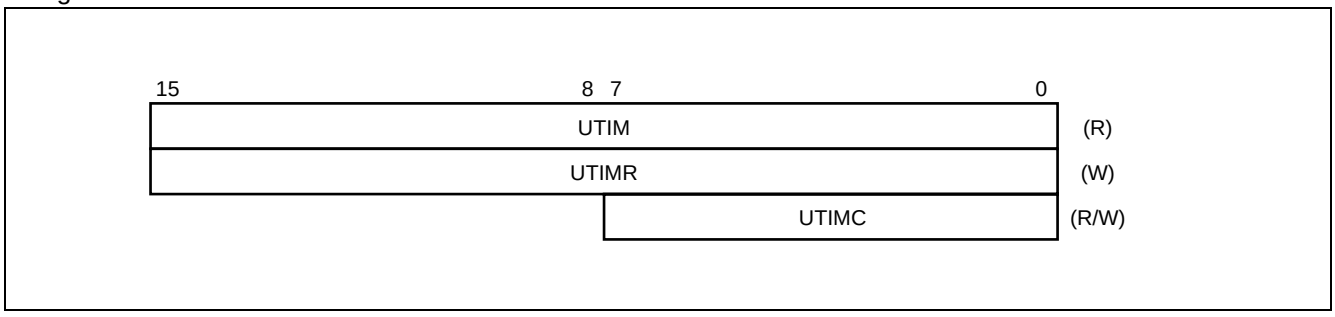
9. U-TIMER (16 bit timer for UART baud rate generation)

The U-TIMER is a 16-bit timer used to generate the baud rate for the UART. Any desired baud rate can be set using the combination of the chip operating frequency and U-TIMER reload value.
The U-TIMER can also be used as an interval timer by generating an interrupt from a count underflow event.
The MB91340/MB91V340 has three U-TIMER channels. When used as an interval timer, two U-TIMER channels can be connected in cascade for a maximum count interval of up to $2^{32} \times \phi$.
Cascade connection is only available for channel 0 and channel 1 or channel 0 and channel 2.

• Block Diagram



• Register List



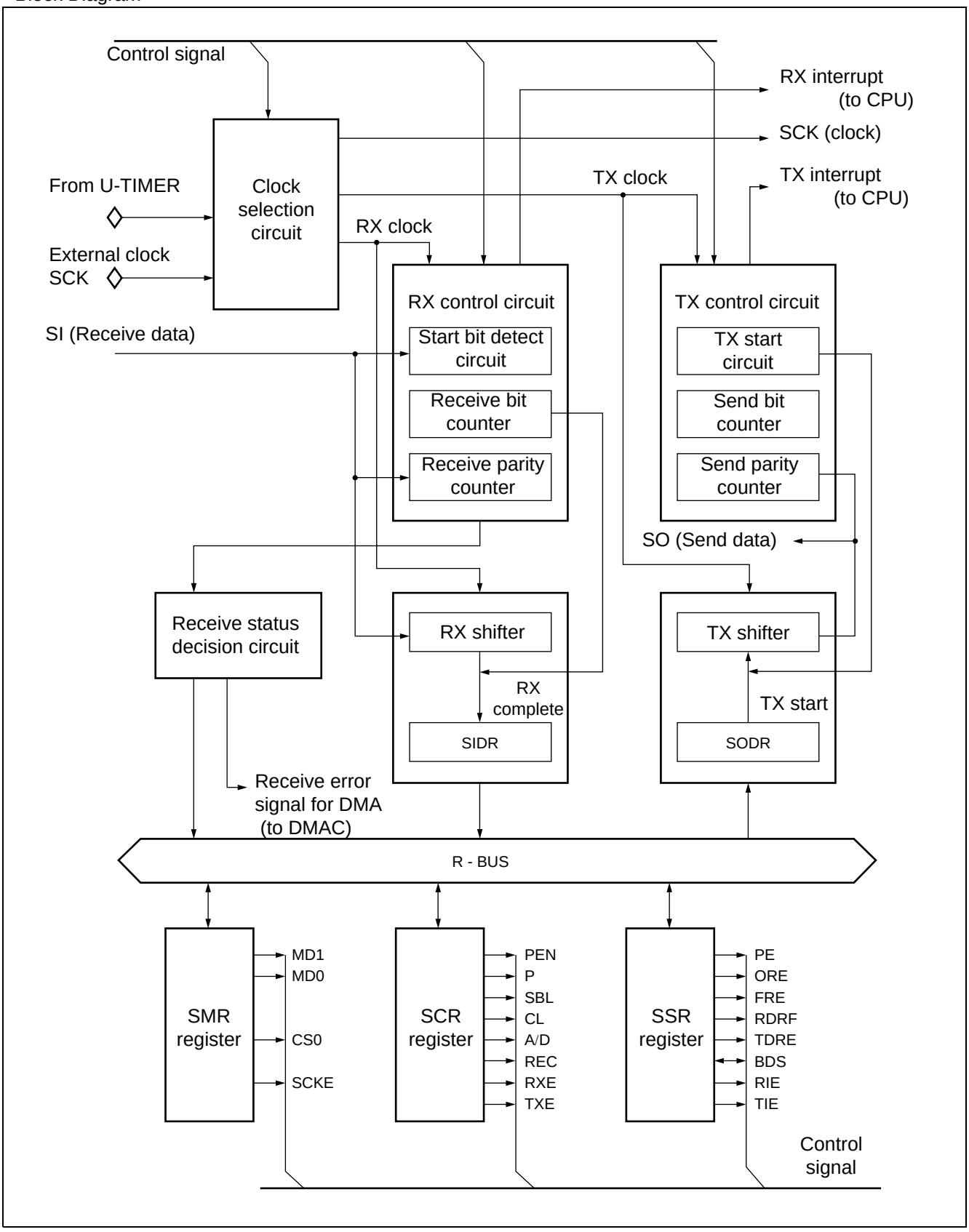
10. UART

The UART is a serial I/O port for asynchronous (start-stop synchronized) or CLK synchronized transmission. The MB91340/MB91V340 has three UART channels.

● UART Features

- Full duplex double buffer
- Asynchronous (start-stop synchronized) or CLK synchronized transmission
- Supports multi-processor mode
- Fully programmable baud rate
  The internal timer can be set to any desired baud rate (see U-TIMER description)
- Variable baud rate can be input from an external clock.
- Error detection functions (parity, framing, overrun)
- Transmission signal format is NRZ
- The interrupt can be used to initiate DMA transfer.
- The DMAC interrupt can be cleared by writing to the DRCL register.

• Block Diagram



• Register List

15	8	7	0	
SCR		SMR		(R/W)
SSR		SIDR (R)/SODR (W)		(R/W)
DRCL				(W)
8 bit		8 bit		

Register List Serial output register (SIDR/SODR)

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Serial status register (SSR)

7	6	5	4	3	2	1	0
PE	ORE	FRE	RDRF	TDRE	BDS	RIE	TIE

Serial mode register (SMR)

7	6	5	4	3	2	1	0
MD1	MD0	—	—	CS0	—	SCKE	—

Serial control register (SCR)

7	6	5	4	3	2	1	0
PEN	P	SBL	CL	A/D	REC	RXE	TXE

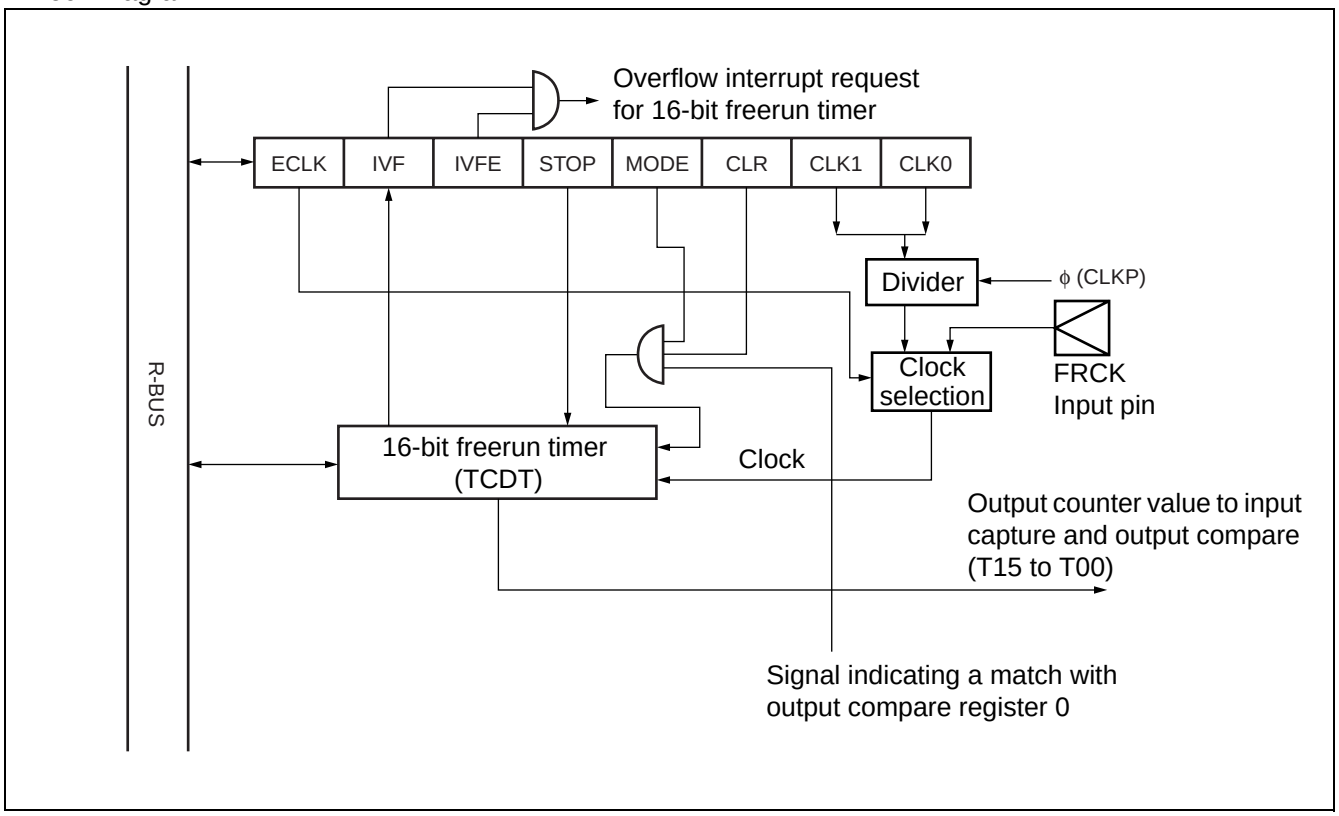
(DRCL)

7	6	5	4	3	2	1	0
—	—	—	—	—	—	—	—

11. 16-Bit Freerun Timer

The 16-bit freerun timer consist of a 16-bit up counter and control status register.
The count value from the 16-bit freerun timer is used as the base time for the output compare and input capture.
The count clock can be selected from four different clocks.
An interrupt can be generated when a counter overflow occurs.
A mode setting is available that initializes the counter when a match with the value in compare register 0 (in the output compare unit) occurs.

• Block Diagram



• Register List (upper)

Timer data register

15	14	13	12	11	10	9	8
T15	T14	T13	T12	T11	T10	T09	T08

Timer data register (lower) (TCDT)

7	6	5	4	3	2	1	0
T07	T06	T05	T04	T03	T02	T01	T00

Timer control status register (lower) (TCCS)

7	6	5	4	3	2	1	0
ECLK	IVF	IVFE	STOP	MODE	CLR	CLK1	CLK0

12. Input Capture

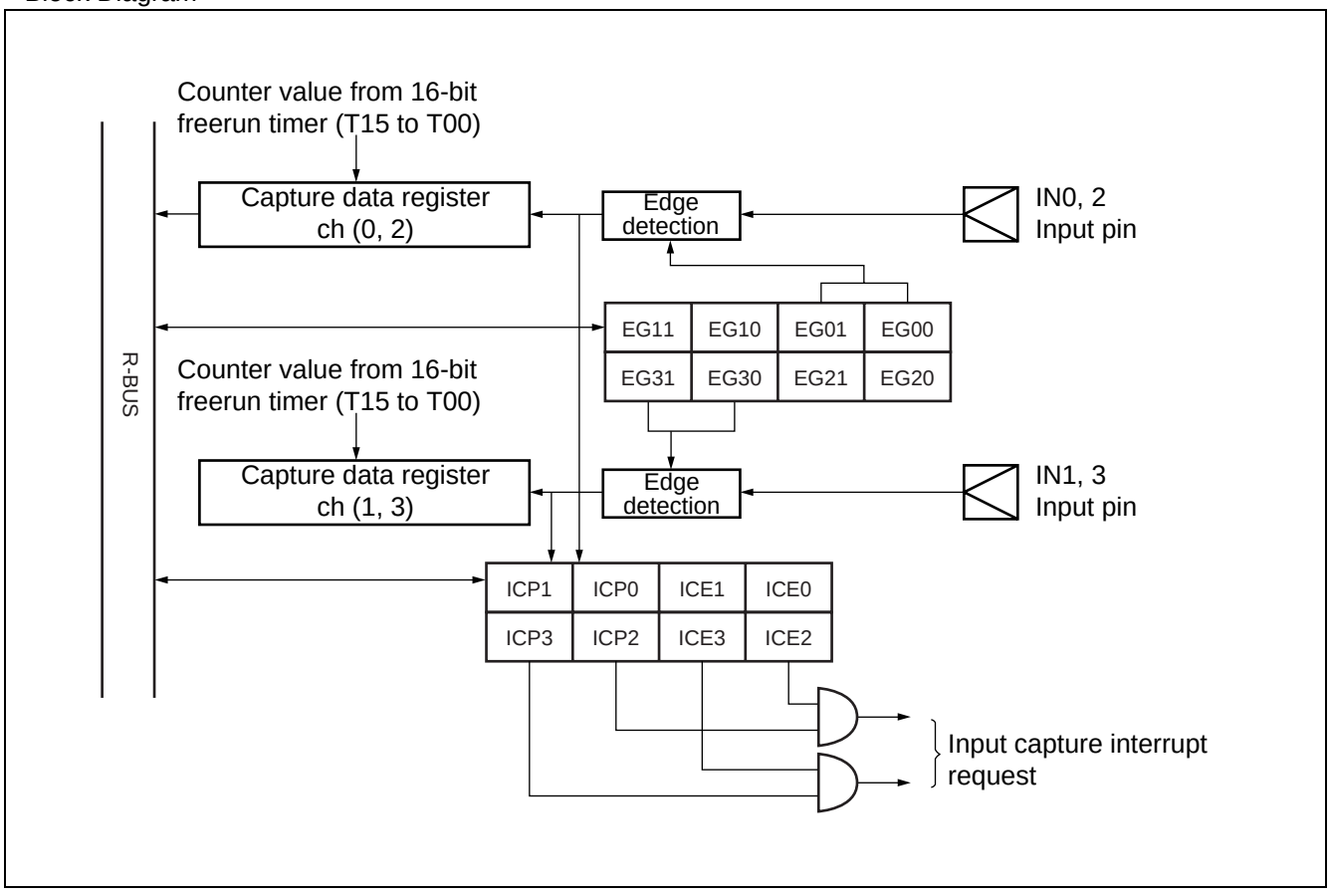
The input capture unit detects rising edges, falling edges, or either edge on the signal input from an external pin and saves the value of the 16-bit freerun timer at that time to a register. The unit can also generate an interrupt when an edge is detected.
The input capture consists of an input capture data register and control register.
Each input capture channel has its own external input pin.

The active edge on the external input can be selected from the following three options :

- Riding edge
- Falling edge
- Either edge

The input capture can generate an interrupt when an active edge is detected.
The MB91340/MB91V340 has four input capture channels.

• Block Diagram



• Register List

Input capture data register (upper) (IPCP)

15	14	13	12	11	10	9	8
CP15	CP14	CP13	CP12	CP11	CP10	CP09	CP08

Input capture data register (lower) (IPCP)

7	6	5	4	3	2	1	0
CP07	CP06	CP05	CP04	CP03	CP02	CP01	CP00

Capture control register (ICS23)

7	6	5	4	3	2	1	0
ICP3	ICP2	ICE3	ICE2	EG31	EG30	EG21	EG20

Capture control register (ICS01)

7	6	5	4	3	2	1	0
ICP1	ICP0	ICE1	ICE0	EG11	EG10	EG01	EG00

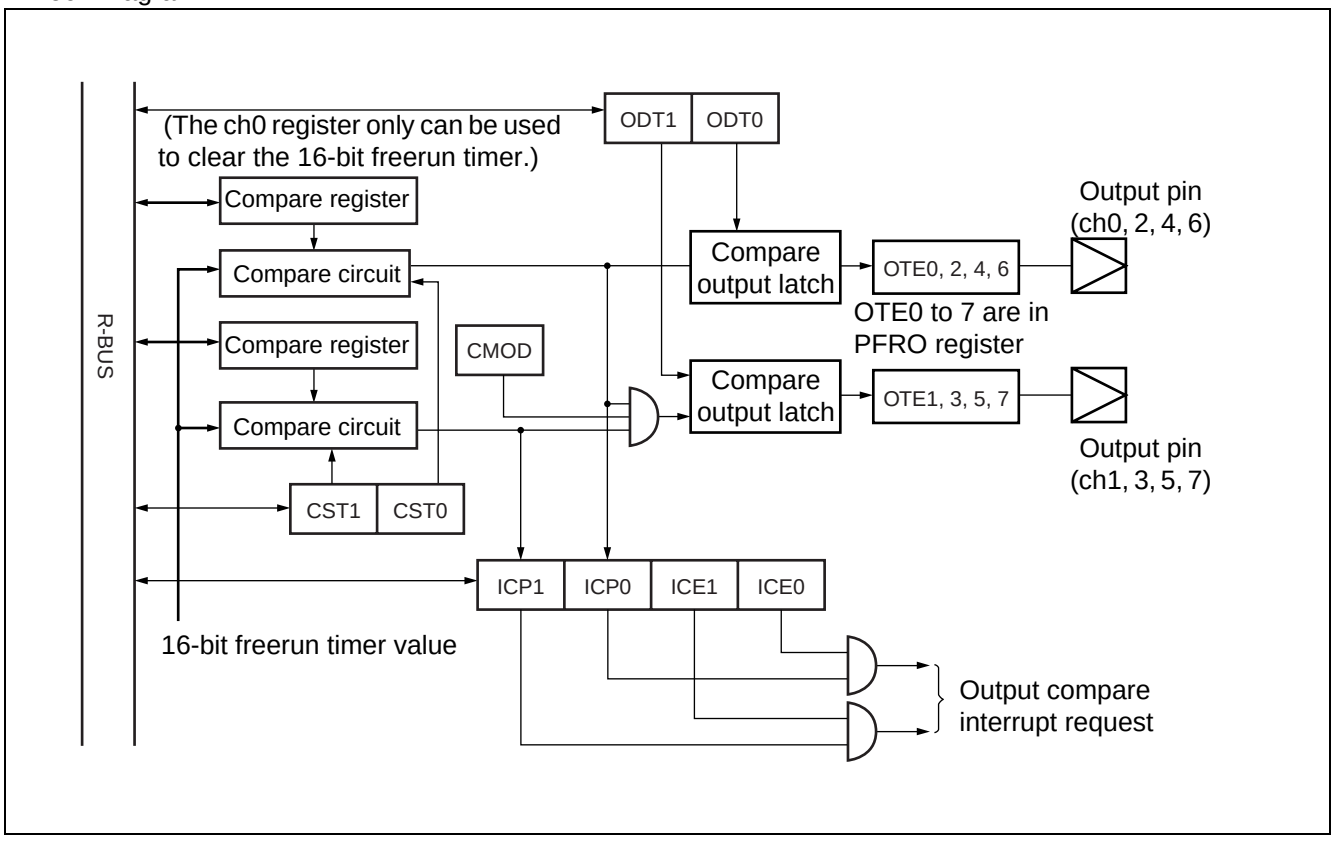
13. Output Compare

The output compare unit consists of a 16-bit compare register, compare output latch, and control register. The unit can toggle the output level and generate an interrupt when a match occurs between the 16-bit freerun timer and compare register.
The MB91340/MB91V340 has eight output compare channels.

Output Compare Features

- The eight compare registers operate independently. Each compare register has its own output pin and interrupt flag.
- Two compare registers can be used together to control an output pin. The output pin is toggled by both registers.
- The initial value of each output pin can be specified.
- An interrupt is generated when a compare match occurs.
- The ch0 compare register can be used to clear the 16-bit freerun timer.

• Block Diagram



- Register List

Compare register (upper) (OCCP)

15	14	13	12	11	10	9	8
C15	C14	C13	C12	C11	C10	C09	C08

Compare register (lower) (OCCP)

7	6	5	4	3	2	1	0
C07	C06	C05	C04	C03	C02	C01	C00

Output control register (upper) (OCS)

15	14	13	12	11	10	9	8
—	—	—	CMOD	—	—	OTD1	OTD0

Output control register (lower) (OCS)

7	6	5	4	3	2	1	0
ICP1	ICP0	ICE1	ICE0	—	—	CST1	CST0

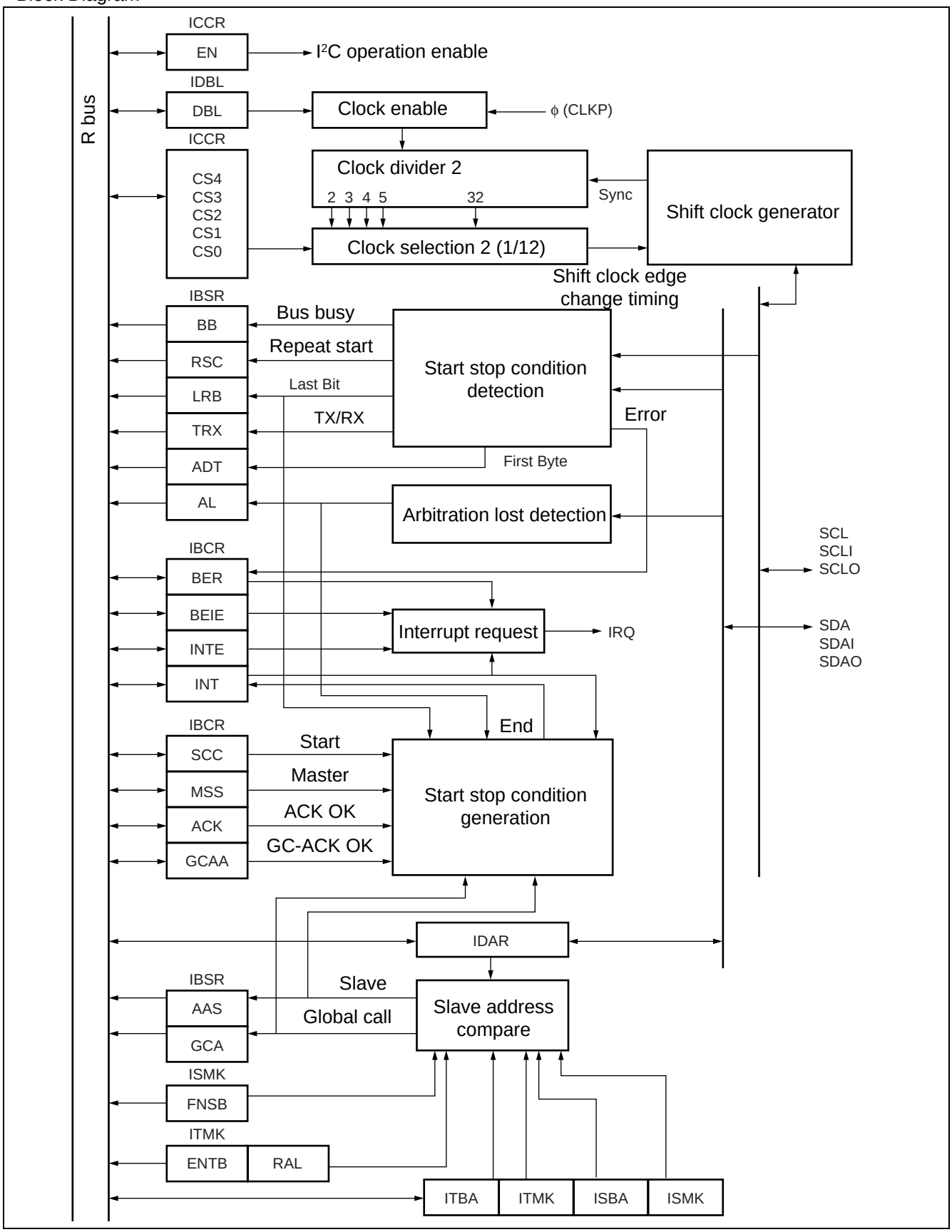
14. I²C Interface

The I²C interface is a serial port that supports the Inter IC Bus protocol. It can operate as a master or slave device on the I²C bus.

I²C Interface Features

- Master/slave send and receive
- Arbitration function
- Clock synchronization function
- Slave address and general call address detection function
- Transmission direction detection function
- Repeated "START" condition generation and detection function
- Bus error detection function
- 10-bit or 7-bit slave address
- Slave address receive acknowledge control when in master mode
- Supports compound slave addresses
- Can generate an interrupt on transmission or bus error
- Supports standard mode (100 Kbps Max) and high-speed mode (400 Kbps Max)
- Both "standard mode" and "terminal split mode" external pins provided.

• Block Diagram



• Register List

• Bus control register (IBCR)

Address : 000094H

15	14	13	12	11	10	9	8
BER	BEIE	SCC	MSS	ACK	GCAA	INTE	INT
R/W	R/W	W	R/W	R/W	R/W	R/W	R/W
Initial value→ 0	0	0	0	0	0	0	0

• Bus status register (IBSR)

Address : 000095H

7	6	5	4	3	2	1	0
BB	RSC	AL	LRB	TRX	AAS	GCA	ADT
R	R	R	R	R	R	R	R
Initial value→ 0	0	0	0	0	0	0	0

• 10-bit slave address register (ITBA)

Address : 000096H

15	14	13	12	11	10	9	8
—	—	—	—	—	—	TA9	TA8
—	—	—	—	—	—	R/W	R/W
Initial value→ —	—	—	—	—	—	0	0

Address : 000097H

7	6	5	4	3	2	1	0
TA7	TA6	TA5	TA4	TA3	TA2	TA1	TA0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value→ 0	0	0	0	0	0	0	0

• 10-bit slave address mask register (ITMK)

Address : 000098H

15	14	13	12	11	10	9	8
ENTB	RAL	—	—	—	—	TM9	TM8
R/W	R	—	—	—	—	R/W	R/W
Initial value→ 0	0	—	—	—	—	1	1

Address : 000099H

7	6	5	4	3	2	1	0
TM7	TM6	TM5	TM4	TM3	TM2	TM1	TM0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value→ 1	1	1	1	1	1	1	1

• 7-bit slave address register (ISBA)

Address : 00009BH

7	6	5	4	3	2	1	0
—	SA6	SA5	SA4	SA3	SA2	SA1	SA0
—	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value→ —	0	0	0	0	0	0	0

• 7-bit slave address mask register (ISMK)

Address : 00009AH

15	14	13	12	11	10	9	8
ENSB	SM6	SM5	SM4	SM3	SM2	SM1	SM0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value→ 0	1	1	1	1	1	1	1

(Continued)

(Continued)

- Data register (IDAR)

Address : 00009D$_H$

	7	6	5	4	3	2	1	0
	D7	D6	D5	D4	D3	D2	D1	D0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value→	0	0	0	0	0	0	0	0

- Clock control register (ICCR)

Address : 00009E$_H$

	15	14	13	12	11	10	9	8
	TEST	—	EN	CS4	CS3	CS2	CS1	CS0
	W	—	R/W	R/W	R/W	R/W	R/W	R/W
Initial value→	0	—	0	1	1	1	1	1

- Clock disable register (IDBL)

Address : 00009F$_H$

	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	DBL
	—	—	—	—	—	—	—	R/W
Initial value→	—	—	—	—	—	—	—	0

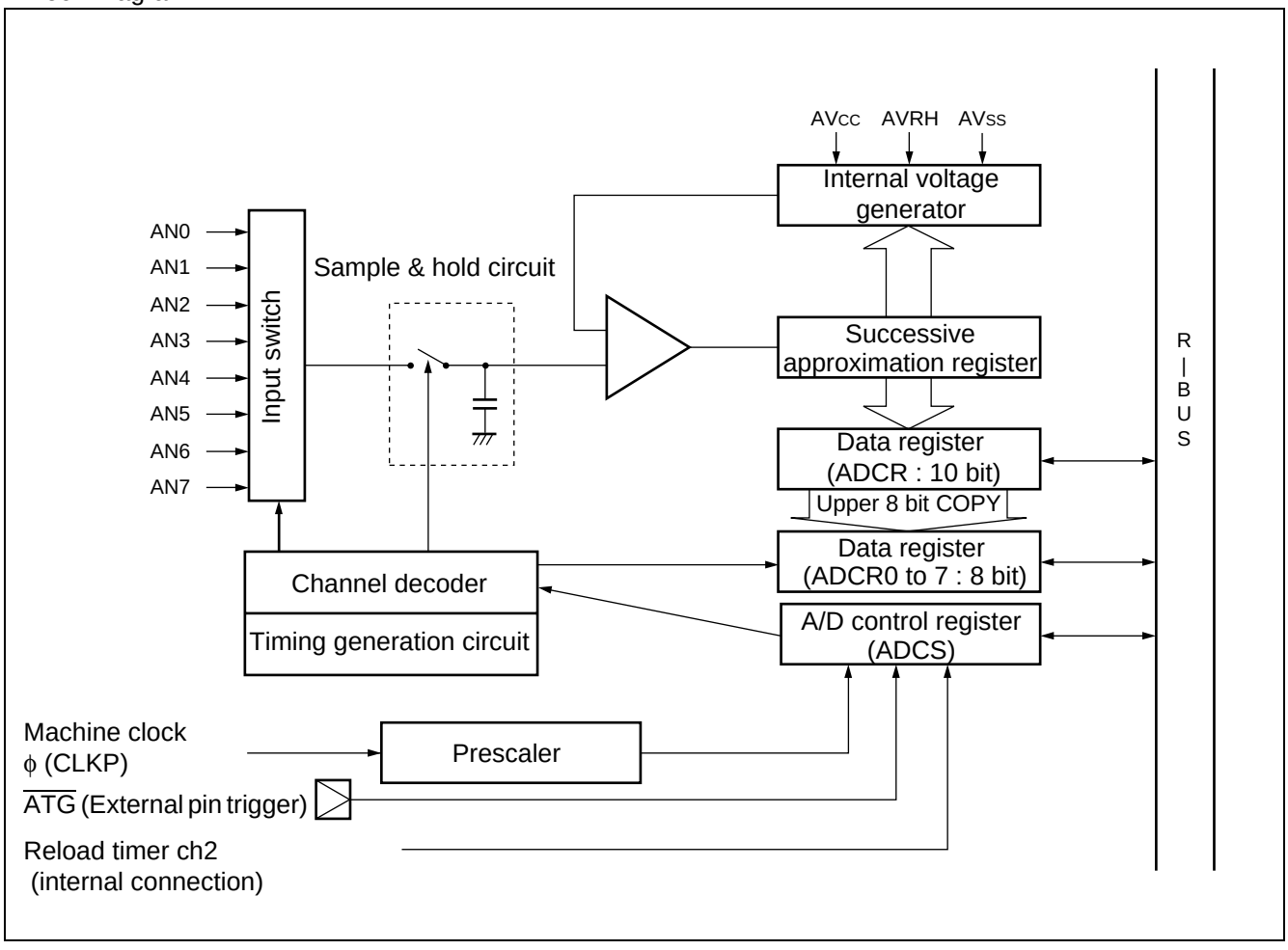
15. A/D Converter (Successive Approximation Type)

The A/D converter converts analog input voltages to digital values.

• A/D Converter Features

- Minimum conversion time 5.4 µs/ch (for machine clock = 33 MHz-CLKP)
- Internal sample & hold circuit
- Resolution = 10-bit (8-bit accuracy)
- 8 program-selectable analog inputs
  Single conversion mode : Convert 1 specified channel
  Scan conversion mode : ontinuous conversion of multiple channels. Conversion can be specified for up to 8 channels.
- Single, continuous, and stop conversion operation is supported.
  Single mode: Convert specified channel then stop.
  Continuous conversion mode: Perform continuous conversion for the selected channel.
  Stop conversion mode: Perform conversion for one channel, then wait for the next activation trigger (synchronizes the conversion start timing)
- DMA transfer can be initiated by an interrupt.
- Selectable conversion activation trigger: Software, external trigger (falling edge), or reload timer (rising edge)

• Block Diagram



• Register List

Control status register (ADCS)

bit	15	14	13	12	11	10	9	8
	BUSY	INT	INTE	CRF	STS1	STS0	STRT	—

bit	7	6	5	4	3	2	1	0
	MD1	MD0	ANS2	ANS1	ANS0	ANE2	ANE1	ANE0

Data register (ADCR)

bit	15	14	13	12	11	10	9	8
	—	—	—	—	—	—	9	8

bit	7	6	5	4	3	2	1	0
	7	6	5	4	3	2	1	0

Conversion result register (ADCR0 to 7)

bit	7	6	5	4	3	2	1	0
	7	6	5	4	3	2	1	0

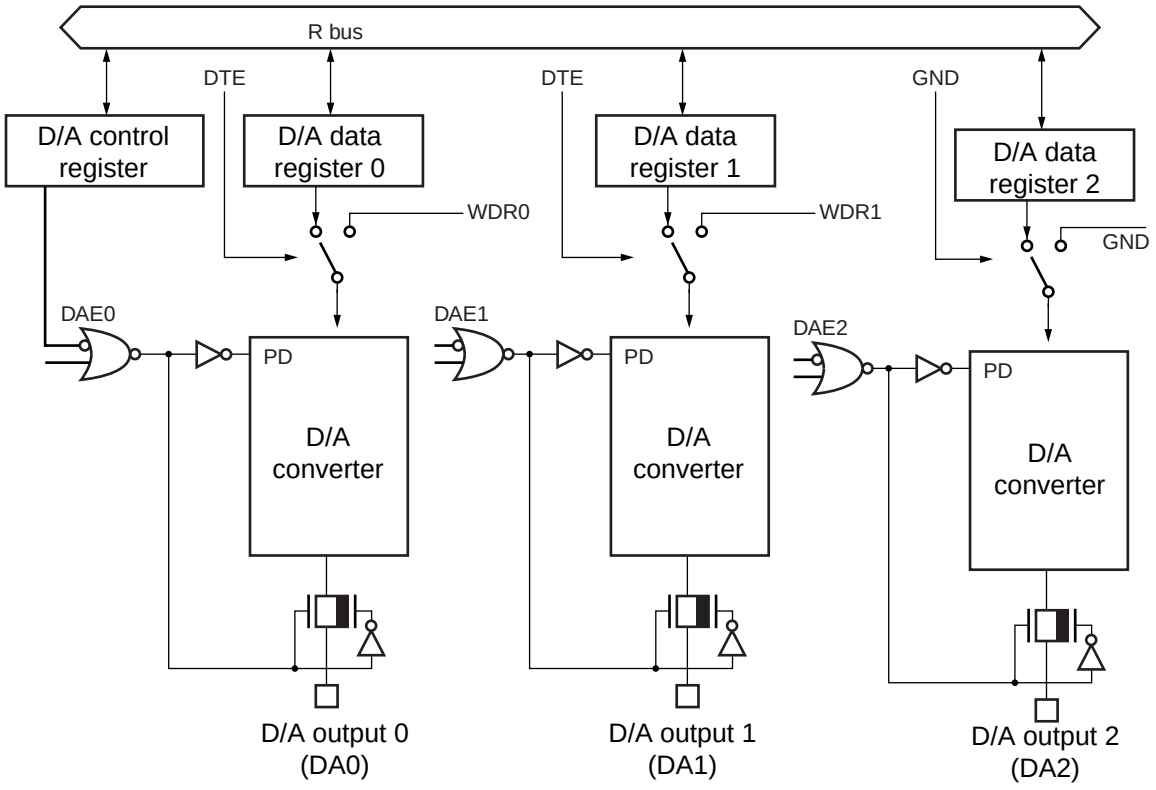
16. 8-Bit D/A Converter

The 8-bit D/A converter consists of three D/A converter channels with 8-bit resolution and independent outputs controlled by the D/A control register.

• 8-bit D/A Converter Features

- Includes power-down function
- Operation : Max 200 kSPS
- Power consumption 2.3 mW (Typ)
- 3.3 V interface

• Block Diagram



• Register List

D/A data register 0 to 2 (DADR0 to 2)

bit	7	6	5	4	3	2	1	0
	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0

D/A control register 0 to 2 (DACR0 to 2)

bit	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	DAE

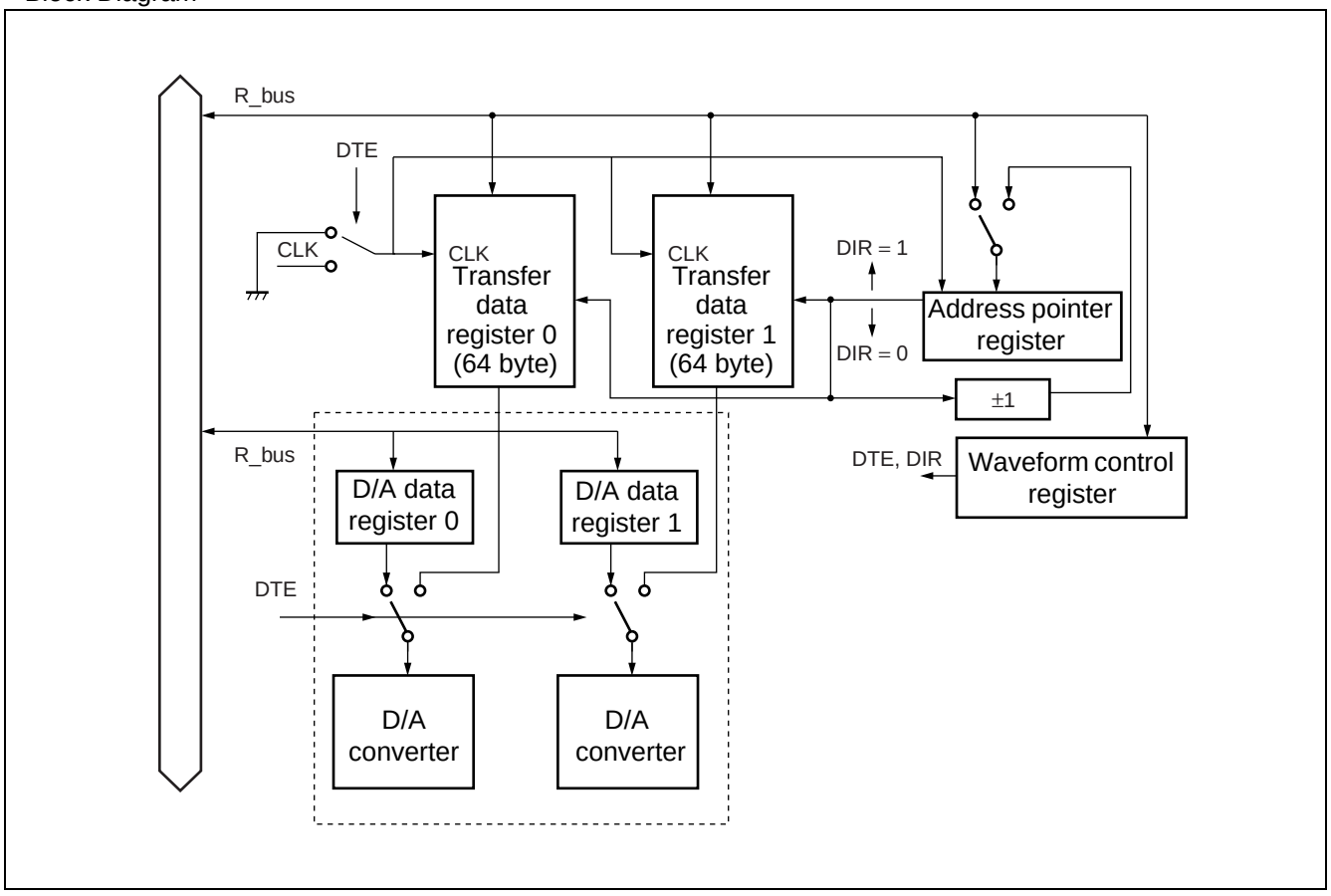
17. Waveform Data Transfer

The waveform data transfer consists of two 64 byte registers used to transfer data to their corresponding D/A converters.

• Waveform Data Transfer Features

- The pulse output of the 8-bit up counter is used as the transfer clock.
- The speed of transfer to the D/A converter can be controlled by changing the frequency of the 8-bit up counter pulse output.
- Forward or reverse direction can be specified.

• Block Diagram



• Register List

Waveform control register (WCR)

7	6	5	4	3	2	1	0
DTE	DIR	EA5	EA4	EA3	EA2	EA1	EA0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address pointer register (APR)

7	6	5	4	3	2	1	0
—	AI	AP5	AP4	AP3	AP2	AP1	AP0
—	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Waveform data register (WDR1)

15	14	13	12	11	10	9	8
WD17	WD16	WD15	WD14	WD13	WD12	WD11	WD10
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Waveform data register (WDR0)

7	6	5	4	3	2	1	0
WD07	WD06	WD05	WD04	WD03	WD02	WD01	WD00

18. Version Register

The version register is a 4-bit internal register.
The version register can be read to determine the device version.

- Register List

Version register (VERR)

7	6	5	4	3	2	1	0
—	—	—	—	VR3	VR2	VR1	VR0

19. DMAC (DMA Controller)

The DMA controller is used to perform DMA (direct memory access) transfer on the FR series device.
Using DMA transfer under the control of the DMA controller improves system performance by enabling data to be transferred at high speed independently of the CPU.

• Hardware Configuration

- 5 independent DMA channels × 5 ch
- 5 independent access control circuits
- 32-bit address register (Supports reloading : 2 per channel)
- 16-bit transfer count register (Supports reloading : 1 per channel)
- 4-bit block count register (1 per channel)
- External transfer request input pins : DREQ0, DREQ1, DREQ2 (ch0, 1, 2 only)
- External transfer request acknowledge output pins : DACK0, DACK1, DACK2 (ch0, 1, 2 only)
- DMA completion output pins : DEOP0, DEOP1, DEOP2 (ch0, 1, 2 only)
- fly-by transfer (memory to I/O , I/O to memory) (ch0, 1, 2 only)
- Two-cycle transfer

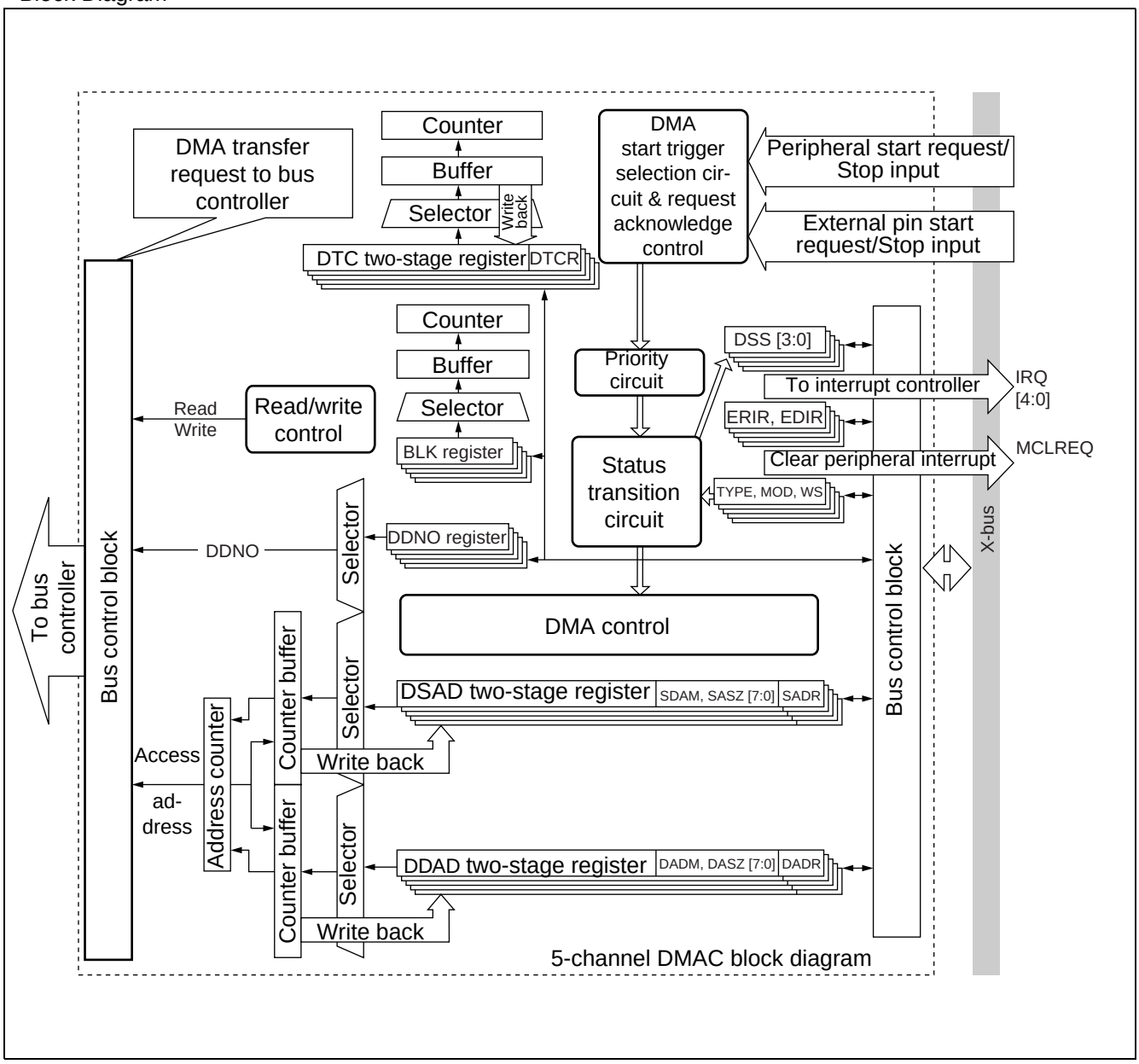
• Main Functions of the DMA Controller

- Supports independent data transfer for multiple channels (5 channels)

(1) Priority order (ch.0 > ch.1 > ch.2 > ch.3 > ch.4)
(2) Order can be reversed for ch0 and ch1
(3) DMAC activation triggers
- Input from dedicated external pin (edge detection/level detection, ch0,1,2 only)
- Request from internal peripheral (shared interrupt request, including external interrupts)
- Software request (register write)

(4) Transfer modes
- Demand transfer, burst transfer, step transfer, or block transfer
  Addressing mode: Full 32-bit address (increment/decrement/fixed)
  (address increment can be in the range−255 to +255)
- Data type : byte/half-word/word
- Single-shot or reload operation selectable

• Block Diagram



• Register List

			(bit) 31 24 23 16 15 08 07 00
ch.0 control/status	register A	DMACA0 0000200H	
ch.0 control/status	register B	DMACB0 0000204H	
ch.1 control/status	register A	DMACA1 0000208H	
ch.1 control/status	register B	DMACB1 000020CH	
ch.2 control/status	register A	DMACA2 0000210H	
ch.2 control/status	register B	DMACB2 0000214H	
ch.3 control/status	register A	DMACA3 0000218H	
ch.3 control/status	register B	DMACB3 000021CH	
ch.4 control/status	register A	DMACA4 0000220H	
ch.4 control/status	register B	DMACB4 0000224H	

		(bit) 31 24 23 16 15 08 07 00
Overall control register	DMACR 0000240H	

ch.0 transfer source address register	DMASA0 0001000H	
ch.0 transfer destination address register	DMADA0 0001004H	
ch.1 transfer source address register	DMASA1 0001008H	
ch.1 transfer destination address register	DMADA1 000100CH	
ch.2 transfer source address register	DMASA2 0001010H	
ch.2 transfer destination address register	DMADA2 0001014H	
ch.3 transfer source address register	DMASA3 0001018H	
ch.3 transfer destination address register	DMADA3 000101CH	
ch.4 transfer source address register	DMASA4 0001020H	
ch.4 transfer destination address register	DMADA4 0001024H	

20. Clock Generation Control

The internal operating clock is generated as follows in MB91340/MB91V340.

- Source clock selection : Selects the clock source.
- Base clock generation : The base clock is generated by dividing the source clock by 2 or using a PLL.
- Generation in each internal block : The base clock is divided to generate the operating clock for each block.

• Register List

• RSRR : Reset initiation register/Watchdog timer control register

bit	15	14	13	12	11	10	9	8
address : 00000480H	INIT	HSTB	WDOG	—	SRST	—	WT1	WT0
	R	R	R	—	R	—	R/W	R/W
Initial value ($\overline{\text{INIT}}$ pin)	1	0	0	—	0	—	0	0
Initial value (INIT)	*	*	*	—	X	—	0	0
Initial value (RST)	X	X	X	—	*	—	0	0

"*" : Changes depending on what triggered the reset.
"×" : Not initialized

• STCR : Standby control register

bit	7	6	5	4	3	2	1	0
address : 00000481H	STOP	SLEEP	HIZ	SRST	OS1	OS0	—	OSCD1
	R/W	R/W	R/W	R/W	R/W	R/W	—	R/W
Initial value ($\overline{\text{INIT}}$ pin)	0	0	1	1	0	0	—	1
Initial value ($\overline{\text{HST}}$) *	0	0	1	1	1	1	—	1
Initial value (INIT)	0	0	1	1	X	X	—	1
Initial value (RST)	0	0	X	1	X	X	—	X

* : Only when asserted during a reset initiated by the $\overline{\text{INIT}}$ pin. Otherwise, same as INIT.

(Continued)

(Continued)

- TBCR : Timebase counter control register

bit	15	14	13	12	11	10	9	8
address : 00000482H	TBIF	TBIE	TBC2	TBC1	TBC0	—	SYNCR	SYNCS
Initial value (INIT)	0	0	X	X	X	—	0	0
Initial value (RST)	0	0	X	X	X	—	X	X
	R/W	R/W	R/W	R/W	R/W	—	R/W	R/W

- CTBR : Timebase counter clear register

bit	7	6	5	4	3	2	1	0
address : 00000483H	D7	D6	D5	D4	D3	D2	D1	D0
Initial value (INIT)	X	X	X	X	X	X	X	X
Initial value (RST)	X	X	X	X	X	X	X	X
	W	W	W	W	W	W	W	W

- CLKR : Clock source control register

bit	15	14	13	12	11	10	9	8
address : 00000484H	—	PLL1S2	PLL1S1	PLL1S0	—	PLL1EN	CLKS1	CLKS0
	—	R/W	R/W	R/W	—	R/W	R/W	R/W
Initial value (INIT)	—	0	0	0	—	0	0	0
Initial value (RST)	—	X	X	X	—	X	X	X

- WPR : Watchdog reset generation delay register

bit	7	6	5	4	3	2	1	0
address : 00000485H	D7	D6	D5	D4	D3	D2	D1	D0
	W	W	W	W	W	W	W	W
Initial value (INIT)	X	X	X	X	X	X	X	X
Initial value (RST)	X	X	X	X	X	X	X	X

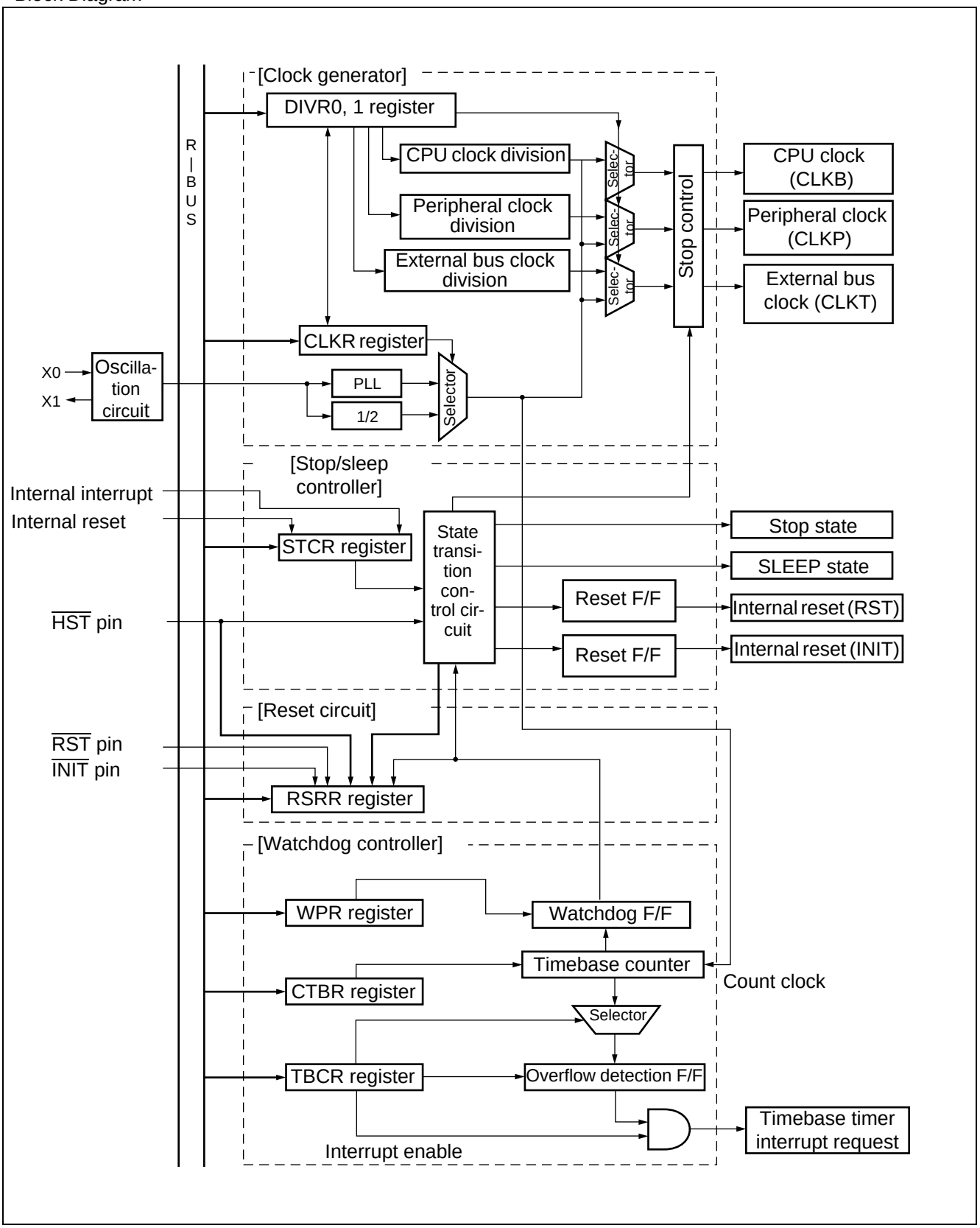
- DIVR0 : Base clock division setting register 0

bit	15	14	13	12	11	10	9	8
address : 00000486H	B3	B2	B1	B0	P3	P2	P1	P0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value (INIT)	0	0	0	0	0	0	1	1
Initial value (RST)	X	X	X	X	X	X	X	X

- DIVR1 : Base clock division setting register 1

bit	7	6	5	4	3	2	1	0
address : 00000487H	T3	T2	T1	T0	—	—	—	—
	R/W	R/W	R/W	R/W	—	—	—	—
Initial value (INIT)	0	0	0	0	—	—	—	—
Initial value (RST)	X	X	X	X	—	—	—	—

• Block Diagram



■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

(V_{SS} = DAVS = AV_{SS} = 0 V)

Parameter	Symbol	Rating		Unit	Remaeks
		Min	Max		
Supply voltage	$V_{CC}3$	V_{SS} – 0.5	V_{SS} + 4.0	V	*1
Supply voltage	$V_{CC}2$	V_{SS} – 0.5	V_{SS} + 3.0	V	*1
Analog supply voltage	DAVC	V_{SS} – 0.5	V_{SS} + 4.0	V	*2
Analog supply voltage	AV_{CC}	V_{SS} – 0.5	V_{SS} + 4.0	V	*2
Analog reference voltage	AVRH	V_{SS} – 0.5	V_{SS} + 4.0	V	*2
Input voltage	V_I	V_{SS} – 0.3	$V_{CC}3$ + 0.3	V	
Analog pin input voltage	V_{IA}	V_{SS} – 0.3	AV_{CC} + 0.3	V	
Output voltage	V_O	V_{SS} – 0.3	$V_{CC}3$ + 0.3	V	
“L” level maximum output current	I_{OL}	—	10	mA	*3
“L” level average output current	I_{OLAV}	—	8	mA	*4
“L” level total maximum output current	ΣI_{OL}	—	100	mA	
“L” level total average output current	ΣI_{OLAV}	—	50	mA	*5
“H” level maximum output current	I_{OH}	—	–10	mA	*3
“H” level average output current	I_{OHAV}	—	–4	mA	*4
“H” level total maximum output current	ΣI_{OH}	—	–50	mA	
“H” level total average output current	ΣI_{OHAV}	—	–20	mA	*5
Power consumption	P_D	—	500	mW	
Storage temperature	T_{STG}	–50	+125	°C	

*1 : $V_{CC}3$/$V_{CC}2$ must not be lower than V_{SS} – 0.5 V.

*2 : Ensure that the voltage does not exceed $V_{CC}3$ + 0.3 V, including at power-on.

*3 : The maximum output current is the peak value for a single pin.

*4 : The average output current is the average current for a single pin over a period of 100ms.

*5 : The total average output current is the average current for all pins over a period of 100ms.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Operating Conditions

(V_{SS} = DAVS = AV_{SS} = 0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Supply voltage	$V_{CC}3$	3.0	3.6	V	
	$V_{CC}2$	2.3	2.7		Normal operation
		2.3	2.7	V	Maintaining RAM state in stop mode
Analog supply voltage	DAVC	V_{SS} – 0.3	V_{SS} + 3.6	V	
	AV_{CC}	V_{SS} – 0.3	V_{SS} + 3.6		
Analog reference voltage	AVRH	AV_{SS}	AV_{CC}	V	
Operating temperature	Ta	–10	+70	°C	

<Power-on precautions>

Although no particular restrictions apply to the sequence for turning the power on or off, the following sequence is recommended.

Power-on : $V_{CC}2 \rightarrow V_{CC}3 \rightarrow$ Pin signal inputs
Power-off : Pin signal inputs $\rightarrow V_{CC}3 \rightarrow V_{CC}2$

Do not leave $V_{CC}3$ connected for a long time period (e.g. 1 minute) while $V_{CC}2$ is disconnected as this may adversely affect the reliability of the LSI.
Due to electrical noise and similar, the state of internal circuits may not be maintained when $V_{CC}3$ (external) is restored from the OFF to the ON state. Always apply a reset ($\overline{INIT}$) after power-on to initialize the LSI.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

3. DC Characteristics

($V_{CC}3$ = 3.0 V to 3.6 V , $V_{CC}2$ = 2.3 V to 2.7 V , V_{SS} = DAVS = AV_{SS} = 0 V, Ta = –10 °C to +70 °C)

Parameter	Sym-bol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	V_{IH}	Pins other than X0, X1, $\overline{INIT}$, $\overline{NMI}$, $\overline{HST}$, MD0 to 2	—	2.0	—	$V_{CC}3$ + 0.3	V	
		$\overline{INIT}$, $\overline{NMI}$, $\overline{HST}$, MD0 to 2	—	0.8×$V_{CC}3$	—	$V_{CC}3$ + 0.3	V	
"L" level input voltage	V_{IL}	Pins other than X0, X1, $\overline{INIT}$, $\overline{NMI}$, $\overline{HST}$, MD0 to 2	—	V_{SS}	—	0.8	V	
		$\overline{INIT}$, $\overline{NMI}$, $\overline{HST}$, MD0 to 2	—	V_{SS}	—	0.2 × $V_{CC}3$	V	
"H" level output voltage	V_{OH}	All output pins	$V_{CC}3$ = 3.0 V I_{OH} = -4.0 mA	$V_{CC}3$ - 0.4	—	$V_{CC}3$	V	
"L" level output voltage	V_{OL}	All output pins	$V_{CC}3$ = 3.0 V I_{OL} = 4.0 mA	V_{SS}	—	0.4	V	
Input leak current (Hi-Z output leak current)	I_{LI}	All input pins*1	$V_{CC}3$ = 3.6 V 0.45 V < V_I < $V_{CC}3$	-5	—	+5	µA	
Pull-up resistance	R_{UP}	$\overline{RST}$, pins with pull-up settings	$V_{CC}3$ = 3.6 V V_I = 0.45 V	10	25	120	kΩ	
Power supply current*2	$I_{CC}2$	$V_{CC}2$	f_C = 16.5 MHz $V_{CC}2$ = 2.7 V	—	100 (150)	130 (200)	mA	When operating at : CLKB:66 MHz CLKP, CLKT : 33 MHz (×4 multiplier)
	$I_{CCS}2$		f_C = 16.5 MHz $V_{CC}2$ = 2.7 V	—	60 (100)	80 (150)	mA	When operating at : CLKP : 33 MHz in sleep mode
	$I_{CCH}2$		Ta = 25 °C $V_{CC}2$ = 2.7 V	—	100	900	µA	In stop mode
Input capacitance	C_{IH}	Other than $V_{CC}3$, $V_{CC}2$, V_{SS}, AV_{CC}, AV_{SS}, DAVC, DAVS	—	—	10	—	pF	

*1 : Excludes X0, X1, pins with internal pull-down resistor (EX_BRQ, BREAK, ICD0 to ICD3), pins with internal pull-up resistor (INIT, RST), and pins with a pull-up resistor set by PCR.

*2 : Values enclosed in brackets ( ) are for theMB91V340.

4. AC Characteristics

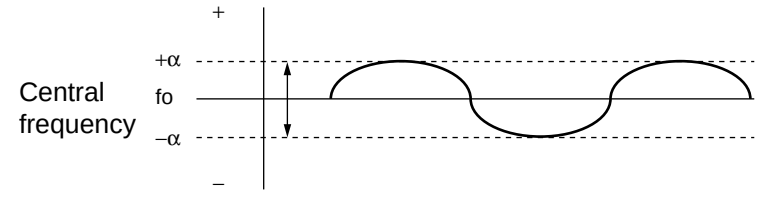
(1) Clock Timing Ratings

($V_{CC}3$ = 3.0 V to 3.6 V , $V_{CC}2$ = 2.3 V to 2.7 V , V_{SS} = DAVS = AV_{SS} = 0 V, Ta = –10 °C to +70 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Clock frequency (1)	f_C	X0 X1	—	12.5	16.5	MHz	Using PLL (When operating at max internal frequency (66 MHz) = 16.5 MHz self-oscillation with ×4 PLL)
Clock cycle time	t_C	X0 X1	—	—	60.6	ns	
Frequency fluctuation*1 (PLL locked)	Δf	—	—	—	5	%	
Clock frequency (2)	f_C	X0 X1	—	10	33	MHz	Self-oscillation (1/2 division input)
Clock frequency (3)	f_C	X0 X1	—	10	33	MHz	External clock
Clock cycle time	t_C	X0 X1		40	100	ns	
Input clock pulse width	P_{WH} P_{WL}	X0 X1		16	—	ns	
Input clock rise, fall time	t_{CR} t_{CF}	X0 X1		—	8	ns	(t_{CR} + t_{CF})
Internal operation clock frequency	f_{CP}	—	—	0.78*2	66	MHz	CPU
	f_{CPP}			0.78*2	33	MHz	Peripherals
	f_{CPT}			0.78*2	33	MHz	External bus
Internal operation clock cycle time	t_{CP}	—	—	15.2	1280*2	ns	CPU
	t_{CPP}			30.3	1280*2	ns	Peripherals
	t_{CPT}			30.3	1280*2	ns	External bus

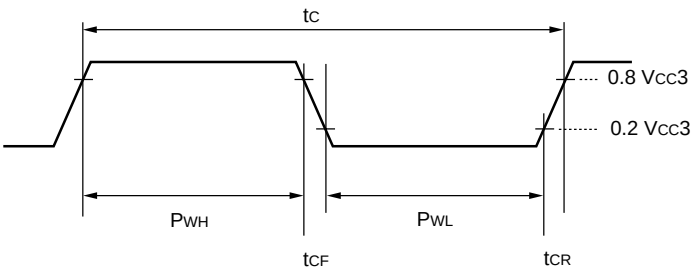
*1 : The frequency fluctuation value is the maximum percentage deviation from the preset central frequency when using the multiplier (when PLL is locked).

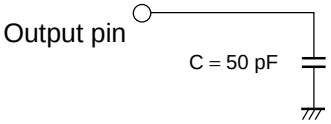
$$\Delta f = \frac{|\alpha|}{fo} \times 100\ (\%)$$



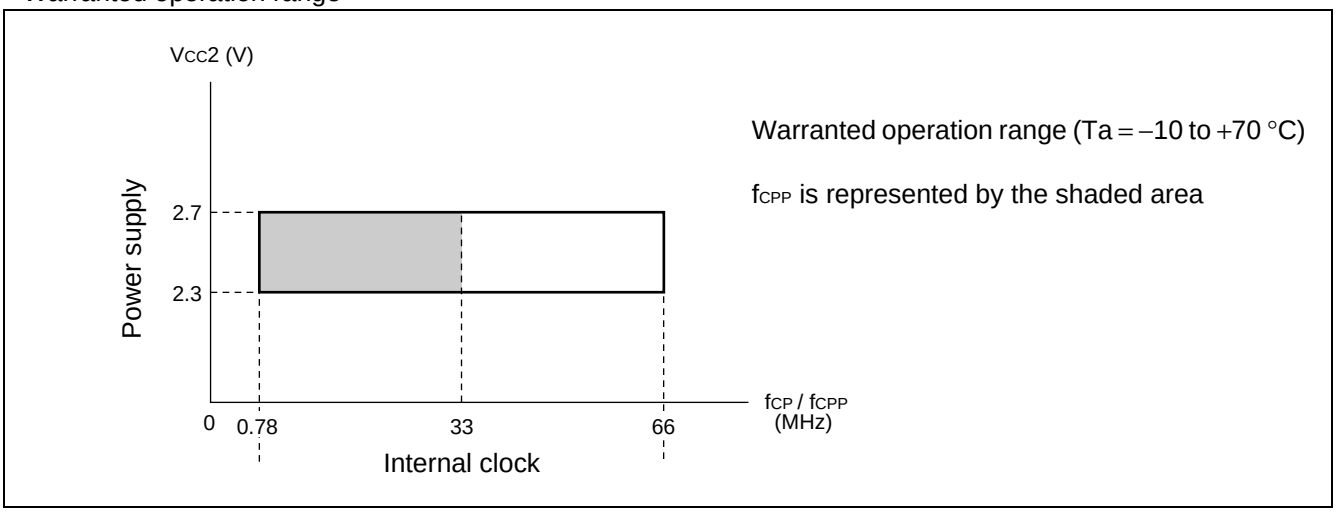
*2 : Values are for minimum clock frequency (12.5 MHz) input to X0, oscillation circuit uses PLL, and gear ratio = 1/16.

• Conditions for measuring the clock timing ratings

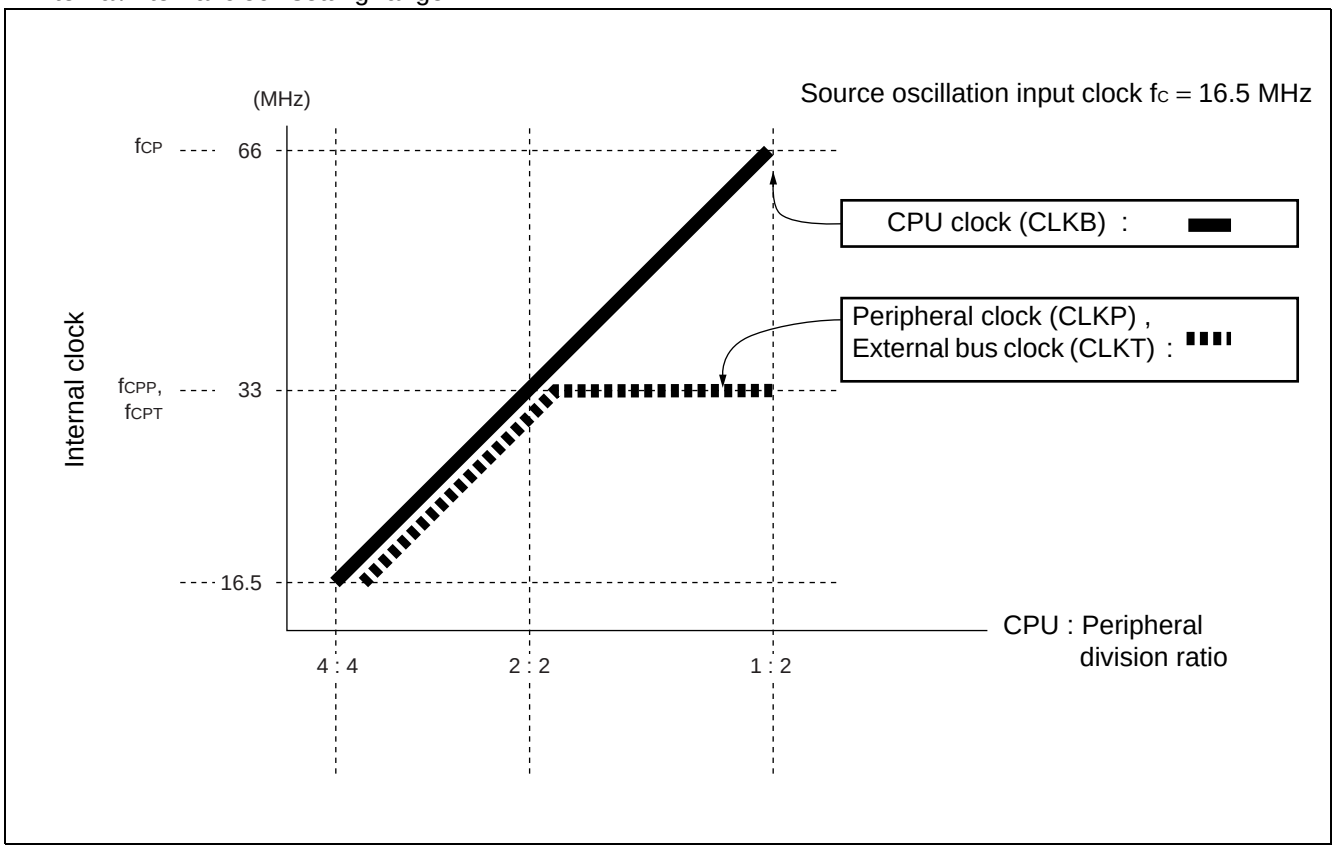




• Warranted operation range



• External/internal clock setting range



*1 : If using the PLL, input an external clock in the range 12.5 MHz to 16.5 MHz.

*2 : Allow a PLL oscillation stabilization time of > 300 µs.

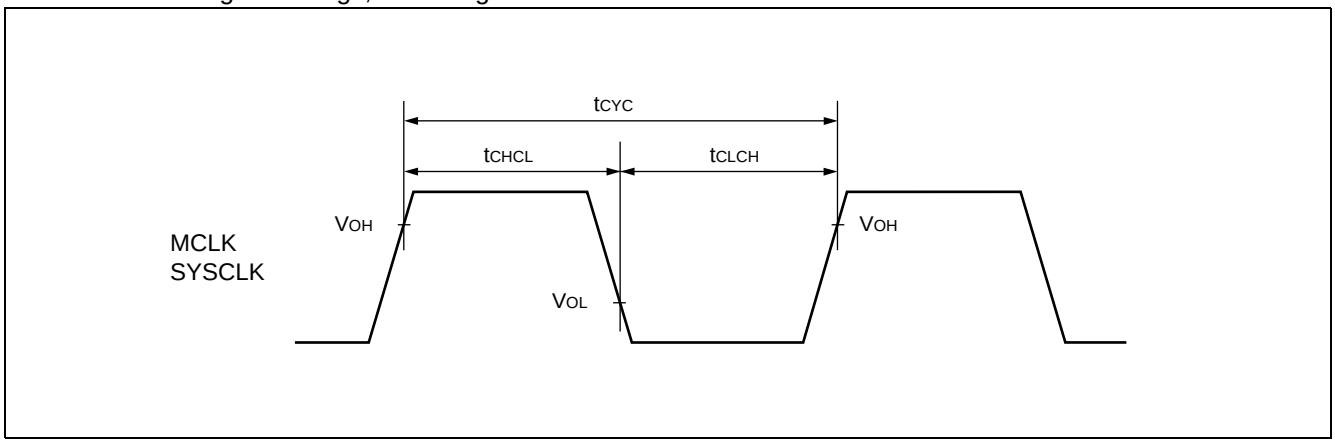
*3 : Set the gear ratio for the internal clock to be within the values shown in the (1) Clock Timing Ratings table.

(2) Clock Output Timing

($V_{CC}3$ = 3.0 V to 3.6 V , $V_{CC}2$ = 2.3 V to 2.7 V , V_{SS} = DAVS = AV_{SS} = 0 V, Ta = –10 °C to +70 °C)

Parameter	Sym-bol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Cycle time	t_{CYC}	MCLK SYSCLK	—	t_{CPT}	—	ns	*1
MCLK↑→MCLK↓ SYSCLK↑→SYSCLK↓	t_{CHCL}	MCLK SYSCLK		t_{CYC} / 2 – 2.5	t_{CYC} / 2 + 2.5	ns	*2
MCLK↓→MCLK↑ SYSCLK↓→SYSCLK↑	t_{CLCL}	MCLK SYSCLK		t_{CYC} / 2 – 2.5	t_{CYC} / 2 + 2.5	ns	*3

For the following AC ratings, the rating for HCLK are the same as for SYSCLK.



*1 : t_{CYC} is the width of one clock cycle after gearing.

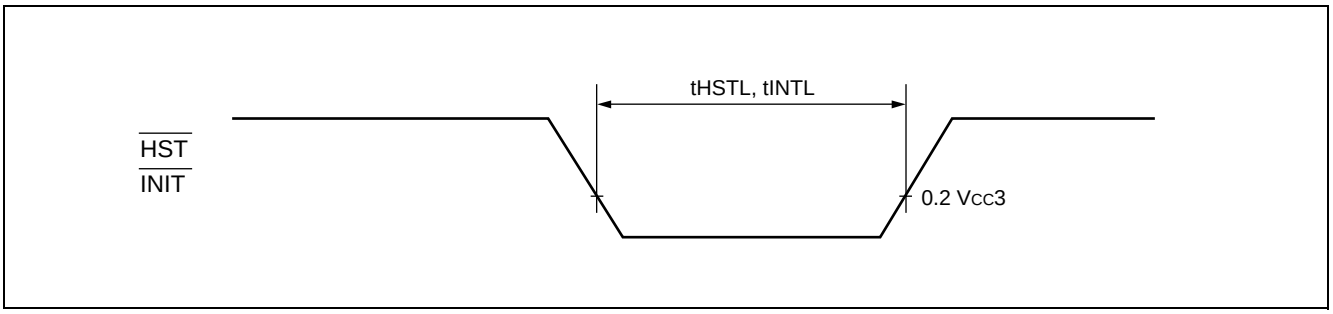
*2 : The following ratings are for the gear ratio set to × 1.
For the ratings when the gear ratio is set to between 1/2 and 1/16 , substitute 1/2 to 1/16 for n in the following equation.
$(1 / 2 \times 1 / n) \times t_{CYC} - 10$

*3 : The following rating are for the gear ratio set to × 1.

(3) Reset and Hardware Standby Ratings

($V_{CC}3$ = 3.0 V to 3.6 V , $V_{CC}2$ = 2.3 V to 2.7 V , V_{SS} = DAVS = AV_{SS} = 0 V, Ta = –10 °C to +70 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Hardware standby input time	t_{HSTL}	$\overline{HST}$	—	$t_C \times 10$	—	ns	
Init input time (at power-on)	t_{INTL}	$\overline{INIT}$		$t_C \times 2^{23}$	—	ns	
Init input time (other than at power-on)				$t_C \times 10$		ns	



(4-1) Normal Bus Access Read/Write Operation

($V_{CC}3$ = 3.0 V to 3.6 V , $V_{CC}2$ = 2.3 V to 2.7 V , V_{SS} = DAVS = AV_{SS} = 0 V, Ta = –10 °C to +70 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
$\overline{CS0}$ to $\overline{CS7}$ setup	t_{CSLCH}	MCLK $\overline{CS0}$ to $\overline{CS7}$	AWRxL : W02 = 0	3	—	ns	*3
	t_{CSDLCH}		AWRxL : W02 = 1	–3	—	ns	*3
$\overline{CS0}$ to $\overline{CS7}$ hold	t_{CHCSH}		—	3	t_{CYC} / 2 + 6	ns	
Address setup	t_{ASCH}	MCLK A23 to A00		3	—	ns	
	t_{ASWL}	$\overline{WR0}$, $\overline{WR1}$, $\overline{WR}$ A23 to A00		3	—	ns	
	t_{ASRL}	$\overline{RD}$ A23 to A00		3	—	ns	
Address hold	t_{CHAX}	MCLK A23 to A00		3	t_{CYC} / 2 + 6	ns	
	t_{WHAX}	$\overline{WR0}$, $\overline{WR1}$, $\overline{WR}$ A23 to A00		3	—	ns	
	t_{RHAX}	$\overline{RD}$ A23 to A00		3	—	ns	
Valid address→ Valid data input time	t_{AVDV}	A23 to A00 D31 to D16		—	3 / 2×t_{CYC} – 11	ns	*1 *2
$\overline{WR0}$, $\overline{WR1}$, $\overline{WR}$ delay time	t_{CHWL}	MCLK $\overline{WR0}$, $\overline{WR1}$, $\overline{WR}$		—	6	ns	
$\overline{WR0}$, $\overline{WR1}$, $\overline{WR}$ delay time	t_{CHWH}			—	6	ns	
$\overline{WR0}$, $\overline{WR1}$, $\overline{WR}$ minimum pulse width	t_{WLWH}	$\overline{WR0}$, $\overline{WR1}$, $\overline{WR}$		12	—	ns	
Data setup →$\overline{WR0}$ to $\overline{WR1}$, $\overline{WR}$↑	t_{DSWH}	$\overline{WR0}$, $\overline{WR1}$, $\overline{WR}$ D31 to D16		t_{CYC}	—	ns	
$\overline{WR0}$, $\overline{WR1}$, $\overline{WR}$↑→ Data hold time	t_{WHDX}			3	—	ns	
$\overline{RD}$ delay time	t_{CHRL}	MCLK $\overline{RD}$		—	6	ns	
$\overline{RD}$ delay time	t_{CHRH}			—	6	ns	
$\overline{RD}$↓→ Valid data input time	t_{RLDV}	$\overline{RD}$ D31 to D16		—	t_{CYC} – 10	ns	*1
Data setup →$\overline{RD}$↑ time	t_{DSRH}			10	—	ns	
$\overline{RD}$↑→ Data hold time	t_{RHDX}			0	—	ns	
$\overline{RD}$ minimum pulse width	t_{RLRH}	$\overline{RD}$		12	—	ns	
$\overline{AS}$ setup	t_{ASLCH}	MCLK $\overline{AS}$		3	—	ns	
$\overline{AS}$ hold	t_{CHASH}			3	t_{CYC} / 2 + 6	ns	

*1 : When the bus is delayed by automatic wait insertion or RDY input, add (t_{CYC}×number of wait cycles) to the rated values.

*2 : These rating are for the gear ratio set to × 1. For the ratings when the gear ratio is set to between 1/2 and 1/16, substitute 1/2 to 1/16

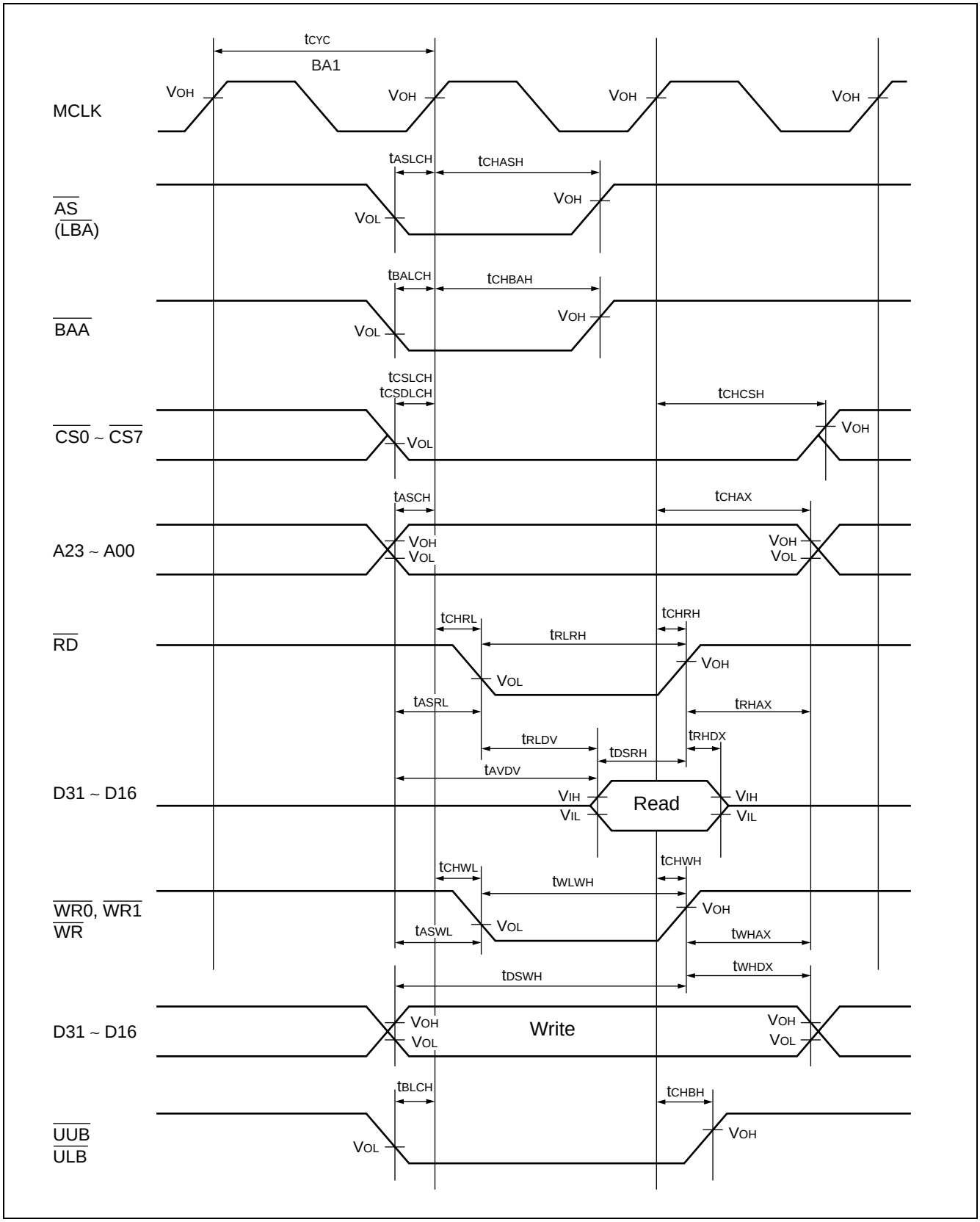
Equation : $3 / (2n) \times t_{CYC} - 11$

*3 : AWRxL : Area Wait Register

(4-2) Normal Bus Access Read/Write Operation

($V_{CC}3$ = 3.0 V to 3.6 V , $V_{CC}2$ = 2.3 V to 2.7 V , V_{SS} = DAVS = AV_{SS} = 0 V, Ta = –10 °C to +70 °C)

Parameter	Sym-bol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
$\overline{BAA}$ setup	t_{BALCH}	MCLK $\overline{BAA}$	—	3	—	ns	
$\overline{BAA}$ hold	t_{CHBAH}			3	t_{CYC} / 2 + 6	ns	
$\overline{UUB}$/$\overline{ULB}$setup	t_{BLCH}	MCLK $\overline{UUB}$/$\overline{ULB}$		3	—	ns	
$\overline{UUB}$/$\overline{ULB}$ hold	t_{CHBH}			3	t_{CYC} / 2 + 6	ns	


tCYC
BA1
MCLK
VOH
AS
(LBA)
tASLCH
tCHASH
VOL
BAA
tBALCH
tCHBAH
CS0 ~ CS7
tCSLCH
tCSDLCH
tCHCSH
A23 ~ A00
tASCH
tCHAX
RD
tCHRL
tRLRH
tCHRH
tASRL
tRHAX
tRLDV
tRHDX
tDSRH
tAVDV
D31 ~ D16
VIH
VIL
Read
WR0, WR1
WR
tCHWL
tWLWH
tCHWH
tASWL
tWHAX
tWHDX
tDSWH
Write
UUB
ULB
tBLCH
tCHBH

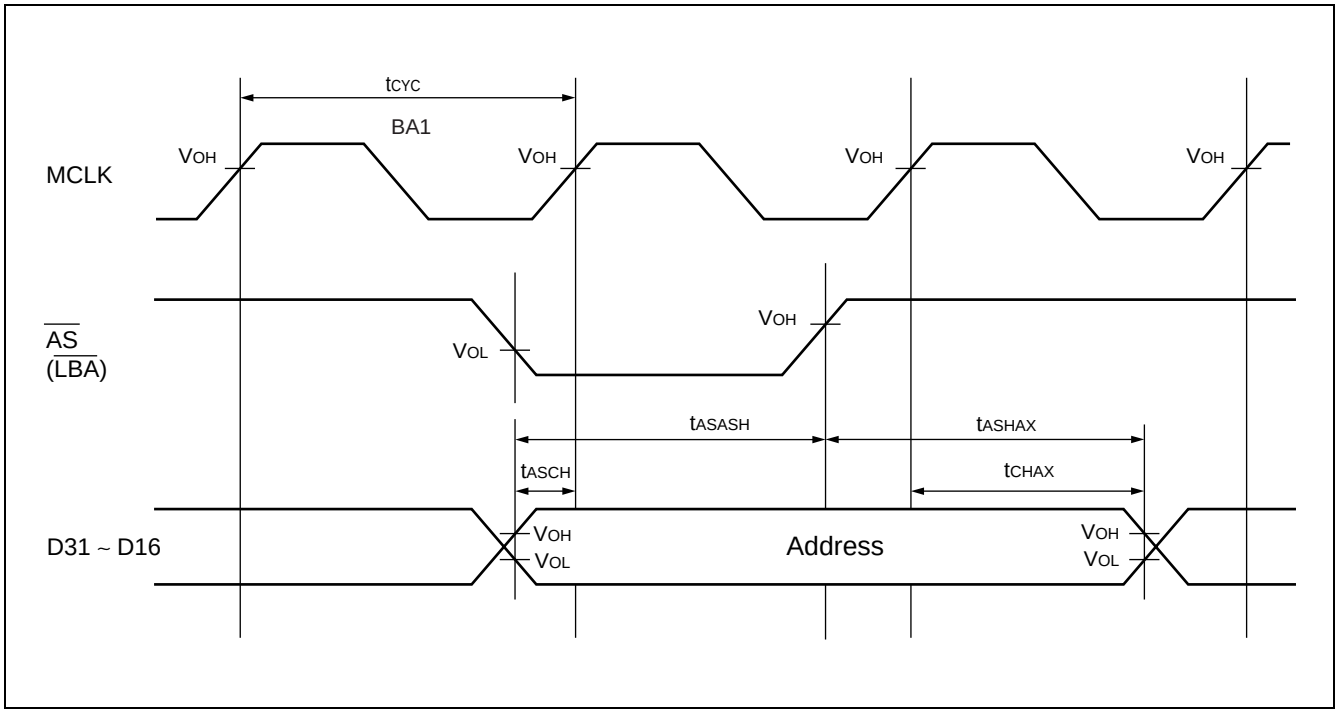
(4-3) Multiplex Bus Access Read/Write Operation

($V_{CC}3$ = 3.0 V to 3.6 V , $V_{CC}2$ = 2.3 V to 2.7 V , V_{SS} = DAVS = AV_{SS} = 0 V, Ta = –10 °C to +70 °C)

Parameter	Sym-bol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
D31 to D16 address setup time →MCLK↑	t_{ASCH}	MCLK D31 to D16	—	3	—	ns	
MCLK↑→ D31 to D16 address hold time	t_{CHAX}		—	3	t_{CYC} / 2 + 6	ns	
D31 to D16 address setup time →$\overline{AS}$↑	t_{ASASH}	$\overline{AS}$ D31 to D16	—	12	—	ns	
$\overline{AS}$↑→ D31 to D16 address hold time	t_{ASHAX}		—	t_{CYC} – 3	t_{CYC} + 3	ns	

*1 : These ratings are not guaranteed when the CS→$\overline{RD}$/$\overline{WR}$ Setup delay setting in AWR:bit1 is set to “0”.

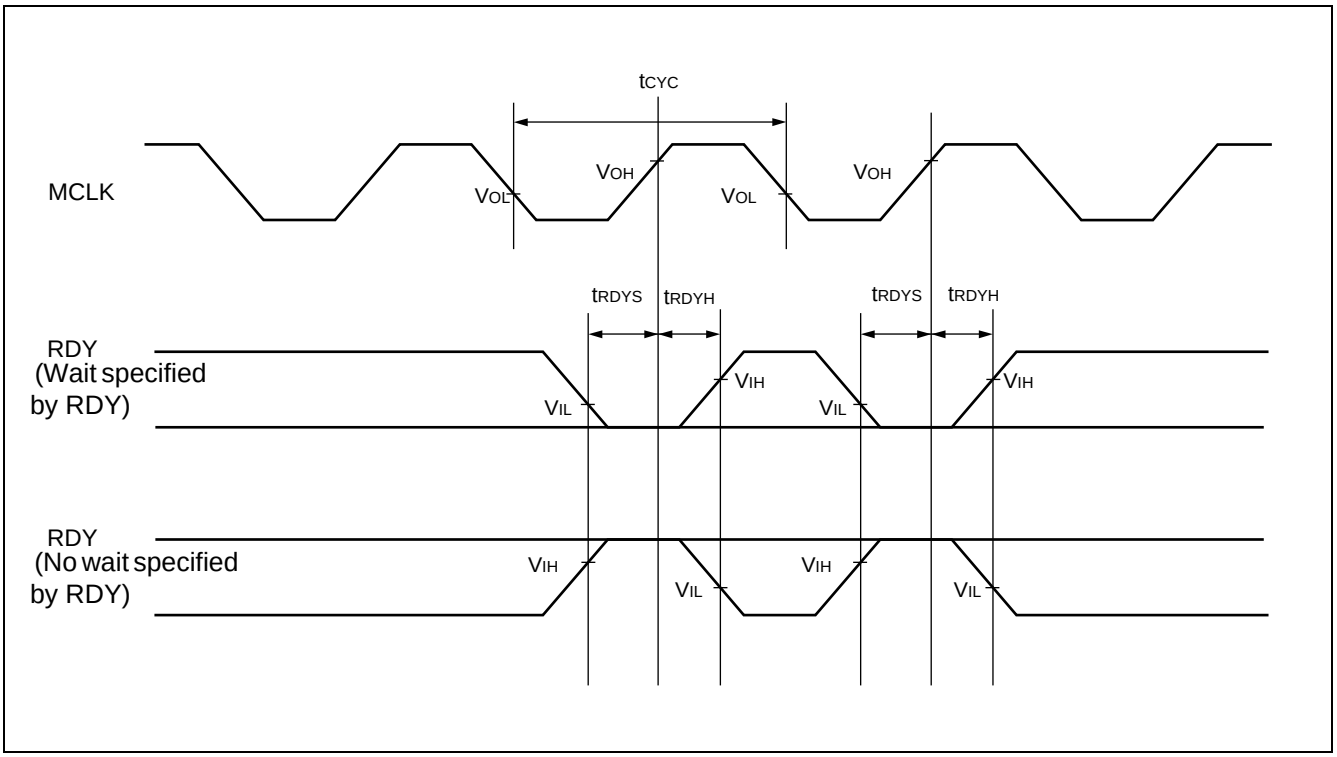
*2 : Ratings other than those shown above are the same as for the normal bus interface.



(5) Ready Input Timings

($V_{CC}3$ = 3.0 V to 3.6 V , $V_{CC}2$ = 2.3 V to 2.7 V , V_{SS} = DAVS = AV_{SS} = 0 V, Ta = –10 °C to +70 °C)

Parameter	Sym-bol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
RDY setup time →MCLK↑	t_{RDYS}	MCLK RDY	—	10	—	ns	
MCLK↑→ RDY hold time	t_{RDYH}	MCLK RDY	—	0	—	ns	

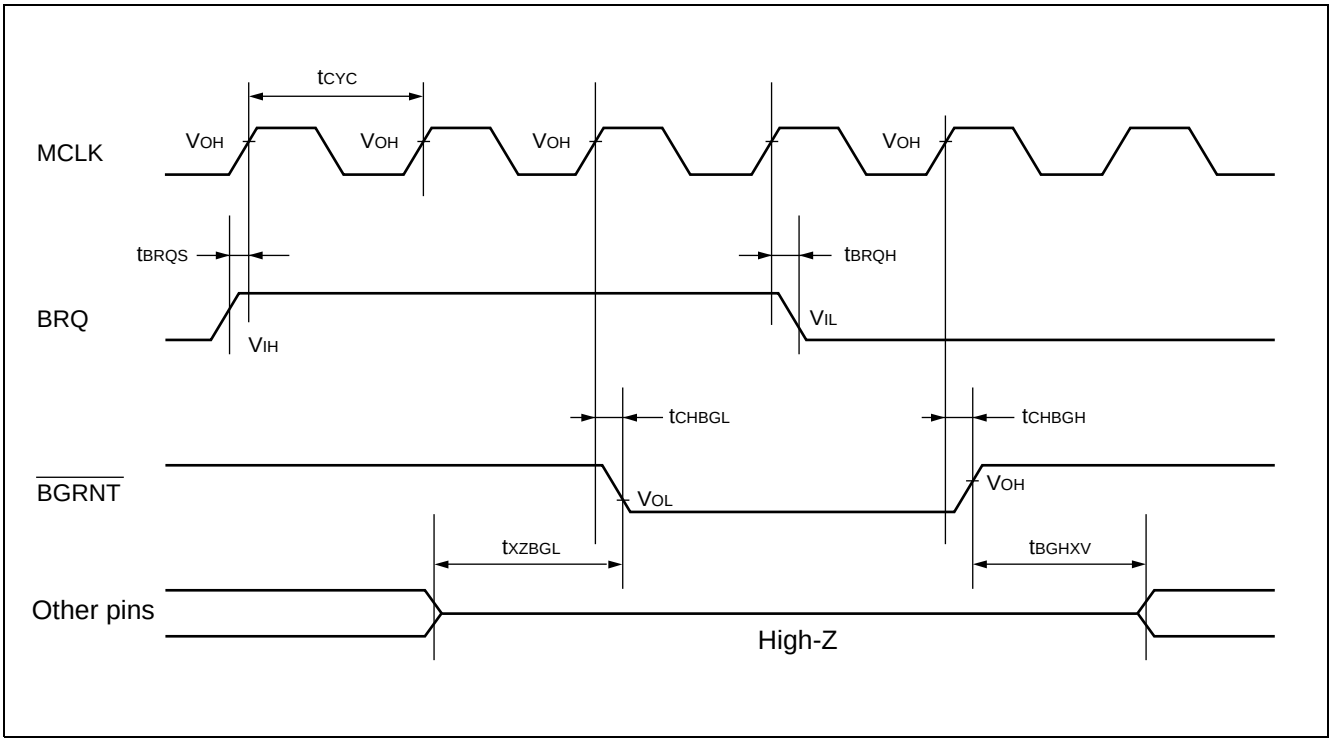


(6) Hold Timing

($V_{CC}3$ = 3.0 V to 3.6 V , $V_{CC}2$ = 2.3 V to 2.7 V , V_{SS} = DAVS = AV_{SS} = 0 V, Ta = –10 °C to +70 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
BRQ setup time →MCLK↑	t_{BRQS}	MCLK BRQ	—	10	—	ns	
MCLK↑→ BRQ hold time	t_{BRQH}			0	—	ns	
$\overline{BGRNT}$ delay time	t_{CHBGL}	MCLK $\overline{BGRNT}$	—	t_{CYC} / 2 – 6	t_{CYC} / 2 + 6	ns	
$\overline{BGRNT}$ delay time	t_{CHBGH}			t_{CYC} / 2 – 6	t_{CYC} / 2 + 6	ns	
Pin floating →$\overline{BGRNT}$↓ time	t_{XZBGL}	$\overline{BGRNT}$ Other pins		t_{CYC} – 10	t_{CYC} + 10	ns	
$\overline{BGRNT}$↑→Pin valid time	t_{BGHXV}			t_{CYC} – 10	t_{CYC} + 10	ns	

* : The time from receiving BRQ to $\overline{BGRNT}$ changing is one cycle or more.



(7) UART Timing

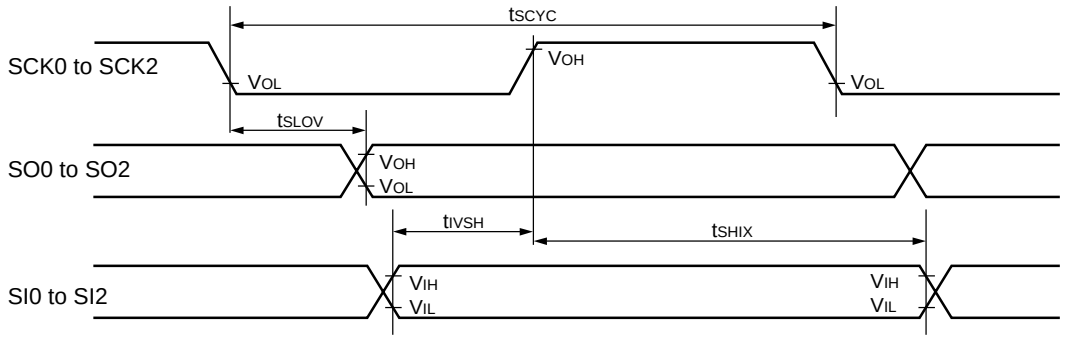
($V_{CC}3$ = 3.0 V to 3.6 V , $V_{CC}2$ = 2.3 V to 2.7 V , V_{SS} = DAVS = AV_{SS} = 0 V, Ta = –10 °C to +70 °C)

Parameter	Sym-bol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK0 to SCK2	Internal shift clock mode	8 t_{CYCP}	—	ns	
SCK↓ →SO delay time	t_{SLOV}	SCK0 to SCK2 SO0 to SO2		–80	80	ns	
Valid SI →SCK↑	t_{IVSH}	SCK0 to SCK2 SI0 to SI2		100	—	ns	
SCK↑ → valid SI hold time	t_{SHIX}	SCK0 to SCK2 SI0 to SI2		60	—	ns	
Serial clock “H” pulse width	t_{SHSL}	SCK0 to SCK2	External shift clock mode	4 t_{CYCP}	—	ns	
Serial clock “L” pulse width	t_{SLSH}	SCK0 to SCK2		4 t_{CYCP}	—	ns	
SCK↓ →SO delay time	t_{SLOV}	SCK0 to SCK2 SO0 to SO2		—	150	ns	
Valid SI→SCK↑	t_{IVSH}	SCK0 to SCK2 SI0 to SI2		60	—	ns	
SCK↑→ valid SI hold time	t_{SHIX}	SCK0 to SCK2 SI0 to SI2		60	—	ns	

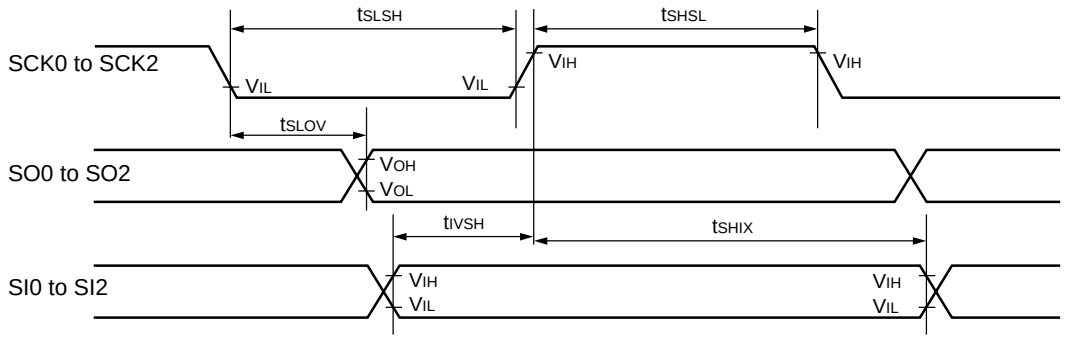
*1 : These are the AC ratings for CLK synchronous mode.

*2 : t_{CYCP} is the peripheral clock cycle time.

• Internal shift clock mode



• External shift clock mode

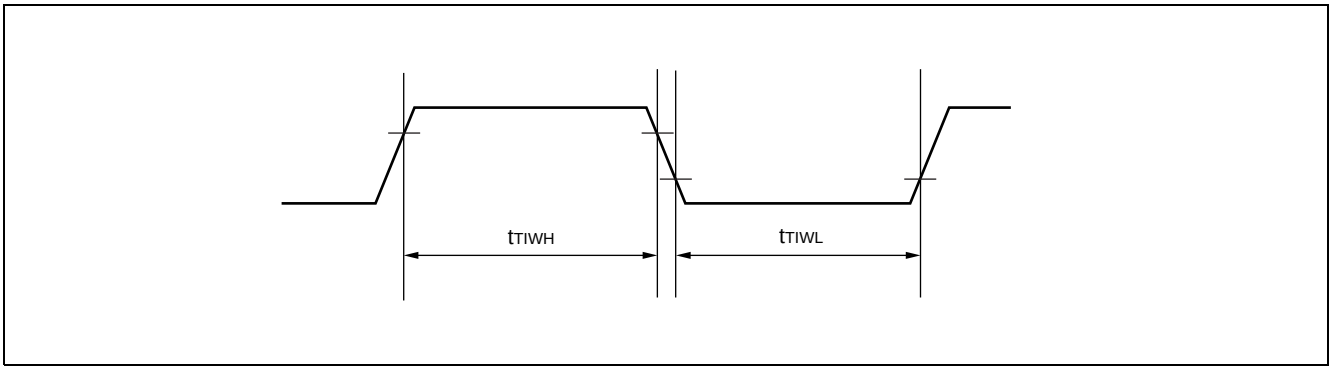


(8) Freerun Timer Clock, Reload Timer Clock, and PPG Timer Input Timings

($V_{CC}3$ = 3.0 V to 3.6 V , $V_{CC}2$ = 2.3 V to 2.7 V , V_{SS} = DAVS = AV_{SS} = 0 V, Ta = –10 °C to +70 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TIWH} t_{TIWL}	FRCK TIN0 to TIN3 AIN0 to AIN3 BIN0 to BIN3 ZIN0 to ZIN3	—	2 t_{CYCP}*	—	ns	

* : t_{CYCP} is the peripheral clock cycle time.

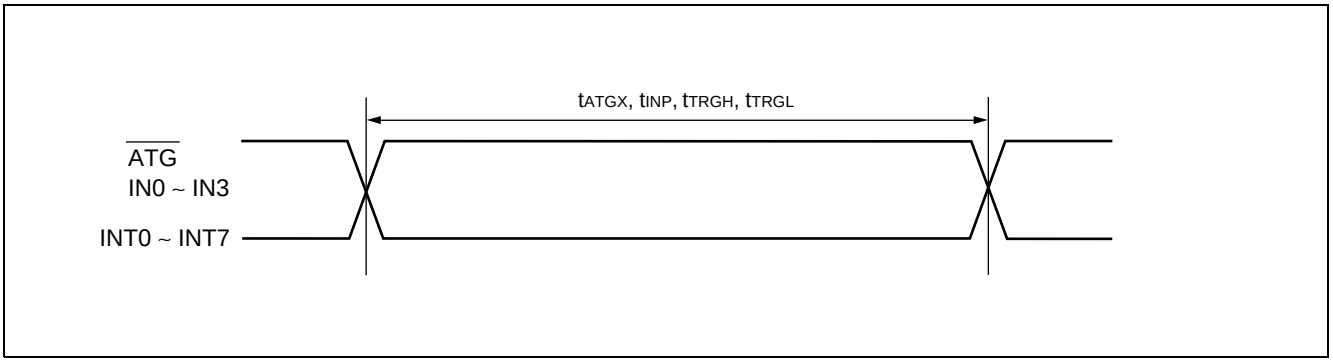


(9) Trigger Input Timing

($V_{CC}3$ = 3.0 V to 3.6 V , $V_{CC}2$ = 2.3 V to 2.7 V , V_{SS} = DAVS = AV_{SS} = 0 V, Ta = –10 °C to +70 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
A/D activation trigger input time	t_{ATGX}	$\overline{ATG}$	—	5 t_{CYCP}*	—	ns	
Input capture input trigger	t_{INP}	IN0 to IN3	—	5 t_{CYCP}*	—	ns	
External interrupt input pulse width	t_{TRGH} t_{TRGL}	INT0 to INT7	—	3 t_{CYCP}*	—	ns	Normal operation
				1	—	µs	In stop mode

* : t_{CYCP} is the peripheral clock cycle time.



(10) DMA Controller Timing

($V_{CC}3$ = 3.0 V to 3.6 V , $V_{CC}2$ = 2.3 V to 2.7 V , V_{SS} = DAVS = AV_{SS} = 0 V, Ta = –10 °C to +70 °C)

[For edge detection] (Block/step transfer mode, burst transfer mode)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
DREQ input pulse width	t_{DRWL}	DREQ0 to DREQ2	—	2 t_{CYC}*	—	ns	
DSTP input pulse width	t_{DSWH}	DSTP0 to DSTP2		2 t_{CYC}*	—	ns	

* : When $f_{CPT} > f_{CP}$, t_{CYC} becomes same as t_{CP}.

[For level detection] (Demand transfer mode)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
DREQ setup time	t_{DRS}	MCLK DREQ0 to DREQ2	—	10	—	ns	
DREQ hold time	t_{DRH}	MCLK DREQ0 to DREQ2		0	—	ns	
DSTP setup time	t_{DSTPS}	MCLK DSTP0 to DSTP2		10	—	ns	
DSTP hold time	t_{DSTPH}	MCLK DSTP0 to DSTP2		0	—	ns	

[For all operation modes]

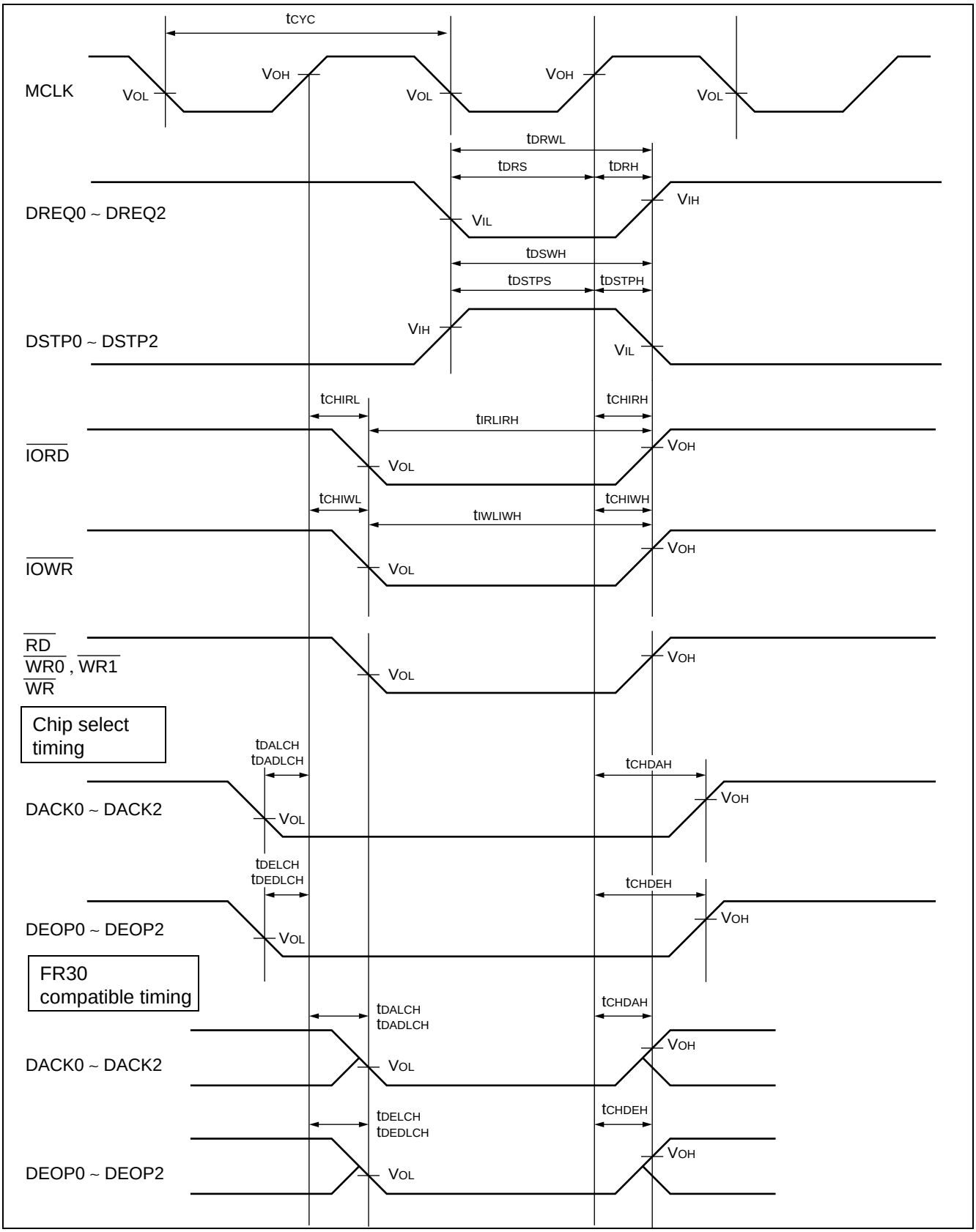
Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
DACK delay time	t_{DALCH}	MCLK DACK0 to DACK2	AWRxL* : W02 = 0	3	—	ns	CS timing
				—	6	ns	FR30 compatible
	t_{DADLCH}		AWRxL : W02 = 1	–3	—	ns	CS timing
				—	6	ns	FR30 compatible
	t_{CHDAH}		—	—	t_{CYC} / 2 + 6	ns	CS timing
				—	6	ns	FR30 compatible
DEOP delay time	t_{DELCH}	MCLK DEOP0 to DEOP2	AWRxL : W02 = 0	3	—	ns	CS timing
				—	6	ns	FR30 compatible
	t_{DEDLCH}		AWRxL : W02 = 1	–3	—	ns	CS timing
				—	6	ns	FR30 compatible
	t_{CHDEH}		—	—	t_{CYC} / 2 + 6	ns	CS timing
				—	6	ns	FR30 compatible

(Continued)

(Continued)

Parameter	Sym-bol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
$\overline{\text{IORD}}$ delay time	t_{CHIRL}	MCLK $\overline{\text{IORD}}$	—	—	6	ns	
	t_{CHIRH}			—	6	ns	
$\overline{\text{IOWR}}$ delay time	t_{CHIWL}	MCLK $\overline{\text{IOWR}}$		—	6	ns	
	t_{CHIWH}			—	6	ns	
$\overline{\text{IORD}}$ minimum pulse width	t_{IRLIRH}	$\overline{\text{IORD}}$	—	12	—	ns	
$\overline{\text{IOWR}}$ minimum pulse width	t_{IWLIWH}	$\overline{\text{IOWR}}$	—	12	—	ns	

* : AWRxL : Area Wait Register


tCYC
MCLK
VOH
VOL
tDRWL
tDRS
tDRH
DREQ0 ~ DREQ2
VIH
VIL
tDSWH
tDSTPS
tDSTPH
DSTP0 ~ DSTP2
tCHIRL
tCHIRH
tIRLIRH
IORD
tCHIWL
tCHIWH
tIWLIWH
IOWR
RD
WR0 , WR1
WR
Chip select timing
tDALCH
tDADLCH
tCHDAH
DACK0 ~ DACK2
tDELCH
tDEDLCH
tCHDEH
DEOP0 ~ DEOP2
FR30 compatible timing

5. Electrical Characteristics for the A/D Converter

($V_{CC}3 = AV_{CC} = 3.0$ V to 3.6 V , $V_{CC}2 = 2.3$ V to 2.7 V , $V_{SS} = DAVS = AV_{SS} = 0$ V, AVRH = 3.0 V to 3.6 V , Ta = –10 °C to +70 °C)

Parameter	Symbol	Pin name	Value			Unit
			Min	Typ	Max	
Resolution	—	—	—	10	10	BIT
Total error	—	—	–8.5	—	8.5	LSB
Linearity error	—	—	–3.0	—	3.0	LSB
Differential linearity error	—	—	–2.5	—	2.5	LSB
Zero transition error	V_{OT}	AN0 to AN7	–8.0	0.5	8.0	LSB
Full-scale transition error	V_{FST}	AN0 to AN7	AVRH – 8.0	AVRH – 1.5	AVRH + 8.0	LSB
Conversion time*1	—	—	5.4	—	—	µs
Analog port input current	I_{AIN}	AN0 to AN7	—	0.1	10	µA
Analog input voltage	V_{AIN}	AN0 to AN7	AVss	—	AVRH	V
Reference voltage	—	AVRH	AVss	—	AV_{CC}	V
Power supply current	I_A	AV_{CC}	—	0.6	2	mA
	I_{AH}*2		—	—	10	µA
Reference voltage supply current	I_R	AVRH	—	0.6	2	mA
	I_{RH}*2		—	—	10	µA
Variation between channels	—	AN0 to AN7	—	—	5	LSB

*1 : For $V_{CC}3 = AV_{CC} = 3.0$ V to 3.6 V , machine clock = 33 MHz

*2 : Current when A/D converter not operating and CPU in stop mode ($V_{CC}3 = AV_{CC} = AVRH = 3.6$ V)

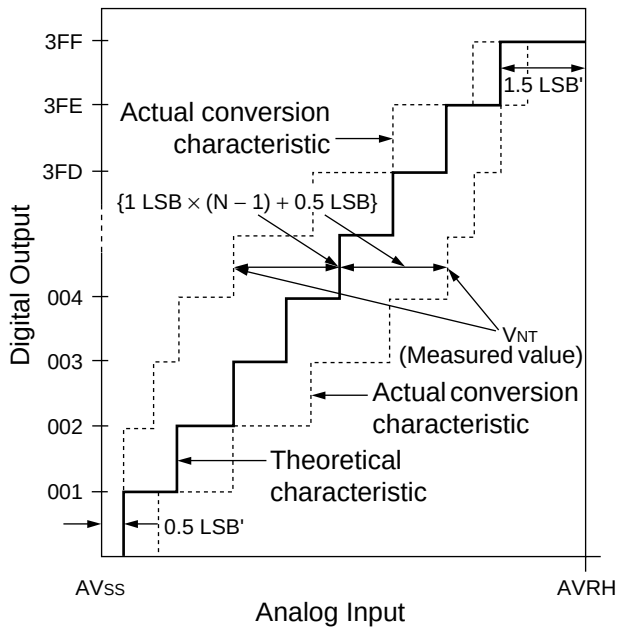
Notes :
- The relative error increases as AVRH becomes smaller.
- Ensure that the output impedance of the external circuit connected to the analog input meets the following condition :

  Output impedance of external circuit < 4 kΩ

  If the output impedance of the external circuit is too high, the analog voltage sampling time may be too short.

- Definition of A/D Converter Terms
  - Resolution : The change in analog voltage that can be recognized by the A/D converter.
  - Linearity error : The deviation between the actual conversion characteristics and the line linking the zero transition point (00 0000 0000←→00 0000 0001) and the full scale transition point (11 1111 1110←→11 1111 1111) .
  - Differential linearity error : The variation from the ideal input voltage required to change the output code by 1 LSB.
  - Total error : The total error is the difference between the actual value and the theoretical value. Includes the zero transition error, full-scale transition error and linearity error.

Total Error



Total error for digital output N =

$$\frac{V_{NT} - \{1\ LSB' \times (N-1) + 0.5\ LSB'\}}{1\ LSB'}\ [V]$$

Linearity error for digital output N =

$$\frac{V_{NT} - \{1\ LSB \times (N-1) + V_{OT}\}}{1\ LSB}\ [LSB]$$

Differential linearity error for digital output N =

$$\frac{V_{(N+1)T} - V_{NT}}{1\ LSB} - 1\ [LSB]$$

$$1\ LSB' \text{ (Theoretical value)} = \frac{AVRH - AV_{SS}}{1024}\ [V]$$

$$1\ LSB = \frac{V_{FST} - V_{OT}}{1022}\ [V]$$

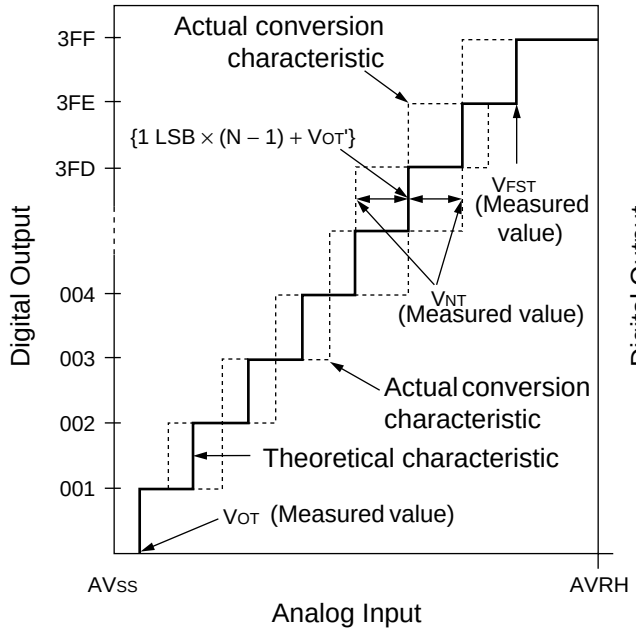
V_{OT}' (Theoretical value) = AV_{SS} + 0.5 LSB' [V]

V_{FST}' (Theoretical value) = AVRH – 1.5 LSB' [V]

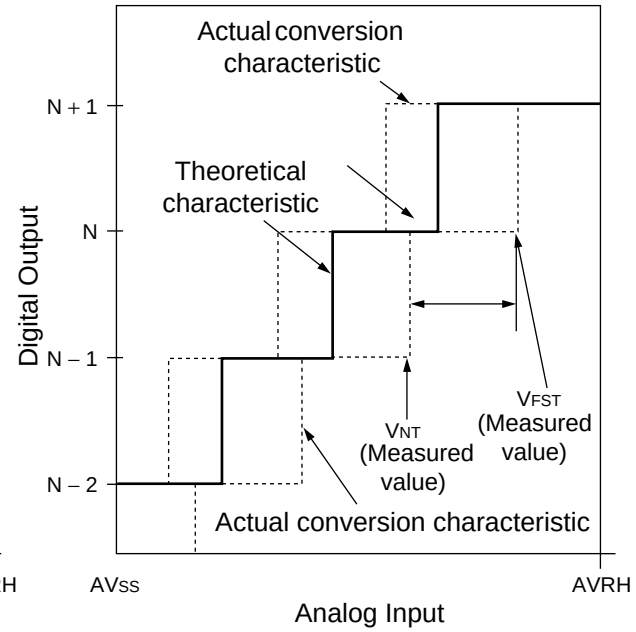
V_{NT} : Voltage at which digital output changes from (N + 1) to N.

V_{OT} : Voltage at which digital output changes from $(000)_H$ to $(001)_H$.

Linearity Error



Differential Linearity Error



6. Electrical Characteristics for the D/A Converter

($V_{CC}3$ = DAVC = 3.0 V to 3.6 V , $V_{CC}2$ = 2.3 V to 2.7 V , V_{SS} = DAVS = AV_{SS} = 0 V, AVRH = 3.0 V to 3.6 V , Ta = –10 °C to +70 °C)

Parameter		Symbol	Pin name	Value			Unit
				Min	Typ	Max	
Resolution		—	—	—	—	8	BIT
DA output guaranteed range for linearity error and differential linearity error		V_{OUT}*1	DA0 to DA2	DAVS + 0.25	—	DAVC – 0.25	V
Linearity error		—	—	–2	0	2	LSB
Differential linearity error		—	—	–0.7	0	0.7	LSB
Conversion time		—	DA0 to DA2	—	—	5	µs
Output offset		V_{OFF}	DA0 to DA2	–50	0	50	mV
Load	Capacitance	C_L	DA0 to DA2	—	—	20	pF
	Current	I_L	DA0 to DA2	–250	—	250	µA
Power supply current		I_{DA}	DAVC	0.35	1	2	mA
		I_{DAH}*2		—	—	10	µA

*1 : No output occurs in the range DAVS to DAVS + 100 mV and DAVC to DAVC - 100 mV.

*2 : Current when D/A converter not operating and CPU in stop mode ($V_{CC}3$ = DAVC = 3.6 V) .

Example Output Linearity Table

($V_{CC}3$ = DAVC = 3.0 V , $V_{CC}2$ = 2.3 V to 2.7 V , V_{SS} = DAVS = AV_{SS} = 0 V, AVRH = 3.0 V , Ta = –10 °C to +70 °C)

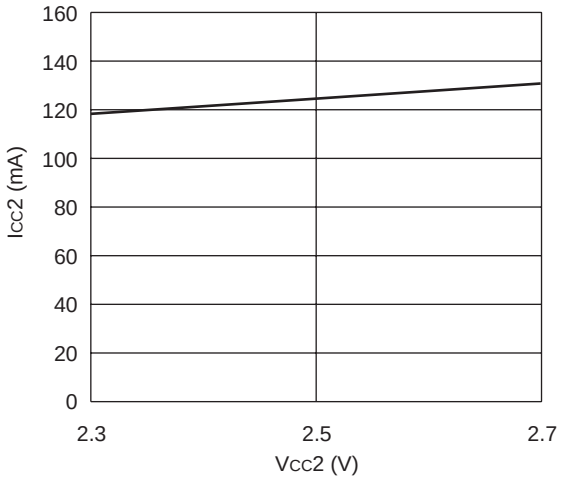
Digital Value										Output voltage (V)
Hex.	Dec.	D7	D6	D5	D4	D3	D2	D1	D0	
FF	255	1	1	1	1	1	1	1	1	Outside guaranteed range for linearity error and differential linearity error (relative size is guaranteed)
≀	≀	≀	≀	≀	≀	≀	≀	≀	≀	
EB	235	1	1	1	0	1	0	1	1	
EA	234	1	1	1	0	1	0	1	0	2.742
E9	233	1	1	1	0	1	0	0	1	2.730
≀	≀	≀	≀	≀	≀	≀	≀	≀	≀	≀
17	23	0	0	0	1	0	1	1	1	0.270
16	22	0	0	0	1	0	1	1	0	0.258
15	21	0	0	0	1	0	1	0	1	Outside guaranteed range for linearity error and differential linearity error (relative size is guaranteed)
≀	≀	≀	≀	≀	≀	≀	≀	≀	≀	
00	0	0	0	0	0	0	0	0	0	

$$\text{D/A output voltage} = \frac{(\text{DAVC} - \text{DAVS}) \times (\text{digital value (dec.)}) + \text{DAVS}}{256} [\text{V}]$$

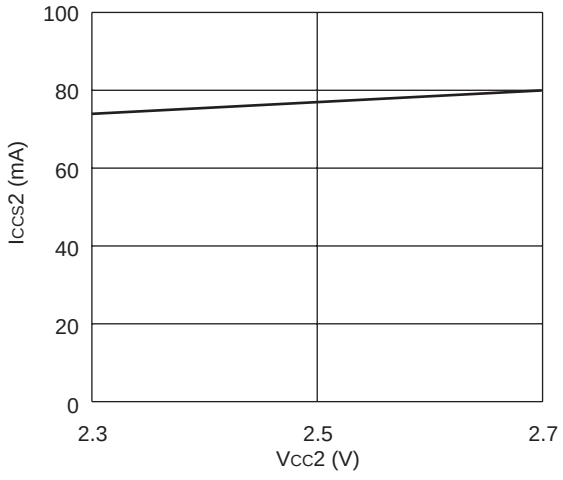
■ EXAMPLE CHARACTERISTICS

Power supply current example characterictics

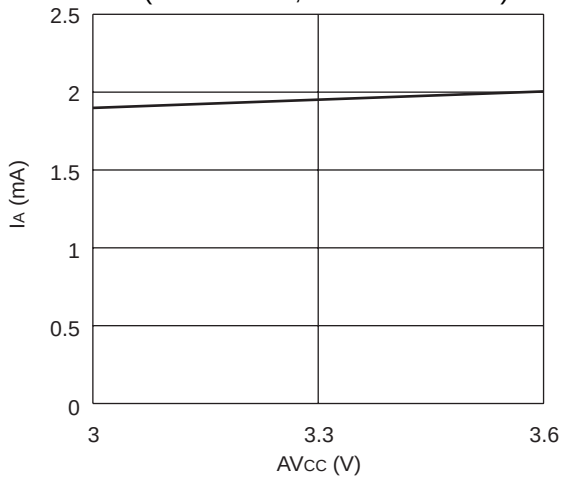
I_{CC2} – V_{CC2}
(Ta = +25 °C, CLKB = 66 MHz)



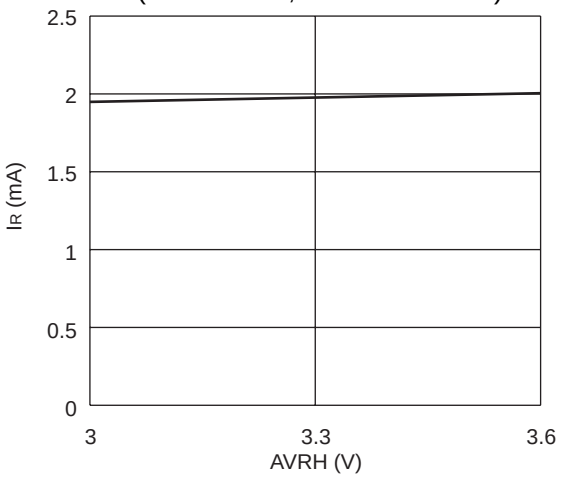
I_{CCS2} – V_{CC2}
(Ta = +25 °C, CLKP = 33 MHz)



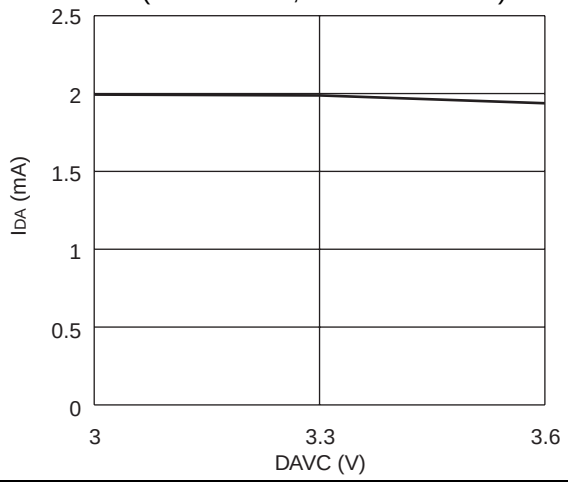
I_A – AV_{CC}
(Ta = +25 °C, CLKP = 33 MHz)



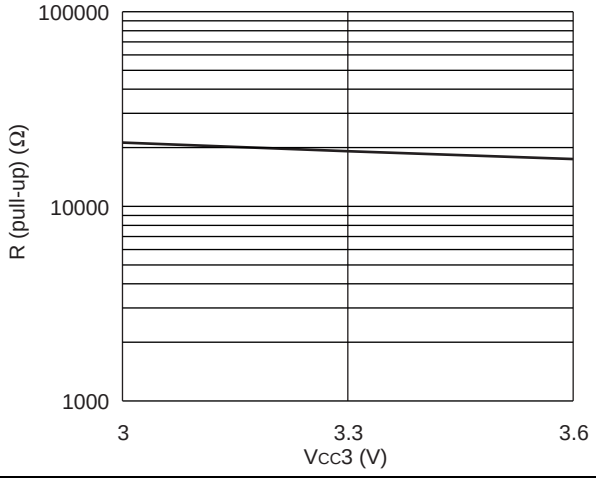
I_R – AVRH
(Ta = +25 °C, CLKP = 33 MHz)



I_{DA} – DAVC
(Ta = +25 °C, CLKP = 33 MHz)



R (pull-up) – V_{CC3}
(Ta = +25 °C)

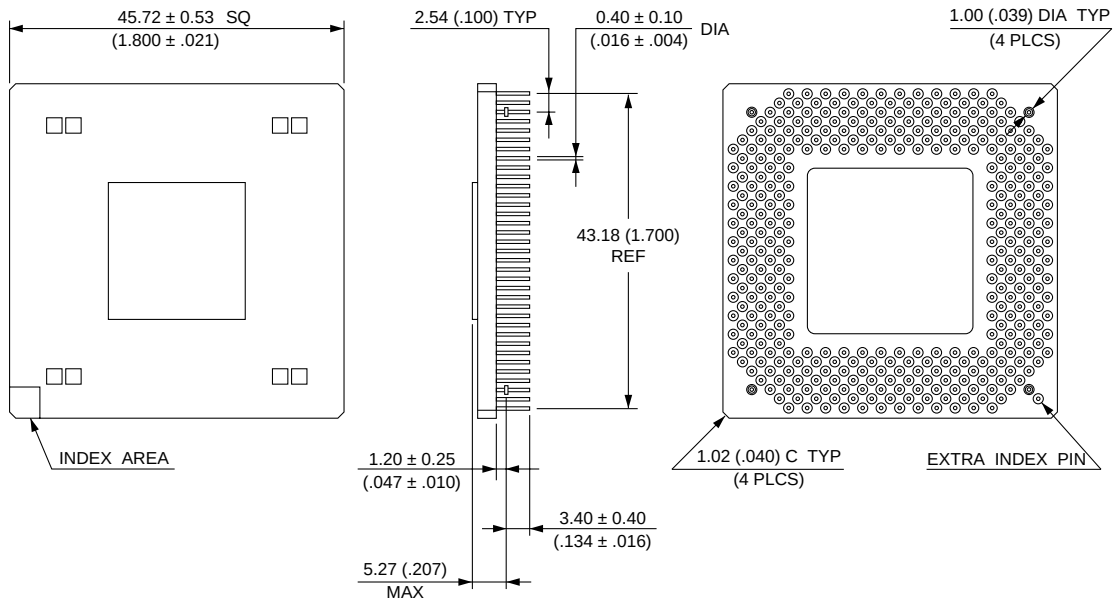


■ ORDERING IMFORMATION

Part No.	Package	Remarks
MB91340PMT	176-pin Plastic LQFP (FPT-176P-M02)	
MB91V340CR	361-pin Ceramic PGA (PGA-361C-A01)	

■ PACKAGE DIMENSIONS

361-pin Ceramic PGA
(PGA-361C-A01)



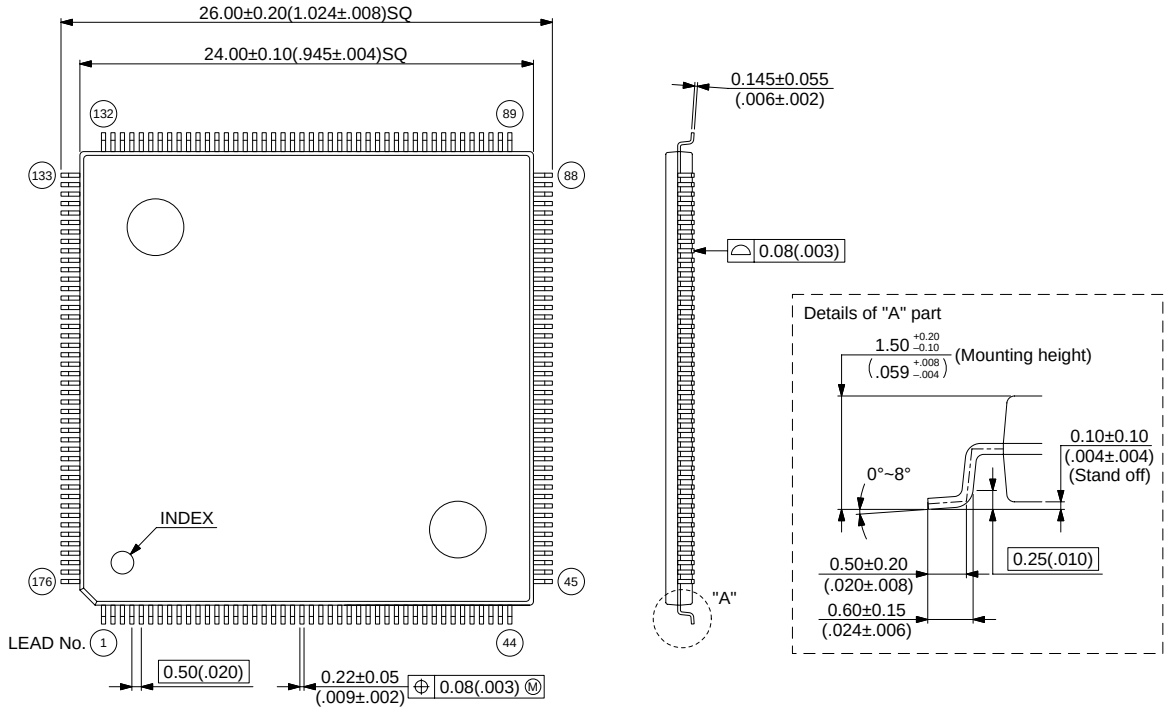
Dimensions in mm (inches)

(Continued)

(Continued)

176-pin Plastic LQFP
(FPT-176P-M02)

*Pins width and pins thickness include plating thickness.



Dimensions in mm (inches)

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F0203