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DESCRIPTION

PT2313L is a four-channel digital control audio processor utilizing CMOS technology. Volume, Bass, Balance, Front/Rear Fader Processor, Selectable Input Gain are incorporated into a single chip having the highest performance and reliability with the least external components. All functions are programmable using the I^2C Bus. PT2313L is housed in 20-pin or 28-pin DIP/SOP package. The 28-pin version provides additional Two Band Tone Control and Loudness Function and is pin-to-pin compatible with TDA7313. Pin assignments and application circuits are optimized for easy PCB layout and cost saving advantages.

FEATURES

- CMOS Technology
- Least External Components
- Treble and Bass Control (available only in the 28-pin version)
- Loudness Function (available only in the 28-pin version)
- 3 Stereo Inputs with Selectable Input Gain
- Input/Output for External Noise Reduction System/Equalizer
- 4 Independent Speaker Controls for Fader and Balance
- Independent Mute Function
- Volume Control in 1.25 dB/step
- Low Distortion
- Low Noise and DC Stepping
- Controlled by I^2C Bus Micro-Processor Interface
- Pin-to-Pin Compatible with TDA7313 (for 28-pin version)

APPLICATIONS

- Car Stereo (Audio)
- Hi-Fi Audio System
- LCD Monitor

Note: Purchase of I^2C Component of Princeton Technology Corporation (PTC) conveys a license under Philips I^2C Patent. Right to use these components in any I^2C System, provided that the system conforms to the I^2C Standard Specification defined by Philips.

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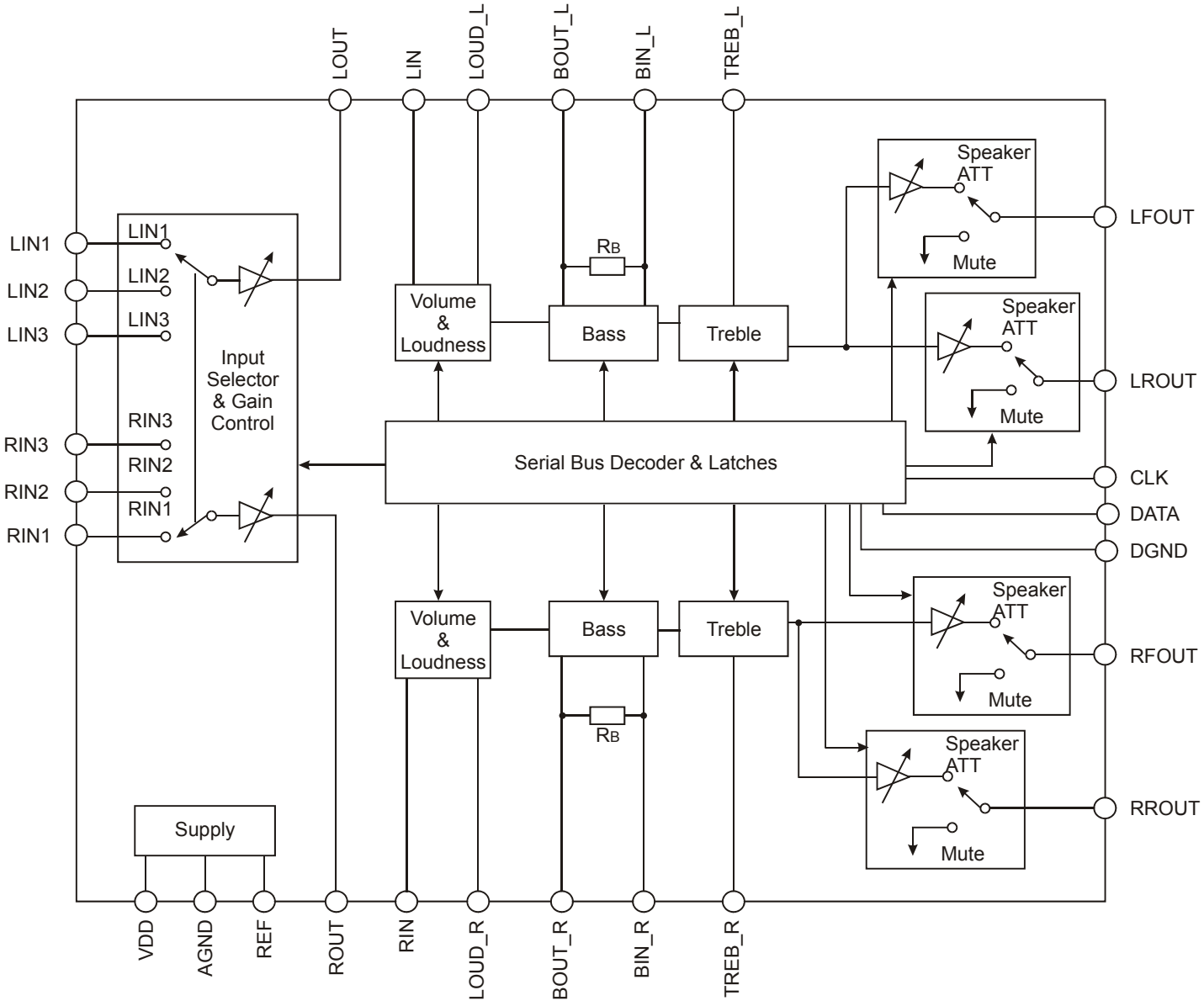
BLOCK DIAGRAM



Note: PT2313L (20-pin version) does not provide LOUDNESS Function (LOUD_L/LOUD_R) and Tone Control (TREB_L/TREB_R, BIN_L/BIN_R, BOUT_L/BOUT_R).

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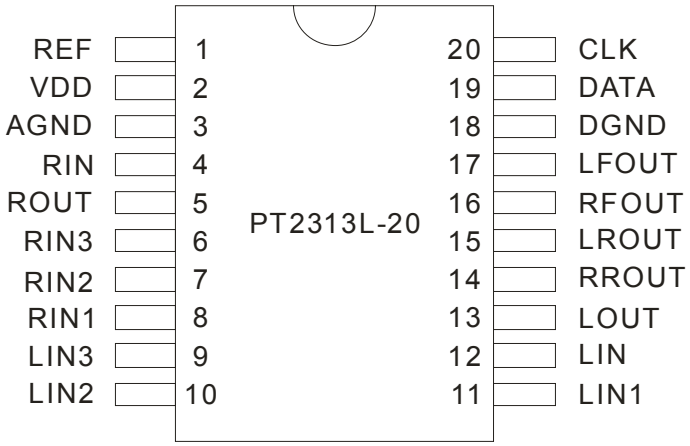
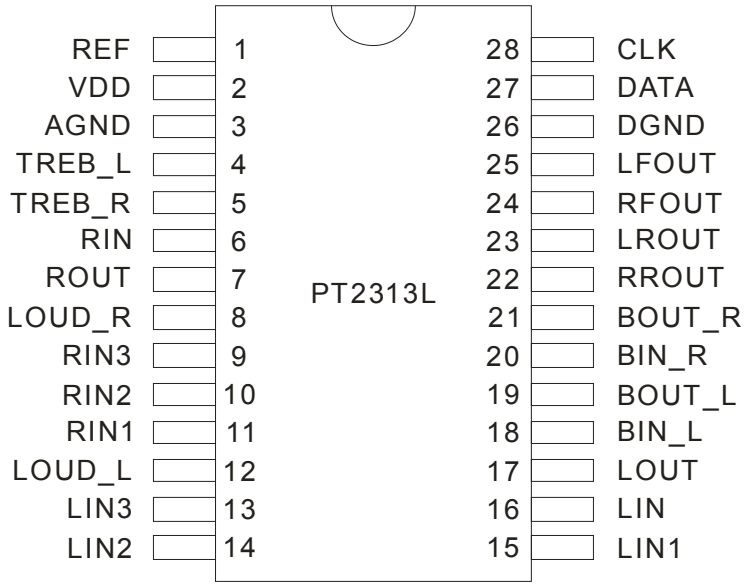
PIN CONFIGURATION





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PIN DESCRIPTION

Pin Name	I/O	Description	Pin No.
REF	-	Analog reference voltage (1/2VDD)	1
VDD	-	Supply input voltage	2
AGND	-	Analog ground	3
TREB_L	I	Left channel input for treble controller	4
TREB_R	I	Right channel input for treble controller	5
RIN	I	Audio processor right channel input	6
ROUT	O	Gain output and input selector for right channel	7
LOUD_R	I	Right channel loudness input	8
RIN3	I	Right channel input 3	9
RIN2	I	Right channel input 2	10
RIN1	I	Right channel input 1	11
LOUD_L	I	Left channel loudness input	12
LIN3	I	Left channel input 3	13
LIN2	I	Left channel input 2	14
LIN1	I	Left channel input 1	15
LIN	I	Audio processor left channel input	16
LOUT	O	Gain output and input selector for left channel	17
BIN_L	I	Left channel input for bass controller	18
BOUT_L	O	Left channel output for bass controller	19
BIN_R	I	Right channel input for bass controller	20
BOUT_R	O	Right channel output for bass controller	21
RROUT	O	Right rear speaker output	22
LROUT	O	Left rear speaker output	23
RFOUT	O	Right front speaker output	24
LFOUT	O	Left front speaker output	25
DGND	-	Digital ground	26
DATA	I	Control data input	27
CLK	I	Clock input for serial data transmission	28

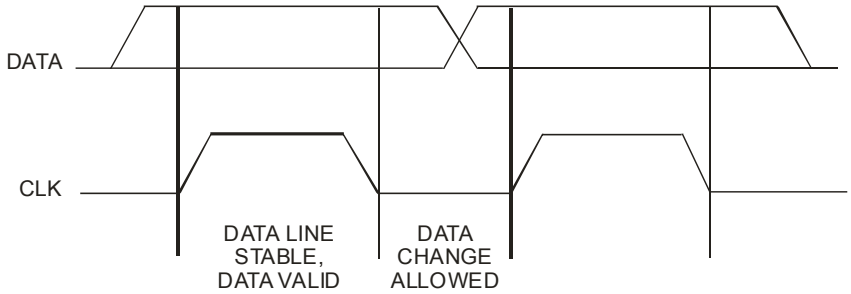
I²C BUS INTERFACE FUNCTION DESCRIPTION

BUS INTERFACE

Data are transmitted to and from the microprocessor to the PT2313L via the DATA and CLK. The DATA and CLK make up the BUS Interface. It should be noted that the pull-up resistors must be connected to the positive supply voltage.

DATA VALIDITY

A data on the DATA Line is considered valid and stable only when the CLK Signal is in HIGH State. The HIGH and LOW States of the DATA Line can only change when the CLK signal is LOW. Please refer to the figure below.



START AND STOP CONDITIONS

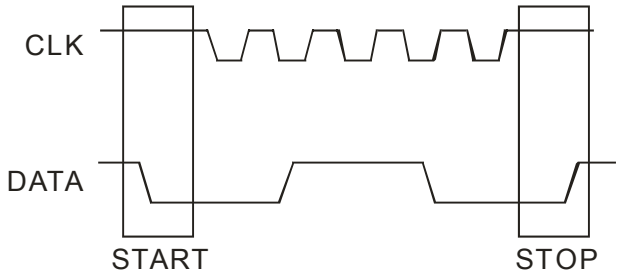
A Start Condition is activated when

1. the CLK is set to HIGH and
2. DATA shifts from HIGH to LOW State.

The Stop Condition is activated when

1. CLK is set to HIGH and
2. DATA shifts from LOW to HIGH State.

Please refer to the timing diagram below.

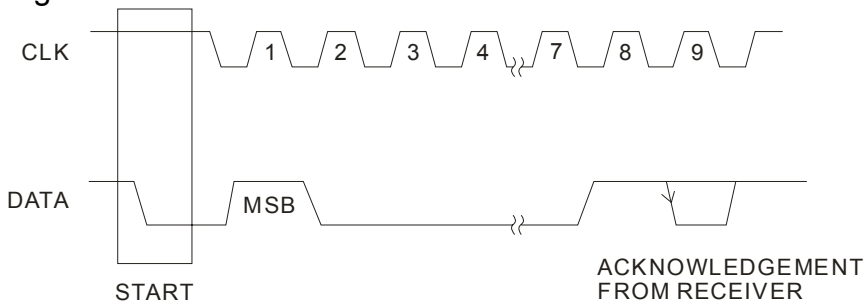


BYTE FORMAT

Every byte transmitted to the DATA Line consists of 8 bits. Each byte must be followed by an Acknowledge Bit. The MSB is transmitted first.

ACKNOWLEDGE

During the Acknowledge Clock Pulse, the master (μP) puts a resistive HIGH level on the DATA Line. The peripheral (audio processor) that acknowledges has to pull-down (LOW) the DATA line during the Acknowledge Clock Pulse so that the DATA Line is in a Stable Low State during this Clock Pulse. Please refer to the diagram below.



The audio processor that has been addressed has to generate an Acknowledge after receiving each byte, otherwise, the DATA Line will remain at the High Level during the ninth (9th) Clock Pulse. In this case, the master transmitter can generate the STOP Information in order to abort the transfer.

TRANSMISSION WITHOUT ACKNOWLEDGE

If you want to avoid the acknowledge detection of the audio processor, a simpler μP transmission may be used. Wait one clock and do not check the slave acknowledge of this same clock then send the new data. If you use this approach, there are greater chances of faulty operation as well as decrease in noise immunity.

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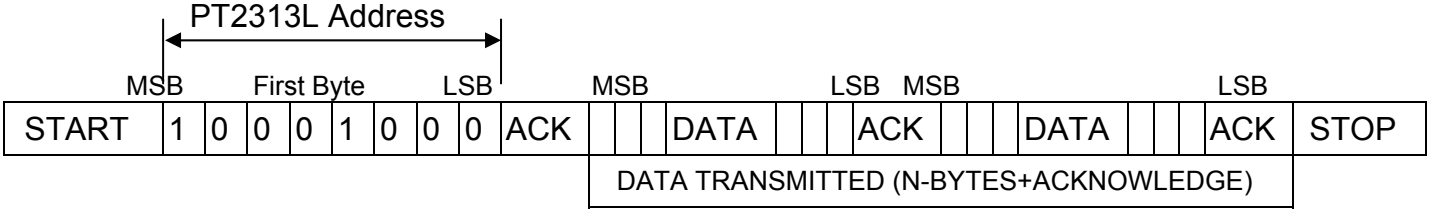
INTERFACE PROTOCOL

The interface protocol consists of the following:

- A Start bit
- A Chip Address Byte=88H
- ACK=Acknowledge bit
- A Data byte
- A Stop bit

Please refer to the diagram below:



Notes:
1. ACK=Acknowledge
2. Max. Clock Speed=100K BITS/S

SOFTWARE SPECIFICATION

PT2313L Address

PT2313L Address is shown below.

1 MSB	0	0	0	1	0	0	0 LSB

Data Bytes

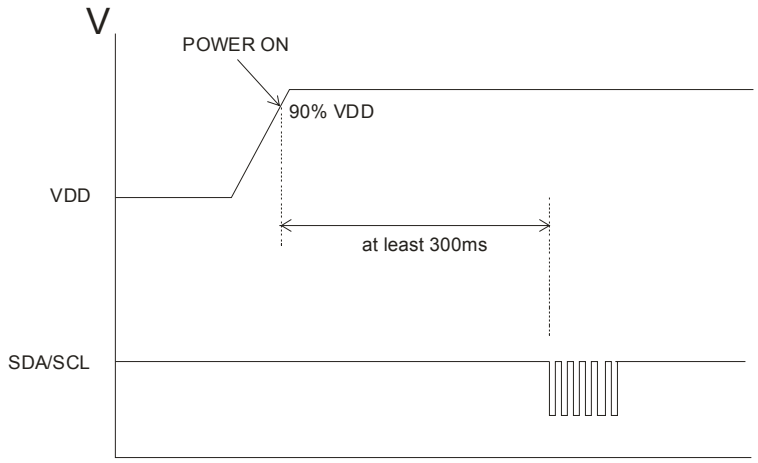
MSB							LSB	FUNCTION
0	0	B2	B1	B0	A2	A1	A0	Volume Control
1	1	0	B1	B0	A2	A1	A0	Speaker ATT LR
1	1	1	B1	B0	A2	A1	A0	Speaker ATT RR
1	0	0	B1	B0	A2	A1	A0	Speaker ATT LF
1	0	1	B1	B0	A2	A1	A0	Speaker ATT RF
0	1	0	G1	G0	S2	S1	S0	Audio Switch
0	1	1	0	C3	C2	C1	C0	Bass Control *
0	1	1	1	C3	C2	C1	C0	Treble Control *

where: Ax=1.25dB/steps; Bx=10dB/steps; Cx=2dB/steps; Gx=3.75dB/steps

Note: *=Only the 28-pin version provides the Loudness and the Tone Control Functions

I²C BUS INTERFACE START TIME

After Power is turned ON, PT2313L needs to wait for a short time in order to insure stability. This waiting period is relative to the value of Cref. As the Cref value is 10μf, the waiting time period for PT2313L to send I²C Bus Signal is at least 300ms. If the waiting time period is less than 300ms, I²C Control may fail. Please refer to the diagram below.



VOLUME

The table below gives a detailed description of the Volume Data Bytes. For example, a volume of -37.5 dB is given by 0 0 0 1 1 1 1 0.

MSB							LSB	Function
0	0	B2	B1	B0	A2	A1	A0	Volume 1.25dB/steps
					0	0	0	0
					0	0	1	-1.25
					0	1	0	-2.5
					0	1	1	-3.75
					1	0	0	-5
					1	0	1	-6.25
					1	1	0	-7.5
					1	1	1	-8.75
0	0	B2	B1	B0	A2	A1	A0	Volume 10dB/steps
		0	0	0				0
		0	0	1				-10
		0	1	0				-20
		0	1	1				-30
		1	0	0				-40
		1	0	1				-50
		1	1	0				-60
		1	1	1				-70

SPEAKER ATTENUATORS

The table below gives a detailed description of the speaker attenuators data bytes. For example, an attenuation of 30dB on the Speaker lF (Right Front) is given by: 1 0 0 1 1 0 0 0.

MSB							LSB	Function
1	0	0	B1	B0	A2	A1	A0	Speaker LF
1	0	1	B1	B0	A2	A1	A0	Speaker RF
1	1	0	B1	B0	A2	A1	A0	Speaker LR
1	1	1	B1	B0	A2	A1	A0	Speaker RR
					0	0	0	0
					0	0	1	-1.25
					0	1	0	-2.5
					0	1	1	-3.75
					1	0	0	-5
					1	0	1	-6.25
					1	1	0	-7.5
					1	1	1	-8.75
			0	0				0
			0	1				-10
			1	0				-20
			1	1				-30
			1	1	1	1	1	Mute

AUDIO SWITCH DATA BYTE

The following table shows the detailed description of the Audio Switch Data Bytes. For example, (in a 28-pin PT2313L version) a Stereo 1 Input with Gain of +11.25dB Loudness ON is given by: 0 1 0 0 0 0 0 0.

MSB							LSB	Function
0	1	0	G1	G0	S2	S1	S0	Audio Switch
						0	0	Stereo 1
						0	1	Stereo 2
						1	0	Stereo 3
						1	1	Stereo 4 *
					0			Loudness ON **
					1			Loudness OFF **
			0	0				+11.25dB
			0	1				+7.5dB
			1	0				+3.75dB
			1	1				0dB

Notes:
1. *=Stereo 4 is internally connected.
2. **=Only available in the 28-pin version.

*BASS AND TREBLE DATA BYTES **

The following table shows a detailed description of the Bass and Treble Data Byte. For example a Treble at -12dB is given by: 0 1 1 1 0 0 0 1.

MSB							LSB	Function
0	1	1	0	C3	C2	C1	C0	Bass
0	1	1	1	C3	C2	C1	C0	Treble
				0	0	0	0	-14
				0	0	0	1	-12
				0	0	1	0	-10
				0	0	1	1	-8
				0	1	0	0	-6
				0	1	0	1	-4
				0	1	1	0	-2
				0	1	1	1	0
				1	1	1	1	0
				1	1	1	0	2
				1	1	0	1	4
				1	1	0	0	6
				1	0	1	1	8
				1	0	1	0	10
				1	0	0	1	12
				1	0	0	0	14

Unit: dB

Notes:
1. *=This is only applicable for the PT2313L 28-pin version.
2. The 20-pin version does not provide the Tone Control Function (Treble and Bass).

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min.	Max.	Unit
Operating supply voltage	Vs		10.5	V
Input current, any pin except supplies	Iin	-10	10	mA
Input voltage (Note 1)	Vin	-0.3	VS+0.3	V
Operating temperature	Topr	-40	85	℃
Storage temperature	Tstg	-65	150	℃

Note: Transient Currents of up to 100mA will not cause SCR latch-up.

QUICK REFERENCE DATA

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	Vs	6	9	10	V
Max. input signal handling	VCL	2	2.5		Vrms
Total harmonic distortion (V=1Vrms, f=1KHz)	THD		0.07	0.15	%
Signal to noise ratio	S/N		95		dB
Channel separation (f=1KHz)	Sc		85		dB
Volume control 1.25dB/step		-75		0	dB
Bass & treble control 2dB/step		-14		+14	dB
Fader & balance control 1.25dB/step		-37.5		0	dB
Input gain 3.75dB/step	GIN	0		11.25	dB
Mute attenuation	AMUTE		85		dB

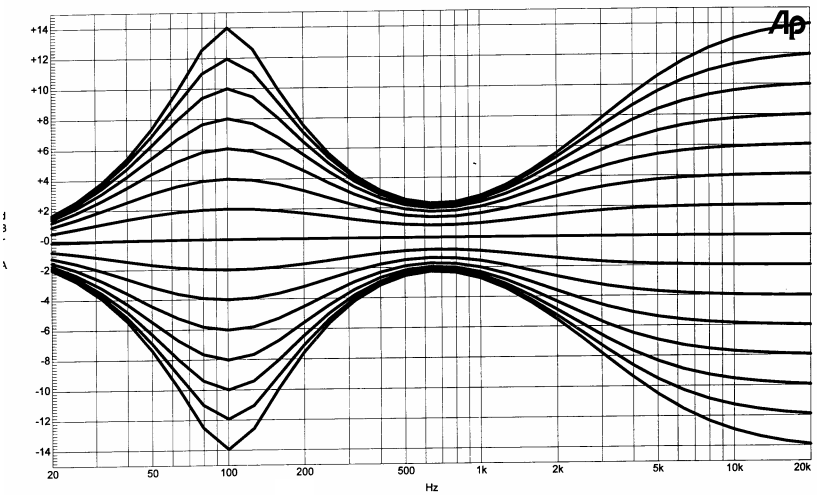
ELECTRICAL CHARACTERISTICS

(Unless specified: Ta=25℃, Vc=9V, RL=100KΩ, Rg=600Ω, all controls flat (G=0), f=1KHz)

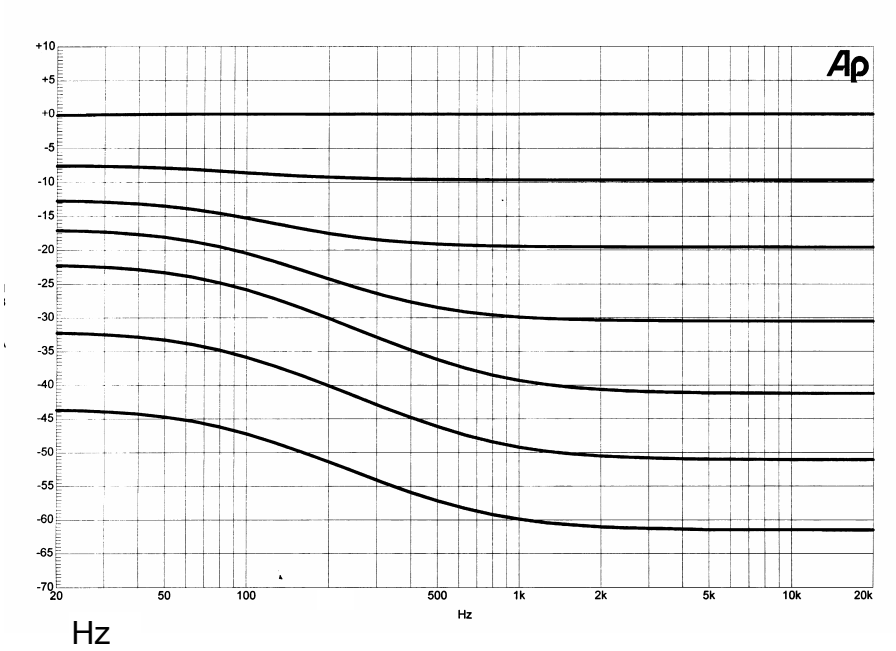
Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Supply						
Supply Voltage	VDD		6	9	10	V
Supply Current	Is			30	40	mA
Input Selectors						
Input Resistance	RII	Input 1, 2, 3	35	50	70	KΩ
Clipping Level	VCL	Av=-8.75 dB ; d=0.3%	2	2.5		Vrms
Input Separation (2)	SIN		80	100		dB
Min. Input Gain	GINmin		-1	0	1	dB
Max. Input Gain	GINmax			11.25		dB
Volume Control						
Control Range	CRANGE		65	70	75	dB
Min. Attenuation	AVMIN		-1	0	1	dB
Max. Attenuation	AVMAX		65	70	75	dB
Step Resolution	ASTEP		0.5	1.25	1.75	dB
Attenuation Set Error	EA	AV=0 to -20dB AV=-20 to -60dB	-1.25 -3.0	0	1.25 2	dB dB
Speaker Attenuators						
Control Range	CRANGE		35	37.5	40	dB
Step Resolution	SSTEP		0.5	1.25	1.75	dB
Attenuation Set Error	EA				1.5	dB
Output Mute Attenuation	AMUTE		70	75		dB
Bass Control (1)						
Control Range	Gb	Max. Boost/Cut	±12	±14	±16	dB
Step Resolution	BSTEP		1	2	3	dB
Internal Feedback Resistance	RB		34	44	58	KΩ
Treble Control (1)						
Control Range	Gt	Max. Boost/Cut	±13	±14	±15	dB
Step Resolution	TSTEP		1	2	3	dB
Audio Outputs						
Clipping Level	VOCL	AV=-8.75dB, d=0.3%	2	2.5		Vrms
Output Resistance	ROUT		-	40	45	Ω
DC Voltage Level	VOUT		4.2	4.5	4.8	V

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
General						
Output Noise	NO	BW=20~20KHz, Flat Output Mute All gains=0dB		-97 -92		dB dB
		A Curve All Gains=0dB		-100		dB
Signal to Noise Ratio	S/N	All Gains=0dB Vo=1Vrms		95		dB
Distortion	d	AV=0, VIN=1Vrms AV=-8.75dB, IN=1Vrms AV=-8.75dB, VIN=0.3Vrms		0.1 0.07 0.03	0.3 0.15 0.1	% % %
Channel Separation Left/Right	Sc		80	90		dB
Bus Inputs						
Input Low Voltage	VIL				1	V
Input High Voltage	VIH		3			V
Input Current	IIN		-5		+5	μA
Output Voltage SDA Acknowledge	Vo	Io=1.6mA			0.4	V

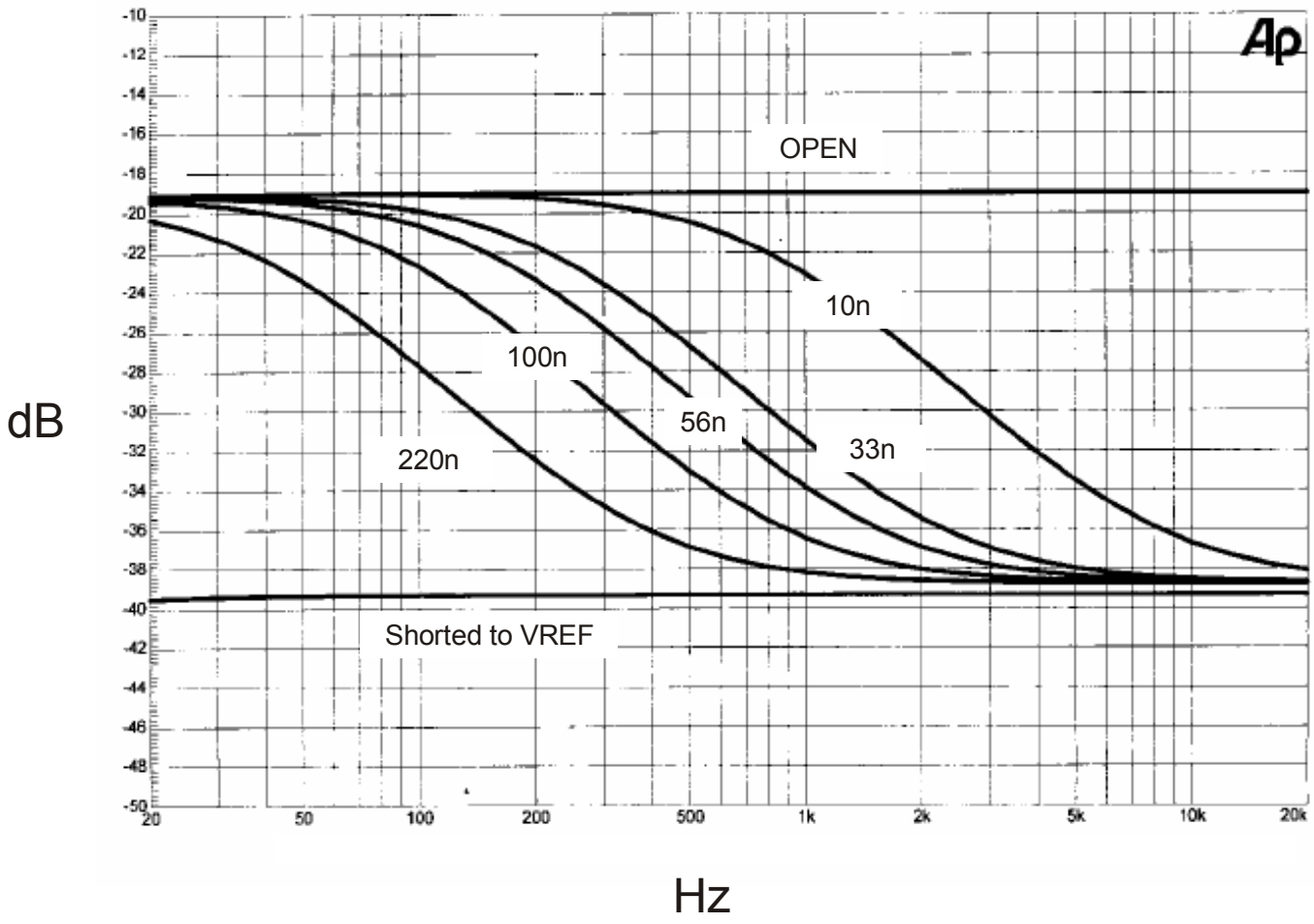
Notes:
1. For the Bass and Treble Response, please, refer to the diagram below. The center frequency and quality of the resonance behavior can be selected by the external circuitry. A standard first order bass response can realized by a standard feedback network.
2. The selected input is grounded thru the 2.2μF capacitor.



Typical Tone Response (with the ext. Components indicated in the test circuit)

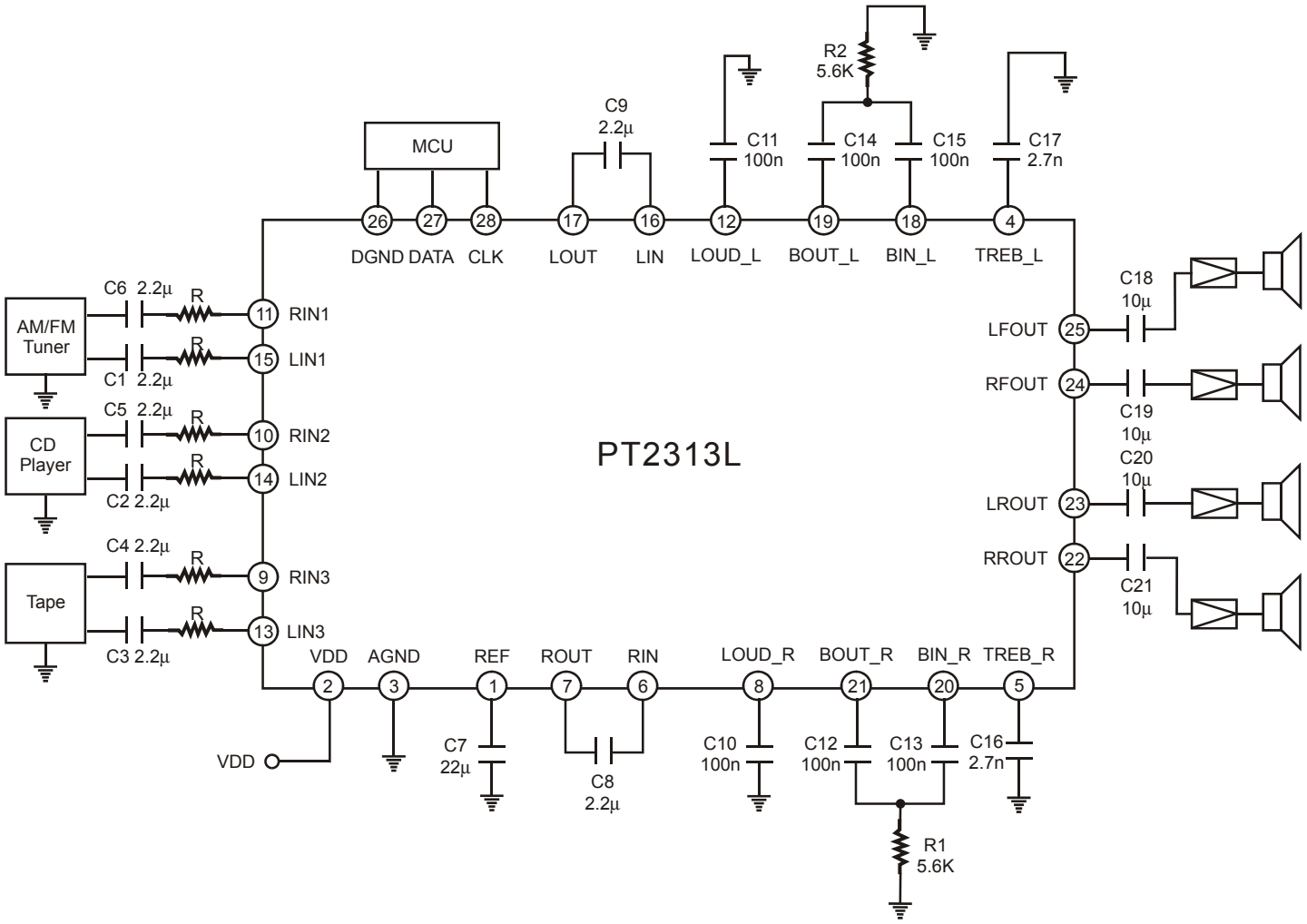


PT2313L: Loudness vs Volume Attenuation Frequency Response (C_{10}=C_{11}=100nF)



PT2313L: C_{10}, C_{11} vs Loudness Frequency Response (Volume=-40dB, all other controls are flat)

APPLICATION CIRCUIT



Notes:
1. The Resistor (R) Range=2.0KΩ to 3.6KΩ
2. Resistor (R) Recommended Value=2.4KΩ

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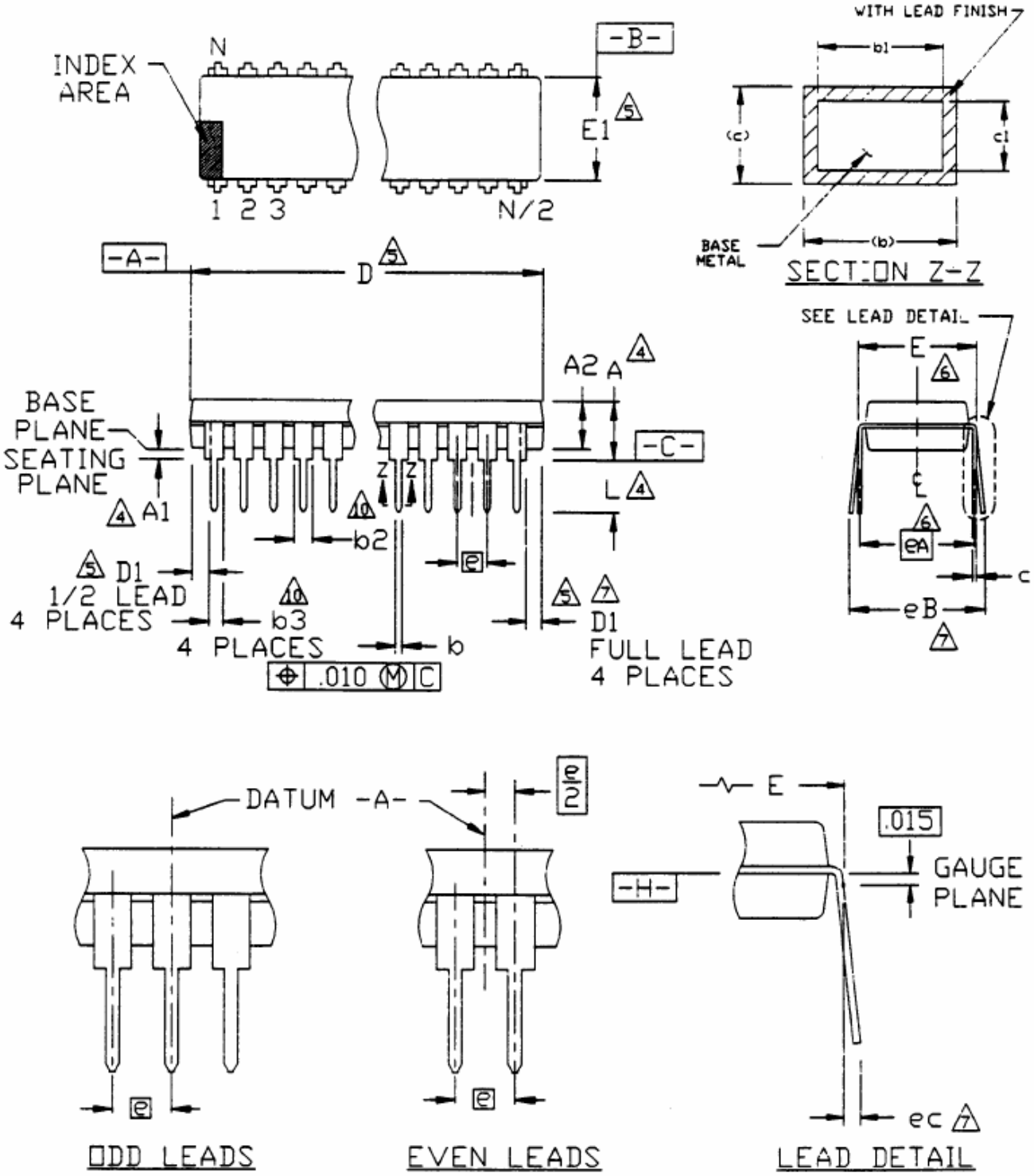
ORDER INFORMATION

Valid Part Number	Package Type	Top Code
PT2313L-D	28 Pins, DIP, 300mil	PT2313L-D
PT2313L	28 Pins, SOP, 300mil	PT2313L
PT2313L-20	20 Pins, SSOP, 150mil	PT2313L-20
PT2313L-D (L)	28 Pins, DIP, 300mil	PT2313L-D
PT2313L (L)	28 Pins, SOP, 300mil	PT2313L
PT2313L-20 (L)	20 Pins, SSOP, 150mil	PT2313L-20

Notes:
1. (L), (C) or (S) = Lead Free.
2. The Lead Free mark is put in front of the date code.

PACKAGE INFORMATION

28 PINS, DIP, 300MIL



Symbol	Min.	Nom.	Max.
A	-	-	0.210
A1	0.015	-	-
A2	0.115	0.130	0.195
b	0.014	0.018	0.022
b1	0.014	0.018	0.020
b2	0.045	0.060	0.070
b3	0.030	0.039	0.045
c	0.008	0.010	0.014
c1	0.008	0.010	0.011
D	1.345	1.365	1.400
D1	0.005	-	-
E	0.300	0.310	0.325
E1	0.240	0.250	0.280
e	-	0.100 BSC	-
eA	-	0.300 BSC	-
eB	-	-	0.430
eC	0.000	-	0.060
L	0.115	0.130	0.150

Notes:
1. All dimensions are in INCHES.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension A, A1 and L are measured with the package seated in JEDEC Seating Plane Gauge GS-3.
4. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch.
5. E and eA measured with the leads constrained to be perpendicular to datum -C-.
6. eB and eC are measured at the lead tips with the leads constrained.
7. N is the number of terminal positions (N=28)
8. Pointed or rounded lead tips are preferred to ease insertion.
9. b2 and b3 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010” (0.25mm).
10. This variation is a ½ lead package.
11. Distance between leads including dambar protrusions to be 0.005 inch minimum.
12. Datum plane -H- coincident with the bottom of lead where lead exits body.
13. Refer to JEDEC MS-001 Variation BF.

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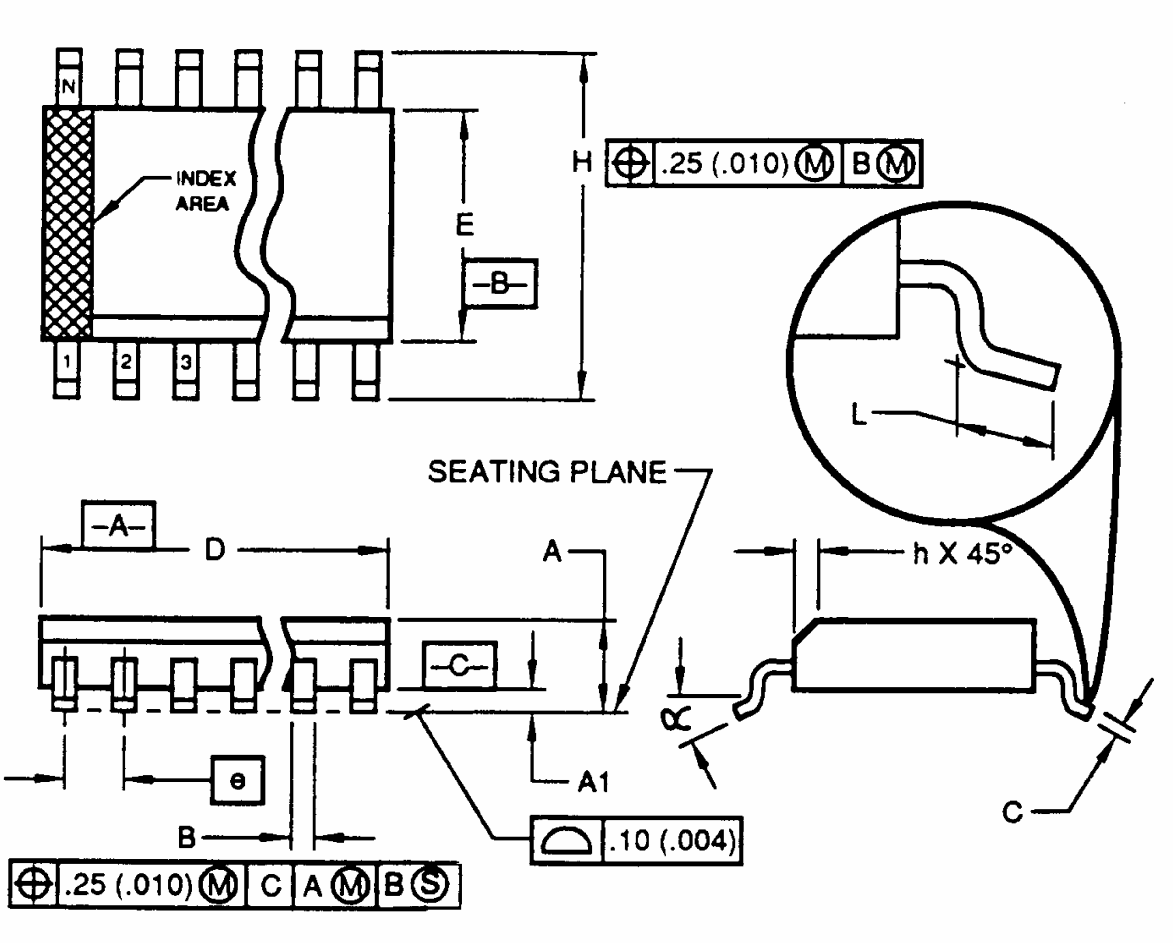
28 PINS, SOP, 300MIL



Symbol	Min.	Max
A	2.35	2.65
A1	0.10	0.30
B	0.33	0.51
C	0.23	0.32
D	17.70	18.10
E	7.40	7.60
e	1.27 bsc	
H	10.00	10.65
h	0.25	0.75
L	0.40	1.27
α	0°	8°

Notes:
1. Dimensioning and tolerancing per ANSI Y14.5-1982.
2. Dimension D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions and gate burrs shall not exceed 0.15mm (0.006 in) per side.
3. Dimension E does not include interlead flash or protrusions. Interlead flash and protrusion shall not exceed 0.15mm (0.016in) per side.
4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
5. L is the length of terminal for soldering to a substrate.
6. N is the number of terminal positions (N=28).
7. The lead width B as measured 0.36mm (0.014in) or greater above the seating plane, shall not exceed a maximum value of 0.61 mm (0.024 in).
8. Controlling dimension: MILLIMETER
9. Refer to JEDEC MS-013 Variation AE.

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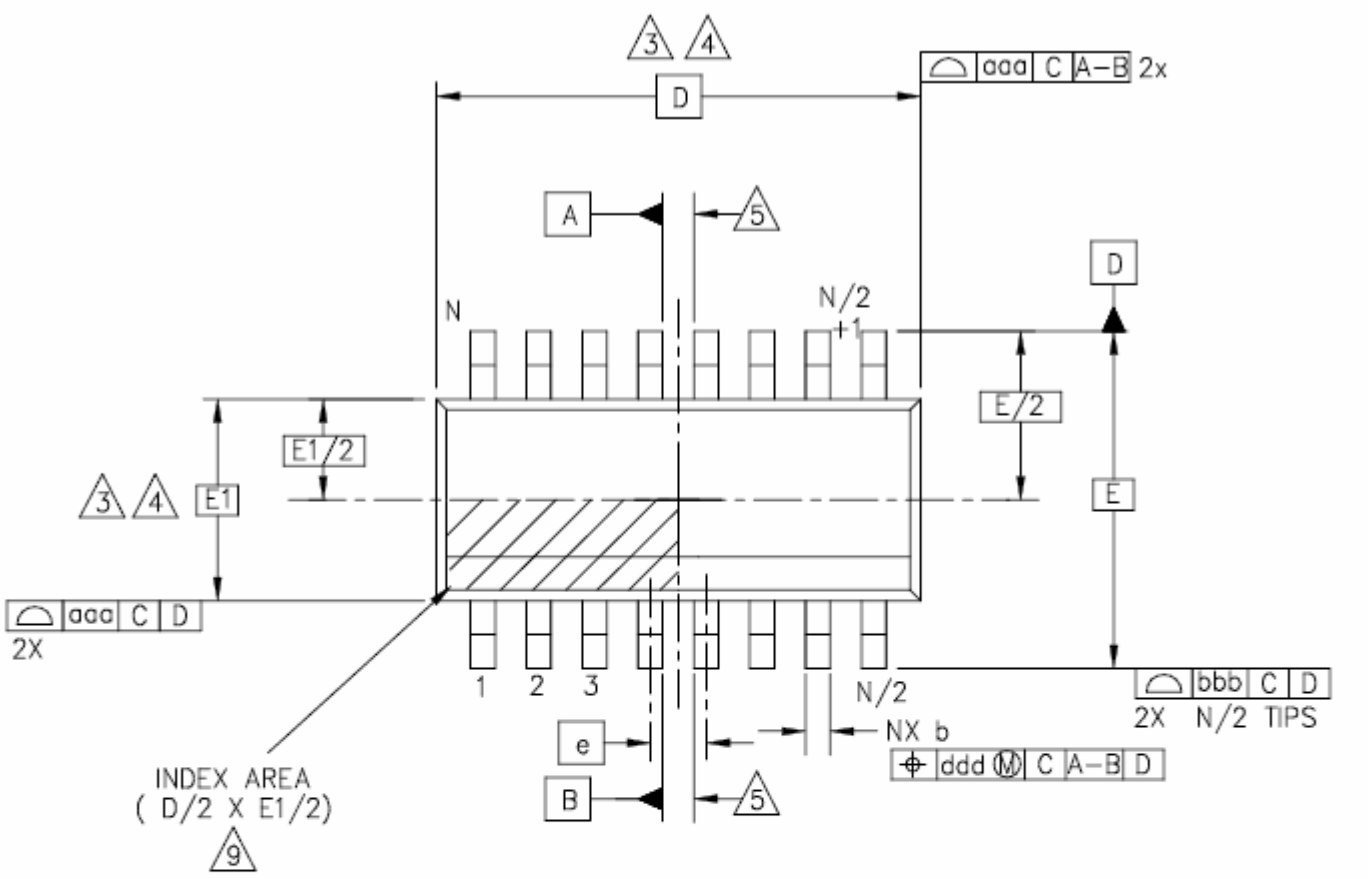
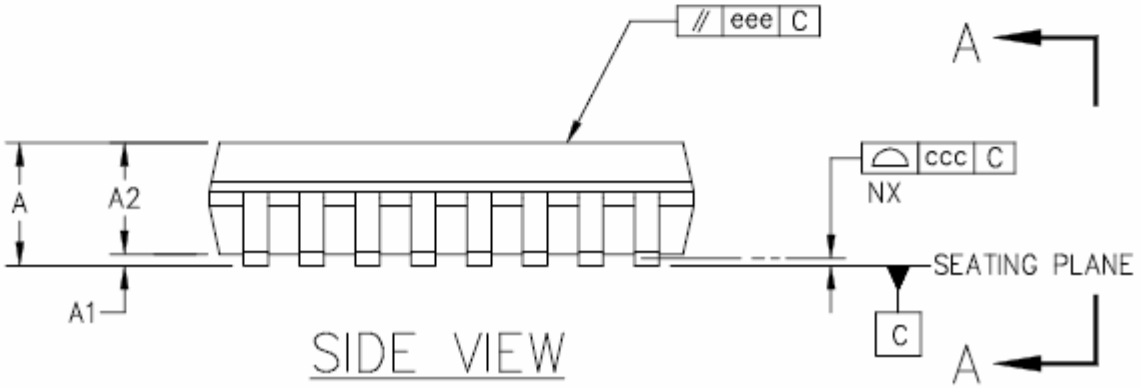
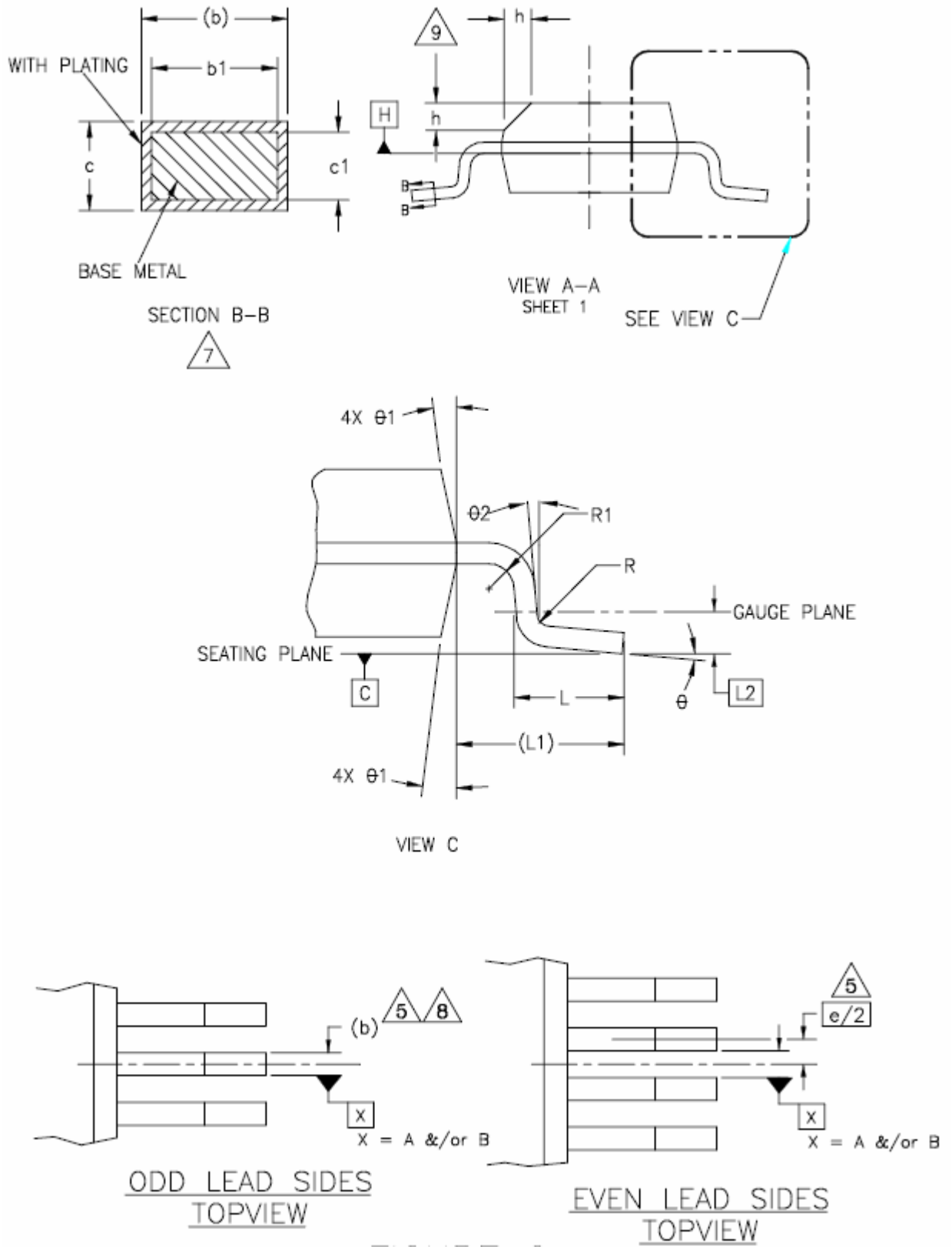
20 PINS, SSOP, 150MIL



TOP VIEW



SIDE VIEW


(b)
WITH PLATING
b1
c
c1
BASE METAL
SECTION B-B
7
9
h
H
h
B
B
VIEW A-A
SHEET 1
SEE VIEW C
4X θ1
θ2
R1
R
GAUGE PLANE
SEATING PLANE
C
L
θ
L2
(L1)
4X θ1
VIEW C
5
8
(b)
X
X = A &/or B
ODD LEAD SIDES
TOPVIEW
5
e/2
X
X = A &/or B
EVEN LEAD SIDES
TOPVIEW

Symbol	Min.	Nom.	Max.
A	0.053	-	0.069
A1	0.004	-	0.010
A2	0.049	-	0.065
b	0.008	-	0.012
b1	0.008	0.010	0.011
c	0.006	-	0.010
c1	0.006	0.008	0.009
D	0.341 BSC		
E	0.236 BSC		
E1	0.154 BSC		
e	0.025 BAS		
L	0.016	-	0.050
L1	0.041 REF		
L2	0.010 BAS		
R	0.003	-	-
R1	0.003	-	-
θ	0°	-	8°
θ1	5°	-	15°
θ2	0°	-	-
aaa	0.004		
bbb	0.008		
ccc	0.004		
ddd	0.007		
eee	0.004		

Notes:
1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. Dimensions in inches (angles in degrees)
3. Dimension D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.006” per end. Dimension E1 does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed “0.006” per side. D1 and E1 dimensions are determined at dutum H.
4. The package top may be smaller than the package bottom. Dimensions D and E1 are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs and interlead flash, but including any mismatch between the top and bottom of the plastic.
5. Datums A and B to be determined at datum H.
6. N is the maximum number of terminal position. (N=20)
7. The dimensions apply to the flat section of the lead between 0.004 to 0.010 inches from the lead tip.
8. Dimension b does not include dambar protrusion. Allowable dambar protrusion shall be 0.004” total in excess of b dimension at maximum material condition. The dambar can not be located on the lower radius of the foot.
9. Refer to JEDEC MO-137 variation AD.

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