

1 2 3 4 5 6 7 8

A

B

C

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E

F

A

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C

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E

F

S-SERIES 2009

INVICTA (Intel-Discrete)

MV Build (A03) - Final

2009.03.18

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| | | |
| | | |
| DATE | CHANGE NO. | REV |

| | | | | | |
|-------------|----------------|-------|-------|------|-----------------------|
| DRAWER | EE | DATE | POWER | DATE | INVENTEC |
| DESIGN | | | | | |
| CHECK | | | | | |
| RESPONSIBLE | | | | | |
| TITLE | | | | | <i>INVICTA Cycle1</i> |
| SIZE = | 3 | VER : | | | SIZE |
| FILE NAME : | XXXX-XXXXXX-XX | | | | CODE |
| P/N | XXXXXXXXXXXX | | | | A3 CS |
| | | | | | DOC. NUMBER |
| | | | | | 1310A22527-0-MTR |
| | | | | | REV |
| | | | | | A03 |
| | | | | | SHEET |
| | | | | | 1 OF 54 |

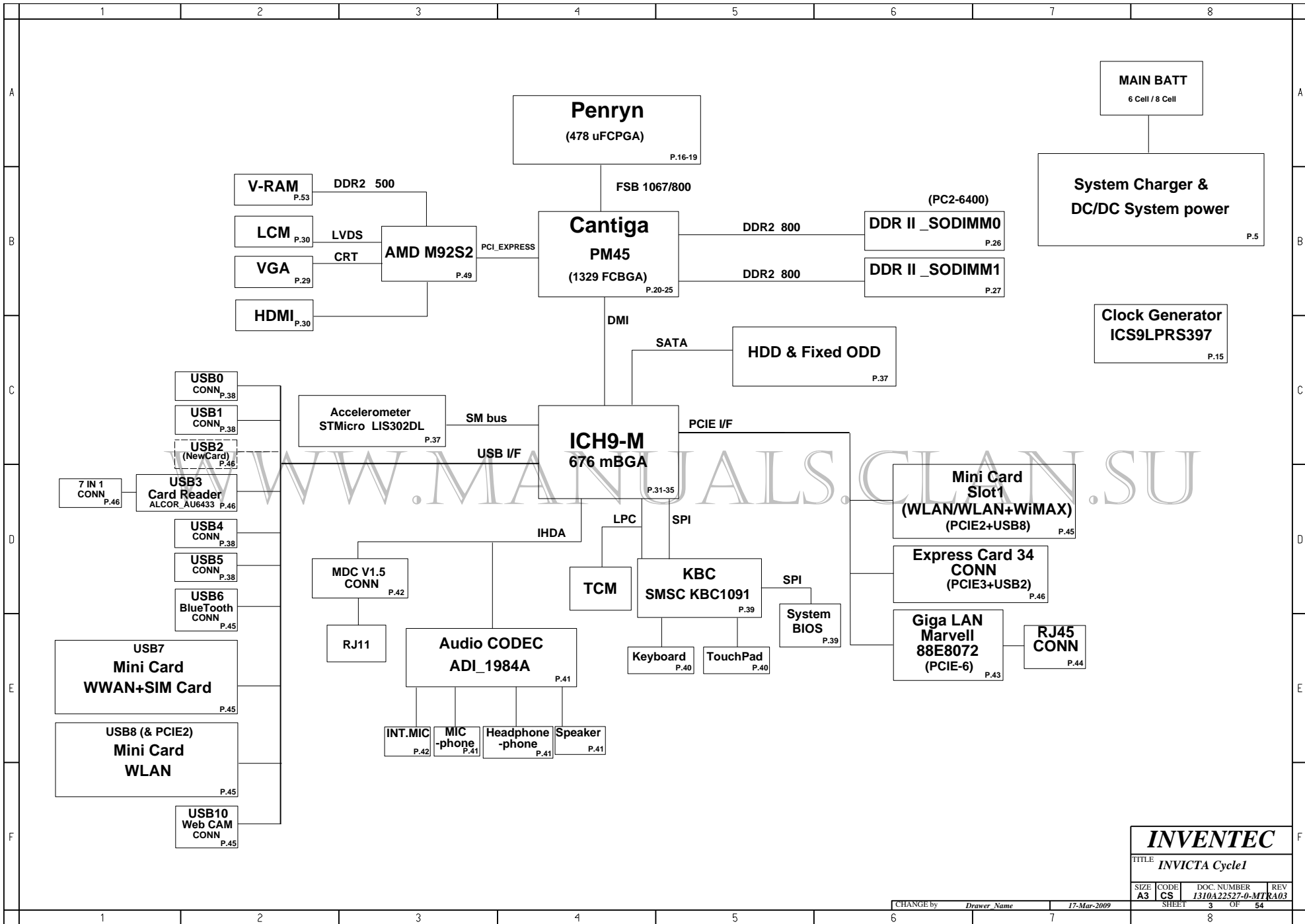
1 2 3 4 5 6 7 8

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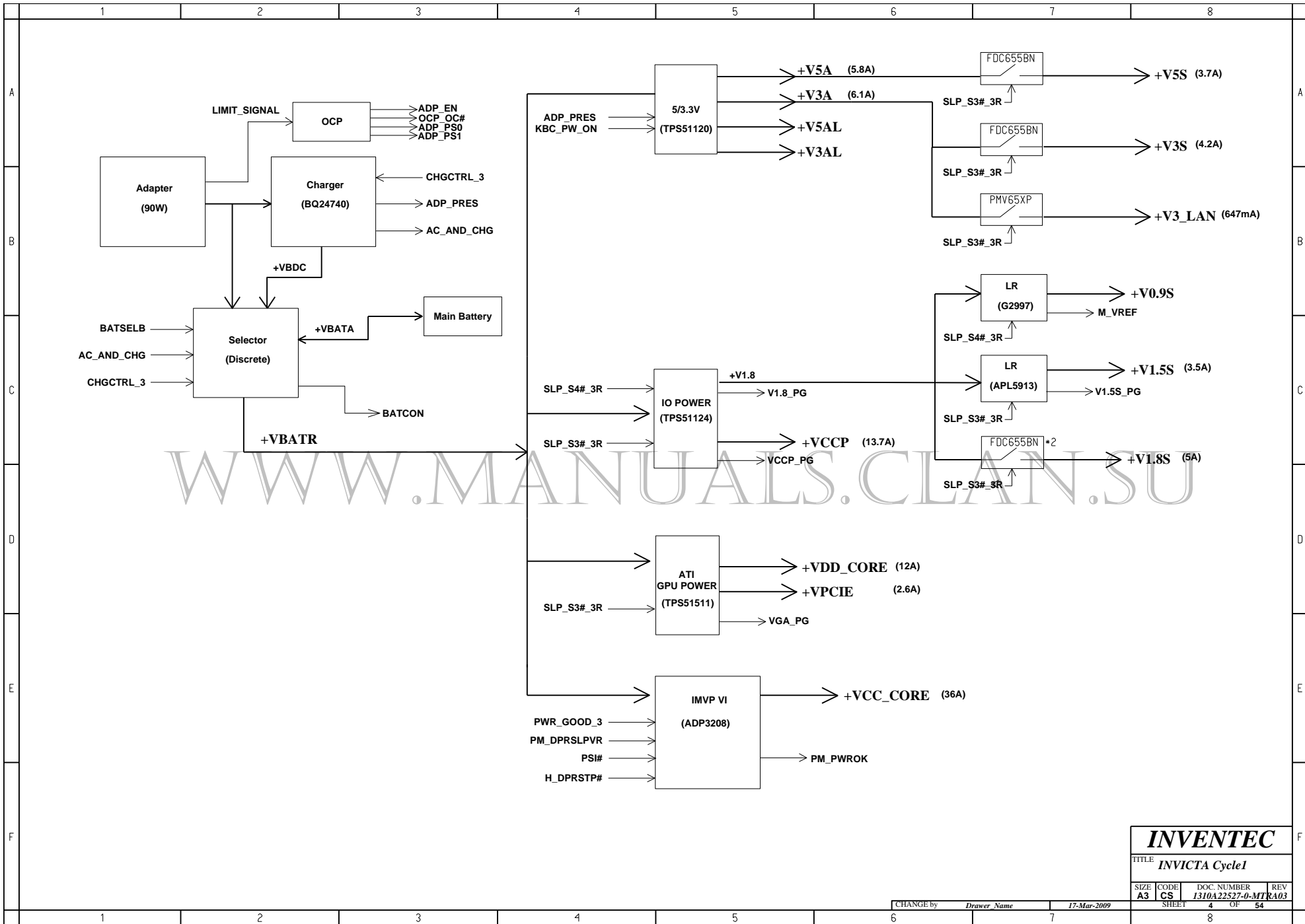
| Page | Page | Page |
|--|---------------------------|--|
| 5- DC & Battery Charger & OCP. | 15- Clock Generator. | 36- Power, LID, APP SW/B. |
| 6- Select & Battery CONN. | 16- CPU Penryn-1. | 37- HDD & ODD,Accelerometer,15" ODD EXT/B. |
| 7- System Power (+V3A/+V5A). | 17- CPU Penryn-2. | 38- USB CONN. |
| 8- System Power (+V1.8/+VCCP) . | 18- CPU Penryn-3. | 39- KBC, BIOS ROM, Debug Port. |
| 9- Graphic Power (+VDD_CORE & +VPCIE). | 19- XDP & Thermal & Fan. | 40- Internal Keyboard & TouchPad CONN. |
| 10- System Power (+V1.5S) . | 20- N/B Cantiga-1. | 41- Audio CODEC & Earphone & Speaker. |
| 11- CPU Power (+VCC_CORE). | 21- N/B Cantiga-2. | 42- Audio MIC & MDC CONN. |
| 12- DDR Termination Voltage(+V0.9S). | 22- N/B Cantiga-3. | 43- Giga LAN controller. |
| 13- Power (Sleep: +V5S/+V3S/+V1.8S). | 23- N/B Cantiga-4. | 44- Magnetic & RJ45 CONN. |
| 14- Power (Sequence). | 24- N/B Cantiga-5. | 45- Mini Card(WLAN/WWAN), BT. |
| | 25- N/B Cantiga-6. | 46- New Card & 4 in 1 Card (SD/MMC/MS/XD). |
| | 26- DDR2-DIMM0. | 47- LEDs, TCM CONN. |
| | 27- DDR2-DIMM1. | 48- Screws, Crack testing circuit. |
| | 28- DDR2-Termination. | 49- AMD M92S2-1. |
| | 29- VGA CONN. | 50- AMD M92S2-2. |
| | 30- LCD,WebCam,HDMI CONN. | 51- AMD M92S2-3. |
| | 31- S/B ICH9-1. | 52- AMD M92S2-4. |
| | 32- S/B ICH9-2. | 53- Video RAM-1 (DDR2). |
| | 33- S/B ICH9-3. | 54- Video RAM-2 (DDR2). |
| | 34- S/B ICH9-4. | |
| | 35- S/B ICH9-5. | |

INVENTEC

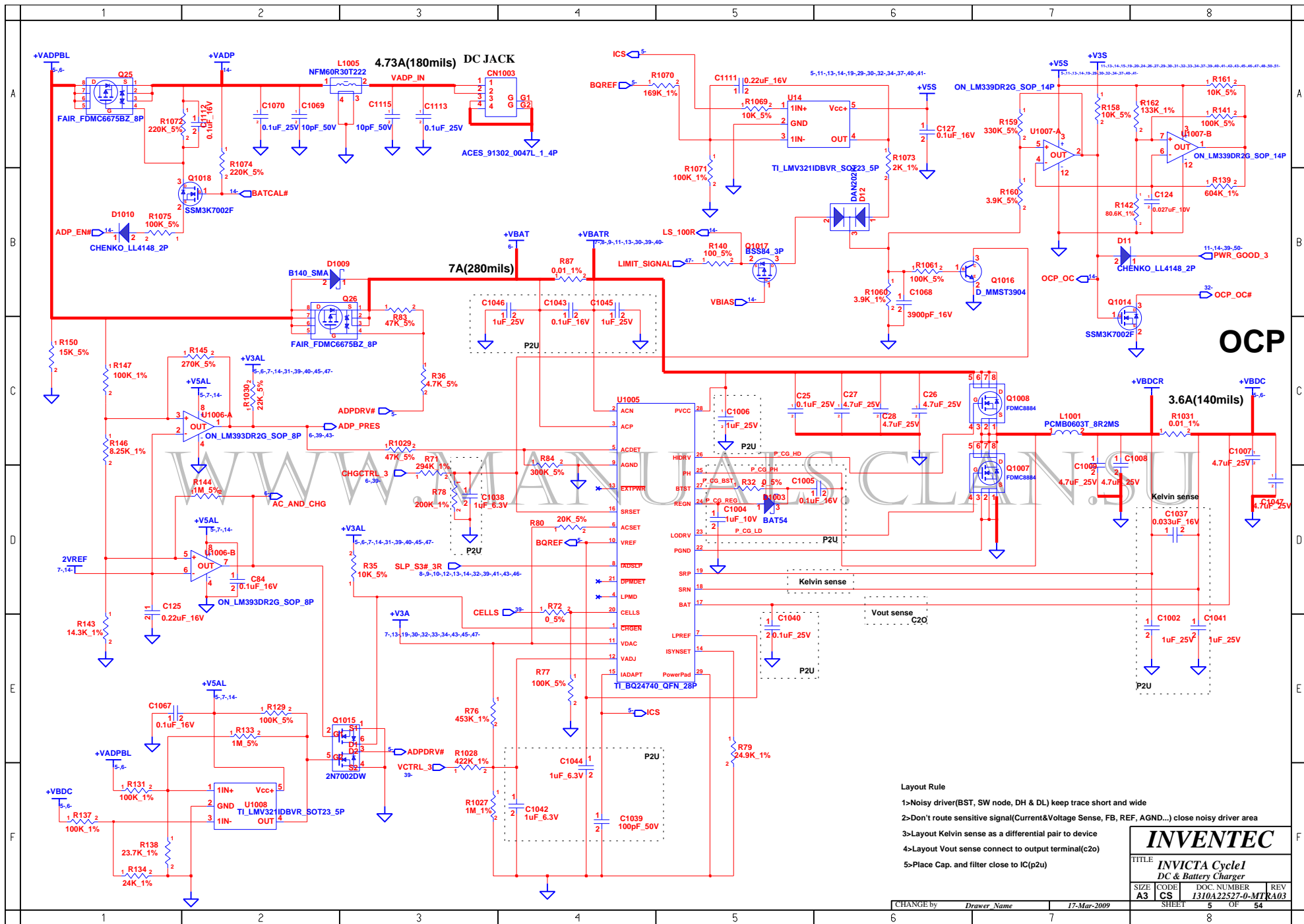
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| TITLE INVICTA Cycle1 Contents | | | |
| SIZE A3 | CODE CS | DOC NUMBER 1310A22527-0-MTR | REV A03 |
| CHANGE by <i>Drawer Name</i> | | 17-Mar-2009 | |
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| | | | |
|---------------------------------|-------------------|--|-----------------------------------|
| INVENTEC | | | |
| TITLE <i>INVICTA Cycle1</i> | | | |
| SIZE A3 | CODE CS | DOC. NUMBER <i>1310A22527-0-MTR</i> | REV A03 |
| CHANGE by <i>Drawer Name</i> | | 17-Mar-2009 | SHEET 3 OF 54 |

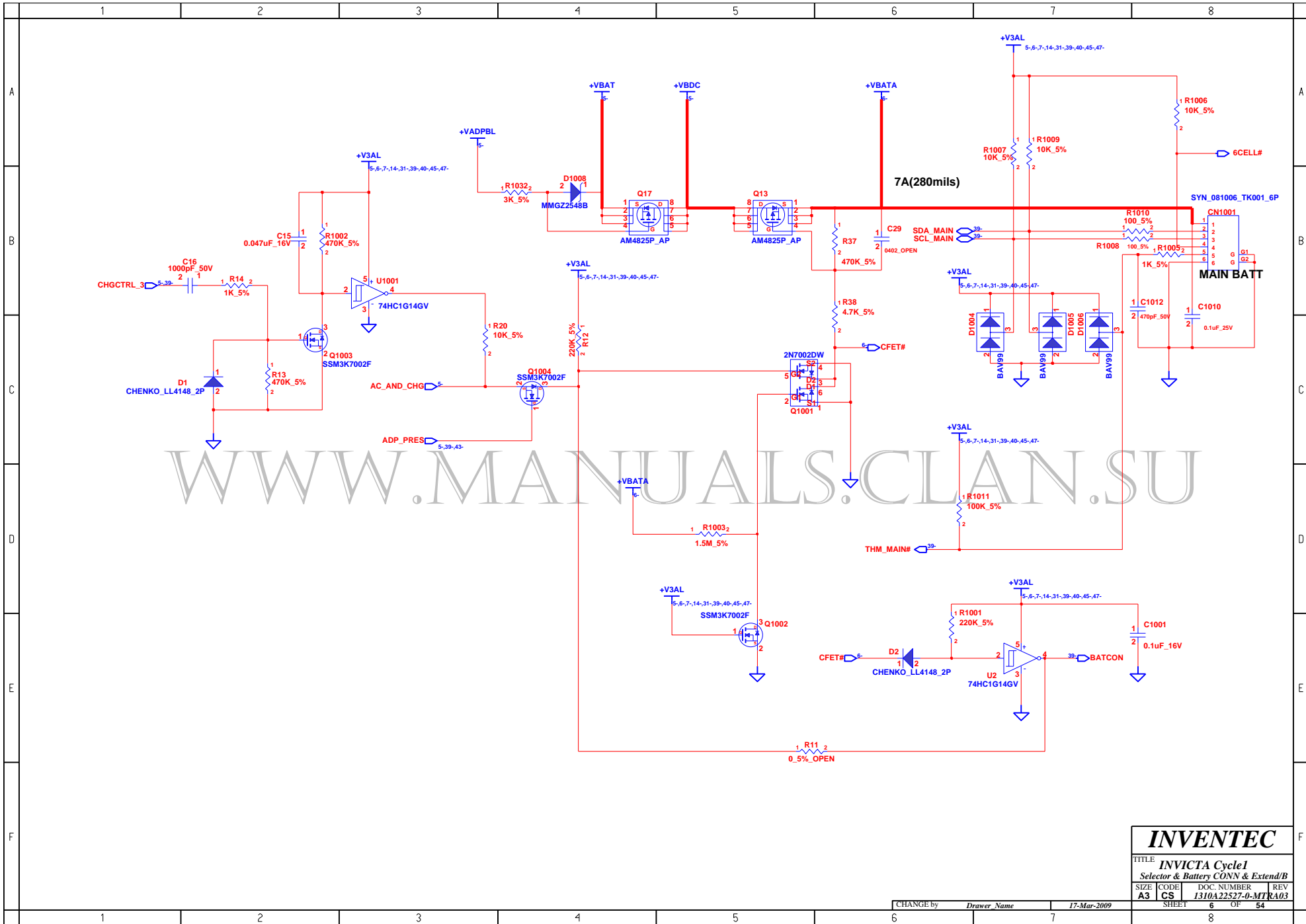


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|-----------------------|------|------------------|-------------|
| INVENTEC | | | |
| TITLE INVICTA Cycle 1 | | | |
| SIZE | CODE | DOC. NUMBER | REV |
| A3 | CS | 1310A22527-0-MTR | A03 |
| CHANGE by | | Drawer Name | 17-Mar-2009 |
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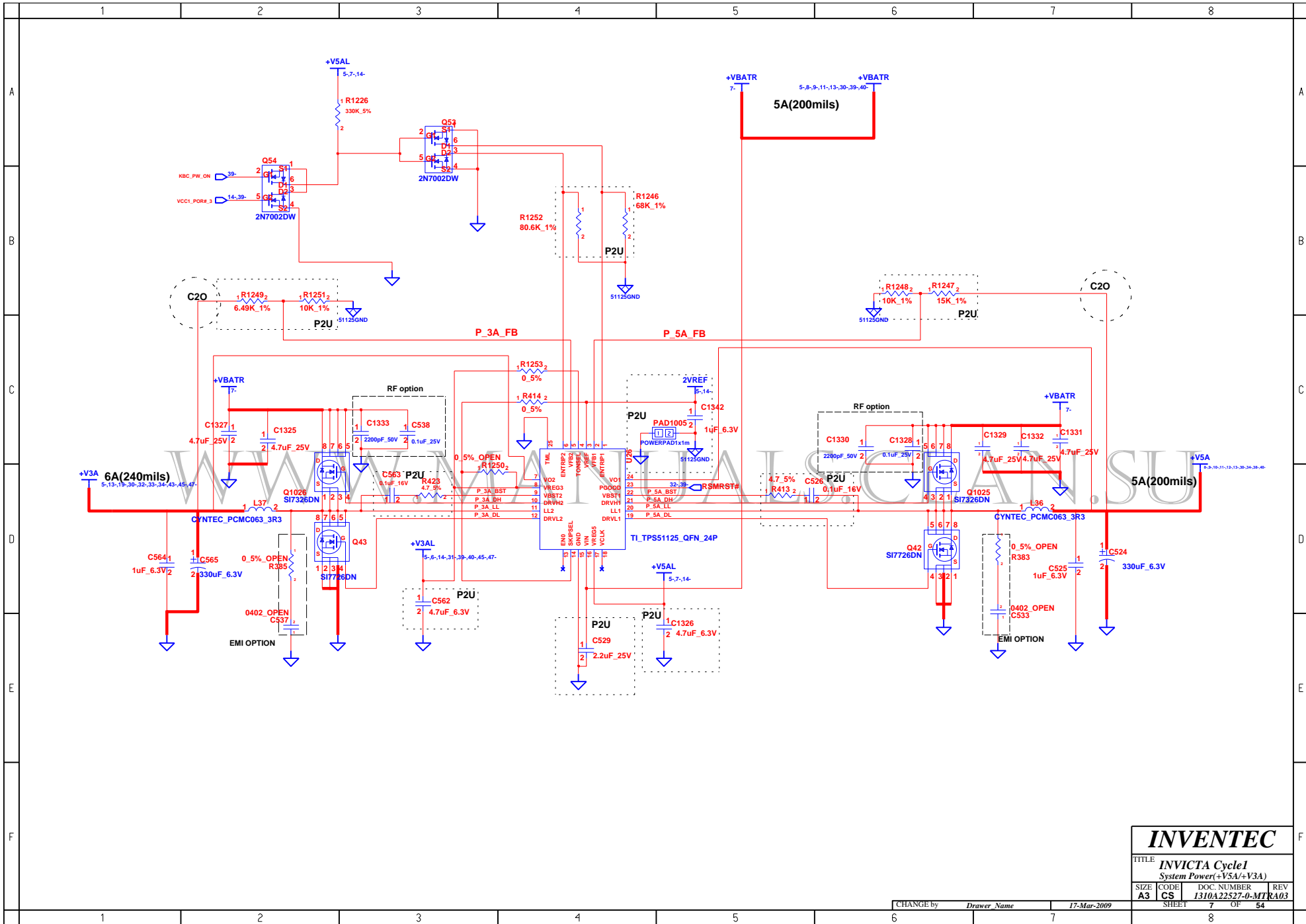


- Layout Rule**
- 1>Noisy driver(BST, SW node, DH & DL) keep trace short and wide
 - 2>Don't route sensitive signal(Current&Voltage Sense, FB, REF, AGND...) close noisy driver area
 - 3>Layout Kelvin sense as a differential pair to device
 - 4>Layout Vout sense connect to output terminal(c2o)
 - 5>Place Cap. and filter close to IC(p2u)

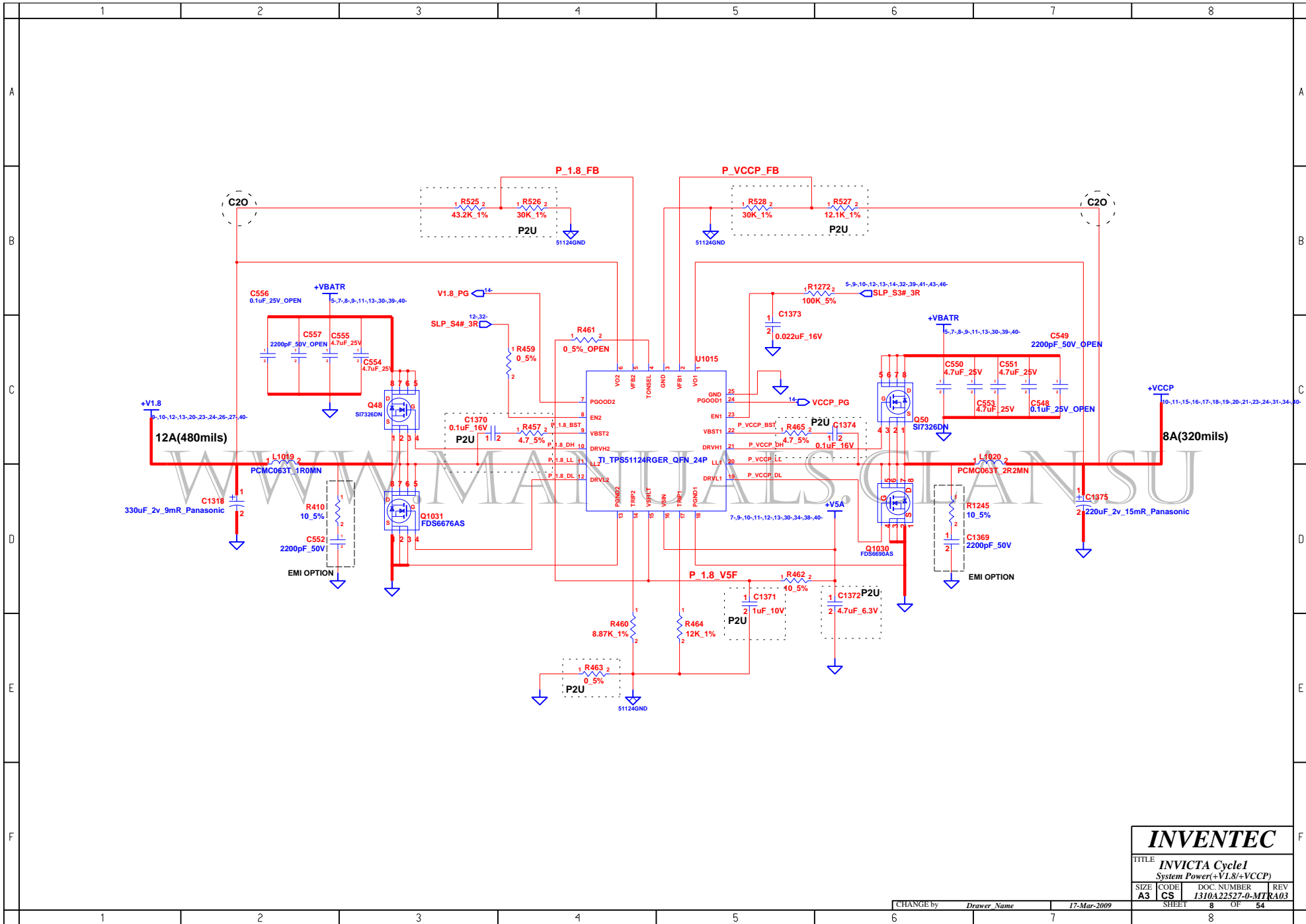
| | | | |
|---|------------|-------------------------------|------------|
| INVENTEC | | | |
| TITLE INVICTA Cycle1 DC & Battery Charger | | | |
| SIZE A3 | CODE CS | DOC NUMBER I310A22527-0-MT | REV A03 |
| CHANGE by Drawer Name | | 17-Mar-2009 | |
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| | | | |
|------------------------------------|----------------|------------------------------------|----------------|
| INVENTEC | | | |
| TITLE INVICTA Cycle1 | | | |
| Selector & Battery CONN & Extend/B | | | |
| SIZE A3 | CODE CS | DOC NUMBER 1310A22527-0-MTR | REV A03 |
| CHANGE by <i>Drawer Name</i> | | 17-Mar-2009 | |
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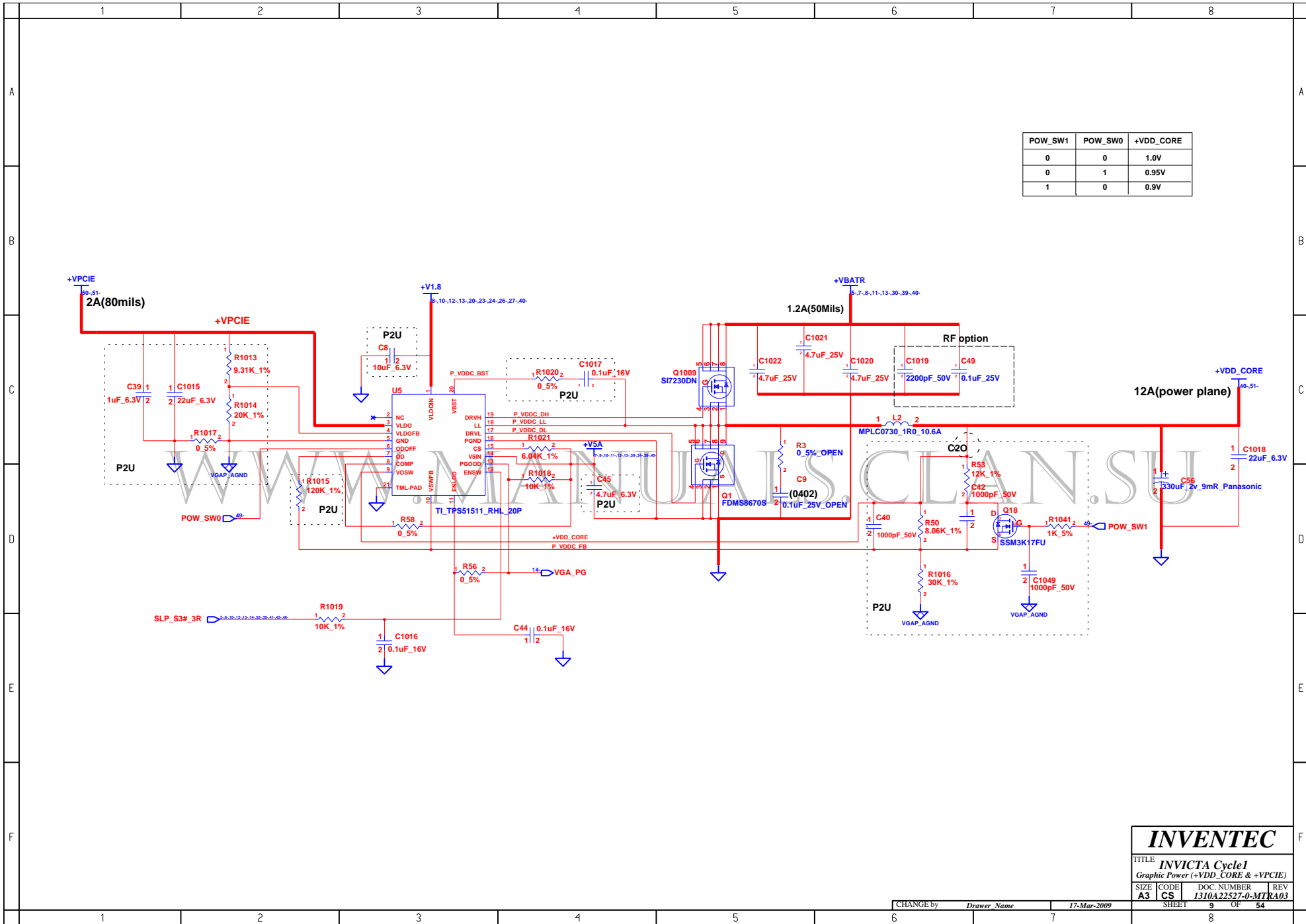
| | | | |
|-------------------------|------|------------------|------|
| INVENTEC | | | |
| TITLE: INVICTA Cycle 1 | | | |
| System Power(+V5A/+V3A) | | | |
| SIZE | CODE | DOC. NUMBER | REV |
| A3 | CS | 1310A22527-0-MIT | R403 |



INVENTEC

TITLE **INVICTA Cycle 1**
System Power(+V1.8/+VCCP)

| | | | |
|-------------------|-------------------|---------------------------------------|-------------------|
| SIZE A3 | CODE CS | DOC NUMBER I310A22527-0-MTR | REV A03 |
|-------------------|-------------------|---------------------------------------|-------------------|



| POW_SW1 | POW_SW0 | +VDD_CORE |
|---------|---------|-----------|
| 0 | 0 | 1.0V |
| 0 | 1 | 0.95V |
| 1 | 0 | 0.9V |

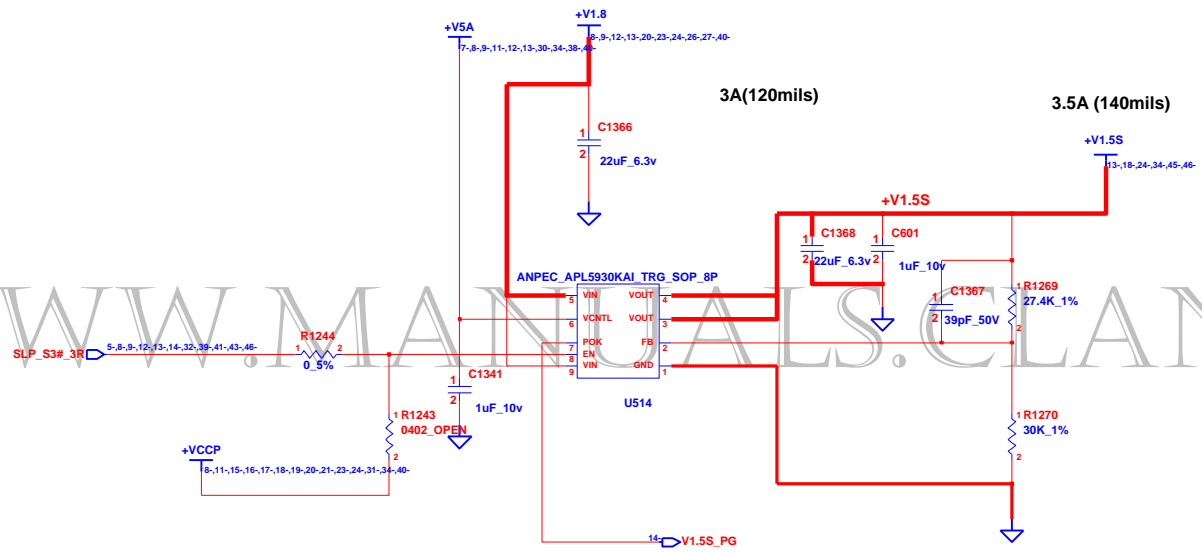
INVENTEC

TITLE: **INVICTA Cycle1**
 Graphic Power (+VDD_CORE & +VPCIE)

| | | | |
|------|------|------------------|-----|
| SIZE | CODE | DOC NUMBER | REV |
| A3 | CS | I310A22527-0-MTR | A03 |

CHANGE by: *Drawer Name* 17-Mar-2009 SHEET 9 OF 54

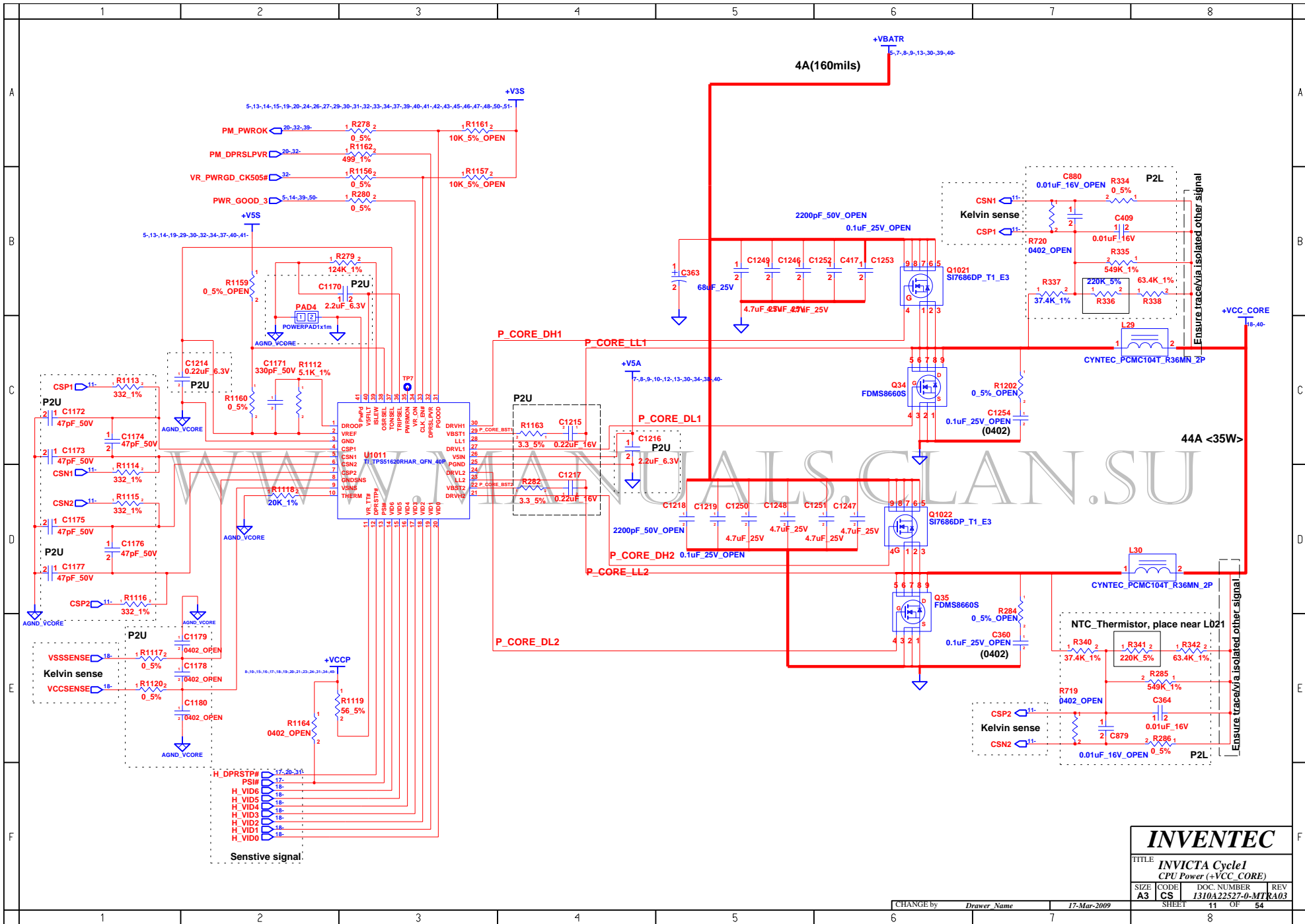
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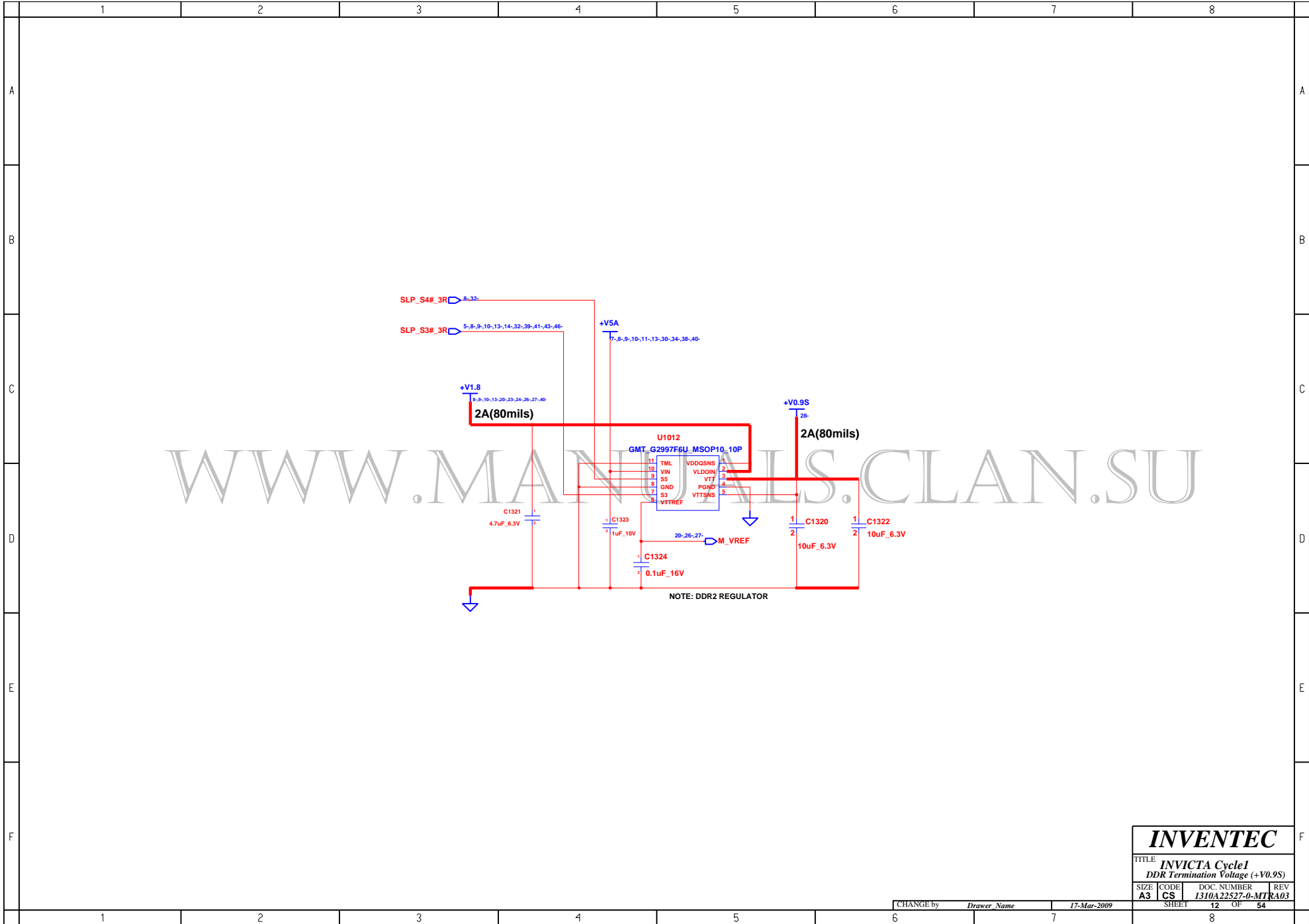
INVENTEC

TITLE **INVICTA Cycle1**
System Power (+V1.5S)

| | | | |
|----------------|----------------|-------------------------------------|----------------|
| SIZE A3 | CODE CS | DOC. NUMBER I310A22527-0-MTR | REV A03 |
|----------------|----------------|-------------------------------------|----------------|

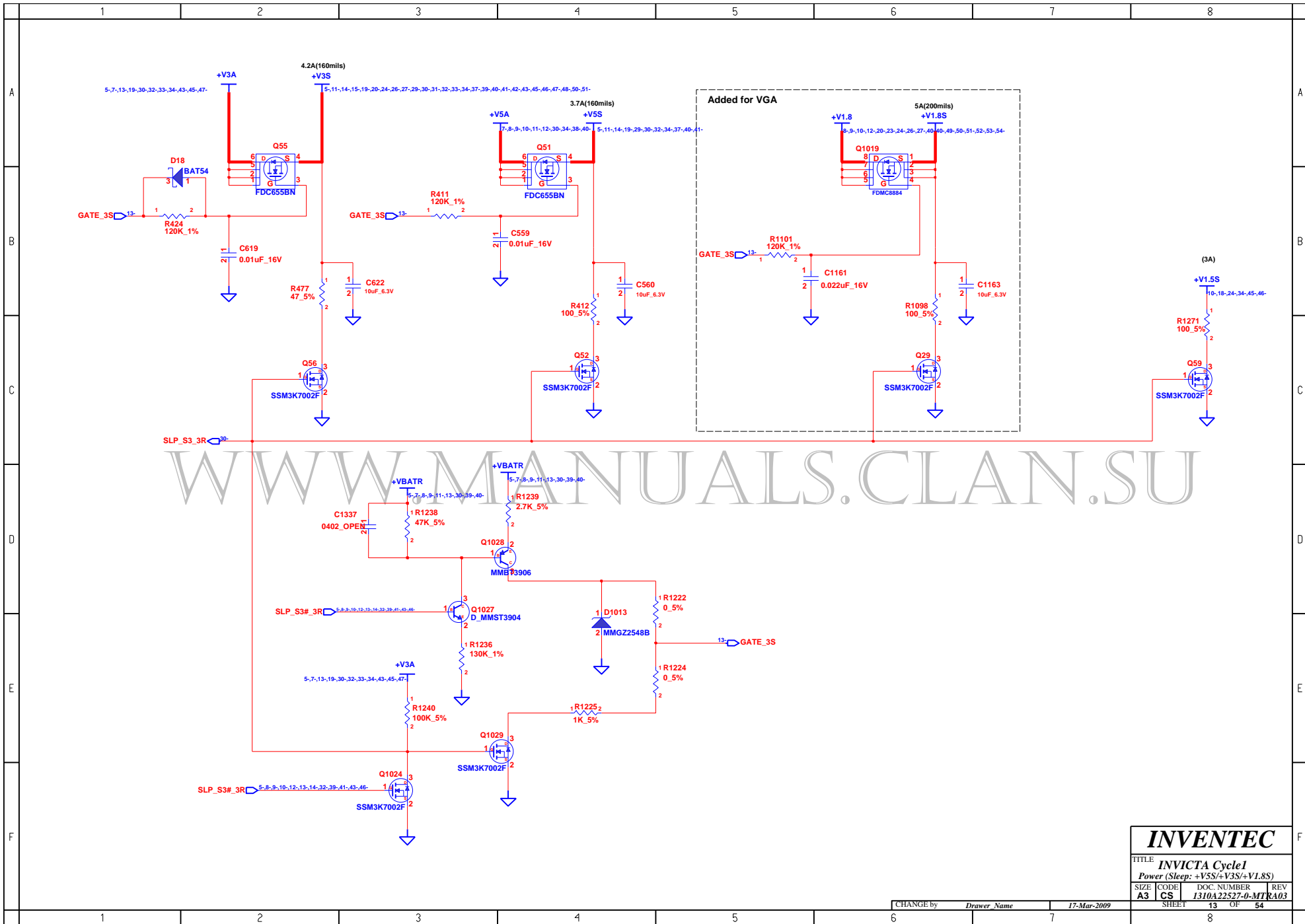


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|------------------------------|------|------------------|-------------|
| INVENTEC | | | |
| TITLE: INVICTA Cycle1 | | | |
| CPU Power (+VCC_CORE) | | | |
| SIZE | CODE | DOC. NUMBER | REV |
| A3 | CS | 1310A22527-0-MTR | A03 |
| CHANGE by | | Drawer Name | 17-Mar-2009 |
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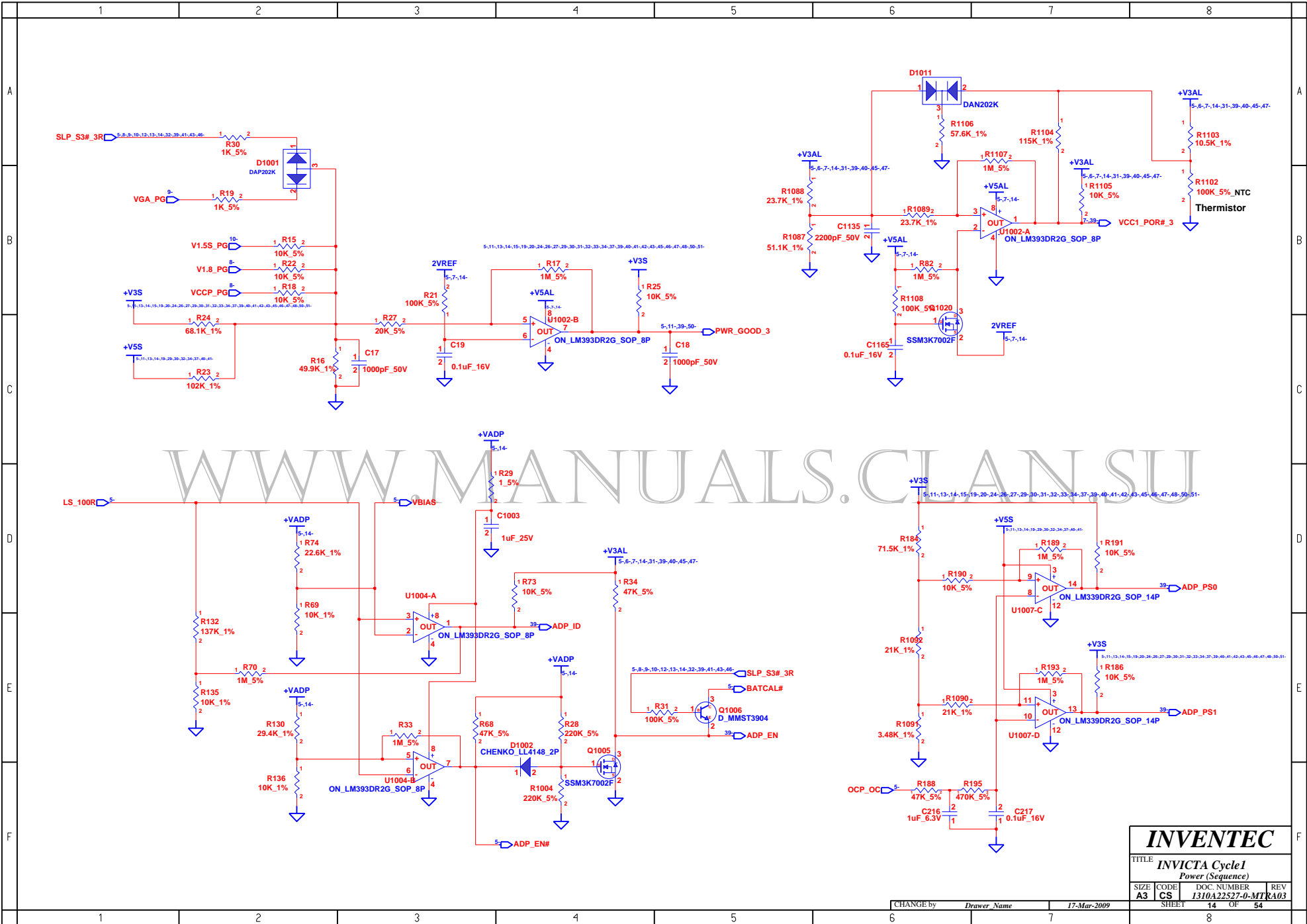
| | | | |
|----------------------------------|------|-----------------|------|
| INVENTEC | | | |
| TITLE INVICTA Cycle1 | | | |
| DDR Termination Voltage (+V0.9S) | | | |
| SIZE | CODE | DOC. NUMBER | REV |
| A3 | CS | 1310A22527-0-MT | RA03 |

CHANGE by *Drawer Name* 17-Mar-2009 SHEET 12 OF 54



INVENTEC

| | | | |
|---------------------------------|------|-----------------|-------------|
| TITLE | | | |
| INVICTA Cycle 1 | | | |
| Power (Sleep: +VSS/+V3S/+V1.8S) | | | |
| SIZE | CODE | DOC NUMBER | REV |
| A3 | CS | I310A22527-0-MT | A03 |
| CHANGE by | | Drawer Name | 17-Mar-2009 |
| SHEET | | 13 | OF 54 |



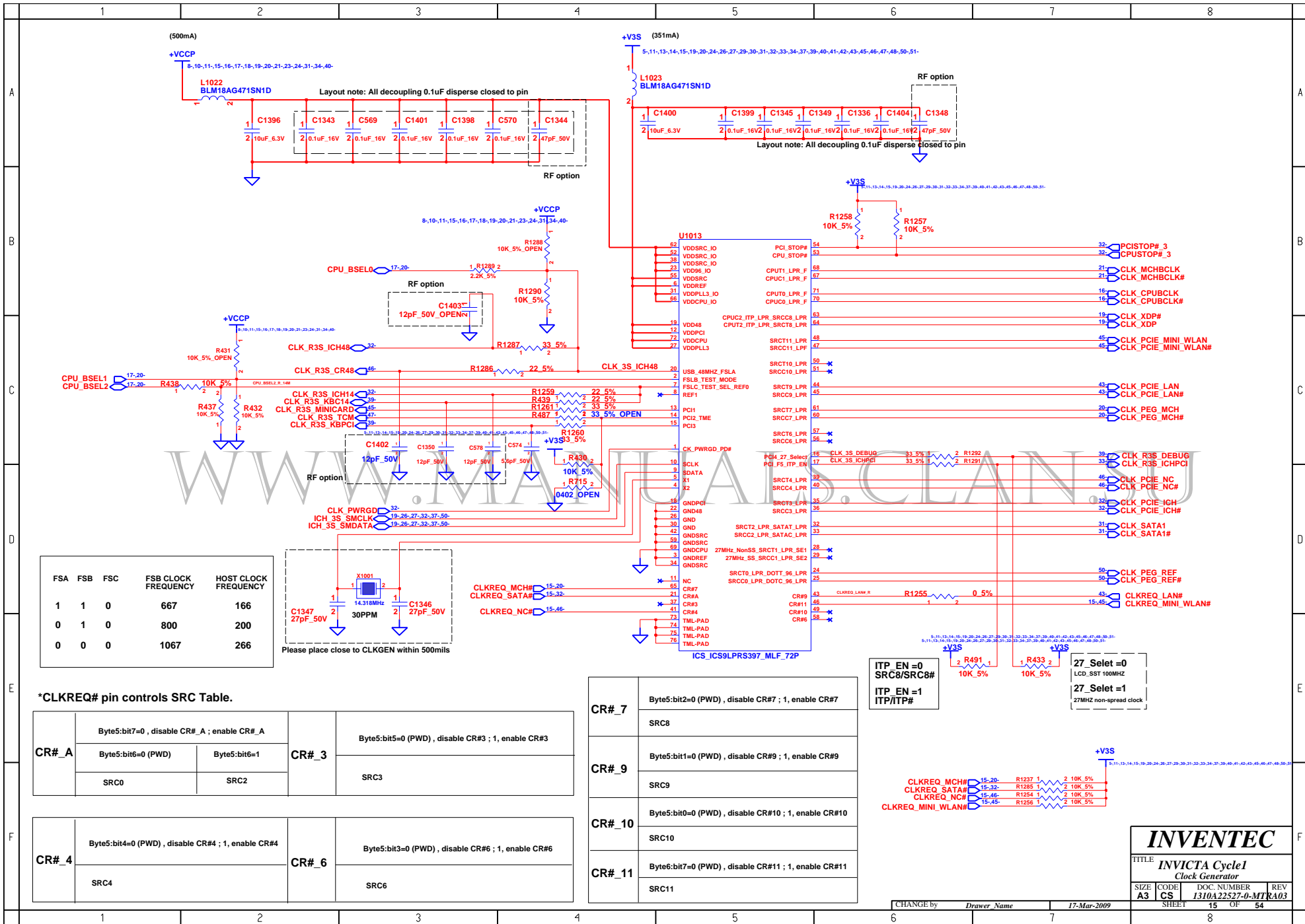
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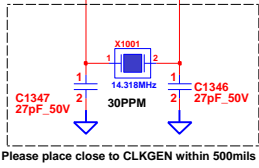
TITLE
**INVICTA Cycle1
Power (Sequence)**

| | | | |
|-------------------|-------------------|---------------------------------------|-------------------|
| SIZE A3 | CODE CS | DOC NUMBER 1310A22527-0-MTR | REV A03 |
|-------------------|-------------------|---------------------------------------|-------------------|

| | | |
|--------------------------|----------|-------------|
| CHANGE by Drawer Name | | 17-Mar-2009 |
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| FSA | FSB | FSC | FSB CLOCK FREQUENCY | HOST CLOCK FREQUENCY |
|-----|-----|-----|---------------------|----------------------|
| 1 | 1 | 0 | 667 | 166 |
| 0 | 1 | 0 | 800 | 200 |
| 0 | 0 | 0 | 1067 | 266 |



*CLKREQ# pin controls SRC Table.

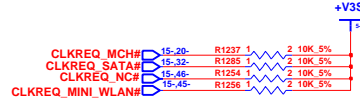
| CR#_A | Byte5:bit7=0 (PWD), disable CR#_A; enable CR#_A | Byte5:bit6=0 (PWD) | Byte5:bit6=1 | CR#_3 | Byte5:bit5=0 (PWD), disable CR#3; 1, enable CR#3 |
|-------|---|--------------------|--------------|-------|--|
| | | SRC0 | | | SRC3 |

| CR#_4 | Byte5:bit4=0 (PWD), disable CR#4; 1, enable CR#4 | CR#_6 | Byte5:bit3=0 (PWD), disable CR#6; 1, enable CR#6 |
|-------|--|-------|--|
| | | | SRC6 |

| | |
|--------|--|
| CR#_7 | Byte5:bit2=0 (PWD), disable CR#7; 1, enable CR#7 |
| | SRC8 |
| CR#_9 | Byte5:bit1=0 (PWD), disable CR#9; 1, enable CR#9 |
| | SRC9 |
| CR#_10 | Byte5:bit0=0 (PWD), disable CR#10; 1, enable CR#10 |
| | SRC10 |
| CR#_11 | Byte6:bit7=0 (PWD), disable CR#11; 1, enable CR#11 |
| | SRC11 |

ITP_EN=0
SRC8/SRC8#
ITP_EN=1
ITP/ITP#

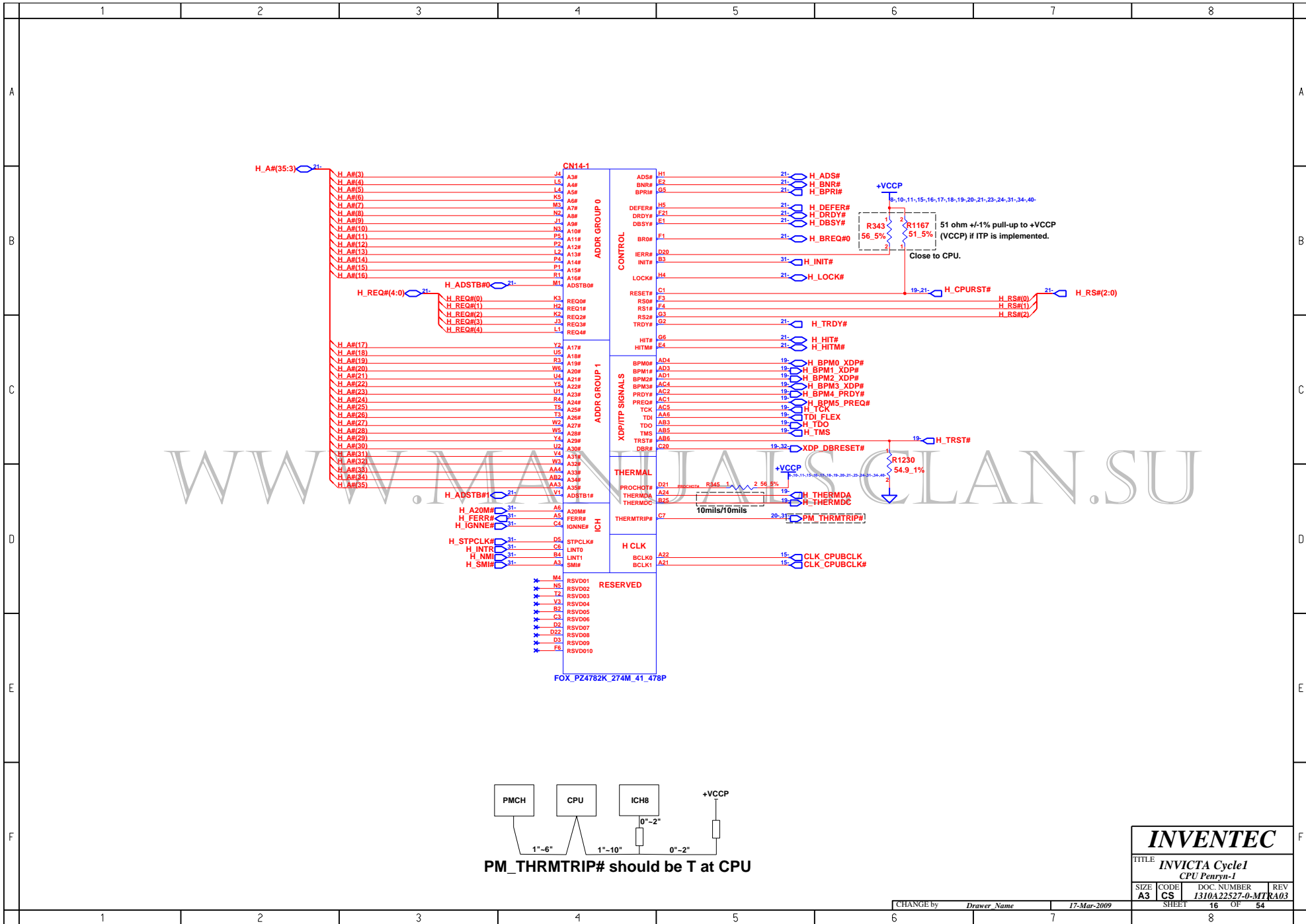
27_Select=0
LCD_SST 100MHz
27_Select=1
27MHz non-spread clock



INVENTEC

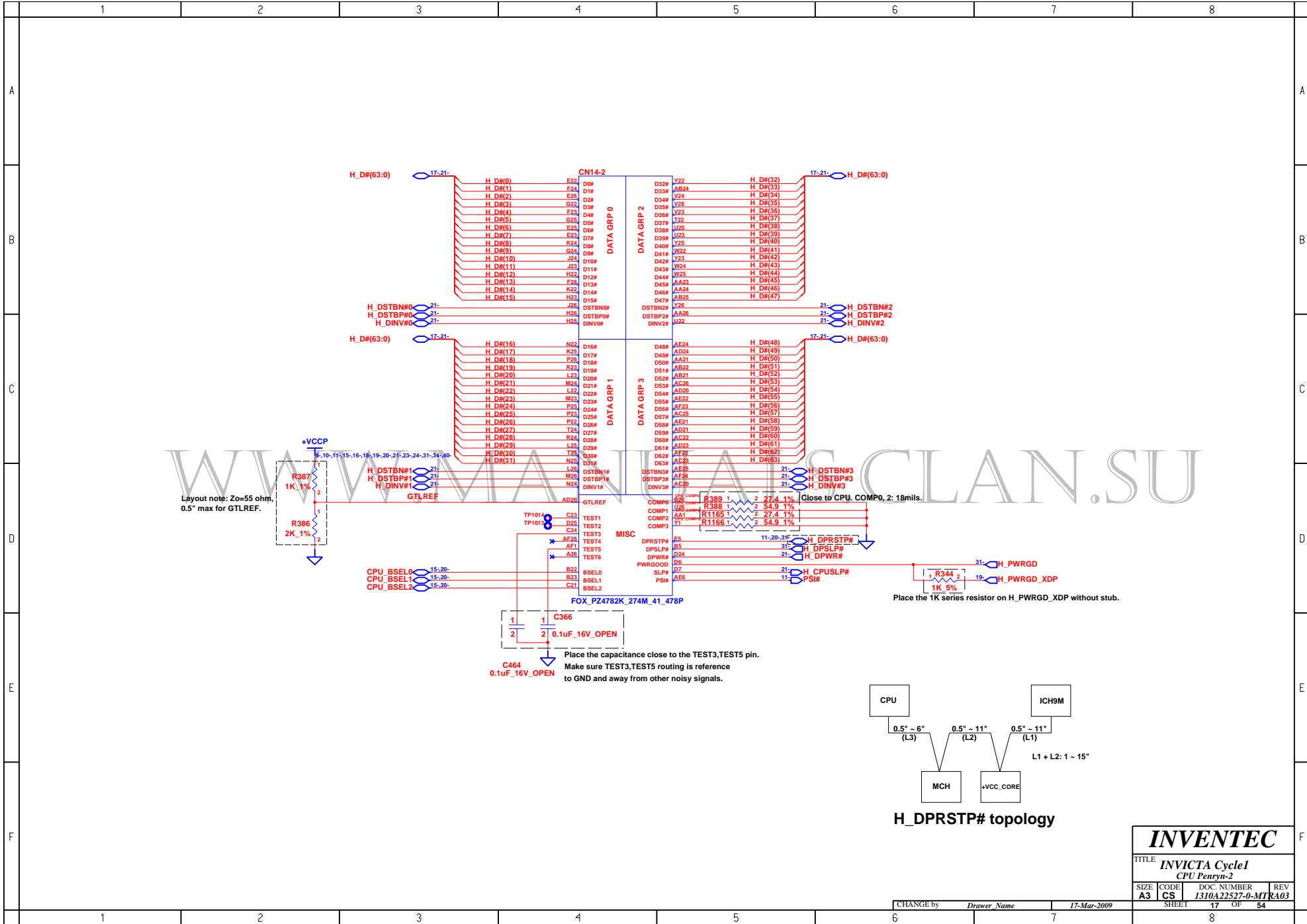
TITLE: INVICTA Cycle1
Clock Generator

| | | | |
|------|------|------------------|-----|
| SIZE | CODE | DOC. NUMBER | REV |
| A3 | CS | I310A22527-0-MTR | A03 |



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|--|----------------|------------------------------------|----------------|
| INVENTEC | | | |
| TITLE <i>INVICTA Cycle1 CPU Penryn-1</i> | | | |
| SIZE A3 | CODE CS | DOC NUMBER <i>1310A22527-0-MTR</i> | REV A03 |
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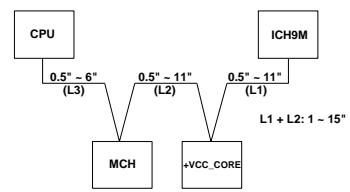


Layout note: Zo=55 ohm,
0.5" max for GTLREF.

Close to CPU_COMP0, 2: 18milis.

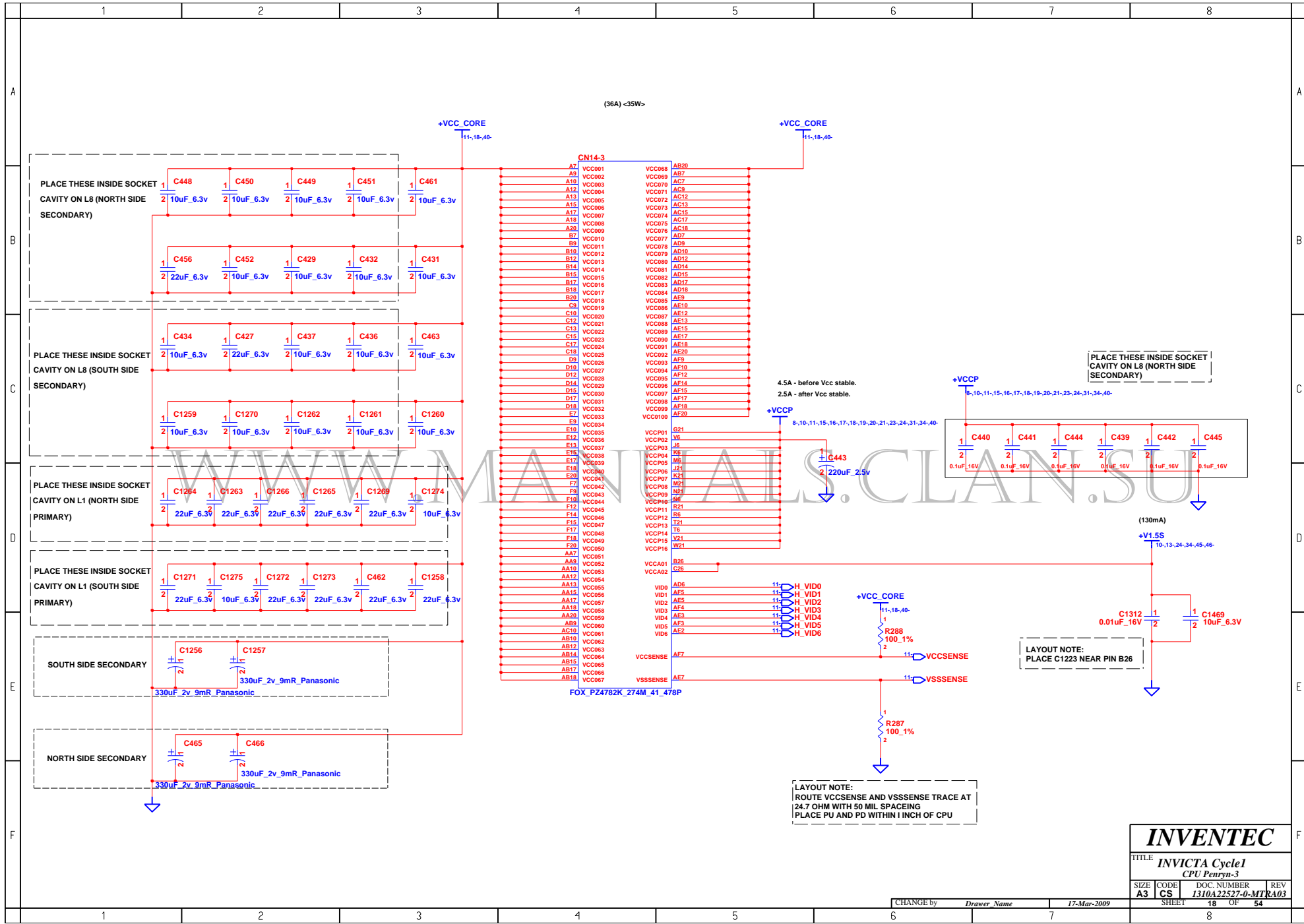
Place the 1K series resistor on H_PWRGD_XDP without stub.

Place the capacitance close to the TEST3,TEST5 pin.
Make sure TEST3,TEST5 routing is reference
to GND and away from other noisy signals.



H_DPRSTP# topology

| | | | |
|-----------------------------|------|------------------|-------------|
| INVENTEC | | | |
| TITLE INVICTA Cycle1 | | | |
| CPU Penryn-2 | | | |
| SIZE | CODE | DOC NUMBER | REV |
| A3 | CS | 1310A22527-0-MTR | A03 |
| CHANGE by | | Drawer Name | 17-Mar-2009 |
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PLACE THESE INSIDE SOCKET
CAVITY ON L8 (NORTH SIDE
SECONDARY)

PLACE THESE INSIDE SOCKET
CAVITY ON L8 (SOUTH SIDE
SECONDARY)

PLACE THESE INSIDE SOCKET
CAVITY ON L1 (NORTH SIDE
PRIMARY)

PLACE THESE INSIDE SOCKET
CAVITY ON L1 (SOUTH SIDE
PRIMARY)

SOUTH SIDE SECONDARY

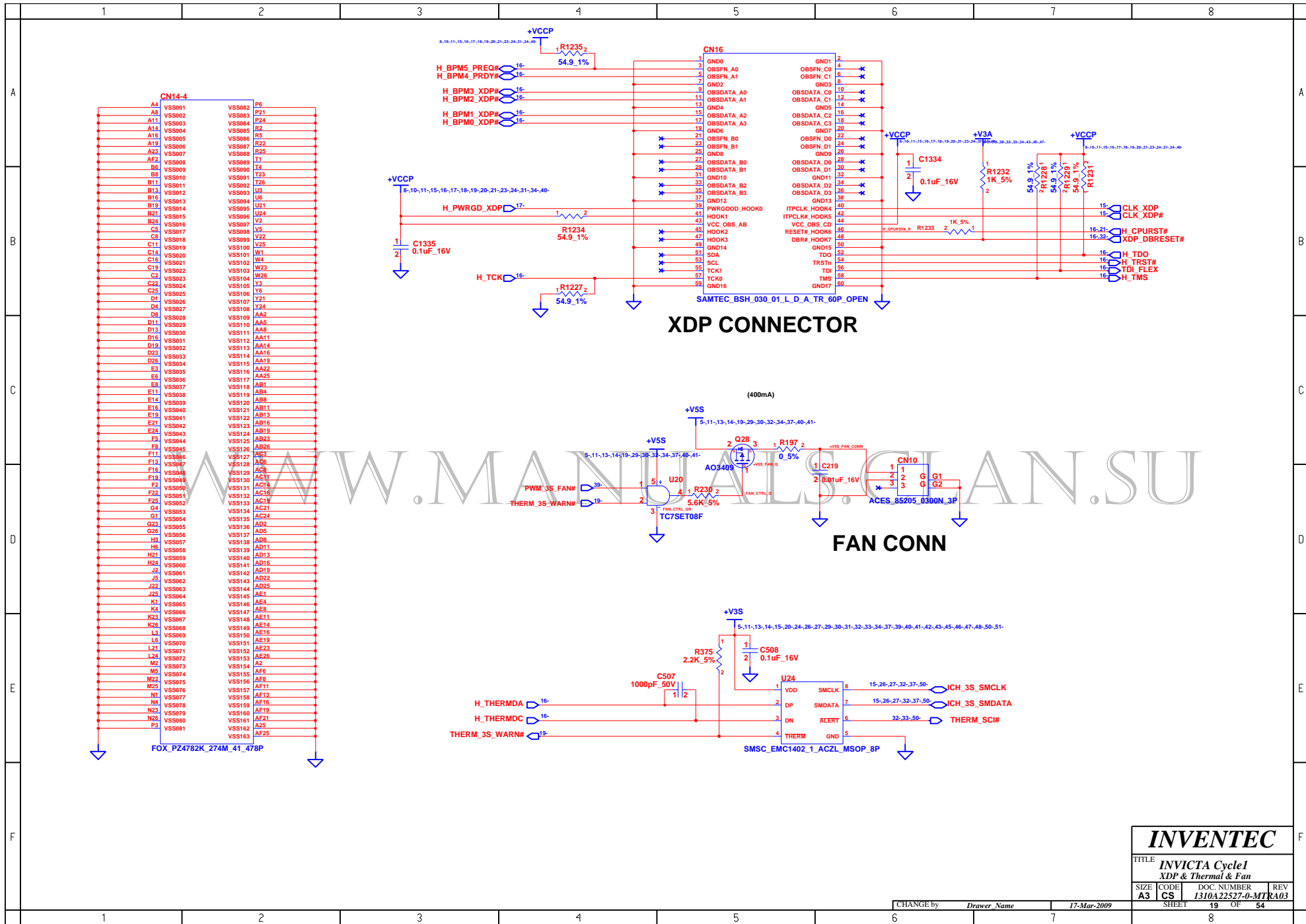
NORTH SIDE SECONDARY

PLACE THESE INSIDE SOCKET
CAVITY ON L8 (NORTH SIDE
SECONDARY)

LAYOUT NOTE:
PLACE C1223 NEAR PIN B26

LAYOUT NOTE:
ROUTE VCCSENSE AND VSSSENSE TRACE AT
24.7 OHM WITH 50 MIL SPACING
PLACE PU AND PD WITHIN 1 INCH OF CPU

| | | | |
|--|------------|---------------------------------|----------------|
| INVENTEC | | | |
| TITLE <i>INVICTA Cycle1</i> CPU Penryn-3 | | | |
| SIZE A3 | CODE CS | DOC. NUMBER I310A22527-0-MTR | REV A03 |
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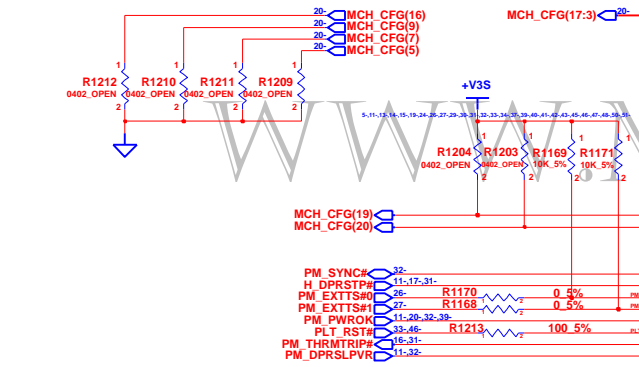


| | | | |
|---|----------|-------------------------------|-----------|
| INVENTEC | | | |
| TITLE: INVICTA Cycle1 XDP & Thermal & Fan | | | |
| SIZE: A3 | CODE: CS | DOC. NUMBER: I310A22527-0-MTR | REV: RA03 |
| CHANGE by: Drawer Name | | 17-Mar-2009 | |
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NOTE : USE 4K-OHM RESISTOR WHEN INSTALLING PULL-UP/PULL-DOWN RESISTOR ON ANY MCH-CFG CONNECTION/PINS.

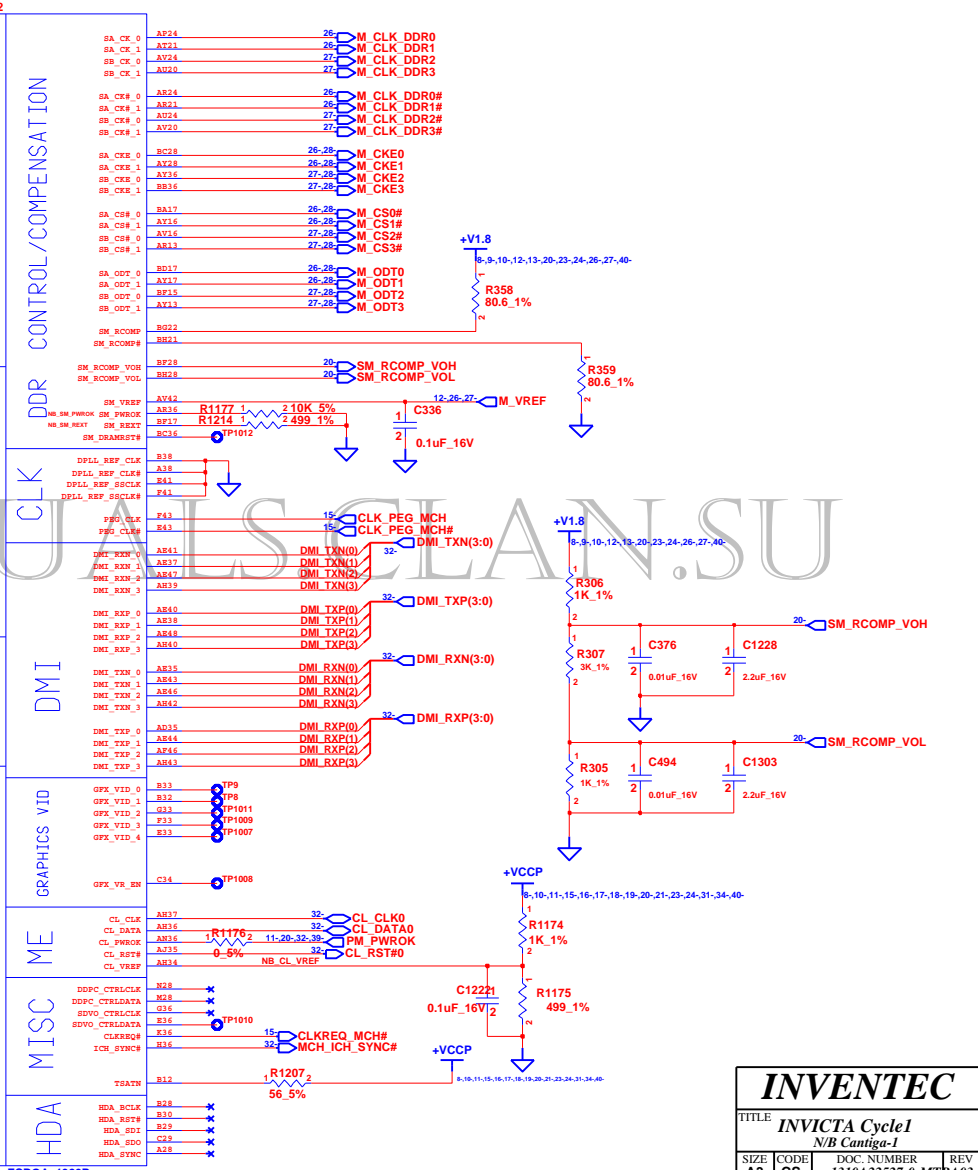
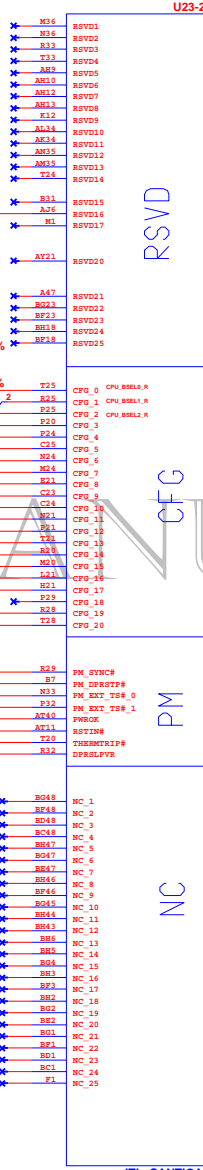
| | | | | | |
|----------------------------|--|---|--|----------------------------------|---|
| MCH_CFG(5) | LOW=DMiX2 HIGH=DMiX4 | MCH_CFG(7) (CPU Strap) | LOW=RSVD HIGH=Mobile CPU | MCH_CFG(9) PCIE Graphics Lane | LOW=Reverse Lane HIGH=Normal operation |
| MCH_CFG(13:12) XOR/ALLZ | 00=PARTIAL CLOCK GATING DISABLE 01=XOR MODE ENABLE 10=ALL-Z MODE ENABLE 11=NORMAL OPERATION | MCH_CFG(16) Dynamic ODT (FSB Dynamic ODT) | LOW=Dynamic ODT Disable HIGH=Dynamic ODT Enable | | |

NOTE: CFG[2:0] STRP : 011b : 667 MT/S
010 : 800 MT/S
000 : 1067 MT/S



| | |
|------------------------------------|-----------------------------------|
| MCH_CFG(19) (DMI LANE REVERSAL) | LOW=NORMAL HIGH=LANES REVERSED |
|------------------------------------|-----------------------------------|

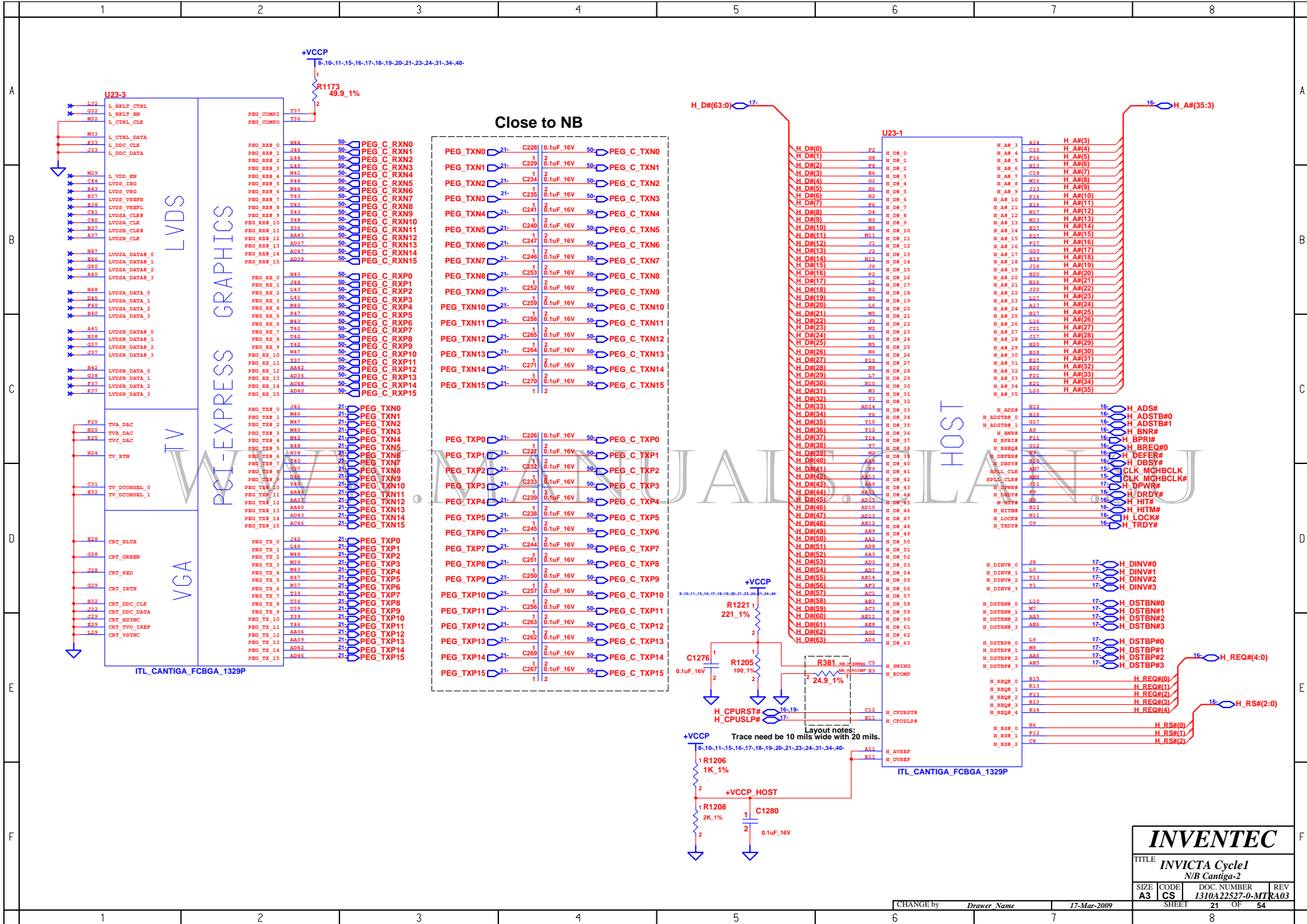
| | |
|--|---|
| MCH_CFG(20) DIGITAL DISPLAY PORT (SDVO(DP/HDMI) OR PCIE'S OPERATIONAL PORT(SDVO(DP/HDMI) CONCURRENT WITH PCIE | LOW=ONLY DIGITAL DISPLAY PORT (SDVO(DP/HDMI) OR PCIE'S OPERATIONAL PORT(SDVO(DP/HDMI) AND PCIE ARE OPERATING VIA THE PEG PORT |
|--|---|



INVENTEC

TITLE: INVICTA Cycle1
N/B Cantiga-1

| | | | |
|----------|---------|-----------------------------|---------|
| SIZE A3 | CODE CS | DOC NUMBER 1310A22527-0-MTR | REV A03 |
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Close to NB

| | | | | | |
|-----------|-----|------|-----------|-----|-------------|
| PEG_TXN0 | 21- | C228 | 0.1uF_16V | 50- | PEG_C_TXN0 |
| PEG_TXN1 | 21- | C229 | 0.1uF_16V | 50- | PEG_C_TXN1 |
| PEG_TXN2 | 21- | C230 | 0.1uF_16V | 50- | PEG_C_TXN2 |
| PEG_TXN3 | 21- | C235 | 0.1uF_16V | 50- | PEG_C_TXN3 |
| PEG_TXN4 | 21- | C241 | 0.1uF_16V | 50- | PEG_C_TXN4 |
| PEG_TXN5 | 21- | C240 | 0.1uF_16V | 50- | PEG_C_TXN5 |
| PEG_TXN6 | 21- | C247 | 0.1uF_16V | 50- | PEG_C_TXN6 |
| PEG_TXN7 | 21- | C246 | 0.1uF_16V | 50- | PEG_C_TXN7 |
| PEG_TXN8 | 21- | C253 | 0.1uF_16V | 50- | PEG_C_TXN8 |
| PEG_TXN9 | 21- | C252 | 0.1uF_16V | 50- | PEG_C_TXN9 |
| PEG_TXN10 | 21- | C259 | 0.1uF_16V | 50- | PEG_C_TXN10 |
| PEG_TXN11 | 21- | C258 | 0.1uF_16V | 50- | PEG_C_TXN11 |
| PEG_TXN12 | 21- | C265 | 0.1uF_16V | 50- | PEG_C_TXN12 |
| PEG_TXN13 | 21- | C264 | 0.1uF_16V | 50- | PEG_C_TXN13 |
| PEG_TXN14 | 21- | C271 | 0.1uF_16V | 50- | PEG_C_TXN14 |
| PEG_TXN15 | 21- | C270 | 0.1uF_16V | 50- | PEG_C_TXN15 |

| | | | | | |
|-----------|-----|------|-----------|-----|-------------|
| PEG_TXP0 | 21- | C226 | 0.1uF_16V | 50- | PEG_C_TXP0 |
| PEG_TXP1 | 21- | C227 | 0.1uF_16V | 50- | PEG_C_TXP1 |
| PEG_TXP2 | 21- | C232 | 0.1uF_16V | 50- | PEG_C_TXP2 |
| PEG_TXP3 | 21- | C233 | 0.1uF_16V | 50- | PEG_C_TXP3 |
| PEG_TXP4 | 21- | C239 | 0.1uF_16V | 50- | PEG_C_TXP4 |
| PEG_TXP5 | 21- | C238 | 0.1uF_16V | 50- | PEG_C_TXP5 |
| PEG_TXP6 | 21- | C245 | 0.1uF_16V | 50- | PEG_C_TXP6 |
| PEG_TXP7 | 21- | C244 | 0.1uF_16V | 50- | PEG_C_TXP7 |
| PEG_TXP8 | 21- | C251 | 0.1uF_16V | 50- | PEG_C_TXP8 |
| PEG_TXP9 | 21- | C250 | 0.1uF_16V | 50- | PEG_C_TXP9 |
| PEG_TXP10 | 21- | C257 | 0.1uF_16V | 50- | PEG_C_TXP10 |
| PEG_TXP11 | 21- | C256 | 0.1uF_16V | 50- | PEG_C_TXP11 |
| PEG_TXP12 | 21- | C263 | 0.1uF_16V | 50- | PEG_C_TXP12 |
| PEG_TXP13 | 21- | C262 | 0.1uF_16V | 50- | PEG_C_TXP13 |
| PEG_TXP14 | 21- | C269 | 0.1uF_16V | 50- | PEG_C_TXP14 |
| PEG_TXP15 | 21- | C267 | 0.1uF_16V | 50- | PEG_C_TXP15 |

U23-1

| | | |
|----------|------|--------|
| H_D#(0) | F2 | H_D#0 |
| H_D#(1) | F2 | H_D#1 |
| H_D#(2) | F2 | H_D#2 |
| H_D#(3) | F6 | H_D#3 |
| H_D#(4) | G2 | H_D#4 |
| H_D#(5) | F6 | H_D#5 |
| H_D#(6) | H2 | H_D#6 |
| H_D#(7) | F6 | H_D#7 |
| H_D#(8) | D4 | H_D#8 |
| H_D#(9) | F2 | H_D#9 |
| H_D#(10) | M2 | H_D#10 |
| H_D#(11) | M2 | H_D#11 |
| H_D#(12) | J2 | H_D#12 |
| H_D#(13) | J2 | H_D#13 |
| H_D#(14) | M2 | H_D#14 |
| H_D#(15) | J6 | H_D#15 |
| H_D#(16) | F2 | H_D#16 |
| H_D#(17) | F2 | H_D#17 |
| H_D#(18) | R2 | H_D#18 |
| H_D#(19) | N2 | H_D#19 |
| H_D#(20) | L6 | H_D#20 |
| H_D#(21) | M2 | H_D#21 |
| H_D#(22) | J2 | H_D#22 |
| H_D#(23) | N2 | H_D#23 |
| H_D#(24) | N2 | H_D#24 |
| H_D#(25) | M2 | H_D#25 |
| H_D#(26) | N6 | H_D#26 |
| H_D#(27) | F2 | H_D#27 |
| H_D#(28) | F2 | H_D#28 |
| H_D#(29) | F2 | H_D#29 |
| H_D#(30) | M2 | H_D#30 |
| H_D#(31) | M2 | H_D#31 |
| H_D#(32) | F2 | H_D#32 |
| H_D#(33) | AD14 | H_D#33 |
| H_D#(34) | F6 | H_D#34 |
| H_D#(35) | F2 | H_D#35 |
| H_D#(36) | F2 | H_D#36 |
| H_D#(37) | F14 | H_D#37 |
| H_D#(38) | F2 | H_D#38 |
| H_D#(39) | F2 | H_D#39 |
| H_D#(40) | F6 | H_D#40 |
| H_D#(41) | F2 | H_D#41 |
| H_D#(42) | AD12 | H_D#42 |
| H_D#(43) | M2 | H_D#43 |
| H_D#(44) | AD13 | H_D#44 |
| H_D#(45) | AD12 | H_D#45 |
| H_D#(46) | AD10 | H_D#46 |
| H_D#(47) | AD14 | H_D#47 |
| H_D#(48) | AD12 | H_D#48 |
| H_D#(49) | AD2 | H_D#49 |
| H_D#(50) | AD2 | H_D#50 |
| H_D#(51) | AD2 | H_D#51 |
| H_D#(52) | AD1 | H_D#52 |
| H_D#(53) | AD1 | H_D#53 |
| H_D#(54) | AD2 | H_D#54 |
| H_D#(55) | AD14 | H_D#55 |
| H_D#(56) | AF1 | H_D#56 |
| H_D#(57) | AC1 | H_D#57 |
| H_D#(58) | AD1 | H_D#58 |
| H_D#(59) | AC1 | H_D#59 |
| H_D#(60) | AD11 | H_D#60 |
| H_D#(61) | AD2 | H_D#61 |
| H_D#(62) | AD2 | H_D#62 |
| H_D#(63) | AD2 | H_D#63 |

| | | |
|---------|-----|-----------|
| H_AD#3 | A14 | H_AD#(3) |
| H_AD#4 | C15 | H_AD#(4) |
| H_AD#5 | F16 | H_AD#(5) |
| H_AD#6 | H13 | H_AD#(6) |
| H_AD#7 | C18 | H_AD#(7) |
| H_AD#8 | M16 | H_AD#(8) |
| H_AD#9 | F13 | H_AD#(9) |
| H_AD#10 | F16 | H_AD#(10) |
| H_AD#11 | R16 | H_AD#(11) |
| H_AD#12 | M17 | H_AD#(12) |
| H_AD#13 | M13 | H_AD#(13) |
| H_AD#14 | F17 | H_AD#(14) |
| H_AD#15 | F17 | H_AD#(15) |
| H_AD#16 | F17 | H_AD#(16) |
| H_AD#17 | G20 | H_AD#(17) |
| H_AD#18 | F19 | H_AD#(18) |
| H_AD#19 | J16 | H_AD#(19) |
| H_AD#20 | F18 | H_AD#(20) |
| H_AD#21 | H16 | H_AD#(21) |
| H_AD#22 | J20 | H_AD#(22) |
| H_AD#23 | L17 | H_AD#(23) |
| H_AD#24 | B17 | H_AD#(24) |
| H_AD#25 | A17 | H_AD#(25) |
| H_AD#26 | L16 | H_AD#(26) |
| H_AD#27 | G21 | H_AD#(27) |
| H_AD#28 | M20 | H_AD#(28) |
| H_AD#29 | B18 | H_AD#(29) |
| H_AD#30 | K17 | H_AD#(30) |
| H_AD#31 | F20 | H_AD#(31) |
| H_AD#32 | F21 | H_AD#(32) |
| H_AD#33 | K21 | H_AD#(33) |
| H_AD#34 | L20 | H_AD#(34) |
| H_AD#35 | L20 | H_AD#(35) |

| | | |
|---------|-----|---------|
| H_AD#0 | B12 | H_AD#0 |
| H_AD#1 | B16 | H_AD#1 |
| H_AD#2 | G17 | H_AD#2 |
| H_AD#3 | A9 | H_AD#3 |
| H_AD#4 | F11 | H_AD#4 |
| H_AD#5 | G12 | H_AD#5 |
| H_AD#6 | B11 | H_AD#6 |
| H_AD#7 | A7 | H_AD#7 |
| H_AD#8 | A6 | H_AD#8 |
| H_AD#9 | G11 | H_AD#9 |
| H_AD#10 | A7 | H_AD#10 |
| H_AD#11 | A6 | H_AD#11 |
| H_AD#12 | G11 | H_AD#12 |
| H_AD#13 | F9 | H_AD#13 |
| H_AD#14 | B9 | H_AD#14 |
| H_AD#15 | B12 | H_AD#15 |
| H_AD#16 | B11 | H_AD#16 |
| H_AD#17 | C9 | H_AD#17 |
| H_AD#18 | C9 | H_AD#18 |

| | | |
|---------|-----|---------|
| H_DIN#0 | J8 | H_DIN#0 |
| H_DIN#1 | L9 | H_DIN#1 |
| H_DIN#2 | Y11 | H_DIN#2 |
| H_DIN#3 | Y1 | H_DIN#3 |

| | | |
|----------|-----|----------|
| H_DSTB#0 | L18 | H_DSTB#0 |
| H_DSTB#1 | M7 | H_DSTB#1 |
| H_DSTB#2 | AA5 | H_DSTB#2 |
| H_DSTB#3 | AE6 | H_DSTB#3 |

| | | |
|-----------|-----|-----------|
| H_REQ#(0) | B15 | H_REQ#(0) |
| H_REQ#(1) | F13 | H_REQ#(1) |
| H_REQ#(2) | B13 | H_REQ#(2) |
| H_REQ#(3) | B14 | H_REQ#(3) |
| H_REQ#(4) | B14 | H_REQ#(4) |

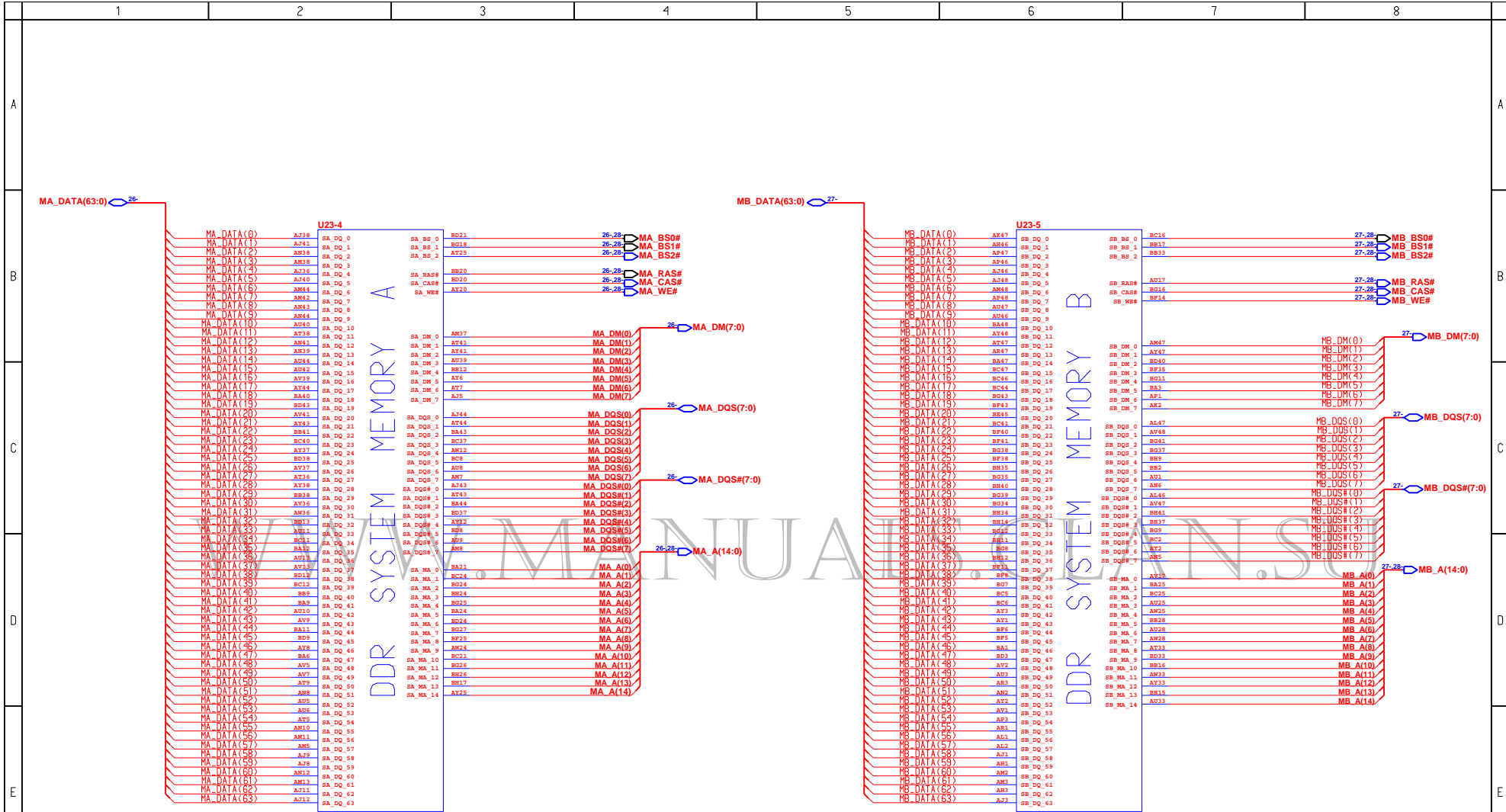
| | | |
|----------|-----|----------|
| H_RS#(0) | B6 | H_RS#(0) |
| H_RS#(1) | F12 | H_RS#(1) |
| H_RS#(2) | C8 | H_RS#(2) |

INVENTEC

TITLE
INVICTA Cycle1
N/B Cantiga-2

| | | | |
|------|------|------------------|-----|
| SIZE | CODE | DOC. NUMBER | REV |
| A3 | CS | 1310A22527-0-MTR | A03 |

CHANGE by *Drawer Name* 17-Mar-2009 SHEET 21 OF 54

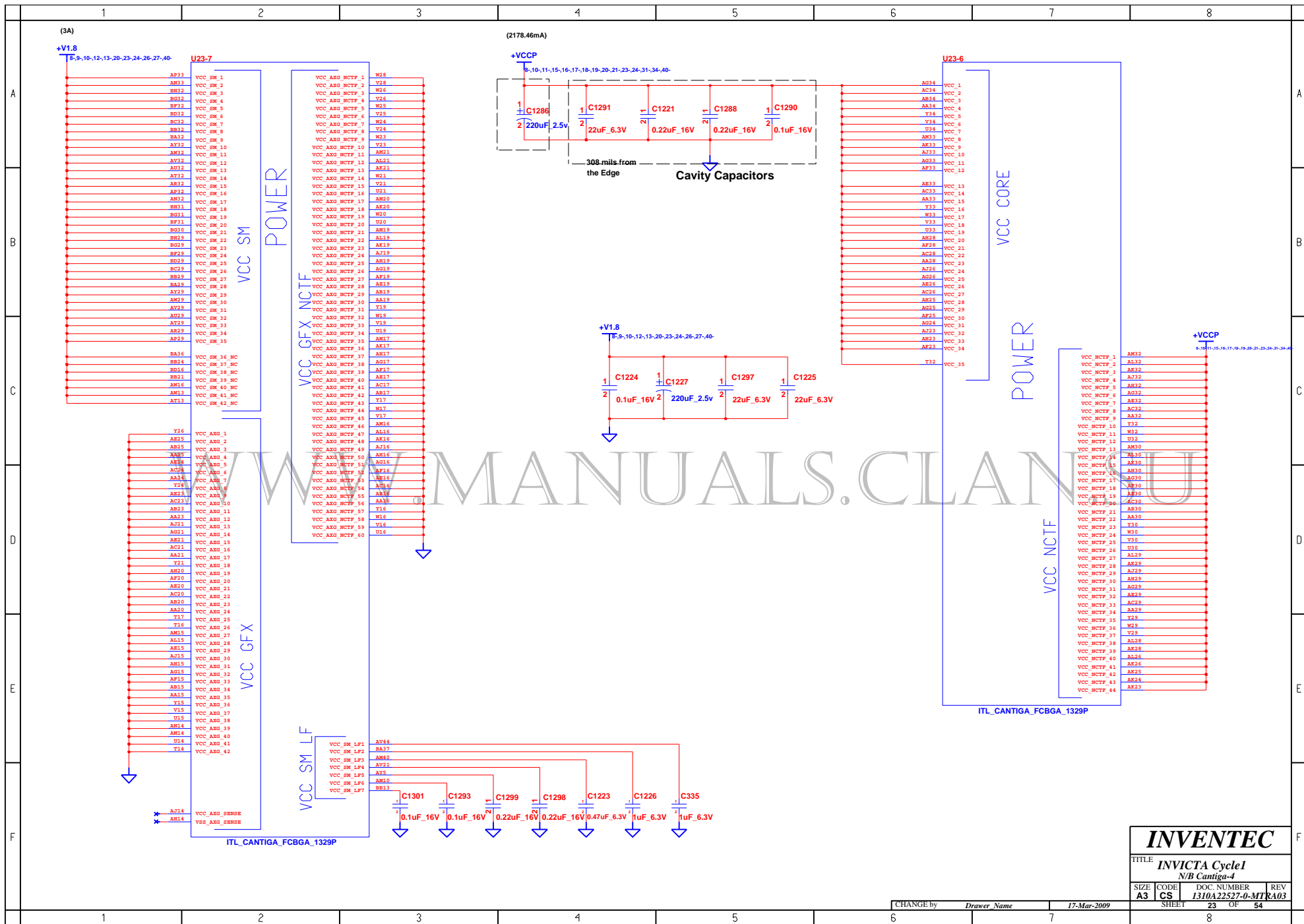


INVENTEC

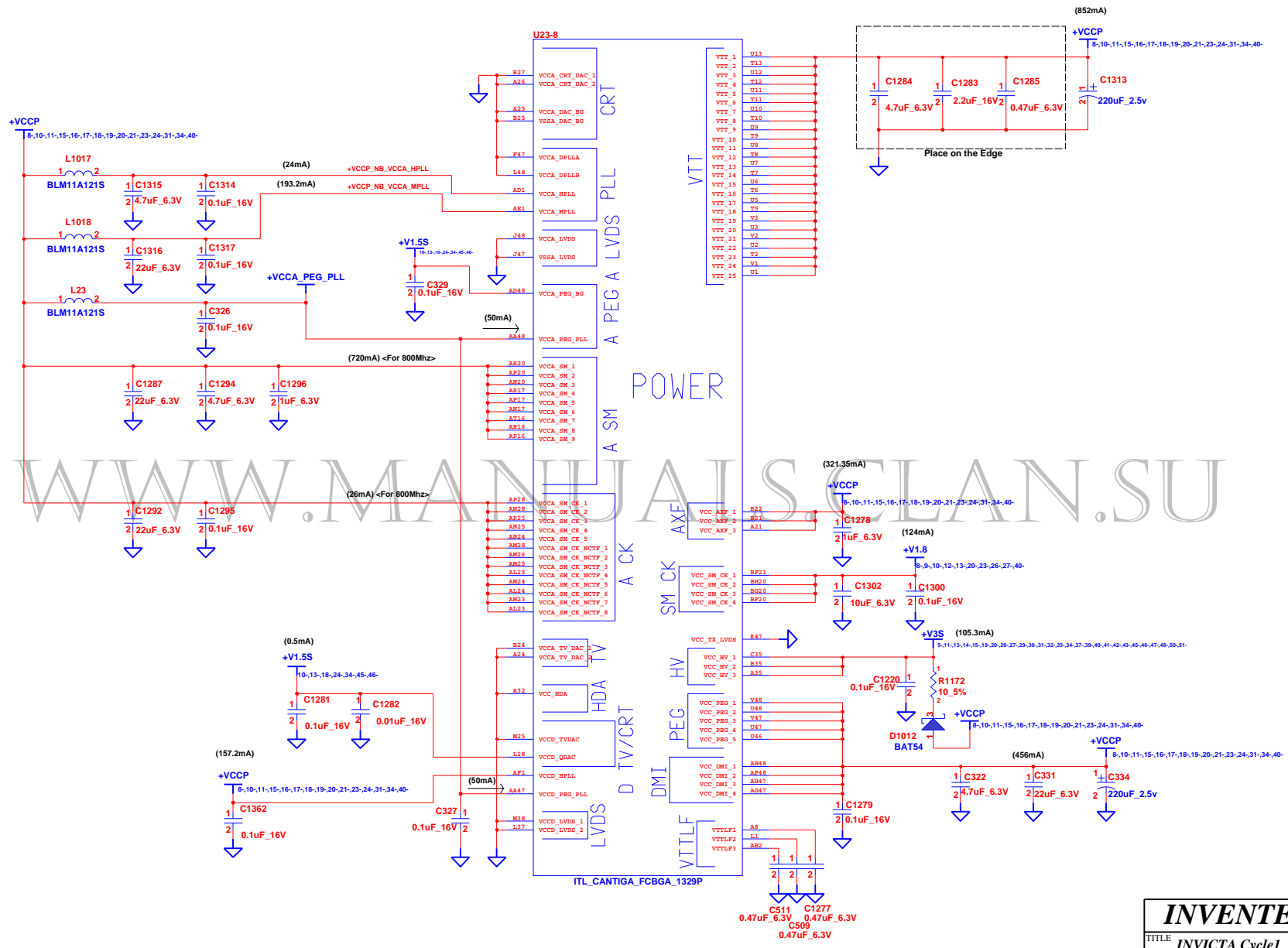
TITLE: **INVICTA Cycle1**
N/B Cantiga-3

| | | | |
|------|------|------------------|-----|
| SIZE | CODE | DOC. NUMBER | REV |
| A3 | CS | 1310A22527-0-MTR | A03 |

CHANGE by: *Drawer Name* 17-Mar-2009 SHEET 22 OF 54

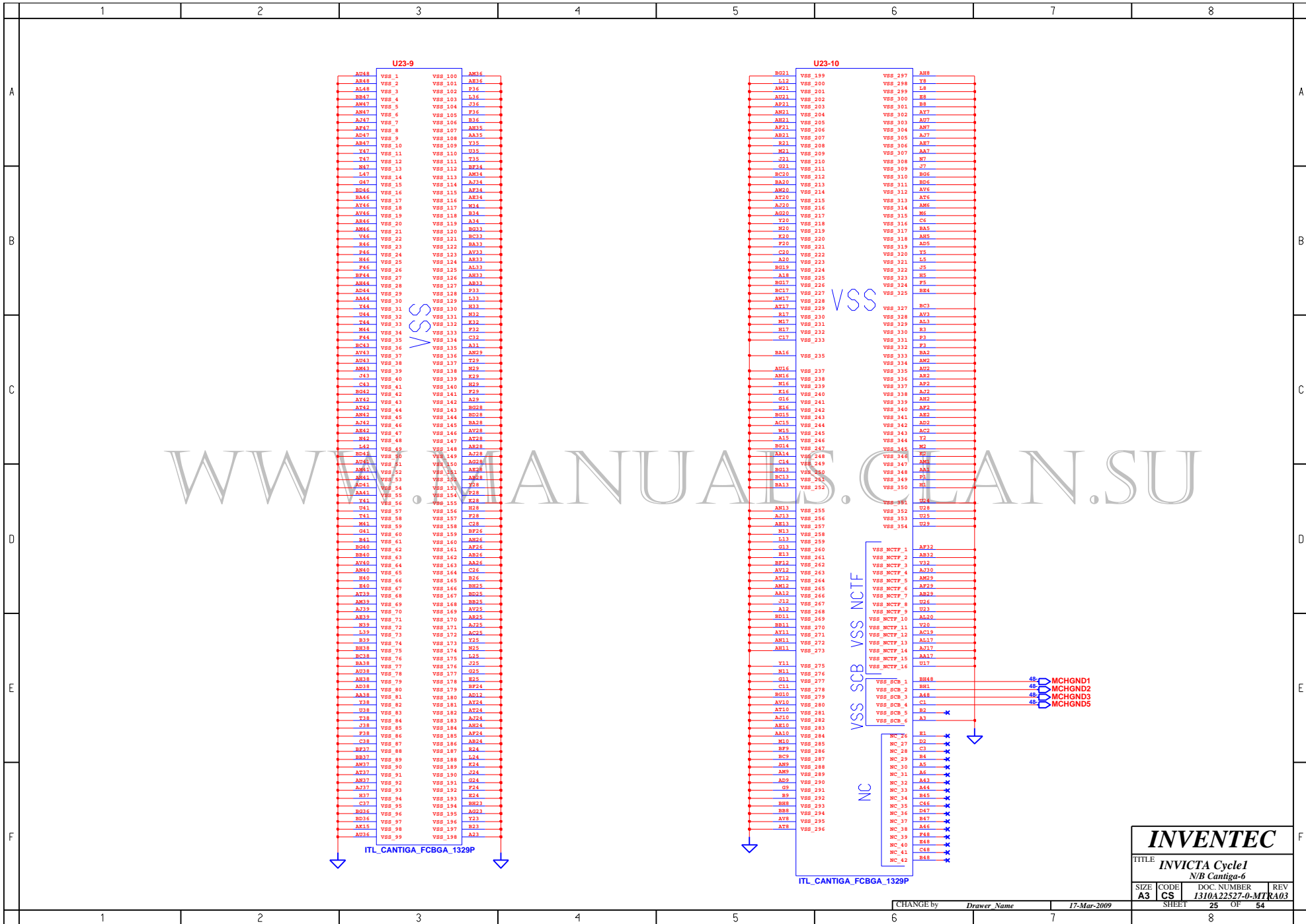


| | | | |
|--|-------------------|--------------------------------------|--------------------|
| INVENTEC | | | |
| TITLE <i>INVICTA Cycle1</i> <i>N/B Cantiga-4</i> | | | |
| SIZE A3 | CODE CS | DOC NUMBER <i>1310A22527-0-MT</i> | REV RA03 |
| CHANGE by <i>Drawer Name</i> | | 17-Mar-2009 | |
| SHEET 23 | | OF 54 | |

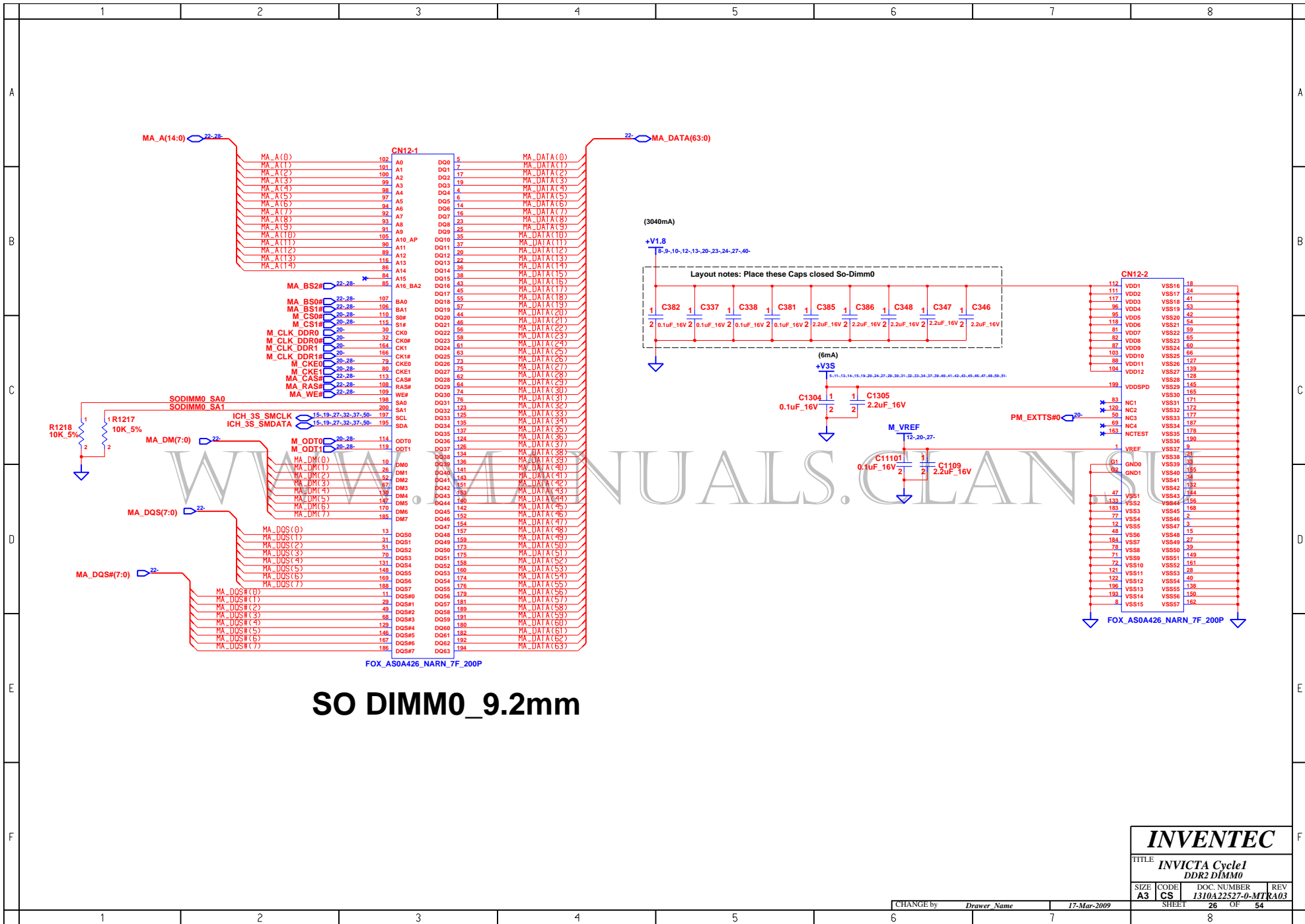


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| | | | |
|---|-------------------|---------------------------------------|-------------------|
| INVENTEC | | | |
| TITLE INVICTA Cycle1 N/B Cantiga-5 | | | |
| SIZE A3 | CODE CS | DOC NUMBER 1310A22527-0-MTR | REV A03 |
| CHANGE by <i>Drawer Name</i> | | 17-Mar-2009 | |
| SHEET 24 | | OF 54 | |



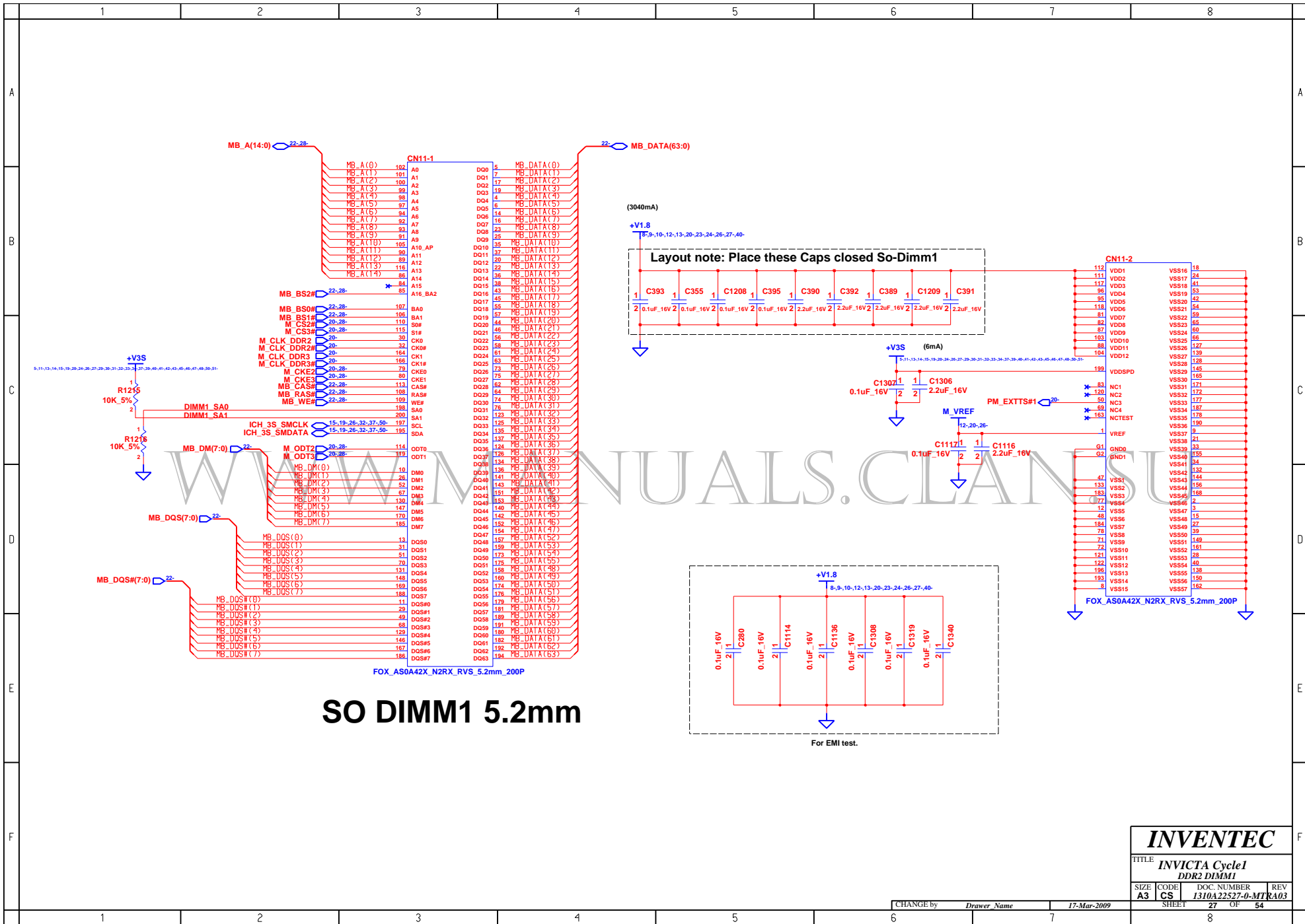
| | | | |
|--|----------------|-------------------------------------|----------------|
| INVENTEC | | | |
| TITLE INVICTA Cycle1 N/B Cantiga-6 | | | |
| SIZE A3 | CODE CS | DOC. NUMBER 1310A22527-0-MTR | REV A03 |
| CHANGE by Drawer Name | | 17-Mar-2009 | |
| SHEET 25 | | OF 54 | |



SO DIMM0_9.2mm

FOX_AS0A426_NARN_7F_200P

| | | | |
|---|-------------------|--|-------------------|
| INVENTEC | | | |
| TITLE INVICTA Cycle1 DDR2 DIMM0 | | | |
| SIZE A3 | CODE CS | DOC. NUMBER 1310A22527-0-MTR | REV A03 |
| CHANGE by <i>Drawer Name</i> | | 17-Mar-2009 | |
| SHEET 26 | | OF 54 | |



SO DIMM1 5.2mm

FOX_AS0A42X_N2RX_RVS_5.2mm_200P

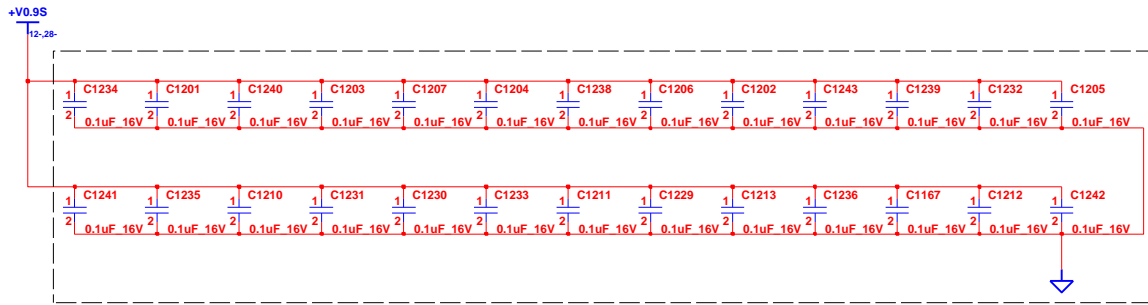
INVENTEC

TITLE: **INVICTA Cycle1
DDR2 DIMM1**

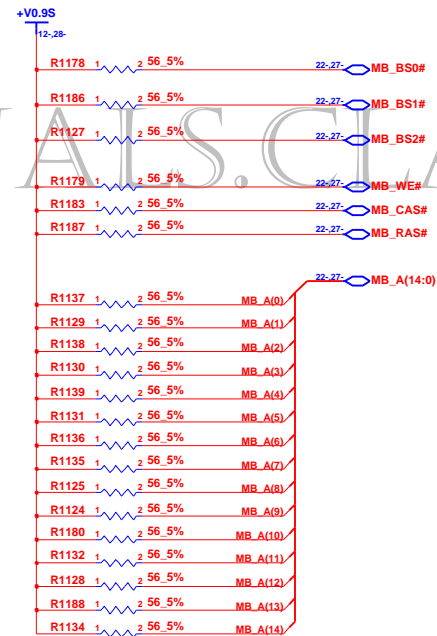
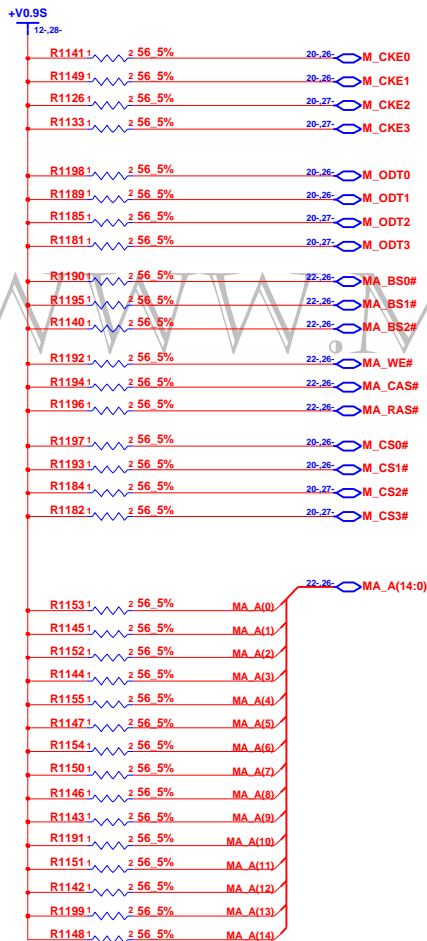
| | | | |
|------|------|-----------------|-----|
| SIZE | CODE | DOC. NUMBER | REV |
| A3 | CS | 1310A22527-0-MT | A03 |

CHANGE by *Drawer Name* 17-Mar-2009

SHEET 27 OF 54

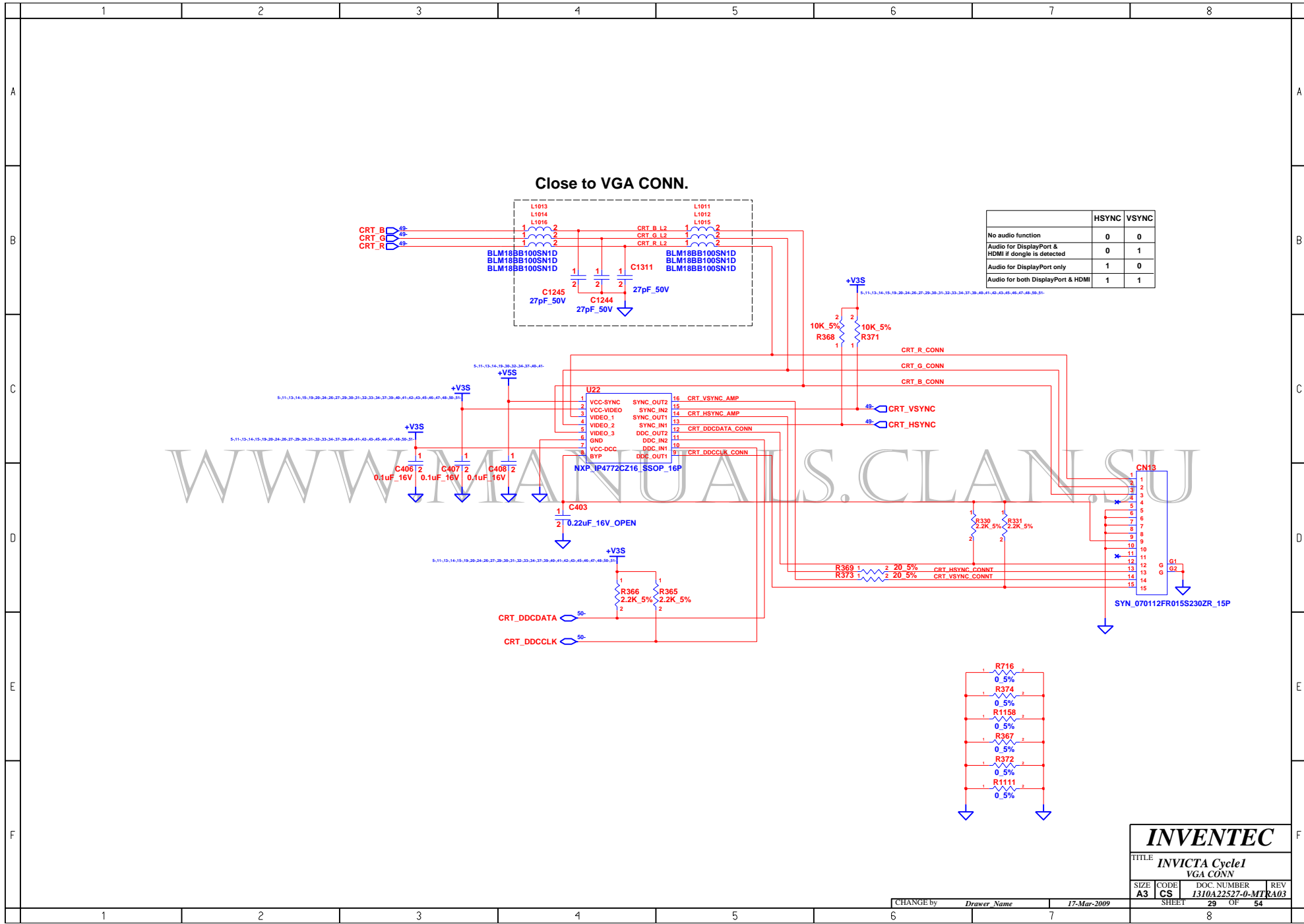


Layout notes : Place one Cap close to every 2 pull up resistor terminated to +V0.9S.



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| | | | |
|-----------------------------|------|------------------|-----|
| INVENTEC | | | |
| TITLE INVICTA Cycle1 | | | |
| DDR2 termination | | | |
| SIZE | CODE | DOC. NUMBER | REV |
| A3 | CS | I310A22527-0-MTR | A03 |
| CHANGE by | | 27-Sep-2003 | REV |
| Drawer Name | | | 54 |
| SHEET | | 28 | OF |
| | | 8 | |



Close to VGA CONN.

| | HSYNC | VSYNC |
|--|-------|-------|
| No audio function | 0 | 0 |
| Audio for DisplayPort & HDMI if dongle is detected | 0 | 1 |
| Audio for DisplayPort only | 1 | 0 |
| Audio for both DisplayPort & HDMI | 1 | 1 |

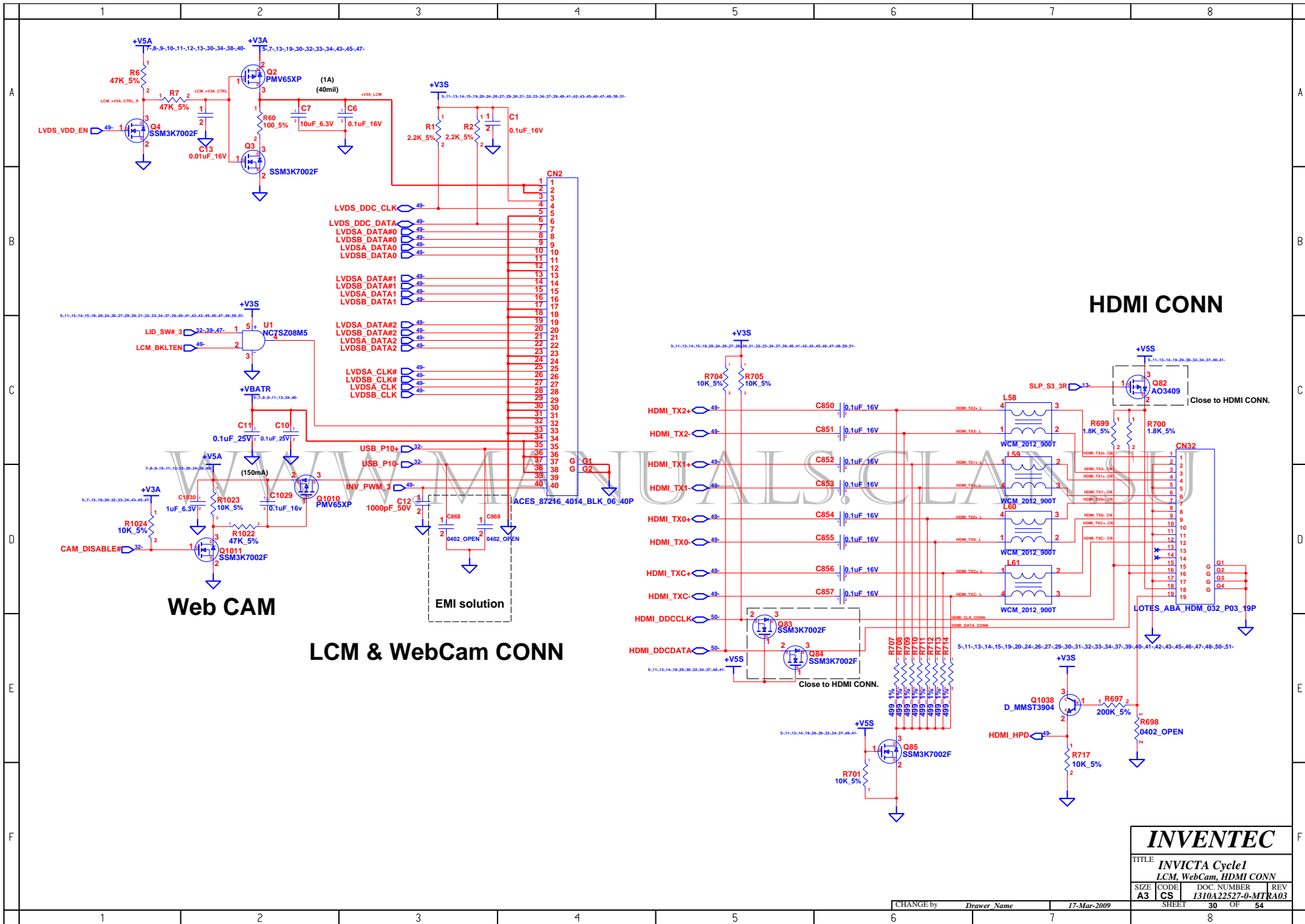
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INVENTEC

TITLE: **INVICTA Cycle1
VGA CONN**

| | | | |
|------|------|------------------|-----|
| SIZE | CODE | DOC. NUMBER | REV |
| A3 | CS | I310A22527-0-MTR | A03 |

CHANGE by: *Drawer Name* 17-Mar-2009 SHEET 29 OF 54



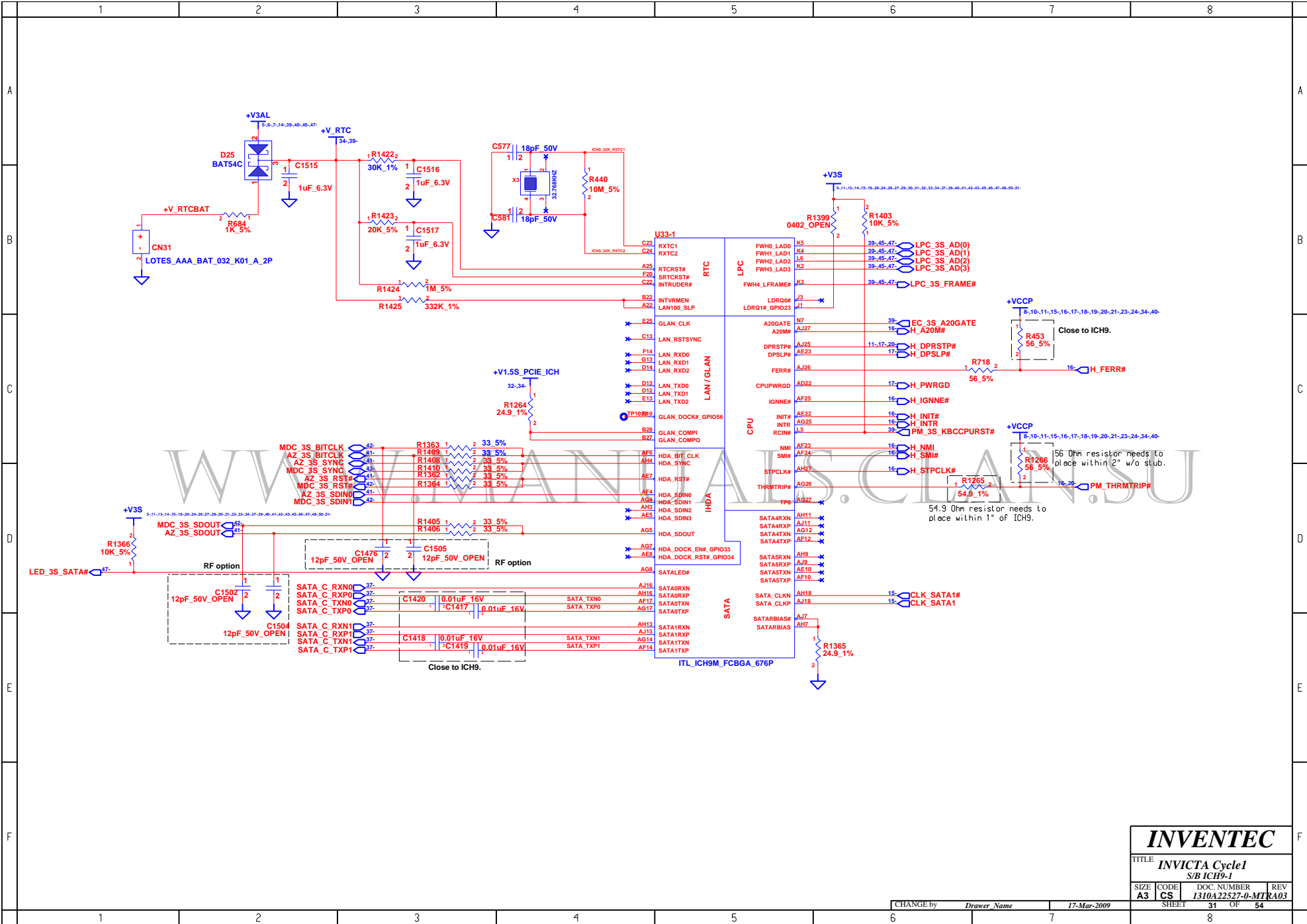
Web CAM

LCM & WebCam CONN

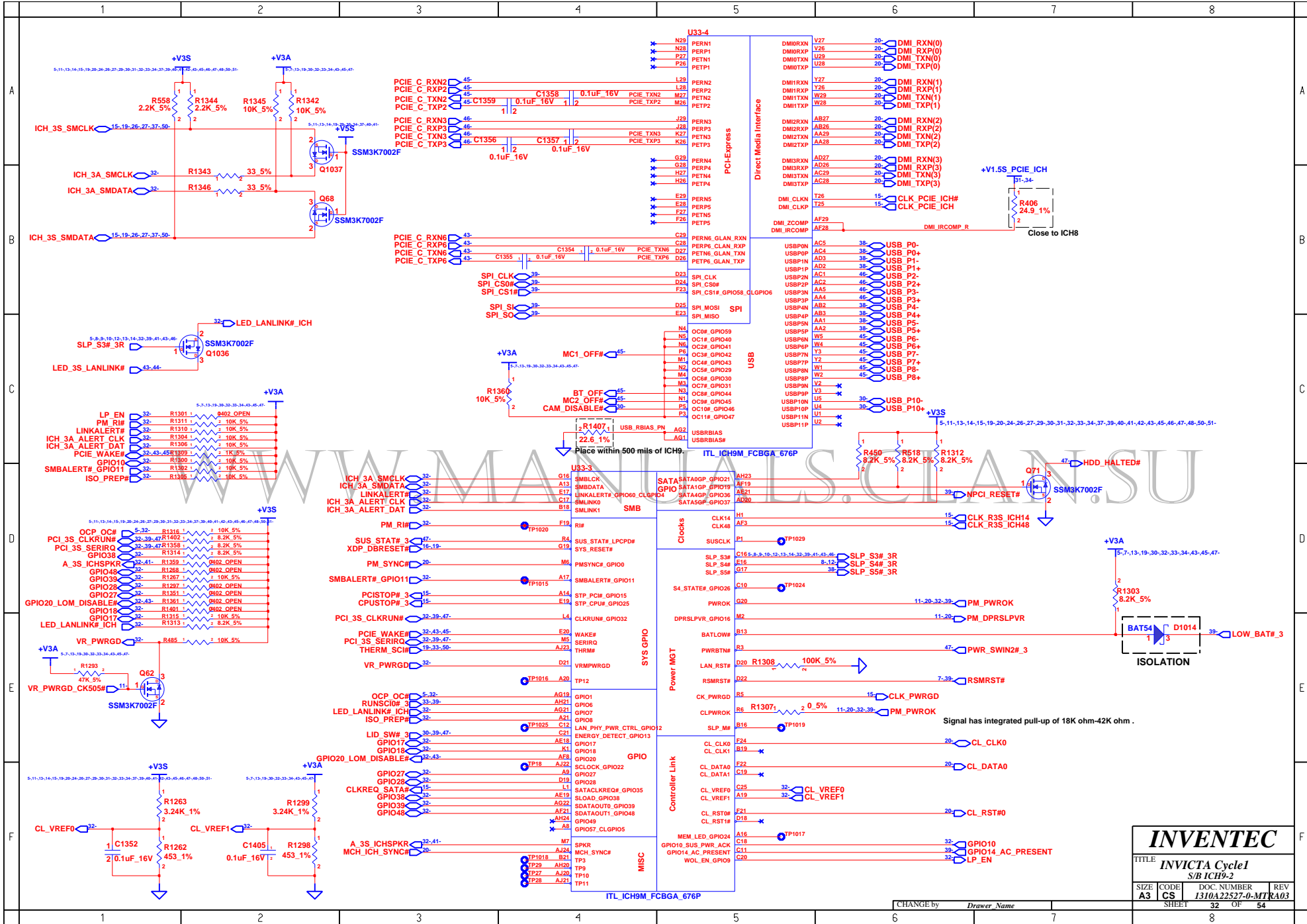
HDMI CONN

INVENTEC

| | | | |
|------------------------------|----------------|-------------------------------------|------------------------------|
| TITLE <i>INVICTA Cycle1</i> | | | |
| LCM, WebCam, HDMI CONN | | | |
| SIZE A3 | CODE CS | DOC. NUMBER I310A22527-0-MTR | REV A03 |
| CHANGE by <i>Drawer Name</i> | | 17-Mar-2009 | SHEET 30 OF 54 |

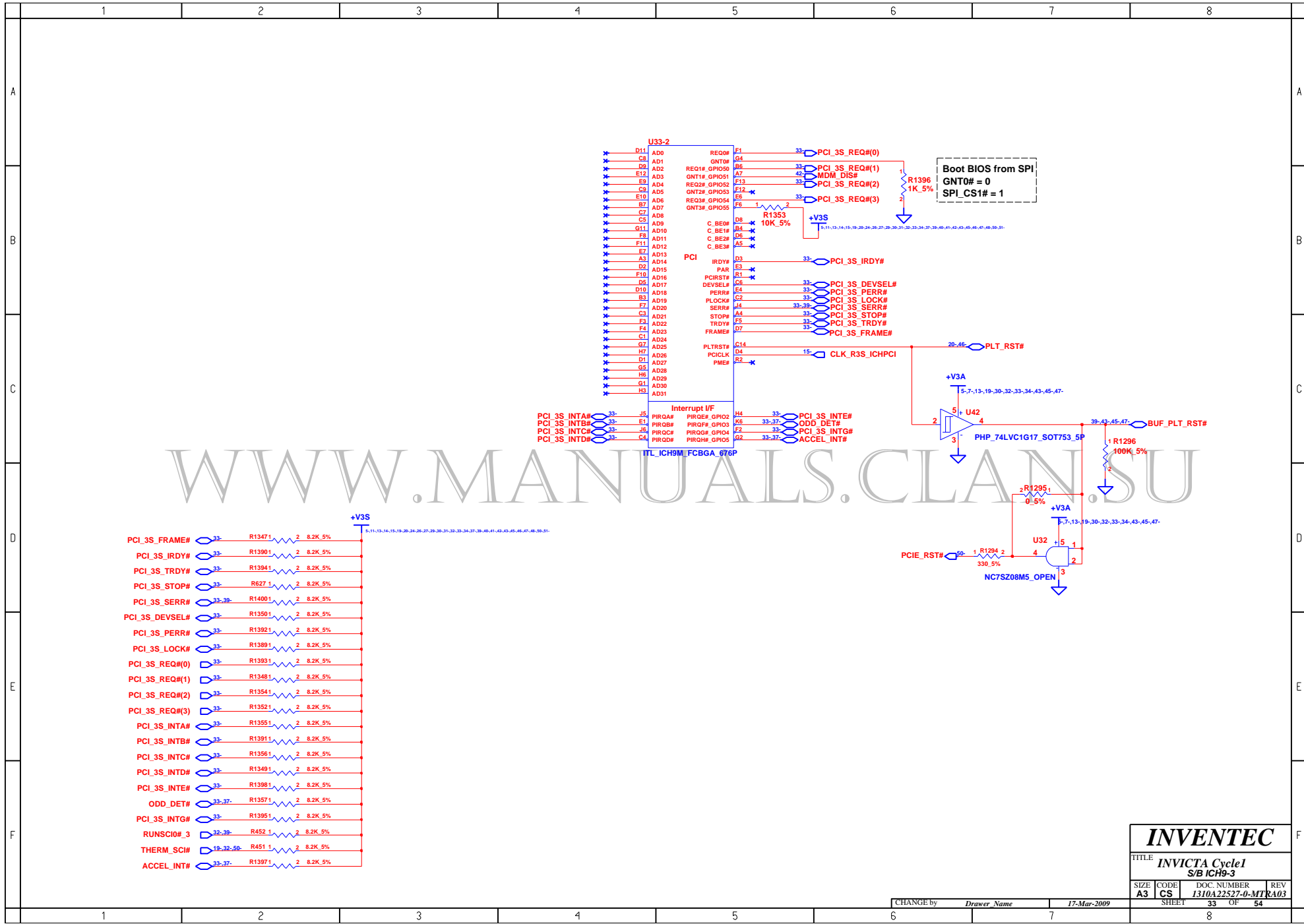


| | | | |
|----------------------------------|----------|-------------------------------|----------------|
| INVENTEC | | | |
| TITLE: INVICTA Cycle1 S/B ICH9-1 | | | |
| SIZE: A3 | CODE: CS | DOC. NUMBER: 1310A22527-0-MTR | REV: A03 |
| CHANGE by: Drawer Name | | 17-Mar-2009 | SHEET 31 OF 54 |

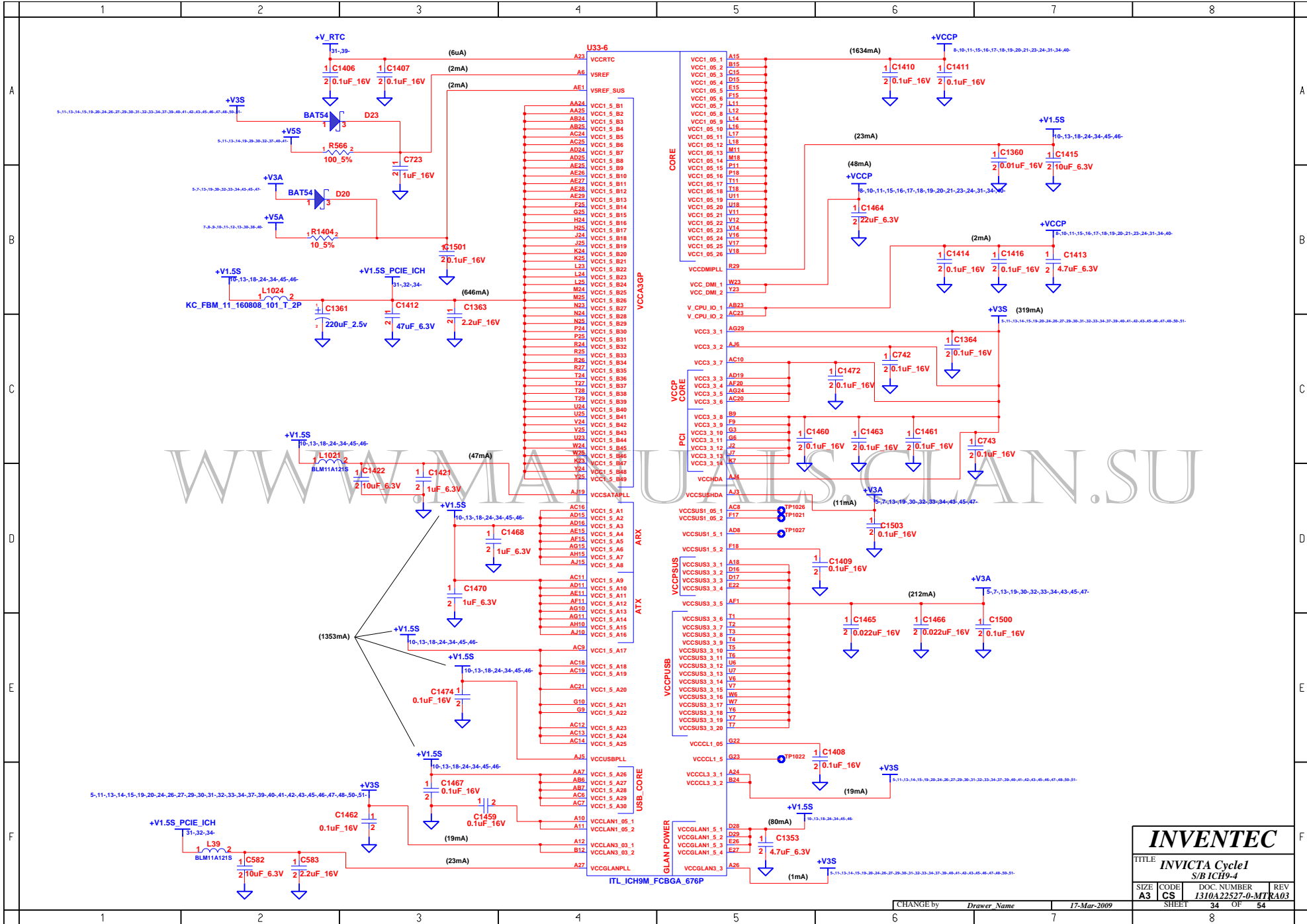


| | | | |
|---|------|------------------|-------|
| INVENTEC | | | |
| TITLE: INVICTA Cycle1 S/B ICH9-2 | | | |
| SIZE | CODE | DOC. NUMBER | REV |
| A3 | CS | 1310A22527-0-MTR | A03 |
| SHEET | | 32 | OF 54 |

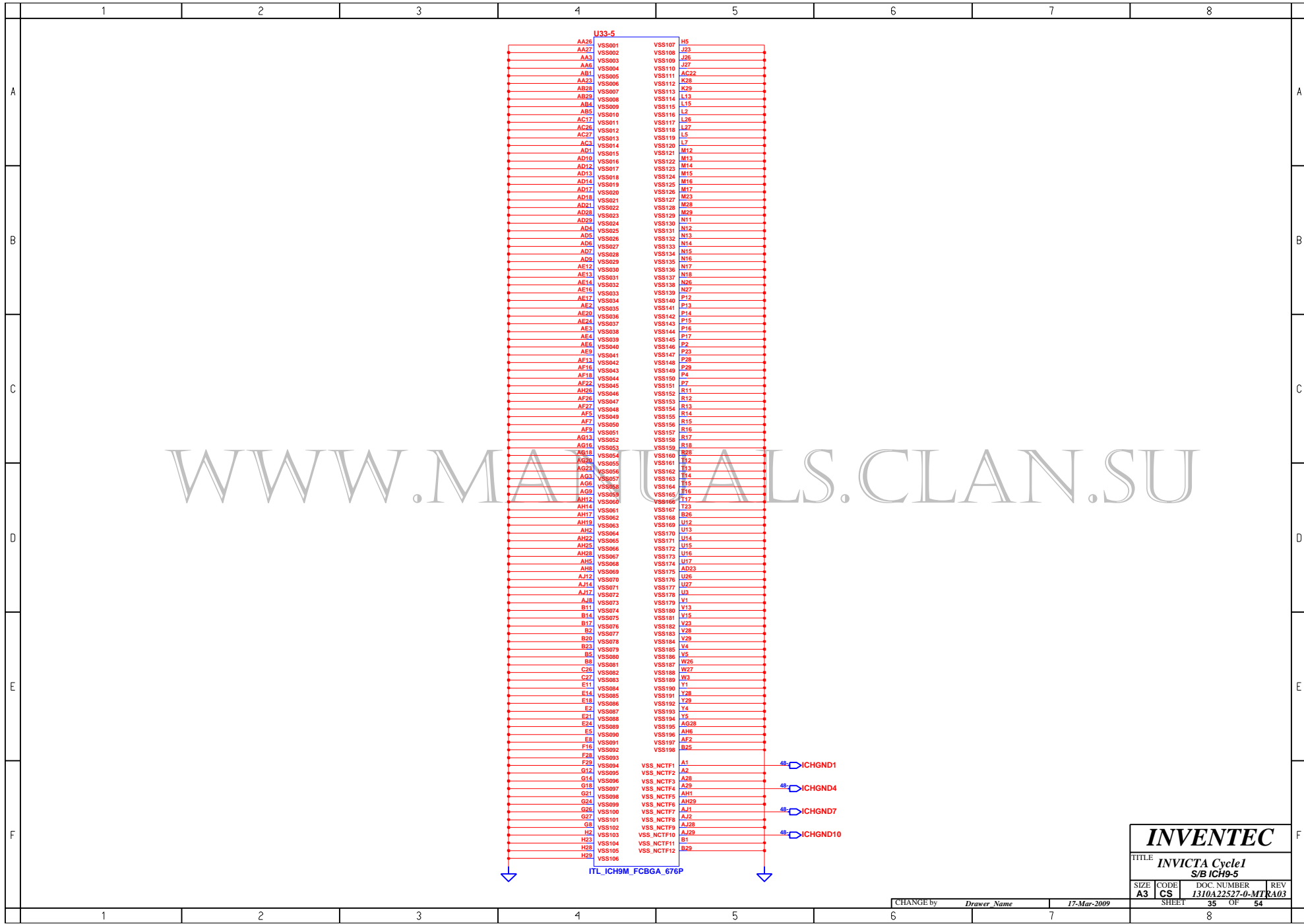
CHANGE by *Drawer Name* 8



| | | | |
|---------------------------------------|------------|--------------------------------|------------|
| INVENTEC | | | |
| TITLE INVICTA Cycle1 S/B ICH9-3 | | | |
| SIZE A3 | CODE CS | DOC NUMBER I310A22527-0-MTR | REV A03 |
| CHANGE by Drawer Name | | 17-Mar-2009 | |
| SHEET 33 | | OF 54 | |



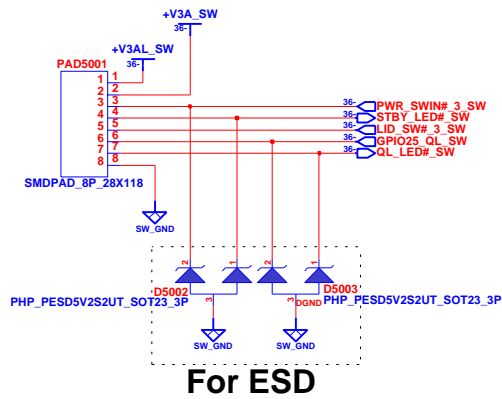
| | | | |
|--|-------------------|--|-------------------|
| INVENTEC | | | |
| TITLE INVICTA Cycle1 S/B ICH9-4 | | | |
| SIZE A3 | CODE CS | DOC. NUMBER I310A22527-0-MTR | REV A03 |
| CHANGE by Drawer Name | | 17-Mar-2009 | |
| SHEET 34 | | OF 54 | |



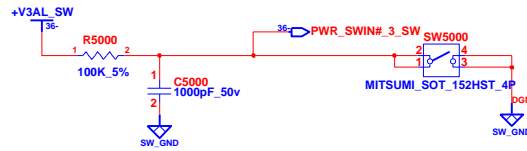
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| | | | |
|-----------------------------|------|------------------|-------------|
| INVENTEC | | | |
| TITLE INVICTA Cycle1 | | | |
| S/B ICH9-5 | | | |
| SIZE | CODE | DOC. NUMBER | REV |
| A3 | CS | 1310A22527-0-MTR | A03 |
| CHANGE by | | Drawer Name | 17-Mar-2009 |
| SHEET | | 35 | OF 54 |

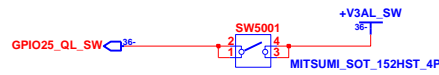
PWR SW B/B CONN



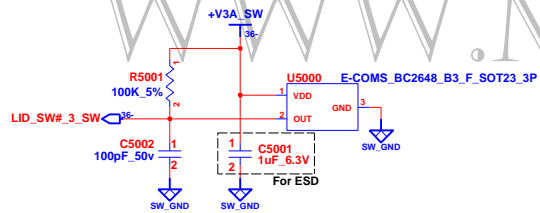
Power Button



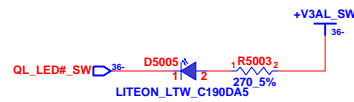
Quick Look Button



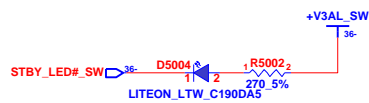
LID Switch



Quick Look LED



Power / Standby LED



- FIX5000
- FIX_MASK
- FIX5001
- FIX_MASK
- FIX5002
- FIX_MASK
- FIX5003
- FIX_MASK
- FIX5004
- FIX_MASK
- FIX5005
- FIX_MASK

Power & LID Switch Board

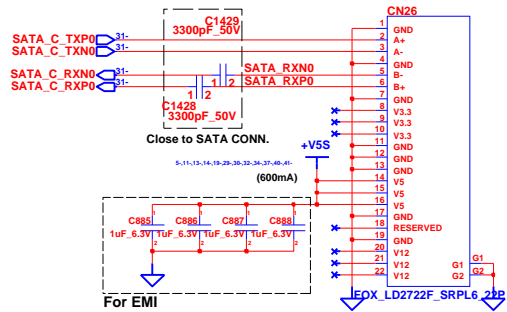
INVENTEC

TITLE *INVICTA Cycle1*
PWR, LID, APP SW/Bs

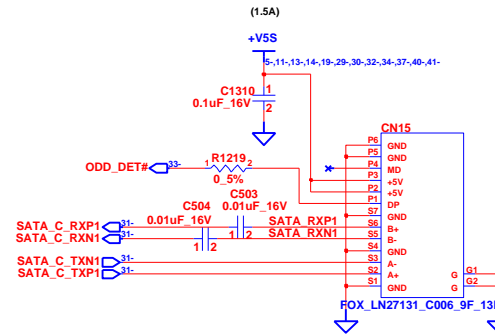
| | | | |
|------|------|------------------|-----|
| SIZE | CODE | DOC NUMBER | REV |
| A3 | CS | 1310A22527-0-MTR | A03 |

CHANGE by *Drawer Name* 17-Mar-2009

SHEET 36 OF 54

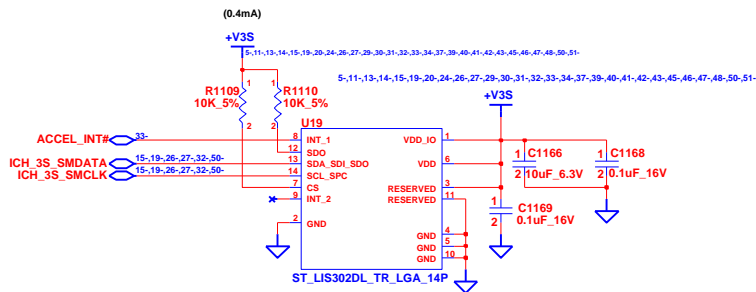


SATA HDD

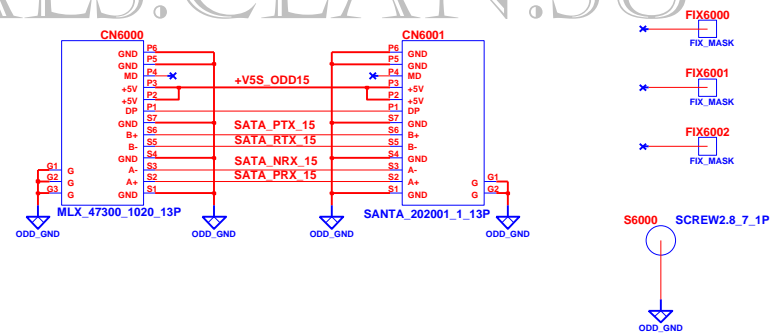


SATA ODD

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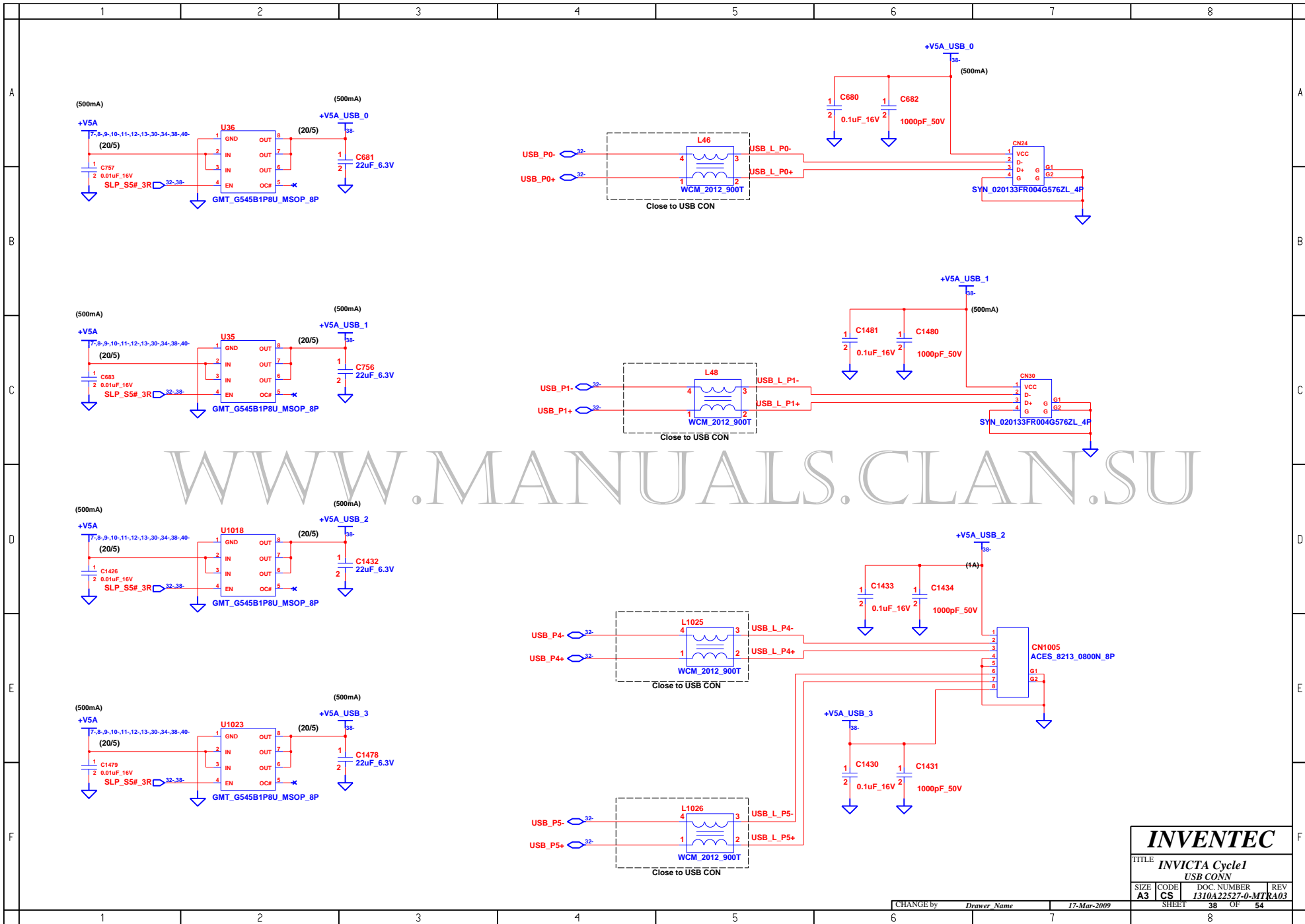
Accelerometer



15" ODD Extend Board

INVENTEC

| | | | |
|--|-------------------|---------------------------------------|-------------------|
| TITLE INVICTA Cycle1 | | | |
| HDD & ODD CONN & Accelerometer & 15" ODD EXT B | | | |
| SIZE A3 | CODE CS | DOC NUMBER I310A22527-0-MTR | REV A03 |
| CHANGE by <i>Drawer Name</i> | | 17-Mar-2009 | |
| SHEET 37 | | OF 54 | |



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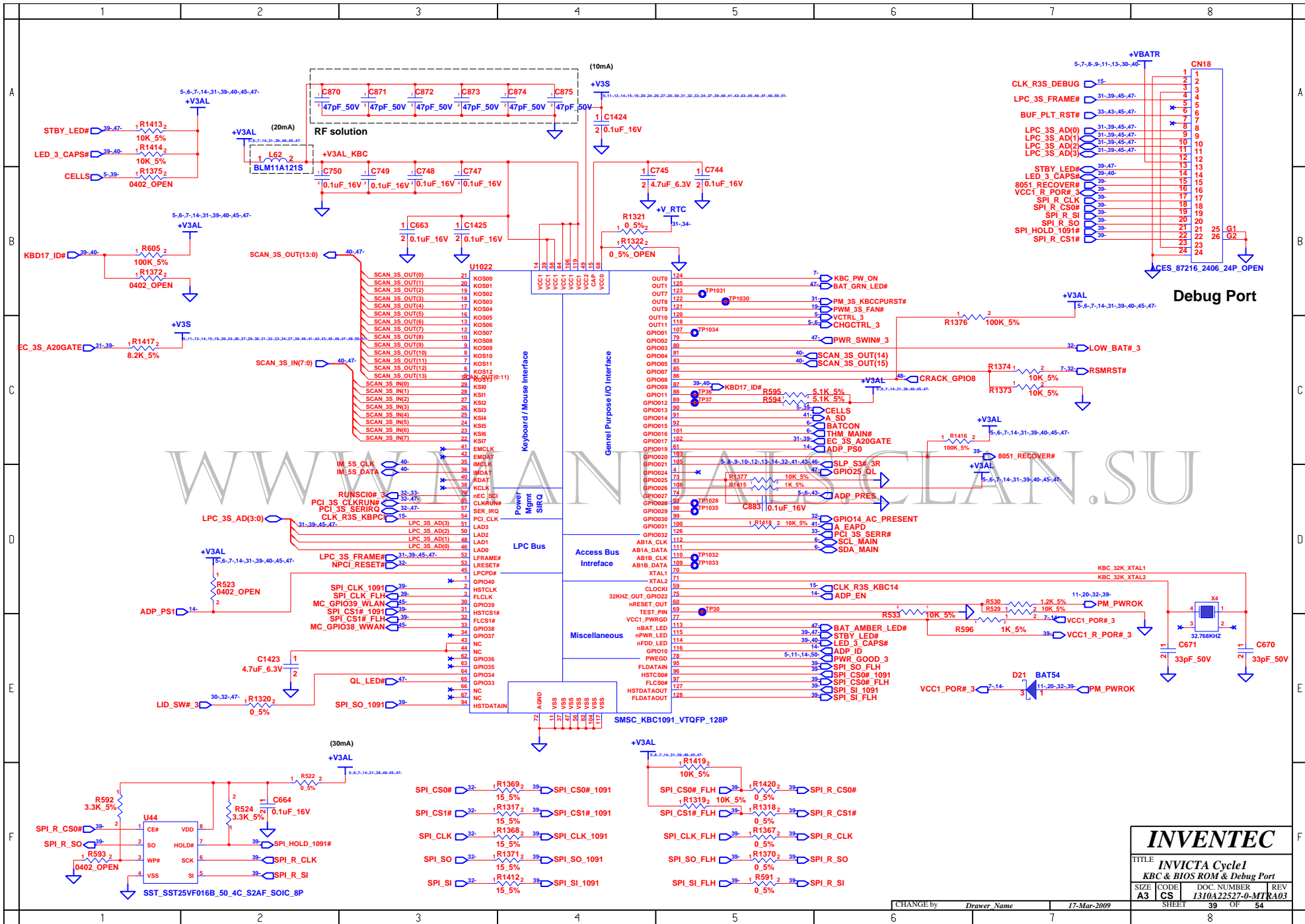
INVENTEC

TITLE
INVICTA Cycle1
 USB CONN

| | | | |
|---------------------------------|-------------------|---------------------------------------|-------------------|
| SIZE A3 | CODE CS | DOC NUMBER 1310A22527-0-MTR | REV A03 |
| CHANGE by <i>Drawer Name</i> | | 17-Mar-2009 | |
| SHEET 38 | | OF 54 | |

CHANGE by *Drawer Name* 17-Mar-2009

SHEET 38 OF 54



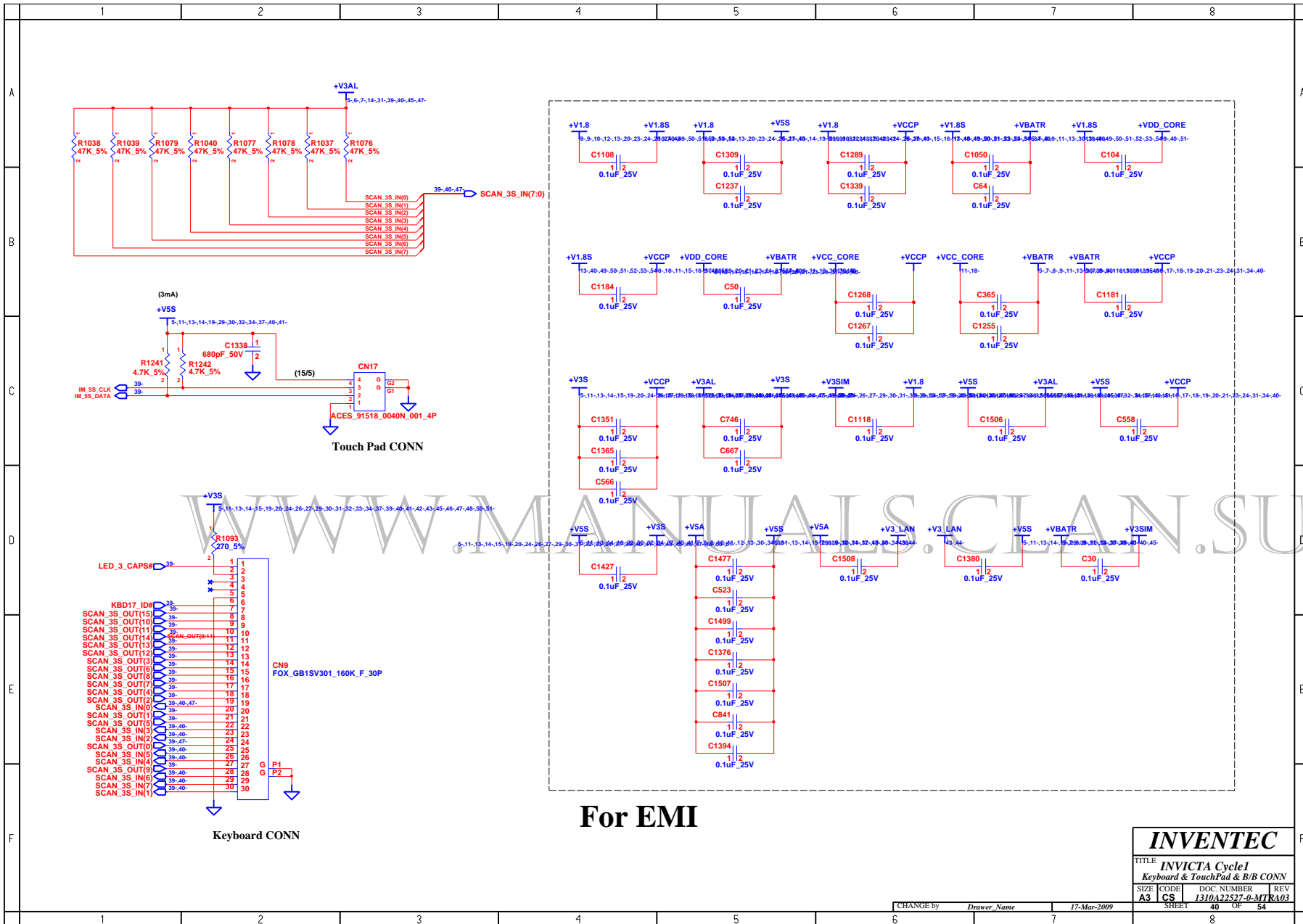
INVENTEC

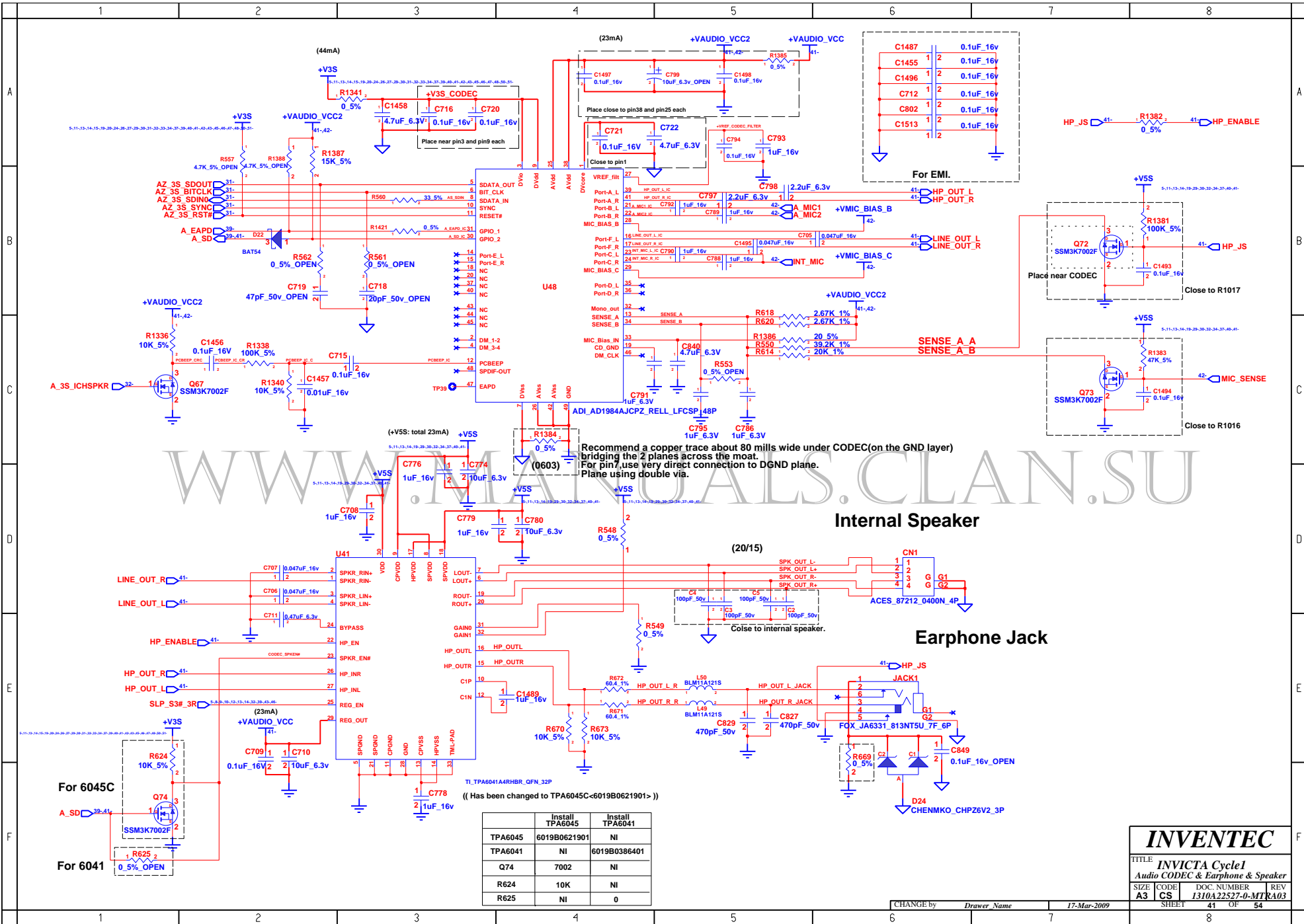
TITLE: **INVICTA Cycle1**
KBC & BIOS ROM & Debug Port

| SIZE | CODE | DOC NUMBER | REV |
|------|------|------------------|-----|
| A3 | CS | 1310A22527-0-MTR | A03 |

SHEET 39 OF 54

CHANGE by *Drawer Name* 17-Mar-2009





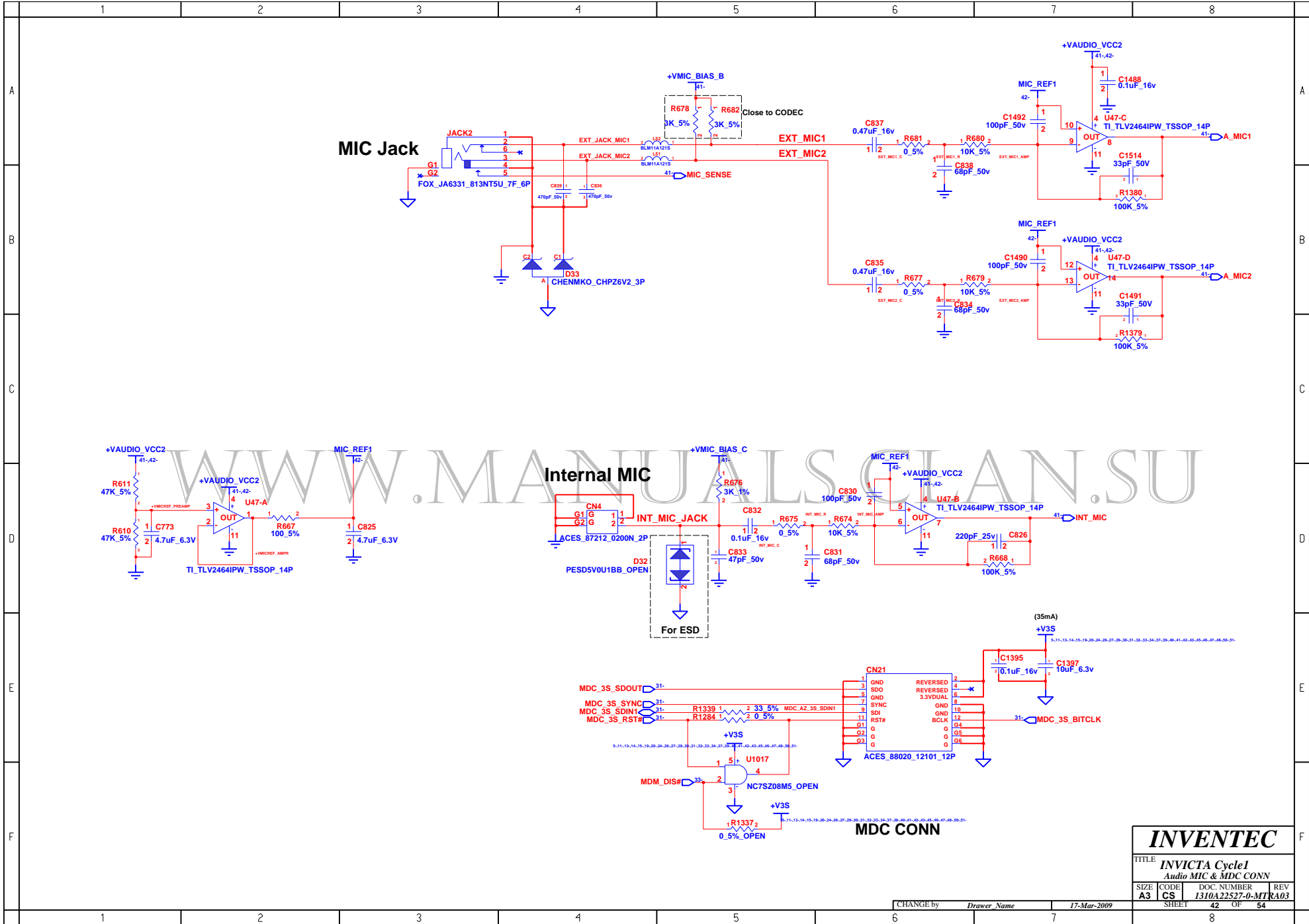
Recommend a copper trace about 80 mills wide under CODEC(on the GND layer) bridging the 2 planes across the moat.
 For pin7, use very direct connection to DGND plane.
 Plane using double via.

Internal Speaker

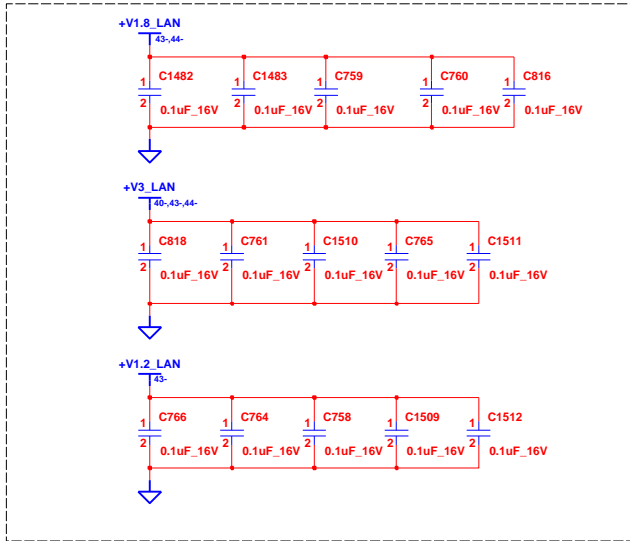
Earphone Jack

| | Install TPA6045 | Install TPA6041 |
|---------|-----------------|-----------------|
| TPA6045 | 6019B0621901 | NI |
| TPA6041 | NI | 6019B0386401 |
| Q74 | 7002 | NI |
| R624 | 10K | NI |
| R625 | NI | 0 |

| | | | |
|----------------------------------|------|------------------|-------------|
| INVENTEC | | | |
| TITLE <i>INVICTA Cycle1</i> | | | |
| Audio CODEC & Earphone & Speaker | | | |
| SIZE | CODE | DOC NUMBER | REV |
| A3 | CS | 1310A22527-0-MTR | A03 |
| CHANGE by | | Drawer Name | 17-Mar-2009 |
| | | SHEET | 41 OF 54 |

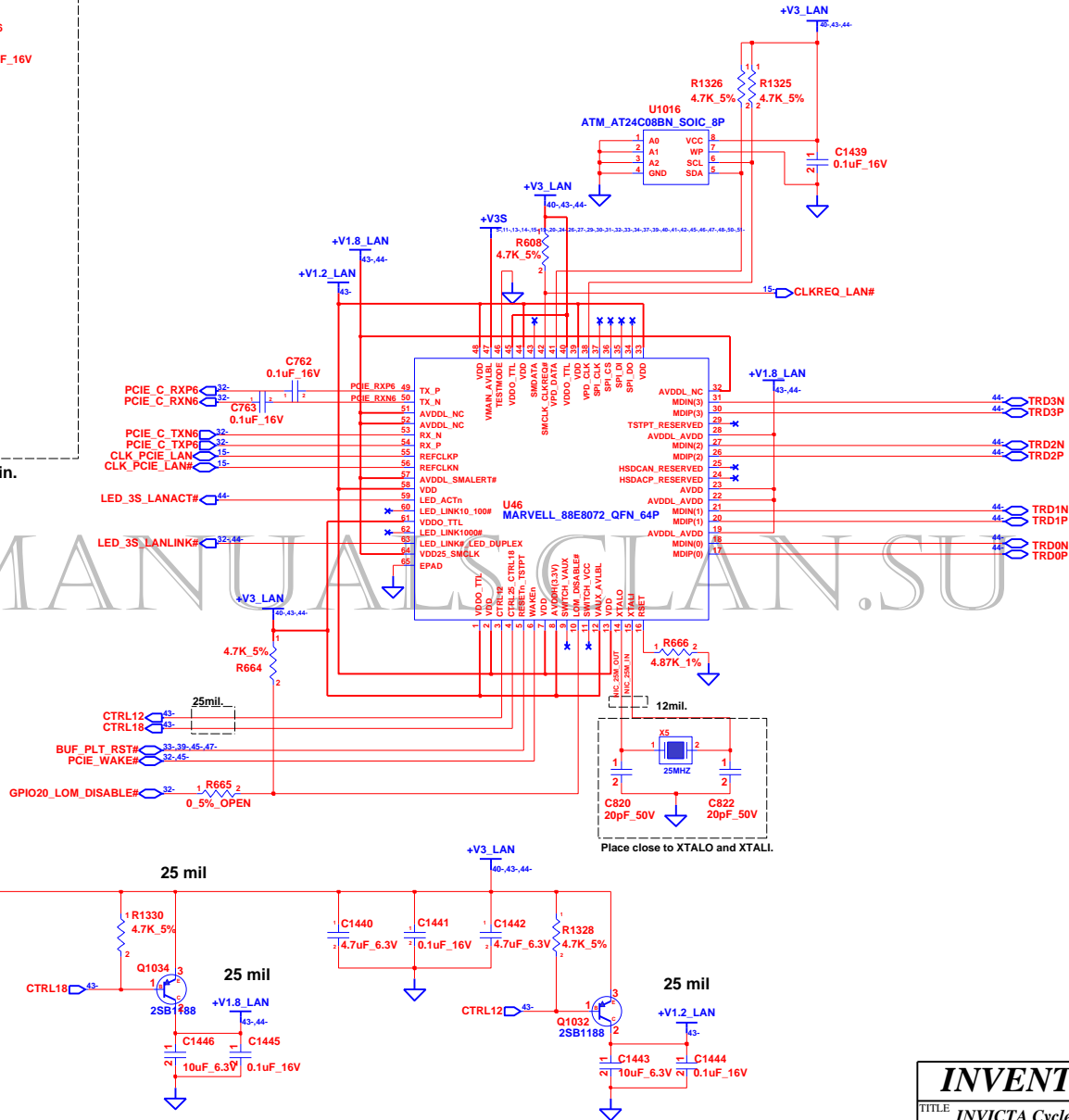


| | | | |
|------------------------------|------|------------------|-------------|
| INVENTEC | | | |
| TITLE: INVICTA Cycle1 | | | |
| Audio MIC & MDC CONN | | | |
| SIZE | CODE | DOC. NUMBER | REV |
| A3 | CS | 1310A22527-0-MTR | A03 |
| CHANGE by | | Drawer Name | 17-Mar-2009 |
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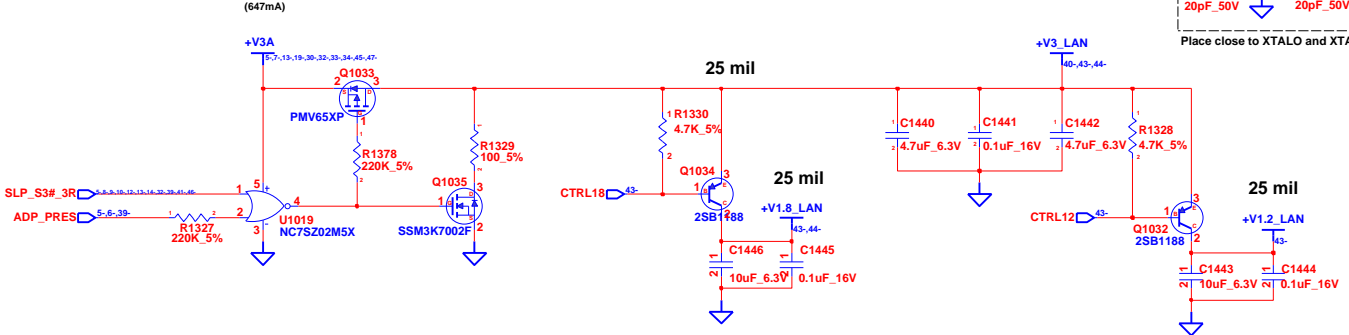


Place bypass cap as close as possible with every power pin.

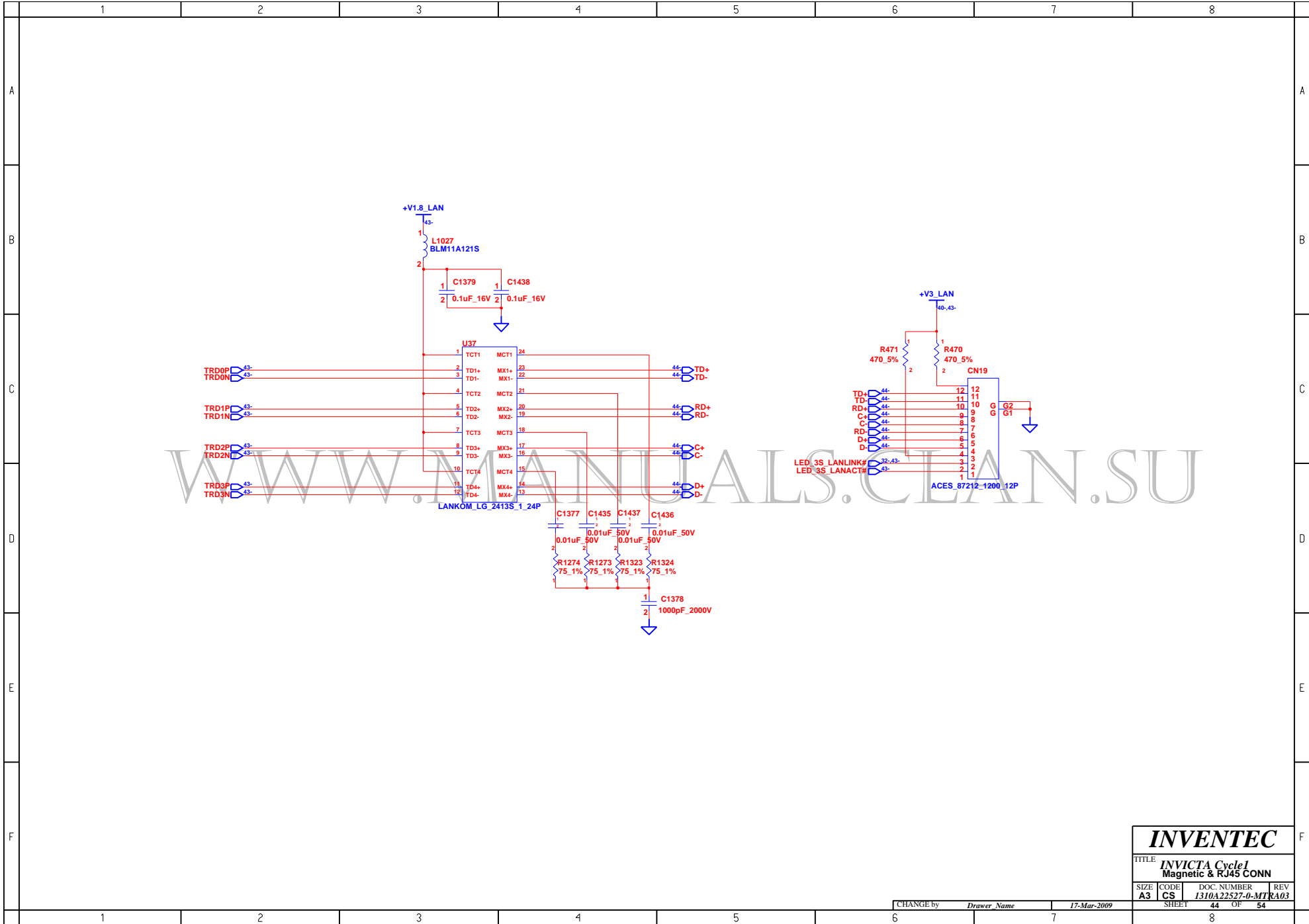
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Place close to XTAL0 and XTAL1.



| | | | |
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| INVENTEC | | | |
| TITLE: INVICTA Cycle1 | | | |
| Giga LAN Controller | | | |
| SIZE | CODE | DOC. NUMBER | REV |
| A3 | CS | 1310A22527-0-MTR | A03 |
| CHANGE by | | Drawer Name | 17-Mar-2009 |
| SHEET | | 43 | OF 54 |



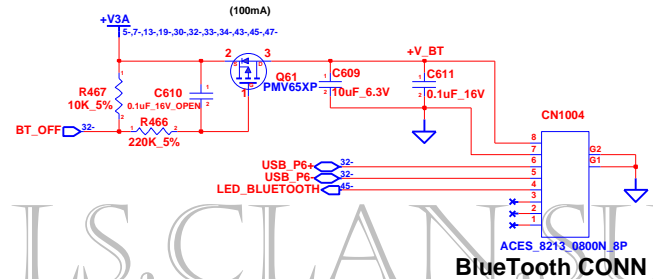
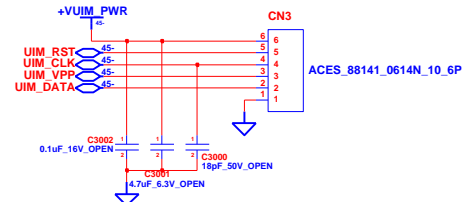
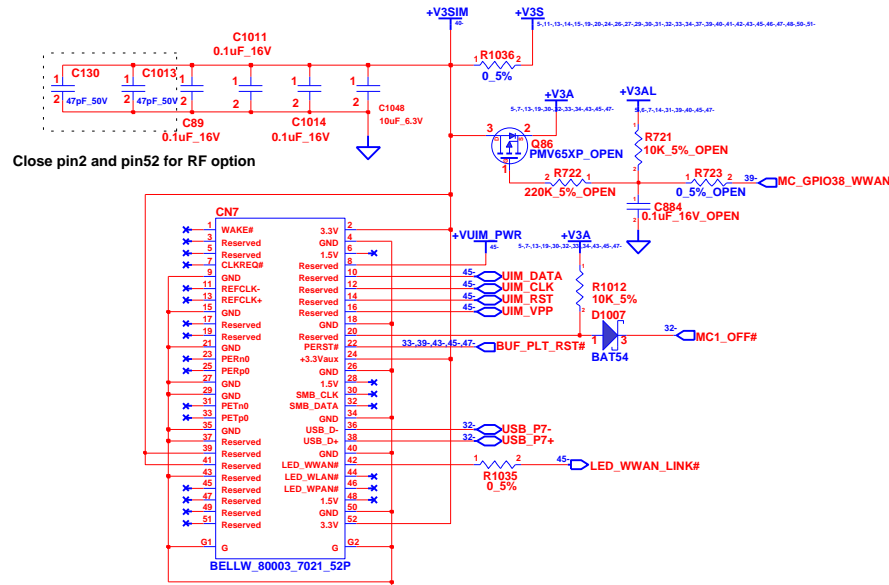
INVENTEC

TITLE *INVICTA Cycle1*
Magnetic & RJ45 CONN

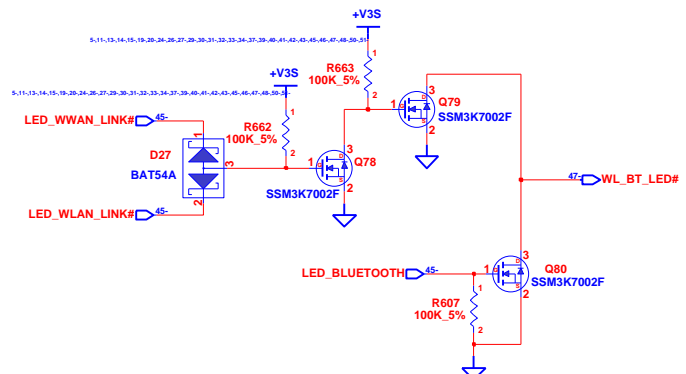
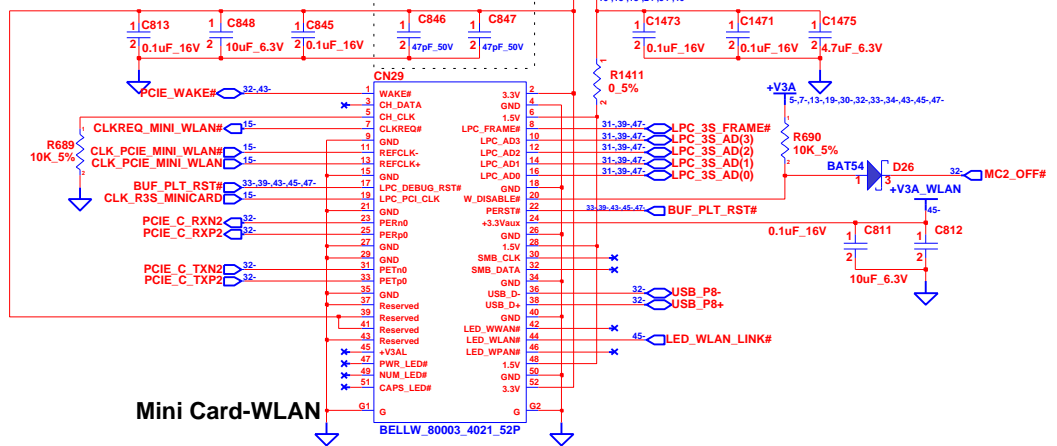
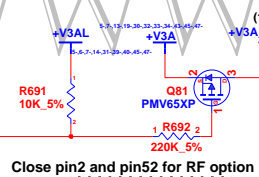
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|-------------------|-------------------|--|-------------------|
| SIZE A3 | CODE CS | DOC. NUMBER 1310A22527-0-MTR | REV A03 |
|-------------------|-------------------|--|-------------------|

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| CHANGE by | Drawer Name | 17-Mar-2009 | SHEET 44 OF 54 |
|-----------|-------------|-------------|----------------|

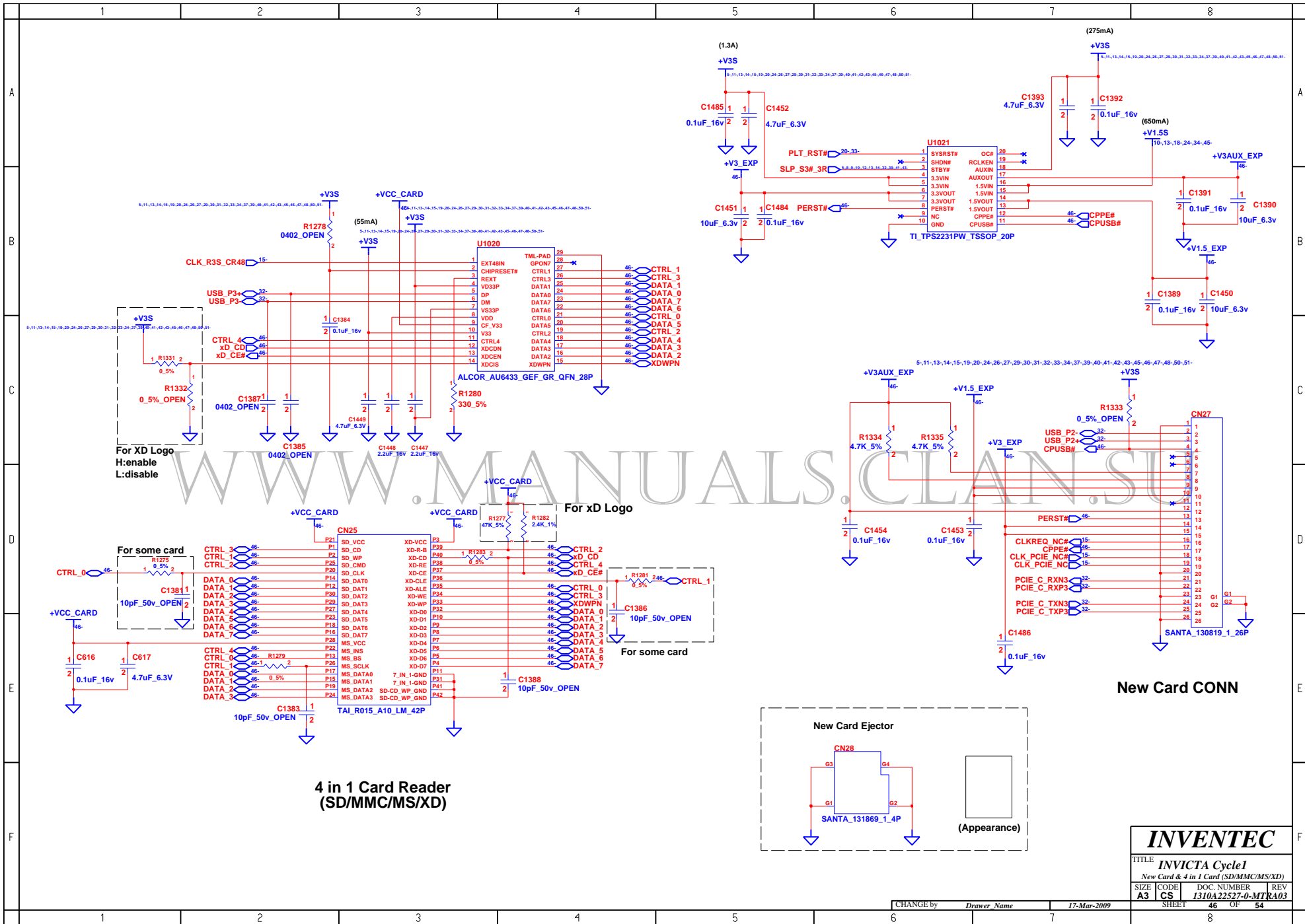
MINI Card-WWAN

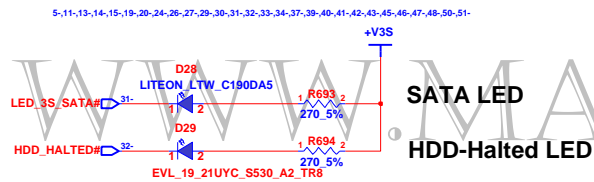
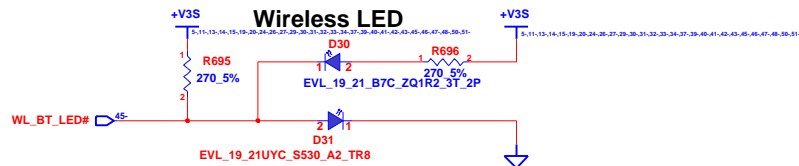
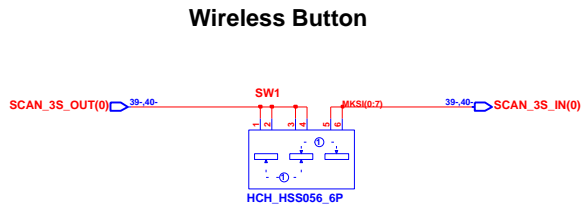


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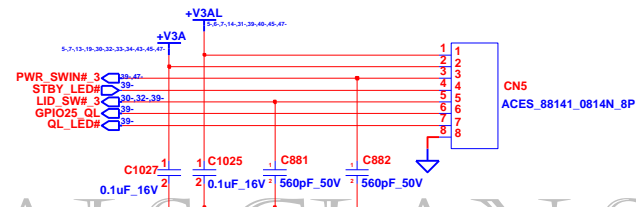
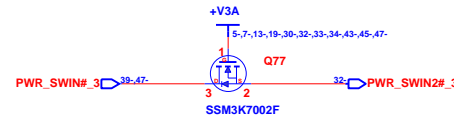
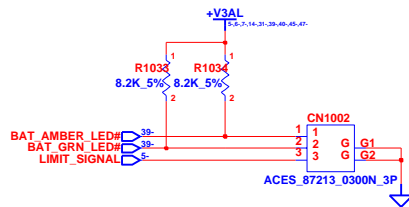


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|------------------------------|------|------------------|-------------|
| INVENTEC | | | |
| TITLE: <i>INVICTA Cycle1</i> | | | |
| Mini Card (WLAN/WWAN) / BT | | | |
| SIZE | CODE | DOC. NUMBER | REV |
| A3 | CS | I310A22527-0-MTR | A03 |
| CHANGE by | | Drawer Name | 17-Mar-2009 |
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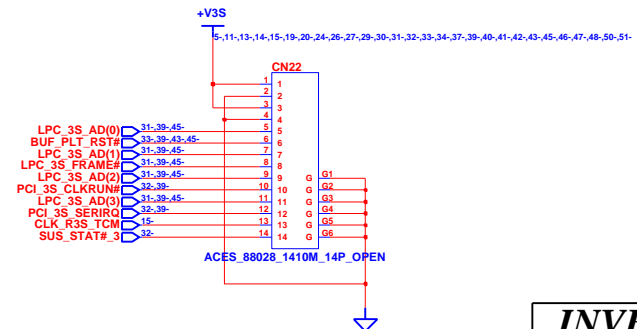




Battery Charge LED CONN



TCM CONN



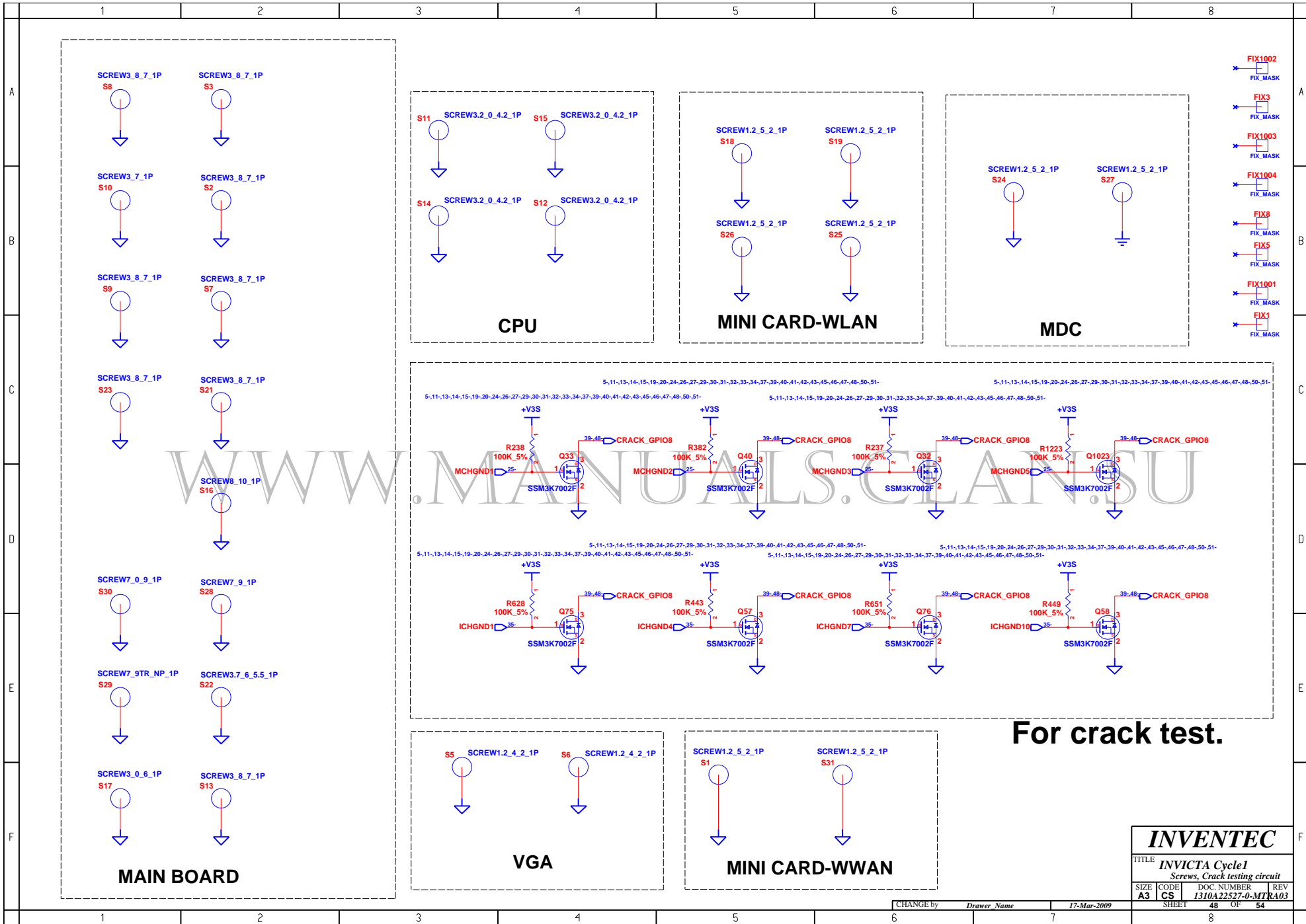
INVENTEC

TITLE
INVICTA Cycle1
LEDs & TCM CONN

| | | | |
|-------------------|-------------------|---------------------------------------|-------------------|
| SIZE A3 | CODE CS | DOC NUMBER I310A22527-0-MTR | REV A03 |
|-------------------|-------------------|---------------------------------------|-------------------|

CHANGE by *Drawer Name* 17-Mar-2009

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- FIX1002
- FIX_MASK
- FIX3
- FIX_MASK
- FIX1003
- FIX_MASK
- FIX1004
- FIX_MASK
- FIX8
- FIX_MASK
- FIX5
- FIX_MASK
- FIX1001
- FIX_MASK
- FIX1
- FIX_MASK

For crack test.

| | | | |
|--------------------------------|------------|--------------------------------|------------|
| INVENTEC | | | |
| TITLE <i>INVICTA Cycle1</i> | | | |
| Screws, Crack testing circuit | | | |
| SIZE A3 | CODE CS | DOC NUMBER 1310A22527-0-MTR | REV A03 |
| CHANGE by Drawer Name | | 17-Mar-2009 | |
| SHEET | | 48 OF 54 | |

| STRAPS | PIN | Description of default settings | |
|------------------|---------------|---------------------------------------|---------|
| TX_PWRS_ENB | GPIO0 | PCIe full TX output swing. | 1 |
| TX_DEEMPH_EN | GPIO1 | PCIe transmitter de-emphasis enabled. | 1 |
| BIF_DEBUG_ACCESS | GPIO4 | Debug signals muxed out. | 0 |
| ROMIDCFG(0:3) | GPIO[11:13,9] | Memory aperture type | X X X X |

X = DESIGN DEPENDANT
0 = DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR

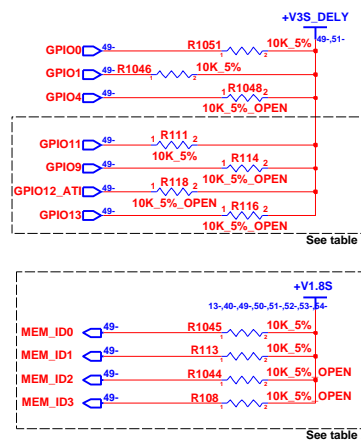
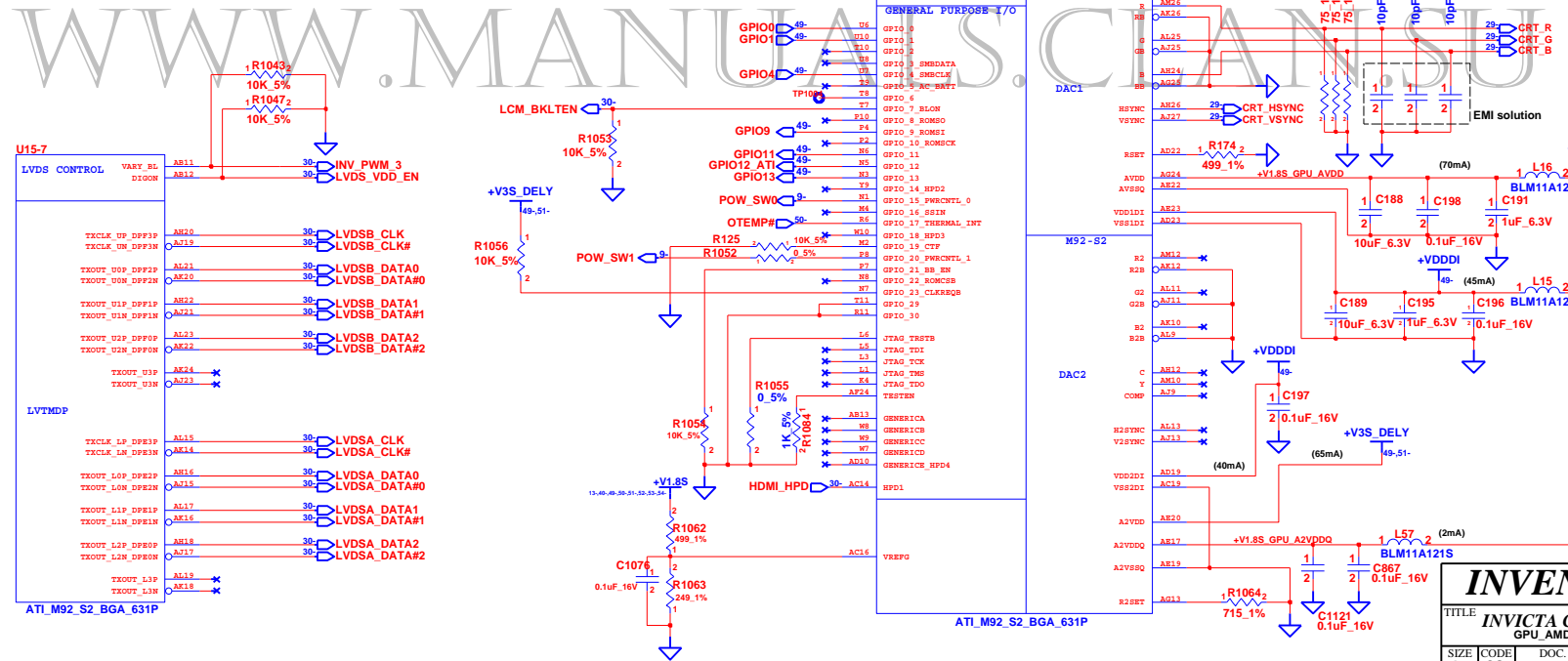
Table 1

| GPIO_13 | GPIO_12 | GPIO_11 | For DIS-GDDR2 |
|---------|---------|---------|---------------------------------------|
| 0 | 0 | 1 | 512MB/256MB memory aperture (Default) |
| 1 | 1 | 0 | reserved |

| POW_SW1 | POW_SW0 | +VDD_CORE |
|---------|---------|-----------|
| 0 | 0 | 1.0V |
| 0 | 1 | 0.95V |
| 1 | 0 | 0.9V |

Table 2

| For DIS-VRAM DDR2 | | | | |
|-------------------|---------|---------|---------|-------------------------|
| MEM_ID3 | MEM_ID2 | MEM_ID1 | MEM_ID0 | vendor |
| 0 | 0 | 0 | 1 | Samsung (512MB) |
| 0 | 0 | 1 | 0 | Qimonda (512MB) |
| 0 | 0 | 1 | 1 | Hynix (512MB) (Default) |

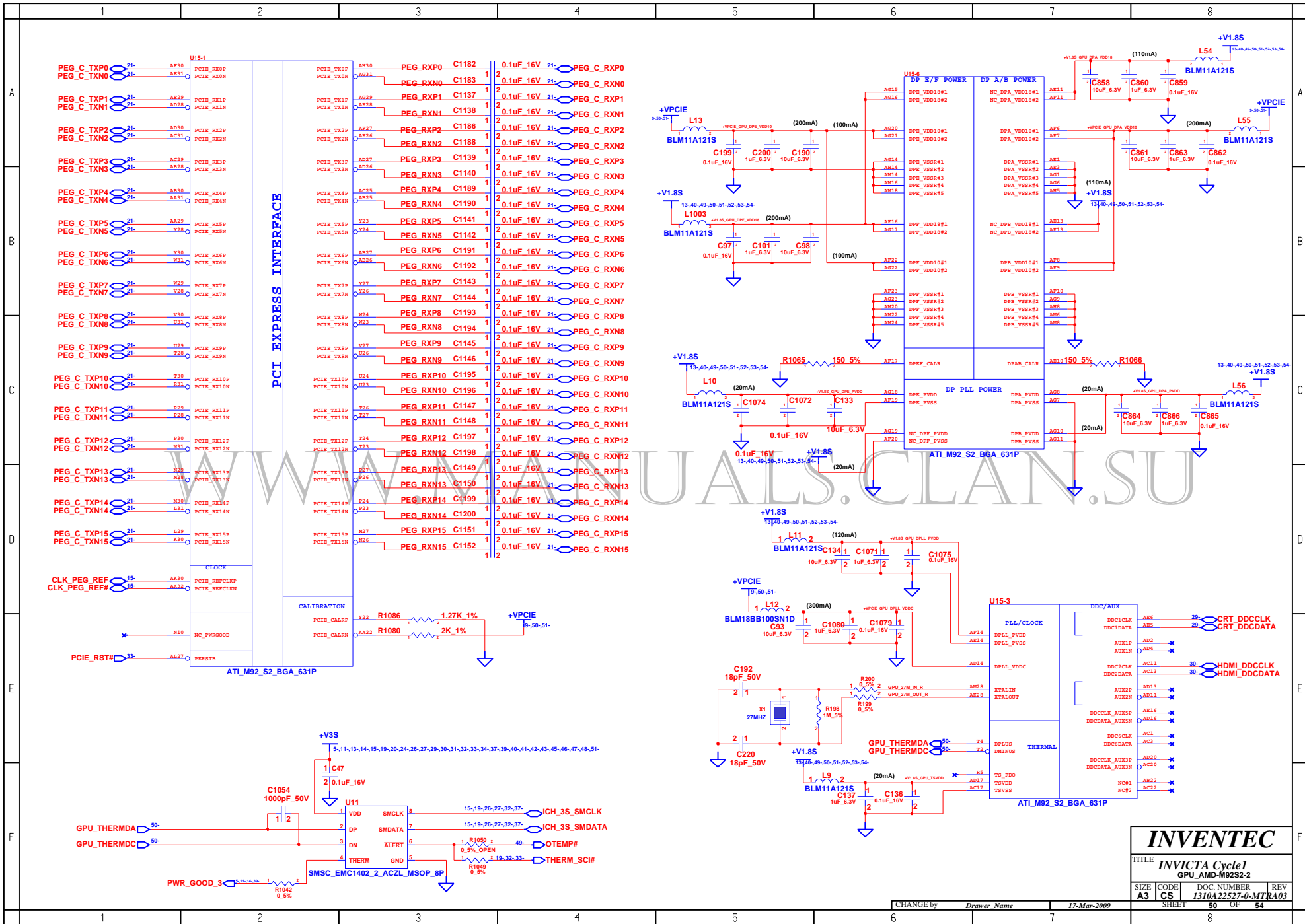


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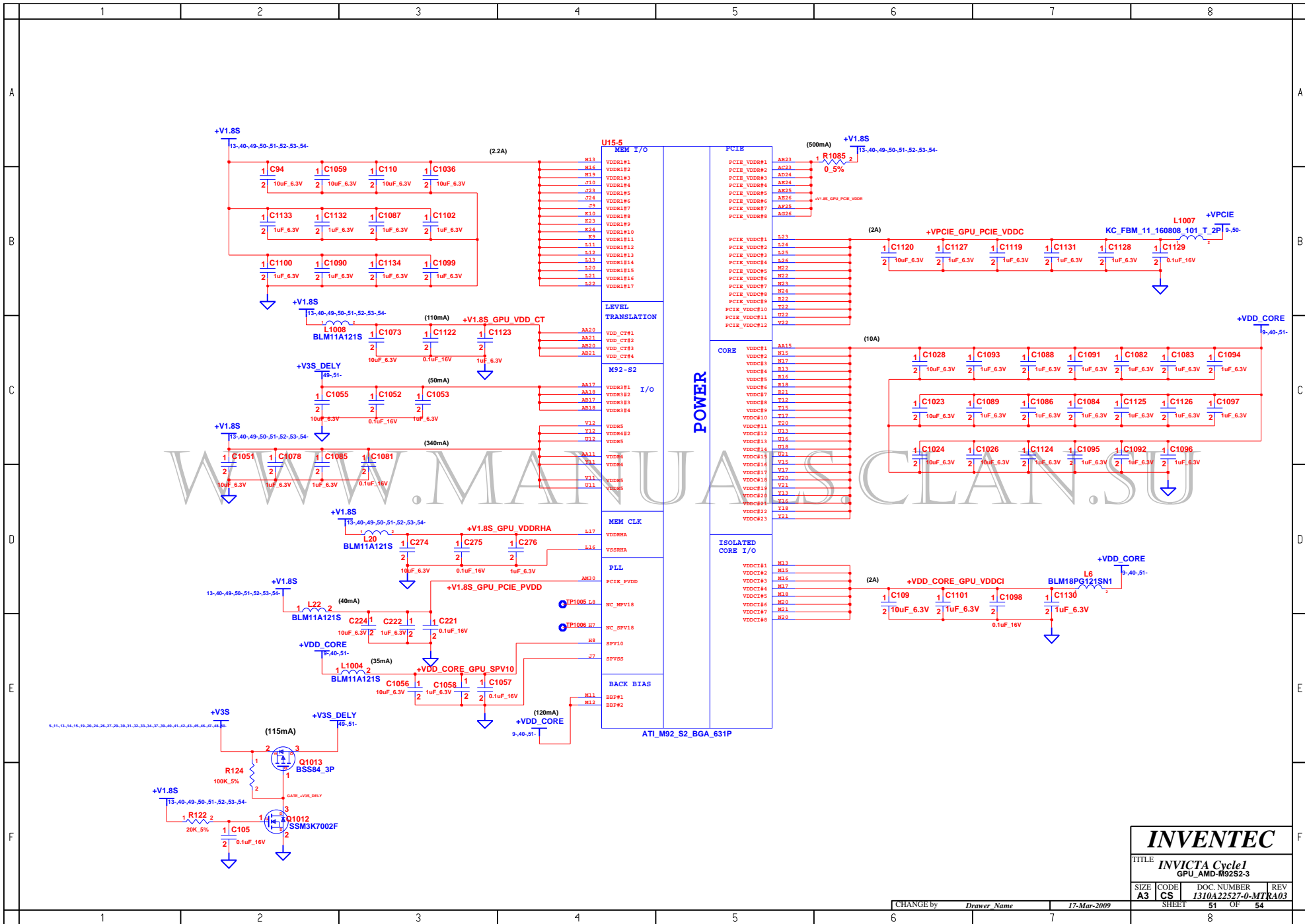
TITLE: INVICTA Cycle1 GPU_AMD-M92S2-1

SIZE: A3, CODE: CS, DOC. NUMBER: I310A22527-0-MTR A03, REV: 1

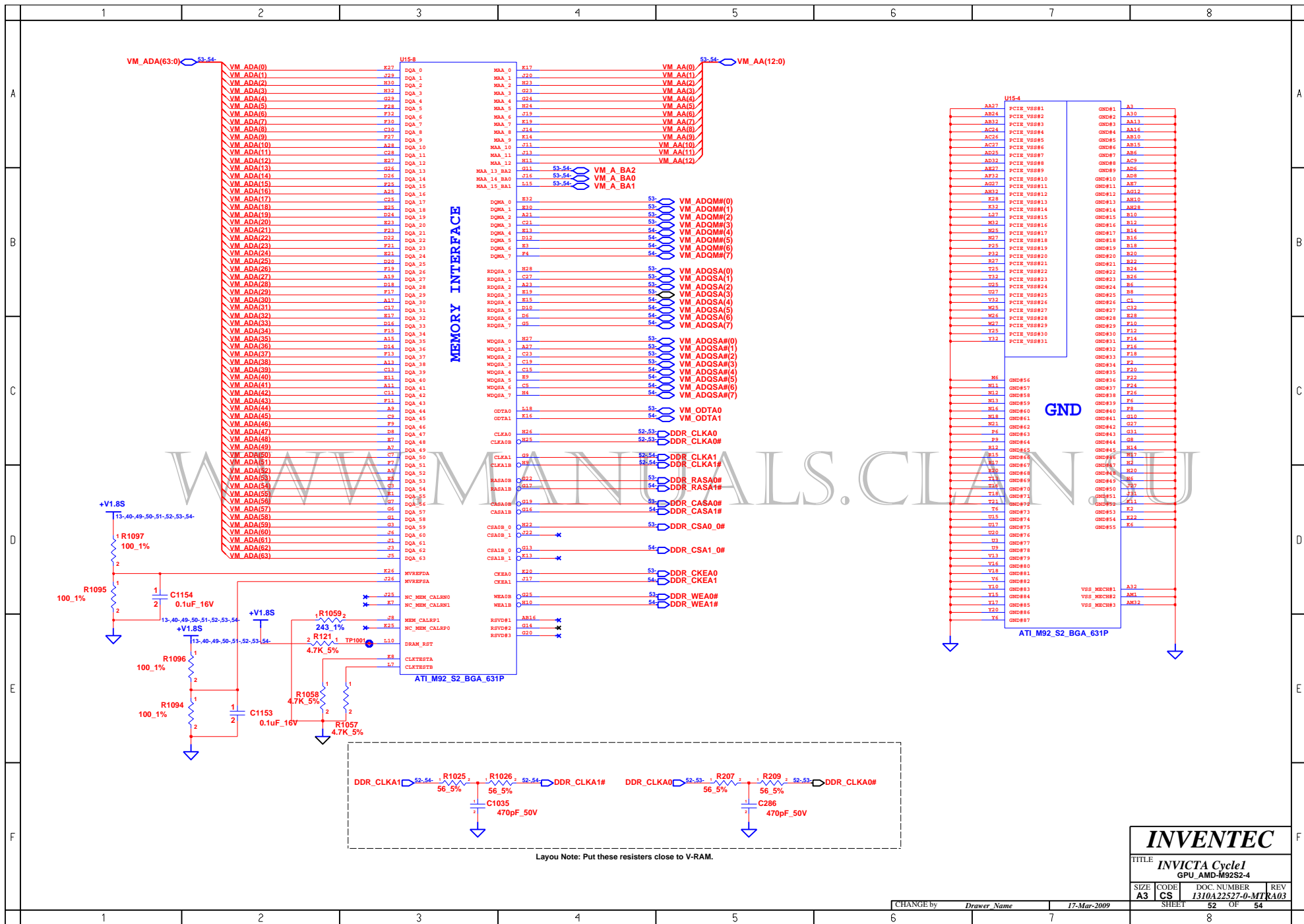
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| | | | |
|---|-------------------|---------------------------------------|-------------------|
| INVENTEC | | | |
| TITLE INVICTA Cycle1 GPU_AMD-M92S2-2 | | | |
| SIZE A3 | CODE CS | DOC NUMBER I310A22527-0-MTR | REV A03 |
| CHANGE by <i>Drawer Name</i> | | 17-Mar-2009 | |
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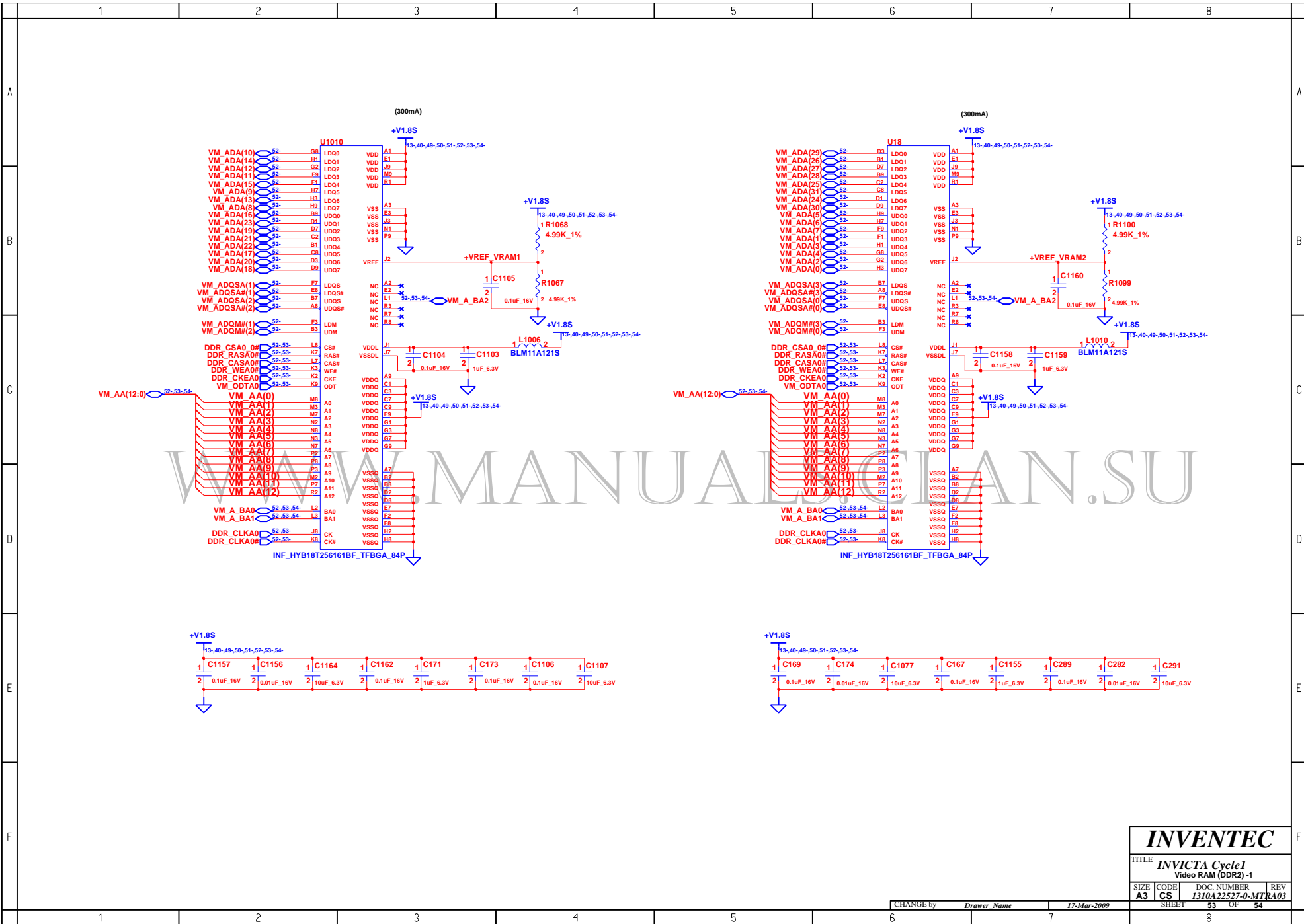


| | | | |
|---------------------------------------|----------|-------------------------------|----------|
| INVENTEC | | | |
| TITLE: INVICTA Cycle1 GPU_AMD-M92S2-3 | | | |
| SIZE: A3 | CODE: CS | DOC. NUMBER: I310A22527-0-MTR | REV: A03 |
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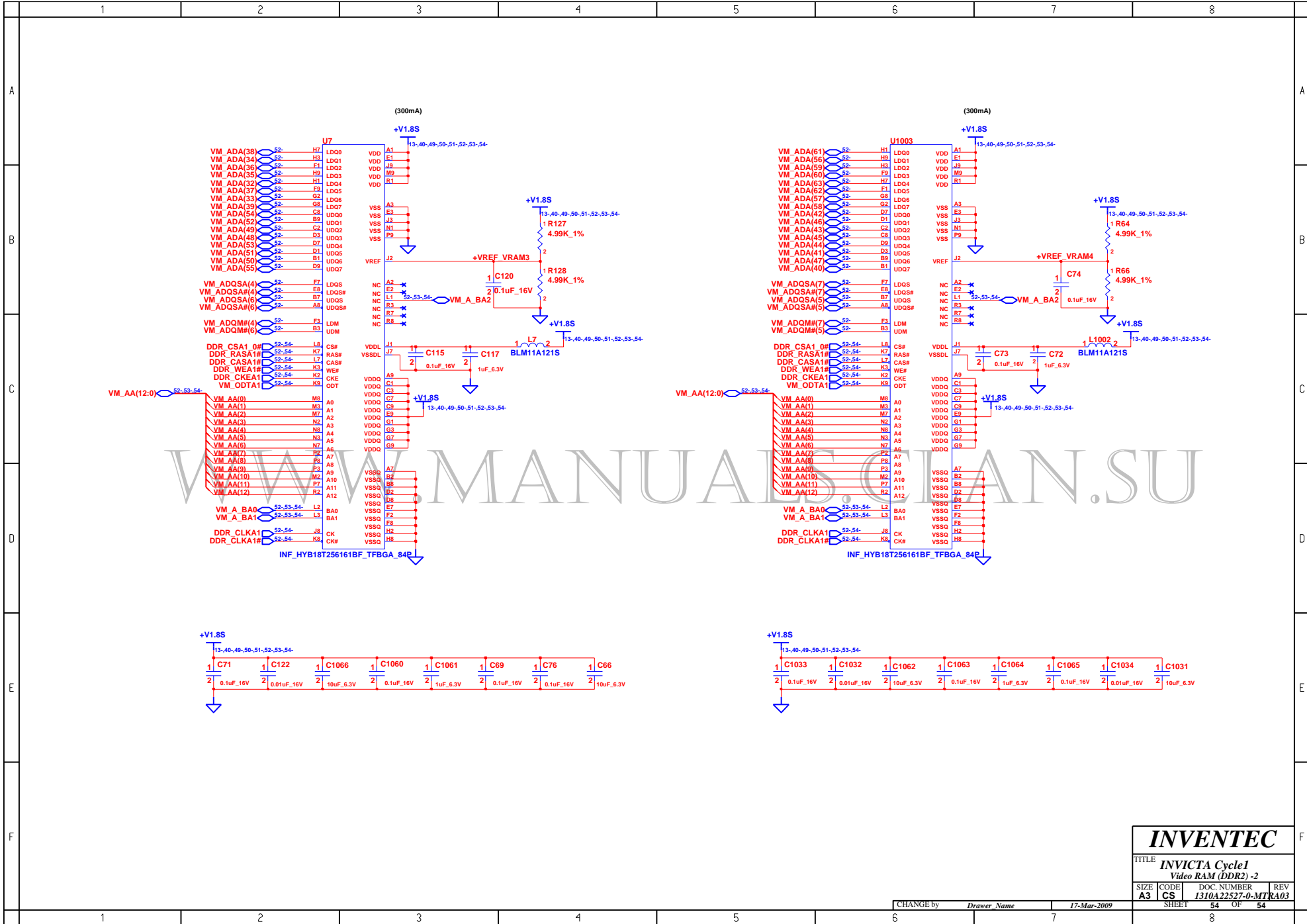
Layout Note: Put these resistors close to V-RAM.

| | | | |
|--|------|-----------------|-------|
| INVENTEC | | | |
| TITLE: INVICTA Cycle1 GPU_AMD-M92S2-4 | | | |
| SIZE | CODE | DOC. NUMBER | REV |
| A3 | CS | 1310A22527-0-MT | A03 |
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|--|------------|---------------------------------|------------|
| INVENTEC | | | |
| TITLE: INVICTA Cycle1 Video RAM (DDR2) -1 | | | |
| SIZE A3 | CODE CS | DOC. NUMBER I310A22527-0-MTR | REV A03 |
| CHANGE by: Drawer Name | | 17-Mar-2009 | |
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INVENTEC

TITLE *INVICTA Cycle1*
Video RAM (DDR2) -2

| SIZE | CODE | DOC. NUMBER | REV |
|------|------|------------------|-----|
| A3 | CS | I310A22527-0-MTR | A03 |

CHANGE by *Drawer Name* 17-Mar-2009

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