Compal Confidential

PAWGC/D Schematics Document

AMD APU Ontario-FT1 + FCH Hudson-M1 + GPU Roberson XT

2010-11-10

REV:1.0

CIT RD Only

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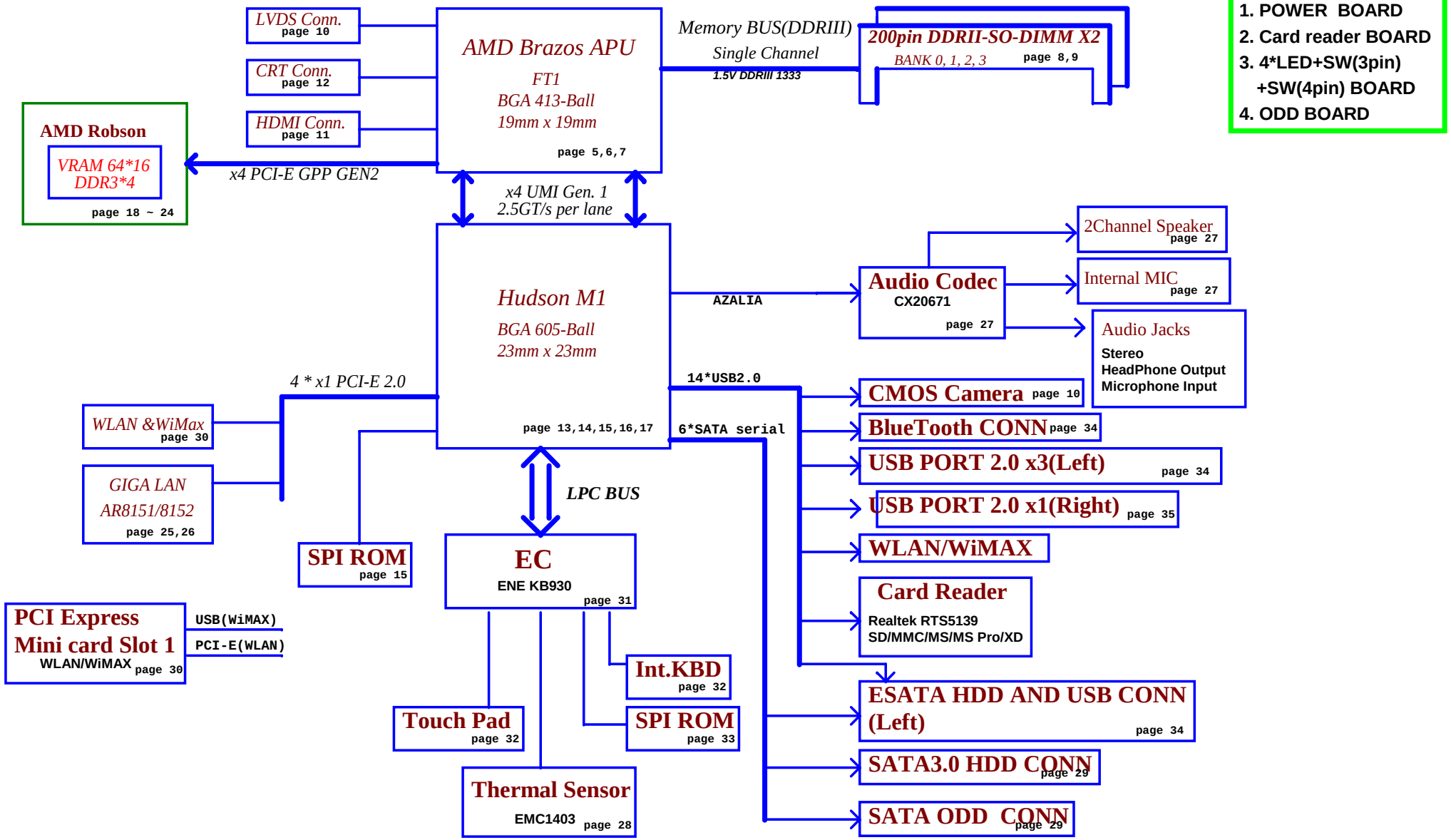
Compal confidential
File Name : PAWGC/D

For PAWGC
1. POWER BOARD
2. Card Reader BOARD

For PAWGD
1. POWER BOARD
2. Card reader BOARD
3. 4*LED+SW(3pin) +SW(4pin) BOARD
4. ODD BOARD



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Title	Block Diagrams		
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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+APU_CORE	Core voltage for CPU (0.7-1.2V)	ON	OFF	OFF
+APU_CORE_NB	1.0V switched power rail	ON	OFF	OFF
+1.5V	1.5V power rail for CPU VDDIO and DDRIII	ON	ON	OFF
+0.75VS	0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.0VS	1.0V switched power rail for NB VDDC & VGA	ON	OFF	OFF
+1.1VS	1.1VS switched power rail	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V_LAN	3.3V power rail for LAN	ON	ON(WOL)	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON
+1.1VALW	1.1V always on power rail	ON	ON	ON*

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

EC SM Bus1 address

Device	Address	HEX
Smart Battery	0001-011xb	15H

EC SM Bus2 address

Device	Address	HEX
EMC1412-2 (dGPU)	1111-100xb	F8H
EMC1403-2(DDR,WLAN)	1001-101xb	9AH
SB-TSI	1001-100xb	98H

SM Bus Controller 0

(FCH_SMB1 ~ FCH_SMB4, SMB_ALERT#)

Device	Address	HEX
APU SIC/SID (FCH_SMB3)		
H_THERMTRIP# (FCH_ALERT#)		

SM Bus Controller 1

(FCH_SMB0)

Device	Address	HEX
DDR DIMM1 (FCH_SMB0)	1001-000xb	90
DDR DIMM2 (FCH_SMB0)	1001-001xb	92
WLAN (FCH_SMB0)		

FCH Hudson-M1 USB Port List

USB1.1	
Port0	NC
Port1	NC
USB2.0	
Port0	Left USB1
Port1	USB Camera
Port2	Left(Combo)
Port3	Left USB2
Port4	Right USB
Port5	BT
Port6	CardReader
Port7	Mini-PCIE
Port8	NC
Port9	NC
Port10	NC
Port11	NC
Port12	NC
Port13	NC

Brazos PCIE Port List

APU	PCIE0	GPU PCIE x4
	PCIE1	
	PCIE2	
	PCIE3	
FCH	PCIE0	LAN
	PCIE1	WLAN
	PCIE2	NC
	PCIE3	NC

FCH Hudson-M1 SATA Port List

SATA0	HDD
SATA1	ODD
SATA2	eSATA
SATA3	NC
SATA4	NC
SATA5	NC

BOM Structure

```
UMA@  : UMA only
PX@   : DIS muxluss
            - PX3@  : PX3.0 only
            - BACO@ : Baco only

GIGA@ : AR8151
8152@ : AR8152
CMOS@ : USB camera
HDMI@ : HDMI function
nonHDMI@ : w/o HDMI function
ESATA@: eSATA function
BT@   : BT function
ME@   : ME components
X76@, H1G@, H512@, S1G@, S512@  : VRAM
45@   : 45 Level
HWM@  : hardware monitor function
nonHWM@: w/o hardware monitor function
```

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Power-Up/Down Sequence

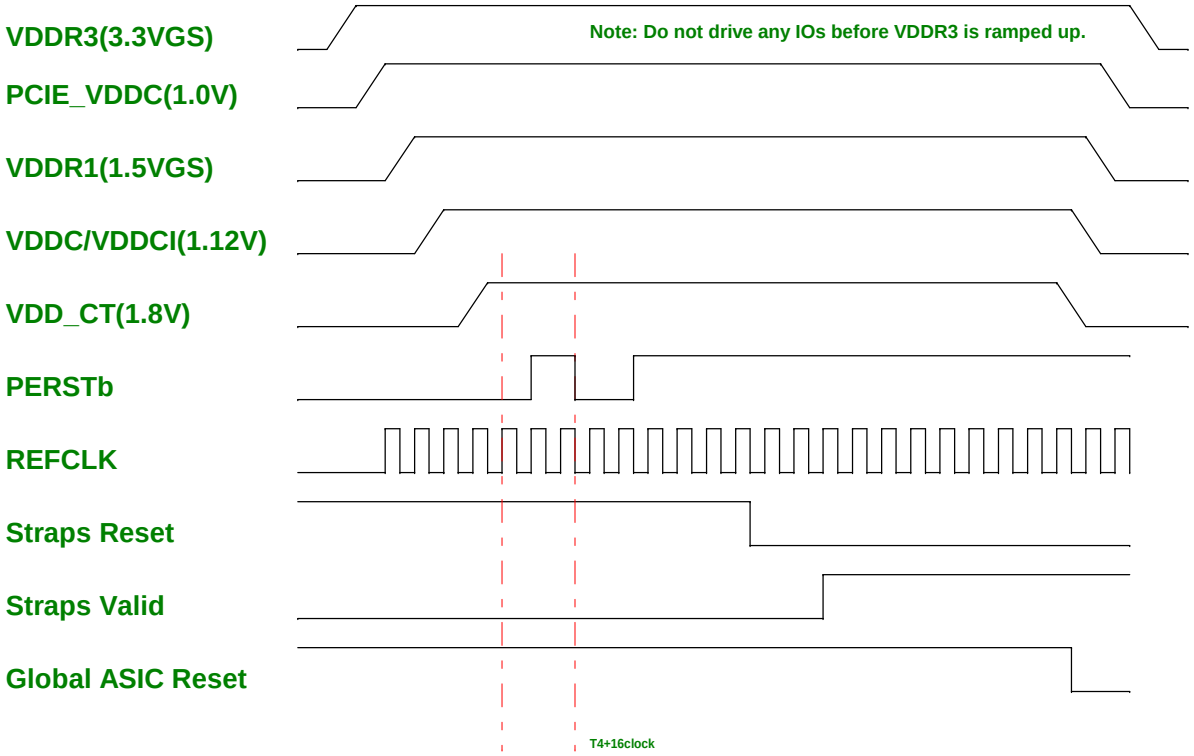
1. All the ASIC supplies must fully reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred.

2. VDDR3 should ramp-up before or simultaneously with VDDC.

3. For LVDS, DPx_VDD10 should ramp-up before DPx_VDD18 and the PCIe Reference clock should begin before DPx_VDD18. For power-down, DPx_VDD18 should ramp-down before DPx_VDD10.

4. The external pull-ups on the DDC/AUX signals (if applicable) should ramp-up before or after both VDDC and VDD_CT have ramped up.

5.VDDC and VDD_CT should not ramp-up simultaneously. (e.g., VDDC should reach 90% before VDD_CT starts to ramp-up (or vice versa).)



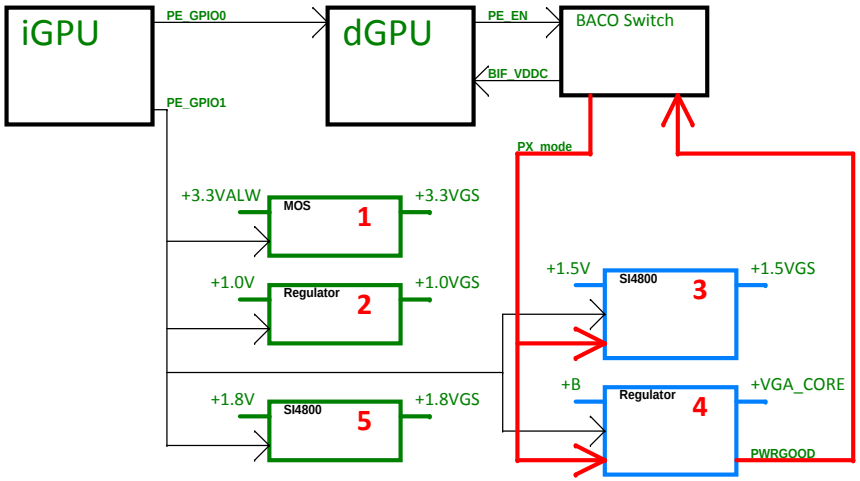
Without BACO option :

PE_GPIO0 : Low -> Reset dGPU ; High ->Normal operation
PE_GPIO1 : Low -> dGPU Power OFF ; High -> dGPU Power ON

BACO option :

PE_GPIO0 : High ->Normal operation (dGPU is not reset on BACO mode)
PE_GPIO1 : Low -> dGPU Power OFF ; High -> dGPU Power ON (always High)

dGPU Power Pins	Voltage	PX 3.0	BACO Mode	Max current
PCIE_PVDD, PCIE_VDDR, TSVDD, VDDR4, VDD_CT, DPE_PVDD, DP[F:E]_VDD18, DP[D:A]_PVDD, DP[D:A]_VDD18, AVDD, VDD1DI, A2VDDQ, VDD2DI, DPLL_PVDD, MPV18, and SPV18	1.8V	OFF	ON	1679mA
DP[F:E]_VDD10, DP[D:A]_VDD10, DPLL_VDDC, and SPV10	1.0V	OFF	ON	575mA
PCIE_VDDC	1.0V	OFF	ON	2A
VDDR3 , and A2VDD	3.3V	OFF	ON	190mA
BIF_VDDC (current consumption = 55mA@1.0V, in BACO mode)	Same as VDDC	OFF	ON Same as PCIE_VDDC	70mA
VDDR1	1.5V	OFF	OFF	2.8A
VDDC/VDDCI	1.12V	OFF	OFF	12.9A



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Title: dGPU Block Diagram

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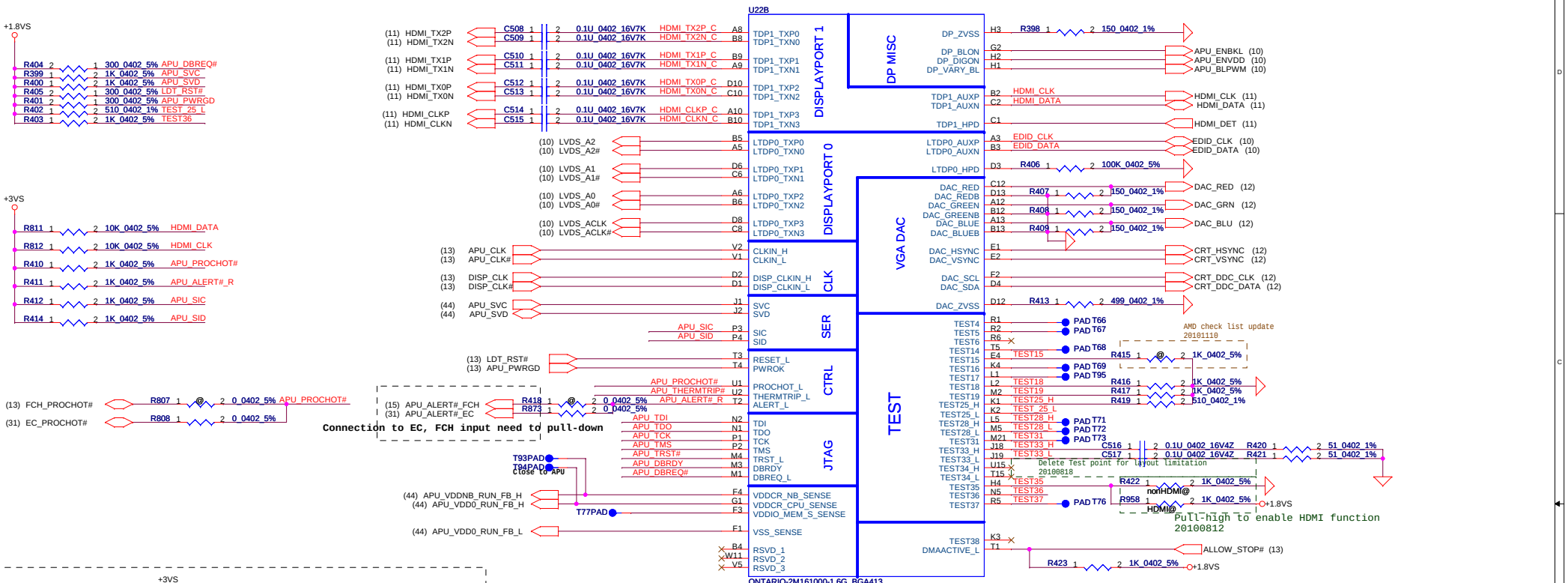

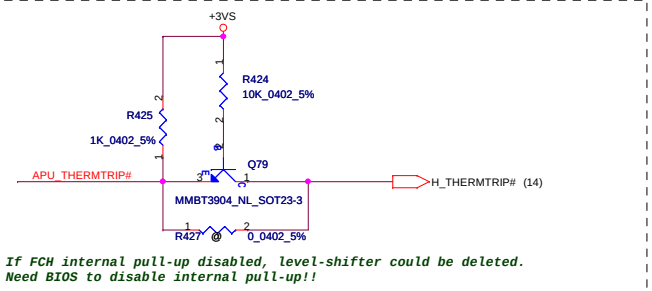

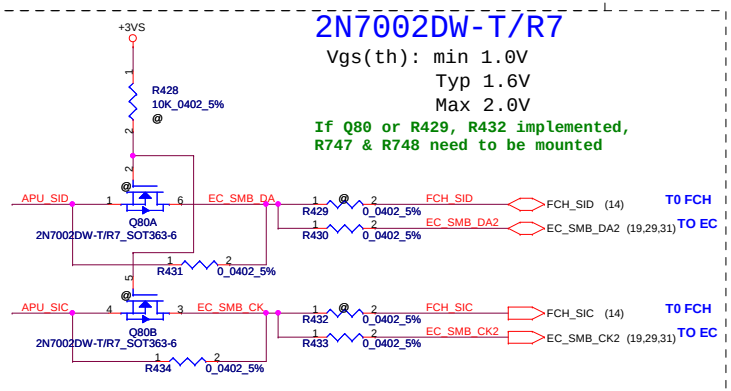

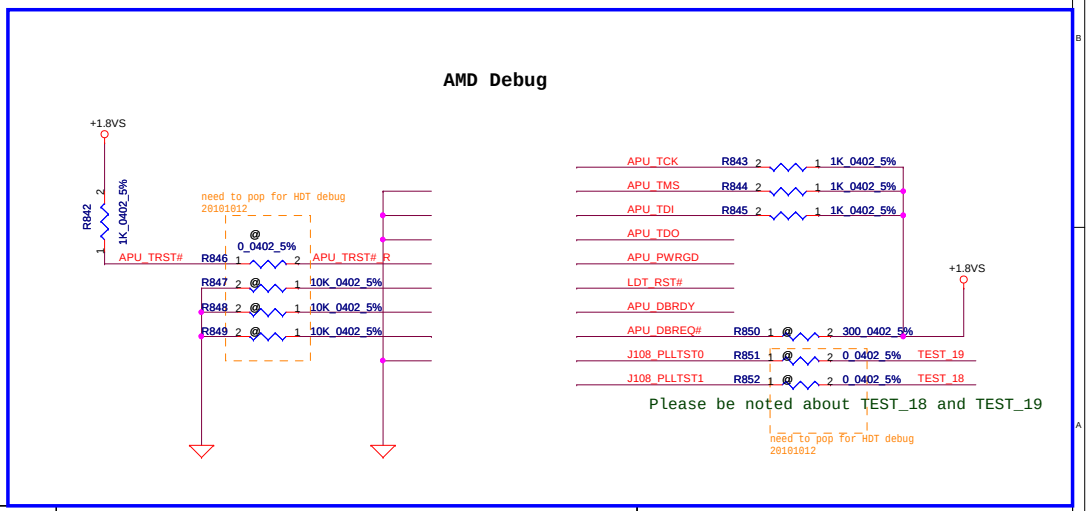

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Title	FT1 CTRL/DP/CRT	
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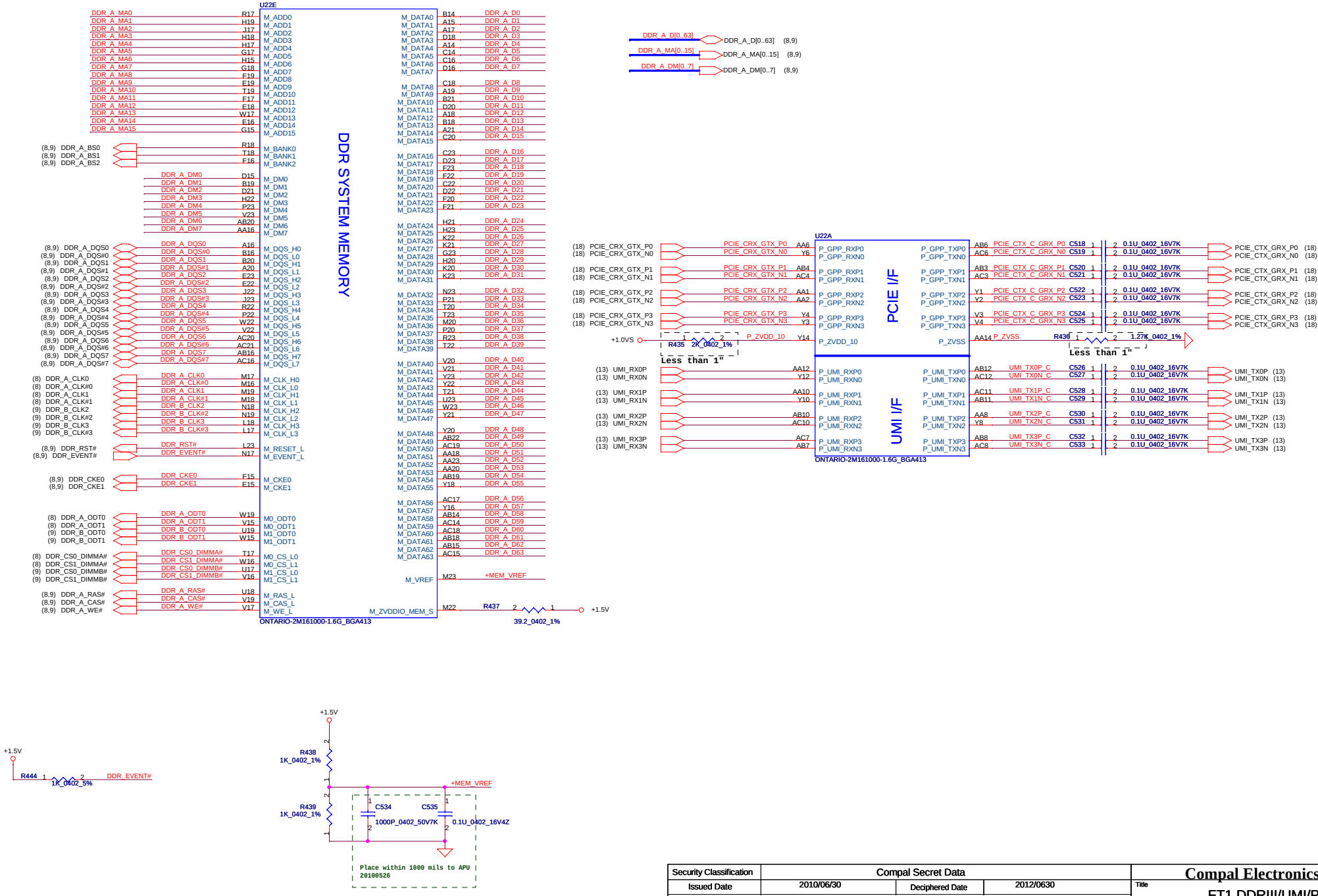

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Title: FT1 DDRIII/UMI/PCIE

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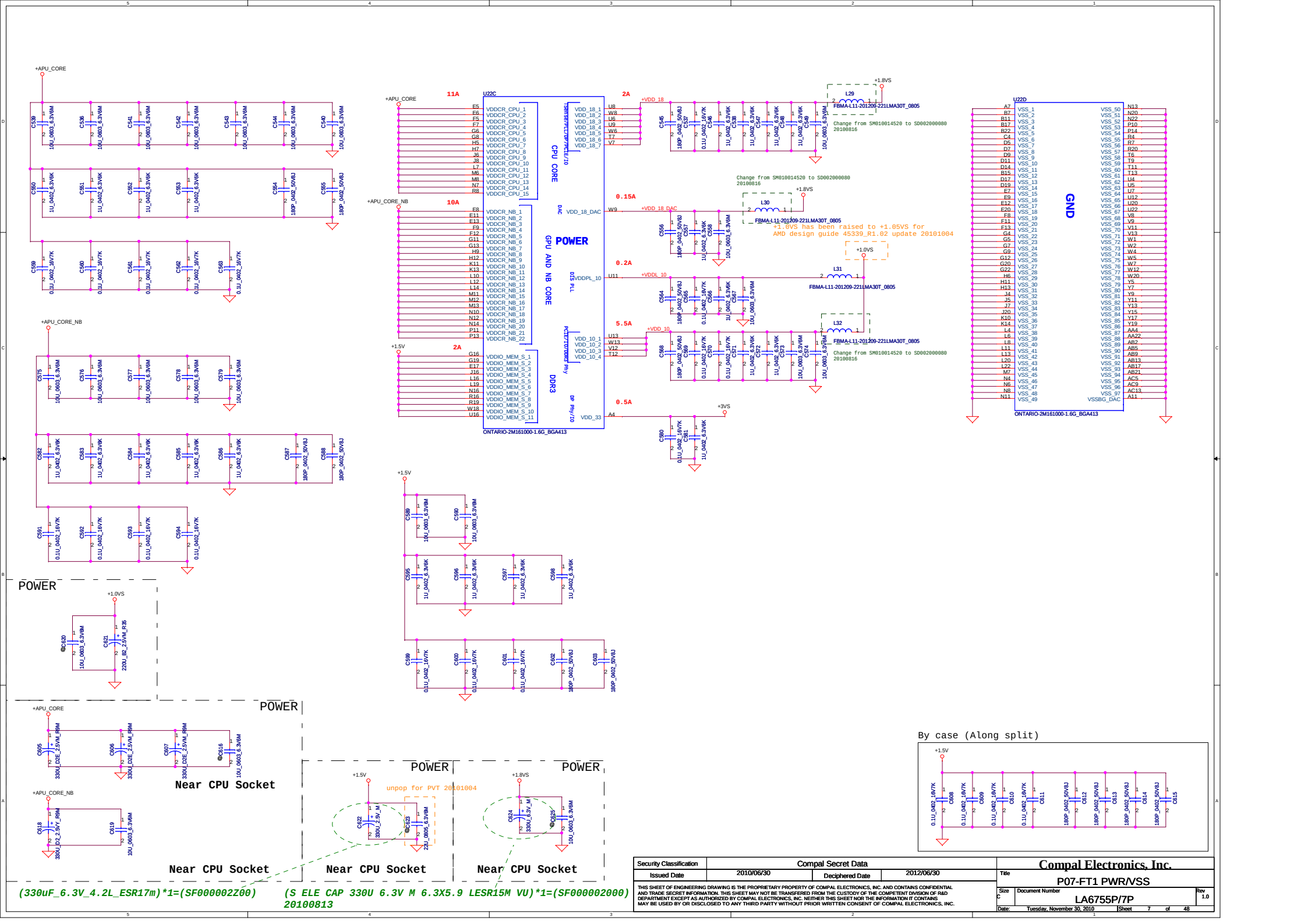

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Title: P07-FT1 PWR/VSS

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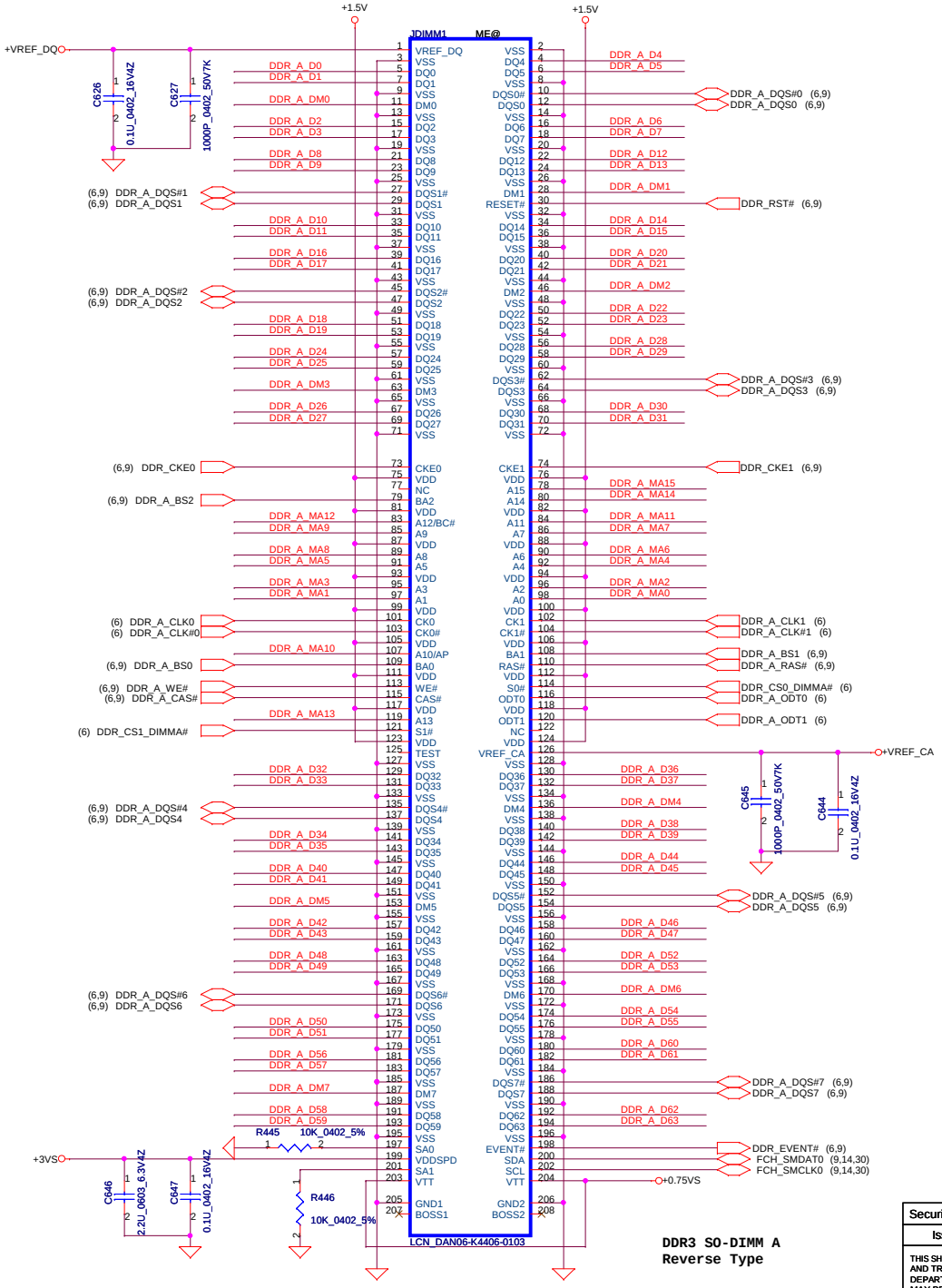
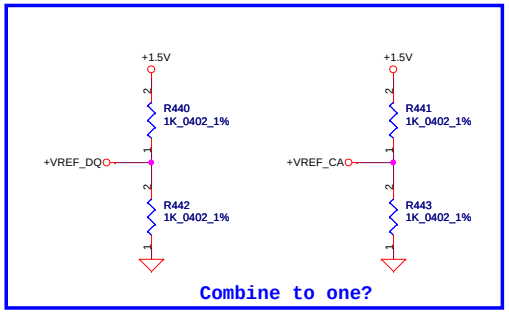
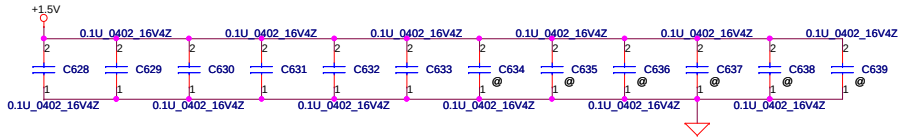
(330uF_6.3V_4.2L_ESR17m)*1=(SF000002Z00)

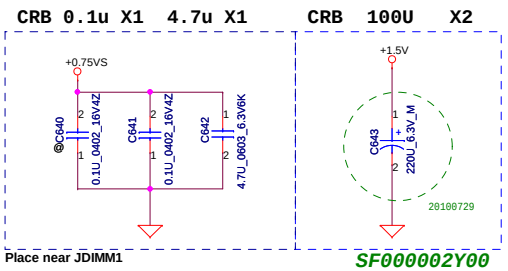
(S ELE CAP 330U 6.3V M 6.3X5.9 LESR15M VU)*1=(SF000002000) 20100813



DDR3 SO-DIMM A
Reverse Type







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Title: DDR3 SODIMM-I Socket

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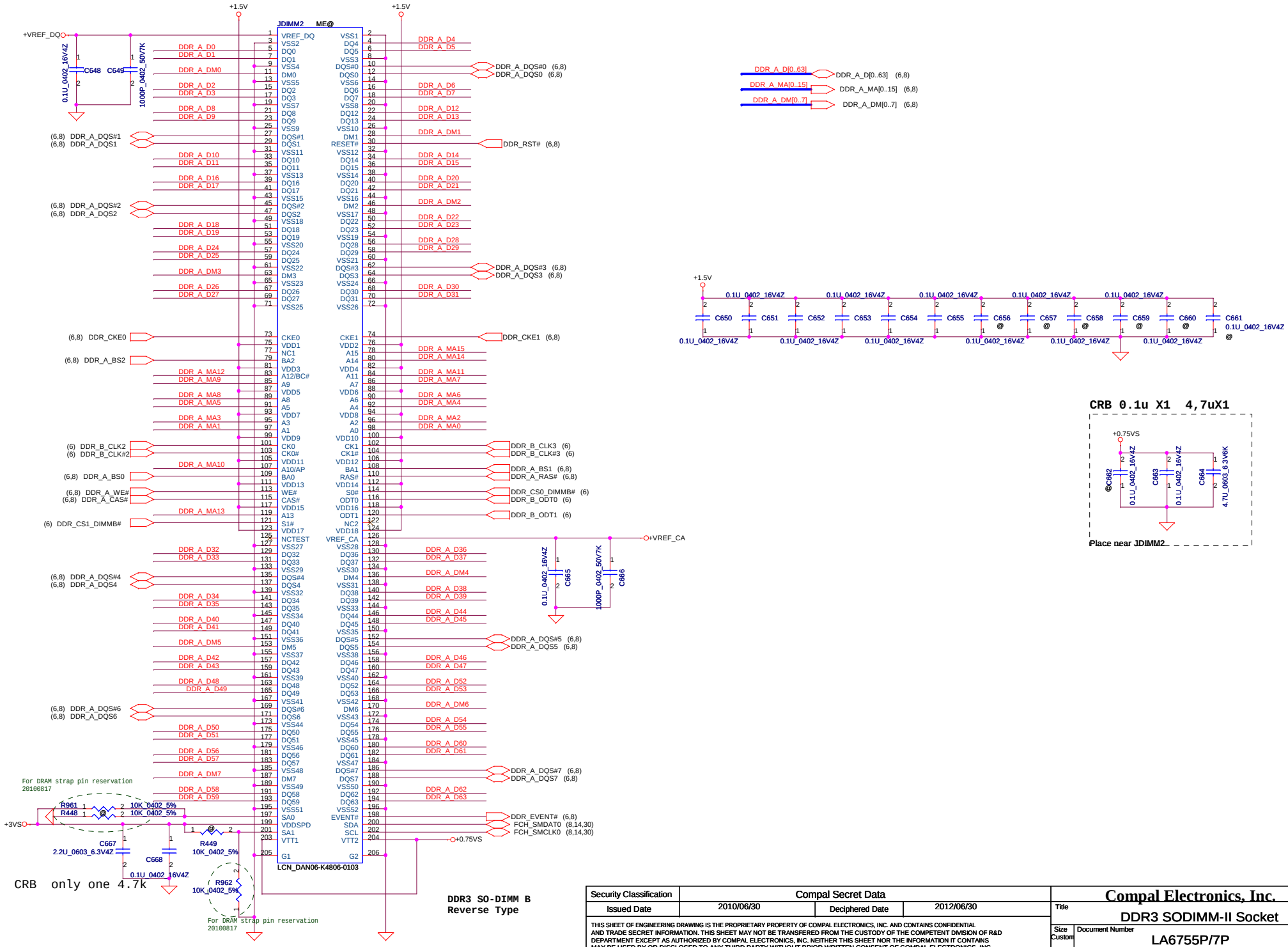

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Title: DDR3 SODIMM-II Socket

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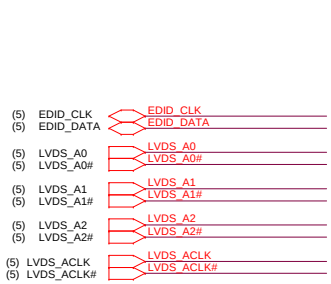
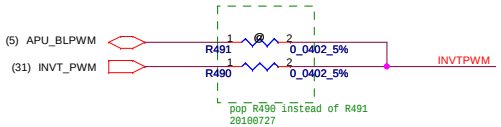
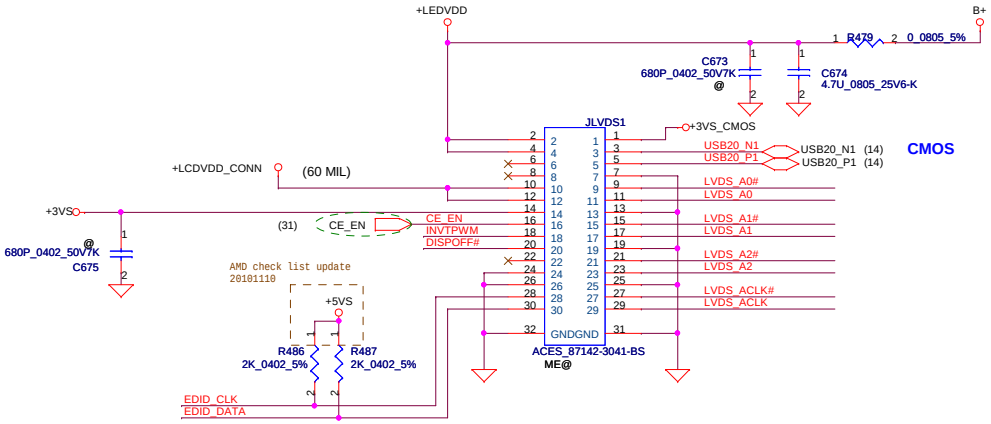
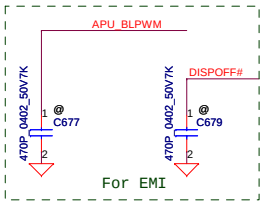
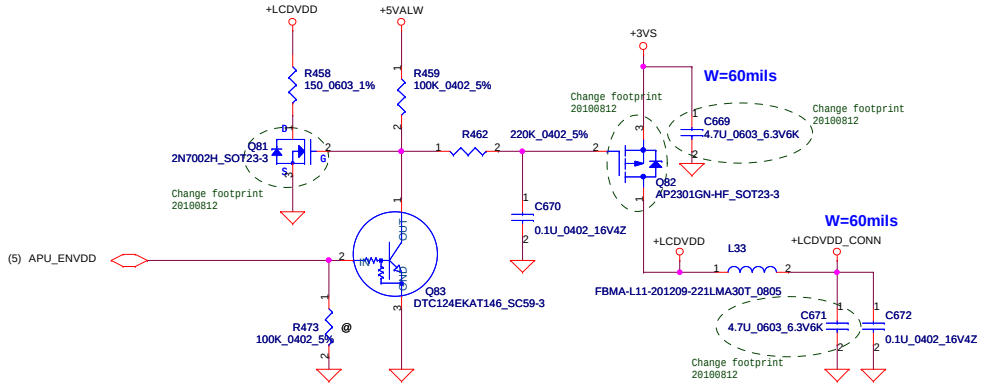
LCD POWER CIRCUIT

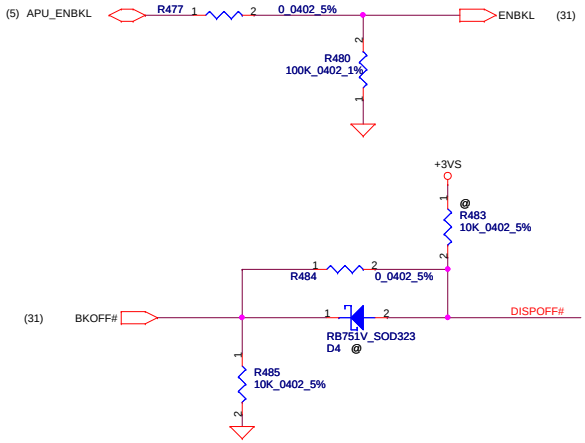




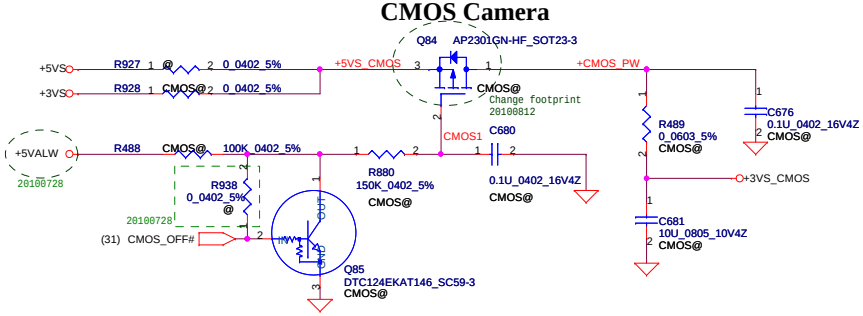








CMOS Camera



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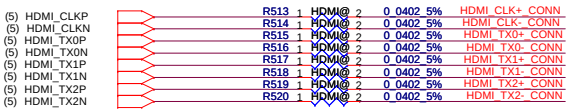

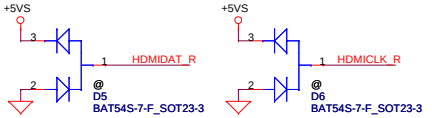

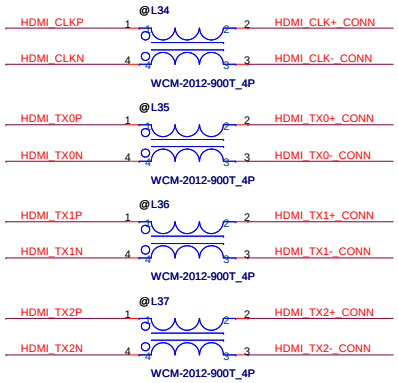

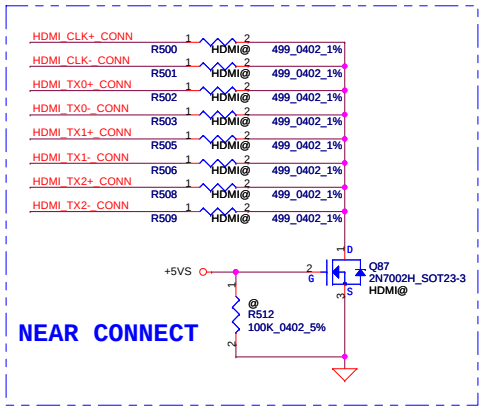

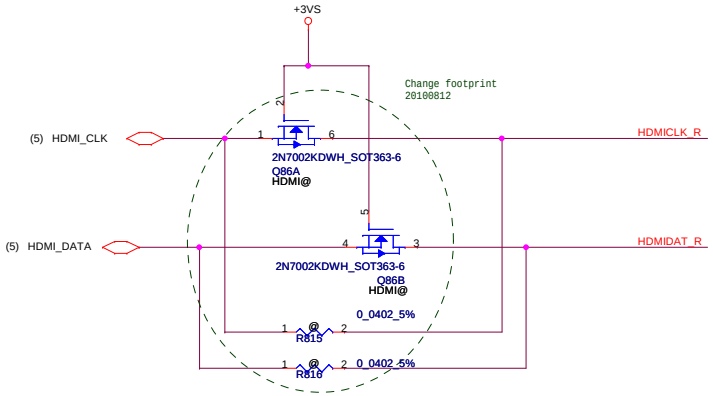

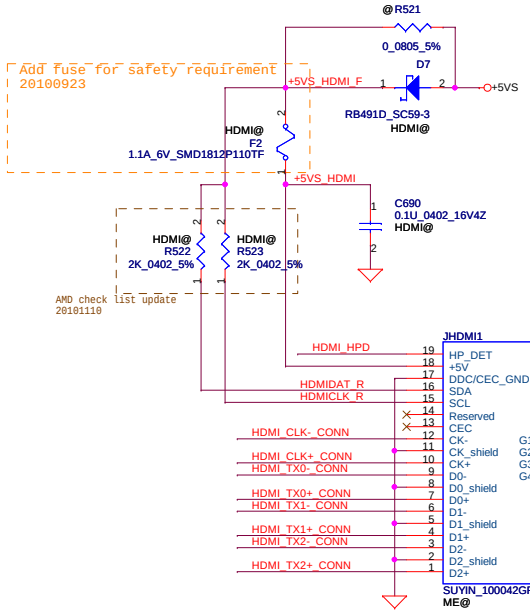

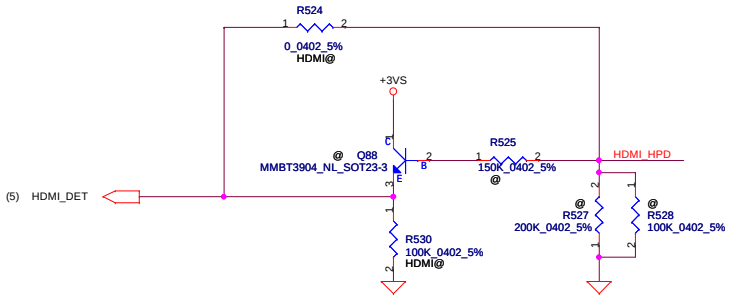

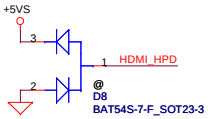

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Compal Electronics, Inc.

Title: HDMI Connector

Size	Document Number	Rev
Custom	LA6755P/7P	1.0

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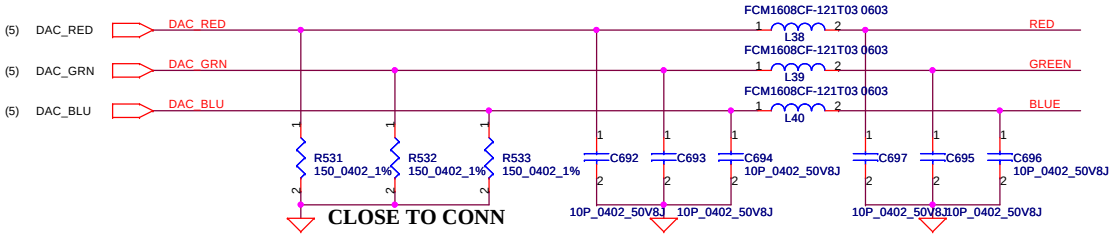

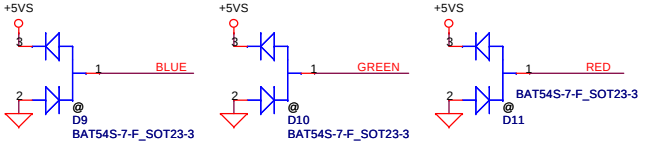

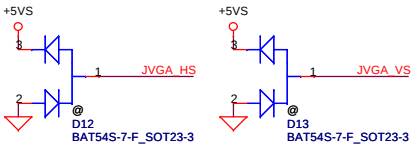

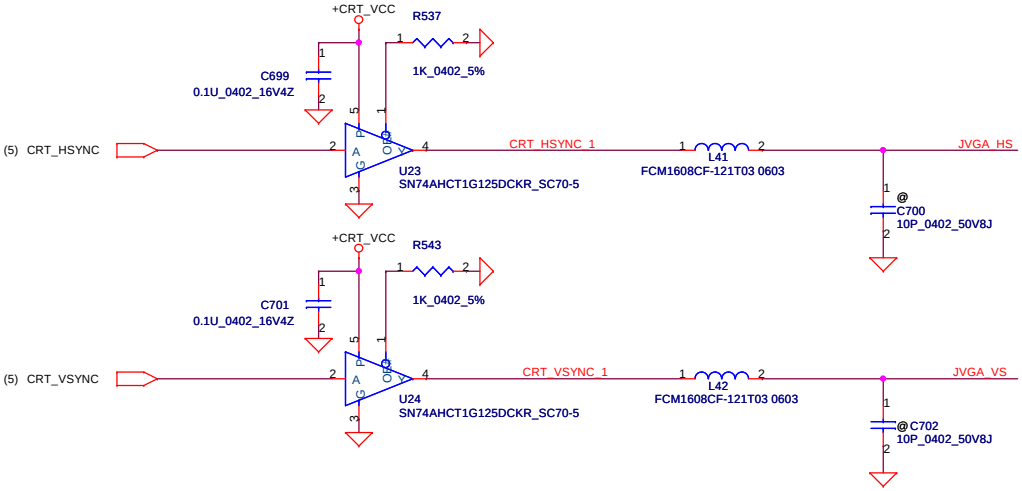

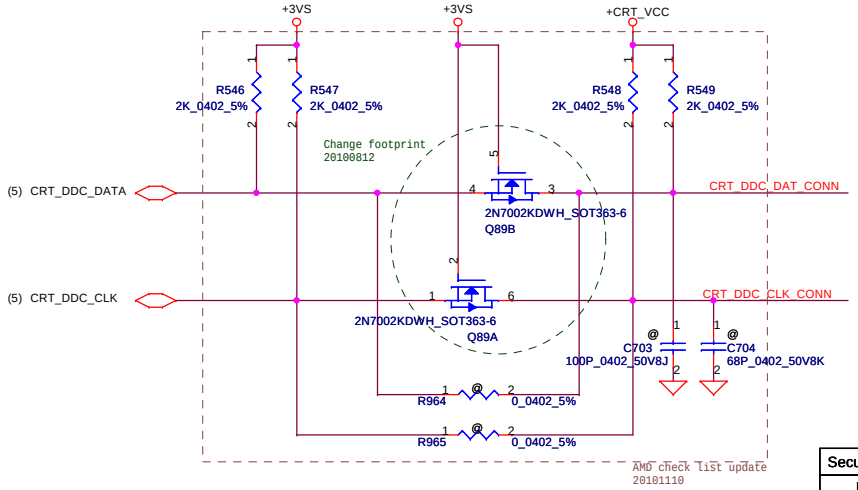

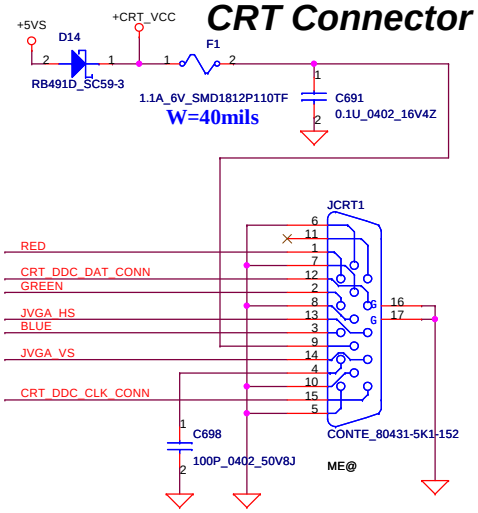

CRT Connector

Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2012/06/30

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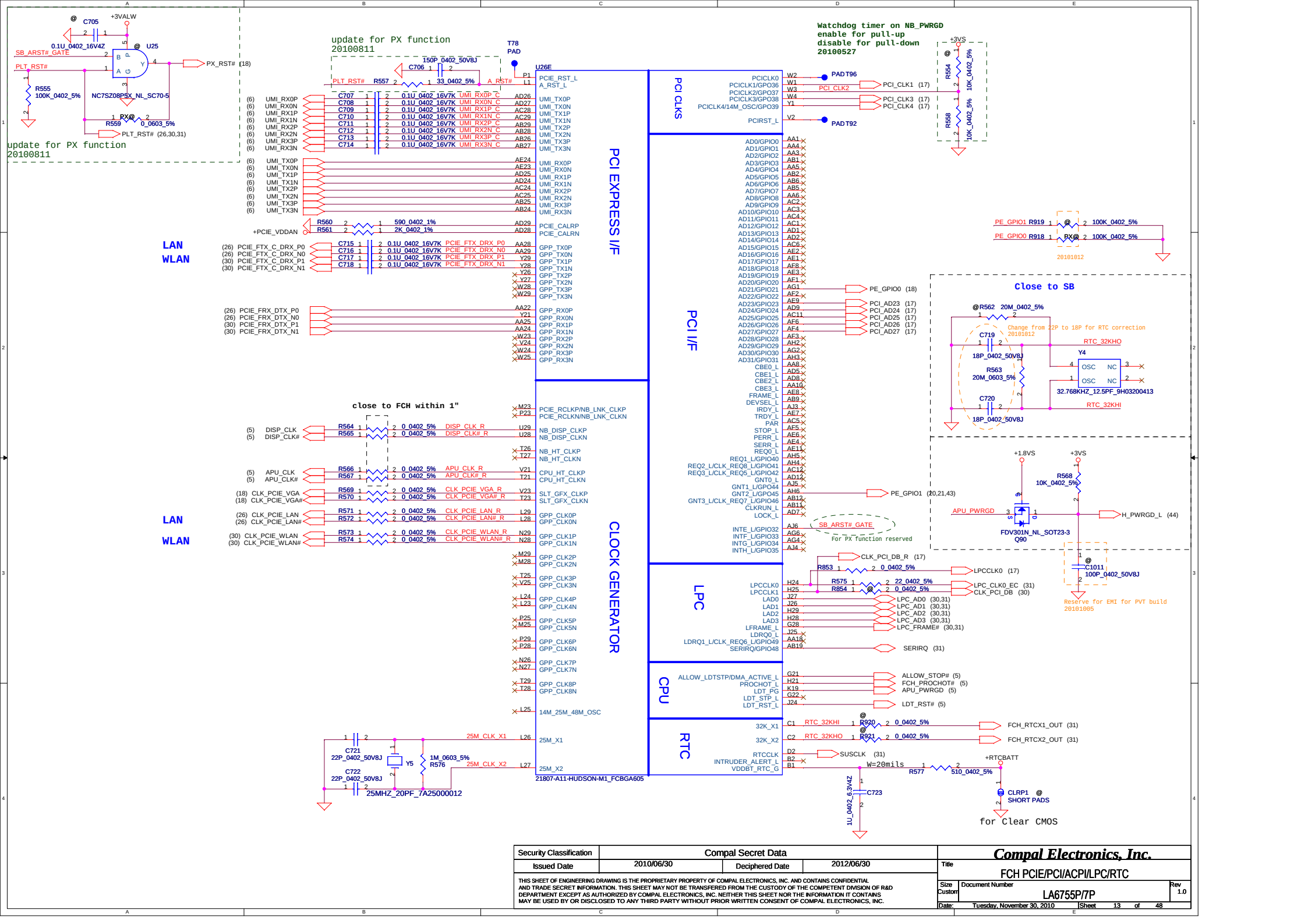
Compal Electronics, Inc.

Title: CRT Connector

Size: Custom | Document Number: LA6755P/7P | Rev: 1.0

Date: Tuesday, November 30, 2010 | Sheet 12 of 48



Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2012/06/30

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Compal Electronics, Inc.

Title: FCH PCIE/PCI/ACPI/LPC/RTC

Size	Document Number	Rev
Custom	LA6755P/7P	1.0

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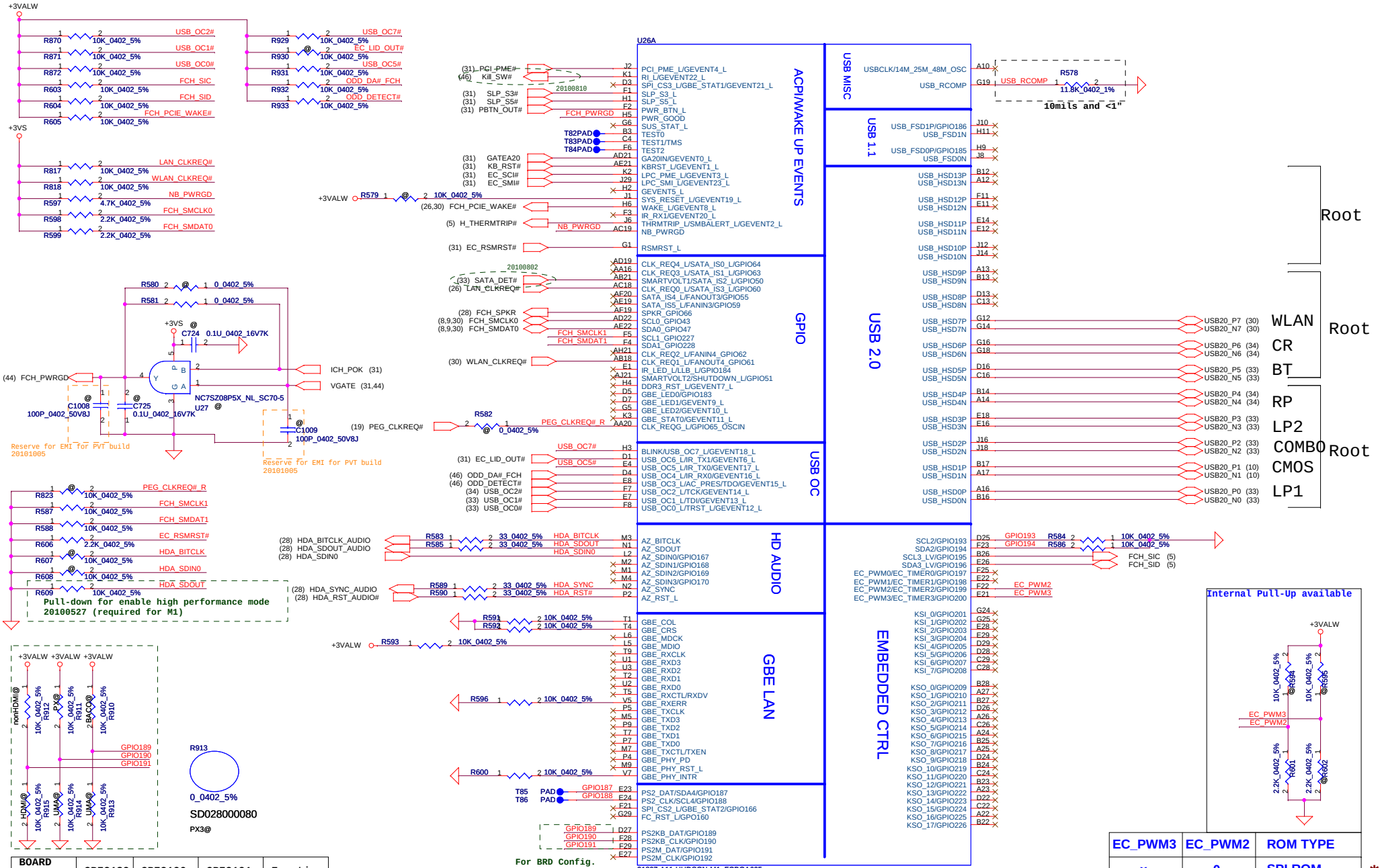

EC_PWM3	EC_PWM2	ROM TYPE
x	0	SPI ROM *
x	x	Reserved
0	0	Reserved
0	x	LPC ROM

BOARD Config.	GPIO189	GPIO190	GPIO191	Function
	0	0	0	UMA
	1	0	0	DIS
	0	1	0	PX3
	1	1	0	PX4
	x	x	1	w/o HDMI

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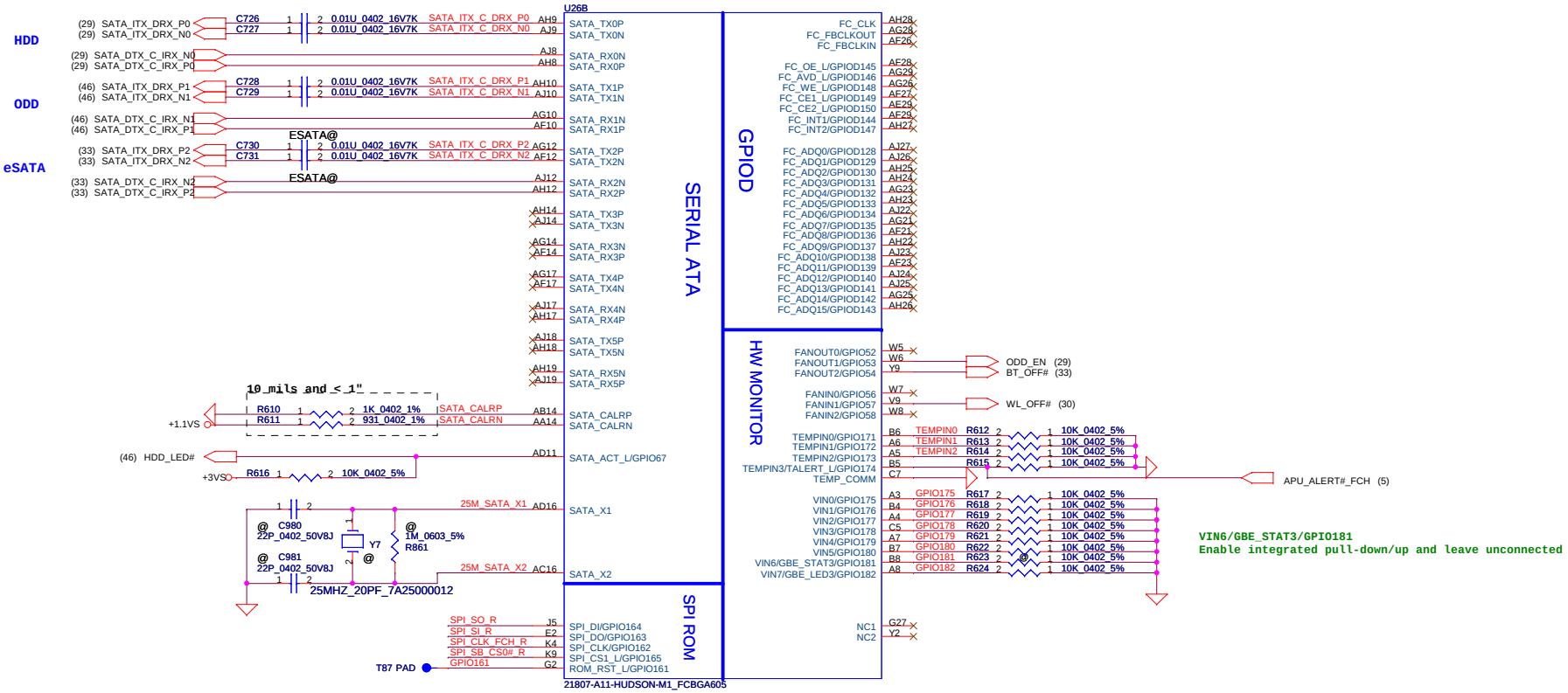
Compal Electronics, Inc.

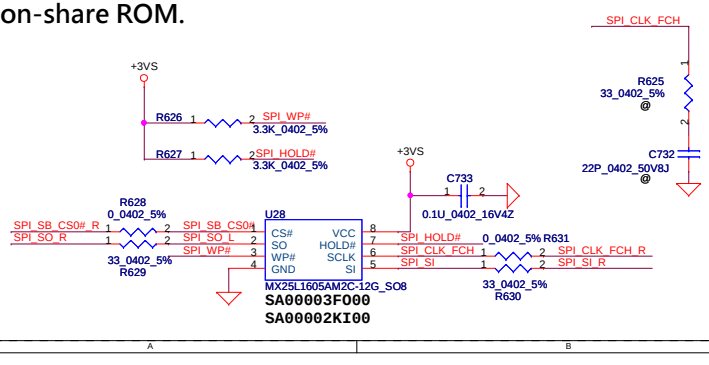
Title: FCH HDA/USB/ACPI

Size: Custom | Document Number: LA6755P/7P | Rev: 1.0

Date: Tuesday, November 30, 2010 | Sheet 14 of 48



2MB SPI ROM
& Non-share ROM.



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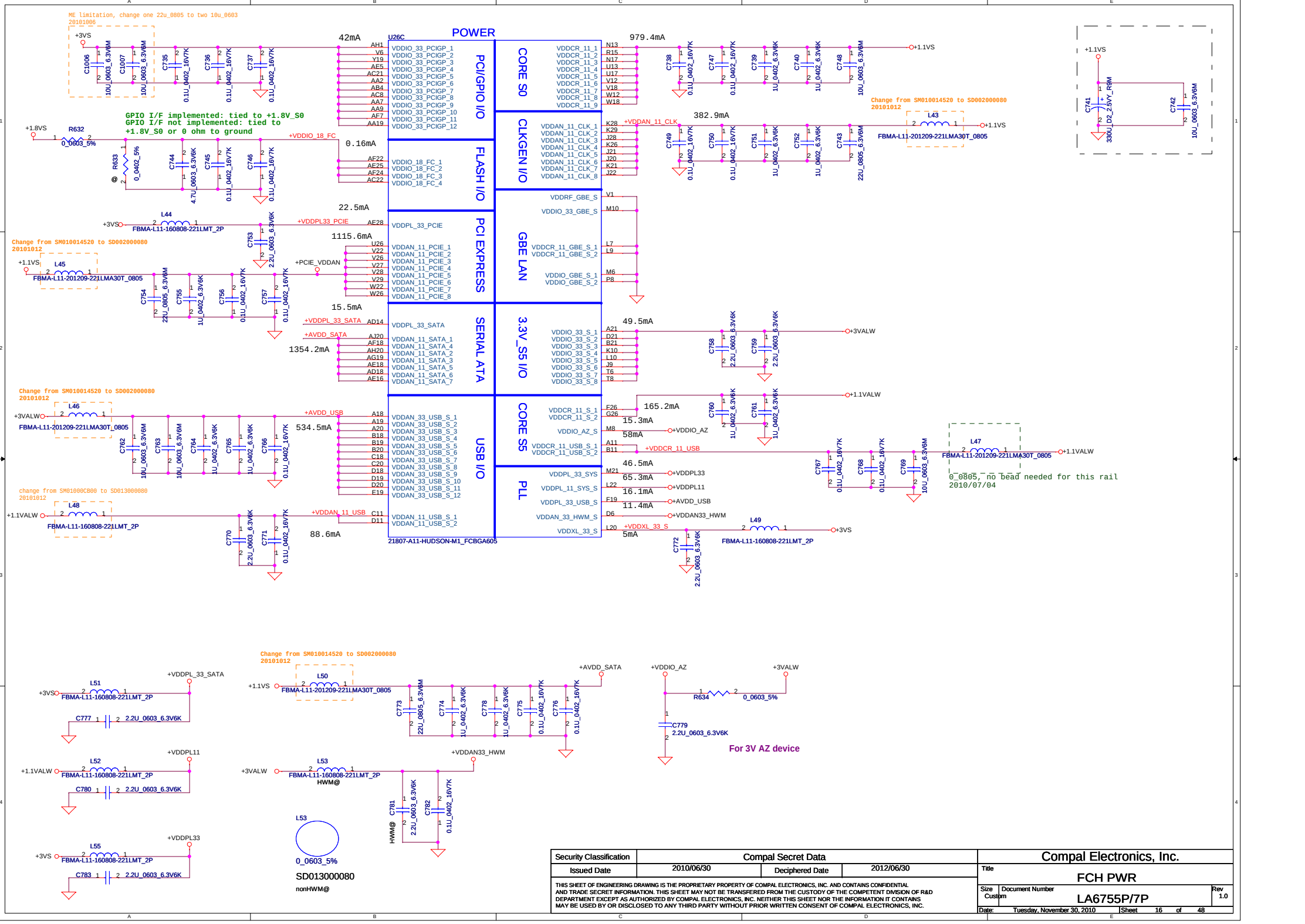
Compal Electronics, Inc.

Title: FCH-SATA/SPI

Size: Custom | Document Number: LA6755P/7P | Rev: 1.0

Date: Tuesday, November 30, 2010 | Sheet 15 of 48



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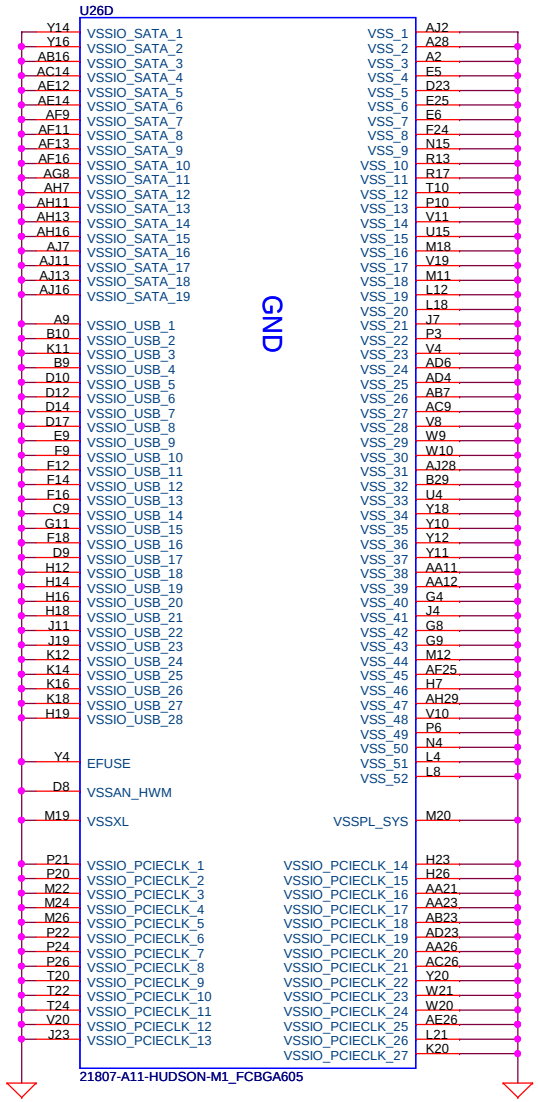
Compal Electronics, Inc.

Title: FCH PWR

Size: Custom | Document Number: LA6755P/7P | Rev: 1.0

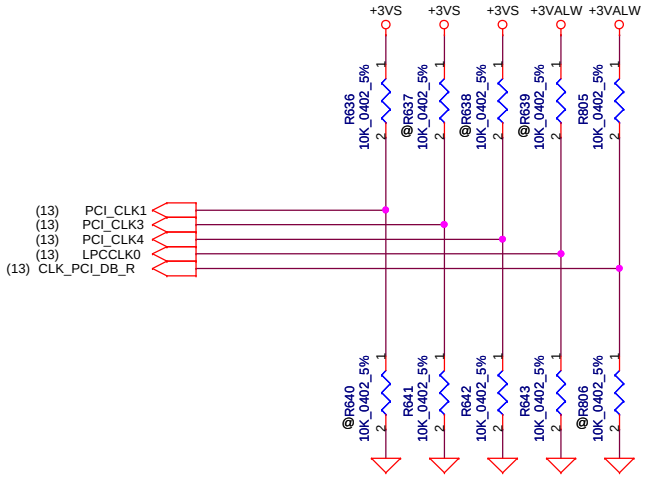
Date: Tuesday, November 30, 2010 | Sheet 16 of 48



REQUIRED STRAPS

Check Internal PU/PD

	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	CLK_PCI_DB				
PULL HIGH	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAP	Reserved	internal EC ENABLE	Internal CLKGEN Mode DEFAULT				
PULL LOW	FORCE PCIE GEN1	IGNORE DEBUG STRAP DEFAULT	CLKGEN Mode Internal DEFAULT	internal EC DISABLE DEFAULT	External CLKGEN Mode				

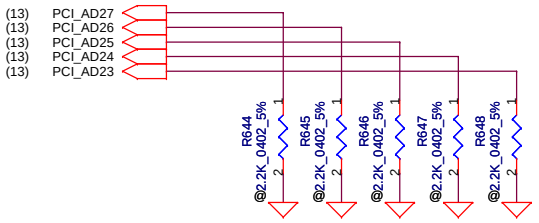


DEBUG STRAPS

FCH M1 HAS 15K INTERNAL PU FOR PCI_AD[27:23]

		PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23 Enable ROM Straps
PULL HIGH		USE internal PLL generated PLL CLK DEFAULT	ILA AUTORUN Disabled DEFAULT	Selects FC PLL DEFAULT	Disable I2C ROM DEFAULT	Required Setting DEFAULT
PULL LOW		BYPASS PCI PLL	ILA AUTORUN Enabled	FC PLL bypassed	Getting Value from I2C EPROM	Reserved

Check AD29,AD28 strap function check default



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Compal Electronics, Inc.

Title: FCH-VSS/Strap

Size	Document Number	Rev
B	LA6755P/7P	1.0

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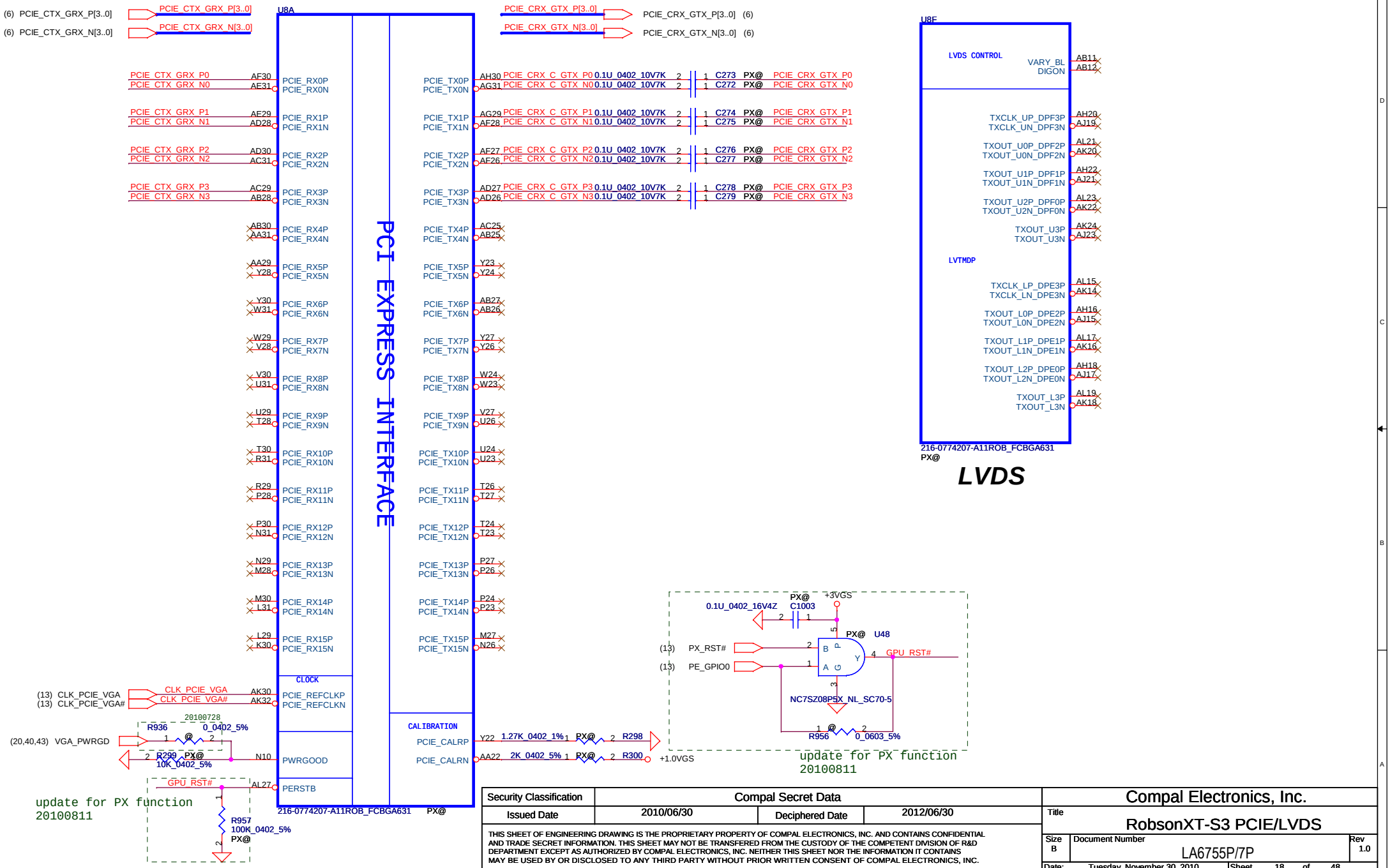

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Compal Electronics, Inc.

Title: RobsonXT-S3 PCIE/LVDS

Size	Document Number	Rev
B	LA6755P/7P	1.0

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TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis diabled for mobile mode 1: Tx de-emphasis enabled (Defailt setting for desktop)

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

Internal pull down

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	0
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	0
RSVD	GPIO2	0 : 2.5GT/s ; 1 : 5.0GT/s, internal PD.	0
RSVD	GPIO8	RESERVED	0
BIF_VGA DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	000
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
RSVD	H2SYNC		0
RSVD	GENERICC		0
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	11

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOS ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET

If we meet some issue on bring up, we can check this item during reset.

GPIO21 H2SYNC GENERICC GPIO2 GPIO8

STRAPS

GPIO_GPIO0	R309	10K_0402_5%
GPIO_GPIO1	R310	10K_0402_5%
GPIO_GPIO2	R311	10K_0402_5%
GPIO_GPIO5	R308	10K_0402_5%
		20100728
GPIO_GPIO8	R313	10K_0402_5%
GPIO_GPIO9	R314	10K_0402_5%
GPIO_GPIO11	R315	10K_0402_5%
GPIO_GPIO12	R316	10K_0402_5%
GPIO_GPIO13	R317	10K_0402_5%

change from SM010009U00 to SD028000080
20101012

Chnge from SM010030010 to SD013000080
since EVT 20101012

0.60 V level, Please VREFG Divider ans cap close to ASIC

XTALIN
Voltage Swing: 1.8 V

For HDMI Audio strap

Change footprint
20100812

Need to change back to 1402-1 after BIOS confirm!!!

VGA Thermal Sensor ADM1032 Closed to GPU

EMC1412-A (SA00003Y A00)
Address 1111_100xb
S IC EMC1412-A-ACZL-TR MSOP 8P SENSOR

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Compal Electronics, Inc.

Title: RobsonXT-S3 Main Generic/MSIC

Size	Document Number	Rev
C	LA6755P/7P	1.0

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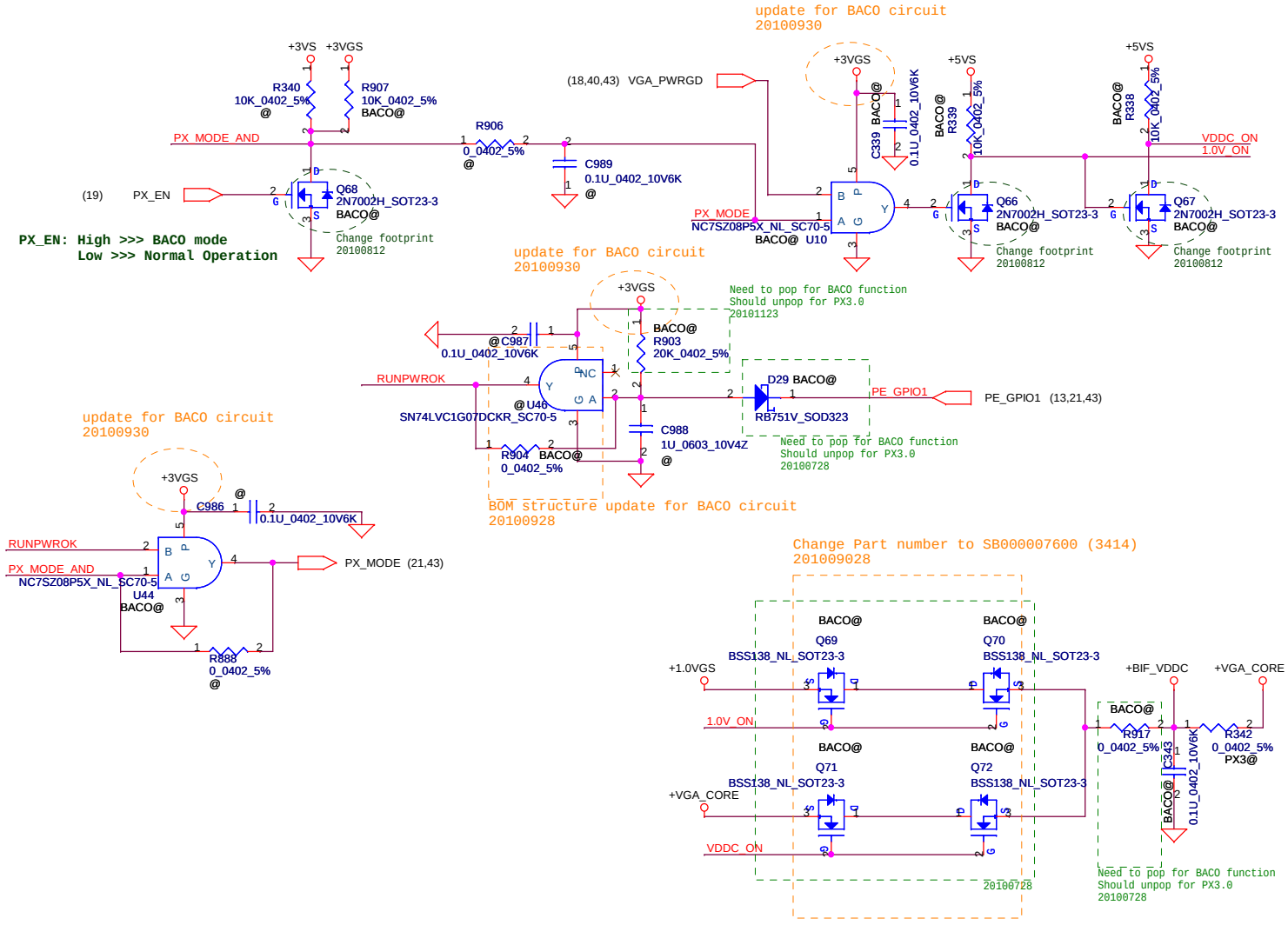

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Compal Electronics, Inc.

Title: RobsonXT-S3 BACO

Size	Document Number	Rev
B	LA6755P/7P	1.0

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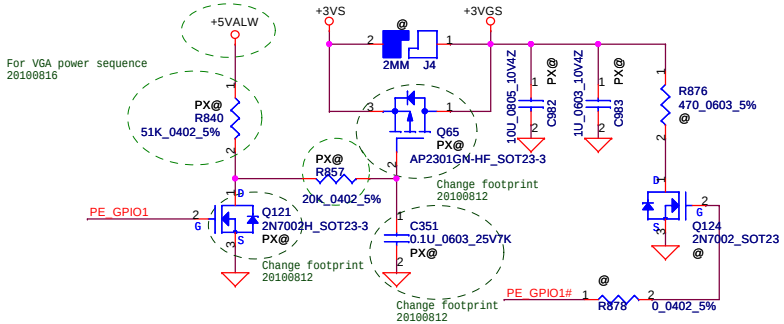
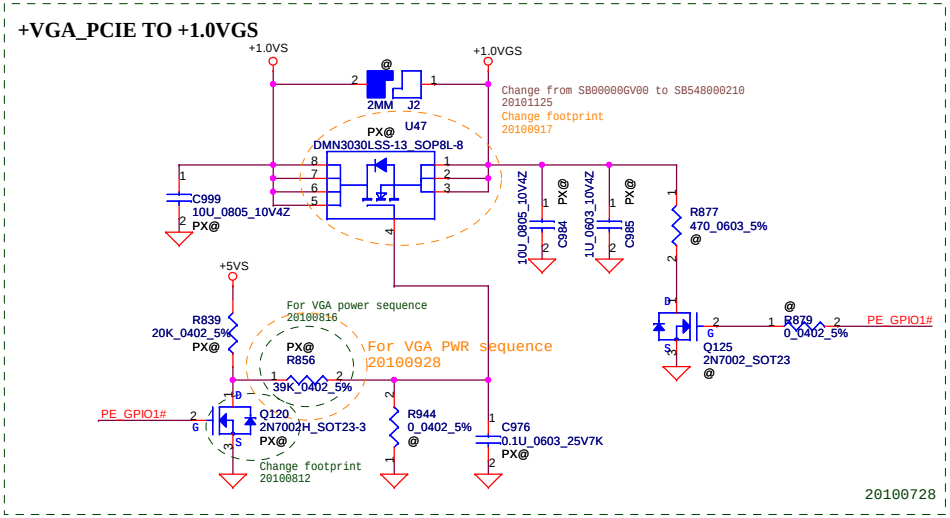
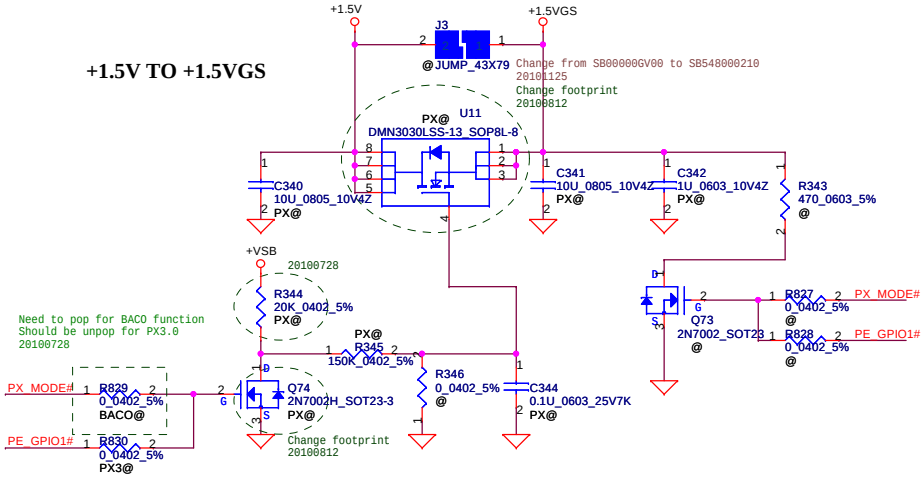
+3.3VS TO +3.3VGS



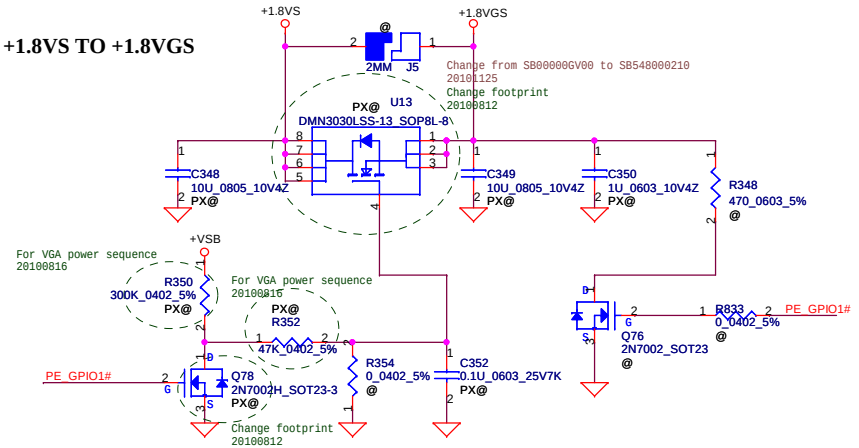
+VGA_PCIE TO +1.0VGS

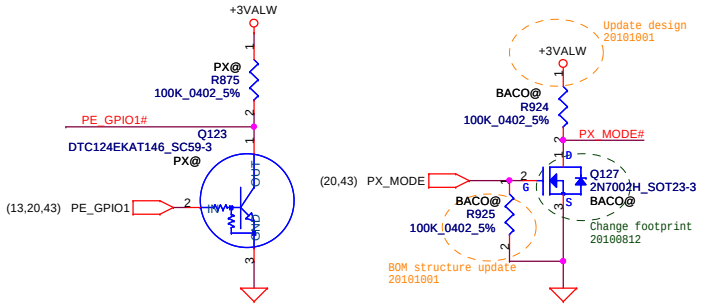


+1.5V TO +1.5VGS



+1.8VS TO +1.8VGS





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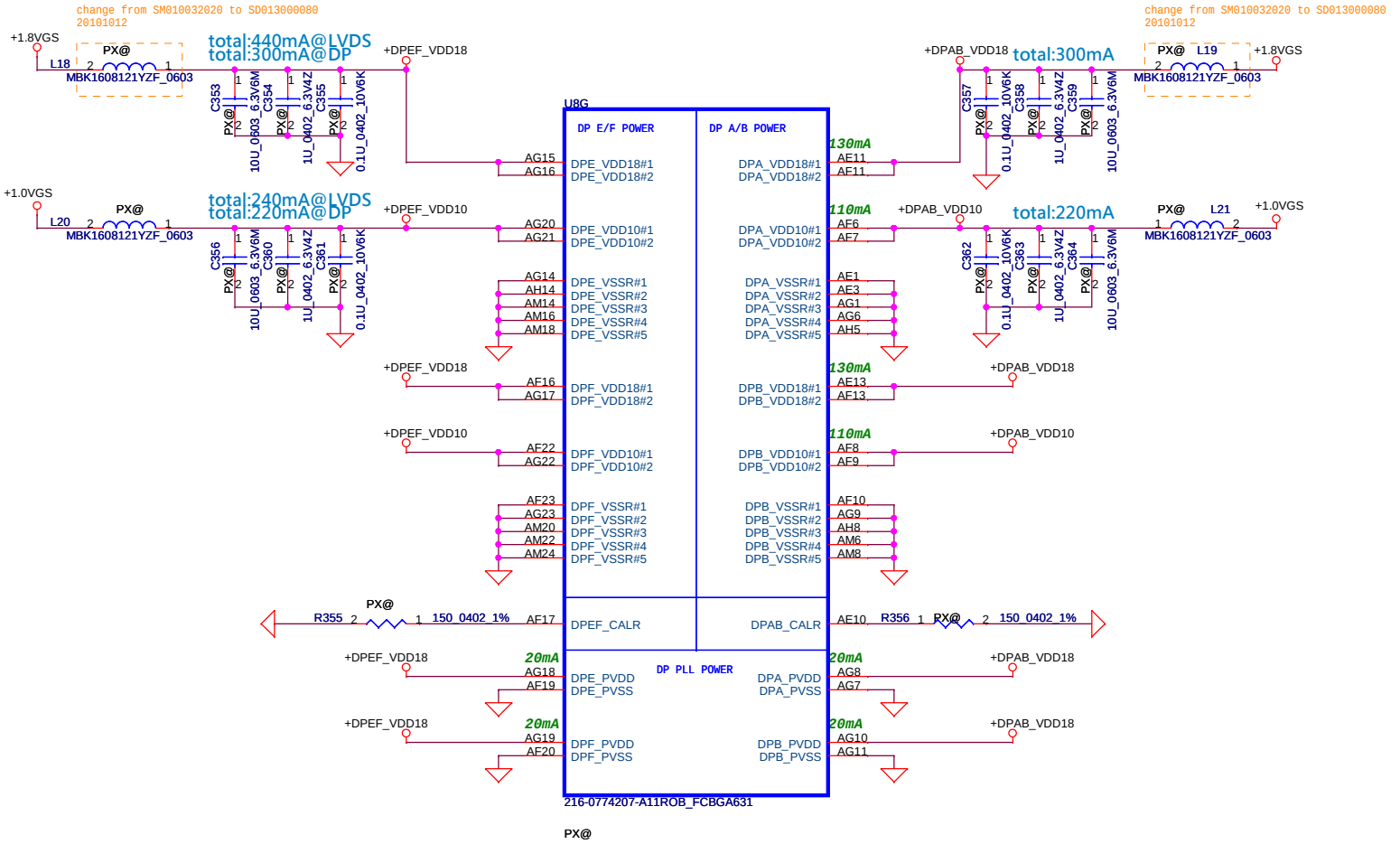
Compal Electronics, Inc.

Title: RobsonXT-S3 DC Interface

Size	Document Number	Rev
Custom	LA6755P/7P	1.0

Date: Tuesday, November 30, 2010 Sheet 21 of 48



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Compal Electronics, Inc.

Title: RobsonXT-S3 DP PWR

Size	Document Number	Rev
B	LA6755P/7P	1.0

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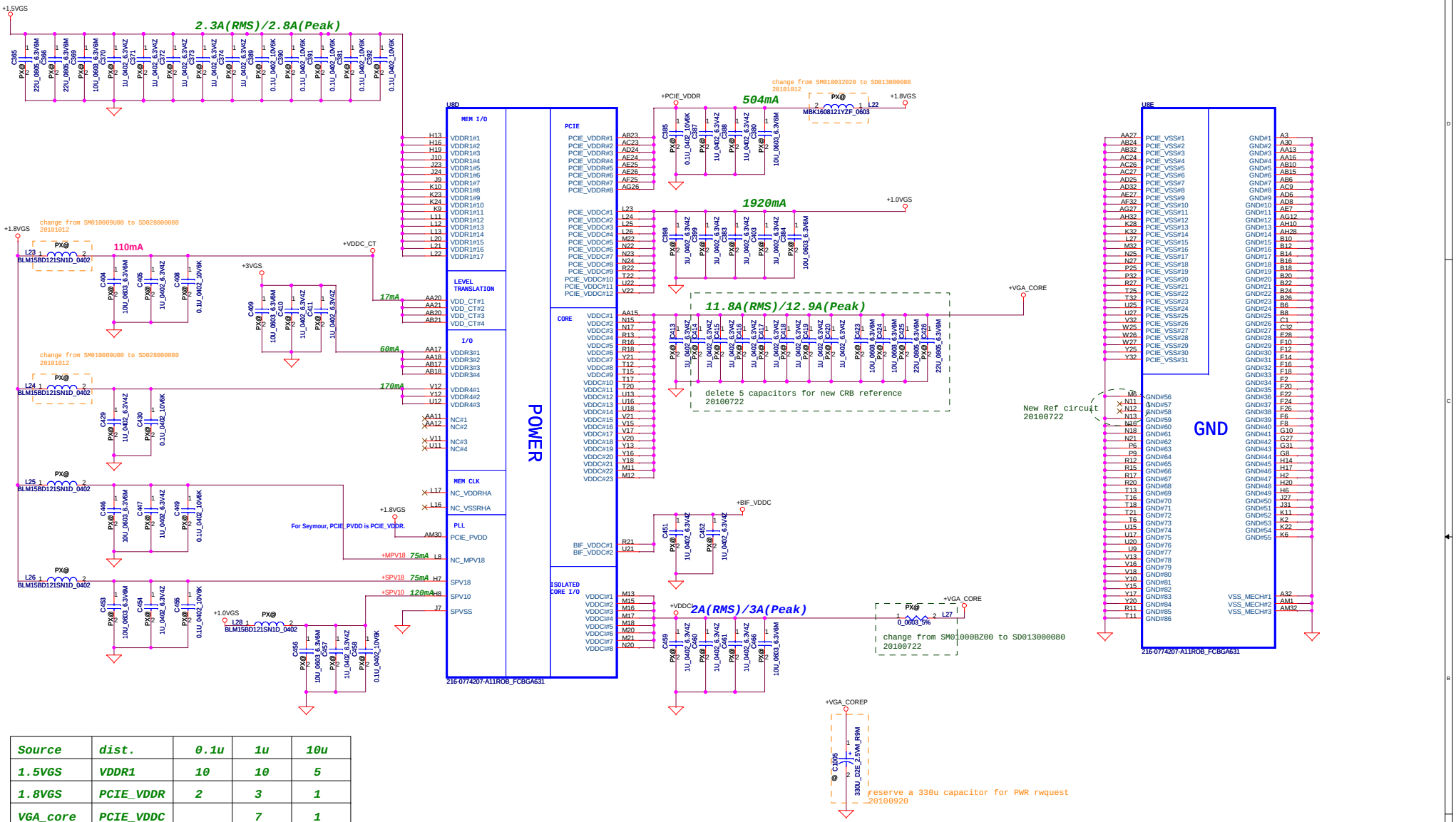

Source	dist.	0.1u	1u	10u
1.5VGS	VDDR1	10	10	5
1.8VGS	PCIE_VDDR	2	3	1
VGA_core	PCIE_VDDC		7	1
	VDDC		25	6
	VDDCI		6	2

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Issued Date	2010/06/30	Deciphered Date	2012/06/30

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Compal Electronics, Inc.

Title: RobsonXT-S3 PWR/GND

Size	Document Number	Rev
C	LA6755P/7P	1.0

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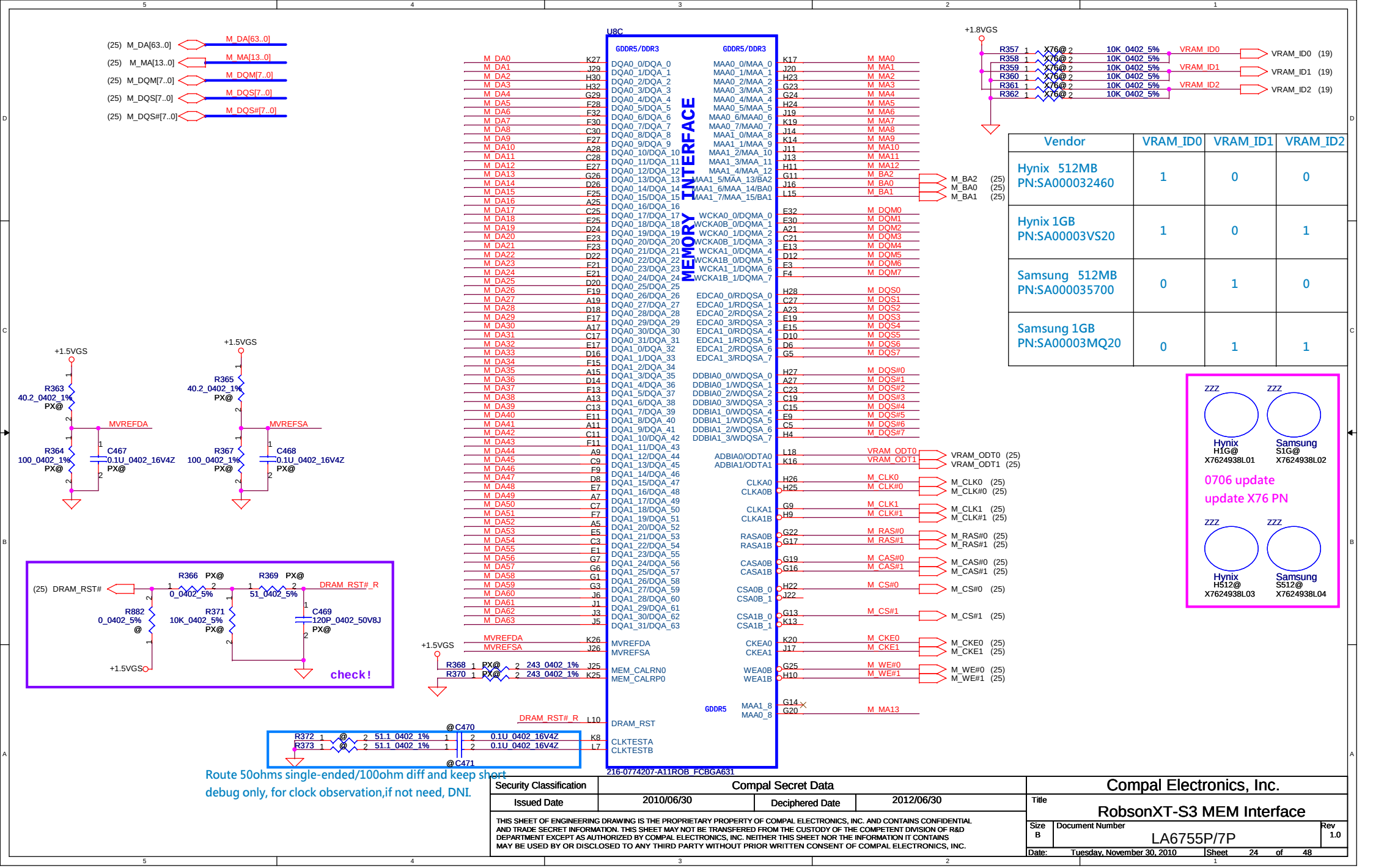

Vendor	VRAM_ID0	VRAM_ID1	VRAM_ID2
Hynix 512MB PN:SA000032460	1	0	0
Hynix 1GB PN:SA00003VS20	1	0	1
Samsung 512MB PN:SA000035700	0	1	0
Samsung 1GB PN:SA00003MQ20	0	1	1

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Compal Electronics, Inc.

Title: RobsonXT-S3 MEM Interface

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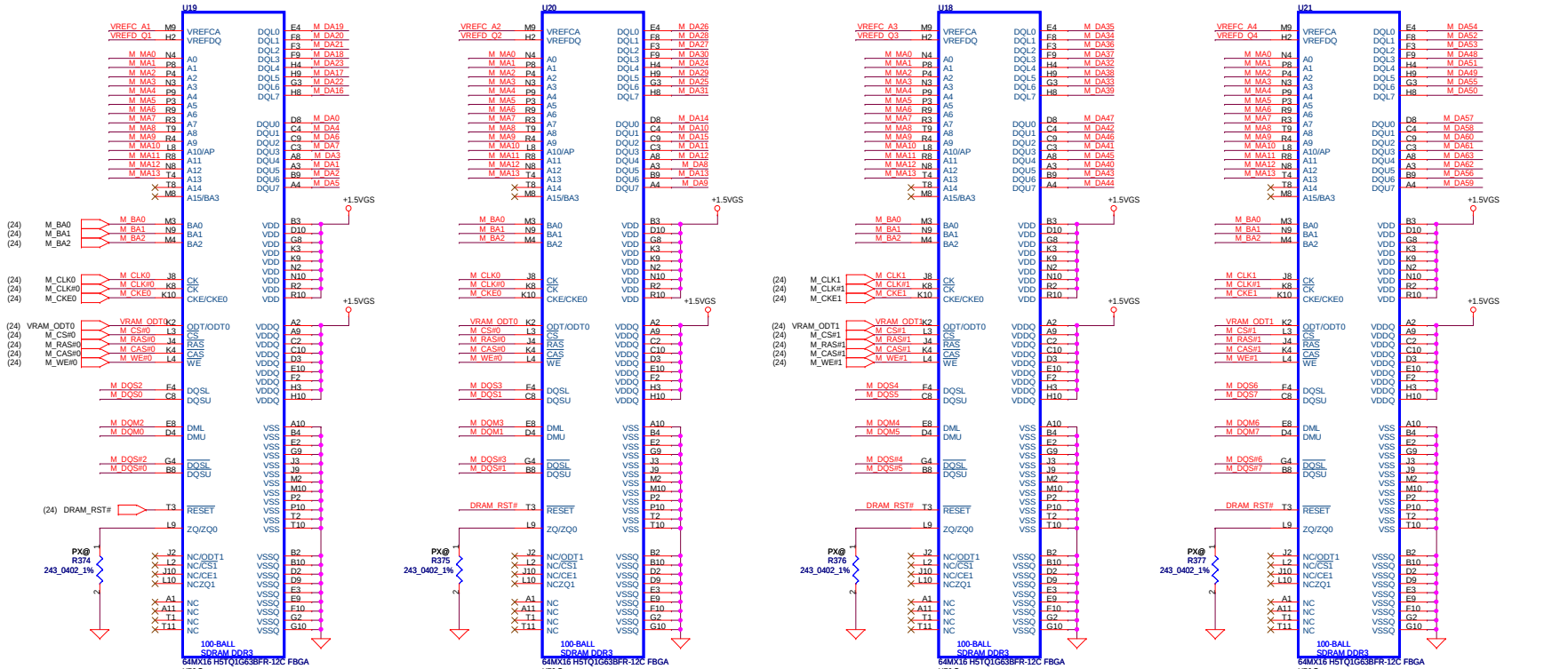
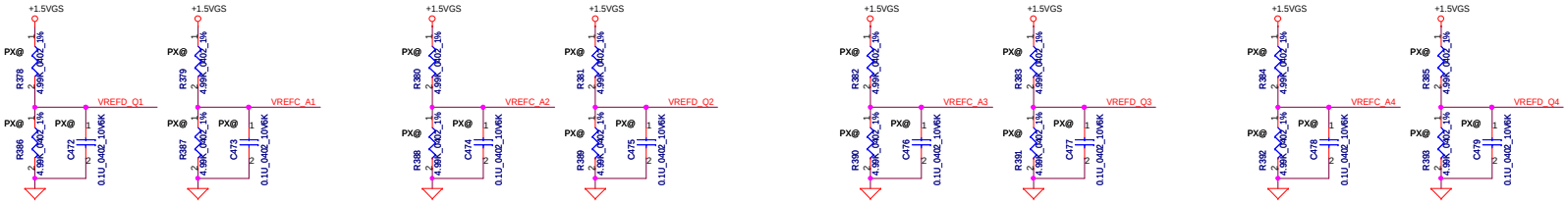
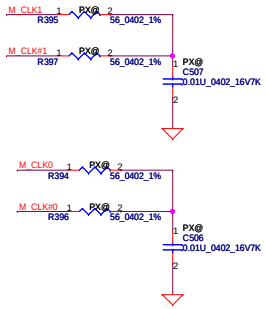
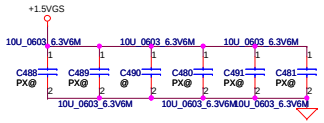
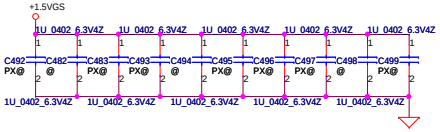
(24) M_DA[63..0] — M_DA[63..0]
(24) M_MA[13..0] — M_MA[13..0]
(24) M_DQM[7..0] — M_DQM[7..0]
(24) M_DQS[7..0] — M_DQS[7..0]
(24) M_DQS#[7..0] — M_DQS#[7..0]

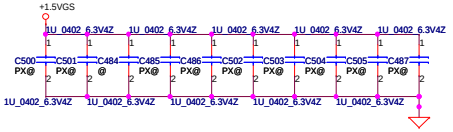












VRAM P/N :
Hynix : SA000041S10 (S IC D3 64MX16 H5TQ1G63BFR-11C FBGA C38!)
Samsung : SA000041T10 (S IC D3 64MX16 K4W1G1646E-HC11 FBGA C38!)
update VRAM PN 0619 update

Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2012/06/30

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Compal Electronics, Inc.

Title: RobsonXT-S3 VRAM

Size	Document Number	Rev
C	LA6755P/7P	1.0

Date: Tuesday, November 30, 2010 Sheet 25 of 48

+3VALW

+3V_LAN

J6

JUMP_43X79

Atheros request can't disable LAN power

+1.7_VDDCT

+1.7_LX

C784 10U_0805_10V4Z

C785 0.1U_0402_16V4Z

@C786 1000P_0402_50V7K

L56 4.7UH_SIA4012-4R7M_20%

Note:
Place Close to LAN chip
L56 DCR< 0.15 ohm
Rate current of L33 > 1A

Close to Pin40

Power On strapping

Pin	Description	Chip Default
LED0	H:Over Clock Enable L:Over Clock Disable *	H
LED2	H:SWR Switch mode regulator Select * AR8151 Pin23=LED2. AR8152, Pin23 is CLKREQ	--

U29 8152@

S IC AR8152-AL1E QFN 40P E-LAN CTRL

Place Close to Chip

no overclocking
PD 5.1K

R650 5.1K_0402_5%

LED0,1,2 intel Pull UP

Atheros
8151-AL1A

(13) PCIE_FRX_DTX_N0 — C789 0.1U_0402_16V7K — PCIE_FRX_DTX_N0_C — 29 TX_N
(13) PCIE_FRX_DTX_P0 — C790 0.1U_0402_16V7K — PCIE_FRX_DTX_P0_C — 30 TX_P
(13) PCIE_FTX_C_DRX_N0 — 36 RX_N
(13) PCIE_FTX_C_DRX_P0 — 35 RX_P
(13) CLK_PCIE_LAN# — 32 REFCLK_N
(13) CLK_PCIE_LAN — 33 REFCLK_P
(13,30,31) PLT_RST# — PLT_RST# — 2 PERST#
(14,30) FCH_PCIE_WAKE# — R652 @ 0_0402_5% — PCIE_WAKE# — 3 WAKE#
(31) LAN_WAKE#
25 SMCLK
26 SMDATA
28 TEST_RST
27 TESTMODE

LED_0 38 — ACTIVITY (27)
LED_1 39 — LAN_LINK# (27)
LED_2 23 — R651 8152@ 0_0402_5% — LAN_CLKREQ#

TRXN0 12 — MDI0- — MDI0- (27)
TRXP0 11 — MDI0+ — MDI0+ (27)
TRXN1 15 — MDI1- — MDI1- (27)
TRXP1 14 — MDI1+ — MDI1+ (27)
TRXN2 18 — MDI2- — MDI2- (27)
TRXP2 17 — MDI2+ — MDI2+ (27)
TRXN3 21 — MDI3- — MDI3- (27)
TRXP3 20 — MDI3+ — MDI3+ (27)

RBIAS 10 — LAN_RBIAS — R654 2.37K_0402_1%
VDD33 1 — +3V_LAN
LX 40 — +1.7_LX
VDDCT 5 — +1.7_VDDCT
DVDDL 24, DVDDL_REG 37 — +1.1_DVDDL — C797 0.1U_0402_16V4Z, C798 1U_0402_6.3V4Z, C800 0.1U_0402_16V4Z — Near Pin37
AVDDH 16, 22, AVDDH_REG 9 — +2.7_AVDDH

C791 0.1U_0402_16V4Z
C792 1U_0402_6.3V4Z
C794 10U_0805_10V4Z
C795 @ 10U_0805_10V4Z
C799 0.1U_0402_16V4Z

C791 & C792 Close pin1 < 200mil
C794 & 795 Close pin < 400mil

+3VALW — @R926 10K_0402_5% — LAN_CLKREQ#

(14) LAN_CLKREQ# — R657 GIGA@ 0_0402_5% — CLKREQ_LAN#_R — C796 0.1U_0402_16V4Z 8152@ — 4 CLKREQ#

LAN_XTALO — 7 XTLO
LAN_XTALI — 8 XTLI

+1.1_AVDDL — 13, 19, 31, 34 AVDDL
6 AVDDL_REG
41 GND

AR8151-AL1A_QFN40_5X5
GIGA@

C801 GIGA@ 0.1U_0402_16V4Z — Near Pin13
C802 GIGA@ 0.1U_0402_16V4Z — Near Pin19
C803 0.1U_0402_16V4Z — Near Pin31
C804 0.1U_0402_16V4Z — Near Pin34
C805 1U_0402_6.3V4Z — Near Pin6
C806 0.1U_0402_16V4Z

C807 1U_0402_6.3V4Z — Near Pin9
C808 0.1U_0402_16V4Z
C809 0.1U_0402_16V4Z — Near Pin22
C810 GIGA@ 0.1U_0402_16V4Z — Near Pin16

LAN_XTALI
LAN_XTALO
Y6 25MHZ_20PF_7A25000012
C815 27P_0402_50V8J
C816 27P_0402_50V8J

Place Close to LAN chip

MDI0+ R658 49.9_0402_1% — @C811 1000P_0402_50V7K
MDI0- R659 49.9_0402_1% — C812 0.1U_0402_16V4Z
MDI1+ R660 49.9_0402_1% — @C813 1000P_0402_50V7K
MDI1- R661 49.9_0402_1% — C814 0.1U_0402_16V4Z
MDI2+ R662 GIGA@ 49.9_0402_1% — @C817 1000P_0402_50V7K
MDI2- R663 GIGA@ 49.9_0402_1% — C818 0.1U_0402_16V4Z GIGA@
MDI3+ R664 GIGA@ 49.9_0402_1% — @C819 1000P_0402_50V7K
MDI3- R665 GIGA@ 49.9_0402_1% — C820 0.1U_0402_16V4Z GIGA@

8152 no mount MDI3+,MDI3-,MDI2-,MDI2+ resister and cap

	Pin4	Configure R657	Configure C796		Pin23	Configure R651
AR8152	VDDCT_REG		*		CLKREQn	*
AR8151	CLKREQn	*			LED[2]	

Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2012/06/30

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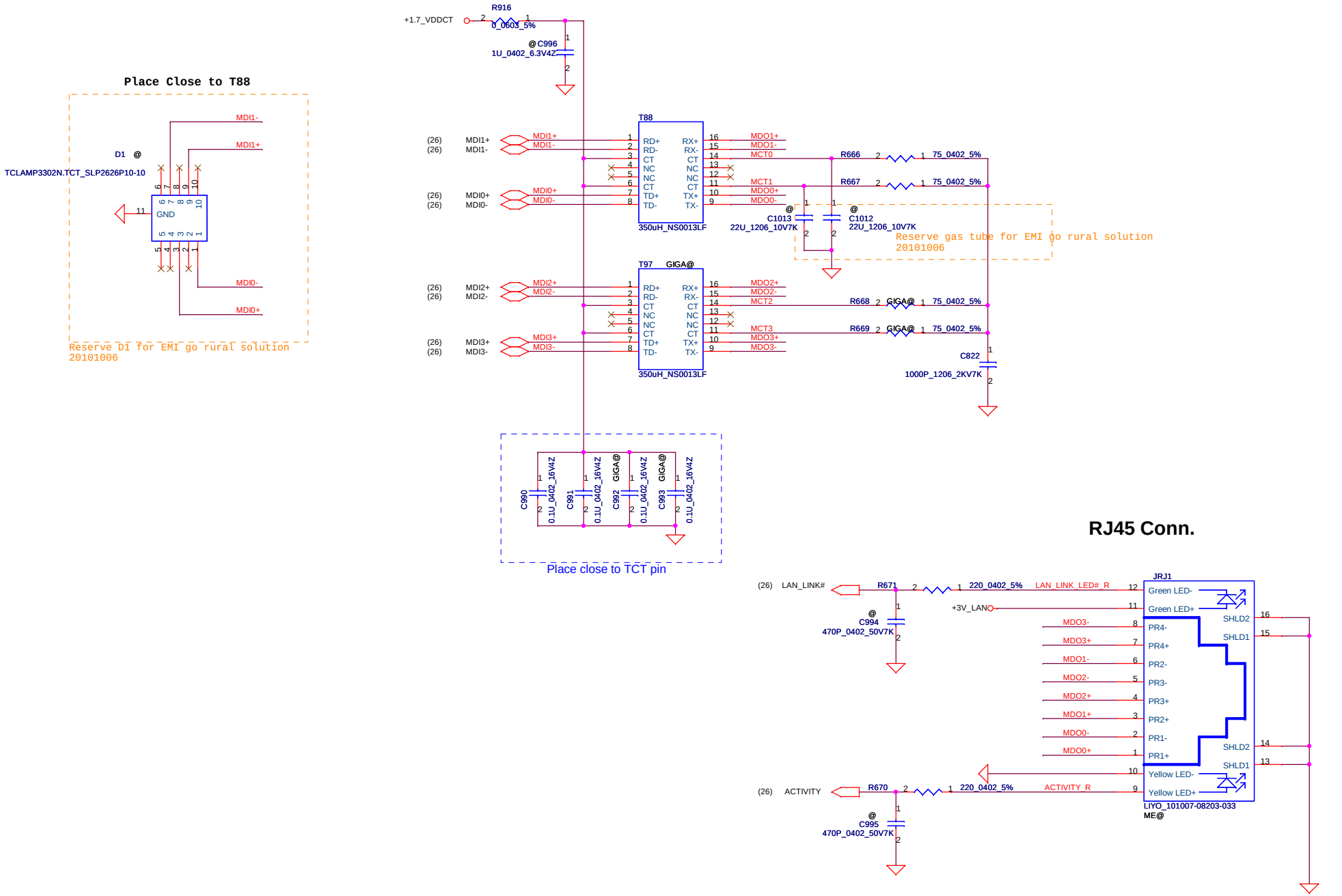
Compal Electronics, Inc.

Title: LAN-AR8151/8152

Size: Custom | Document Number: LA6755P/7P | Rev: 1.0

Date: Tuesday, November 30, 2010 | Sheet 26 of 48



Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2012/06/30

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Compal Electronics, Inc.

Title: LAN_Transformer

Size	Document Number	Rev
Custom	LA6755P/7P	1.0

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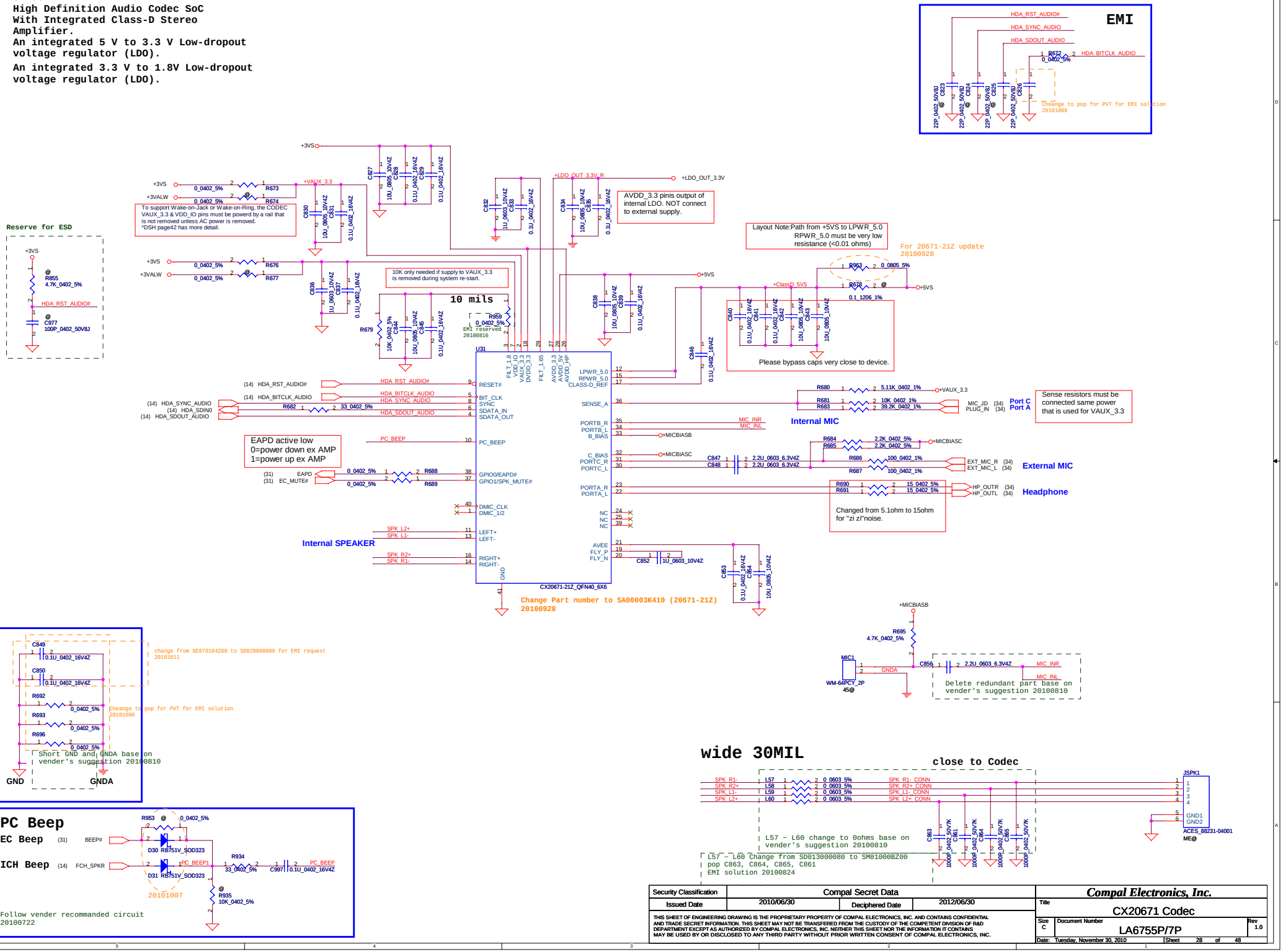
CX20671
High Definition Audio Codec SoC With Integrated Class-D Stereo Amplifier.
An integrated 5 V to 3.3 V Low-dropout voltage regulator (LDO).
An integrated 3.3 V to 1.8V Low-dropout voltage regulator (LDO).



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Issued Date	2010/06/30	Deciphered Date	2012/06/30

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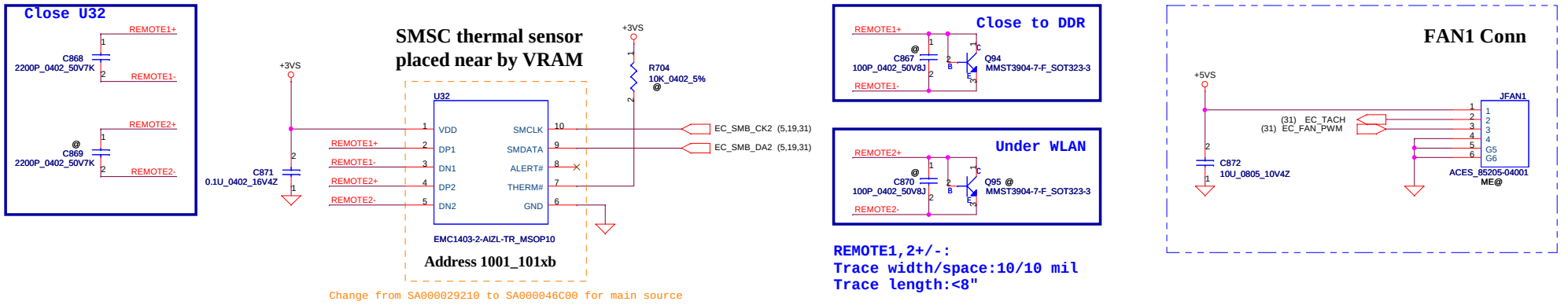
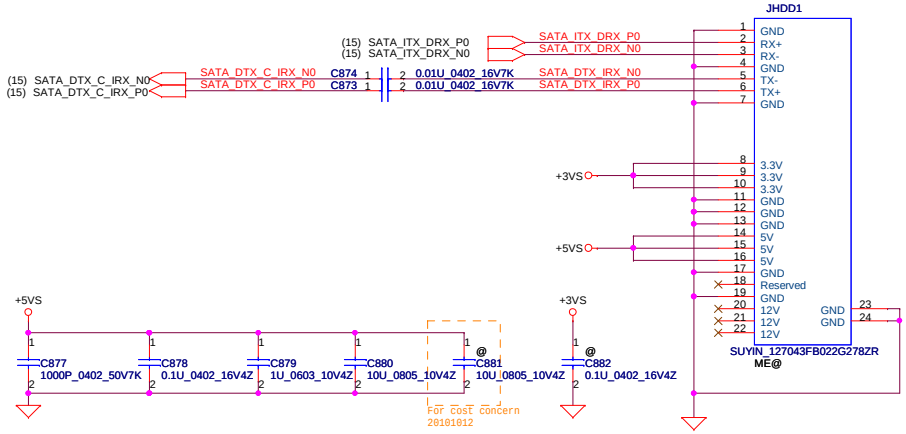
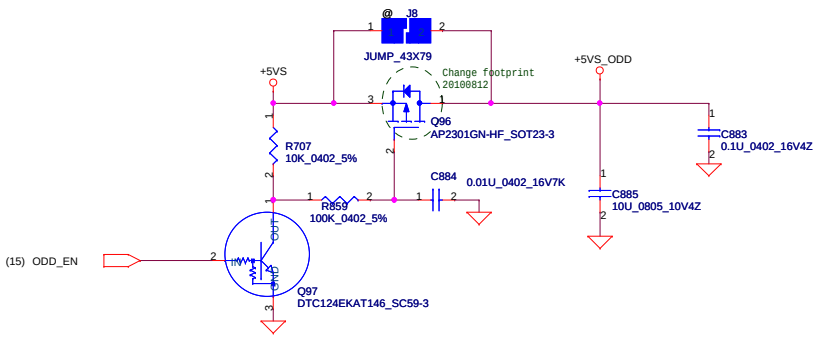
Compal Electronics, Inc.			
Title	CX20671 Codec		
Size C	Document Number LA6755P/7P		Rev 1.0
Date: Tuesday, November 30, 2010	Sheet 28 of 48		



SATA HDD Conn.



ODD Power Control



Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2012/06/30

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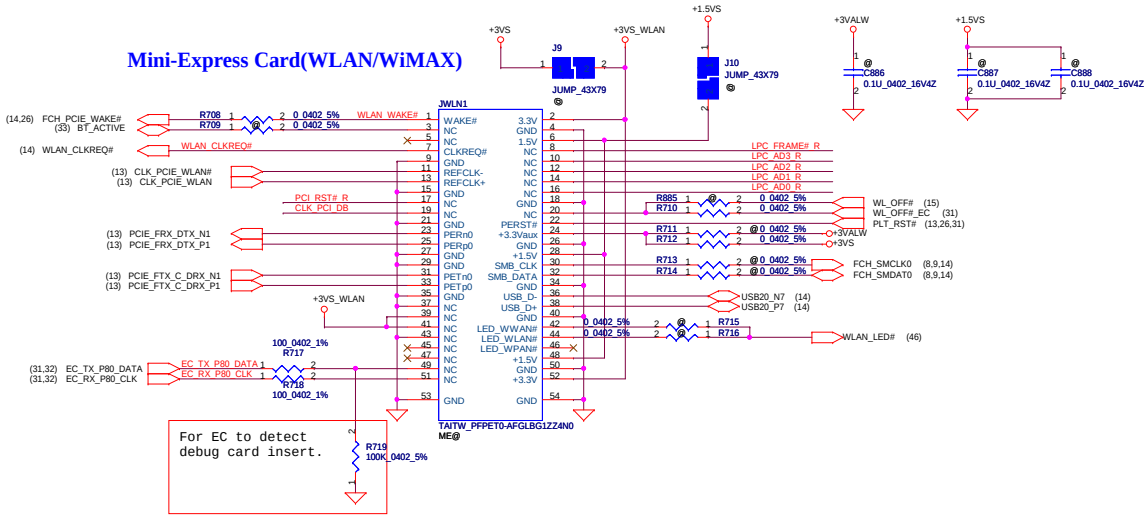
Compal Electronics, Inc.			
Title	HDD/ODD/EMC1403/FAN		
Size B	Document Number LA6755P/7P		Rev 1.0
Date: Tuesday, November 30, 2010	Sheet 29 of 48		

Mini-Express Card for WLAN/WiMAX(Half)



Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.

LPC_FRAME#_R	R720	@	0_0402_5%	LPC_FRAME#	LPC_FRAME# (13,31)
LPC_AD3_R	R721	@	0_0402_5%	LPC_AD3	LPC_AD3 (13,31)
LPC_AD2_R	R722	@	0_0402_5%	LPC_AD2	LPC_AD2 (13,31)
LPC_AD1_R	R723	@	0_0402_5%	LPC_AD1	LPC_AD1 (13,31)
LPC_AD0_R	R724	@	0_0402_5%	LPC_AD0	LPC_AD0 (13,31)
PCI_RST#_R	R725	@	0_0402_5%	PLT_RST#	
CLK_PCI_DB					CLK_PCI_DB (13)

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Issued Date	2010/06/30	Deciphered Date	2012/06/30

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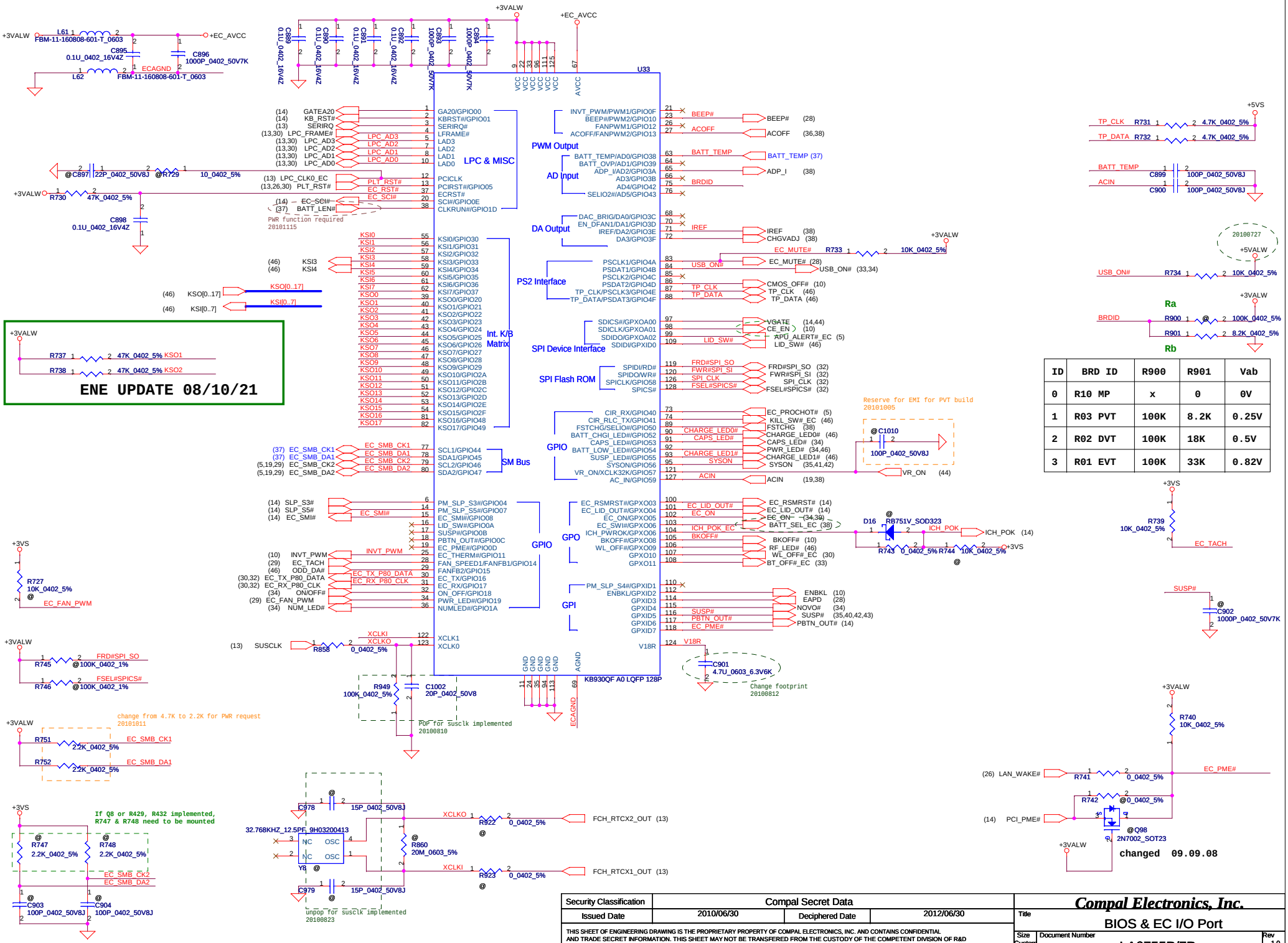
Compal Electronics, Inc.

Title	Mini PCIE		
Size	Document Number		Rev
	LA6755P/7P		1.0
Date:	Tuesday, November 30, 2010	Sheet	30 of 48



ID	BRD ID	R900	R901	Vab
0	R10 MP	x	0	0V
1	R03 PVT	100K	8.2K	0.25V
2	R02 DVT	100K	18K	0.5V
3	R01 EVT	100K	33K	0.82V

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Issued Date	2010/06/30	Deciphered Date	2012/06/30

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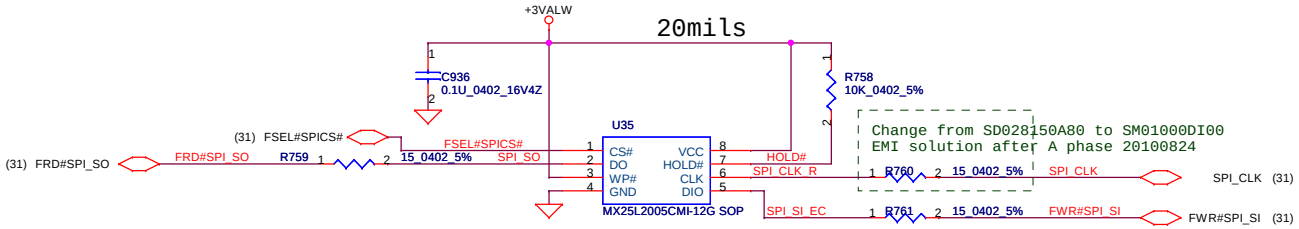
Compal Electronics, Inc.

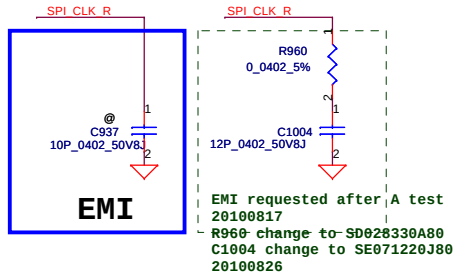
Title: BIOS & EC I/O Port

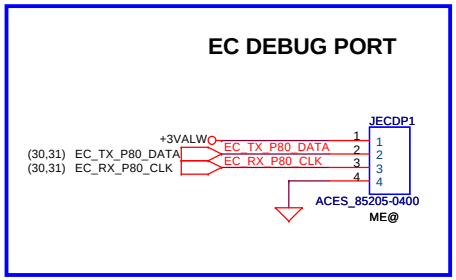
Size	Document Number	Rev
Custom	LA6755P/7P	1.0

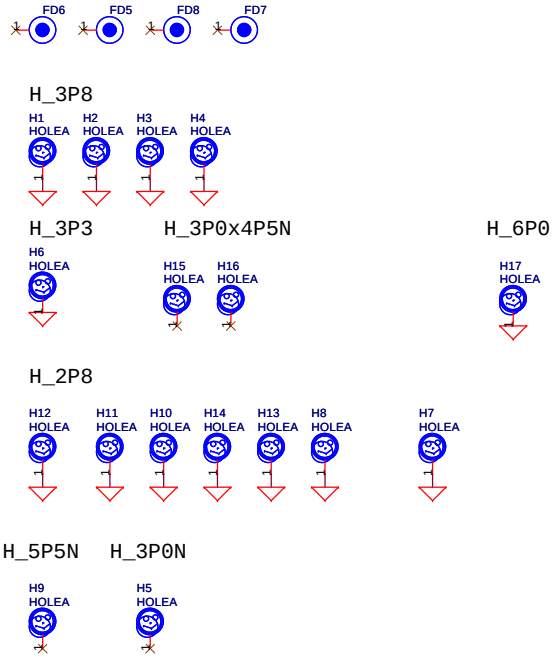
Date: Tuesday, November 30, 2010 | Sheet 31 of 48

FOR EC 128KB SPI ROM
(150mil PACKAGE)
SA00003FL10
SA00003JD00









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Compal Electronics, Inc.

Title: EC SPI ROM/LPC Debug Conn.

Size	Document Number	Rev
B	LA6755P/7P	1.0

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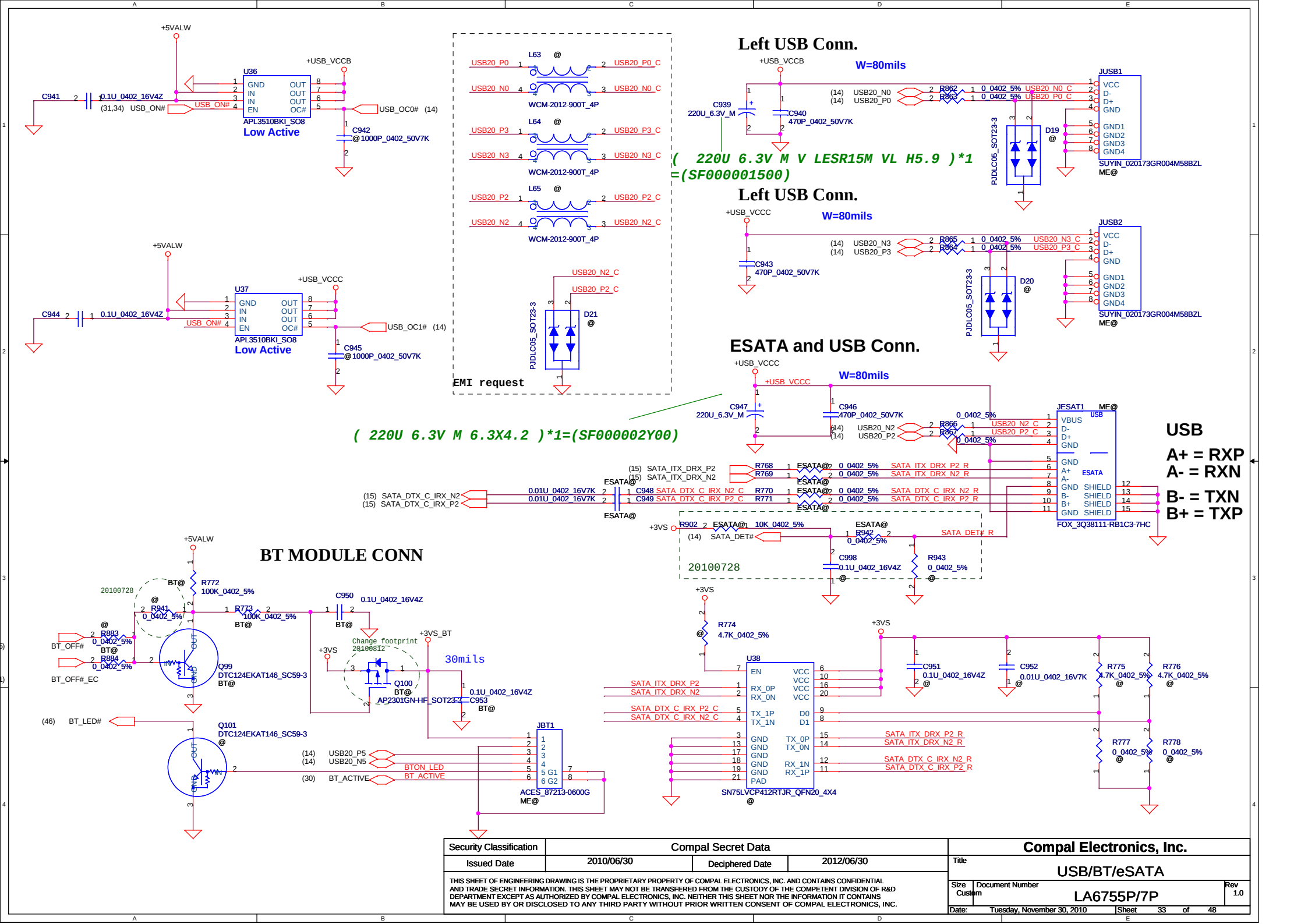

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Compal Electronics, Inc.

Title: USB/BT/eSATA

Size	Document Number	Rev
Custom	LA6755P/7P	1.0

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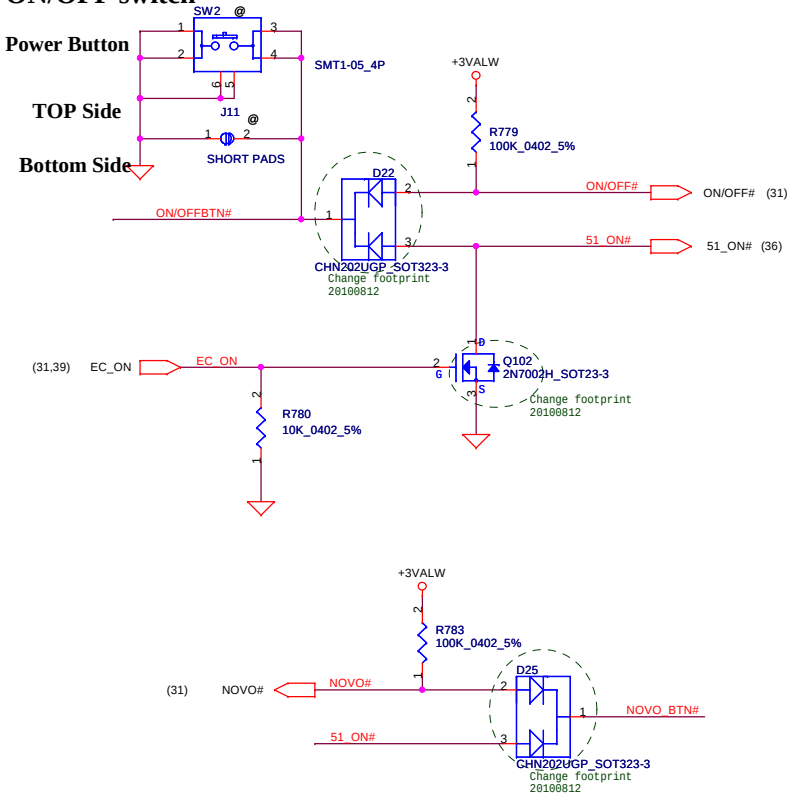
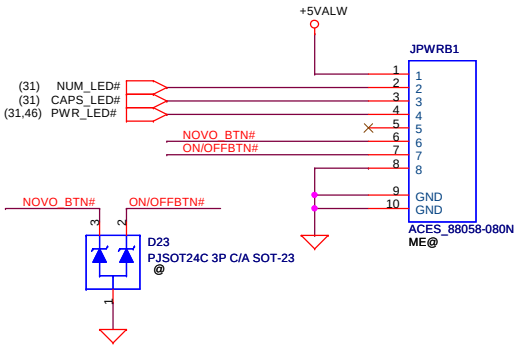
ON/OFF switch

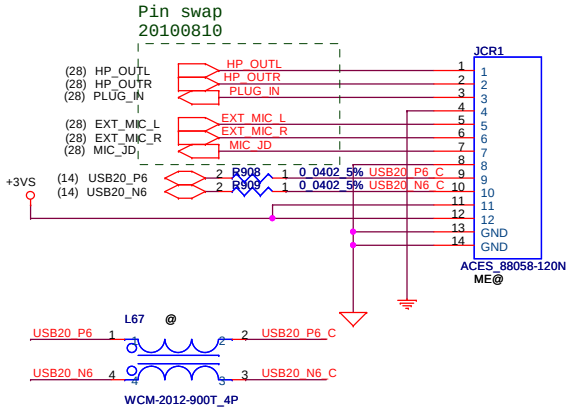


Power Button Board Conn. 8pin

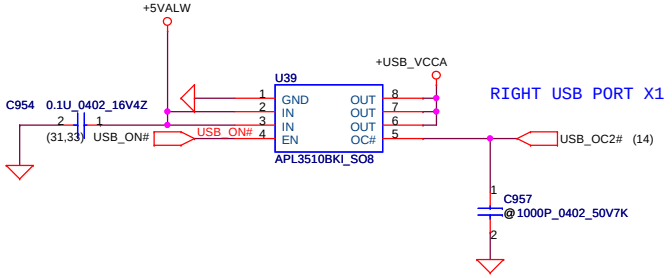


EMI REQUEST 1ST = SCA00000E00
2ST = SCA00000R00

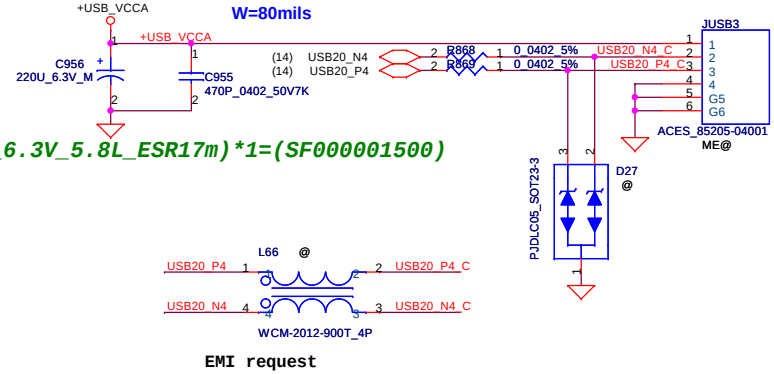
Card Reader/Audio Jack SB CONN



EMI request



Right USB Conn.



*(220uF_6.3V_5.8L_ESR17m)*1=(SF000001500)*

EMI request

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Issued Date	2010/06/30	Deciphered Date	2012/06/30

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Compal Electronics, Inc.

Title: Other IO/USB (right)

Size	Document Number	Rev
Custom	LA6755P/7P	1.0

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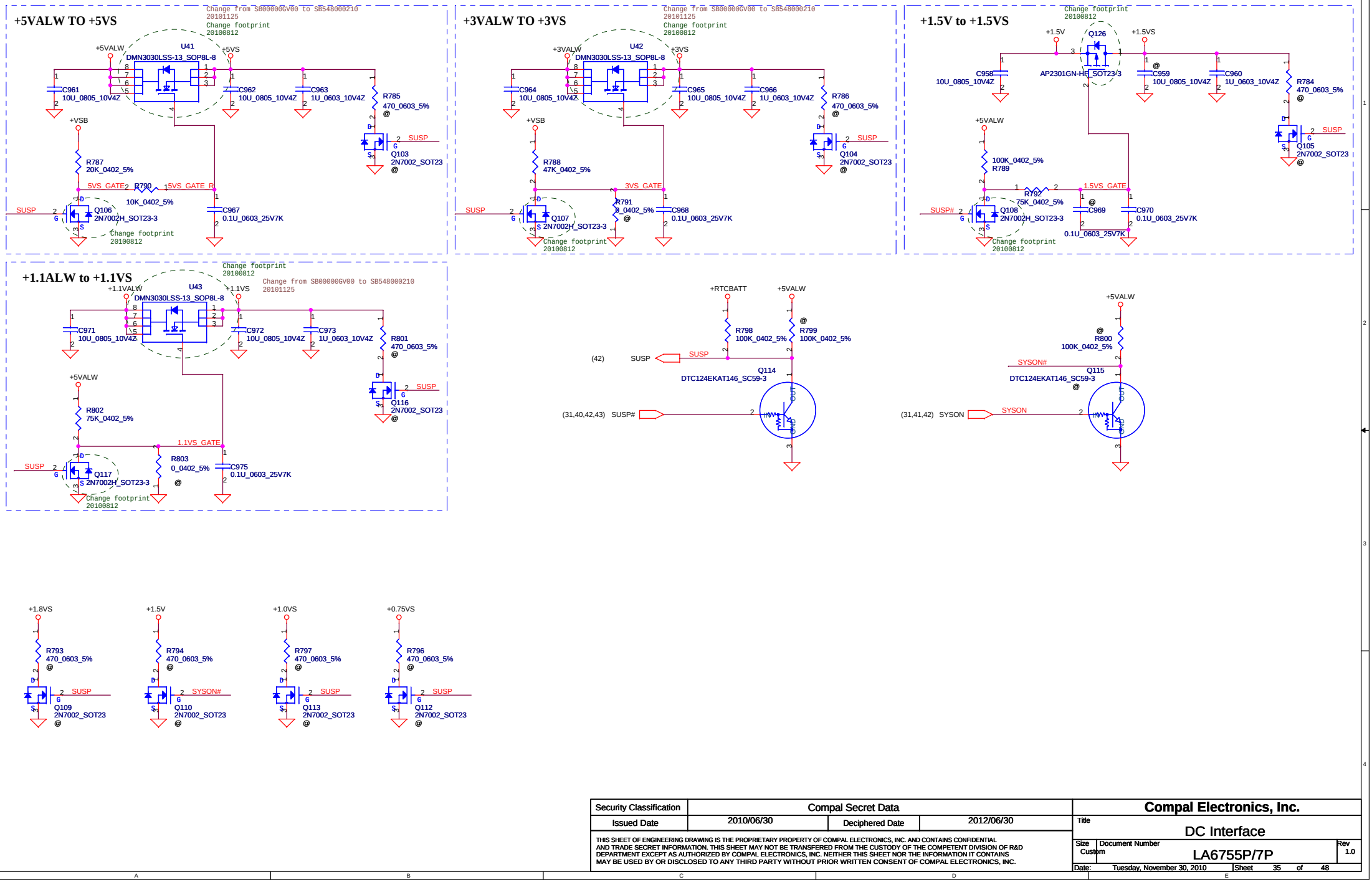

Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2012/06/30

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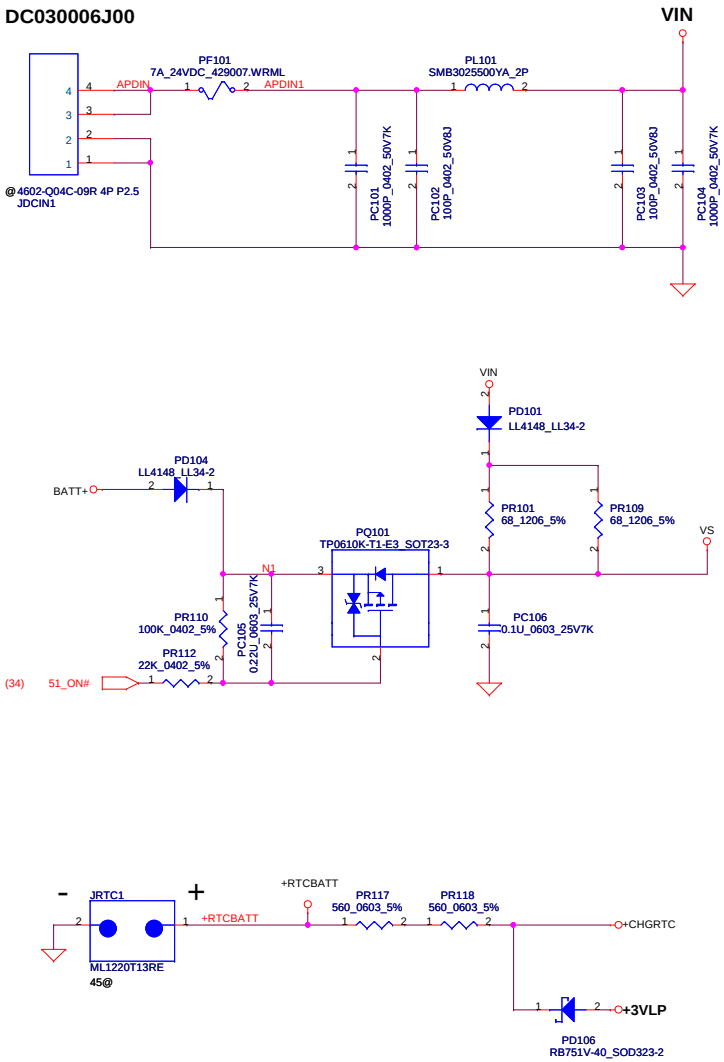
Compal Electronics, Inc.

Title: DC Interface

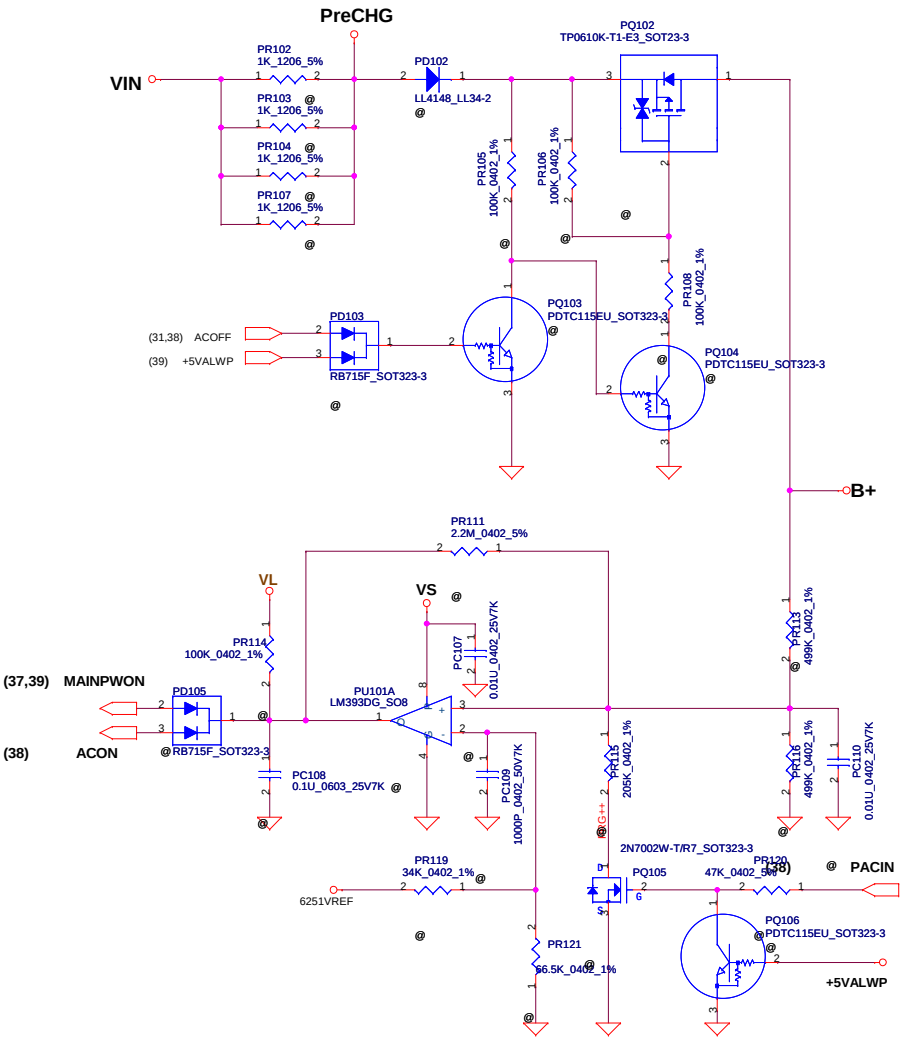
Size	Document Number	Rev
Custom	LA6755P/7P	1.0

Date: Tuesday, November 30, 2010 | Sheet 35 of 48

DC030006J00



Precharge detector 15.97V/14.84V FOR ADAPTOR



ACIN

Precharge detector	Min.	typ.	Max.
L-->H	14.991V	15.381V	15.782V
H-->L	13.860V	14.247V	14.621V

BATT ONLY

Precharge detector	Min.	typ.	Max.
L-->H	7.196V	7.349V	7.505V
H-->L	6.138V	6.214V	6.056V

Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2012/06/30

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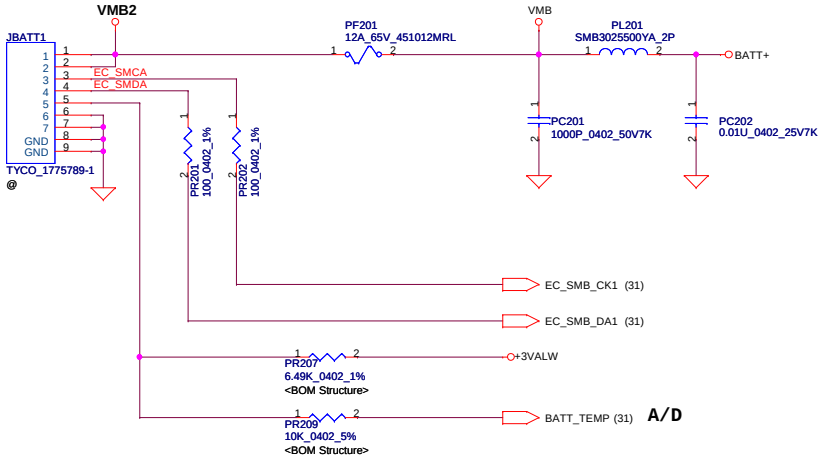
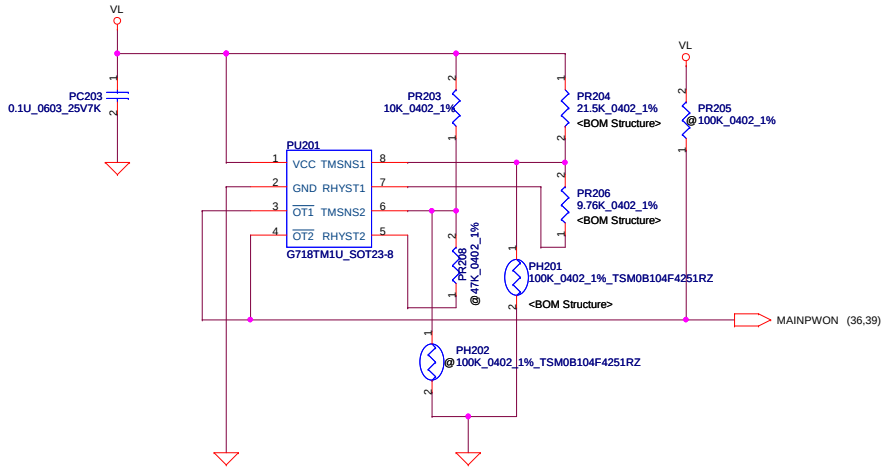
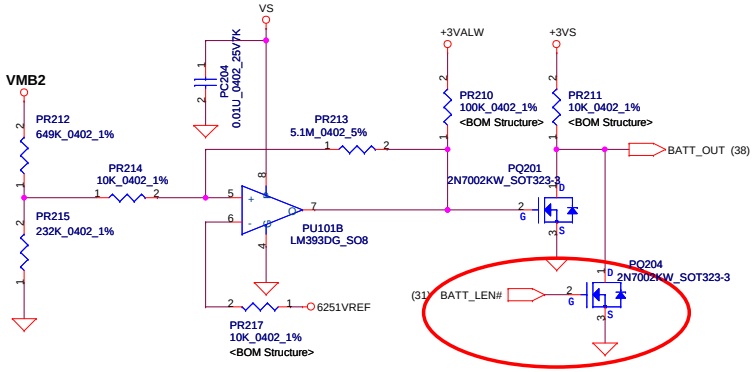
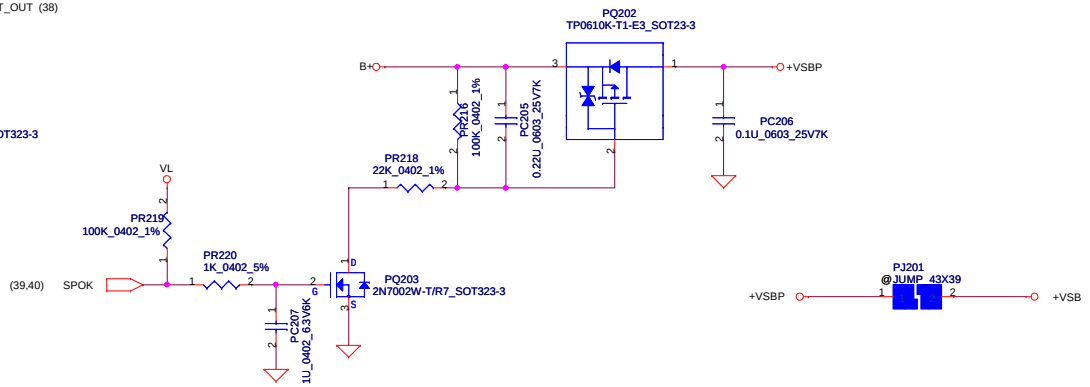
Compal Electronics, Inc.	
Title	DCIN / Vin Detector /Pre-charge
Size: Custom	Document Number: PAWGC
Rev	0.1
Date: Tuesday, November 30, 2010	Sheet 36 of 47

PH1 under CPU botten side :
CPU thermal protection at 92 degree C
Recovery at 56 degree C









Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2012/06/30

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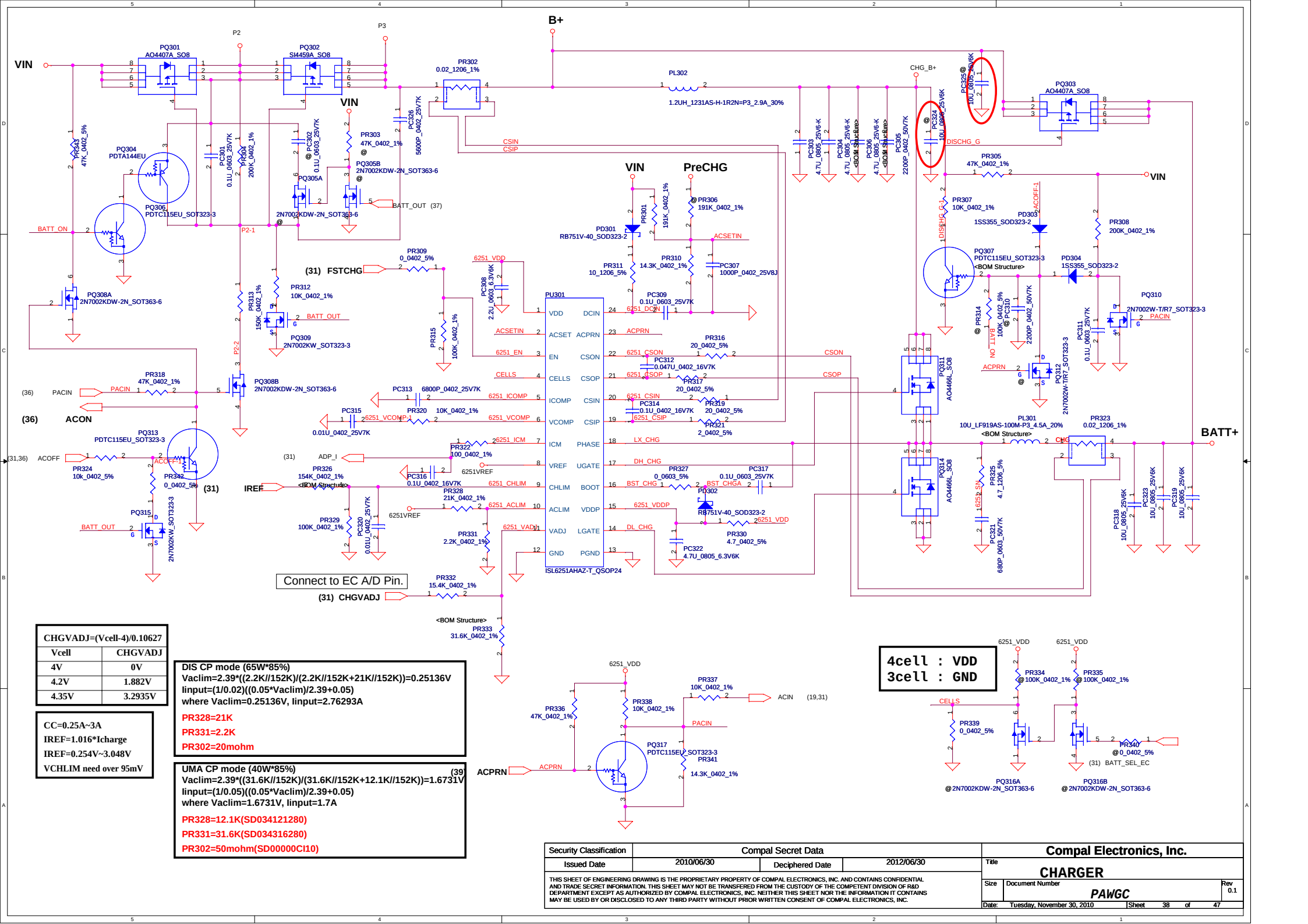
Compal Electronics, Inc.

Title: BATTERY CONN/OTP

Size: Custom | Document Number: PAWGC | Rev: 0.1

Date: Tuesday, November 30, 2010 | Sheet 37 of 47



CHGVADJ=(Vcell-4)/0.10627	
Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

CC=0.25A~3A
IREF=1.016*Icharge
IREF=0.254V~3.048V
VCHLIM need over 95mV

DIS CP mode (65W*85%)
Vaclim=2.39*((2.2K//152K)/(2.2K//152K+21K//152K))=0.25136V
Iinput=(1/0.02)((0.05*Vaclim)/2.39+0.05)
where Vaclim=0.25136V, Iinput=2.76293A
PR328=21K
PR331=2.2K
PR302=20mohm

UMA CP mode (40W*85%) (39
Vaclim=2.39*((31.6K//152K)/(31.6K//152K+12.1K//152K))=1.6731V
Iinput=(1/0.05)((0.05*Vaclim)/2.39+0.05)
where Vaclim=1.6731V, Iinput=1.7A
PR328=12.1K(SD034121280)
PR331=31.6K(SD034316280)
PR302=50mohm(SD00000CI10)

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Issued Date	2010/06/30	Deciphered Date	2012/06/30

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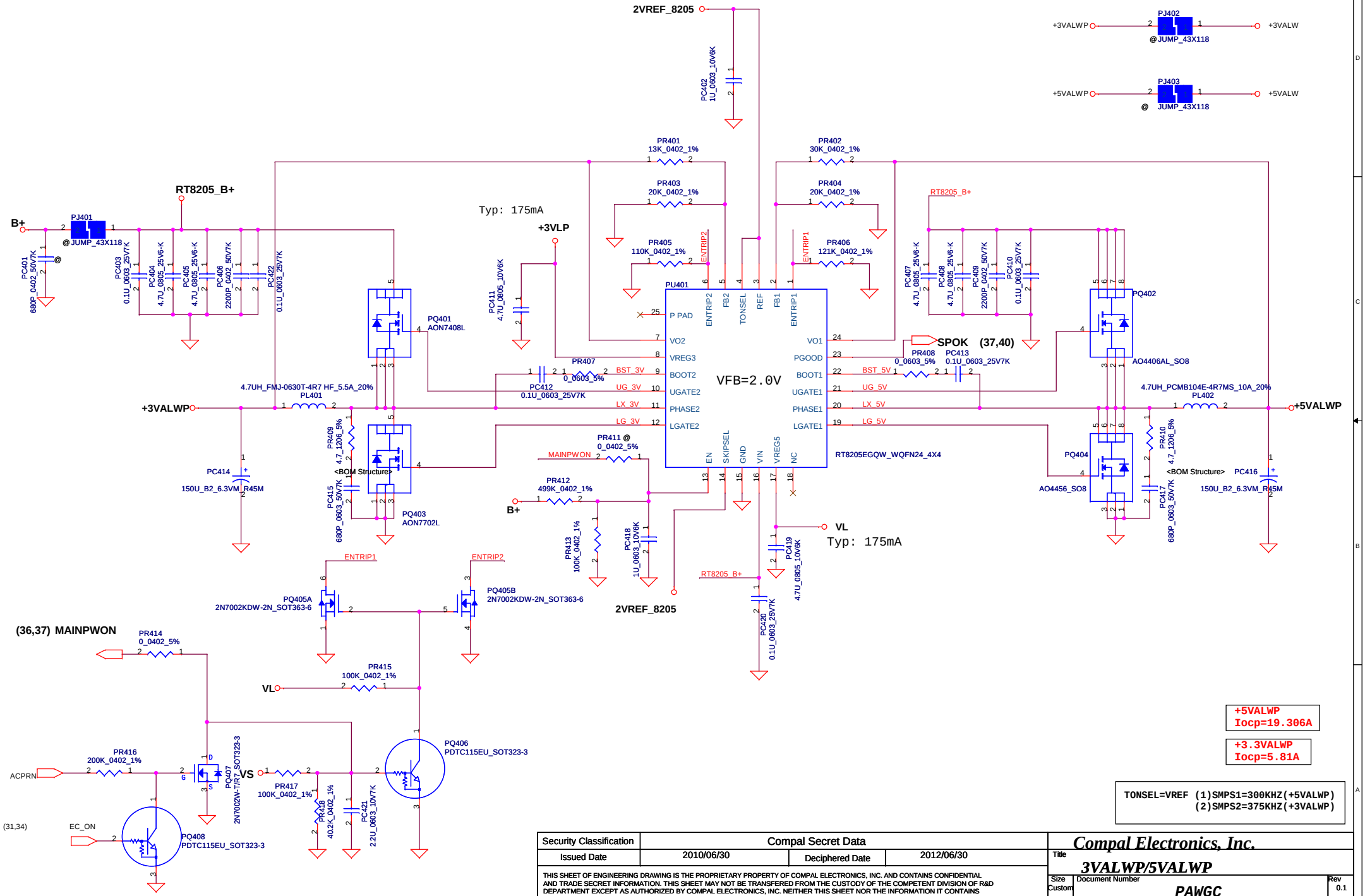
Compal Electronics, Inc.

Title: **CHARGER**

Size	Document Number	Rev
	PAWGC	0.1

Date: Tuesday, November 30, 2010 | Sheet 38 of 47

Note:
Use TPS51125 IC can remove RTC refernece LDO
Use TPS51427 IC must keep RTC refernece LDO



Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2012/06/30

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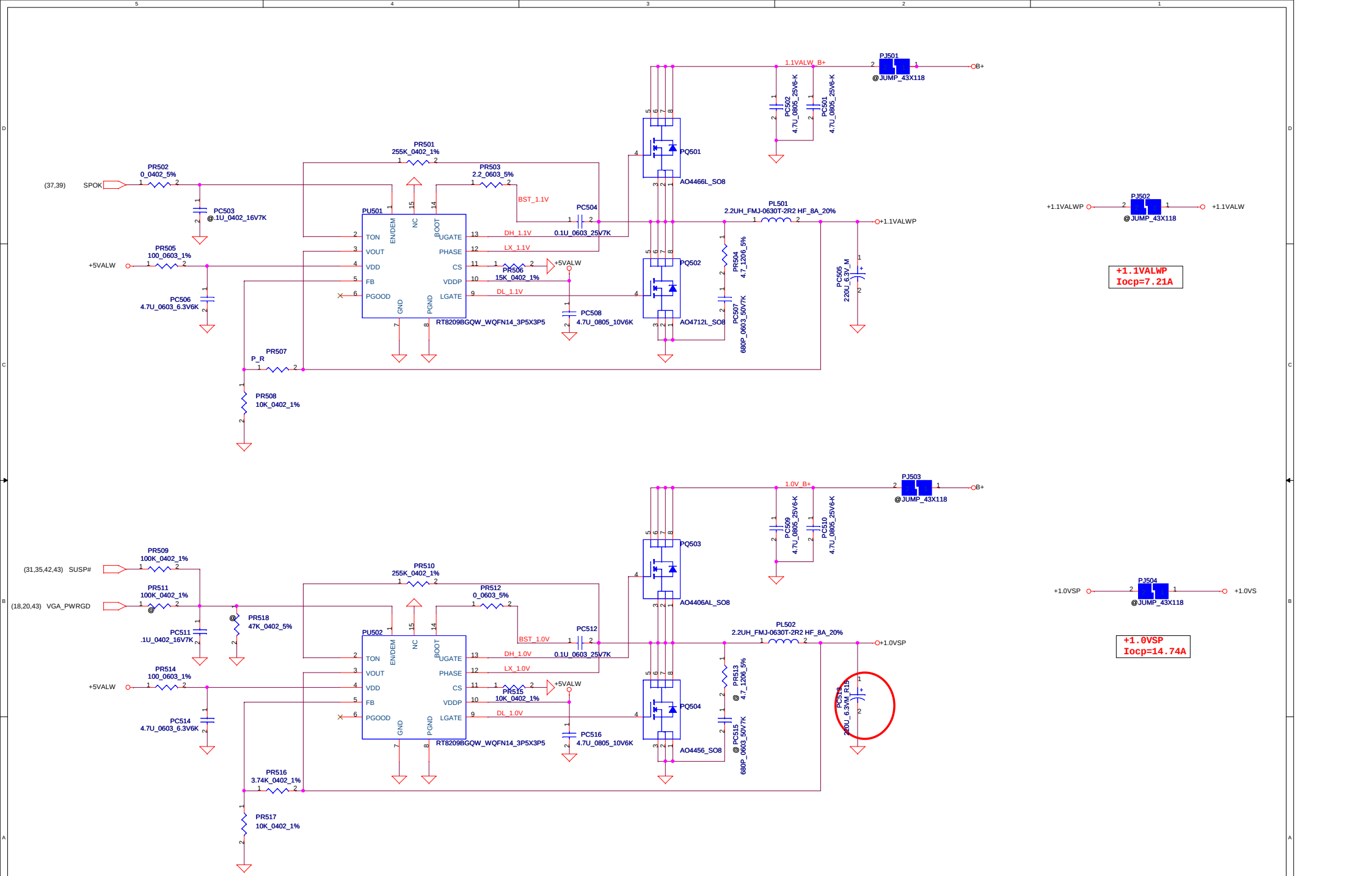
Compal Electronics, Inc.

Title: 3VALWP/5VALWP

Size	Document Number	Rev
Custom	PAWGC	0.1

Date: Tuesday, November 30, 2010 Sheet 39 of 47



Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2012/06/30

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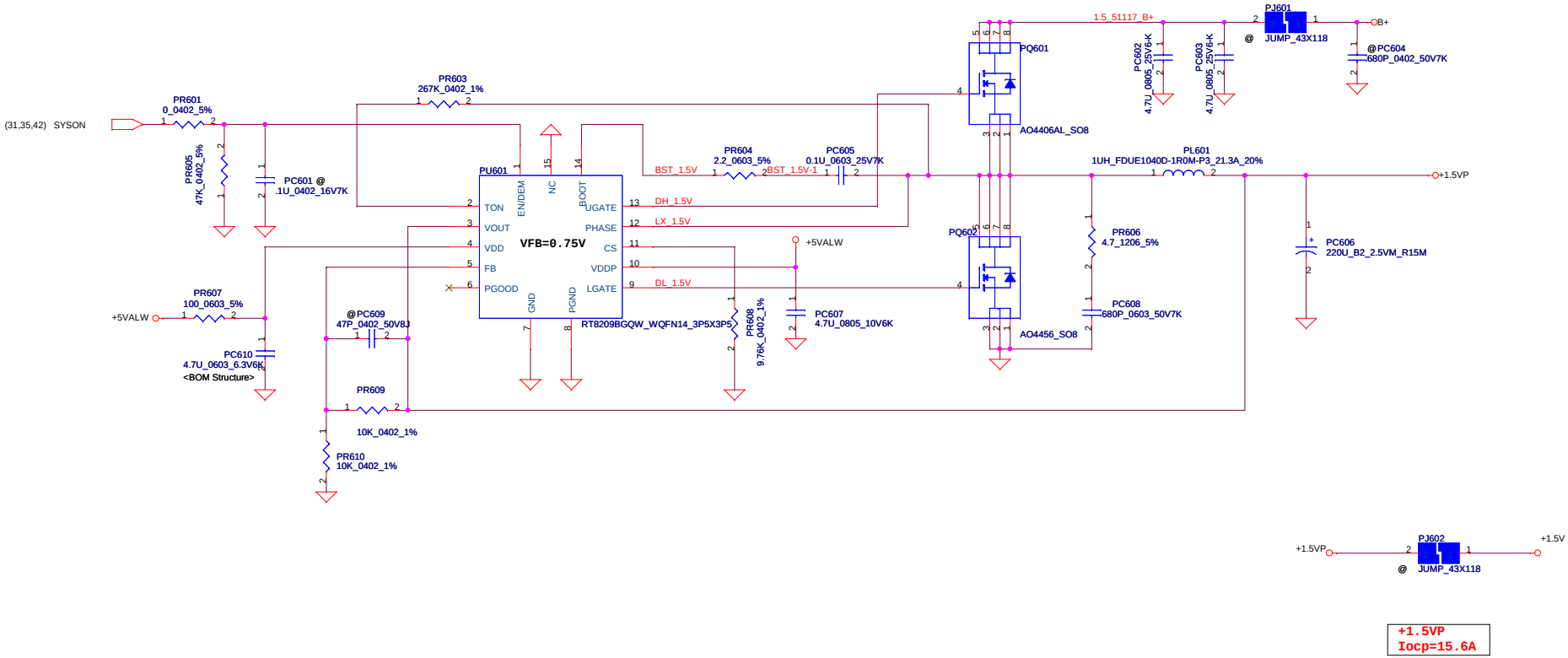
Compal Electronics, Inc.

Title: **+1.1VALWP/+1.0VSP**

Size	Document Number	Rev
	PAWGC	0.1

Date: Tuesday, November 30, 2010 | Sheet 40 of 47



+1.5VP
Iocp=15.6A

Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2012/06/30

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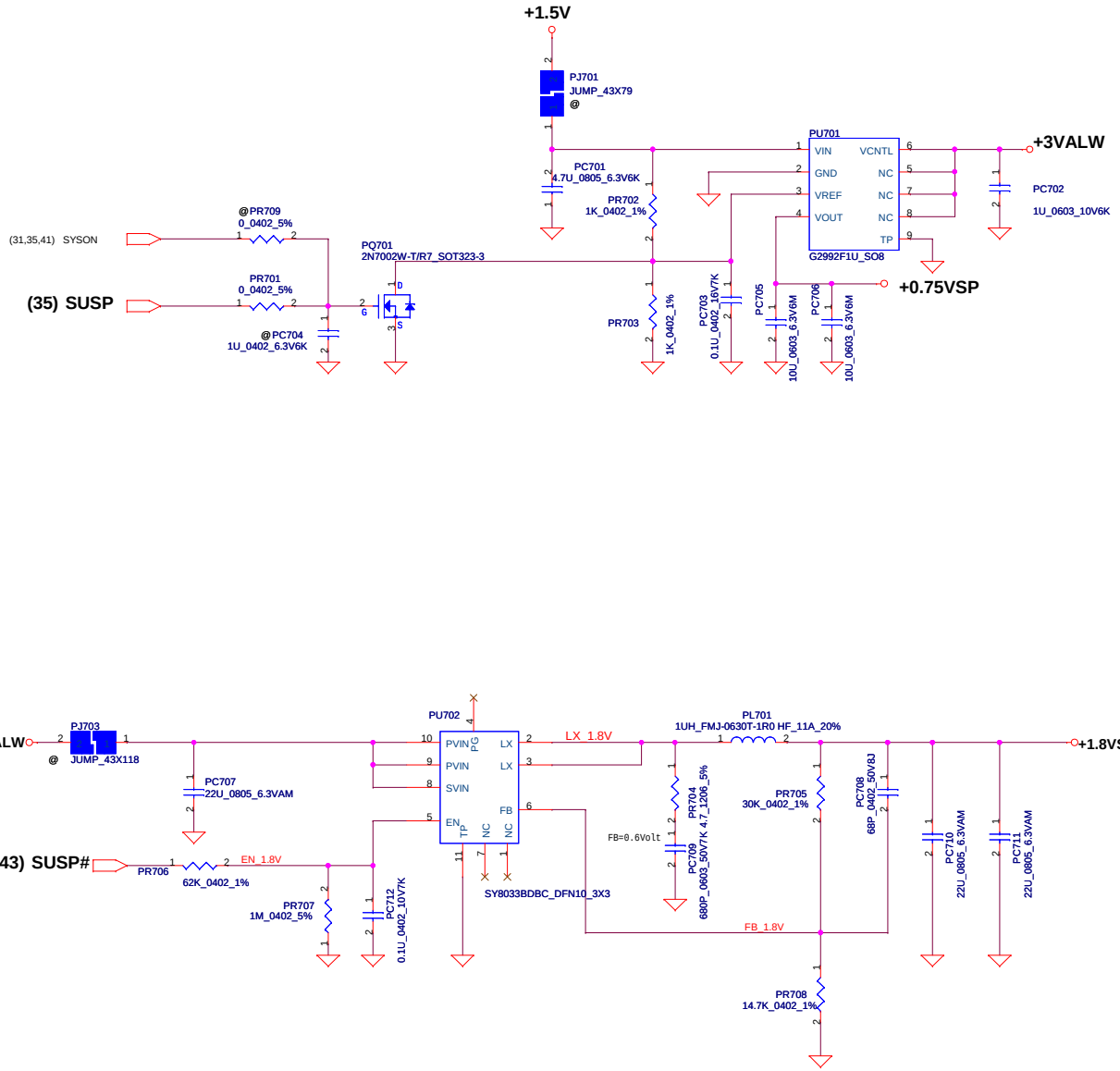
Compal Electronics, Inc.

Title: **1.5VP**

Size	Document Number	Rev
	PAWGC	0.1

Date: Tuesday, November 30, 2010 | Sheet 41 of 47



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Issued Date	2010/06/30	Deciphered Date	2012/06/30

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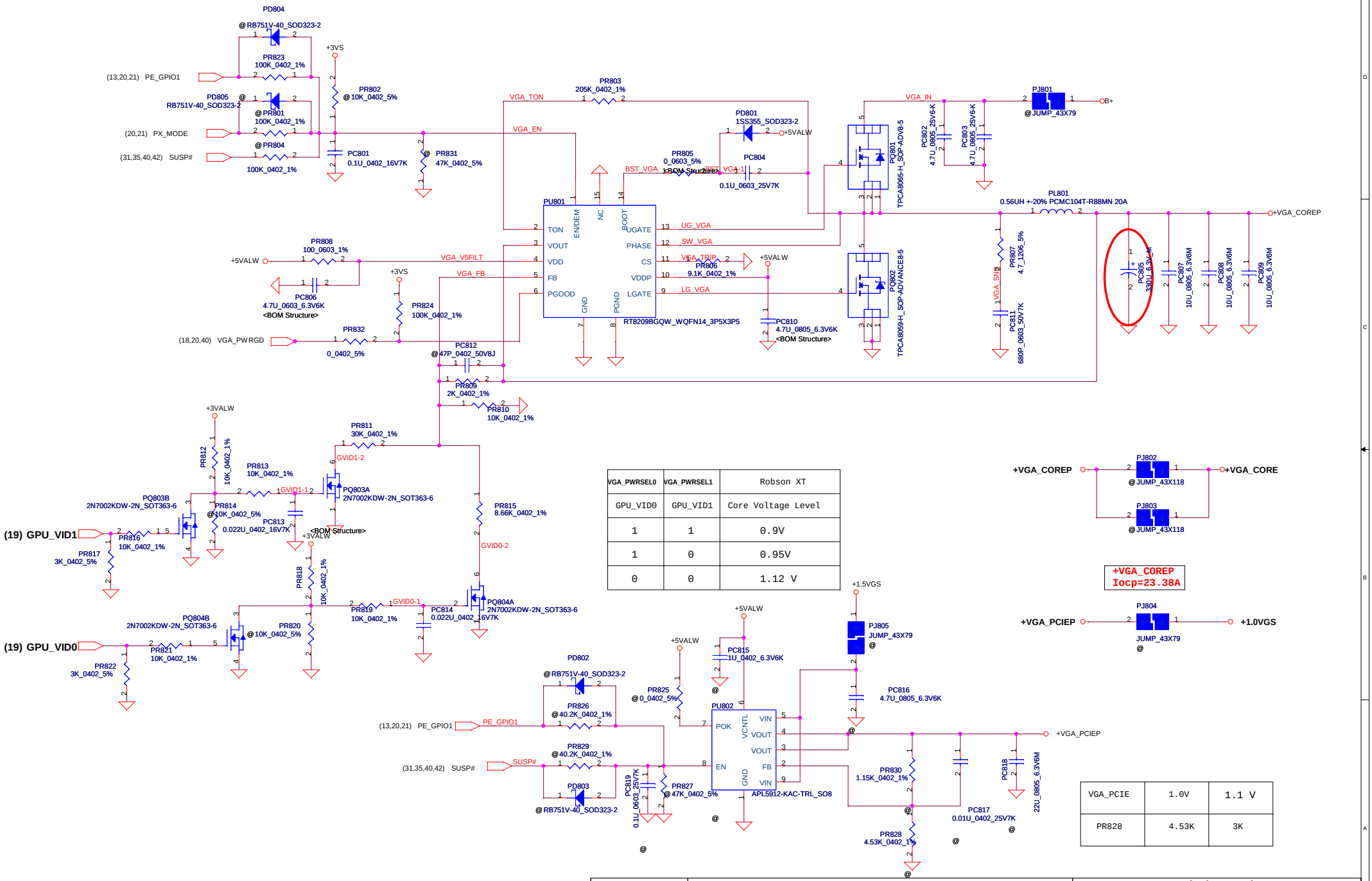
Compal Electronics, Inc.			
Title	0.75VP/1.8VP		
Size	Document Number	PAWGC	Rev 0.1
Date: Tuesday, November 30, 2010	Sheet 42 of 47		



VGA_PWRSEL0	VGA_PWRSEL1	Robson XT
GPU_VID0	GPU_VID1	Core Voltage Level
1	1	0.9V
1	0	0.95V
0	0	1.12 V

VGA_PCIE	1.0V	1.1 V
PR828	4.53K	3K

Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2012/06/30

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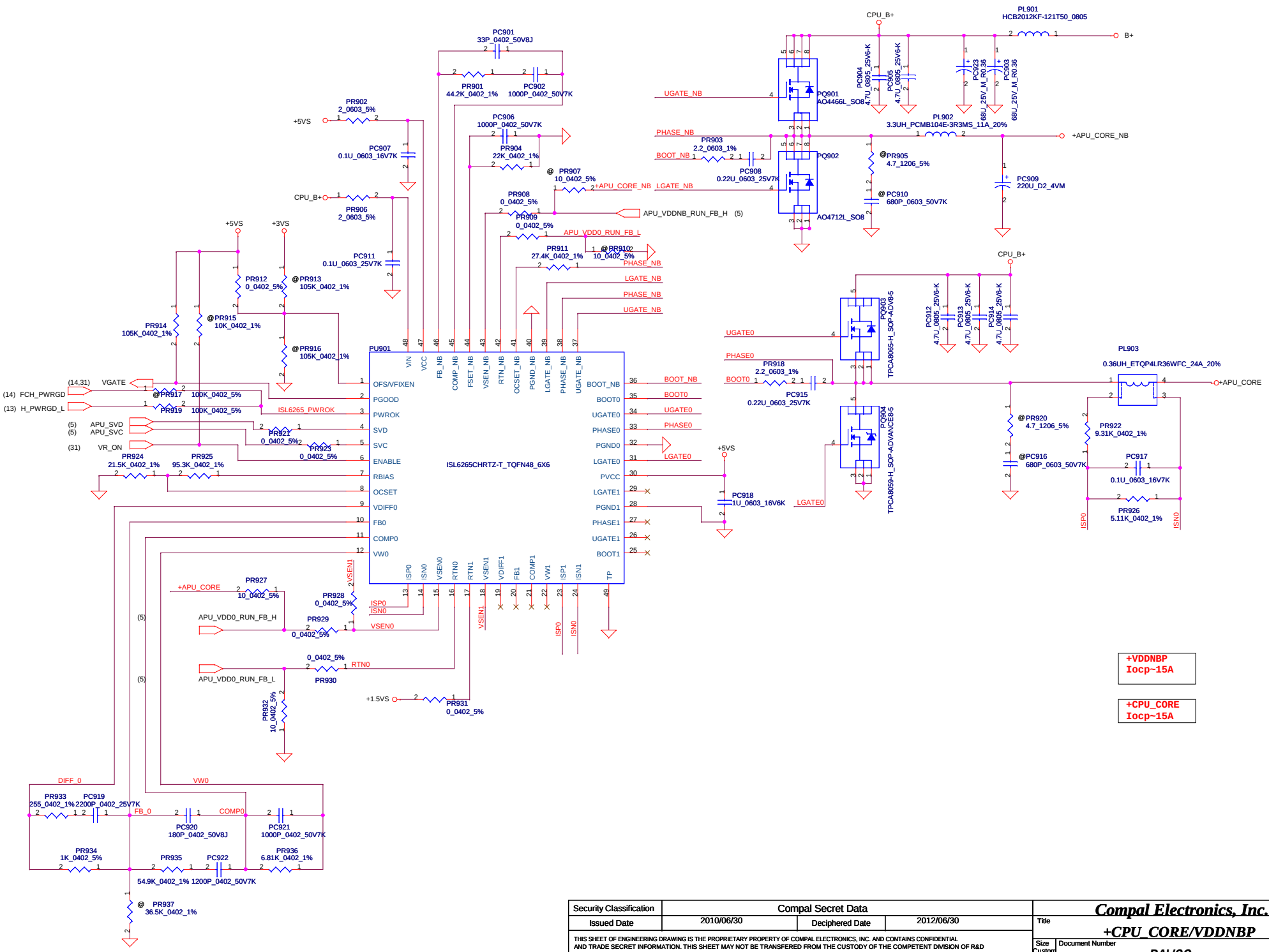
Compal Electronics, Inc.			
Title	VGA_COREP		
Size	Document Number	PAWGC	Rev 0.1
Date: Tuesday, November 30, 2010	Sheet 43 of 47		



Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2012/06/30

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Compal Electronics, Inc.

Title: +CPU_CORE/VDDNBP

Size	Document Number	Rev
Custom	PAWGC	0.1

Date: Tuesday, November 30, 2010 | Sheet 44 of 47

Version Change List (P. I. R. List) for Power Circuit

Page#	Title	Date	Request Owner	Issue Description	Solution Description
	power sequence	2010/07/30	HW		PR701 change to 0 ohm and PC704 non mount.
	Add PU802 for AMD's request	2010/09/21	AMD		
	Add PL302,PC324 and PC325 for EMC Solution.	2010/10/04	EMC		change PJ301 to PL302.
	Add PC422 for EMC Solution.	2010/10/06	EMC		
	Add PQ204 for EM6.0 battery learning function.	2010/11/12	PWR		

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Issued Date	2010/06/30	Deciphered Date	2012/06/30

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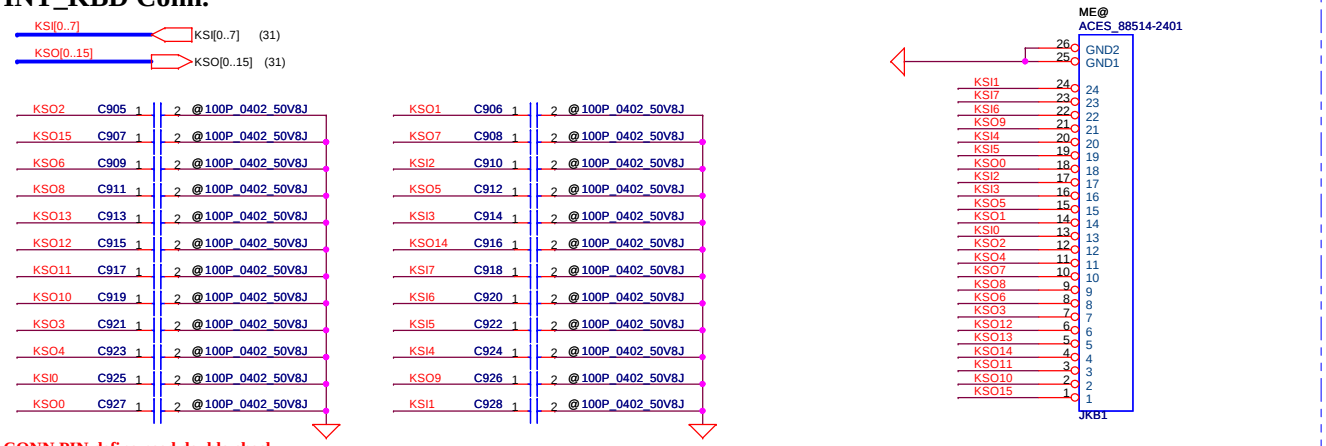
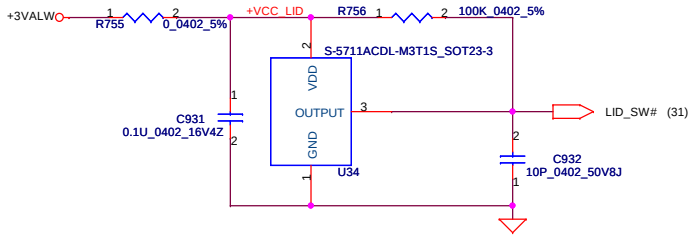
INT_KBD Conn.

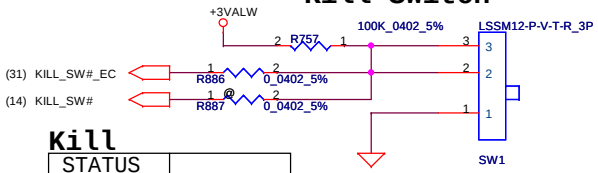


CONN PIN define need double check

Lid Switch



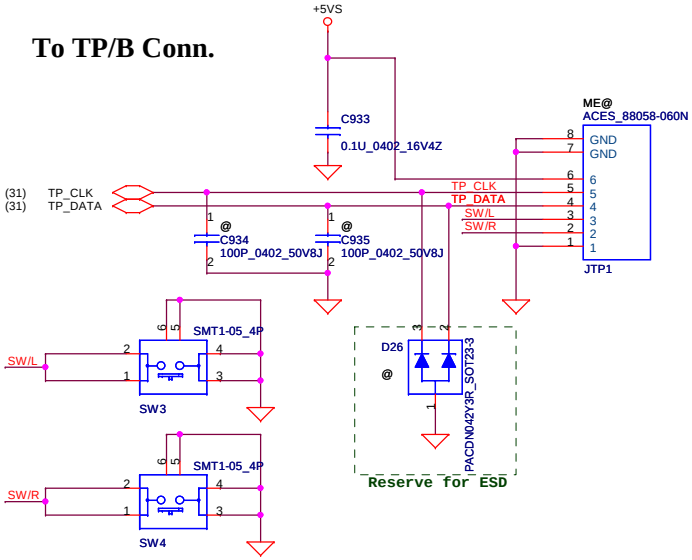
Kill Switch



Kill

STATUS	
1,2(LOW)	OFF
2,3(HI)	ON

To TP/B Conn.



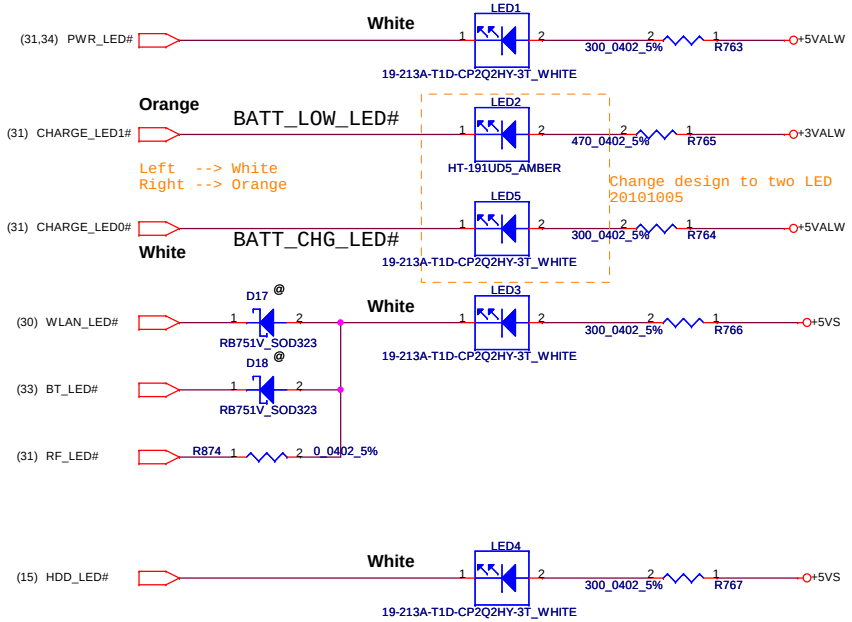
ZZZ PCB

ZZZ1 LA6755P <BOM Structure>

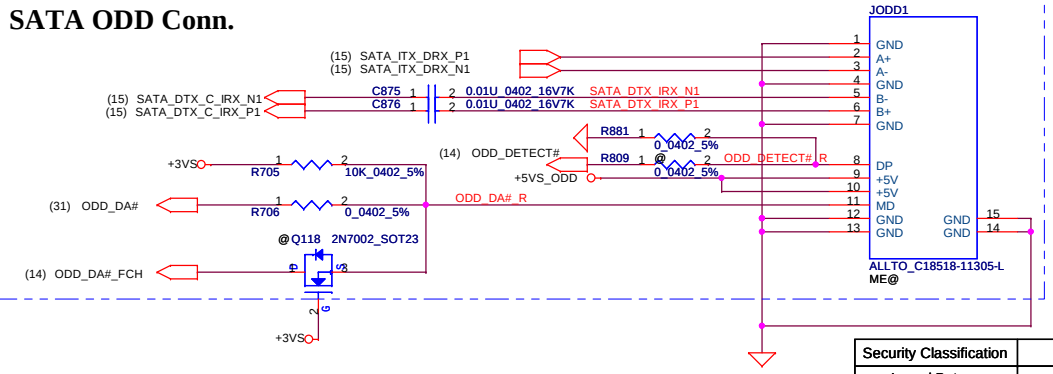
ZZZ2 CR2032_0 <BOM Structure>

ZZZ3 CR2032_0 <BOM Structure>

LED



SATA ODD Conn.



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Issued Date	2010/06/30	Deciphered Date	2012/06/30

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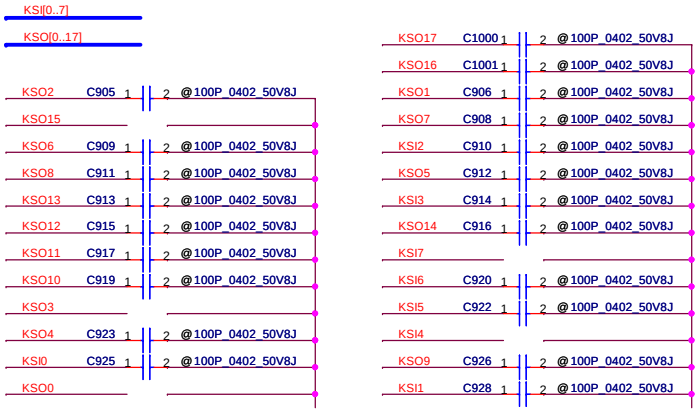
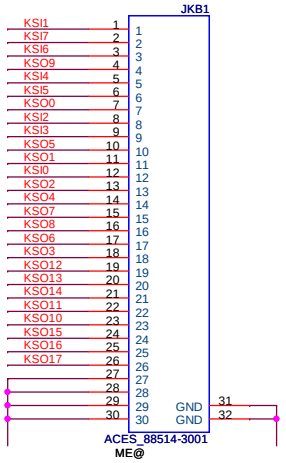
Compal Electronics, Inc.

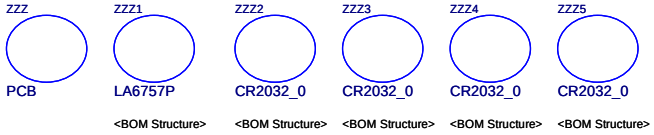
Title: 14" ONLY

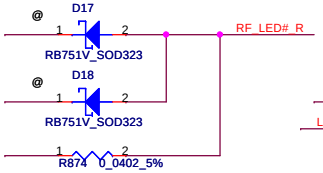
Size: B | Document Number: LA6755P/7P | Rev: 1.0

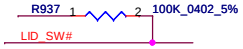
Date: Tuesday, November 30, 2010 | Sheet 46 of 48

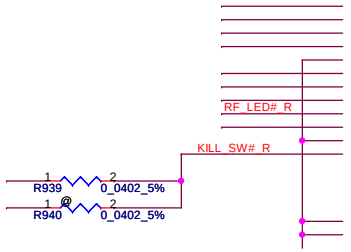


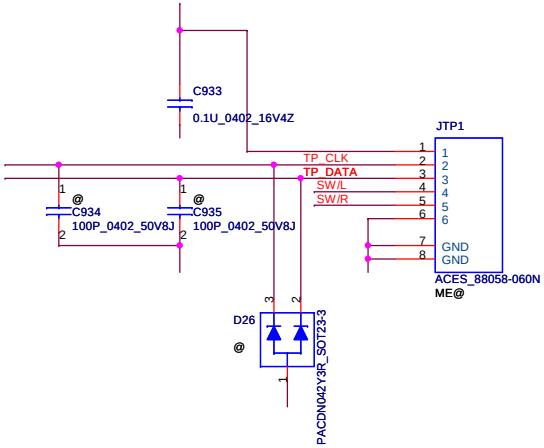


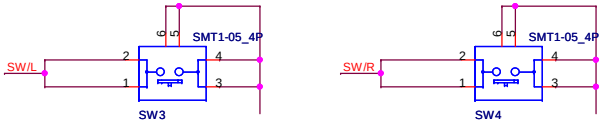


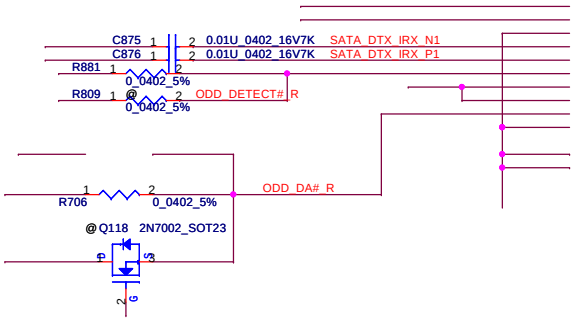












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Compal Electronics, Inc.

Title: 15" ONLY

Size	Document Number	Rev
B	LA6757P	1.0

Date: Tuesday, November 30, 2010 Sheet 46 of 48

PHASE	PAGE	Modification list	PURPOSE
0.2	P08	C643 change to OS-CON type	For cost down purpose
0.2	P10	pop R490, unpop R491	LVDS PWM controls by EC
0.2	P10	Add CE_EN @ JLVDS1.16 and U33.98	For color engine function
0.2	P10	R488 pull-up to +5VALW	For C38 module design
0.2	P10	Add R938	For CMOS cost down purpose
0.2	P12	JCRT1 change foot-print from DC060003O00 to DC060004S00	Foot-print is wrong
0.2	P14	SATA_DET# change from U26.AE19 to U26.AB21	For corresponding SATA port assigned
0.2	P16	Delete R635	Our codec consumes +3V
0.2	P18	Add R936	For VGA_PWRGD reservation
0.2	P20	Q69 ~ Q72 change to N-MOS	Follow BACO suggestion SCH
0.2	P21	R840 pull-up change to +5VALW and R857 change to 20K ohms	For +3VGS sequence design
0.2	P21	Delete Q122, Add U47, C999, R944	For +1.0VGS DC power design
0.2	P23	L27 change to 0 ohms	For new reference circuit
0.2	P23	Delete GND connection of U8.N11 and U8.N12	For new reference circuit
0.2	P21	R344 change to 20K ohms	Prevent Q74 damage
0.2	P28	J7 foot-print update	Base on DFX request
0.2	P28	Add net CLK_PCI_DB_R and unpop R854	for EMI concern
0.2	P28	Modify PC_Beep circuit	Base on vender suggestion
0.2	P23	Delete C421, C422, C431, C432, C433	For new reference circuit
0.2	P31	R734 pull-high change to +5VALW	For USB ports ACIN leakage
0.2	P31	Add BATT_SEL_EC at U33.103	For Battery selection reservation
0.2	P33	Add R941	For further cost down purpose
0.2	P33	Add R942, R943, C998	For SATA_DET# function design
0.2	P28	Delete C851, C855	For useless AGND bridge
0.2	P34	Change JP7 to JPWRB1 and JP8 to JCR1	For standard naming
0.2	P34	Del U45, R890 ~ R899, J12, CHR_ON# (U33.70)	Deleting USB charge function
0.2	P35	Delete C974	Deleting unnecessary part for +1.1VS
0.2	P19	Add R945, R946	For HDMI Audio strap
0.2	P13	Delete T79, T80	For layout space needed for SATA calibration
0.2	P28	Add R947, R948	For EMI solution reservation base on vender suggetion
0.2	P28	Delete C857, R694	To delete redundant part base on vender suggestion
0.2	P28	L57 ~ L60 change to 0_0603_5%	Base on vender suggestion
0.2	P28	R672 change to 0ohm and location to be series on HDA_BITCLK_AUDIO	For EMI solution reservation base on vender suggetion
0.2	P14	Kill_SW# change from U26.G24 to U26.K1	Kill_SW# function needs event pin
0.2	P31	Add R949, C1002	Requirement of implementing SUSCLK
0.2	P28	Add R950 @ +3VS, R951 @ +LDO_OUT_3.3V, R952 @ +5VS	For customer request (PWR consumption)
0.2	P28	Add R953	For PC Beep circuit
0.2	P29	Add R954, R955	For customer request (PWR consumption)
0.2	P13 P18	Add C1003, U48, R956, R957 Delete R556, R841, R889, D28	For PX GPU_RST# function
0.2	P05	Add R958	For enabling HDMI function
0.2	P28	Add R959	For EMI reservation
0.2	P32	Add R960 and c1004	For EMI reservation
0.2	P09	Add R961 and R962	For DDR SO-DIMMB strap pin reservation
0.2	P05	Delete T74, T75	For layout limitation
0.3	P29 P46	change +5V_ODD to +5VS_ODD	For better net name
0.3	P32	R760 change to 100ohm bead and R761 change back to 15ohm resistor	For correct EMI solution
0.3	P21	U47 change to SB00000GV00 footprint	For correct symbol
0.3	P05	R958 change to HDMI@ and R422 change to nonHDMI@	For SKU without HDMI function
0.3	P21	Add PX_MODE off page	For design correction

Change footprint
20100812 : For cost down purpose to change parts

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PHASE	PAGE	Modification list	PURPOSE
0.2	P08	C643 change to OS-CON type	For cost down purpose
0.2	P10	pop R490, unpop R491	LVDS PWM controls by EC
0.2	P10	Add CE_EN @ JLVDS1.16 and U33.98	For color engine function
0.2	P10	R488 pull-up to +5VALW	For C38 module design
0.2	P10	Add R938	For CMOS cost down purpose
0.2	P12	JCRT1 change foot-print from DC060003O00 to DC060004S00	Foot-print is wrong
0.2	P14	SATA_DET# change from U26.AE19 to U26.AB21	For corresponding SATA port assigned
0.2	P16	Delete R635	Our codec consumes +3V
0.2	P18	Add R936	For VGA_PWRGD reservation
0.2	P20	Q69 ~ Q72 change to N-MOS	Follow BACO suggestion SCH
0.2	P21	R840 pull-up change to +5VALW and R857 change to 20K ohms	For +3VGS sequence design
0.2	P21	Delete Q122, Add U47, C999, R944	For +1.0VGS DC power design
0.2	P23	L27 change to 0 ohms	For new reference circuit
0.2	P23	Delete GND connection of U8.N11 and U8.N12	For new reference circuit
0.2	P21	R344 change to 20K ohms	Prevent Q74 damage
0.2	P28	J7 foot-print update	Base on DFX request
0.2	P28	Add net CLK_PCI_DB_R and unpop R854	for EMI concern
0.2	P28	Modify PC_Beep circuit	Base on vender suggestion
0.2	P23	Delete C421, C422, C431, C432, C433	For new reference circuit
0.2	P31	R734 pull-high change to +5VALW	For USB ports ACIN leakage
0.2	P31	Add BATT_SEL_EC at U33.103	For Battery selection reservation
0.2	P33	Add R941	For further cost down purpose
0.2	P33	Add R942, R943, C998	For SATA_DET# function design
0.2	P28	Delete C851, C855	For useless AGND bridge
0.2	P34	Change JP7 to JPWRB1 and JP8 to JCR1	For standard naming
0.2	P34	Del U45, R890 ~ R899, J12, CHR_ON# (U33.70)	Deleting USB charge function
0.2	P35	Delete C974	Deleting unnecessary part for +1.1VS
0.2	P19	Add R945, R946	For HDMI Audio strap
0.2	P13	Delete T79, T80	For layout space needed for SATA calibration
0.2	P28	Add R947, R948	For EMI solution reservation base on vender suggetion
0.2	P28	Delete C857, R694	To delete redundant part base on vender suggestion
0.2	P28	L57 ~ L60 change to 0_0603_5%	Base on vender suggestion
0.2	P28	R672 change to 0ohm and location to be series on HDA_BITCLK_AUDIO	For EMI solution reservation base on vender suggetion
0.2	P14	Kill_SW# change from U26.G24 to U26.K1	Kill_SW# function needs event pin
0.2	P31	Add R949, C1002	Requirement of implementing SUSCLK
0.2	P28	Add R950 @ +3VS, R951 @ +LDO_OUT_3.3V, R952 @ +5VS	For customer request (PWR consumption)
0.2	P28	Add R953	For PC Beep circuit
0.2	P29	Add R954, R955	For customer request (PWR consumption)
0.2	P13 P18	Add C1003, U48, R956, R957 Delete R556, R841, R889, D28	For PX GPU_RST# function
0.2	P05	Add R958	For enabling HDMI function
0.2	P28	Add R959	For EMI reservation
0.2	P32	Add R960 and c1004	For EMI reservation
0.2	P09	Add R961 and R962	For DDR SO-DIMMB strap pin reservation
0.2	P05	Delete T74, T75	For layout limitation

15 only part

0.2	P46	Add C1000, C1001	For 15" 30pin KB connector

Change footprint
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PHASE	PAGE	Modification list	PURPOSE
0.3	P14	R603 and R604 change to pop	For SM Bus pull-high
0.3	P23	Reserve C1005	For PWR team request reserving a 330u capcitor
0.3	P33	C939 change to 5.9H OS-con	For cost saving
0.3	P33	R902 and R942 change to unpop	For eSATA function deletion
0.3	P29	U32 change PN to SA000046C00	For main source PN concern
0.3	P05	Delete JHDT1	For layout limitation
0.3	P11	Add F2 and change SM-BUS pull high net name to +5VS_HDMI_F	For safety team requirement
0.3	P21	change J3 footprint	For larger jumper footprint
0.3	P21	R856 change from 20K to 39K	For VGA power sequence
0.3	P11	Add net name +5VS_HDMI_F	For power trace indecation
0.3	P20	Change Q69 ~ Q72 PN	For design correction
0.3	P28	Add R963	For 20671-21Z update
0.3	P28	Change U31 PN to SA00003K410	For 20671-21Z PN
0.3	P20	U10.5, U46.5, and U44.5 change from +3VS to +3VGS	For BACO circuit update
0.3	P28	Delete R951	For unnecessary part deletion
0.3	P07	C623 change to unpop	Base on AMD checklist
0.3	P16	Delete C734, add C1006, C1007	For ME concern
0.3	P21	R924 cahgne pull-up from +3VS to +3VALW	For BACO design correction
0.3	P21	R925 change to pop	For BACO design correction
0.3	P14	Reserve C1008 at FCH_PWRGD	For EMI request
0.3	P14	Reserve C1009 at VGATE	For EMI request
0.3	P31	Reserve C1010 at VR_ON	For EMI request
0.3	P13	Reserve C1011 at H_PWRGD_L	For EMI request
0.3	P28	pop C849, C850, R692, R693, R696, C826	For EMI request
0.3	P27	Add C1012, C1013	For EMI request (gas discharge tube)
0.3	P27	Add D1	For EMI request (ESD diode)
0.3	P28	update R672 location	For EMI request (RC to GND for codec BIT_CLK)
0.3	P07	Delete C617	For EMI solution space needed
0.3	P28	Pop D30, D31, unpop R953	For FCH PC-beep function
0.3	P31	R751 and R752 change from 4.7K ohm to 2.2K ohm	For PWR team request
0.3	P13	C719, C720 change from 22P to 18P	For RTC design
14" only part			
0.3	P46	Change one dual-diode LED2 to two single diode LED2 and LED5	For design change
1.0	P5	unpop R415	AMD checklist update
1.0	P10	R486, R487 change pull-high to +5VS	AMD checklist update
1.0	P11	R522, R523 change from 2.2K to 2K	AMD checklist update
1.0	P12	reserve R964, R965, change R546 ~ R549 from 4.7K to 2K	AMD checklist update
1.0	P31	BATT_LEN# added to U33.38	PWR team request
1.0	P20	Delete R341	For design update
1.0	P21	Delete R837, R832, R836	For design update
1.0	P28	Delete R947, R948, R950, R952	For design update
1.0	P29	Delete R955, R954, R810	For design update
1.0	P30	unpop C887, C888	For design update
1.0	P25	unpop C494, C484, C498, C482, C490	For design update

Change footprint
20100812 : For cost down purpose to change parts

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PHASE	PAGE	Modification list	PURPOSE
0.3	P29 P46	change +5V_ODD to +5VS_ODD	For better net name
0.3	P32	R760 change to 100ohm bead and R761 change back to 15ohm resistor	For correct EMI solution
0.3	P21	U47 change to SB000000GV00 footprint	For correct symbol
0.3	P05	R958 change to HDMI@ and R422 change to nonHDMI@	For SKU without HDMI function
0.3	P21	Add PX_MODE off page	For design correction
0.3	P14	R603 and R604 change to pop	For SM Bus pull-high
0.3	P23	Reserve C1005	For PWR team request reserving a 330u capcitor
0.3	P33	C939 change to 5.9H OS-con	For cost saving
0.3	P33	R902 and R942 change to unpop	For eSATA function deletion
0.3	P29	U32 change PN to SA000046C00	For main source PN concern
0.3	P05	Delete JHDT1	For layout limitation
0.3	P11	Add F2 and change SM-BUS pull high net name to +5VS_HDMI_F	For safety team requirement
0.3	P21	change J3 footprint	For larger jumper footprint
0.3	P21	R856 change from 20K to 39K	For VGA power sequence
0.3	P11	Add net name +5VS_HDMI_F	For power trace indecation
0.3	P20	Change Q69 ~ Q72 PN	For design correction
0.3	P28	Add R963	For 20671-21Z update
0.3	P28	Change U31 PN to SA00003K410	For 20671-21Z PN
0.3	P20	U10.5, U46.5, and U44.5 change from +3VS to +3VGS	For BACO circuit update
0.3	P28	Delete R951	For unnecessary part deletion
0.3	P07	C623 change to unpop	Base on AMD checklist
0.3	P16	Delete C734, add C1006, C1007	For ME concern
0.3	P21	R924 cahgne pull-up from +3VS to +3VALW	For BACO design correction
0.3	P21	R925 change to pop	For BACO design correction
0.3	P14	Reserve C1008 at FCH_PWRGD	For EMI request
0.3	P14	Reserve C1009 at VGATE	For EMI request
0.3	P31	Reserve C1010 at VR_ON	For EMI request
0.3	P13	Reserve C1011 at H_PWRGD_L	For EMI request
0.3	P28	pop C849, C850, R692, R693, R696, C826	For EMI request
0.3	P27	Add C1012, C1013	For EMI request (gas discharge tube)
0.3	P27	Add D1	For EMI request (ESD diode)
0.3	P28	update R672 location	For EMI request (RC to GND for codec BIT_CLK)
0.3	P07	Delete C617	For EMI solution space needed
0.3	P28	Pop D30, D31, unpop R953	For FCH PC-beep function
0.3	P31	R751 and R752 change from 4.7K ohm to 2.2K ohm	For PWR team request
0.3	P13	C719, C720 change from 22P to 18P	For RTC design
1.0	P5	unpop R415	AMD checklist update
1.0	P10	R486, R487 change pull-high to +5VS	AMD checklist update
1.0	P11	R522, R523 change from 2.2K to 2K	AMD checklist update
1.0	P12	Add R964, R965, change R548, R549 from 4.7K to 2K unpop R546, R547, Q89	AMD checklist update
1.0	P31	BATT_LEN# added to U33.38	PWR team request
1.0	P46	Kill_SW#_R change from JLED1.5 to JLED1.12	Design change update
1.0	P20	Delete R341	For design update
1.0	P21	Delete R837, R832, R836	For design update
1.0	P28	Delete R947, R948, R950, R952	For design update
1.0	P29	Delete R955, R954, R810	For design update
1.0	P30	unpop C887, C888	For design update
1.0	P25	unpop C494, C484, C498, C482, C490	For design update

Change footprint
20100812 : For cost down purpose to change parts

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