TDA8948J

4-channel audio amplifier

Rev. 01 — 27 February 2008 Product data sheet

1. General description

The TDA8948J contains four identical audio power amplifiers. The TDA8948J can be used as four Single-Ended (SE) channels with a fixed gain of 26 dB, two times Bridge-Tied Load (BTL) channels with a fixed gain of 32 dB or two times SE channels (26 dB gain) plus one BTL channel (32 dB gain) operating as a 2.1 system.

The TDA8948J comes in a 17-pin Dil-Bent-Sil (DBS) power package. The TDA8948J is pin compatible with the TDA8944AJ, TDA8946AJ and TDA8947J.

The TDA8948J contains a unique protection circuit that is solely based on multiple temperature measurements inside the chip. This gives maximum output power for all supply voltages and load conditions with no unnecessary audio holes. Almost any supply voltage and load impedance combination can be made as long as thermal boundary conditions (number of channels used, external heat sink and ambient temperature) allow it.

2. Features

2.1 Functional features

- SE: 1 W to 18 W, BTL: 4 W to 36 W operation possibility (2.1 system)
  Soft clipping.
- Standby and mute mode.
- No on/off switching plops.
- Low standby current.
- High supply voltage ripple rejection.
- Outputs short-circuit protected to ground, supply and across the load.
- Thermally protected.
- Pin compatible with TDA8944AJ, TDA8946AJ and TDA8947J.

3. Applications

- Television
- PC speakers
- Boom box
- Mini and micro audio receivers

4. Quick reference data

Table 1. Quick reference data

SE: V_{CC} = 17 V; T_{amb} = 25 °C; R_L = 4 Ω; f_i = 1 kHz; V_{MODE1} = V_{CC}; V_{MODE2} = V_{CC}; measured in test circuit Figure 11; unless otherwise specified.
BTL: V_{CC} = 17 V; T_{amb} = 25 °C; R_L = 8 Ω; f = 1 kHz; V_{MODE1} = V_{CC}; V_{MODE2} = V_{CC}; measured in test circuit Figure 11; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{CC}	supply voltage	operating	[1]	9	17	26	V
		no (clipping signal)	[2]	-	-	28	V
I_q	quiescent current	V_{CC} = 17 V; R_L = ∞	[3]	-	100	145	mA
I_{stb}	standby current	-		-	-	10	µA
$P_{o(SE)}$	SE output power	V_{CC} = 17 V; see Figure 7:					
		THD = 10 %; R_L = 4 Ω		6.5	8	-	W
		THD = 0.5 %; R_L = 4 Ω		-	6	-	W
		V_{CC} = 20 V:					
		THD = 10 %; R_L = 4 Ω		-	12	-	W
$P_{o(BTL)}$	BTL output power	V_{CC} = 17 V; see Figure 7:					
		THD = 10 %; R_L = 8 Ω		14	16	-	W
		THD = 0.5 %; R_L = 8 Ω		-	12	-	W
		V_{CC} = 20 V:					
		THD = 10 %; R_L = 8 Ω		-	24	-	W
THD	total harmonic distortion	SE; P_o = 1 W		-	0.1	0.5	%
		BTL; P_o = 1 W		-	0.05	0.5	%
G_v	voltage gain	SE		25	26	27	dB
		BTL		31	32	33	dB
SVRR	supply voltage ripple rejection	SE:					
		f_{ripple} = 1 kHz	[4]	-	60	-	dB
		f_{ripple} = 100 Hz to 20 kHz	[4]	-	60	-	dB
		BTL:					
		f_{ripple} = 1 kHz	[4]	-	65	-	dB
		f_{ripple} = 100 Hz to 20 kHz	[4]	-	65	-	dB

[1] A minimum load is required at supply voltages of V_{CC} > 22 V; R_L = 3 Ω for SE and R_L = 6 Ω for BTL.

[2] The amplifier can deliver output power with non-clipping output signals into nominal loads as long as the ratings of the IC are not exceeded.

[3] With a load connected at the outputs the quiescent current will increase.

[4] Supply voltage ripple rejection is measured at the output with a source impedance R_{SOURCE} = 0 Ω at the input and with a frequency range from 20 Hz to 22 kHz (unweighted). The ripple voltage is a sine wave with a frequency f_{ripple} and an amplitude of 300 mV (RMS), which is applied to the positive supply rail.

5. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
TDA8948J	DBS17P	DBS17P: plastic DIL-bent-SIL power package; 17 leads (lead length 12 mm)	SOT243-1

6. Block diagram

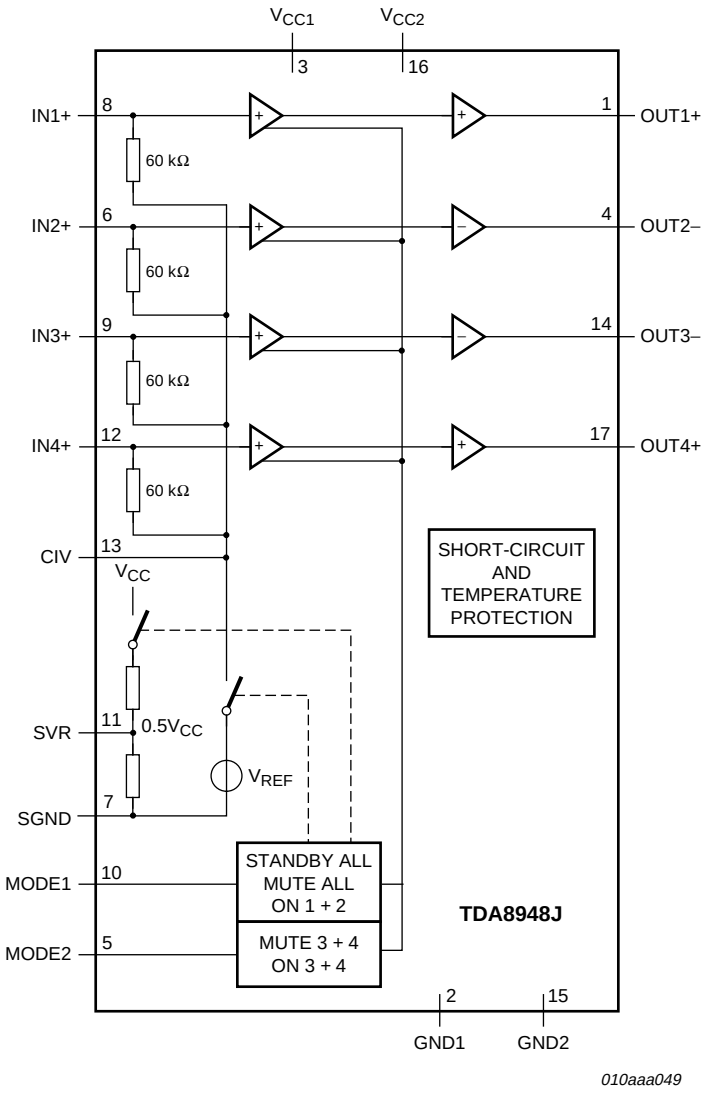


Fig 1. Block diagram

7. Pinning information

7.1 Pinning

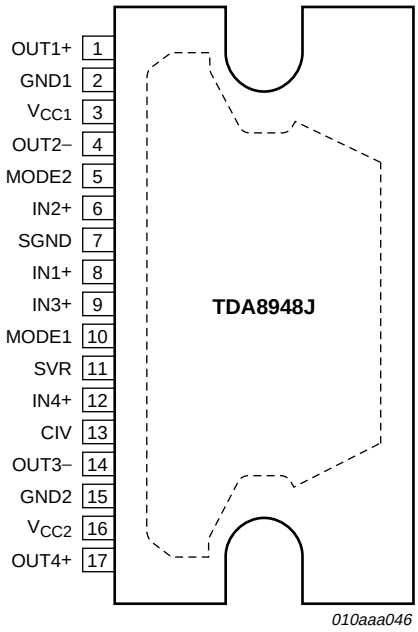


Fig 2. Pin configuration diagram

7.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
OUT1+	1	non inverted loudspeaker output of channel 1
GND1	2	ground of channels 1 and 2
V_{CC1}	3	supply voltage channels 1 and 2
OUT2–	4	inverted loudspeaker output of channel 2
MODE2	5	mode selection 2 input: Mute and On mode for channels 3 and 4
IN2+	6	input channel 2
SGND	7	signal ground
IN1+	8	input channel 1
IN3+	9	input channel 3
MODE1	10	mode selection 1 input: Standby, Mute and On mode for all channels
SVR	11	half supply voltage decoupling (ripple rejection)
IN4+	12	input channel 4
CIV	13	common input voltage decoupling
OUT3–	14	inverted loudspeaker output of channel 3

Table 3. Pin description *...continued*

Symbol	Pin	Description
GND2	15	ground of channels 3 and 4
V_{CC2}	16	supply voltage channels 3 and 4
OUT4+	17	non inverted loudspeaker output of channel 4

8. Functional description

8.1 Input configuration

The input cut-off frequency is:

$$f_{i(cut-off)} = \frac{1}{2\pi(R_i \times C_i)} \quad (1)$$

For SE application R_i = 60 kΩ and C_i = 220 nF:

$$f_{i(cut-off)} = \frac{1}{2\pi(60 \times 10^3 \times 220 \times 10^{-9})} = 12 \text{ Hz} \quad (2)$$

For BTL application R_i = 30 kΩ and C_i = 470 nF:

$$f_{i(cut-off)} = \frac{1}{2\pi(30 \times 10^3 \times 470 \times 10^{-9})} = 11 \text{ Hz} \quad (3)$$

As shown in Equation 2 and Equation 3, large capacitor values for the inputs are not necessary, so the switch-on delay during charging of the input capacitors can be minimized. This results in a good low frequency response and good switch-on behavior.

8.2 Power amplifier

The power amplifier is a BTL and/or SE amplifier with an all-NPN output stage, capable of delivering a peak output current of 4 A.

Using the TDA8948J as a BTL amplifier offers the following advantages:

- Low peak value of the supply current
- Ripple frequency on the supply voltage is twice the signal frequency
- No expensive DC-blocking capacitor
- Good low frequency performance

8.2.1 Output power measurement

The output power as a function of the supply voltage is measured on the output pins at THD = 10 %; see Figure 7.

The maximum output power is limited by the supply voltage (V_{CC} = 26 V) and the maximum output current (I_O = 4 A repetitive peak current).

For supply voltages V_{CC} > 22 V, a minimum load is required; see Figure 5:

- SE: R_L = 3 Ω
- BTL: R_L = 6 Ω

8.2.2 Headroom

Typical CD music requires at least 12 dB (factor 15.85) dynamic headroom, compared to the average power output, for transferring the loudest parts without distortion.

The Average Listening Level (ALL) music power, without any distortion, yields:

- SE at $P_{o(SE)}$ = 5 W, V_{CC} = 17 V, R_L = 4 Ω and THD = 0.2 %:

$$P_{o(ALL)SE} = \frac{5 \cdot 10^3}{15.85} = 315 \text{ mW} \quad (4)$$

- BTL at $P_{o(BTL)}$ = 10 W, V_{CC} = 17 V, R_L = 8 Ω and THD = 0.1 %:

$$P_{o(ALL)BTL} = \frac{10 \cdot 10^3}{15.85} = 630 \text{ mW} \quad (5)$$

The power dissipation can be derived from Figure 8 (SE and BTL) for a headroom of 0 dB and 12 dB, respectively.

Table 4. Power rating as function of headroom

Headroom	Power output		Power dissipation (all channels driven)
	SE	BTL	
0 dB	P_o = 5 W	P_o = 10 W	P = 17 W
12 dB	$P_{o(ALL)}$ = 315 mW	$P_{o(ALL)}$ = 630 mW	P = 9 W

For heat sink calculation at the average listening level, a power dissipation of 9 W can be used.

8.3 Mode selection

The TDA8948J has three functional modes which can be selected by applying the proper DC voltage to pin MODE1.

Standby - The current consumption is very low and the outputs are floating. The device is in standby mode when V_{MODE1} < 0.8 V, or when the MODE1 pin is grounded. In standby mode, the function of pin MODE2 has been disabled.

Mute - The amplifier is DC-biased, but not operational (no audio output). This allows the input coupling capacitors to be charged to avoid pop-noise. The device is in mute mode when 4.5 V < V_{MODE1} < (V_{CC} - 3.5 V).

On - The amplifier is operating normally. The on mode is activated at $V_{MODE1} > (V_{CC} - 2.0\ V)$. The output of channels 3 and 4 can be set to mute or on mode.

The output channels 3 and 4 can be switched on/off by applying a proper DC voltage to pin MODE2, under the condition that the output channels 1 and 2 are in the on mode (see Figure 3).

Table 5. Mode selection

Voltage on pin		Channel 1 and 2	Channel 3 and 4 (sub woofer)
MODE1	**MODE2**		
0 V to 0.8 V	0 V to V_{CC}	Standby mode	Standby mode
4.5 V to (V_{CC} – 3.5 V)	0 V to V_{CC}	Mute mode	Mute mode
(V_{CC} – 2.0 V) to V_{CC}	0 V to (V_{CC} – 3.5 V)	On mode	Mute mode
	(V_{CC} – 2 V) to V_{CC}	On mode	On mode

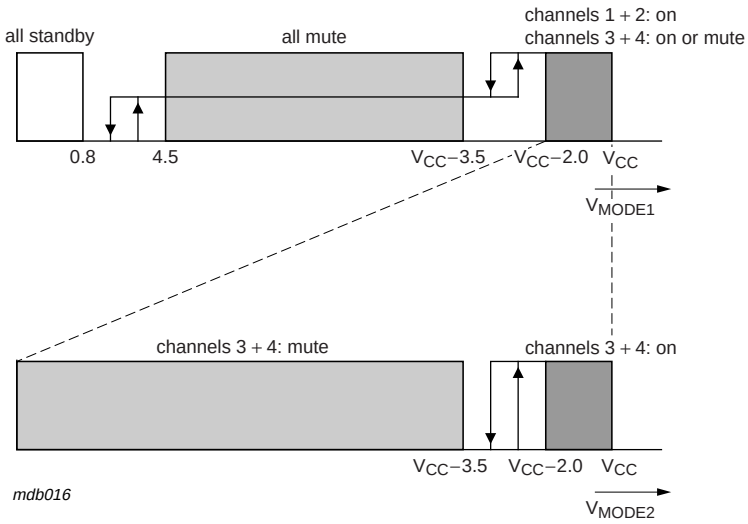


Fig 3. Mode selection

8.4 Supply voltage ripple rejection

The Supply Voltage Ripple Rejection (SVRR) is measured with an electrolytic capacitor of 150 µF on pin SVR using a bandwidth of 20 Hz to 22 kHz. Figure 10 illustrates the SVRR as function of the frequency. A larger capacitor value on pin SVR improves the ripple rejection behavior at the lower frequencies.

8.5 Built-in protection circuits

The TDA8948J contains two types of detection sensors: one measures local temperatures of the power stages and one measures the global chip temperature. At a local temperature of approximately 185 °C or a global temperature of approximately 150 °C, this detection circuit switches off the power stages for 2 ms. High-impedance of the outputs is the result. After this time period the power stages switch on automatically and the detection will take place again; still a too high temperature switches off the power stages immediately. This protects the TDA8948J against shorts to ground, to the supply voltage and across the load, and against too high chip temperatures.

The protection will only be activated when necessary, so even during a short-circuit condition, a certain amount of (pulsed) current will still be flowing through the short, just as much as the power stage can handle without exceeding the critical temperature level.

9. Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage	operating	–0.3	+26	V
		no (clipping) signal [1]	–0.3	+28	V
V_I	input voltage	-	–0.3	V_{CC} + 0.3	V
I_{ORM}	repetitive peak output current	-	-	4	A
T_{stg}	storage temperature	non-operating	–55	+150	°C
T_{amb}	ambient temperature	-	–40	+85	°C
P_{tot}	total power dissipation	-	-	69	W
$V_{CC(sc)}$	supply voltage (short circuit)	-	-	24	V

[1] The amplifier can deliver output power with non-clipping output signals into nominal loads as long as the ratings of the IC are not exceeded.

10. Thermal characteristics

Table 7. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	40	K/W
$R_{th(j-c)}$	thermal resistance from junction to case	all channels driven	2	K/W

11. Static characteristics

Table 8. Static characteristics

V_{CC} = 17 V; T_{amb} = 25 °C; R_L = 8 Ω; V_{MODE1} = V_{CC}; V_{MODE2} = V_{CC}; V_I = 0 V; measured in test circuit Figure 11; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supply							
V_{CC}	supply voltage	operating	[1]	9	17	26	V
		no (clipping) signal	[2]	-	-	28	V
I_q	quiescent current	V_{CC} = 17 V; R_L = ∞	[3]	-	100	145	mA
I_{stb}	standby current	-		-	-	10	µA
Output pins							
V_O	output voltage	-	[4]	-	9	-	V
$\Delta V_{O(offset)}$	differential output voltage offset	BTL mode	[5]	-	-	170	mV
Mode selection pins							
V_{MODE1}	voltage on pin MODE1	on mode		V_{CC} – 2.0	-	V_{CC}	V
		mute mode		4.5	-	V_{CC} – 3.5	V
		standby mode		0	-	0.8	V
V_{MODE2}	voltage on pin MODE2	on mode: channels 3 and 4	[6]	V_{CC} – 2.0	-	V_{CC}	V
		mute mode: channels 3 and 4		0	-	V_{CC} – 3.5	V
I_{MODE1}	current on pin MODE1	0 V < V_{MODE1} < (V_{CC} – 3.5 V)		-	-	20	µA
I_{MODE2}	current on pin MODE2	0 V < V_{MODE2} < (V_{CC} – 3.5 V)		-	-	20	µA

[1] A minimum load is required at supply voltages of V_{CC} > 22 V: R_L = 3 Ω for SE and R_L = 6 Ω for BTL.

[2] The amplifier can deliver output power with non-clipping output signals into nominal loads as long as the ratings of the IC are not exceeded.

[3] With a load connected at the outputs the quiescent current will increase.

[4] The DC output voltage, with respect to ground, is approximately 0.5 V_{CC}.

[5] $\Delta V_{O(offset)} = |V_{OUT+} - V_{OUT-}|$

[6] Channels 3 and 4 can only be set to mute or on mode by MODE2 when V_{MODE1} > V_{CC} – 2.0 V.

12. Dynamic characteristics

Table 9. Dynamic characteristics SE

V_{CC} = 17 V; T_{amb} = 25 °C; R_L = 4 Ω; f_i = 1 kHz; V_{MODE1} = V_{CC}; V_{MODE2} = V_{CC}; measured in test circuit Figure 11; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$P_{o(SE)}$	SE output power	V_{CC} = 17 V; see Figure 7				
		THD = 10 %; R_L = 4 Ω	6.5	8	-	W
		THD = 0.5 %; R_L = 4 Ω	-	6	-	W
		V_{CC} = 20 V				
		THD = 10 %; R_L = 4 Ω	-	12	-	W
THD	total harmonic distortion	P_o = 1 W	-	0.1	0.5	%
G_v	voltage gain	-	25	26	27	dB
Z_i	input impedance	-	40	60	-	kΩ

Table 9. Dynamic characteristics SE *...continued*

V_{CC} = 17 V; T_{amb} = 25 °C; R_L = 4 Ω; f_i = 1 kHz; V_{MODE1} = V_{CC}; V_{MODE2} = V_{CC}; measured in test circuit Figure 11; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{n(o)}$	output noise voltage	-	[1]	-	150	-	µV
SVRR	supply voltage ripple rejection	f_{ripple} = 1 kHz	[2]	-	60	-	dB
		f_{ripple} = 100 Hz to 20 kHz	[2]	-	60	-	dB
$V_{o(mute)}$	mute output voltage	-	[3]	-	-	150	µV
α_{cs}	channel separation	R_{SOURCE} = 0 Ω		50	60	-	dB
$\lvert\Delta G_v\rvert$	voltage gain difference	-		-	-	1	dB

[1] The noise output voltage is measured at the output in a frequency range from 20 Hz to 22 kHz (unweighted), with a source impedance R_{SOURCE} = 0 Ω at the input.

[2] Supply voltage ripple rejection is measured at the output, with a source impedance R_{SOURCE} = 0 Ω at the input and with a frequency range from 20 Hz to 22 kHz (unweighted). The ripple voltage is a sine wave with a frequency f_{ripple} and an amplitude of 300 mV (RMS), which is applied to the positive supply rail.

[3] Output voltage in mute mode is measured with V_{MODE1} = V_{MODE2} = 7 V, and V_i = 1 V (RMS) in a bandwidth from 20 Hz to 22 kHz, including noise.

Table 10. Dynamic characteristics BTL

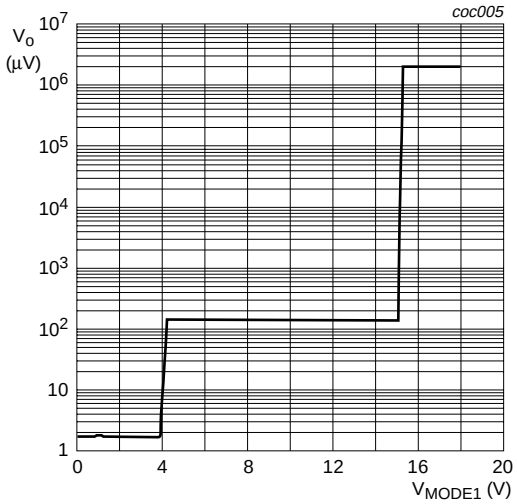
V_{CC} = 17 V; T_{amb} = 25 °C; R_L = 8 Ω; f = 1 kHz; V_{MODE1} = V_{CC}; V_{MODE2} = V_{CC}; measured in test circuit Figure 11; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$P_{o(BTL)}$	BTL output power	V_{CC} = 17 V; see Figure 7					
		THD = 10 %; R_L = 8 Ω		14	16	-	W
		THD = 0.5 %; R_L = 8 Ω		-	12	-	W
		V_{CC} = 20 V					
		THD = 10 %; R_L = 8 Ω		-	24	-	W
THD	total harmonic distortion	P_o = 1 W		-	0.05	0.5	%
G_v	voltage gain	-		31	32	33	dB
Z_i	input impedance	-		20	30	-	kΩ
$V_{n(o)}$	noise output voltage	-	[1]	-	200	-	µV
SVRR	supply voltage ripple rejection	f_{ripple} = 1 kHz	[2]	-	65	-	dB
		f_{ripple} = 100 Hz to 20 kHz	[2]	-	65	-	dB
$V_{o(mute)}$	mute output voltage	-	[3]	-	-	250	µV
α_{cs}	channel separation	R_{SOURCE} = 0 Ω		50	65	-	dB
$\lvert\Delta G_v\rvert$	voltage gain difference	-		-	-	1	dB

[1] The noise output voltage is measured at the output in a frequency range from 20 Hz to 22 kHz (unweighted), with a source impedance R_{SOURCE} = 0 Ω at the input.

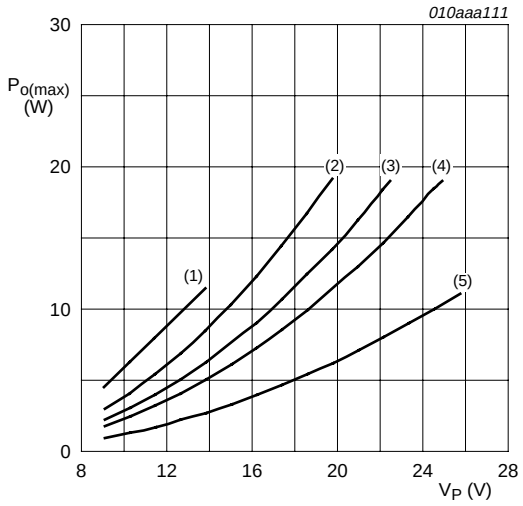
[2] Supply voltage ripple rejection is measured at the output, with a source impedance R_{SOURCE} = 0 Ω at the input and with a frequency range from 20 Hz to 22 kHz (unweighted). The ripple voltage is a sine wave with a frequency f_{ripple} and an amplitude of 300 mV (RMS), which is applied to the positive supply rail.

[3] Output voltage in mute mode is measured with V_{MODE1} = V_{MODE2} = 7 V, and V_i = 1 V (RMS) in a bandwidth from 20 Hz to 22 kHz, including noise.



a. BTL; V_{CC} = 17 V; V_i = 50 mV.

Fig 4. AC output voltage as a function of voltage on pin MODE1



f_i =1 kHz

(1) 1 Ω SE at THD = 10 %

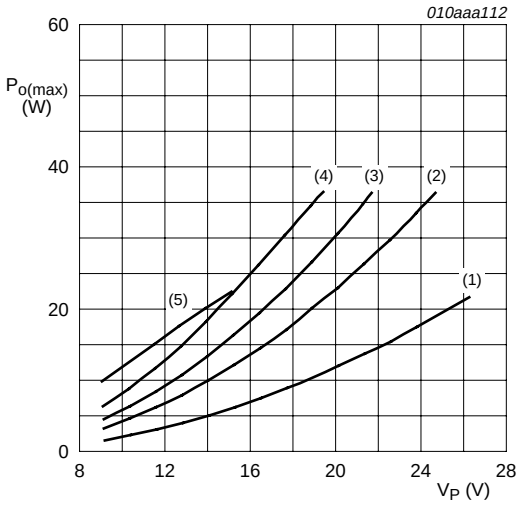
(2) 2 Ω SE at THD = 10 %

(3) 3 Ω SE at THD = 10 %

(4) 4 Ω SE at THD = 10 %

(5) 8 Ω SE at THD = 10 %

a. SE: THD = 10 %; one channel



f_i = 1 kHz

(1) 16 Ω BTL at THD = 10 %

(2) 8 Ω BTL at THD = 10 %

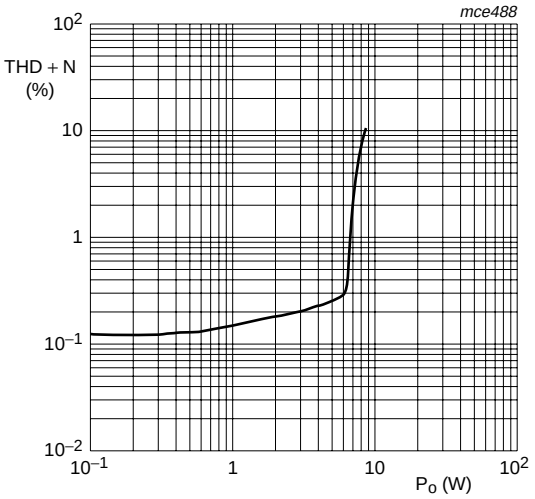
(3) 6 Ω BTL at THD = 10 %

(4) 4 Ω BTL at THD = 10 %

(5) 2 Ω BTL at THD = 10 %

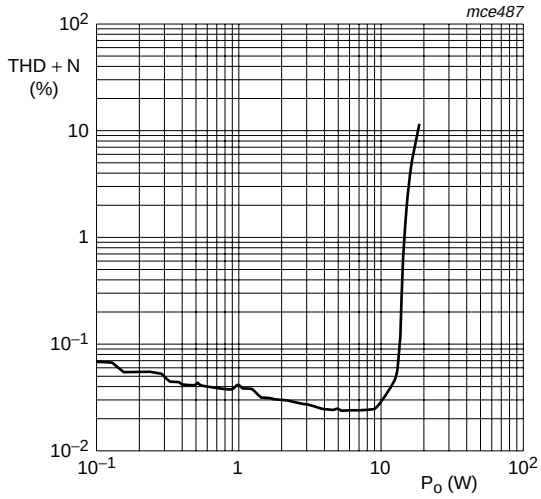
b. BTL: THD = 10 %; one channel

Fig 5. Maximum output power as a function of supply voltage at various loads



V_{CC} = 17 V; f_i = 1 kHz; R_L = 4 Ω.

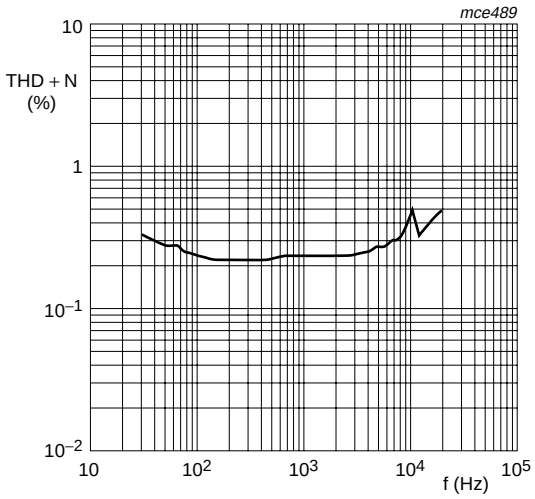
a. SE



V_{CC} = 17 V; f_i = 1 kHz; R_L = 8 Ω.

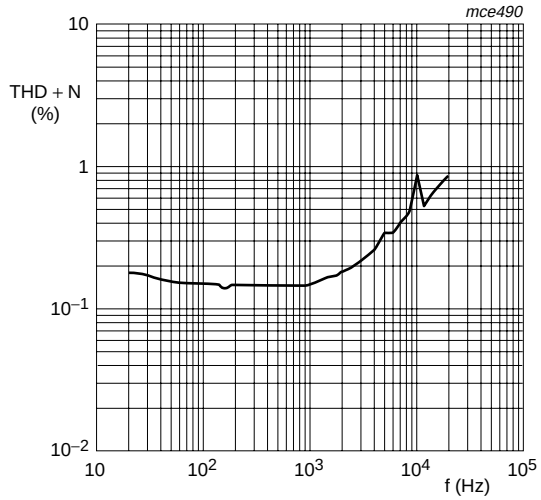
b. BTL

Fig 6. Total harmonic distortion-plus-noise as a function of output power



V_{CC} = 17 V; P_o = 1 W; R_L = 4 Ω.

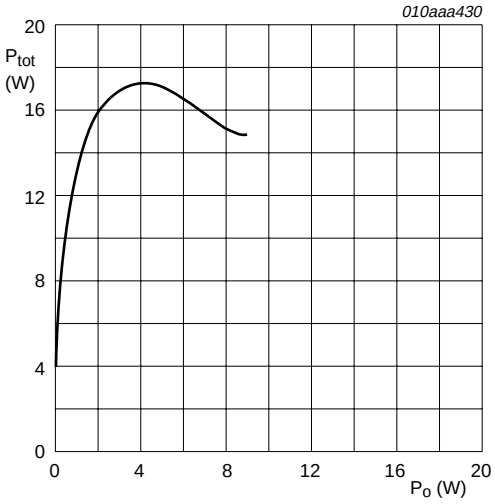
a. SE



V_{CC} = 17 V; P_o = 1 W; R_L = 8 Ω.

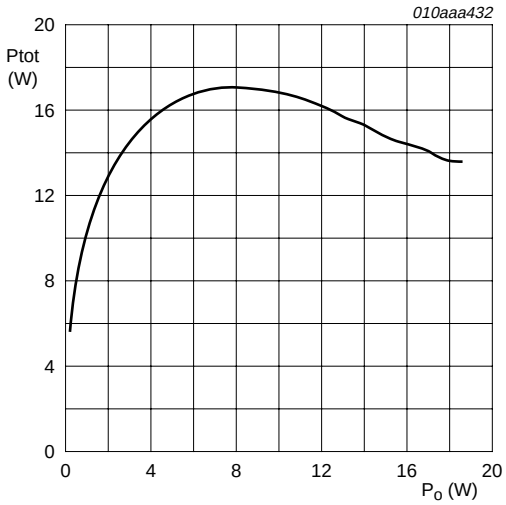
b. BTL

Fig 7. Total harmonic distortion-plus-noise as a function of frequency



V_{CC} = 17 V; R_L = 4 Ω.

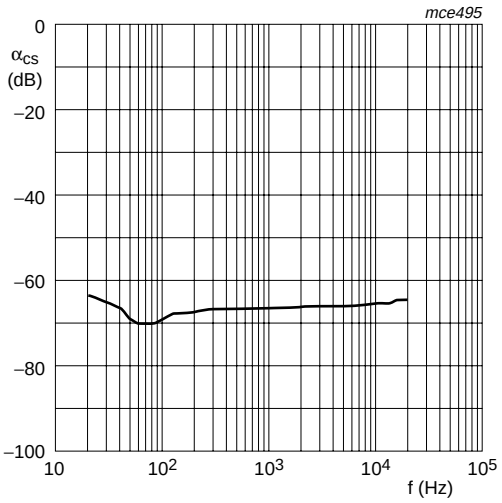
a. SE



V_{CC} = 17 V; R_L = 8 Ω.

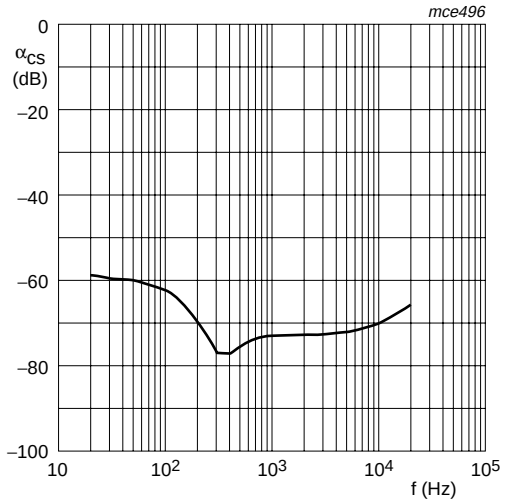
b. BTL

Fig 8. Total power dissipation as a function of channel output power per channel (worst case, all channels driven)



V_{CC} = 17 V; R_L = 4 Ω.

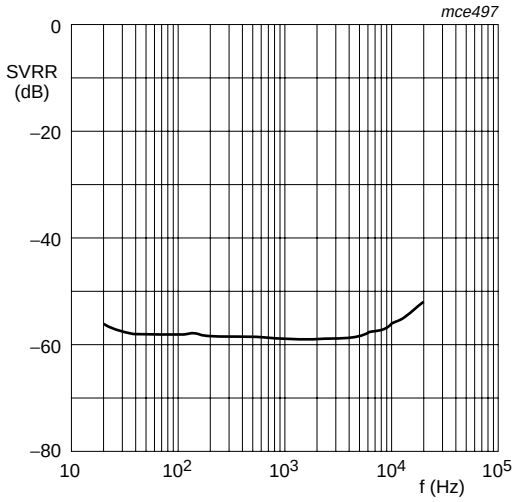
a. SE



V_{CC} = 17 V; R_L = 8 Ω.

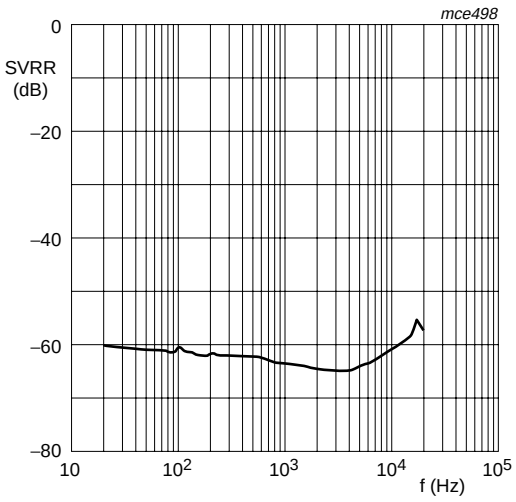
b. BTL

Fig 9. Channel separation as a function of frequency (no band-pass filter applied)



V_{CC} = 17 V; R_{SOURCE} = 0 Ω; V_{ripple} = 300 mV (RMS).
A band-pass filter of 20 Hz to 22 kHz has been applied.
Inputs short-circuited.

a. SE



V_{CC} = 17 V; R_{SOURCE} = 0 Ω; V_{ripple} = 300 mV (RMS).
A band-pass filter of 20 Hz to 22 kHz has been applied.
Inputs short-circuited.

b. BTL

Fig 10. Supply voltage ripple rejection as a function of frequency

13. Application information

13.1 Application diagrams

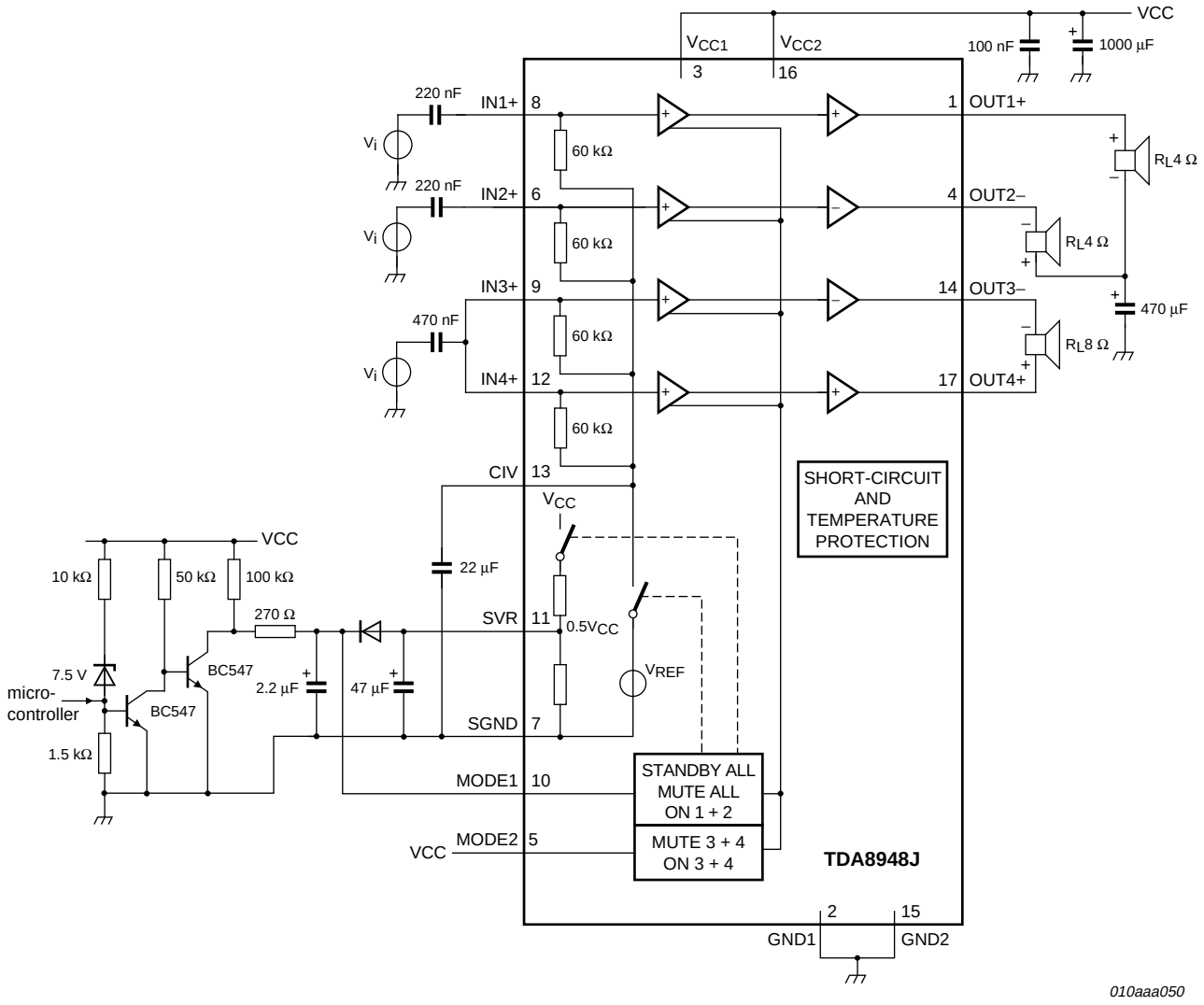


Fig 11. Typical application diagram without on/off switching plops

Table 11. Amplifier selection by microcontroller

Microcontroller with open-collector output; see Figure 11.

Microcontroller	Channels 1 and 2	Channels 3 and 4
LOW	On mode	On mode
HIGH	Mute mode	Mute mode

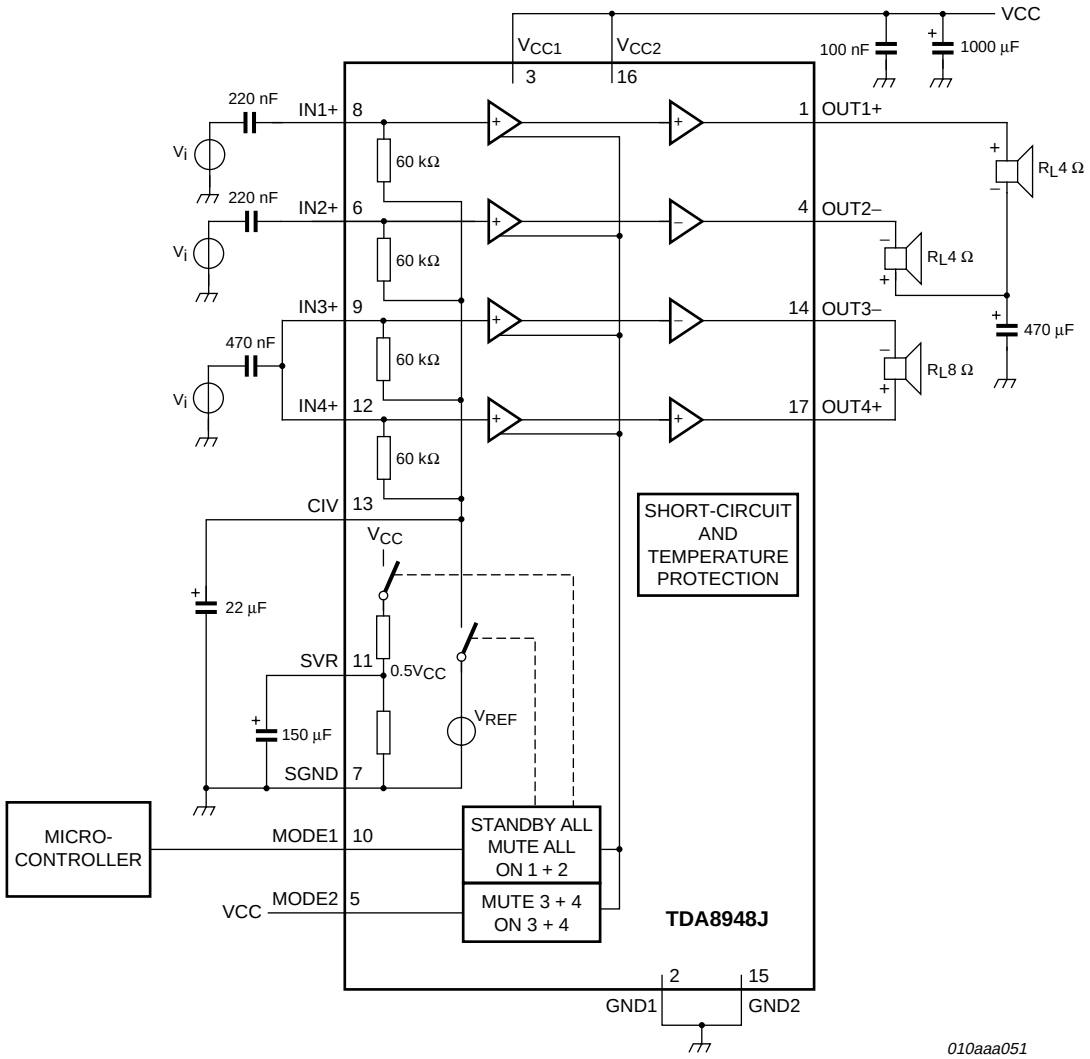


Fig 12. Application diagram with one pin control and reduction of capacitor

Remark: Because of switching inductive loads, the output voltage can rise beyond the maximum supply voltage of 28 V. At high supply voltages, it is recommended to use (Schottky) diodes to the supply voltage and ground.

13.2 Printed-circuit board

13.2.1 Layout and grounding

To obtain a high-level system performance, certain grounding techniques are essential. The input reference grounds have to be tied with their respective source grounds and must have separate tracks from the power ground tracks; this will prevent the large (output) signal currents from interfering with the small AC input signals. The small signal ground tracks should be physically located as far as possible from the power ground tracks. Supply and output tracks should be as wide as possible for delivering maximum output power.

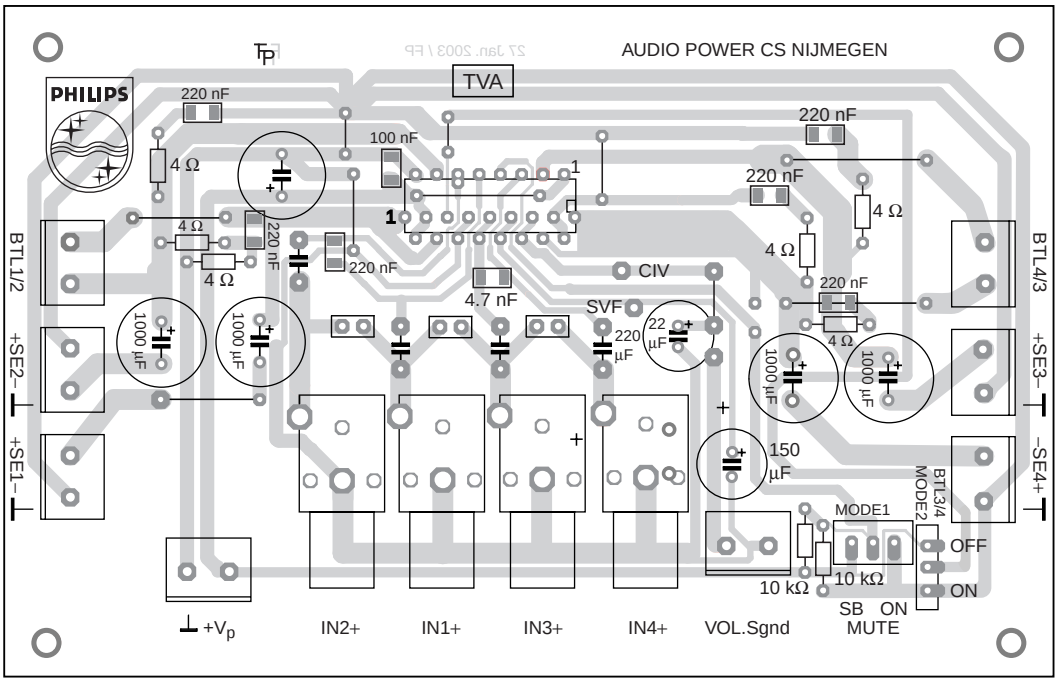


Fig 13. Printed-circuit board layout (single-sided); components view

13.2.2 Power supply decoupling

Proper supply bypassing is critical for low-noise performance and high supply voltage ripple rejection. The respective capacitor location should be as close as possible to the device and grounded to the power ground. Proper power supply decoupling also prevents oscillations.

For suppressing higher frequency transients (spikes) on the supply line a capacitor with low Equivalent Series Resistance (ESR), typical 100 nF, has to be placed as close as possible to the device. For suppressing lower frequency noise and ripple signals, a large electrolytic capacitor, e.g. 1000 µF or greater, must be placed close to the device.

The bypass capacitor on pin SVR reduces the noise and ripple on the mid rail voltage. For good Total Harmonic Distortion (THD) and noise performance a low ESR capacitor is recommended.

13.3 Thermal behavior and heat sink calculation

The measured maximum thermal resistance of the IC package, $R_{th(j-mb)}$, is 1.3 K/W. A calculation for the heat sink can be made, with the following parameters:

$T_{amb(max)}$ = 60 °C (example)

V_{CC} = 17 V and R_L = 4 Ω (SE)

$T_{j(max)}$ = 150 °C (specification)

$R_{th(tot)}$ is the total thermal resistance between the junction and the ambient including the heat sink. This can be calculated using the maximum temperature increase divided by the power dissipation:

$$R_{th(tot)} = (T_{j(max)} - T_{amb(max)})/P$$

At V_{CC} = 17 V and R_L = 4 Ω (4 × SE) the measured worst-case sine-wave dissipation is 17 W; see Figure 8. For $T_{j(max)}$ = 150 °C the temperature raise, caused by the power dissipation, is: 150 °C – 60 °C = 90 °C:

$P \times R_{th(tot)}$ = 90 °C

$R_{th(tot)}$ = 90/17 K/W = 5.29 K/W

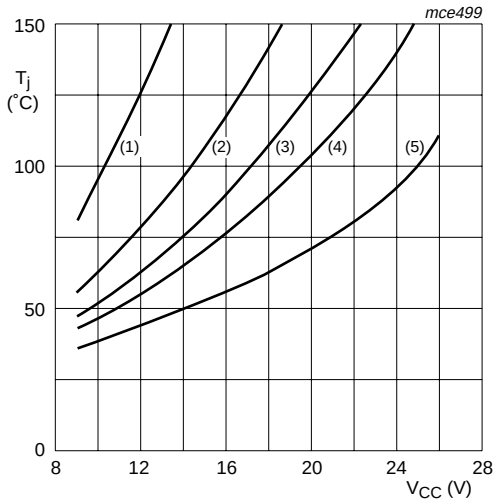
$R_{th(h-a)} = R_{th(tot)} - R_{th(j-mb)}$ = 5.29 K/W – 2 K/W = 3.29 K/W

This calculation is for an application at worst-case (stereo) sine-wave output signals. In practice music signals will be applied, which decreases the maximum power dissipation to approximately half of the sine-wave power dissipation of 9 W (see Section 8.2.2). This allows for the use of a smaller heat sink:

$P \times R_{th(tot)}$ = 90 °C

$R_{th(tot)}$ = 90/9 K/W = 10 K/W

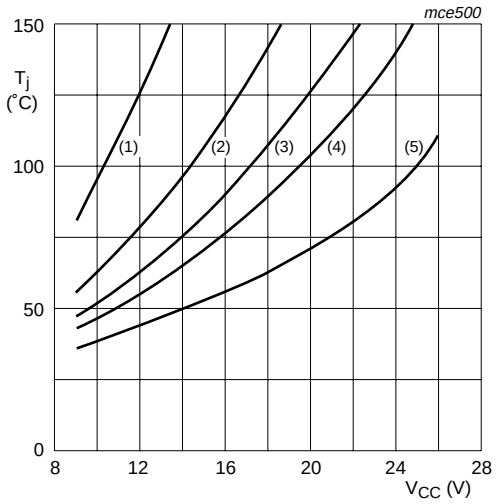
$R_{th(h-a)} = R_{th(tot)} - R_{th(j-mb)}$ = 10 K/W - 2 K/W = 8 K/W



T_{amb} = 25 °C; external heat sink of 4.3 K/W.

(1) R_L = 1 Ω.
(2) R_L = 2 Ω.
(3) R_L = 3 Ω.
(4) R_L = 4 Ω.
(5) R_L = 8 Ω.

a. 4 times various SE loads with music signals.



T_{amb} = 25 °C; external heat sink of 4.3 K/W.

(1) R_L = 2 Ω.
(2) R_L = 4 Ω.
(3) R_L = 6 Ω.
(4) R_L = 8 Ω.
(5) R_L = 16 Ω.

b. 2 times various BTL loads with music signals.

Fig 14. Junction temperature as a function of supply voltage for various loads with music signals

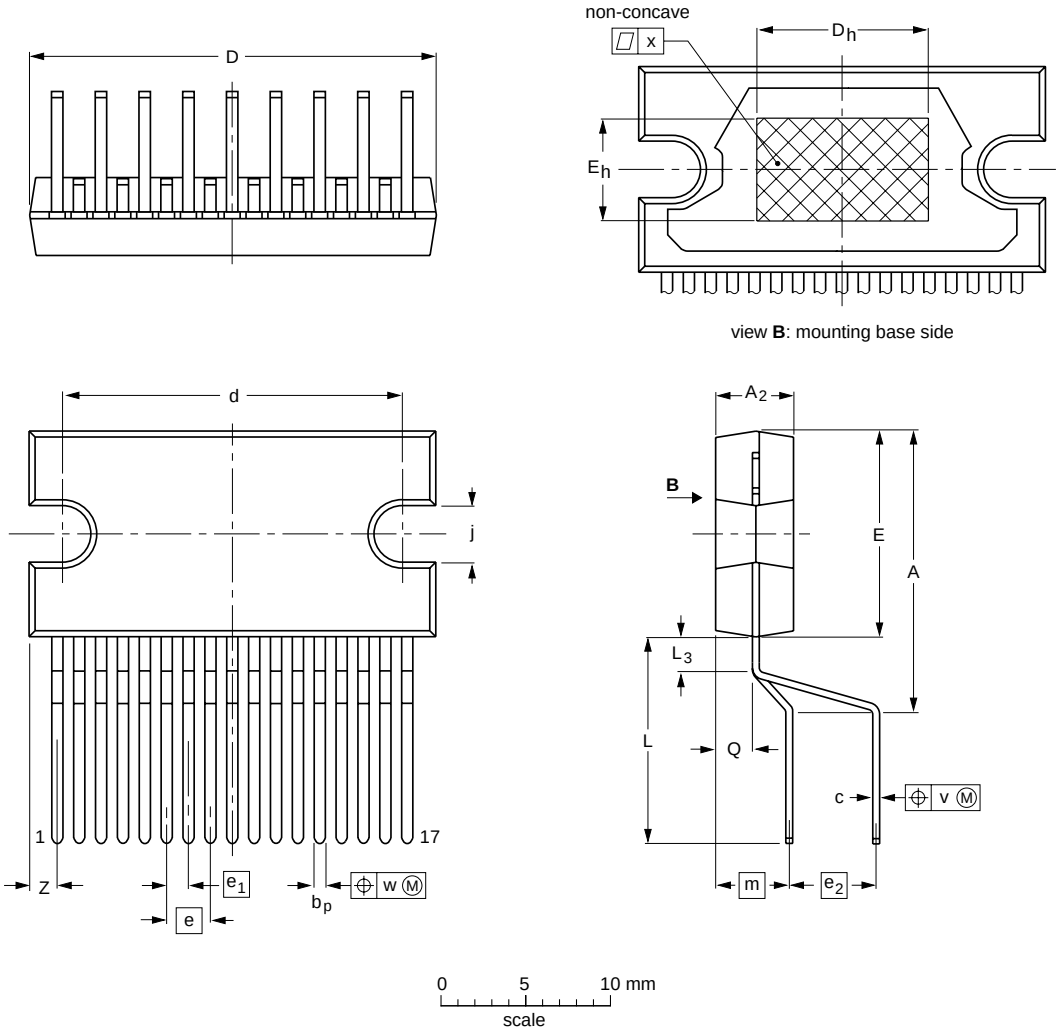
14. Test information

14.1 Quality information

The General Quality Specification for Integrated Circuits, SNW-FQ-611 is applicable.

15. Package outline

DBS17P: plastic DIL-bent-SIL power package; 17 leads (lead length 12 mm) **SOT243-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_2	b_p	c	$D^{(1)}$	d	D_h	$E^{(1)}$	e	e_1	e_2	E_h	j	L	L_3	m	Q	v	w	x	$Z^{(1)}$
mm	17.0 15.5	4.6 4.4	0.75 0.60	0.48 0.38	24.0 23.6	20.0 19.6	10	12.2 11.8	2.54	1.27	5.08	6	3.4 3.1	12.4 11.0	2.4 1.6	4.3	2.1 1.8	0.8	0.4	0.03	2.00 1.45

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT243-1						~~99-12-17~~ 03-03-12

Fig 15. Package outline SOT243-1 (DBS17P)

16. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

16.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

16.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

16.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

16.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 16) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 12 and 13

Table 12. SnPb eutectic process (from J-STD-020C)

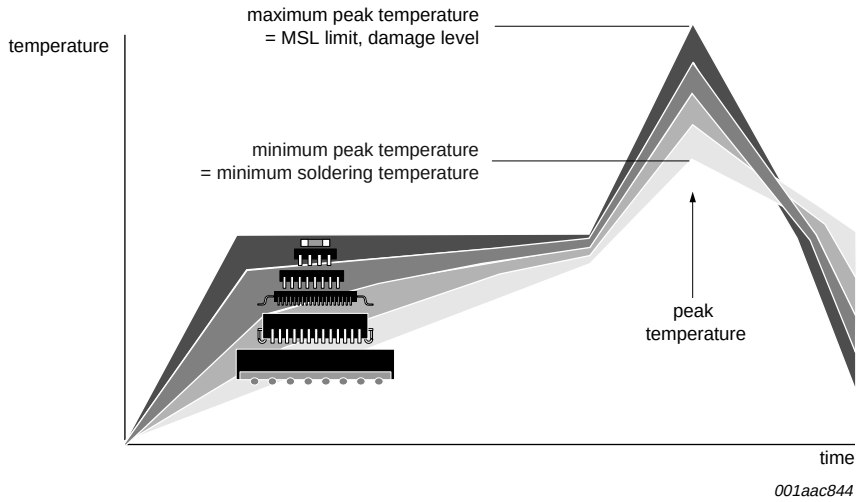
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 13. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 16.



MSL: Moisture Sensitivity Level

Fig 16. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

17. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TDA8948J_1	20080227	Product data sheet	-	-

18. Legal information

18.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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