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NEW50/70/80/90 M/B Schematics Document

Intel Arrandale Processor with DDRIII + Ibex Peak-M
ATI Madision/Park

2010-01-07

REV:1.0

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2009/08/01	Deciphered Date	2010/08/01	Title: Cover Page
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Model Name : NEW50/70/80/90
File Name : LA5891P

Fan Control page 38

Clock Generator
IDT: 9LVS3199AKLFT
Realtek: RTM890N-631-VB-GRT
133/120/100/96/14.318MHZ to PCH
page 12

Madision/Park
page 22,23,24,25,26,27,28

PEG(DIS) 100MHz PCI-E 2.0x16 5GT/s PER LANE 133MHz

Intel Arrandale (UMA/DIS) Processor rPGA988A
page 4,5,6,7,8,9

Memory BUS(DDRIII) Dual Channel 1.5V DDRIII 800/1066

204pin DDRIII-SO-DIMM X2
BANK 0, 1, 2, 3 page 10,11

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HDMI(DIS)
CRT(DIS)

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CRT Conn. page 30
LVDS Conn. page 29

FDI x8 (UMA) 100MHz 2.7GT/s
DMI x4 100MHz 1GB/s x4

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USB port 0, 2 on USB/B
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Bluetooth Conn
USB port 11
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CMOS Camera
USB port 8
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Card Reader RTS5160
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USBx14 3.3V 48MHz

HDMI(UMA)
HDMI Level Shift page 31

LVDS(UMA)
CRT(UMA)
TMDS(UMA)

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HD Audio 3.3V 24MHz

HDA Codec ALC272X page 40

PCI-Express x 8 (ARD PCIE2.0 2.5GT/s) 100MHz
SATA x 6 (GEN1 1.5GT/S ,GEN2 3GT/S) 100MHz

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MINI Card x2
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RTC CKT. page 15

Power On/Off CKT. page 34

DC/DC Interface CKT. page 38

Power Circuit DC/DC page 40~48

Sub-board

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LS-5892P
Card Reader
USB Port9
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Power/B
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LS-5894P
LID_SW/B

LS-5895P
3G
USB Port10,13
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Title: Block Diagrams

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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF
+VGFX_CORE	Core voltage for Arrandale GPU (only for arrandaleCPU)	ON	OFF	OFF
+0.75VS	+0.75VP to +0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.0VSDGPU	+1.0VSPDGPU to +1.0VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.05VS_VTT	+1.05VS_VTTP to +1.05VS_VTT switched power rail for ARD CPU	ON	OFF	OFF
+1.05VS_PCH	+1.05VS_VTT to +1.05VS_PCH power for PCH	ON	OFF	OFF
+1.5V	+1.5VP to +1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	+1.5V to +1.5VS switched power rail	ON	OFF	OFF
+1.5VSDGPU	+1.5VS to +1.5VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.8VS	(+5VALW or +3VALW) to 1.8V switched power rail to PCH & GPU	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+3VALW_EC	+3VALW always to KBC	ON	ON	ON*
+3V_LAN	+3VALW to +3V_LAN power rail for LAN	ON	ON	ON*
+3V	+3VALW to +3V power rail for PCH (Short Jumper)	ON	ON	ON*
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5V	+5VALW to +5V switched power rail for PCH (Short resister)	ON	ON	ON*
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+VSB	+VSBP to +VSB always on power rail for sequence control	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON
Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.				

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address

PCH SM Bus address

Device	Address
Clock Generator (9LVS3199AKLFT, RTM890N-631-VB-GRT)	1101 0010b
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

Option	UMAHD@	VGAHD@	HDMI@	@	SG@
UMA	V	X	V	X	X
VGA	X	V	V	X	X
SG	X	V	V	X	V
NO HDMI	X	X	X	X	X

LED BOM config

NEW70,80 SKU: 7080@
NEW50,90 SKU: 5090@

3G & BT Config

3G SKU: 3G@
BT SKU: BT@

GPU BOM Config

Madision SKU: MADI@
Park SKU: PARK@

VRAM BOM Config

X761@: X76198BOL01 Park Samsung 512MB
X762@: X76198BOL02 Park Hynix 512MB
X763@: X76198BOL03 Madision Samsung 1024MB
X764@: X76198BOL04 Madision Hynix 1024MB
X765@: X76198BOL05 Park AMD 512MB
X766@: X76198BOL06 Madision AMD 1024MB

BOM Config

UMA W/O HDMI SKU: BT@/3G@/UMA@/UMAO@
UMA W/ HDMI SKU: BT@/3G@/UMA@/UMAO@/HDMI@/UMAHD@
Discrete W/O HDMI SKU: BT@/3G@/DIS@/DISO@/VGA@
Discrete W/ HDMI SKU: BT@/3G@/DIS@/DISO@/VGA@/HDMI@/VGAHD@
Switchable W/O HDMI SKU: BT@/3G@/DIS@/UMA@/VGA@/SG@
Switchable W HDMI SKU: BT@/3G@/DIS@/UMA@/VGA@/SG@/HDMI@/VGAHD@

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure
UMA	UMA@
UMA Only	UMAO@
Discrete	DIS@
Discrete Only	DISO@
GPU ALL Components	VGA@
VRAM	X76@
Switchable	SG@
Connector	CONN@
3G	3G@
Blue Tooth	BT@
Unpop	@
UMA HDMI	UMAHD@
Discrete HDMI	VGAHD@
UMA & DIS POP HDMI	HDMI@
GPU Madision	MADI@
GPU Park	PARK@
NEW70,80 LED	7080@
NEW50,90 LED	5090@

USB Port Table

USB 2.0	USB 1.1	Port	3 External USB Port
EHCI1	UHCI0	0	USB/B (Right Side)
		1	USB Port (Left Side)
	UHCI1	2	USB/B (Right Side)
		3	
	UHCI2	4	
		5	
	UHCI3	6	
		7	
EHCI2	UHCI4	8	Camera
		9	Card Reader
	UHCI5	10	SIM Card
		11	Blue Tooth
	UHCI6	12	Mini Card(WLAN)
		13	Mini Card(GPS)

X76@

ID3 , ID1 : VRAM Vender

Location / VRAM	VRAM_ID3		VRAM_ID1	
Samsung	0	R492	0	R474
HYNIX	1	R491	0	R474
AMD	1	R491	1	R473

ID2: VRAM Size

Location / VRAM	VRAM_ID2	
8PCS 64Mx16	0	R482
4PCS 64Mx16	1	R483

VRAM P/N :
Samsung : SA000035700 (S IC D3 64MX16 K4W1G1646E-HC12 FBGA 96P)
Hynix : SA000032400 (S IC D3 64MX16 H5TQ1G63BFR-12C FBGA 1.5V)
AMD: SA00003PF20 (S IC D3 23EY2387MB-12)

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Title	Notes List		
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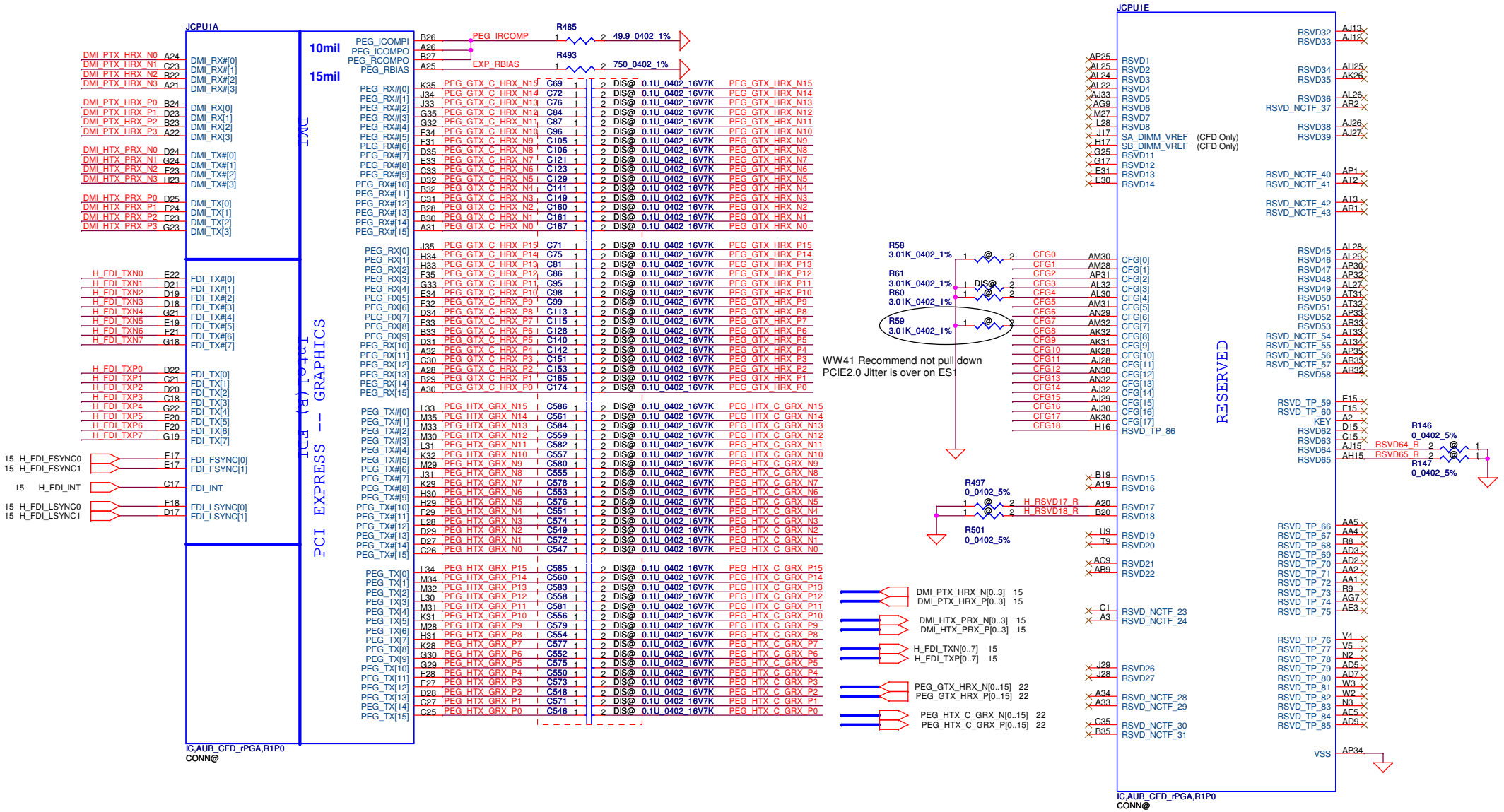
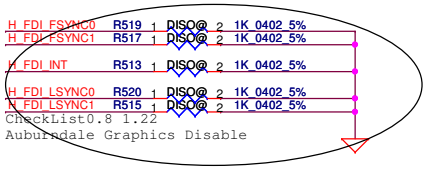


eDP Signals Mapping

eDP Singal	PEG Singals	Lane Reversal
eDP_TX0	PEG_HTX_C_GRX_P15	PEG_HTX_C_GRX_P0
eDP_TX#0	PEG_HTX_C_GRX_N15	PEG_HTX_C_GRX_N0
eDP_TX1	PEG_HTX_C_GRX_P14	PEG_HTX_C_GRX_P1
eDP_TX#1	PEG_HTX_C_GRX_N14	PEG_HTX_C_GRX_N1
eDP_TX2	PEG_HTX_C_GRX_P13	PEG_HTX_C_GRX_P2
eDP_TX#2	PEG_HTX_C_GRX_N13	PEG_HTX_C_GRX_N2
eDP_TX3	PEG_HTX_C_GRX_P12	PEG_HTX_C_GRX_P3
eDP_TX#3	PEG_HTX_C_GRX_N12	PEG_HTX_C_GRX_N3
eDP_AUX	PEG_GTX_C_HRX_P13	PEG_GTX_C_HRX_P2
eDP_AUX#	PEG_GTX_C_HRX_N13	PEG_GTX_C_HRX_N2
eDP_HPD#	PEG_GTX_C_HRX_P12	PEG_GTX_C_HRX_P3



CFG0 - PCI-Express Configuration Select

*1:Single PEG
0:Bifurcation enabled

CFG3 - PCI-Express Static Lane Reversal

*1 :Normal Operation
0 :Lane Numbers Reversed
15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence

*1:Disabled; No Physical Display Port attached to Embedded Display Port
0:Enabled; An external Display Port device is connected to the Embedded Display Port

*:Default

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Title: PROCESSOR (1/6) DMI,FDI,PEG

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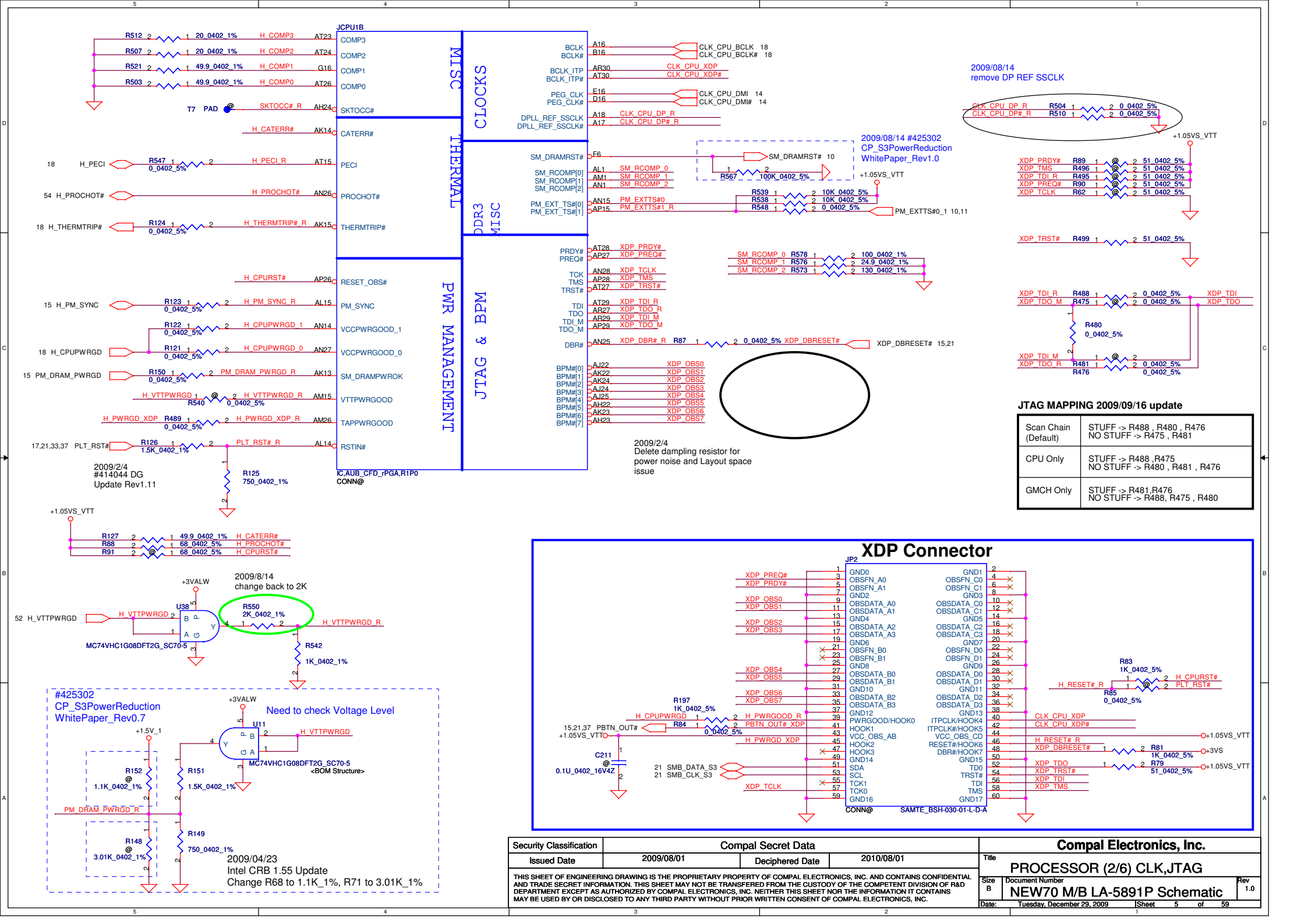

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Title: PROCESSOR (2/6) CLK,JTAG

Size	Document Number	Rev
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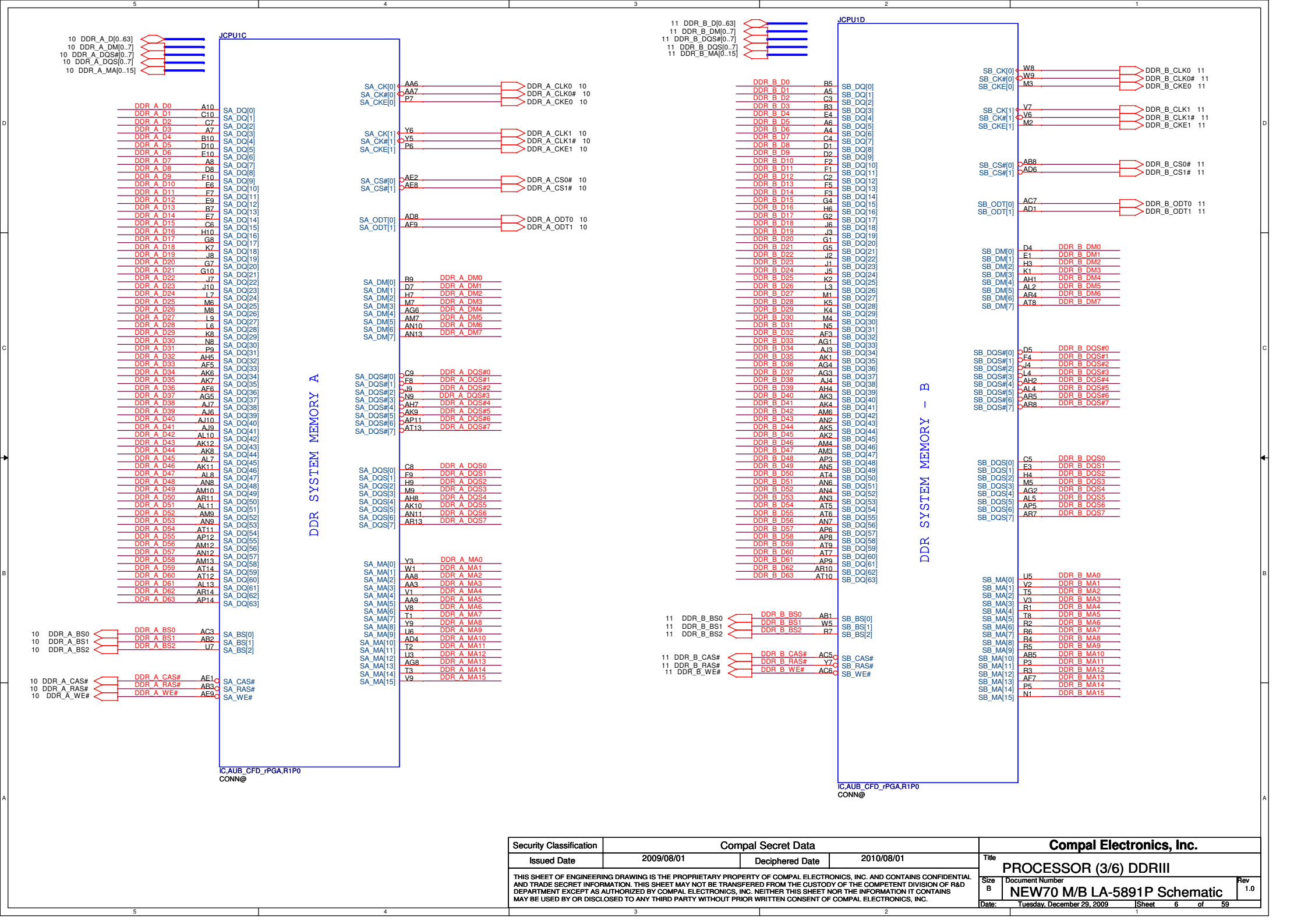

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Title: PROCESSOR (3/6) DDRIII

Size	Document Number	Rev
B	NEW70 M/B LA-5891P Schematic	1.0

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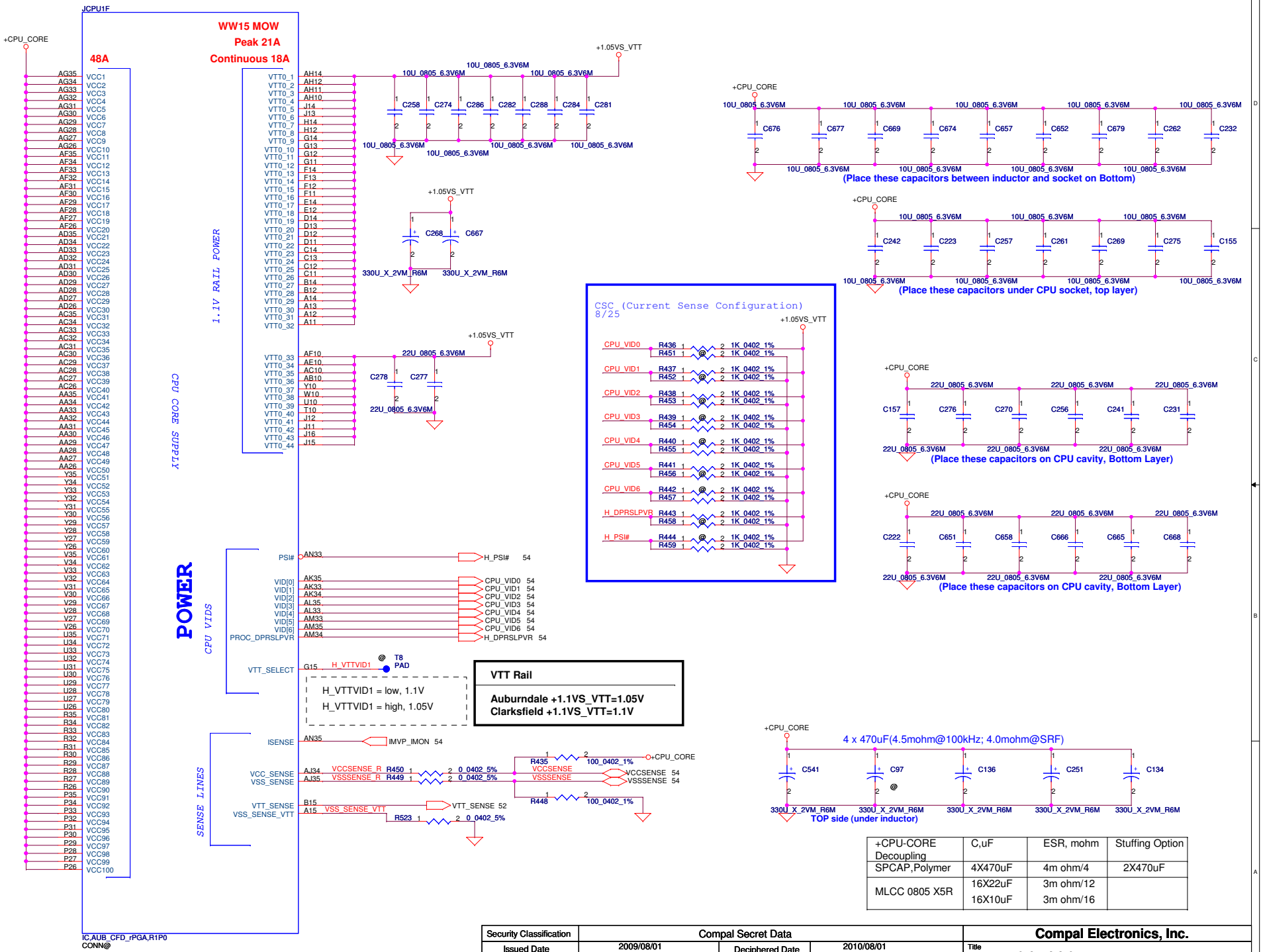

+CPU-CORE Decoupling	C,uF	ESR, mohm	Stuffing Option
SPCAP,Polymer	4X470uF	4m ohm/4	2X470uF
MLCC 0805 X5R	16X22uF 16X10uF	3m ohm/12 3m ohm/16	

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Title: PROCESSOR (4/6) PWR,Bypass

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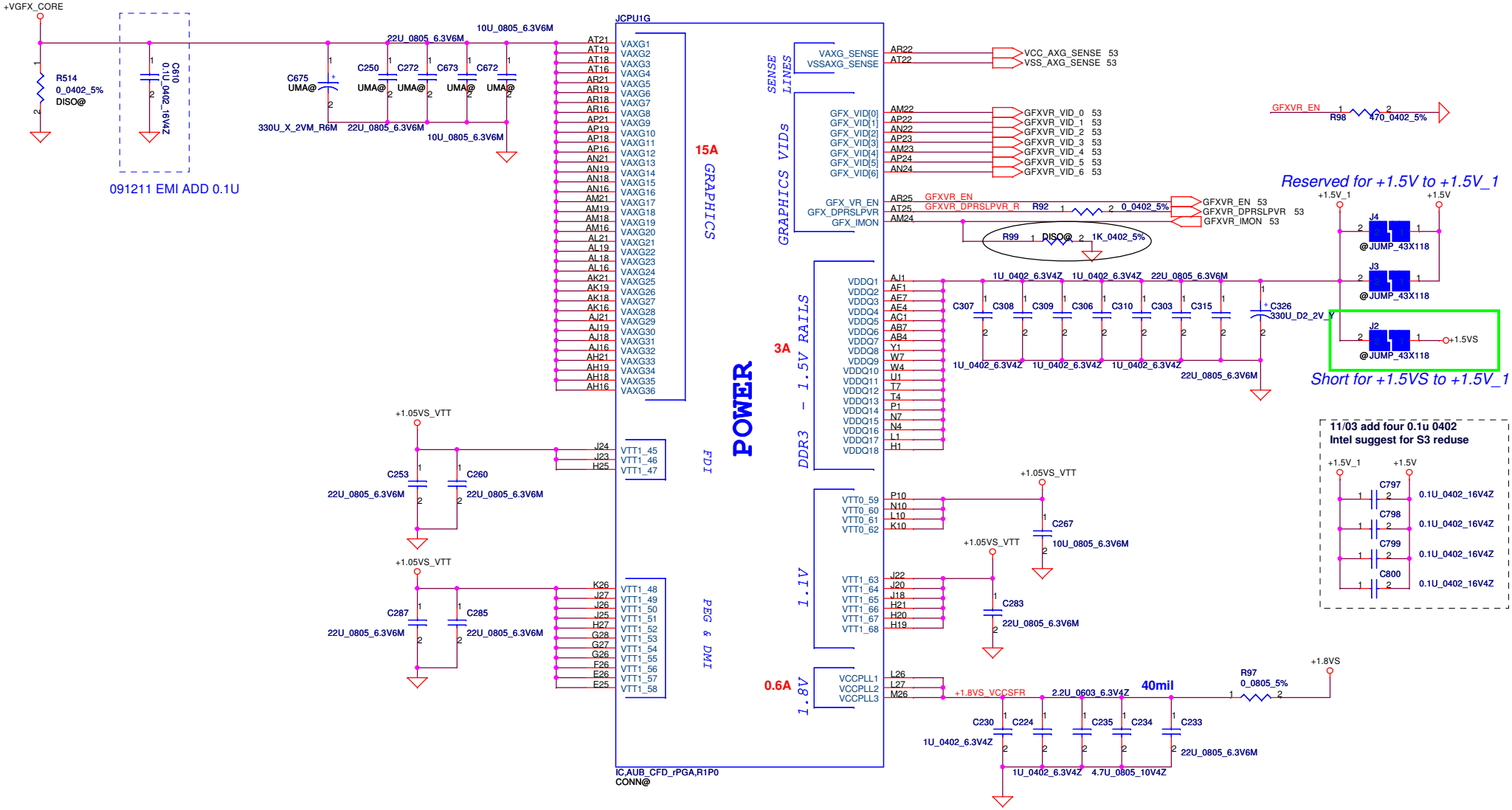

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Title: PROCESSOR (5/6) PWR

Size: Custom | Document Number: NEW70 M/B LA-5891P Schematic | Rev: 1.0

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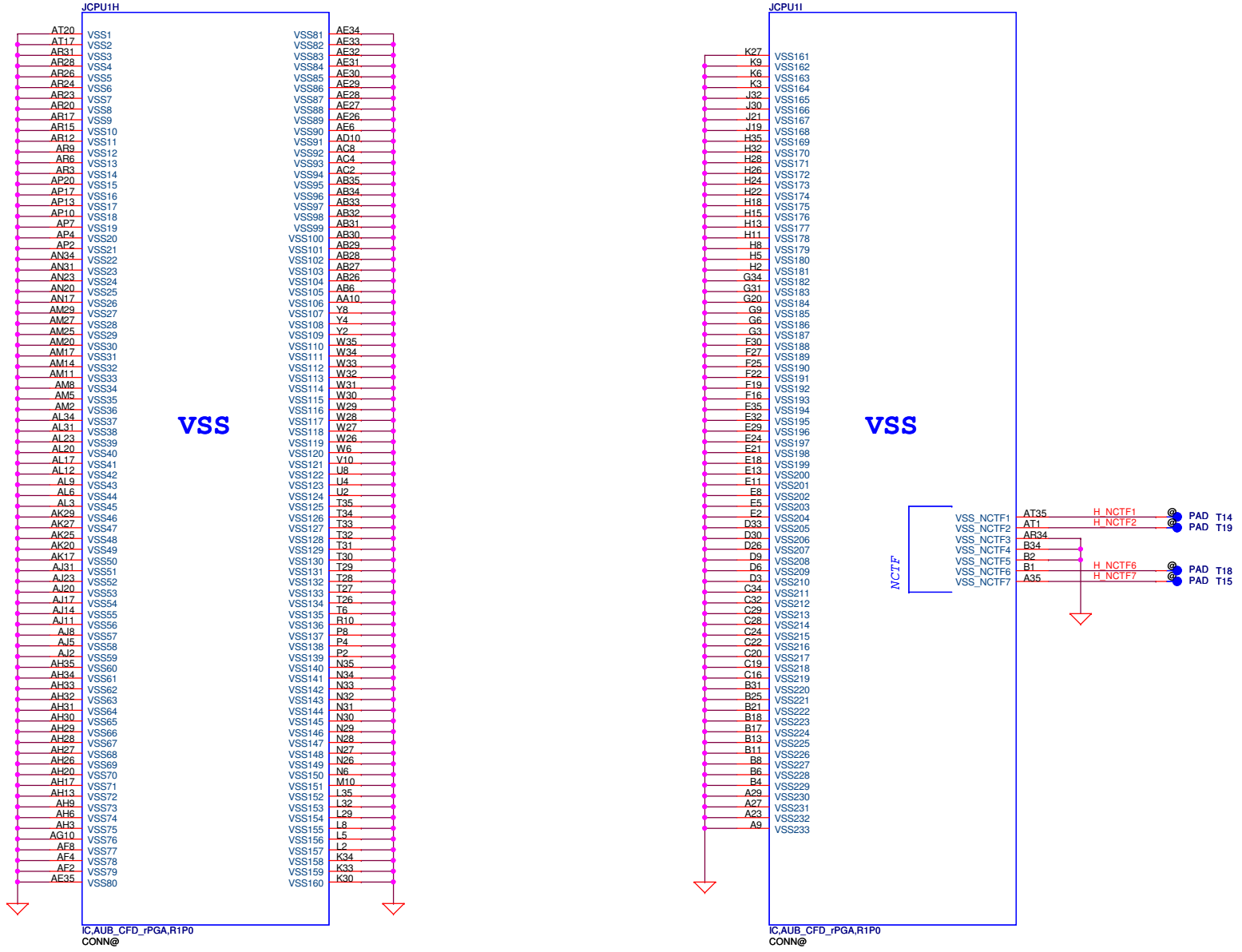

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Title: PROCESSOR (6/6) VSS

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DIMMA VREFDQ M1 Circuit

+1.5V
R222 1K_0402_1%
+DIMM_VREFDQA
20mil
R227 1K_0402_1%

DIMMA & DIMMB VREFCA circuit

+1.5V
R203 1K_0402_1%
+DIMM_VREFCA
20mil
R201 1K_0402_1%

6 DDR_A_DQS#[0..7]
6 DDR_A_D[0..63]
6 DDR_A_DM[0..7]
6 DDR_A_DQS[0..7]
6 DDR_A_MA[0..15]

#425302
CP_S3PowerReduction
WhitePaper_Rev1.0

+1.5V
R254 0_0402_5%
R274 1K_0402_1%
5 SM_DRAMRST#
DIMM_DRAMRST#
DIMM_DRAMRST# 11
Q17 BSS138LT1G_SOT23-3
C422
18 RST_GATE
RST_GATE
0.047U_0402_16V7K

Layout Note:
Place near JDIMM1

Layout Note: Place these 4 Caps near Command and Control signals of DIMMA

+1.5V
C354 10U_0805_6.3V6M
C355 10U_0805_6.3V6M
C356 10U_0805_6.3V6M
C405 10U_0805_6.3V6M
C404 10U_0805_6.3V6M
C406 10U_0805_6.3V6M
C362 0.1U_0402_16V4Z
C363 0.1U_0402_16V4Z
C399 0.1U_0402_16V4Z
C400 0.1U_0402_16V4Z
C425 330U_2.5V_M_R15 @

Layout Note:
Place near JDIMM1.203 & JDIMM1.204

+0.75VS
C391 1U_0402_6.3V4Z
C388 1U_0402_6.3V4Z
C397 1U_0402_6.3V4Z
C396 1U_0402_6.3V4Z
C394 10U_0805_6.3V6M
1U_0402_6.3V4Z
1U_0402_6.3V4Z

+DIMM_VREFDQA
C401 0.1U_0402_16V4Z
C402 2.2U_0603_6.3V4Z

JDIMM1

		VREF_DQ	1	2	VSS1
		VSS2	3	4	DQ4
DDR_A_D0		DQ0	5	6	DQ5
DDR_A_D1		DQ1	7	8	VSS3
	DDR_A_DM0	VSS4	9	10	DQS#0
		DM0	11	12	DQS0
		VSS5	13	14	VSS6
DDR_A_D2		DQ2	15	16	DQ6
DDR_A_D3		DQ3	17	18	DQ7
		VSS7	19	20	VSS8
DDR_A_D8		DQ8	21	22	DQ12
DDR_A_D9		DQ9	23	24	DQ13
		VSS9	25	26	VSS10
DDR_A_DQS#1		DQS#1	27	28	DM1
DDR_A_DQS1		DQS1	29	30	RESET#
		VSS11	31	32	VSS12
DDR_A_D10		DQ10	33	34	DQ14
DDR_A_D11		DQ11	35	36	DQ15
		VSS13	37	38	VSS14
DDR_A_D16		DQ16	39	40	DQ20
DDR_A_D17		DQ17	41	42	DQ21
		VSS15	43	44	VSS16
DDR_A_DQS#2		DQS#2	45	46	DM2
DDR_A_DQS2		DQS2	47	48	VSS17
		VSS18	49	50	DQ22
DDR_A_D18		DQ18	51	52	DQ23
DDR_A_D19		DQ19	53	54	VSS19
		VSS20	55	56	DQ28
DDR_A_D24		DQ24	57	58	DQ29
DDR_A_D25		DQ25	59	60	VSS21
		VSS22	61	62	DQS#3
DDR_A_DM3		DM3	63	64	DQS3
		VSS23	65	66	VSS24
DDR_A_D26		DQ26	67	68	DQ30
DDR_A_D27		DQ27	69	70	DQ31
		VSS25	71	72	VSS26
6 DDR_A_CKE0	DDR_A_CKE0	CKE0	73	74	CKE1
		VDD1	75	76	VDD2
		NC1	77	78	A15
6 DDR_A_BS2		BA2	79	80	A14
		VDD3	81	82	VDD4
DDR_A_MA12		A12/BC#	83	84	A11
DDR_A_MA9		A9	85	86	A7
		VDD5	87	88	VDD6
DDR_A_MA8		A8	89	90	A6
DDR_A_MA5		A5	91	92	A4
		VDD7	93	94	VDD8
DDR_A_MA3		A3	95	96	A2
DDR_A_MA1		A1	97	98	A0
		VDD9	99	100	VDD10
6 DDR_A_CLK0	DDR_A_CLK0	CK0	101	102	CK1
6 DDR_A_CLK0#	DDR_A_CLK0#	CK0#	103	104	CK1#
		VDD11	105	106	VDD12
DDR_A_MA10		A10/AP	107	108	BA1
6 DDR_A_BS0	DDR_A_BS0	BA0	109	110	RAS#
		VDD13	111	112	VDD14
6 DDR_A_WE#	DDR_A_WE#	WE#	113	114	S0#
6 DDR_A_CAS#	DDR_A_CAS#	CAS#	115	116	ODT0
		VDD15	117	118	VDD16
DDR_A_MA13		A13	119	120	ODT1
6 DDR_A_CS1#	DDR_A_CS1#	S1#	121	122	NC2
		VDD17	123	124	VDD18
		NCTEST	125	126	VREF_CA
		VSS27	127	128	VSS28
DDR_A_D32		DQ32	129	130	DQ36
DDR_A_D33		DQ33	131	132	DQ37
		VSS29	133	134	VSS30
DDR_A_DQS#4		DQS#4	135	136	DM4
DDR_A_DQS4		DQS4	137	138	VSS31
		VSS32	139	140	DQ38
DDR_A_D34		DQ34	141	142	DQ39
DDR_A_D35		DQ35	143	144	VSS33
		VSS34	145	146	DQ44
DDR_A_D40		DQ40	147	148	DQ45
DDR_A_D41		DQ41	149	150	VSS35
		VSS36	151	152	DQS#5
DDR_A_DM5		DM5	153	154	DQS5
		VSS37	155	156	VSS38
DDR_A_D42		DQ42	157	158	DQ46
DDR_A_D43		DQ43	159	160	DQ47
		VSS39	161	162	VSS40
DDR_A_D48		DQ48	163	164	DQ52
DDR_A_D49		DQ49	165	166	DQ53
		VSS41	167	168	VSS42
DDR_A_DQS#6		DQS#6	169	170	DM6
DDR_A_DQS6		DQS6	171	172	VSS43
		VSS44	173	174	DQ54
DDR_A_D50		DQ50	175	176	DQ55
DDR_A_D51		DQ51	177	178	VSS45
		VSS46	179	180	DQ60
DDR_A_D56		DQ56	181	182	DQ61
DDR_A_D57		DQ57	183	184	VSS47
		VSS48	185	186	DQS#7
DDR_A_DM7		DM7	187	188	DQS7
		VSS49	189	190	VSS50
DDR_A_D58		DQ58	191	192	DQ62
DDR_A_D59		DQ59	193	194	DQ63
		VSS51	195	196	VSS52
		SA0	197	198	EVENT#
		VDDSPD	199	200	SDA
		SA1	201	202	SCL
		VTT1	203	204	VTT2
		G1	205	206	G2

FOX_AS0A626-U8RN-7F

DDR_A_CKE1 6
DDR_A_MA15
DDR_A_MA14
DDR_A_MA11
DDR_A_MA7
DDR_A_MA6
DDR_A_MA4
DDR_A_MA2
DDR_A_MA0
DDR_A_CLK1 6
DDR_A_CLK1# 6
DDR_A_BS1 6
DDR_A_RAS# 6
DDR_A_CS0# 6
DDR_A_ODT0 6
DDR_A_ODT1 6
20mil
DDR_VREF_CA_DIMMA R202 1 2 0_0402_5%
DDR_A_D36
DDR_A_D37
DDR_A_DM4
DDR_A_D38
DDR_A_D39
DDR_A_D44
DDR_A_D45
DDR_A_DQS#5
DDR_A_DQS5
DDR_A_D46
DDR_A_D47
DDR_A_D52
DDR_A_D53
DDR_A_DM6
DDR_A_D54
DDR_A_D55
DDR_A_D60
DDR_A_D61
DDR_A_DQS#7
DDR_A_DQS7
DDR_A_D62
DDR_A_D63
PM_EXTTS#0_1
PM_EXTTS#0_1 5,11
D_CK_SDATA
D_CK_SDATA 11,12
D_CK_SCLK
D_CK_SCLK 11,12
+0.75VS

+DIMM_VREFCA
C358 2.2U_0603_6.3V4Z
C361 0.1U_0402_16V4Z

+3VS
R218 10K_0402_5%
C403 2.2U_0603_6.3V4Z
C398 0.1U_0402_16V4Z
R217 10K_0402_5%

DDR3 SO-DIMM A
H=8mm

Security Classification	Compal Secret Data		
Issued Date	2009/08/01	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: DDRIII-SODIMM SLOT1

Size: Custom | Document Number: NEW70 M/B LA-5891P Schematic | Rev: 1.0

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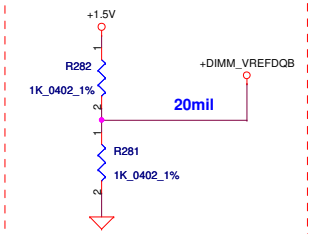
6 DDR_B_DQS#[0..7]
6 DDR_B_D[0..63]
6 DDR_B_DM[0..7]
6 DDR_B_DQS[0..7]
6 DDR_B_MA[0..15]

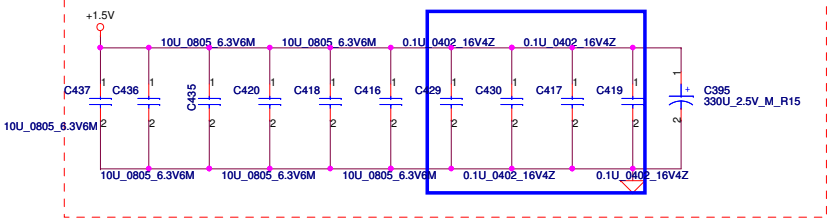
2008/9/8 #400755
Calpella Clarksfield
DDR3 SO-DIMM
VREFDQ Platform
Design Guide Change Details

DIMMB VREFDQ M1 Circuit

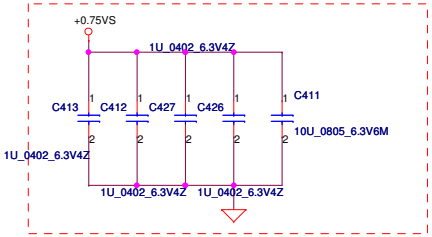


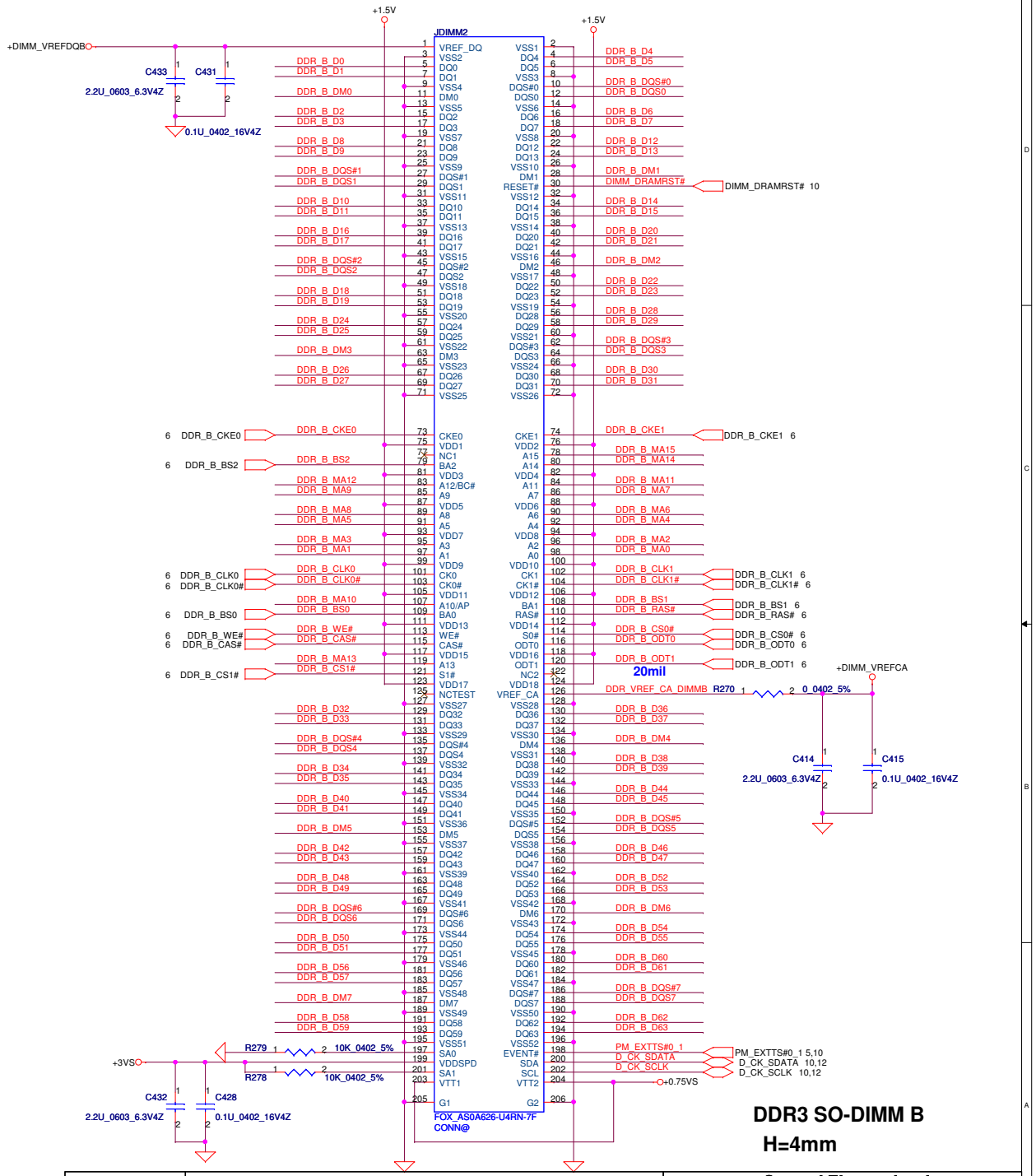
Layout Note:
Place near JDIMM2

Layout Note: Place these 4 Caps near Command and Control signals of DIMMB



Layout Note:
Place near JDIMM2.203 & JDIMM2.204





DDR3 SO-DIMM B
H=4mm

Security Classification	Compal Secret Data		
Issued Date	2009/08/01	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: DDRIII-SODIMM SLOT2

Size: Custom | Document Number: NEW70 M/B LA-5891P Schematic | Rev: 1.0

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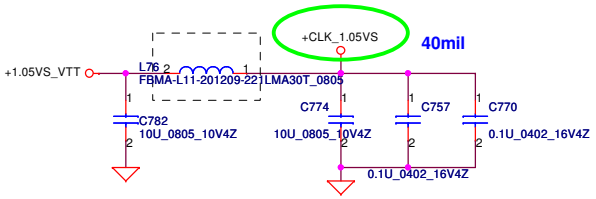
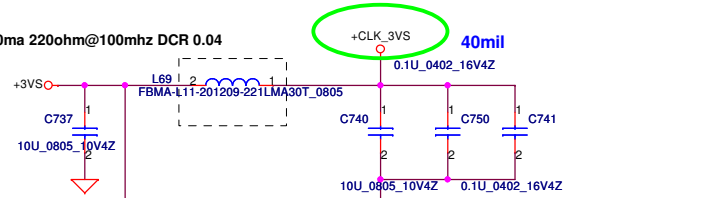
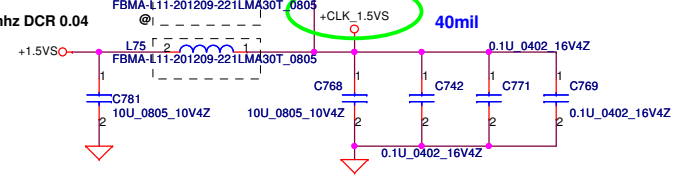
SM010014520 3000ma 220ohm@100mhz DCR 0.04



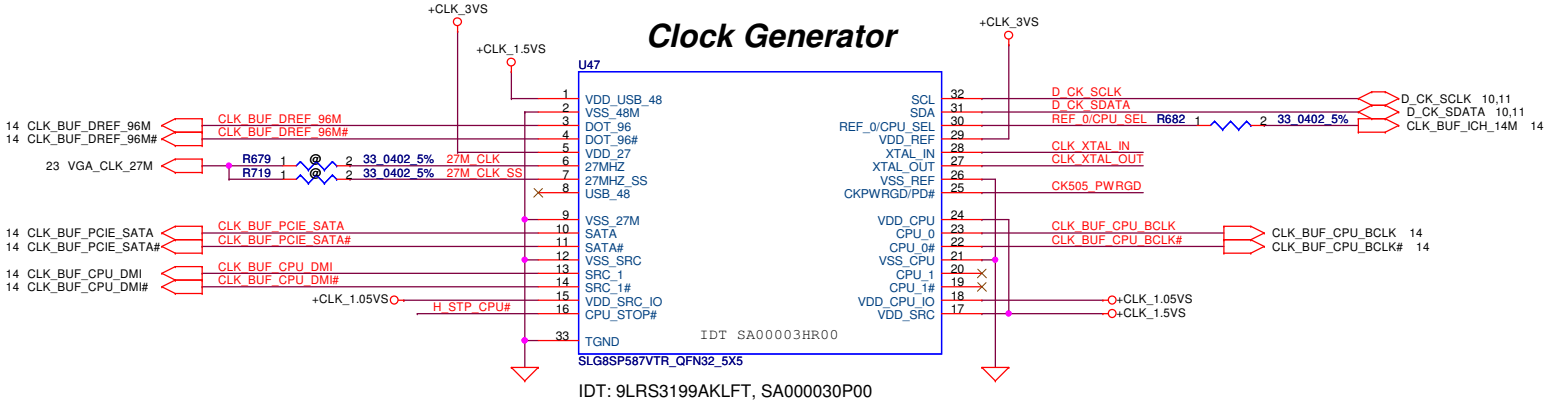
SM010014520 3000ma 220ohm@100mhz DCR 0.04



SM010014520 3000ma 220ohm@100mhz DCR 0.04



Clock Generator



IDT: 9LRS3199AKLFT, SA000030P00

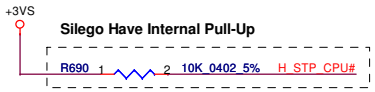
SILEGO: SLG8SP587V(WF), SA00002XY10

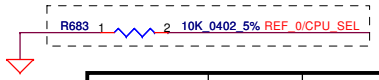
Low Power:

IDT: 9LVS3199AKLFT, SA00003HR00

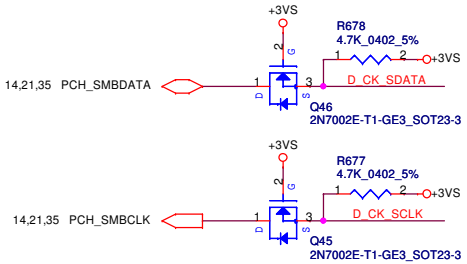
Realtek: RTM890N-631-VB-GRT, SA00003HQ10

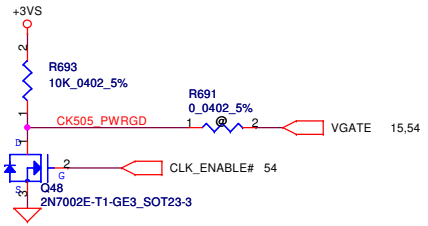
IDT 9LVS3199AKLFT NC

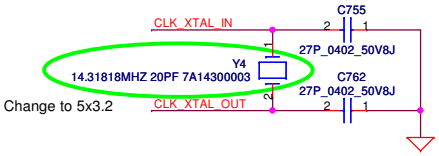




PIN 30	CPU_0	CPU_1
0 (Default)	133MHz	133MHz
1	100MHz	100MHz







Change to 5x3.2

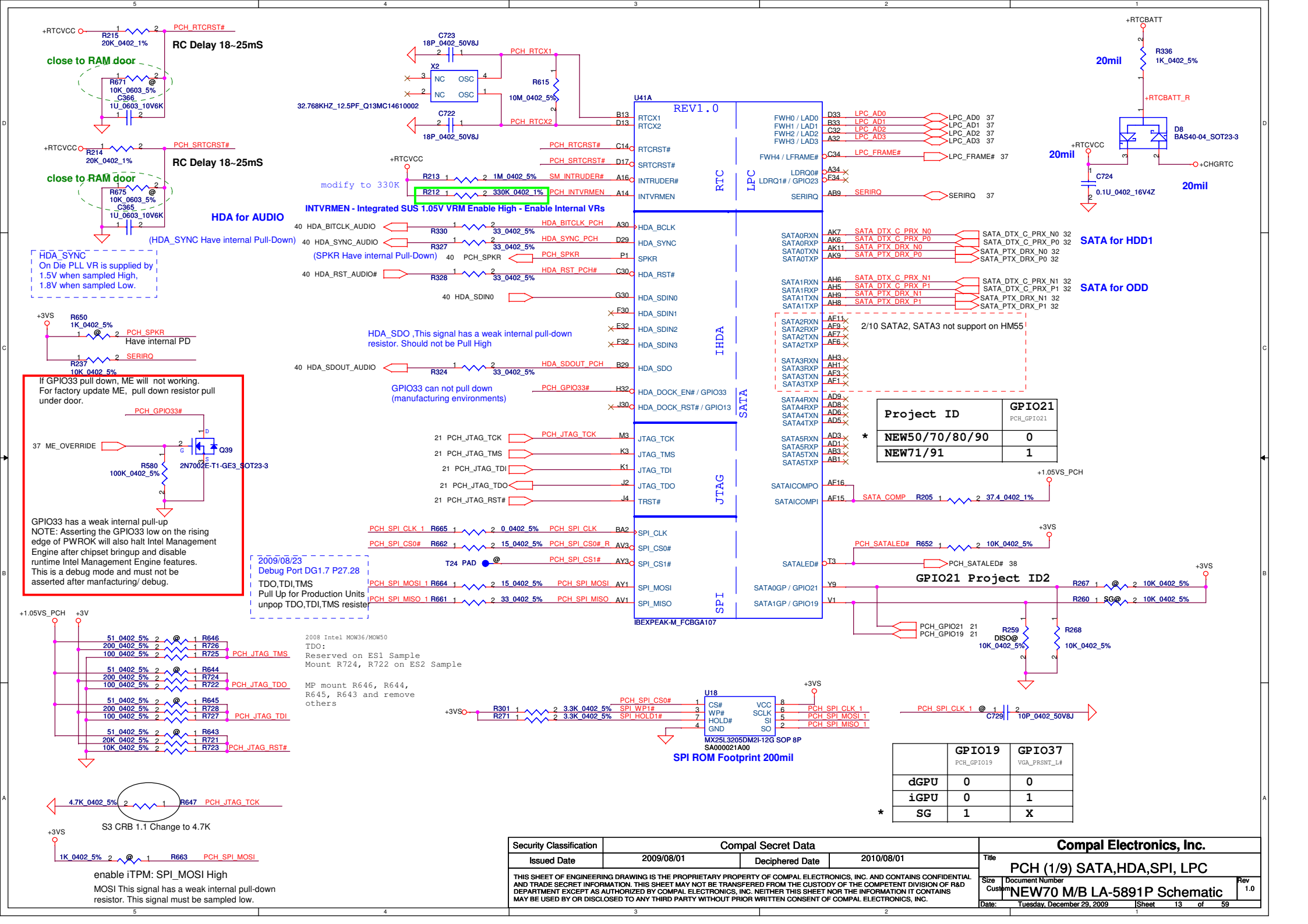
Security Classification	Compal Secret Data		
Issued Date	2009/08/01	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: Clock Generator (CK505)

Size: Custom | Document Number: NEW70 M/B LA-5891P Schematic | Rev: 1.0

Date: Tuesday, December 29, 2009 | Sheet 12 of 59


RC Delay 18~25mS
close to RAM door
R215 20K_0402_1%
R671 10K_0603_5%
C366 1U_0603_10V6K
PCH_RTCRST#
RC Delay 18~25mS
close to RAM door
R214 20K_0402_1%
R675 10K_0603_5%
C365 1U_0603_10V6K
PCH_SRTCRST#
HDA for AUDIO
(HDA_SYNC Have internal Pull-Down)
HDA_SYNC
On Die PLL VR is supplied by
1.5V when sampled High,
1.8V when sampled Low.
R650 1K_0402_5%
PCH_SPKR
Have internal PD
R237 10K_0402_5%
SERIRQ
If GPIO33 pull down, ME will not working.
For factory update ME, pull down resistor pull under door.
PCH_GPIO33#
37 ME_OVERRIDE
Q39
2N7002E-T1-GE3_SOT23-3
R580 100K_0402_5%
GPIO33 has a weak internal pull-up
NOTE: Asserting the GPIO33 low on the rising edge of PWROK will also halt Intel Management Engine after chipset bringup and disable runtime Intel Management Engine features.
This is a debug mode and must not be asserted after manfacturing/ debug.
C723 18P_0402_50V8J
X2
32.768KHZ_12.5PF_Q13MC14610002
C722 18P_0402_50V8J
PCH_RTCX1
PCH_RTCX2
R615 10M_0402_5%
+RTCVCC
R213 1M_0402_5%
SM_INTRUDER#
modify to 330K
R212 330K_0402_1%
PCH_INTVRMEN
INTVRMEN - Integrated SUS 1.05V VRM Enable High - Enable Internal VRs
40 HDA_BITCLK_AUDIO
R330 33_0402_5%
HDA_BITCLK_PCH
40 HDA_SYNC_AUDIO
R327 33_0402_5%
HDA_SYNC_PCH
(SPKR Have internal Pull-Down)
40 PCH_SPKR
PCH_SPKR
40 HDA_RST_AUDIO#
R328 33_0402_5%
HDA_RST_PCH#
40 HDA_SDIN0
HDA_SDO ,This signal has a weak internal pull-down resistor. Should not be Pull High
40 HDA_SDOUT_AUDIO
R324 33_0402_5%
HDA_SDOUT_PCH
GPIO33 can not pull down (manufacturing environments)
PCH_GPIO33#
2009/08/23
Debug Port DG1.7 P27.28
TDO,TDI,TMS
Pull Up for Production Units
unpop TDO,TDI,TMS resister
21 PCH_JTAG_TCK
21 PCH_JTAG_TMS
21 PCH_JTAG_TDI
21 PCH_JTAG_TDO
21 PCH_JTAG_RST#
PCH_SPI_CLK_1 R665 0_0402_5%
PCH_SPI_CS0# R662 15_0402_5%
T24 PAD
PCH_SPI_CS1#
PCH_SPI_MOSI_1 R664 15_0402_5%
PCH_SPI_MISO_1 R661 33_0402_5%
U41A
REV1.0
RTC
LPC
IHDA
SATA
JTAG
SPI
RTCX1
RTCX2
RTCRST#
SRTCRST#
INTRUDER#
INTVRMEN
HDA_BCLK
HDA_SYNC
SPKR
HDA_RST#
HDA_SDIN0
HDA_SDIN1
HDA_SDIN2
HDA_SDIN3
HDA_SDO
HDA_DOCK_EN# / GPIO33
HDA_DOCK_RST# / GPIO13
JTAG_TCK
JTAG_TMS
JTAG_TDI
JTAG_TDO
TRST#
SPI_CLK
SPI_CS0#
SPI_CS1#
SPI_MOSI
SPI_MISO
FWH0 / LAD0
FWH1 / LAD1
FWH2 / LAD2
FWH3 / LAD3
FWH4 / LFRAME#
LDRQ0#
LDRQ1# / GPIO23
SERIRQ
SATA0RXN
SATA0RXP
SATA0TXN
SATA0TXP
SATA1RXN
SATA1RXP
SATA1TXN
SATA1TXP
SATA2RXN
SATA2RXP
SATA2TXN
SATA2TXP
SATA3RXN
SATA3RXP
SATA3TXN
SATA3TXP
SATA4RXN
SATA4RXP
SATA4TXN
SATA4TXP
SATA5RXN
SATA5RXP
SATA5TXN
SATA5TXP
SATAICOMPO
SATAICOMPI
SATALED#
SATA0GP / GPIO21
SATA1GP / GPIO19
IBEXPEAK-M_FCBGA107
LPC_AD0 37
LPC_AD1 37
LPC_AD2 37
LPC_AD3 37
LPC_FRAME# 37
SERIRQ 37
SATA_DTX_C_PRX_N0 32
SATA_DTX_C_PRX_P0 32
SATA_PTX_DRX_N0 32
SATA_PTX_DRX_P0 32
SATA for HDD1
SATA_DTX_C_PRX_N1 32
SATA_DTX_C_PRX_P1 32
SATA_PTX_DRX_N1 32
SATA_PTX_DRX_P1 32
SATA for ODD
2/10 SATA2, SATA3 not support on HM55
SATA_COMP R205 37.4_0402_1%
+1.05VS_PCH
PCH_SATALED# R652 10K_0402_5%
PCH_SATALED# 38
GPIO21 Project ID2
R267 10K_0402_5%
R260 SG@ 10K_0402_5%
PCH_GPIO21 21
PCH_GPIO19 21
R259 DISO@ 10K_0402_5%
R268 10K_0402_5%
Project ID | GPIO21 (PCH_GPIO21)
NEW50/70/80/90 | 0
NEW71/91 | 1
+RTCBATT
R336 1K_0402_5%
20mil
+RTCBATT_R
D8 BAS40-04_SOT23-3
+CHGRTC
C724 0.1U_0402_16V4Z
+3VS
51_0402_5% R646
200_0402_5% R726
100_0402_5% R725
PCH_JTAG_TMS
51_0402_5% R644
200_0402_5% R724
100_0402_5% R722
PCH_JTAG_TDO
51_0402_5% R645
200_0402_5% R728
100_0402_5% R727
PCH_JTAG_TDI
51_0402_5% R643
20K_0402_5%
10K_0402_5% R721 R723
PCH_JTAG_RST#
2008 Intel MOW36/MOW50
TDO:
Reserved on ES1 Sample
Mount R724, R722 on ES2 Sample
MP mount R646, R644, R645, R643 and remove others
4.7K_0402_5% R647
PCH_JTAG_TCK
S3 CRB 1.1 Change to 4.7K
1K_0402_5% R663
PCH_SPI_MOSI
enable iTPM: SPI_MOSI High
MOSI This signal has a weak internal pull-down resistor. This signal must be sampled low.
U18
CS# WP# HOLD# GND VCC SCLK SI SO
R301 3.3K_0402_5%
R271 3.3K_0402_5%
SPI_WP1#
SPI_HOLD1#
PCH_SPI_CS0#
PCH_SPI_CLK_1
PCH_SPI_MOSI_1
PCH_SPI_MISO_1
C729 10P_0402_50V8J
MX25L3205DM2I-12G SOP 8P
SA000021A00
SPI ROM Footprint 200mil
GPIO19 (PCH_GPIO19) | GPIO37 (VGA_PRSNT_L#)
dGPU | 0 | 0
iGPU | 0 | 1
SG | 1 | X
Security Classification: Compal Secret Data
Issued Date: 2009/08/01
Deciphered Date: 2010/08/01
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Compal Electronics, Inc.
Title: PCH (1/9) SATA,HDA,SPI, LPC
Size: Custom
Document Number: NEW70 M/B LA-5891P Schematic
Rev: 1.0
Date: Tuesday, December 29, 2009
Sheet 13 of 59

1. Connect Directly EXPRESS CARD, MINI1, MINI2
2. Level Shift1, Pull-Up to +3VS CLOCK GEN, DIMM1, DIMM2
3. Level Shift2, Pull-Up to +3VS LAN
4. Level Shift3, Pull-Up to +3VS CPU & PCH XDP

U41B REV1.0

For PCIE LAN
For Wireless LAN
For Mini2
2009/08/25: remove PCIE5
2/10 PCIE7, PCIE8 not support on HM55
For PCIE LAN
For Wireless LAN
2009/08/25: Change back to +3V remove mini2
2009/08/25: remove mini2 clk

6/9 MOW23 Request add 25MHz crystal supporting Integrated Graphics
Change to 5x3.2
1109 RF request
Project Structure ID
1216 GPIO65 PULL HIGH:PVT PULL DOWN:DVT
1222 GPIO66 PULL HIGH:8L PULL DOWN:6L

Project Structure			
GPIO21 ID2	GPIO65 ID1	GPIO66 ID0	Structure
0	0	0	DVT
0	0	1	
* 0	1	0	PVT

9/1: Change to +3VS
2009/08/13: Change back to +3V

Pull high +3VS at KB926 side

IBEXPEAK-M_FCBGA107

Security Classification	Compal Secret Data		
Issued Date	2009/08/01	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: PCH (2/9) PCIE, SMBUS, CLK

Size: Custom | Document Number: NEW70 M/B LA-5891P Schematic | Rev: 1.0

Date: Friday, January 08, 2010 | Sheet 14 of 59

4 DMI_HTX_PRX_N[0..3] DMI_HTX_PRX_N[0..3]
4 DMI_HTX_PRX_P[0..3] DMI_HTX_PRX_P[0..3]
4 DMI_PTX_HRX_N[0..3] DMI_PTX_HRX_N[0..3]
4 DMI_PTX_HRX_P[0..3] DMI_PTX_HRX_P[0..3]

4 H_FDI_TXN[0..7] H_FDI_TXN[0..7]
4 H_FDI_TXP[0..7] H_FDI_TXP[0..7]

+3VS
R657 1 2 8.2K_0402_5%
PM_CLKRUN#

+3V
R648 1 2 10K_0402_5% SUS_PWR_DN_ACK
R628 1 2 8.2K_0402_5% PCH_GPIO72
R198 1 2 10K_0402_5% EC_SWI#
R641 1 2 10K_0402_5% PCH_PCIE_WAKE#
R248 1 @ 2 10K_0402_5% PM_SLP_LAN#

+1.05VS_PCH
R600 49.9_0402_1% 1 2 DMI_COMP

09/09/14 WW37 PCH WAKE# PU 10K

U41C

DMI_HTX_PRX_N0 BC24 DMI0RXN
DMI_HTX_PRX_N1 BJ22 DMI1RXN
DMI_HTX_PRX_N2 AW20 DMI2RXN
DMI_HTX_PRX_N3 BJ20 DMI3RXN
DMI_HTX_PRX_P0 BD24 DMI0RXP
DMI_HTX_PRX_P1 BG22 DMI1RXP
DMI_HTX_PRX_P2 BA20 DMI2RXP
DMI_HTX_PRX_P3 BG20 DMI3RXP
DMI_PTX_HRX_N0 BE22 DMI0TXN
DMI_PTX_HRX_N1 BF21 DMI1TXN
DMI_PTX_HRX_N2 BD20 DMI2TXN
DMI_PTX_HRX_N3 BE18 DMI3TXN
DMI_PTX_HRX_P0 BD22 DMI0TXP
DMI_PTX_HRX_P1 BH21 DMI1TXP
DMI_PTX_HRX_P2 BC20 DMI2TXP
DMI_PTX_HRX_P3 BD18 DMI3TXP
BH25 DMI_ZCOMP
BF25 DMI_IRCOMP

DMI

FDI_RXN0 BA18 H_FDI_TXN0
FDI_RXN1 BH17 H_FDI_TXN1
FDI_RXN2 BD16 H_FDI_TXN2
FDI_RXN3 BJ16 H_FDI_TXN3
FDI_RXN4 BA16 H_FDI_TXN4
FDI_RXN5 BE14 H_FDI_TXN5
FDI_RXN6 BA14 H_FDI_TXN6
FDI_RXN7 BC12 H_FDI_TXN7
FDI_RXP0 BB18 H_FDI_TXP0
FDI_RXP1 BF17 H_FDI_TXP1
FDI_RXP2 BC16 H_FDI_TXP2
FDI_RXP3 BG16 H_FDI_TXP3
FDI_RXP4 AW16 H_FDI_TXP4
FDI_RXP5 BD14 H_FDI_TXP5
FDI_RXP6 BB14 H_FDI_TXP6
FDI_RXP7 BD12 H_FDI_TXP7
FDI_INT BJ14 H_FDI_INT 4
FDI_FSYNC0 BF13 H_FDI_FSYNC0 4
FDI_FSYNC1 BH13 H_FDI_FSYNC1 4
FDI_LSYNC0 BJ12 H_FDI_LSYNC0 4
FDI_LSYNC1 BG14 H_FDI_LSYNC1 4

REV1.0

5,21 XDP_DBRESET# XDP_DBRESET# T6 SYS_RESET#
SYS_PWROK R620 2 @ 1 0_0402_5% SYS_PWROK_R M6 SYS_PWROK
VGATE R631 2 @ 1 0_0402_5%
SYS_PWROK B17 PWROK
K5 MEPWROK
LAN_RST# A10 LAN_RST#
5 PM_DRAM_PWRGD D9 DRAMPWROK
PCH_RSMRST# C16 RSMRST#
37 SUS_PWR_DN_ACK SUS_PWR_DN_ACK M1 SUS_PWR_DN_ACK / GPIO30
5,21,37 PBTN_OUT# PBTN_OUT# P5 PWRBTN#
+3V R240 1 2 10K_0402_5%
23,37 EC_ACIN 1 2 D6 CH751H-40PT_SOD323-2 PCH_ACIN P7 ACPRESENT / GPIO31
PCH_GPIO72 A6 BATLOW# / GPIO72
37 EC_SWI# EC_SWI# F14 RI#

System Power Management

WAKE# J12 PCH_PCIE_WAKE# PCH_PCIE_WAKE# 33,35
CLKRUN# / GPIO32 Y1 PM_CLKRUN# PM_CLKRUN# 37
SUS_STAT# / GPIO61 P8 PCH_GPIO61 @ PAD T10
SUSCLK / GPIO62 F3 SUSCLK SUSCLK 37
SLP_S5# / GPIO63 E4 PM_SLP_S5# 37
SLP_S4# H7 PM_SLP_S4# 37
SLP_S3# P12 PM_SLP_S3# 37
SLP_M# K8 PM_SLP_M# @ PAD T11
TP23 N2 PM_SLP_DSW# @ PAD T22
PMSYNCH BJ10 H_PM_SYNC 5
SLP_LAN# / GPIO29 F6 PM_SLP_LAN#

IBEXPEAK-M_FCBGA107

+3VS
21 SYS_PWROK SYS_PWROK 4 Y
U44 5 B 2 EC_PWROK EC_PWROK 37,39
A 1 VGATE VGATE 12,54
3
MC74VHC1G08DFT2G_SC70-5

SYS_PWROK R606 1 2 10K_0402_5%
EC_PWROK R632 1 2 10K_0402_5%
LAN_RST# R617 1 2 10K_0402_5%

No used Integrated LAN,
connecting LAN_RST# to GND

R605 2 @ 1 0_0402_5%
Q41 MMBT3906_SOT23-3
PCH_RSMRST# 1 3 EC_RSMRST# 37
2
R604 10K_0402_5%
R598 1 2 4.7K_0402_5% +3V
D20A 1 6
2 5
BAV99DW-7_SOT363
D20B 4 3
5 2
BAV99DW-7_SOT363
R591 2.2K_0402_5%

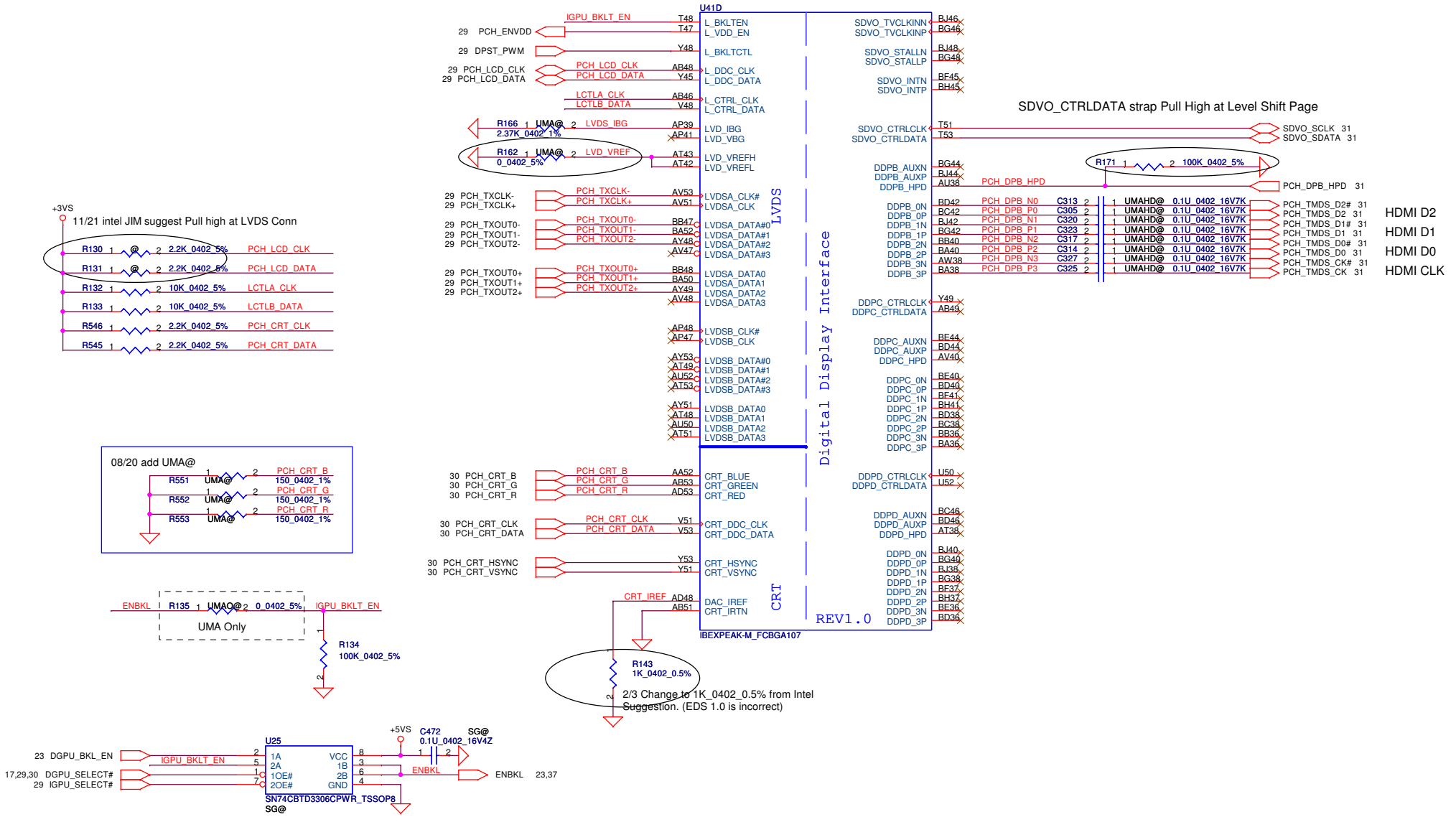
Security Classification	Compal Secret Data		
Issued Date	2009/08/01	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: PCH (3/9) DMI, FDI, PM

Size: Custom | Document Number: NEW70 M/B LA-5891P Schematic | Rev: 1.0

Date: Tuesday, December 29, 2009 | Sheet 15 of 59



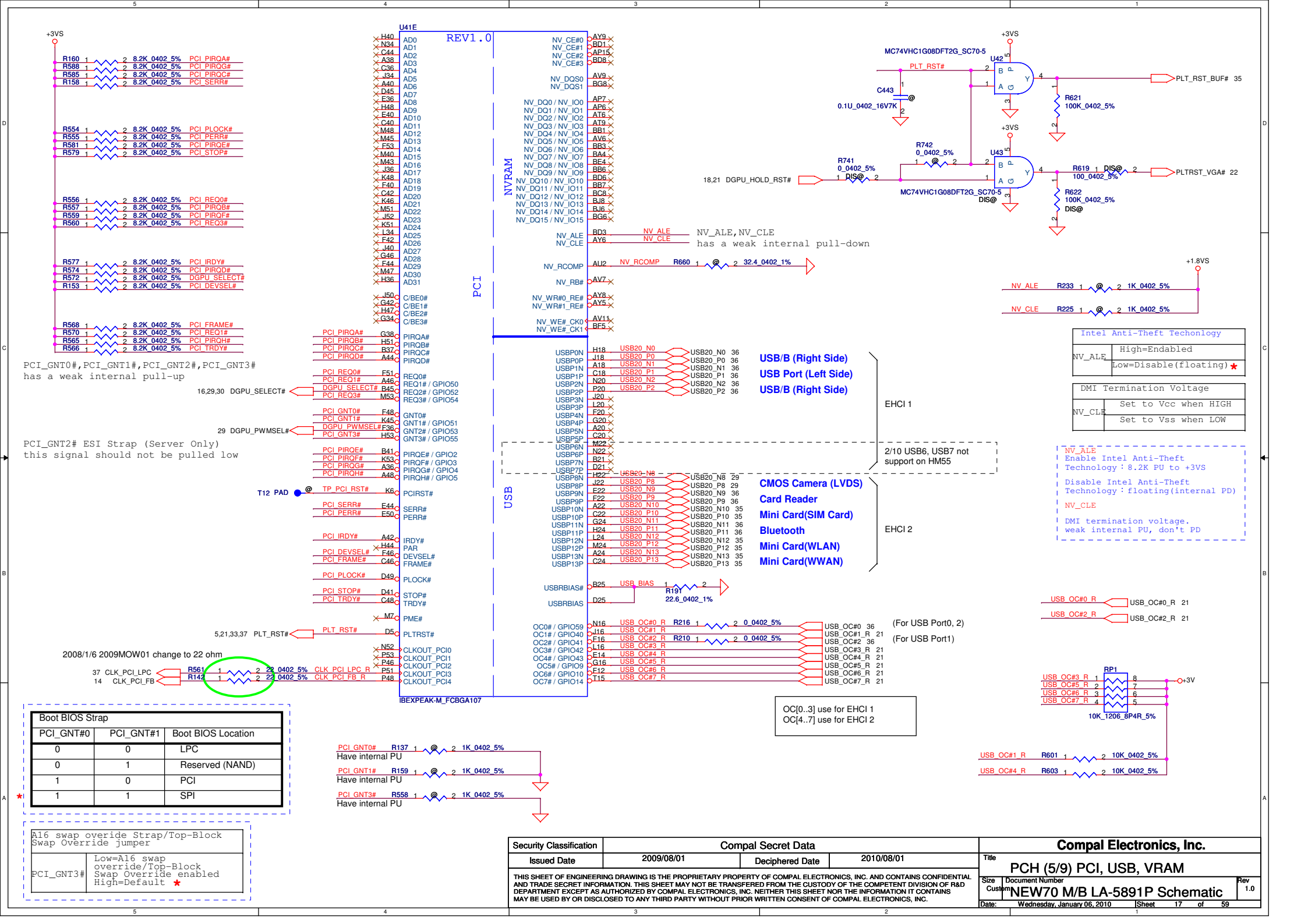
Security Classification	Compal Secret Data		
Issued Date	2009/08/01	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: PCH (4/9) LVDS, CRT, DPI

Size: Custom | Document Number: NEW70 M/B LA-5891P Schematic | Rev: 1.0

Date: Tuesday, December 29, 2009 | Sheet 16 of 59



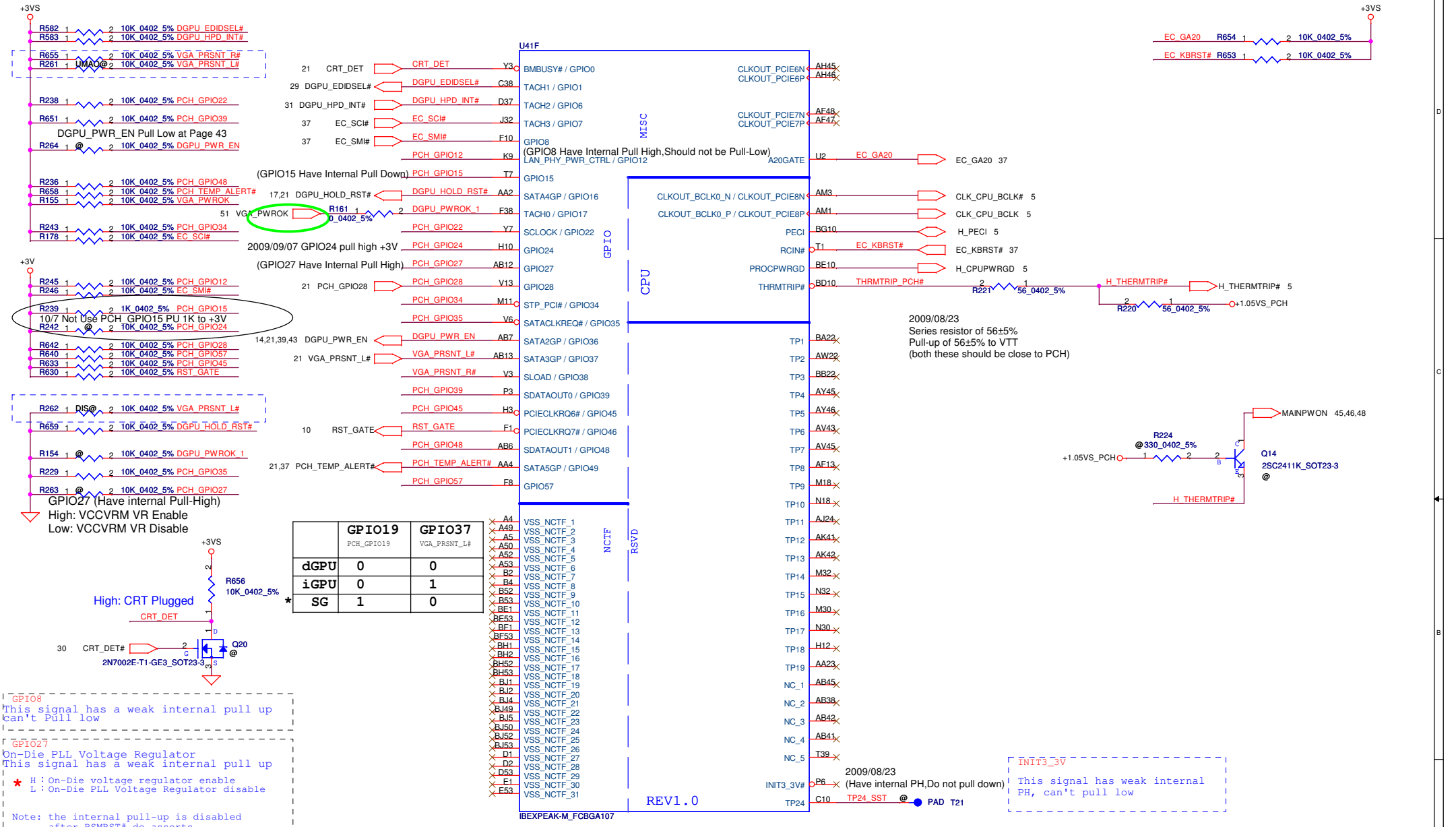
Security Classification	Compal Secret Data		
Issued Date	2009/08/01	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: PCH (5/9) PCI, USB, VRAM

Size: Custom | Document Number: NEW70 M/B LA-5891P Schematic | Rev: 1.0

Date: Wednesday, January 06, 2010 | Sheet 17 of 59



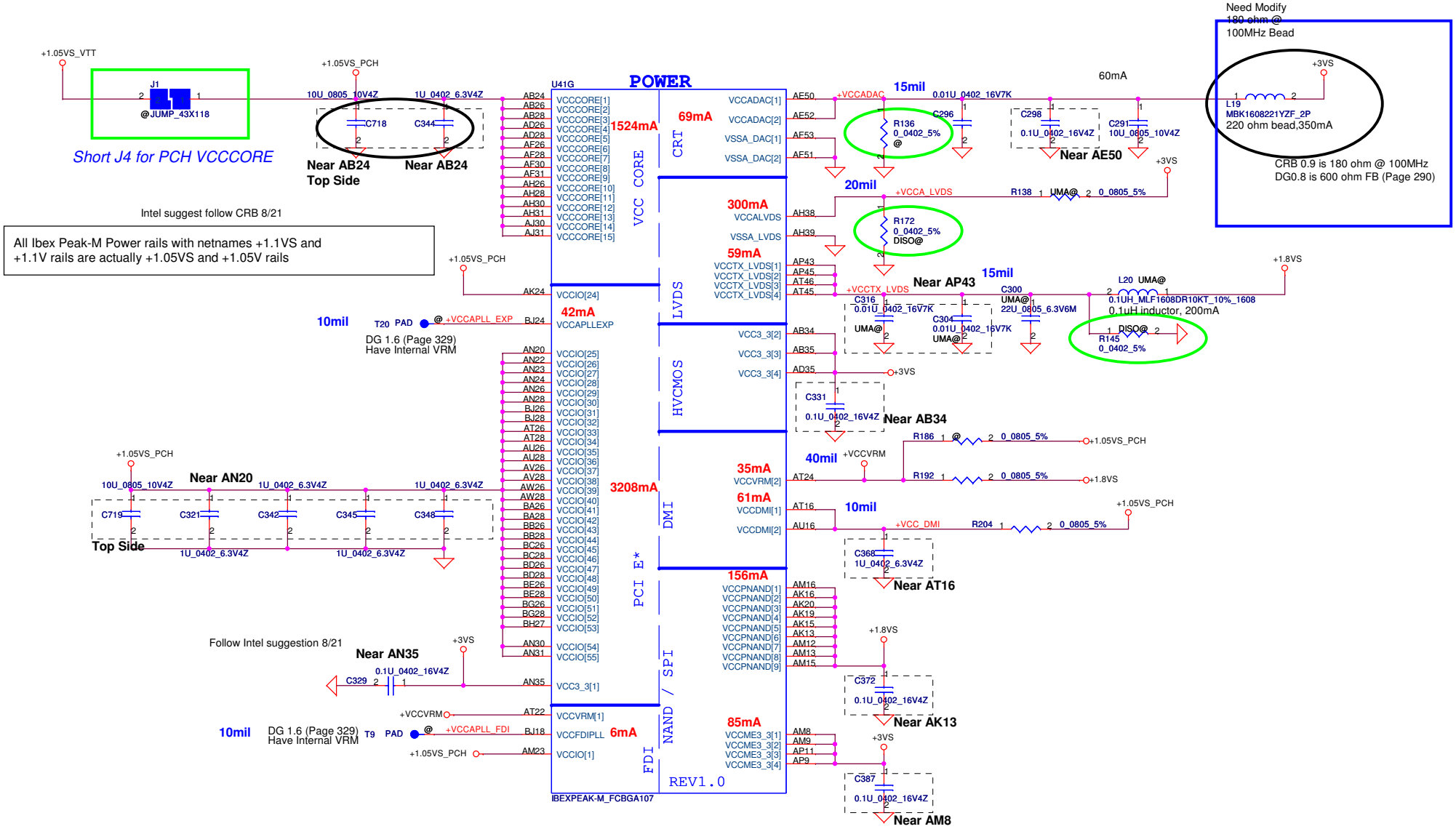
Security Classification	Compal Secret Data		
Issued Date	2009/08/01	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: PCH (6/9) GPIO, CPU, MISC

Size: Custom | Document Number: NEW70 M/B LA-5891P Schematic | Rev: 1.0

Date: Tuesday, December 29, 2009 | Sheet 18 of 59



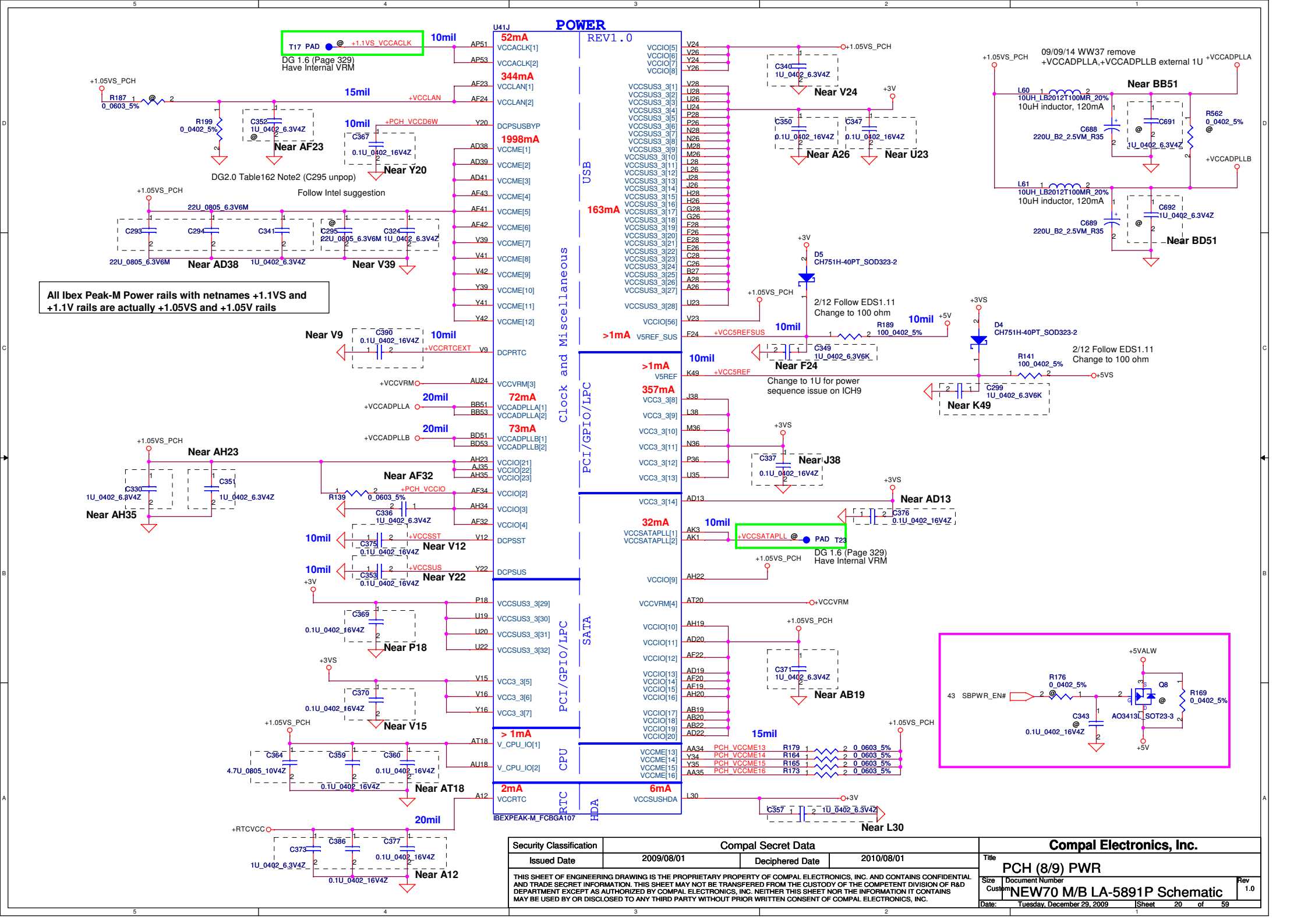
Security Classification	Compal Secret Data		
Issued Date	2009/08/01	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: PCH (7/9) PWR

Size: Custom | Document Number: NEW70 M/B LA-5891P Schematic | Rev: 1.0

Date: Tuesday, December 29, 2009 | Sheet 19 of 59



Security Classification	Compal Secret Data		
Issued Date	2009/08/01	Deciphered Date	2010/08/01

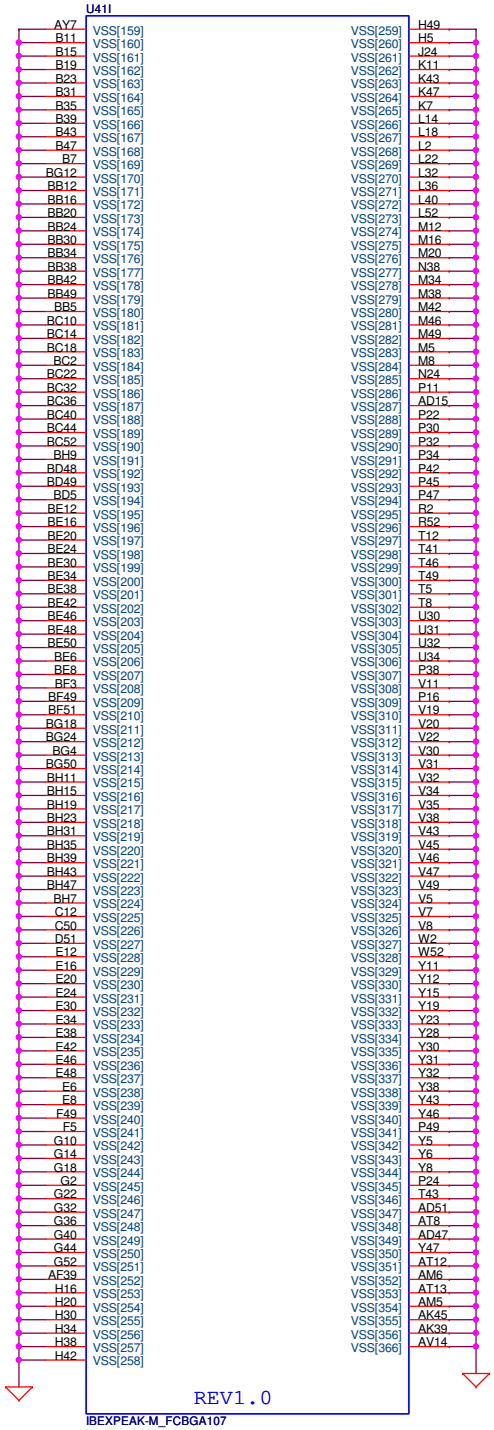
Compal Electronics, Inc.

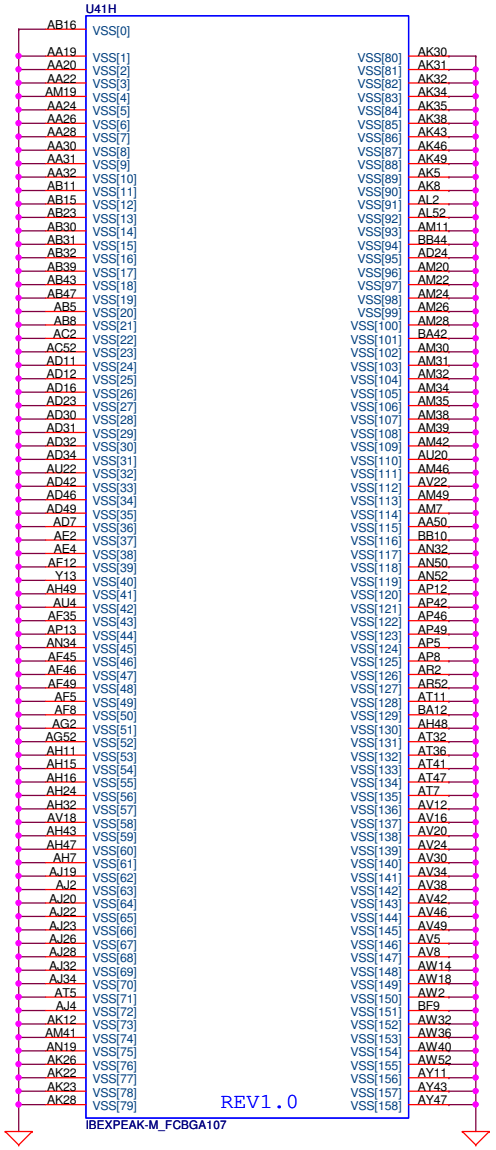
Title: PCH (8/9) PWR

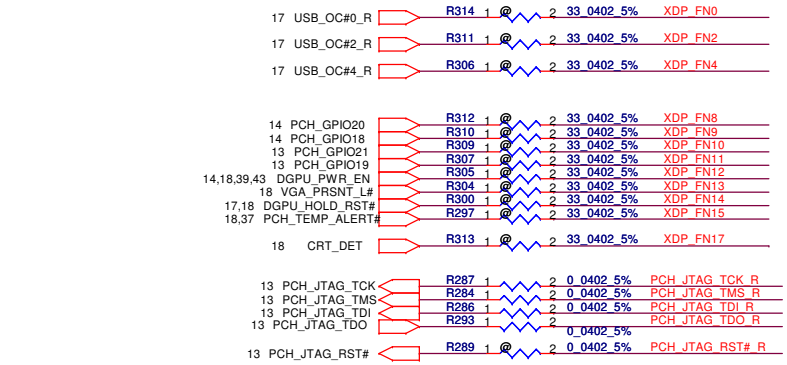
Size: Custom | Document Number: NEW70 M/B LA-5891P Schematic | Rev: 1.0

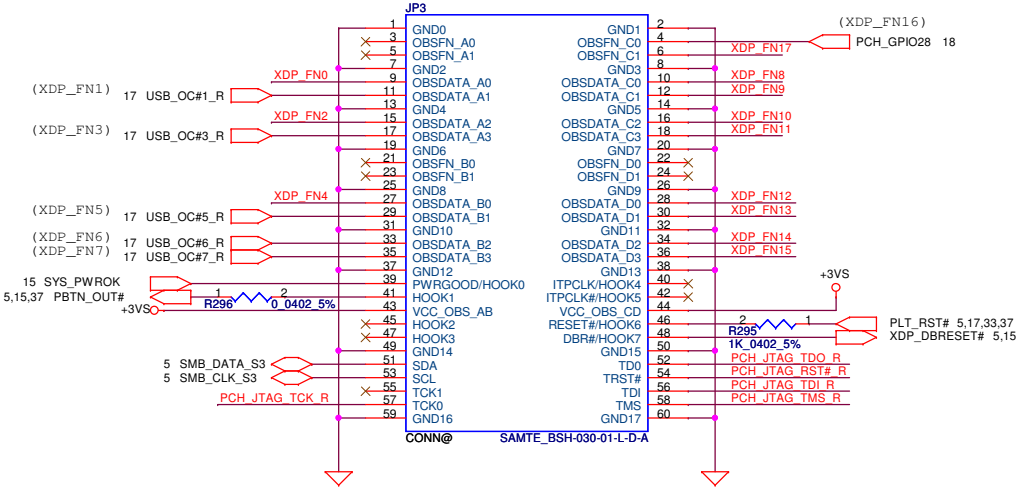
Date: Tuesday, December 29, 2009 | Sheet 20 of 59

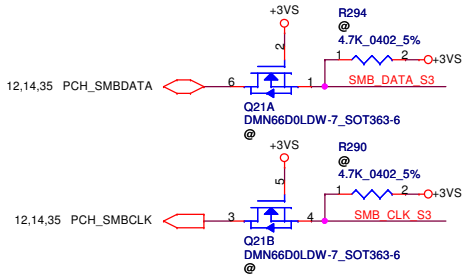
PCH XDP Port











Security Classification	Compal Secret Data		
Issued Date	2009/08/01	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: PCH (9/9) VSS & PCH XDP Port

Size: Custom | Document Number: NEW70 M/B LA-5891P Schematic | Rev: 1.0

Date: Thursday, January 07, 2010 | Sheet 21 of 59

4 PEG_GTX_HRX_N[0..15]
4 PEG_GTX_HRX_P[0..15]

4 PEG_HTX_C_GRX_N[0..15]
4 PEG_HTX_C_GRX_P[0..15]

GFX PCIE LANE REVERSAL

U34A

PCI EXPRESS INTERFACE

PEG_HTX_C_GRX_P0	AA38	PCIE_RX0P	PCIE_TX0P	Y33	PEG_GTX_HRX_P0
PEG_HTX_C_GRX_N0	Y37	PCIE_RX0N	PCIE_TX0N	Y32	PEG_GTX_HRX_N0
PEG_HTX_C_GRX_P1	Y35	PCIE_RX1P	PCIE_TX1P	W33	PEG_GTX_HRX_P1
PEG_HTX_C_GRX_N1	W36	PCIE_RX1N	PCIE_TX1N	W32	PEG_GTX_HRX_N1
PEG_HTX_C_GRX_P2	W38	PCIE_RX2P	PCIE_TX2P	U33	PEG_GTX_HRX_P2
PEG_HTX_C_GRX_N2	V37	PCIE_RX2N	PCIE_TX2N	U32	PEG_GTX_HRX_N2
PEG_HTX_C_GRX_P3	V35	PCIE_RX3P	PCIE_TX3P	U30	PEG_GTX_HRX_P3
PEG_HTX_C_GRX_N3	U36	PCIE_RX3N	PCIE_TX3N	U29	PEG_GTX_HRX_N3
PEG_HTX_C_GRX_P4	U38	PCIE_RX4P	PCIE_TX4P	T33	PEG_GTX_HRX_P4
PEG_HTX_C_GRX_N4	T37	PCIE_RX4N	PCIE_TX4N	T32	PEG_GTX_HRX_N4
PEG_HTX_C_GRX_P5	T35	PCIE_RX5P	PCIE_TX5P	T30	PEG_GTX_HRX_P5
PEG_HTX_C_GRX_N5	R36	PCIE_RX5N	PCIE_TX5N	T29	PEG_GTX_HRX_N5
PEG_HTX_C_GRX_P6	R38	PCIE_RX6P	PCIE_TX6P	P33	PEG_GTX_HRX_P6
PEG_HTX_C_GRX_N6	P37	PCIE_RX6N	PCIE_TX6N	P32	PEG_GTX_HRX_N6
PEG_HTX_C_GRX_P7	P35	PCIE_RX7P	PCIE_TX7P	P30	PEG_GTX_HRX_P7
PEG_HTX_C_GRX_N7	N36	PCIE_RX7N	PCIE_TX7N	P29	PEG_GTX_HRX_N7
PEG_HTX_C_GRX_P8	N38	PCIE_RX8P	PCIE_TX8P	N33	PEG_GTX_HRX_P8
PEG_HTX_C_GRX_N8	M37	PCIE_RX8N	PCIE_TX8N	N32	PEG_GTX_HRX_N8
PEG_HTX_C_GRX_P9	M35	PCIE_RX9P	PCIE_TX9P	N30	PEG_GTX_HRX_P9
PEG_HTX_C_GRX_N9	L36	PCIE_RX9N	PCIE_TX9N	N29	PEG_GTX_HRX_N9
PEG_HTX_C_GRX_P10	L38	PCIE_RX10P	PCIE_TX10P	L33	PEG_GTX_HRX_P10
PEG_HTX_C_GRX_N10	K37	PCIE_RX10N	PCIE_TX10N	L32	PEG_GTX_HRX_N10
PEG_HTX_C_GRX_P11	K35	PCIE_RX11P	PCIE_TX11P	L30	PEG_GTX_HRX_P11
PEG_HTX_C_GRX_N11	J36	PCIE_RX11N	PCIE_TX11N	L29	PEG_GTX_HRX_N11
PEG_HTX_C_GRX_P12	J38	PCIE_RX12P	PCIE_TX12P	K33	PEG_GTX_HRX_P12
PEG_HTX_C_GRX_N12	H37	PCIE_RX12N	PCIE_TX12N	K32	PEG_GTX_HRX_N12
PEG_HTX_C_GRX_P13	H35	PCIE_RX13P	PCIE_TX13P	J33	PEG_GTX_HRX_P13
PEG_HTX_C_GRX_N13	G36	PCIE_RX13N	PCIE_TX13N	J32	PEG_GTX_HRX_N13
PEG_HTX_C_GRX_P14	G38	PCIE_RX14P	PCIE_TX14P	K30	PEG_GTX_HRX_P14
PEG_HTX_C_GRX_N14	F37	PCIE_RX14N	PCIE_TX14N	K29	PEG_GTX_HRX_N14
PEG_HTX_C_GRX_P15	F35	PCIE_RX15P	PCIE_TX15P	H33	PEG_GTX_HRX_P15
PEG_HTX_C_GRX_N15	E37	PCIE_RX15N	PCIE_TX15N	H32	PEG_GTX_HRX_N15

CLOCK

14 CLK_PEG_VGA — AB35 PCIE_REFCLKP
14 CLK_PEG_VGA# — AA36 PCIE_REFCLKN

For M96, AH16 is NC

AJ21 NC#1
AK21 NC#2
2 VGA@ 1 R498 10K_0402_5% — AH16 NC_PWRGOOD

17 PLTRST_VGA# — AA30 PERSTB

CALIBRATION

PCIE_CALRP Y30 — R55 1 VGA@ 2 1.27K_0402_1%
PCIE_CALRN Y29 — R52 1 VGA@ 2 2K_0402_1% — +1.0VSDGPU

216-0729002 A12 M96_BGA962
MADI@

Park XT P/N : SA00003M500 (S IC 216-0774009 A11 PARK XT S3 631P C38)

Madision Pro P/N : SA00003M300 (S IC 216-0772000 MADISON PRO FCBGA 0FA)

add for VB support.

U34G

LVDS CONTROL

VARY_BL AK27 — R73 10K_0402_5% 1 VGA@ 2 — VGA_PNL_PWM 29
DIGON AJ27 — R76 1 VGA@ 2 10K_0402_5% — ENVDD 29

TXCLK_UP_DPF3P	AK35		
TXCLK_UN_DPF3N	AL36		
TXOUT_U0P_DPF2P	AJ38		
TXOUT_U0N_DPF2N	AK37		
TXOUT_U1P_DPF1P	AH35		
TXOUT_U1N_DPF1N	AJ36		
TXOUT_U2P_DPF0P	AG38		
TXOUT_U2N_DPF0N	AH37		
TXOUT_U3P	AF35		
TXOUT_U3N	AG36		

LVTMDP

TXCLK_LP_DPE3P	AP34	VGA_TXCLK+	VGA_TXCLK+ 29
TXCLK_LN_DPE3N	AR34	VGA_TXCLK-	VGA_TXCLK- 29
TXOUT_L0P_DPE2P	AW37	VGA_TXOUT0+	VGA_TXOUT0+ 29
TXOUT_L0N_DPE2N	AU35	VGA_TXOUT0-	VGA_TXOUT0- 29
TXOUT_L1P_DPE1P	AR37	VGA_TXOUT1+	VGA_TXOUT1+ 29
TXOUT_L1N_DPE1N	AU39	VGA_TXOUT1-	VGA_TXOUT1- 29
TXOUT_L2P_DPE0P	AP35	VGA_TXOUT2+	VGA_TXOUT2+ 29
TXOUT_L2N_DPE0N	AR35	VGA_TXOUT2-	VGA_TXOUT2- 29
TXOUT_L3P	AN36		
TXOUT_L3N	AP37		

216-0729002 A12 M96_BGA962
MADI@

Security Classification	Compal Secret Data		
Issued Date	2009/08/01	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: M96_ PCIE / LVDS

Size: Custom | Document Number: NEW70 M/B LA-5891P Schematic | Rev: 1.0

Date: Tuesday, December 29, 2009 | Sheet 22 of 59

Strap Name		Pin Straps description <all internal PD>	Setting
VIP_DEVICE_EN	V2SYNC	VIP Device Strap Enable indicates to the software driver 0: Driver would ignore the value sampled on VHAD_0 during reset 1: VHAD_0 to determine whether or not a VIP slave device	0
VGA_DIS	GPIO9	VGA Disable determines 0: VGA Controller capacity enabled 1: The device will not be recognized as the system's VGA controller	0
TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis diabled for mobile mode 1: Tx de-emphasis enabled (Defailt setting for desktop)	1
CONFIG[2] CONFIG[1] CONFIG[0]	GPIO13 GPIO12 GPIO11	GPIO13,12,11 (config 2,1,0) : a) If BIOS_ROM_EN = 1, then Config[2:0] defines the ROM type. (memory apertures CONFIG[3:0]) b) If BIOS_ROM_EN = 0, then Config[2:0] defines the primary memory aperture size. 128 MB 000 256 MB 001 * 64 MB 010	001
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device 0: Diable, 1: Enable	0
AUD[1] AUD(0)	HSYNC VSYNC	00: No audio function; 10: Audio for DisplayPort only; 01: Audio for DisplayPort and HDMI if adapter is detected; 11: Audio for both DisplayPort and HDMI	11
BIF_GEN2_EN	GPIO2	0= Advertises the PCI-E device as 2.5 GT/s capable at power-on 1= Advertises the PCI-E device as 5.0 GT/s capable at power-on 5.0 GT/s capability will be controlled by software	0
RESERVED	H2SYNC GPIO8 GPIO21	Internal use only. THIS PAD HAS AN INTERNAL PULL-DOWN AND MUST BE 0 V AT RESET. The pad may be left unconnected	

External VGA Thermal Sensor

+3VSDGPU, C283 0.1U_0402_16V4Z VGA@, U9 ADM1032ARMZ-2REEL_MSOP8 VGA@ (VDD, SCLK, D+, SDATA, D-, ALERT#, THERM#, GND), GPU_THERM_D+, GPU_THERM_D-, 2200P_0402_50V7K VGA@ C247, VGA_SMB_CK2, VGA_SMB_DA2, THM_ALERT#, R102 4.7K_0402_5% VGA@, +3VSDGPU

+3VSDGPU, R108 4.7K_0402_5% VGA@, R115 4.7K_0402_5% VGA@, +3VSDGPU, VGA_SMB_CK2, Q5B DMN66D0LDW-7_SOT363-6 VGA@, EC_SMB_CK2 14,37, VGA_SMB_DA2, Q5A DMN66D0LDW-7_SOT363-6 VGA@, EC_SMB_DA2 14,37

+3VSDGPU

+3VS, AO3413L_SOT23-3 Q6, 100mA, +3VSDGPU, R120 0_0603_5%, C609 0.1U_0402_16V7K VGA@, R128 100K_0402_5% VGA@, C279 10U_0805_6.3V6M VGA@, R106 470_0603_5% VGA@, R739 24K_0402_1% VGA@, Q4 2N7002E-T1-GE3_SOT23-3 VGA@, 2VGA_ON#, R129 0_0402_5% VGA@, Q7 2N7002E-T1-GE3_SOT23-3 VGA@, C289 0.1U_0402_16V4Z VGA@, VGA_ON 39,43,51,52, 43,51,52 VGA_ON#

+3VSDGPU, R74/R111/R487 10K_0402_5% VGA@ (VGA_GPIO0, VGA_GPIO1, VGA_GPIO2), R71 VGA_AC_DET, R95 SOUT_GPIO8, R93 SIN_GPIO9, R113/R112/R110/R96/R109 (VGA_GPIO11, VGA_GPIO12, VGA_GPIO13, ROMSE_GPIO22, GENERICC), 16,37 ENBKL, R103 0_0402_5% DGPU_BKL_EN, DISCRETE ONLY

Park(XT)

Location / VRAM	VRAM_ID3 64Mx16	VRAM_ID2 64Mx16	VRAM_ID1	VRAM_ID0
Samsung	0	1 <4PCS>	0	0
HYNIX	1	1 <4PCS>	0	0
AMD	1	1 <4PCS>	1	0

Madison(Pro)

Location / VRAM	VRAM_ID3 64Mx16	VRAM_ID2 64Mx16	VRAM_ID1	VRAM_ID0
Samsung	0	0 <8PCS>	0	0
HYNIX	1	0 <8PCS>	0	0
AMD	1	0 <8PCS>	1	0

ID3: VRAM Vender ID2: VRAM Size ID1: VRAM Vender

+1.8VSDGPU, X76@ R472/R473/R477/R478 10K_0402_5% (VRAM_ID0, VRAM_ID1, VRAM_ID2, VRAM_ID3), PD-Reset

2009/09/18 For AMD roger
FIX intermittent system boot up hangs issue

JTAG_TRSTB R717 10K_0402_5%, JTAG_TMS R718 10K_0402_5%, +3VSDGPU, TESTEN R720 10K_0402_5% 24, 12 VGA_CLK_27M, R509 0_0402_5% VGA_CLK_27M_R, C802 12P_0402_50V8J @

External 27MHZ 3.3V CLK

XTALOUT, R500 1M_0402_5% VGA@ 27MCLK, Y1 27MHZ_16PF_X5H027000FG1H VGA@, C635 18P_0402_50V8J VGA@, C647 18P_0402_50V8J VGA@

2009/08/27
remove BB_EN

2009/09/18 For AMD roger
Ass Option Circuit for Solve Intermittent System
Boot-up Hangs,R717,R718,VGA_CLK_27M_R

+3VSDGPU, R117/R116 4.7K_0402_5% VGA@, 29 VGA_LCD_CLK, 29 VGA_LCD_DATA, VGA_LCD_CLK AK26, VGA_LCD_DATA AJ26

CH751H-40PT_SOD323-2 D3, 15,37 EC_ACIN, VGA_AC_DET, 16 DGPU_BKL_EN, DGPU_BKL_EN, R104 10K_0402_5% VGA@

51 GPU_VID0, T1 THM_ALERT#, GPU_VID0 AM13, 51 GPU_VID1, GPU_VID1 AL13, 14 PEG_CLKREQ#, ROMSE_GPIO22 AN13, JTAG_TRSTB AM23, T6, VGA_CLK_27M_R AN23, JTAG_TMS AL24, T5, AM24, GENERICC AJ19

Park NC pins

31 VGA_HDMI_DET, VGA_HDMI_DET AK24

+1.8VSDGPU, R100 499_0402_1%, R101 249_0402_1%, C244 0.1U_0402_16V4Z VGA@, +VGA_VREF AH13

+1.8VSDGPU, L15 BLM18AG121SN1D_0603 VGA@, C249 10U_0603_6.3V6M VGA@, C189 0.1U_0402_16V4Z VGA@, C236 1U_0402_6.3V4Z VGA@, +DPLL_PVDD AM32, AN32

+1.0VSDGPU, L11 BLM18AG121SN1D_0603 VGA@, +DPLL_VDDC AN31, C243 10U_0603_6.3V6M VGA@, C196 0.1U_0402_16V4Z VGA@, C197 1U_0402_6.3V4Z VGA@, 27MCLK AV33, XTALOUT AU34

SM010030010
200ma 120ohm@100mhz DCR 0.2

GPU_THERM_D+ AF29, GPU_THERM_D- AG29

+1.8VSDGPU, L7 BLM18AG121SN1D_0603 VGA@, +TSVDD, C220 10U_0603_6.3V6M VGA@, C221 1U_0402_6.3V4Z VGA@, C180 0.1U_0402_16V4Z VGA@, AK32, AJ32, AJ33

U34B

MUTI GFX

NC on Park: VRAM_ID0 AR8, VRAM_ID1 AU8, VRAM_ID2 AP8, VRAM_ID3 AW8, AR3, AR1

DVPCNTL_MVP_0 AU1, DVPCNTL_MVP_1 AU3, DVPCNTL_0 AW3, DVPCNTL_1 AP6, DVPCNTL_2 AW5, DVPCLK AU5, DVPDATA_0 AR6, DVPDATA_1 AW6, DVPDATA_2 AU6, DVPDATA_3 AT7, DVPDATA_4 AV7, DVPDATA_5 AN7, DVPDATA_6 AV9, DVPDATA_7 AT9, DVPDATA_8 AR10, DVPDATA_9 AW10, DVPDATA_10 AU10, DVPDATA_11 AP10, DVPDATA_12 AV11, DVPDATA_13 AT11, DVPDATA_14 AR12, DVPDATA_15 AW12, DVPDATA_16 AU12, DVPDATA_17 AP12, DVPDATA_18, DVPDATA_19, DVPDATA_20, DVPDATA_21, DVPDATA_22, DVPDATA_23

NC on Park

I2C: SCL, SDA

GENERAL PURPOSE I/O: GPIO_0, GPIO_1, GPIO_2, GPIO_3_SMBDATA, GPIO_4_SMBCLK, GPIO_5_AC_BATT, GPIO_6, GPIO_7_BLON, GPIO_8_ROMSO, GPIO_9_ROMSI, GPIO_10_ROMSCK, GPIO_11, GPIO_12, GPIO_13, GPIO_14_HPD2, GPIO_15_PWRCNTL_0, GPIO_16_SSIN, GPIO_17_THERMAL_INT, GPIO_18_HPD3, GPIO_19_CTF, GPIO_20_PWRCNTL_1, GPIO_21_BB_EN, GPIO_22_ROMCSB, GPIO_23_CLKREQB, JTAG_TRSTB, JTAG_TDI, JTAG_TCK, JTAG_TMS, JTAG_TDO, GENERICA, GENERICB, GENERICC, GENERICD, GENERICE_HPD4, GENERICF, GENERICG, HPD1, VREFG

PLL/CLOCK: DPLL_PVDD 120mA, DPLL_PVSS, DPLL_VDDC 150mA, XTALIN, XTALOUT

THERMAL: DPLUS, DMINUS, TS_FDO, TSVDD, TSVSS 20mA

DDC/AUX: DDC1CLK, DDC1DATA, AUX1P, AUX1N, DDC2CLK, DDC2DATA, AUX2P, AUX2N, DDCCLK_AUX3P, DDCDATA_AUX3N, DDCCLK_AUX4P, DDCDATA_AUX4N NC on Park, DDCCLK_AUX5P, DDCDATA_AUX5N, DDC6CLK, DDC6DATA, NC_DDCCLK_AUX7P, NC_DDCDATA_AUX7N NC on Park

DPA: TXCAP_DPA3P AL24, TXCAM_DPA3N AV23, TX0P_DPA2P AT25, TX0M_DPA2N AR24, TX1P_DPA1P AU26, TX1M_DPA1N AV25, TX2P_DPA0P AT27, TX2M_DPA0N AR26, TXCBP_DPB3P AR30, TXCBM_DPB3N AT29

DPB: TX3P_DPB2P AV31, TX3M_DPB2N AU30, TX4P_DPB1P AR32, TX4M_DPB1N AT31, TX5P_DPB0P AT33, TX5M_DPB0N AU32

DPC: TXCCP_DPC3P AU14, TXCCM_DPC3N AV13, TX0P_DPC2P AT15, TX0M_DPC2N AR14, TX1P_DPC1P AU16, TX1M_DPC1N AV15, TX2P_DPC0P AT17, TX2M_DPC0N AR16

DPD: TXCDP_DPD3P AU20, TXCDM_DPD3N AT19, TX3P_DPD2P AT21, TX3M_DPD2N AR20, TX4P_DPD1P AU22, TX4M_DPD1N AV21, TX5P_DPD0P AT23, TX5M_DPD0N AR22

NC on Park

Not share via for other GND

DAC1: R AD39, RB AD37, G AD36, GB AD35, B AD37, BB AD38, HSYNC AD36, VSYNC AD38, RSET AB34, AVDD AD34, AVSSQ AE34, VDD1DI AD33, VSS1DI AE34

VGA_CRT_R 30, VGA_CRT_G 30, VGA_CRT_B 30, VGA_CRT_HSYNC 30, VGA_CRT_VSYNC 30

70mA, 45mA, R53 VGA@ 499_0402_1%, +AVDD, +VDD1DI, 10mil, L3 BLM18AG121SN1D_0603 VGA@ +1.8VSDGPU, C188 1U_0402_6.3V4Z VGA@, C182 1U_0402_6.3V4Z VGA@, C221 10U_0805_6.3V6M VGA@, C198 0.1U_0402_16V4Z VGA@

L8 BLM18AG121SN1D_0603 VGA@ +1.8VSDGPU, C158 1U_0402_6.3V4Z VGA@, C154 1U_0402_6.3V4Z VGA@, C219 10U_0603_6.3V6M VGA@

SM010030010
200ma 120ohm@100mhz DCR 0.2

DAC2: R2 R2B, G2 G2B, B2 B2B, C COMP, H2SYNC AD29, V2SYNC AC29, VDD2DI AG31, VSS2DI AG32, A2VDD AG33, A2VDDQ AD33, A2VSSQ AF33, R2SET AA29

50mA, 130mA, 20mA, +VDD1DI, +A2VDD, +A2VDDQ, 10mil, R56 715_0402_1% VGA@

+3VSDGPU, C699 1U_0402_6.3V4Z @, C172 0.1U_0402_16V4Z @, C600 10U_0603_6.3V6M @

HDMI: DDC1CLK AM26 VGA_HDMI_SCLK, DDC1DATA AN26 VGA_HDMI_SDATA, VGA_HDMI_SCLK 31, VGA_HDMI_SDATA 31

+1.8VSDGPU, C215 1U_0402_6.3V4Z VGA@, C216 0.1U_0402_16V4Z VGA@, C218 10U_0603_6.3V6M VGA@

CRT: VGA_DDC_CLK AN21, VGA_DDC_DATA AM21, VGA_DDC_CLK 30, VGA_DDC_DATA 30

Strap: V2SYNC R107 10K_0402_5%, H2SYNC R114 10K_0402_5%, VGA_CRT_VSYNC R447 10K_0402_5%, VGA_CRT_HSYNC R460 10K_0402_5%, VGA_HDMI_SCLK R506 10K_0402_5%, VGA_HDMI_SDATA R511 10K_0402_5%, VGA_DDC_CLK R118 10K_0402_5%, VGA_DDC_DATA R119 10K_0402_5%, VGA_CRT_R R462 150_0402_1%, VGA_CRT_G R463 150_0402_1%, VGA_CRT_B R465 150_0402_1%

FLASH ROM

U8 @ M25P10-AVMN6P (SIN_GPIO9, CLK_GPIO10, ROMSE_GPIO22, SOUT_GPIO8, HOLD, W, TYPE 1), +3VSDGPU, R94 0_0402_5%, R86 0_0402_5%, C227 0.1U_0402_16V4Z

216-0729002 A12 M96_BGA962
MADI@

Security Classification	Compal Secret Data		
Issued Date	2009/08/01	Deciphered Date	2010/08/01

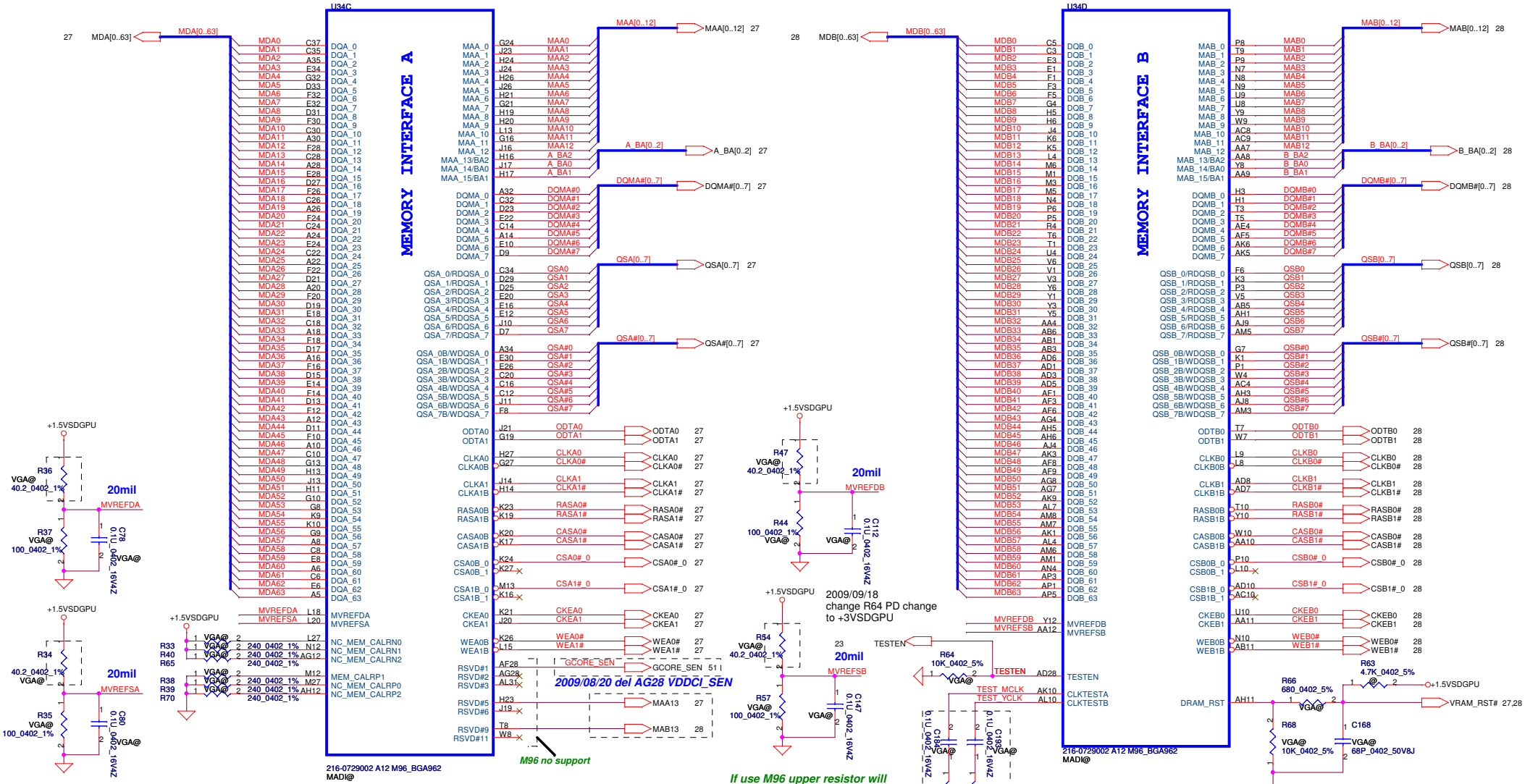
Compal Electronics, Inc.

Title: M96_Strape/DP/HDMI//CRT

Size: C | Document Number: NEW70 M/B LA-5891P Schematic | Rev: 1.0

Date: Thursday, January 07, 2010 | Sheet 23 of 59

Park is single channel for memory (channel B only)



	M96	Broadway
R228	4.7k Ohm SD028470180	10k Ohm SD028100280
R159	0 Ohm SD028000080	680 Ohm SD028680080
R159	4.7k Ohm SD028470180	DNI
C659	1000 pF SE074102K80	68 pF SE071680J80

Compal Electronics, Inc.

Title: Memory

Size: Custom | Document Number: NEW70 M/B LA-5891P Schematic | Rev: 1.0

Date: Tuesday, December 29, 2009 | Sheet 24 of 59

2009/09/14
update P/N SM010005500 500ma 600ohm@100MHZ DCR 0.38

2009/09/14
update P/N SM010005500 500ma 600ohm@100MHZ DCR 0.38

U34F

POWER

MEM I/O
LEVEL TRANSLATION
I/O
MEM CLK
PLL
BACK BIAS
PCIE
CORE
ISOLATED CORE I/O

2900mA
TBD

400mA
40mil
2A
34.6A
20mil
136mA
60mA
10mil
20mil
170mA
170mA
10mil
68mA
20mil
150mA
10mil
50mA
20mil
136mA
32mA
10mil
160mil
4A

SM010030010
200ma 120ohm@100mhz DCR 0.2

SM010030010
200ma 120ohm@100mhz DCR 0.2

SM010030010
200ma 120ohm@100mhz DCR 0.2

SM010014520 3000ma 220ohm@100mhz DCR 0.04

2009/08/27
RemoveBack Biasing

2009/09/17
ADD BIF_VDDCI N27,T27

2009/08/27
remove VDDRHA,VDDRHB

For M96 only,
Manhattan are NC pin

MPV18 For
Mahattan only

SPV18 For
Mahattan only

For M96 SPV10=+GPU_CORE
For M97,Nahattan SPV10=+1.0VS

2009/08/27
remove +VGA_CORE power

M97 and Mahattan VDDC and
VDDCI ball assignments are
different from M96, If M96 is
populated on this
design,VDDC and VDDCI
shoudl be shorted.

2009/08/27
short BBP

Back Bias is not supported on
M97,Broadway,Madison and Park
Connect to VDDCI directly

216-0729002 A12 M96_BGA962
MADI@

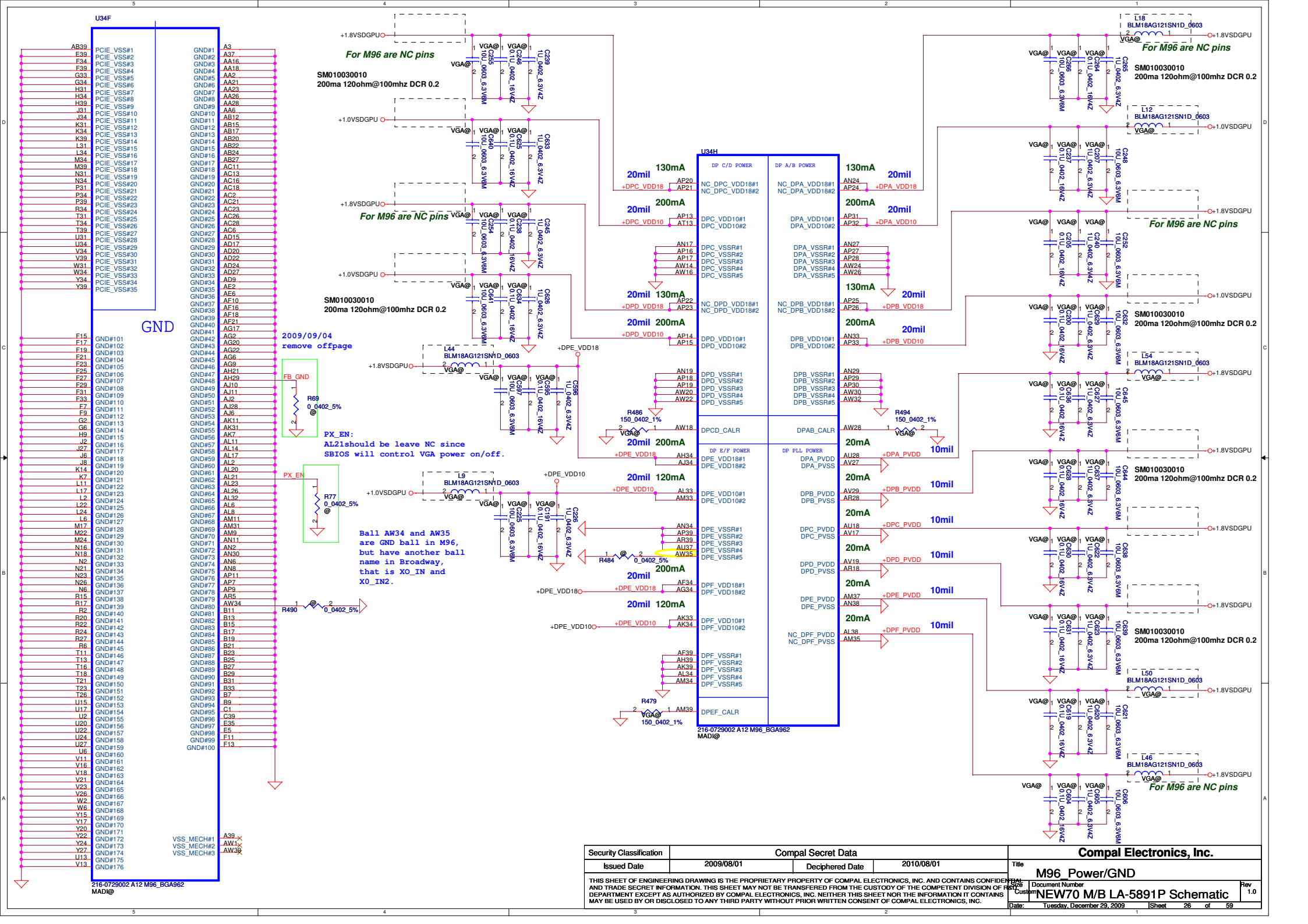
Security Classification	Compal Secret Data		
Issued Date	2009/08/01	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: M96_Power/GND

Size: Custom | Document Number: NEW70 M/B LA-5891P Schematic | Rev: 1.0

Date: Tuesday, December 29, 2009 | Sheet 25 of 59



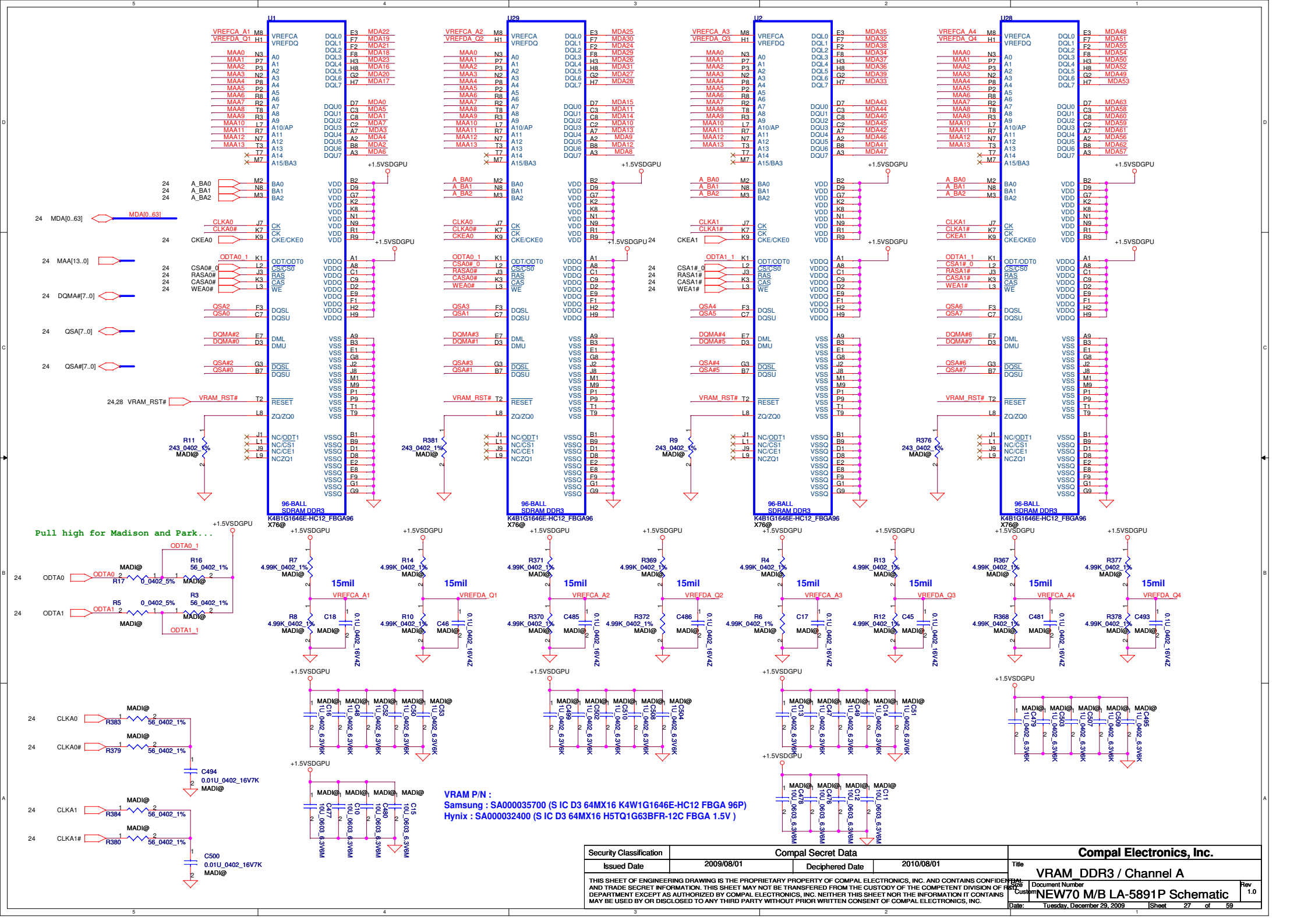
Security Classification	Compal Secret Data		
Issued Date	2009/08/01	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: M96_Power/GND

Size: Custom | Document Number: NEW70 M/B LA-5891P Schematic | Rev: 1.0

Date: Tuesday, December 29, 2009 | Sheet 26 of 59



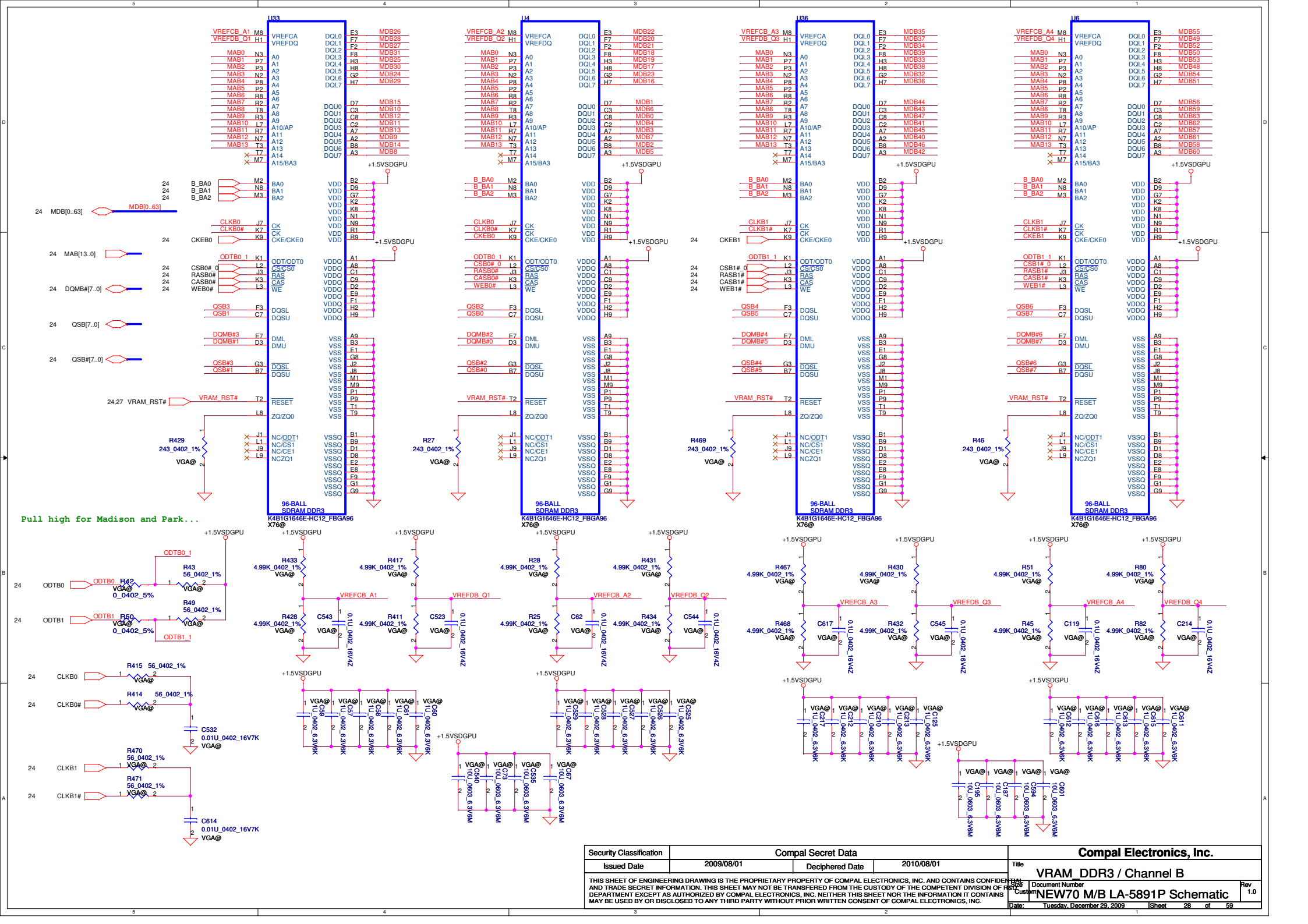
Security Classification	Compal Secret Data		
Issued Date	2009/08/01	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: VRAM_DDR3 / Channel A

Size: Custom | Document Number: NEW70 M/B LA-5891P Schematic | Rev: 1.0

Date: Tuesday, December 29, 2009 | Sheet 27 of 59


U33
U4
U36
U6
96-BALL SDRAM DDR3
K4B1G1646E-HC12_FBGA96
X76@
Pull high for Madison and Park...
+1.5VSDGPU
MDB[0..63]
MAB[13..0]
DQMB#[7..0]
QSB[7..0]
QSB#[7..0]
VRAM_RST#
B_BA0
B_BA1
B_BA2
CKEB0
CKEB1
CLKB0
CLKB0#
CLKB1
CLKB1#
CSB0#
RASB0#
CASB0#
WEB0#
CSB1#
RASB1#
CASB1#
WEB1#
ODTB0
ODTB1
VREFCB_A1
VREFDB_Q1
VREFCB_A2
VREFDB_Q2
VREFCB_A3
VREFDB_Q3
VREFCB_A4
VREFDB_Q4
Security Classification
Compal Secret Data
Issued Date
2009/08/01
Deciphered Date
2010/08/01
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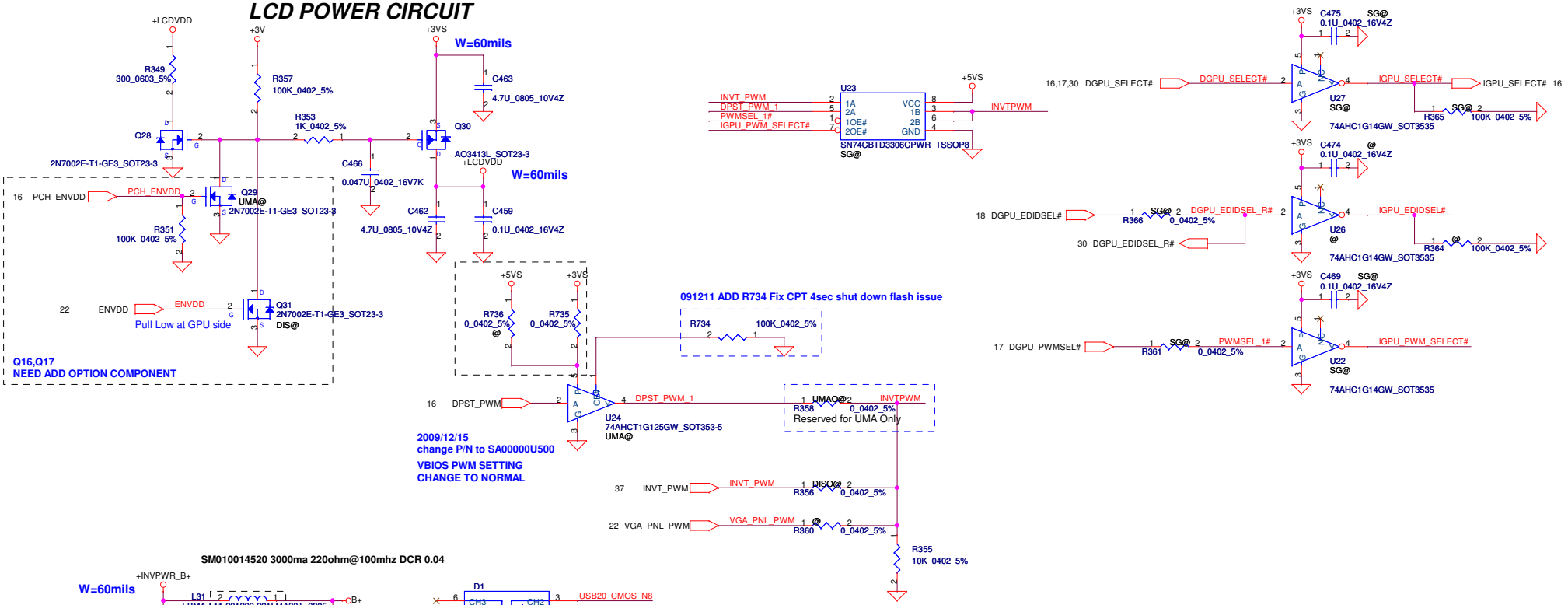
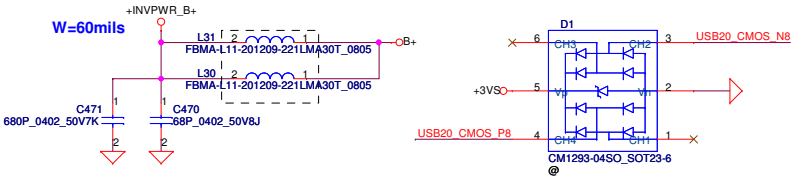
Compal Electronics, Inc.
Title
VRAM_DDR3 / Channel B
Size
Custom
Document Number
NEW70 M/B LA-5891P Schematic
Rev
1.0
Date:
Tuesday, December 29, 2009
Sheet
28
of
59

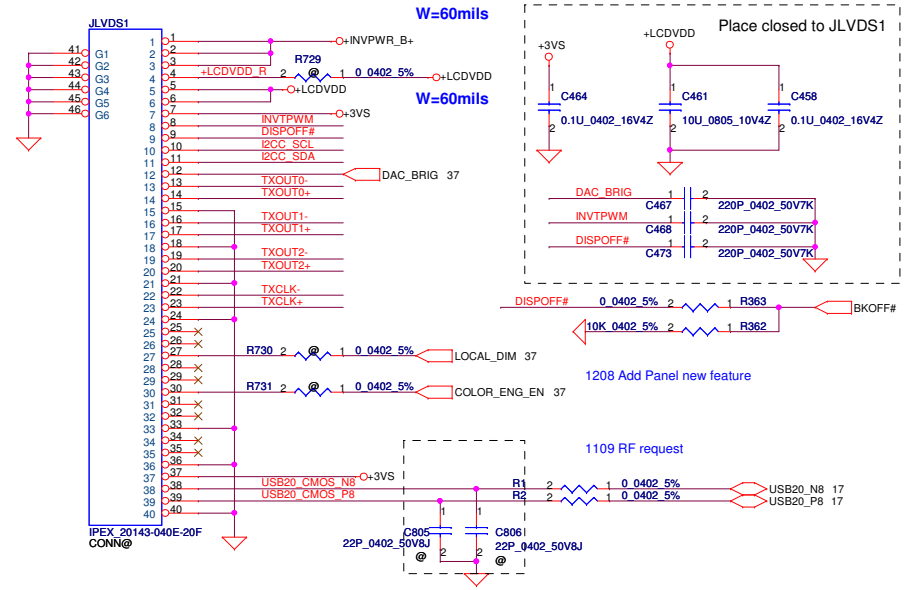
LCD POWER CIRCUIT

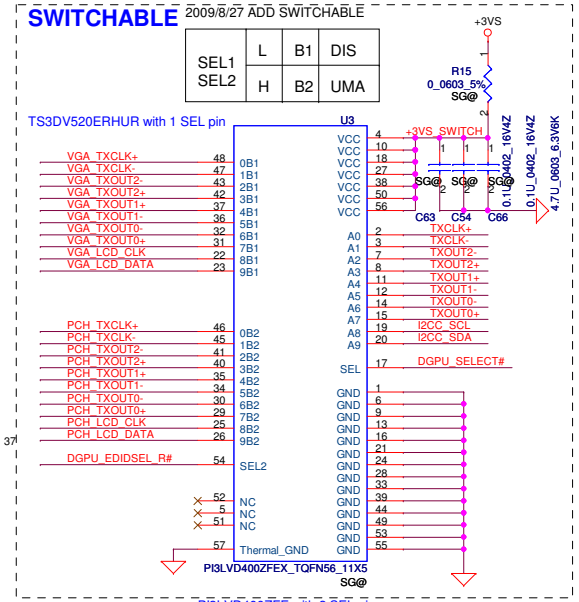


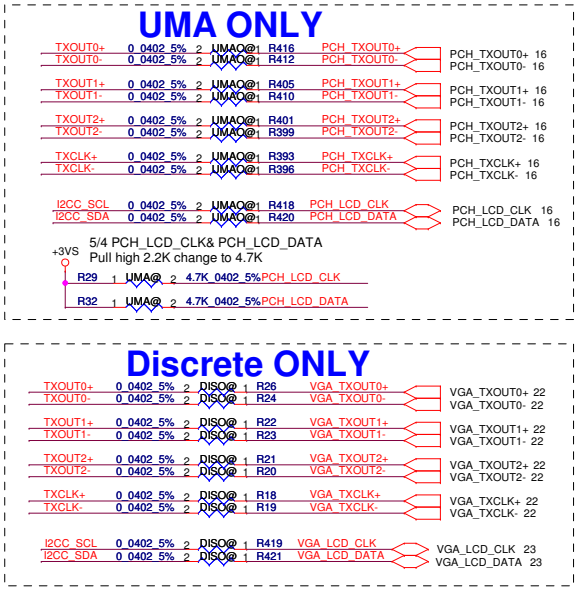
SM010014520 3000ma 220ohm@100mhz DCR 0.04



LCD/LED PANEL Conn.







Security Classification	Compal Secret Data		
Issued Date	2009/08/01	Deciphered Date	2010/08/01

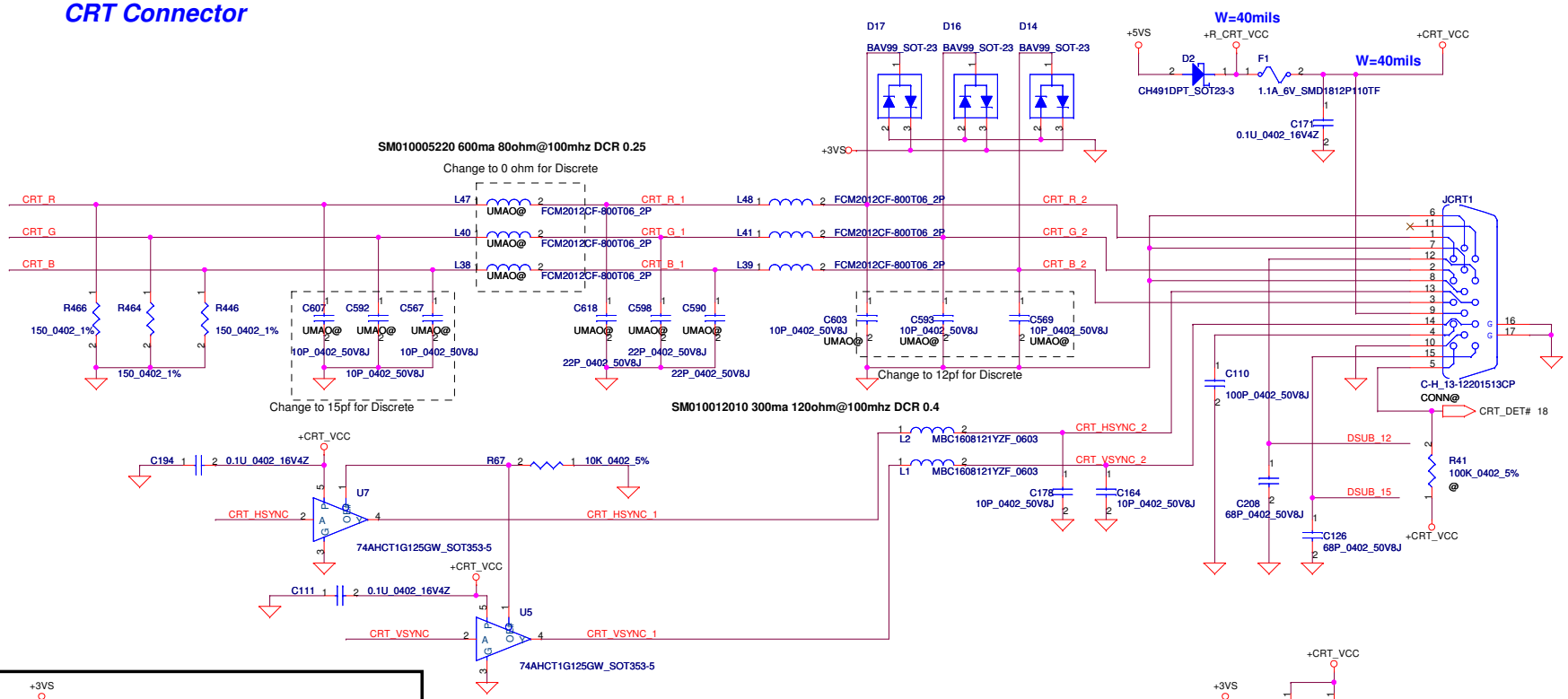
Compal Electronics, Inc.

Title: LVDS Connector

Size: Custom | Document Number: NEW70 M/B LA-5891P Schematic | Rev: 1.0

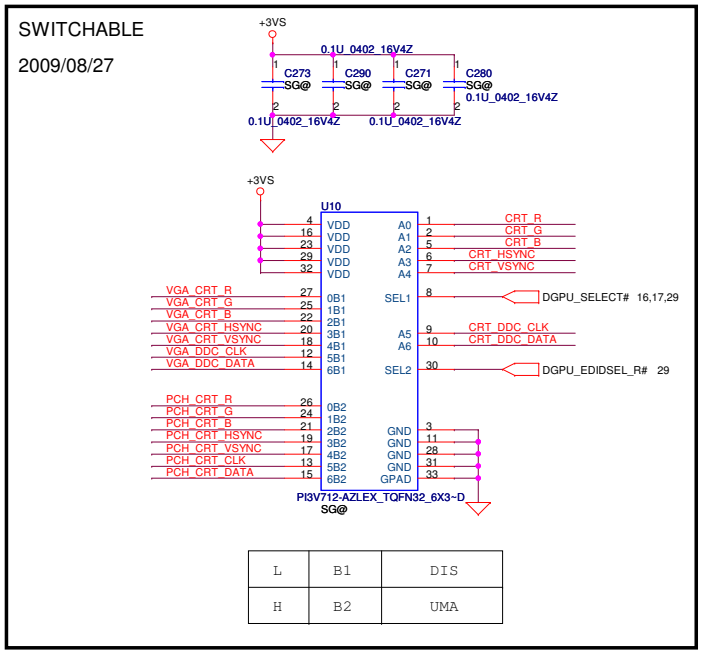
Date: Wednesday, January 06, 2010 | Sheet 29 of 59

CRT Connector



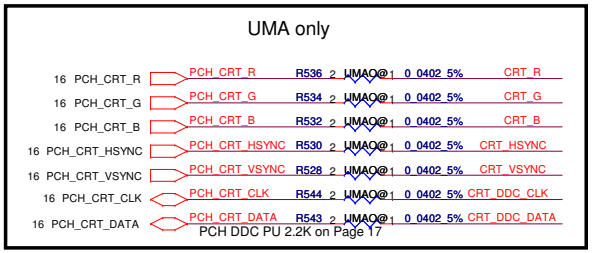
SWITCHABLE

2009/08/27

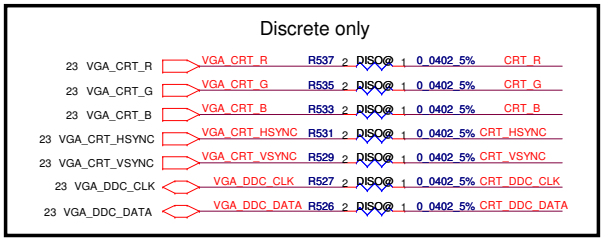


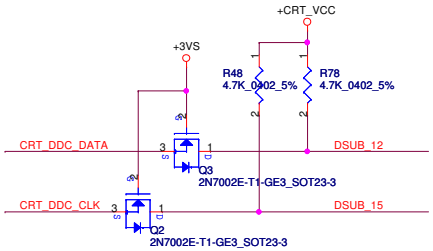
L	B1	DIS
H	B2	UMA

UMA only



Discrete only





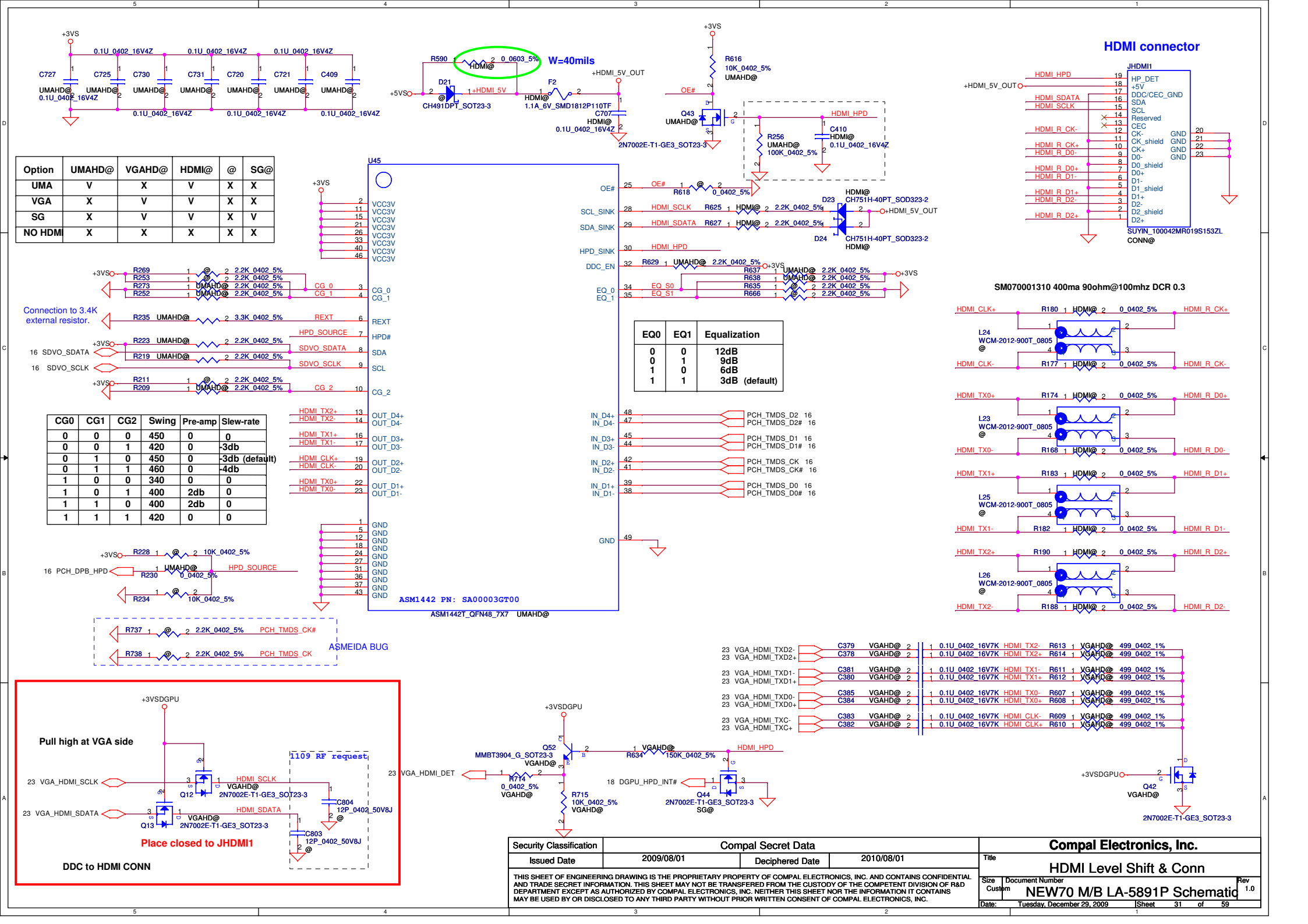
Security Classification	Compal Secret Data		
Issued Date	2009/08/01	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: CRT Connector

Size: B | Document Number: NEW70 M/B LA-5891P Schematic | Rev: 1.0

Date: Tuesday, December 29, 2009 | Sheet 30 of 59



Option	UMAHD@	VGAHD@	HDMI@	@	SG@
UMA	V	X	V	X	X
VGA	X	V	V	X	X
SG	X	V	V	X	V
NO HDMI	X	X	X	X	X

EQ0	EQ1	Equalization
0	0	12dB
0	1	9dB
1	0	6dB
1	1	3dB (default)

CG0	CG1	CG2	Swing	Pre-amp	Slew-rate
0	0	0	450	0	0
0	0	1	420	0	-3db
0	1	0	450	0	-3db (default)
0	1	1	460	0	-4db
1	0	0	340	0	0
1	0	1	400	2db	0
1	1	0	400	2db	0
1	1	1	420	0	0

Security Classification	Compal Secret Data		
Issued Date	2009/08/01	Deciphered Date	2010/08/01

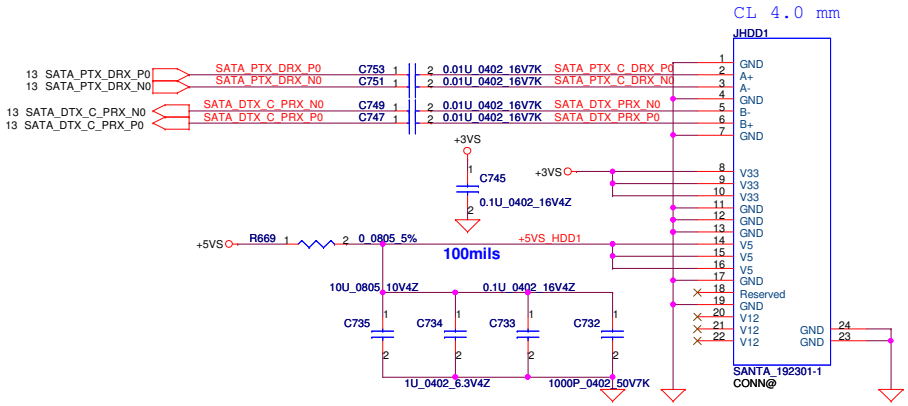
Compal Electronics, Inc.

Title: HDMI Level Shift & Conn

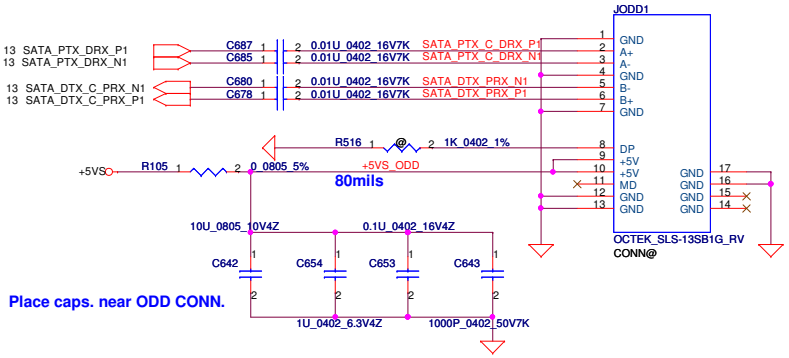
Size: Custom | Document Number: NEW70 M/B LA-5891P Schematic | Rev: 1.0

Date: Tuesday, December 29, 2009 | Sheet 31 of 59

SATA HDD1 Conn.



SATA ODD Conn.



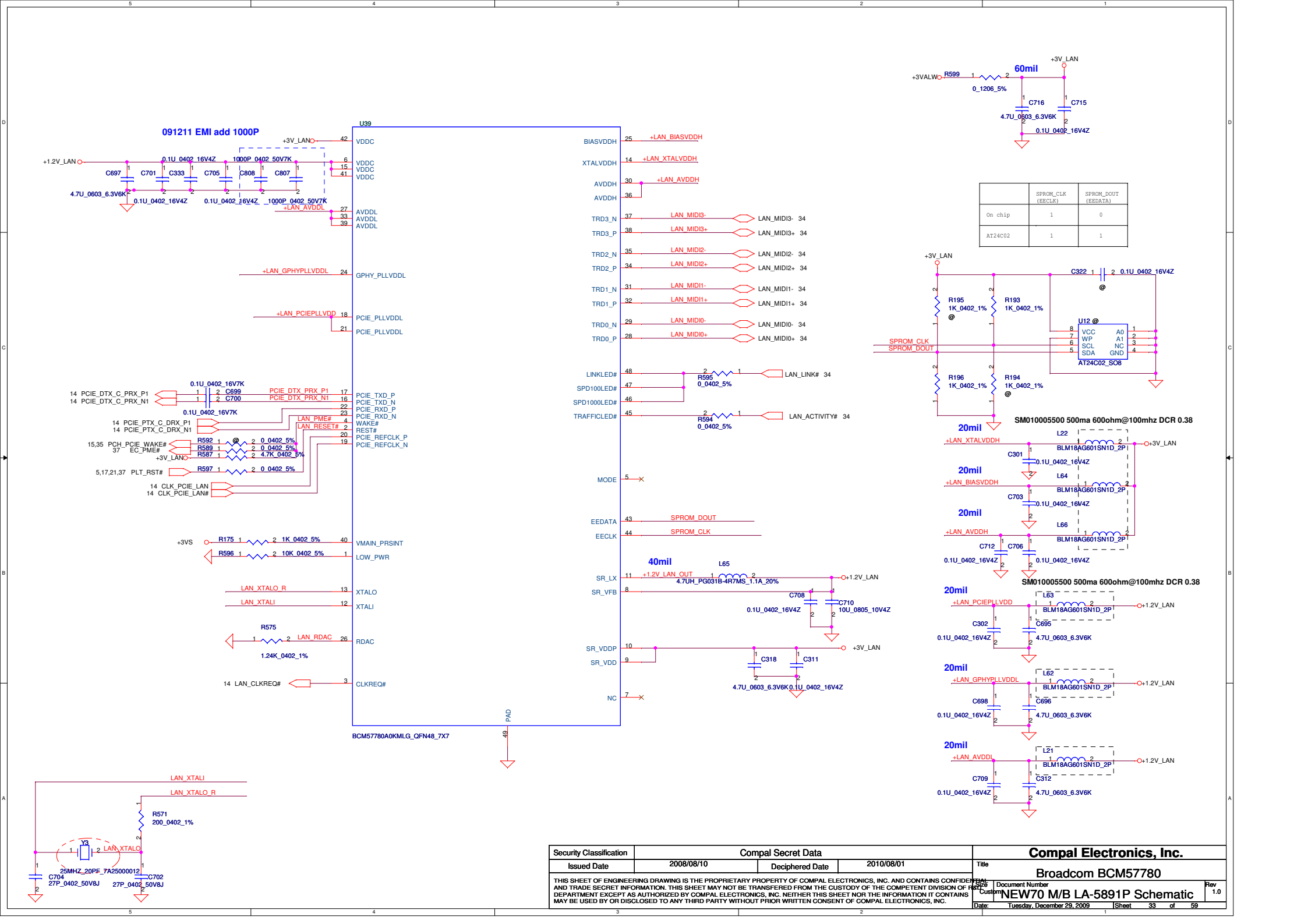
Security Classification	Compal Secret Data		
Issued Date	2008/08/10	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: HDD & ODD Connector

Size: Custom | Document Number: NEW70 M/B LA-5891P Schematic | Rev: 1.0

Date: Tuesday, December 29, 2009 | Sheet 32 of 59


091211 EMI add 1000P
U39
BCM57780A0KMLG_QFN48_7X7
+3V_LAN
+1.2V_LAN
+3VALW
R599
0_1206_5%
60mil
C716
C715
4.7U_0603_6.3V6K
0.1U_0402_16V4Z
0.1U_0402_16V4Z
1000P_0402_50V7K
C697
C701
C333
C705
C808
C807
4.7U_0603_6.3V6K
0.1U_0402_16V4Z
0.1U_0402_16V4Z
1000P_0402_50V7K
+LAN_AVDDL
VDDC
VDDC
VDDC
VDDC
AVDDL
AVDDL
AVDDL
+LAN_GPHYPLLVDDL
GPHY_PLLVDDL
+LAN_PCIEPLLVDD
PCIE_PLLVDDL
PCIE_PLLVDDL
0.1U_0402_16V7K
14 PCIE_DTX_C_PRX_P1
14 PCIE_DTX_C_PRX_N1
C699
C700
PCIE_DTX_PRX_P1
PCIE_DTX_PRX_N1
0.1U_0402_16V7K
14 PCIE_PTX_C_DRX_P1
14 PCIE_PTX_C_DRX_N1
PCIE_TXD_P
PCIE_TXD_N
PCIE_RXD_P
PCIE_RXD_N
WAKE#
REST#
PCIE_REFCLK_P
PCIE_REFCLK_N
LAN_PME#
LAN_RESET#
15,35 PCH_PCIE_WAKE#
37 EC_PME#
+3V_LAN
R592
R589
R587
0_0402_5%
0_0402_5%
4.7K_0402_5%
5,17,21,37 PLT_RST#
R597
0_0402_5%
14 CLK_PCIE_LAN
14 CLK_PCIE_LAN#
+3VS
R175
1K_0402_5%
R596
10K_0402_5%
VMAIN_PRSINT
LOW_PWR
LAN_XTALO_R
LAN_XTALI
XTALO
XTALI
R575
LAN_RDAC
1.24K_0402_1%
RDAC
14 LAN_CLKREQ#
CLKREQ#
PAD
BIASVDDH
XTALVDDH
AVDDH
AVDDH
+LAN_BIASVDDH
+LAN_XTALVDDH
+LAN_AVDDH
TRD3_N
TRD3_P
TRD2_N
TRD2_P
TRD1_N
TRD1_P
TRD0_N
TRD0_P
LAN_MIDI3-
LAN_MIDI3+
LAN_MIDI2-
LAN_MIDI2+
LAN_MIDI1-
LAN_MIDI1+
LAN_MIDI0-
LAN_MIDI0+
LAN_MIDI3- 34
LAN_MIDI3+ 34
LAN_MIDI2- 34
LAN_MIDI2+ 34
LAN_MIDI1- 34
LAN_MIDI1+ 34
LAN_MIDI0- 34
LAN_MIDI0+ 34
LINKLED#
SPD100LED#
SPD1000LED#
TRAFFICLED#
R595
0_0402_5%
R594
0_0402_5%
LAN_LINK# 34
LAN_ACTIVITY# 34
MODE
EEDATA
EECLK
SPROM_DOUT
SPROM_CLK
SR_LX
SR_VFB
SR_VDDP
SR_VDD
NC
40mil
L65
+1.2V_LAN_OUT
4.7UH_PG031B-4R7MS_1.1A_20%
+1.2V_LAN
C708
C710
0.1U_0402_16V4Z
10U_0805_10V4Z
+3V_LAN
C318
C311
4.7U_0603_6.3V6K
0.1U_0402_16V4Z
SPROM_CLK (EECLK)
SPROM_DOUT (EEDATA)
On chip 1 0
AT24C02 1 1
+3V_LAN
C322
0.1U_0402_16V4Z
R195
1K_0402_1%
R193
1K_0402_1%
U12
VCC
WP
SCL
SDA
A0
A1
NC
GND
AT24C02_SO8
SPROM_CLK
SPROM_DOUT
R196
1K_0402_1%
R194
1K_0402_1%
SM010005500 500ma 600ohm@100mhz DCR 0.38
20mil
+LAN_XTALVDDH
L22
BLM18AG601SN1D_2P
+3V_LAN
C301
0.1U_0402_16V4Z
20mil
+LAN_BIASVDDH
L64
BLM18AG601SN1D_2P
C703
0.1U_0402_16V4Z
20mil
+LAN_AVDDH
L66
BLM18AG601SN1D_2P
C712
C706
0.1U_0402_16V4Z
0.1U_0402_16V4Z
SM010005500 500ma 600ohm@100mhz DCR 0.38
20mil
+LAN_PCIEPLLVDD
L63
BLM18AG601SN1D_2P
+1.2V_LAN
C302
C695
0.1U_0402_16V4Z
4.7U_0603_6.3V6K
20mil
+LAN_GPHYPLLVDDL
L62
BLM18AG601SN1D_2P
+1.2V_LAN
C698
C696
0.1U_0402_16V4Z
4.7U_0603_6.3V6K
20mil
+LAN_AVDDL
L21
BLM18AG601SN1D_2P
+1.2V_LAN
C709
C312
0.1U_0402_16V4Z
4.7U_0603_6.3V6K
LAN_XTALI
LAN_XTALO_R
R571
200_0402_1%
Y3
LAN_XTALO
25MHZ_20PF_7A25000012
C704
27P_0402_50V8J
C702
27P_0402_50V8J
Security Classification
Compal Secret Data
Issued Date
2008/08/10
Deciphered Date
2010/08/01
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Compal Electronics, Inc.
Title
Broadcom BCM57780
Size
Custom
Document Number
NEW70 M/B LA-5891P Schematic
Rev
1.0
Date:
Tuesday, December 29, 2009
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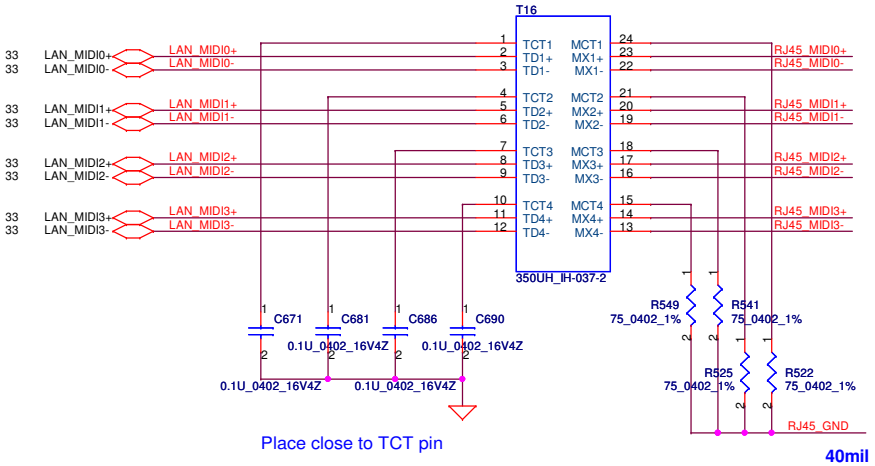
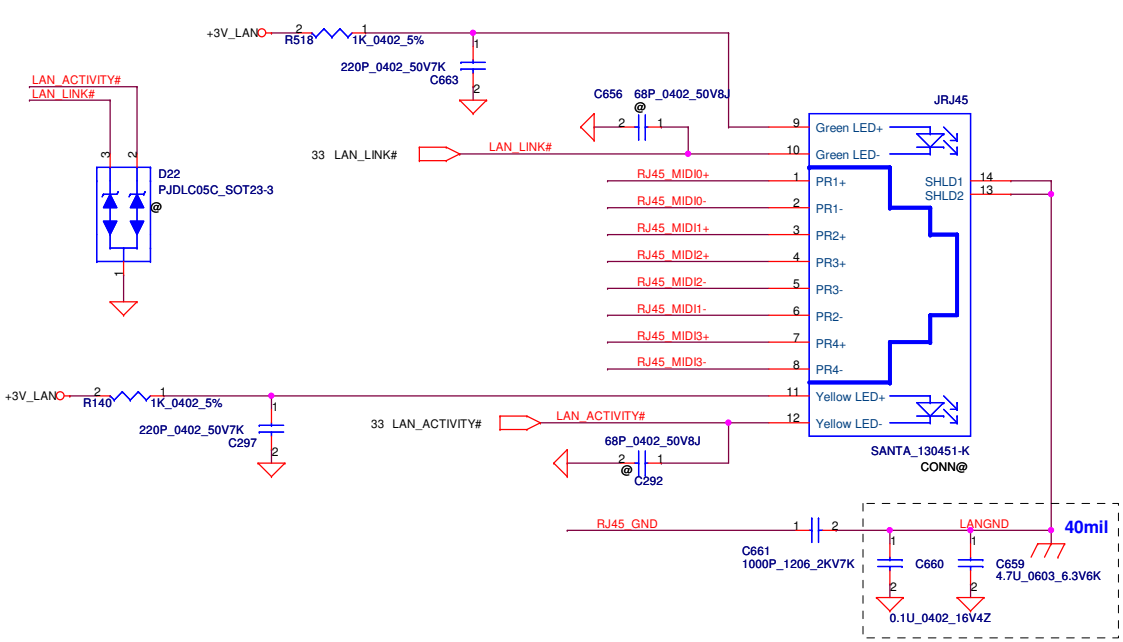
of
59

LAN Connector





BOTHHAND: S X'FORM_ GST5009-D LF LAN, SP050006B00
TIMAG:S X'FORM_ IH-160 LAN , SP050006F00

Security Classification	Compal Secret Data		
Issued Date	2008/08/10	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: LAN Magnetic & RJ45

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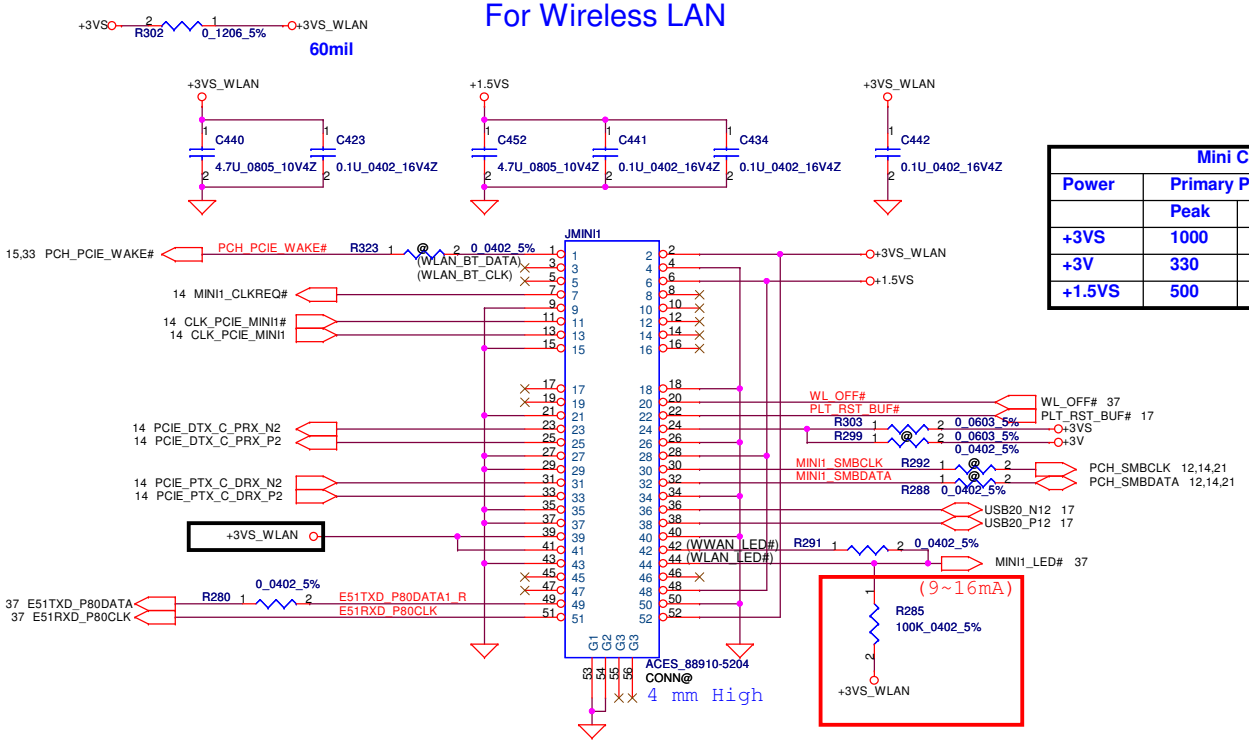
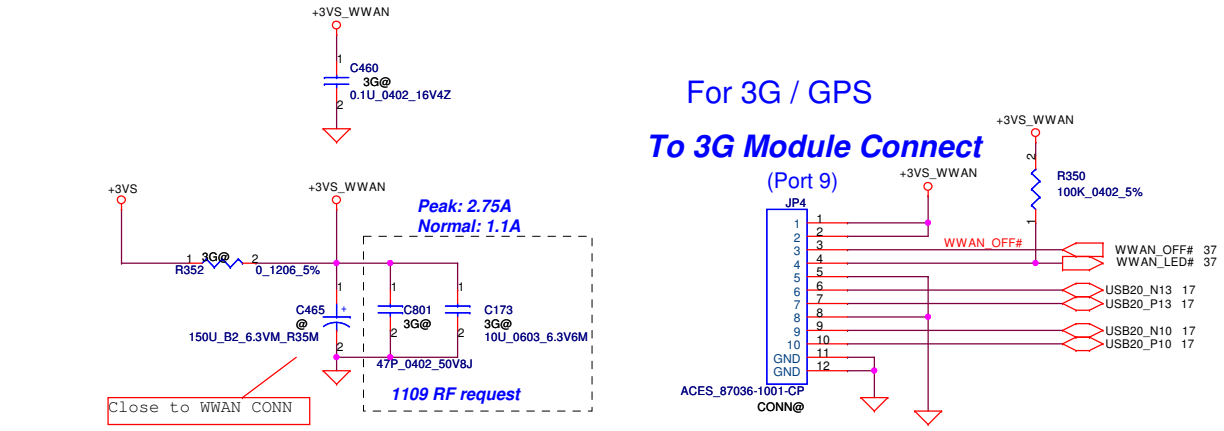


Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)



Security Classification	Compal Secret Data		
Issued Date	2008/08/10	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: MINI CARD (WLAN & TV-Tuner)

Size: Custom | Document Number: NEW70 M/B LA-5891P Schematic | Rev: 1.0

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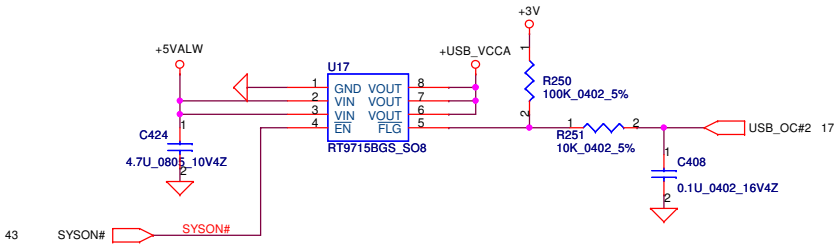
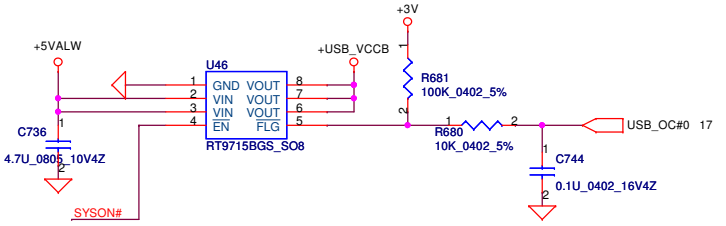
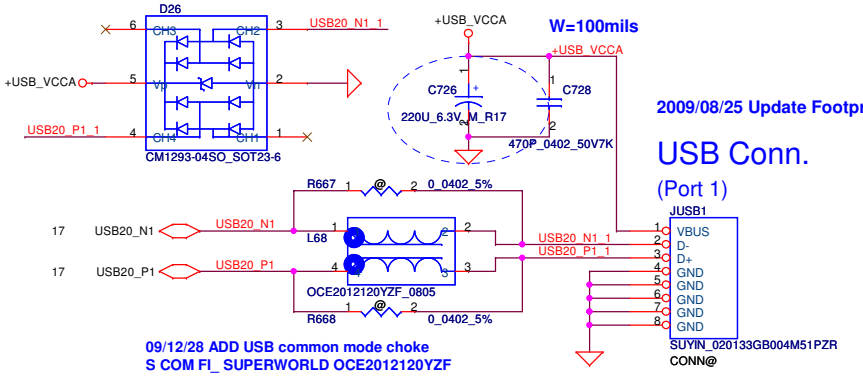




2009/08/14 CHANGE cap



09/12/28 ADD USB common mode choke
S COM FI_ SUPERWORLD OCE2012120YZF

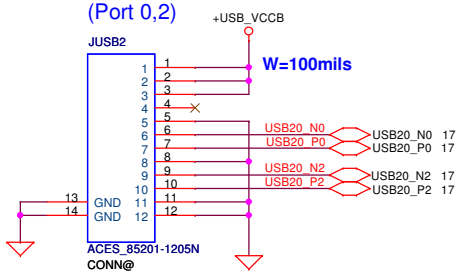
2009/08/25 Update Footprint(follow NAL00)

USB Conn.

(Port 1)

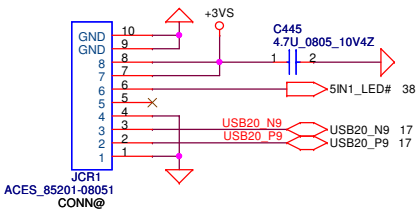
USB/B Conn.

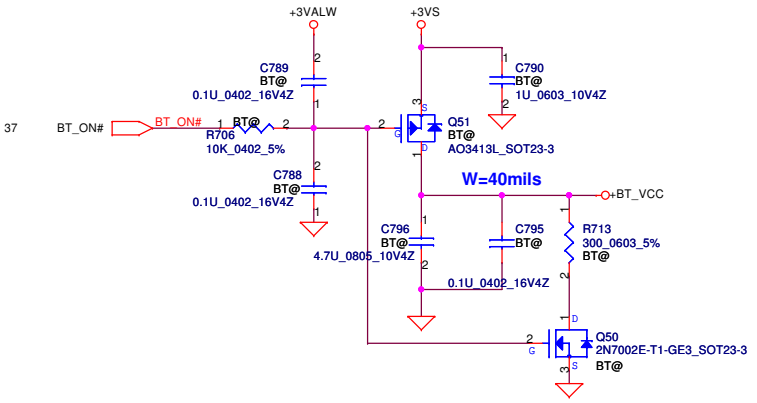
(Port 0,2)



2009/08/24 CHANGE Conn to FFC Type

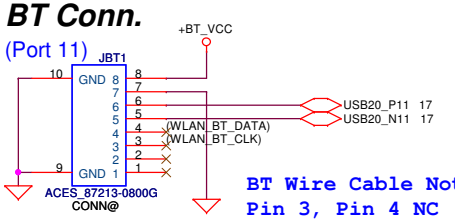
Card Reader Conn.





BT Conn.

(Port 11)



BT Wire Cable Note:
Pin 3, Pin 4 NC

Security Classification	Compal Secret Data		
Issued Date	2008/08/10	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: USB / BT / USBB

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SM010015410 300ma 80ohm@100mhz DCR 0.3

For EC Tools

Place on RAM door

Place on MiniCard

Board ID definition, Please see page 3.

Project ID definition, Please see page 3.

1109 RF request

PCH_TEMP_ALERT# Pull high at Page 18 (PCH side)

EC_PROJECTID	HIGH	LOW

SM010015410 300ma 80ohm@100mhz DCR 0.3

Security Classification	Compal Secret Data		
Issued Date	2008/08/10	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: EC ENE KB926

Size: B | Document Number: NEW70 M/B LA-5891P Schematic | Rev: 1.0

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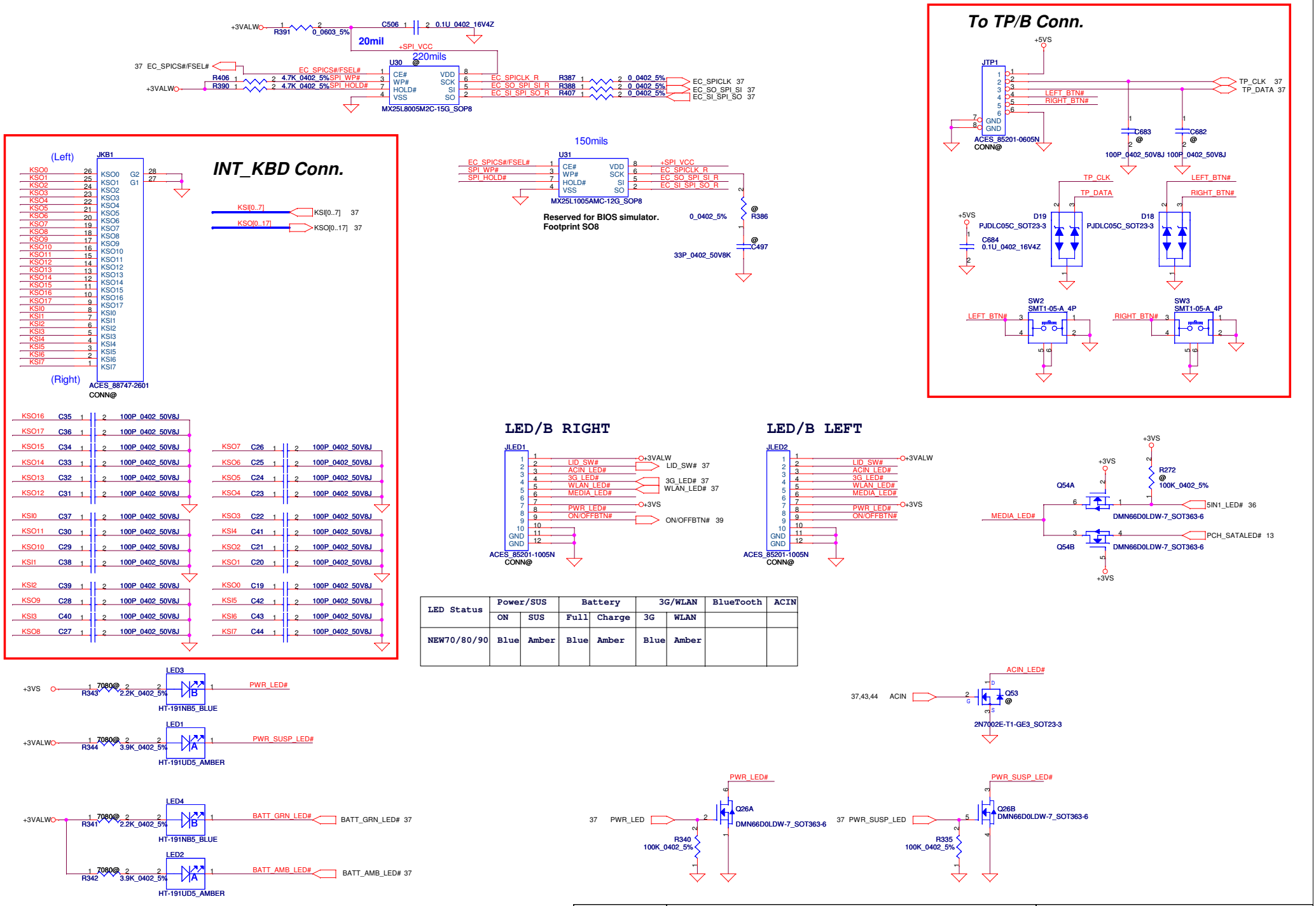

LED Status	Power/SUS		Battery		3G/WLAN		BlueTooth	ACIN
	ON	SUS	Full	Charge	3G	WLAN		
NEW70/80/90	Blue	Amber	Blue	Amber	Blue	Amber		

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2008/08/10	Deciphered Date	2010/08/01

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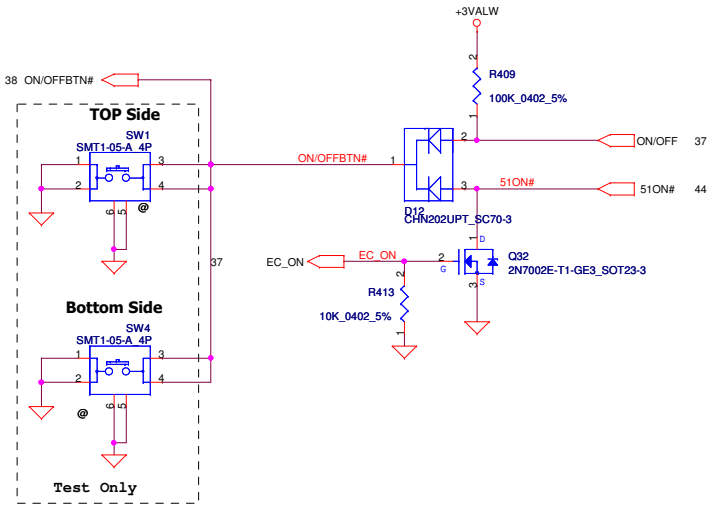
Title: BIOS, I/O Port & K/B Connector

Size: B | Document Number: NEW70 M/B LA-5891P Schematic | Rev: 1.0

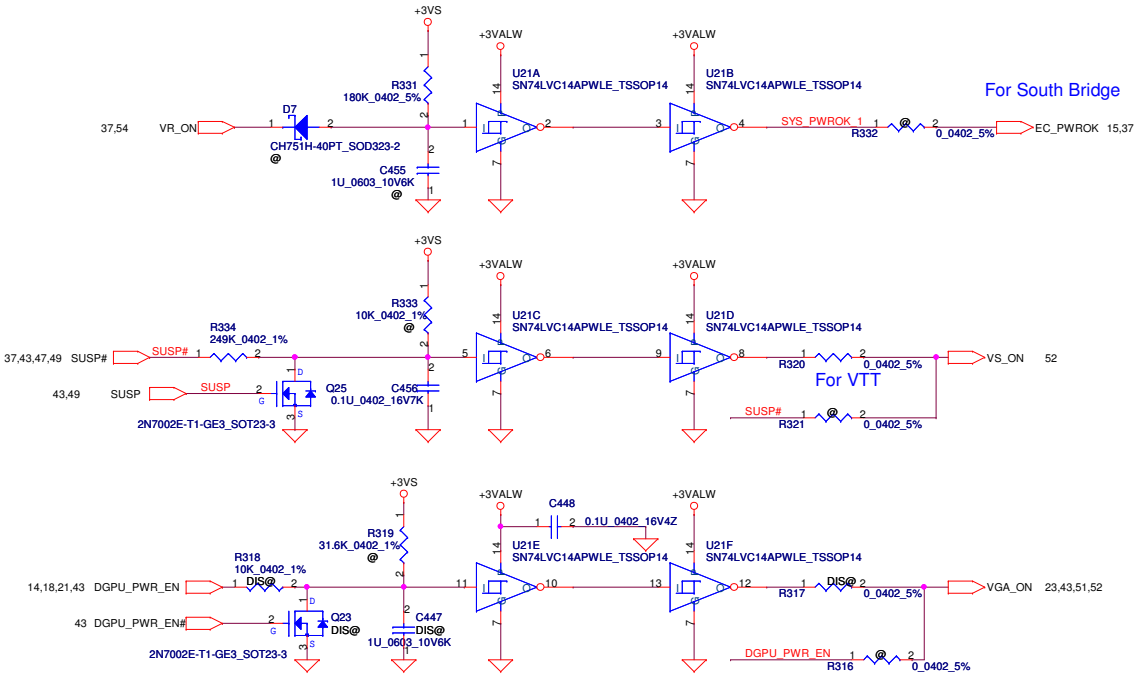
Date: Thursday, January 07, 2010 | Sheet 38 of 59

Power Button

ON/OFF switch



Power ON Circuit



Security Classification	Compal Secret Data		
Issued Date	2008/08/10	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: Power OK

Size: B | Document Number: NEW70 M/B LA-5891P Schematic | Rev: 1.0

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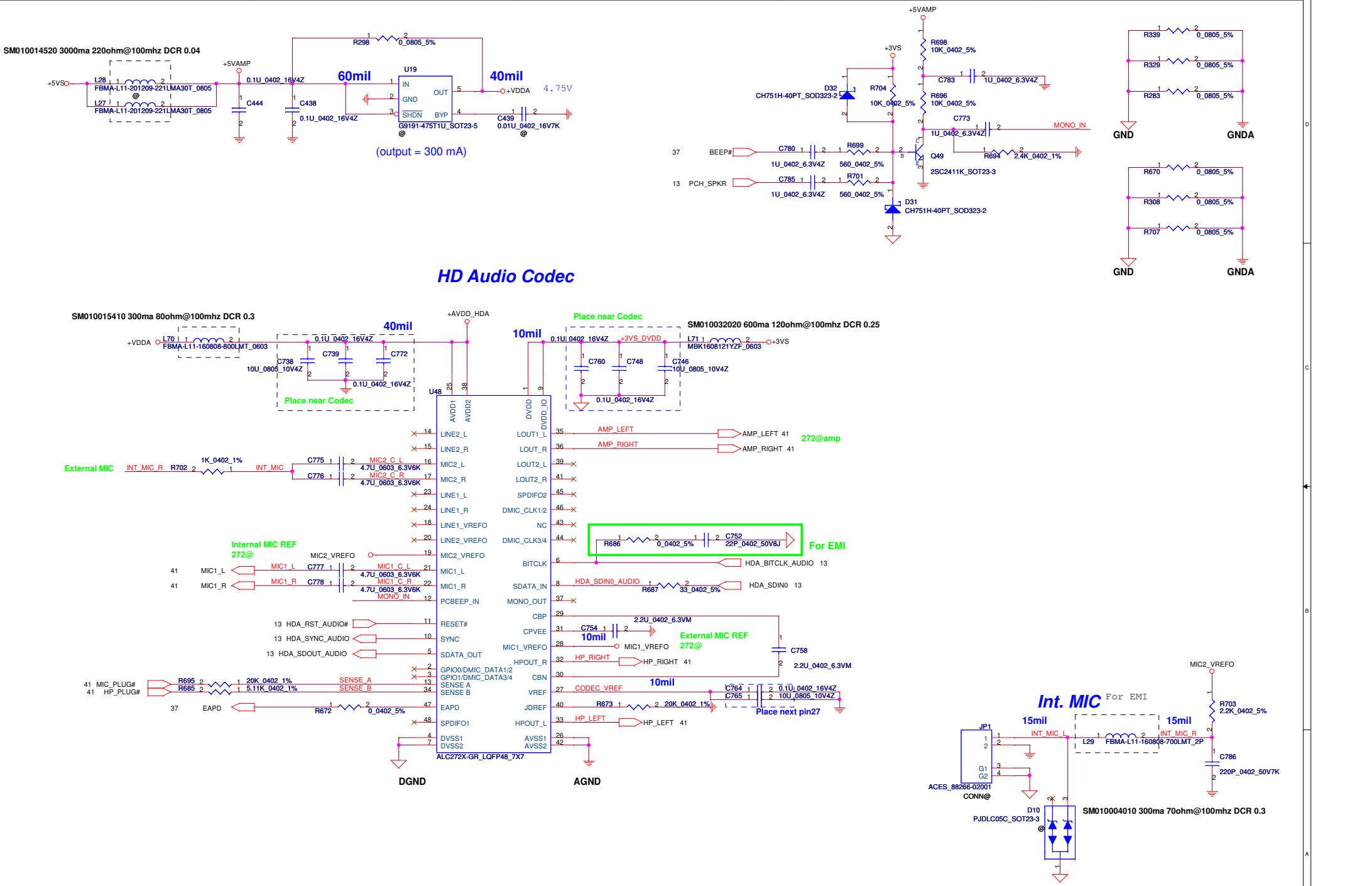

Security Classification	Compal Secret Data		
Issued Date	2008/08/10	Deciphered Date	2010/08/01

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Compal Electronics, Inc.

Title: HD Audio Codec ALC272X

Size: Custom | Document Number: NEW70 M/B LA-5891P Schematic | Rev: 1.0

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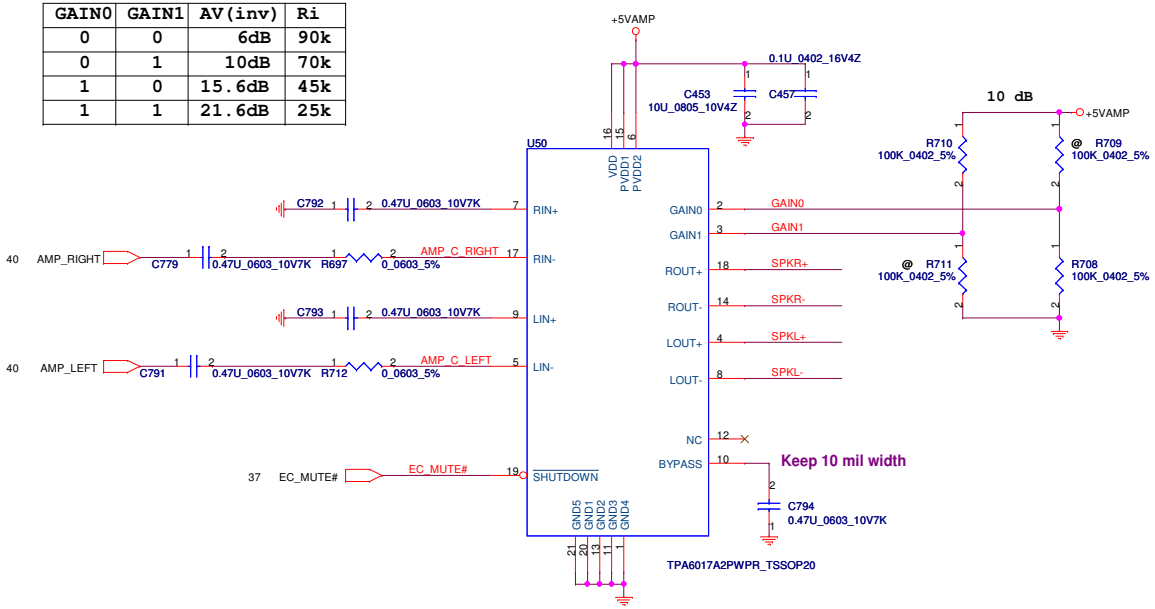
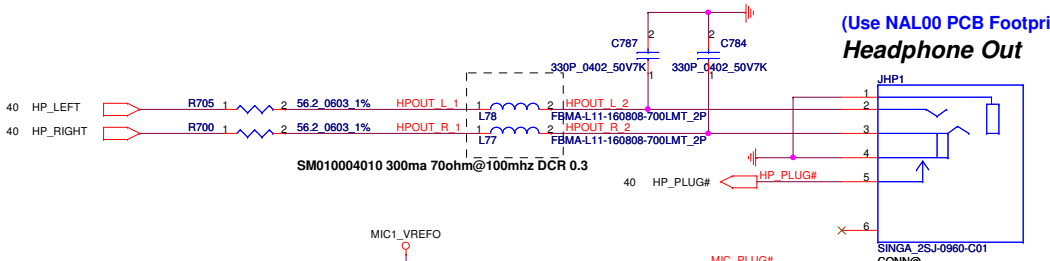
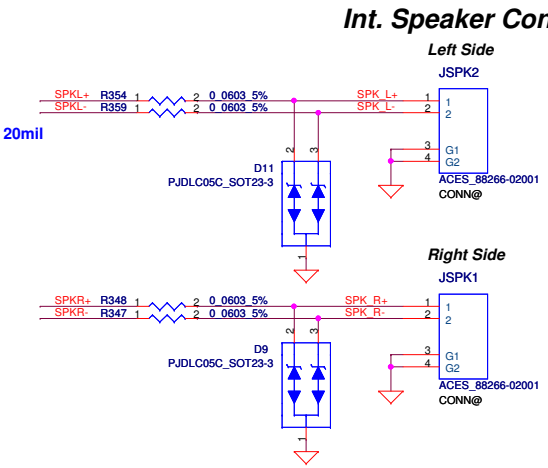
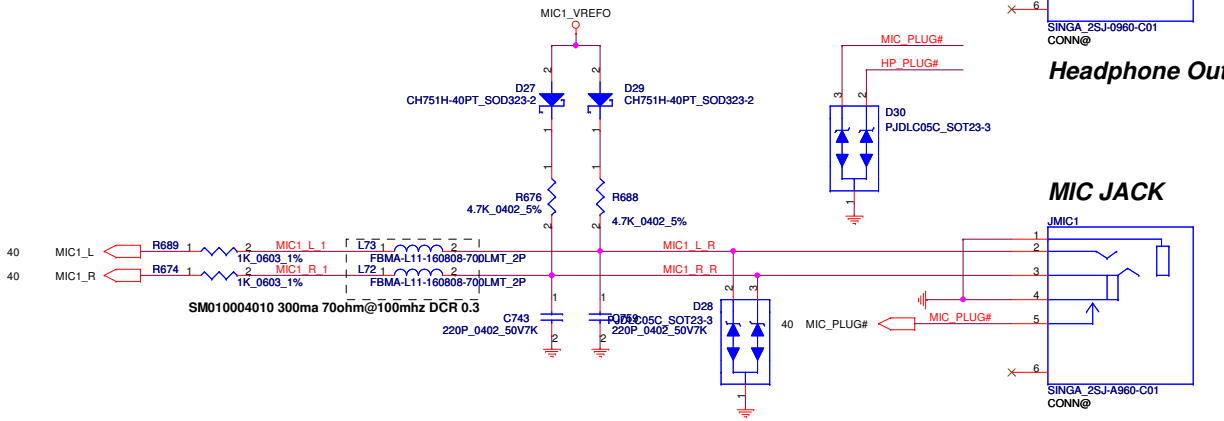
GAIN0	GAIN1	AV(inv)	Ri
0	0	6dB	90k
0	1	10dB	70k
1	0	15.6dB	45k
1	1	21.6dB	25k









Security Classification	Compal Secret Data		
Issued Date	2008/08/10	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: Amplifier & Audio Jack

Size: Custom | Document Number: NEW70 M/B LA-5891P Schematic | Rev: 1.0

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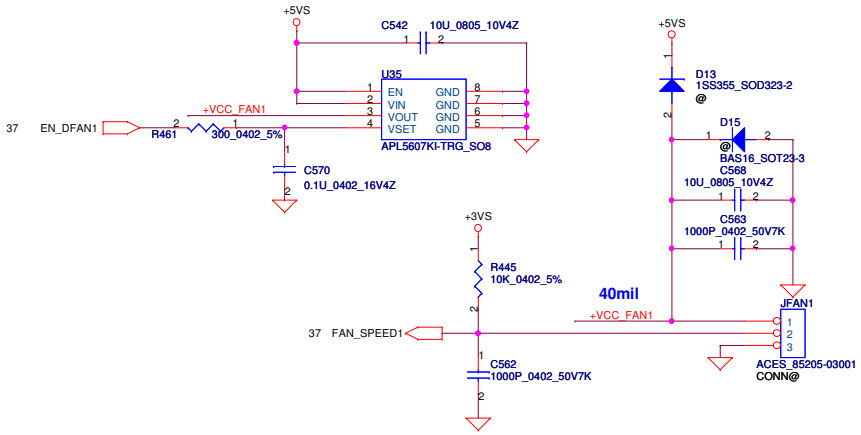
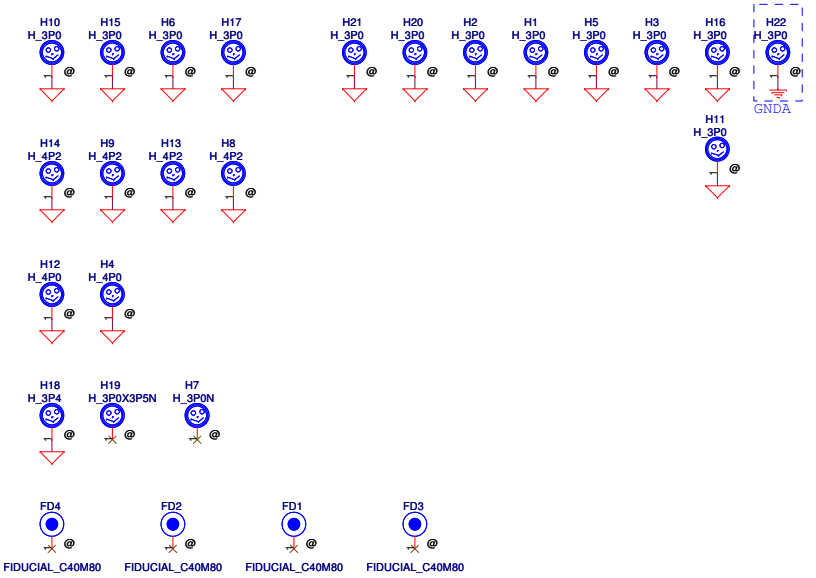
FAN1 Conn





Security Classification	Compal Secret Data		
Issued Date	2008/08/10	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: FAN & Screw Hole

Size: B | Document Number: NEW70 M/B LA-5891P Schematic | Rev: 1.0

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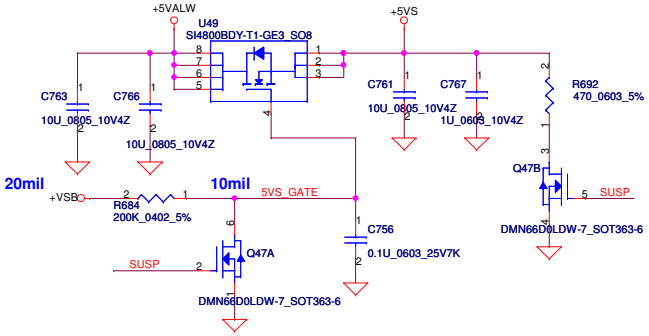
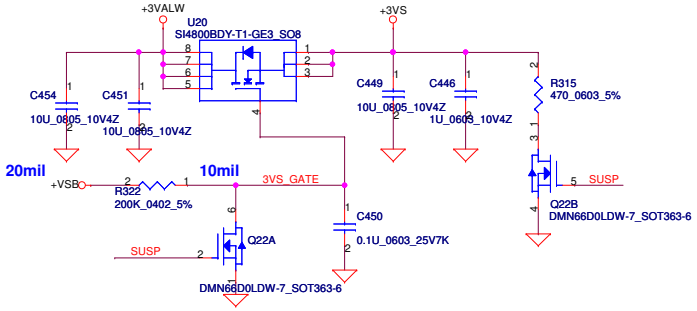
+5VALW TO +5VS

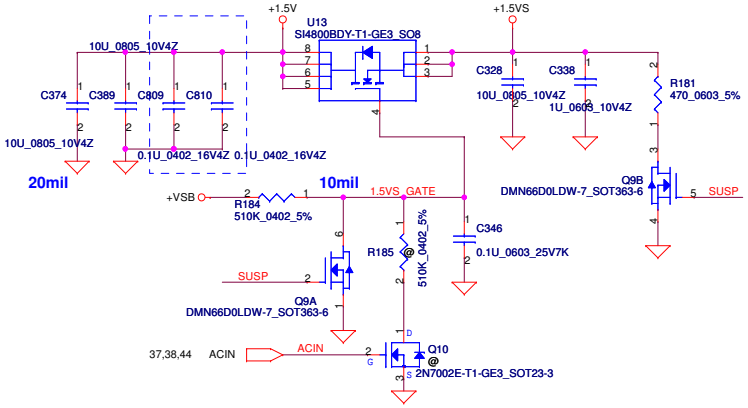


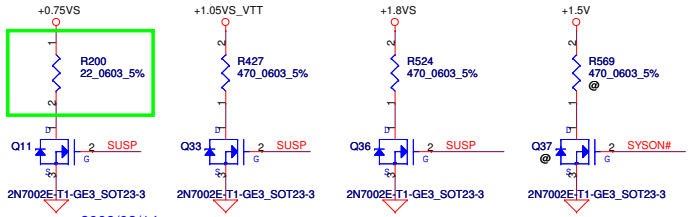
+3VALW TO +3VS



1211 EMI ADD 0.1U close PJ5

+1.5V to +1.5VS

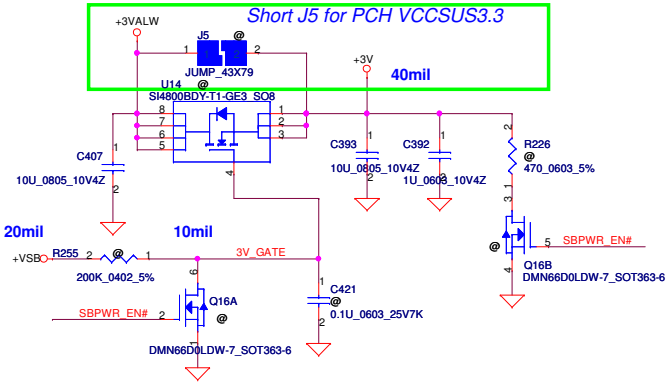




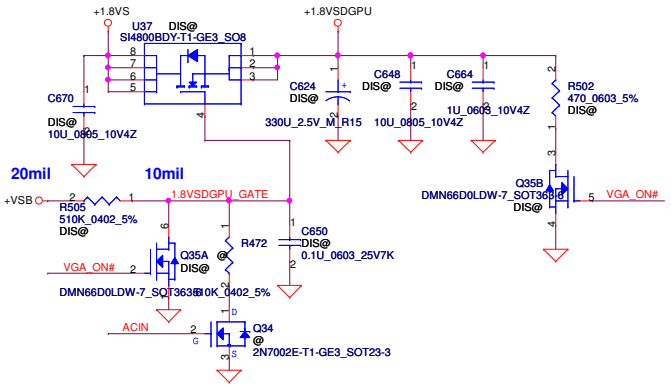
2009/08/14
CP_S3PowerReduction
WhitePaper_Rev0.9
0.75VS speed up discharge

+3VALW TO +3V(PCH AUX Power)

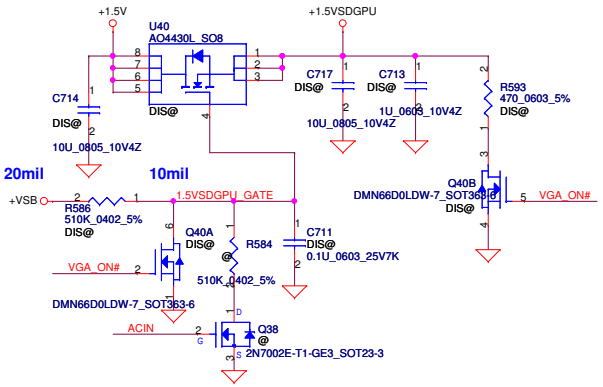
Short J5 for PCH VCCSUS3.3

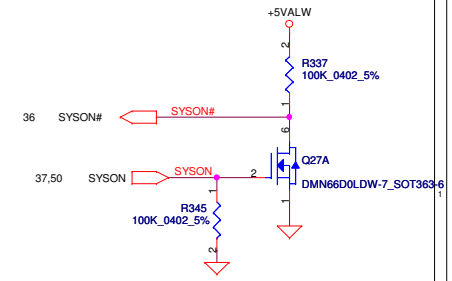


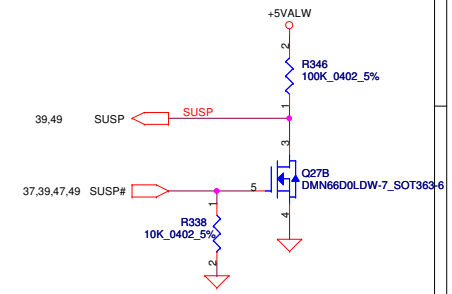
+1.8VS to +1.8VSDGPU for GPU

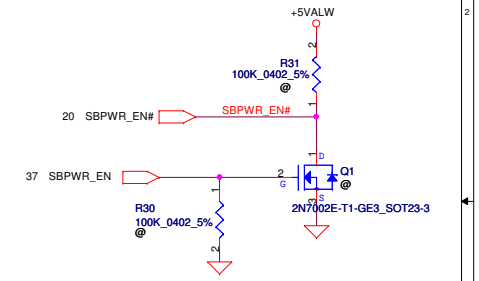


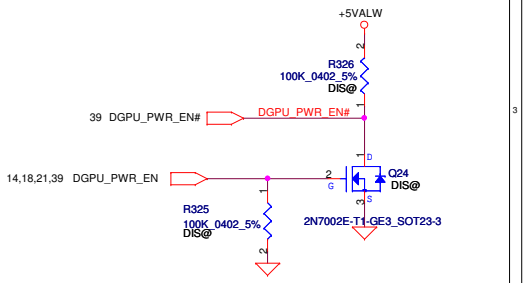
+1.5V to +1.5VSDGPU for GPU



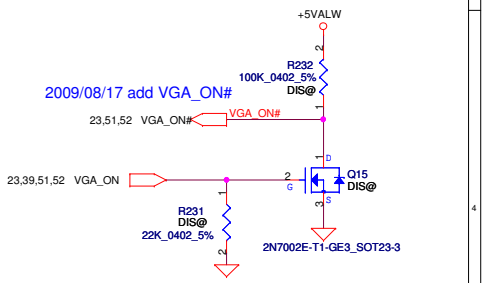








2009/08/17 add VGA_ON#



Security Classification	Compal Secret Data		
Issued Date	2008/08/10	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: DC Interface

Size: B | Document Number: NEW70 M/B LA-5891P Schematic | Rev: 1.0

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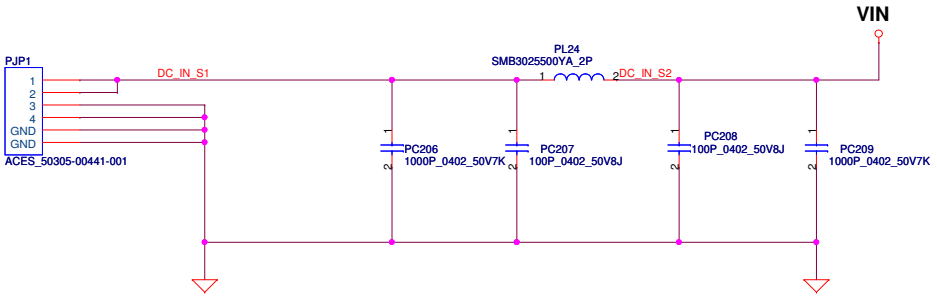
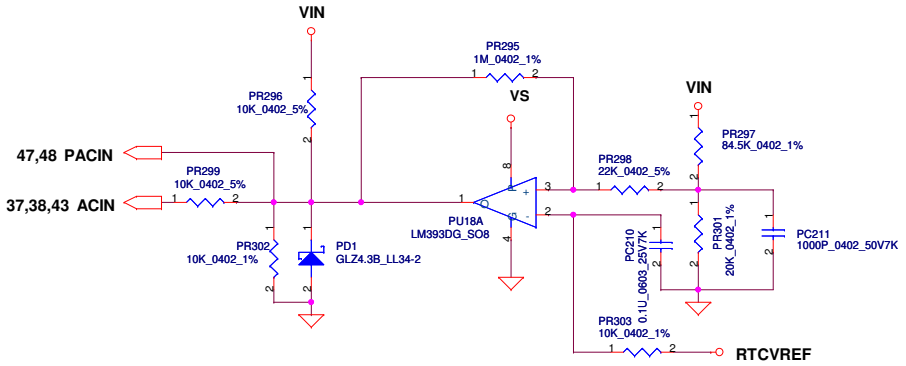
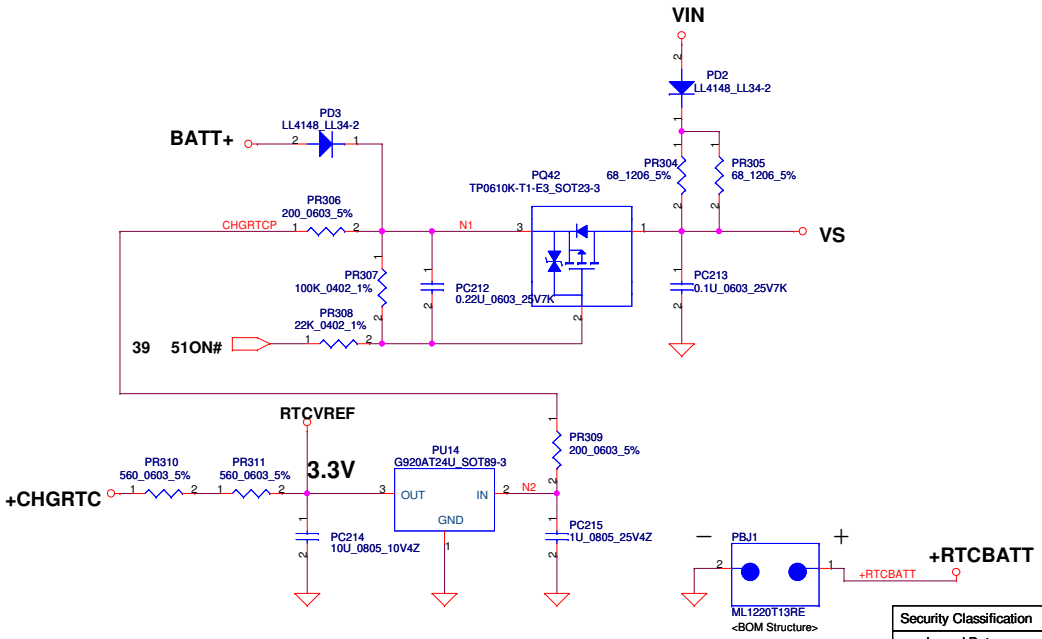
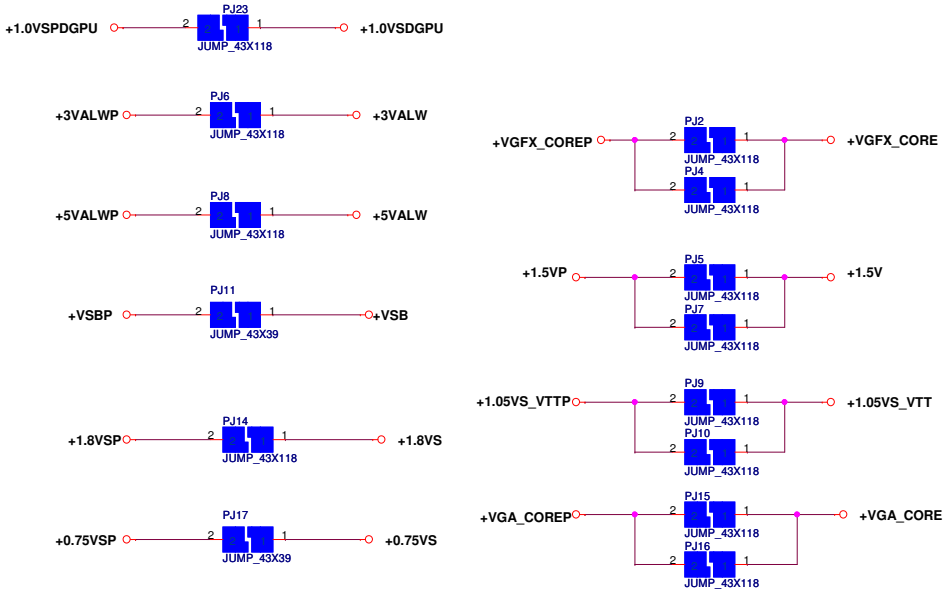




Vin Dectector

	Min.	Typ	Max.
H-->L	16.976V	17.525V	17.728V
L-->H	17.430V	17.901V	18.384V





Security Classification	Compal Secret Data		
Issued Date	2007/09/20	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: **DCIN & DETECTOR**

Size	Document Number	Rev
Custom	NEW70 M/B LA-5891P Schematic	1.0

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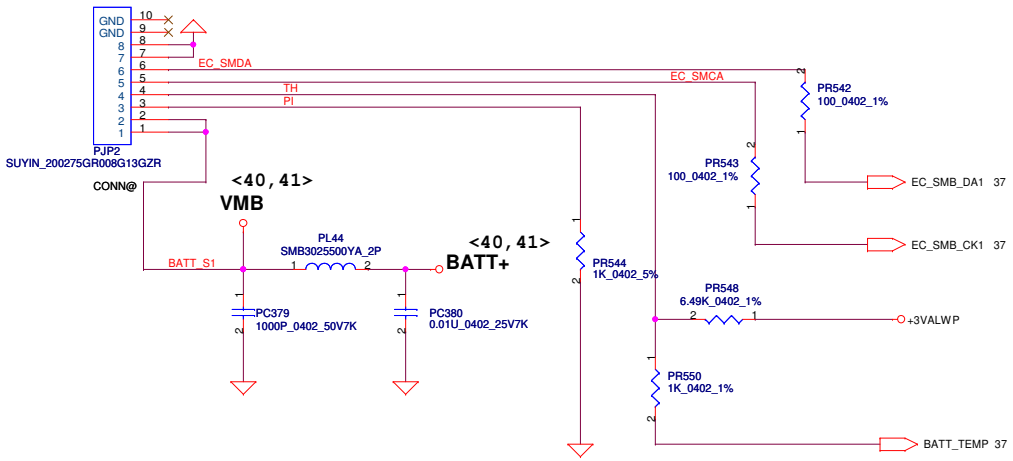
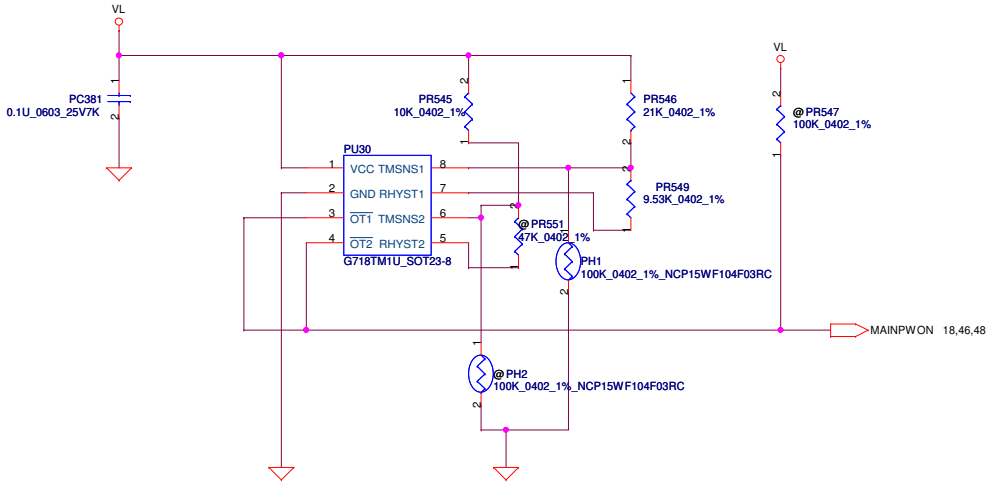
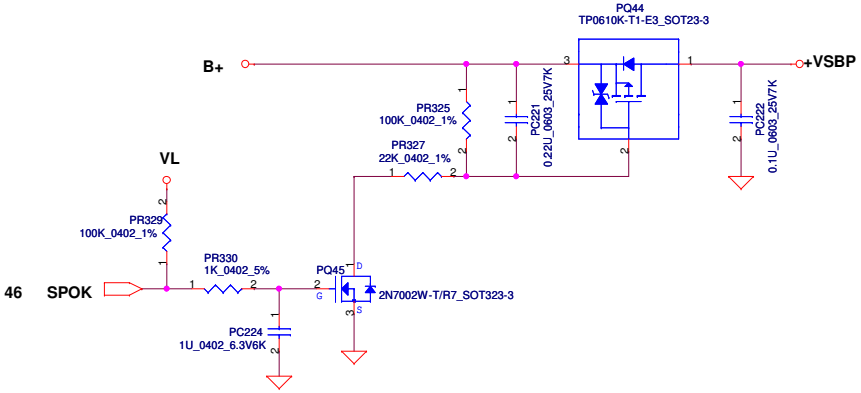


PH1 under CPU botten side :

CPU thermal protection at 92 degree C

Recovery at 56 degree C





Security Classification	Compal Secret Data		
Issued Date	2007/09/20	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: **BATTERY CONN / OTP**

Size	Document Number	Rev
Custom	NEW70 M/B LA-5891P Schematic	1.0

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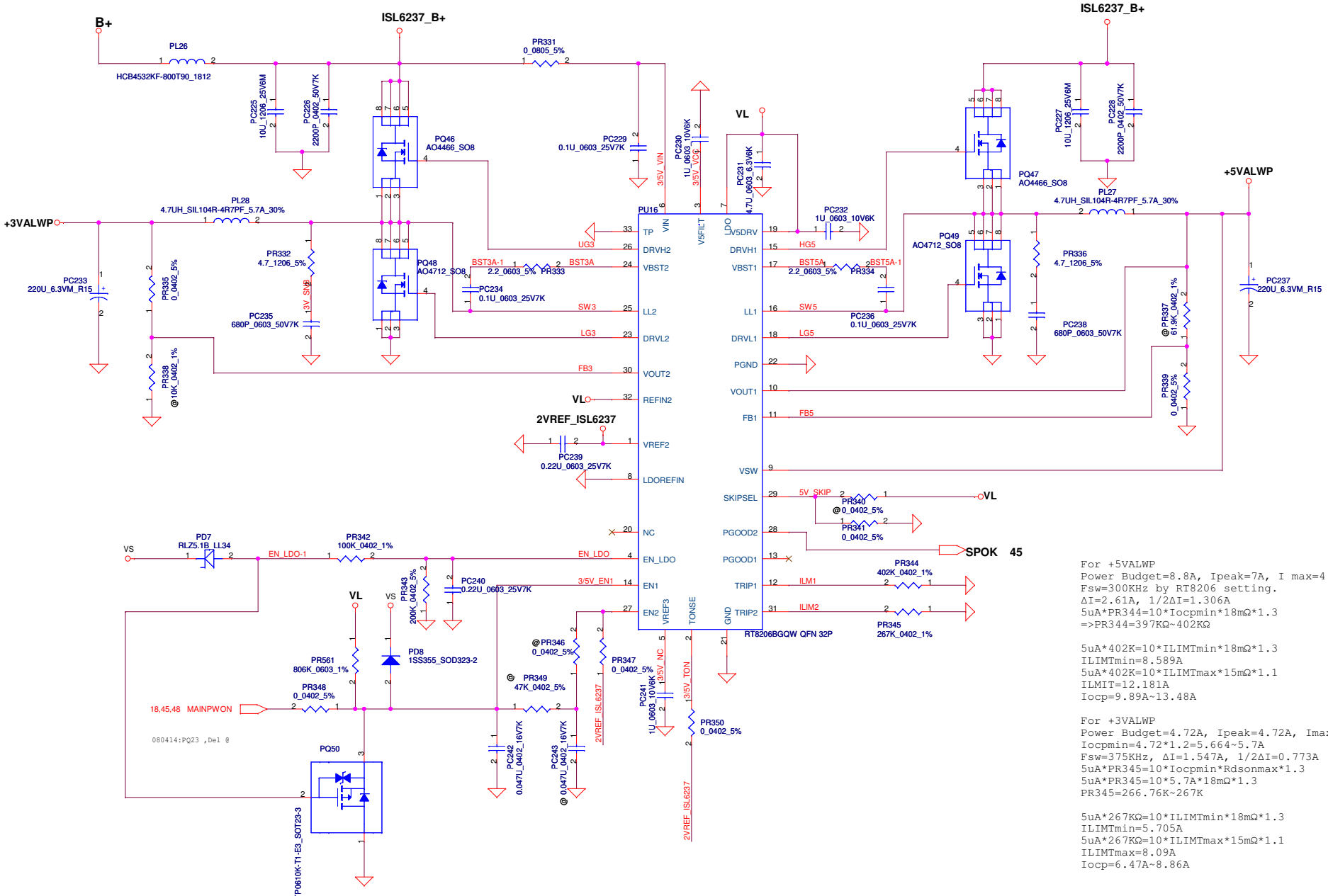

For +5VALWP
Power Budget=8.8A, Ipeak=7A, I max=4.9A
Fsw=300KHz by RT8206 setting.
ΔI=2.61A, 1/2ΔI=1.306A
5uA*PR344=10*Iocpmin*18mΩ*1.3
=>PR344=397KΩ~402KΩ

5uA*402K=10*ILIMTmin*18mΩ*1.3
ILIMTmin=8.589A
5uA*402K=10*ILIMTmax*15mΩ*1.1
ILMIT=12.181A
Iocp=9.89A~13.48A

For +3VALWP
Power Budget=4.72A, Ipeak=4.72A, Imax=4A
Iocpmin=4.72*1.2=5.664~5.7A
Fsw=375KHz, ΔI=1.547A, 1/2ΔI=0.773A
5uA*PR345=10*Iocpmin*Rdsonmax*1.3
5uA*PR345=10*5.7A*18mΩ*1.3
PR345=266.76K~267K

5uA*267KΩ=10*ILIMTmin*18mΩ*1.3
ILIMTmin=5.705A
5uA*267KΩ=10*ILIMTmax*15mΩ*1.1
ILIMTmax=8.09A
Iocp=6.47A~8.86A

Security Classification	Compal Secret Data		
Issued Date	2009/02/04	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: 3VALW/5VALW

Size: Custom | Document Number: NEW70 M/B LA-5891P Schematic | Rev: 1.0

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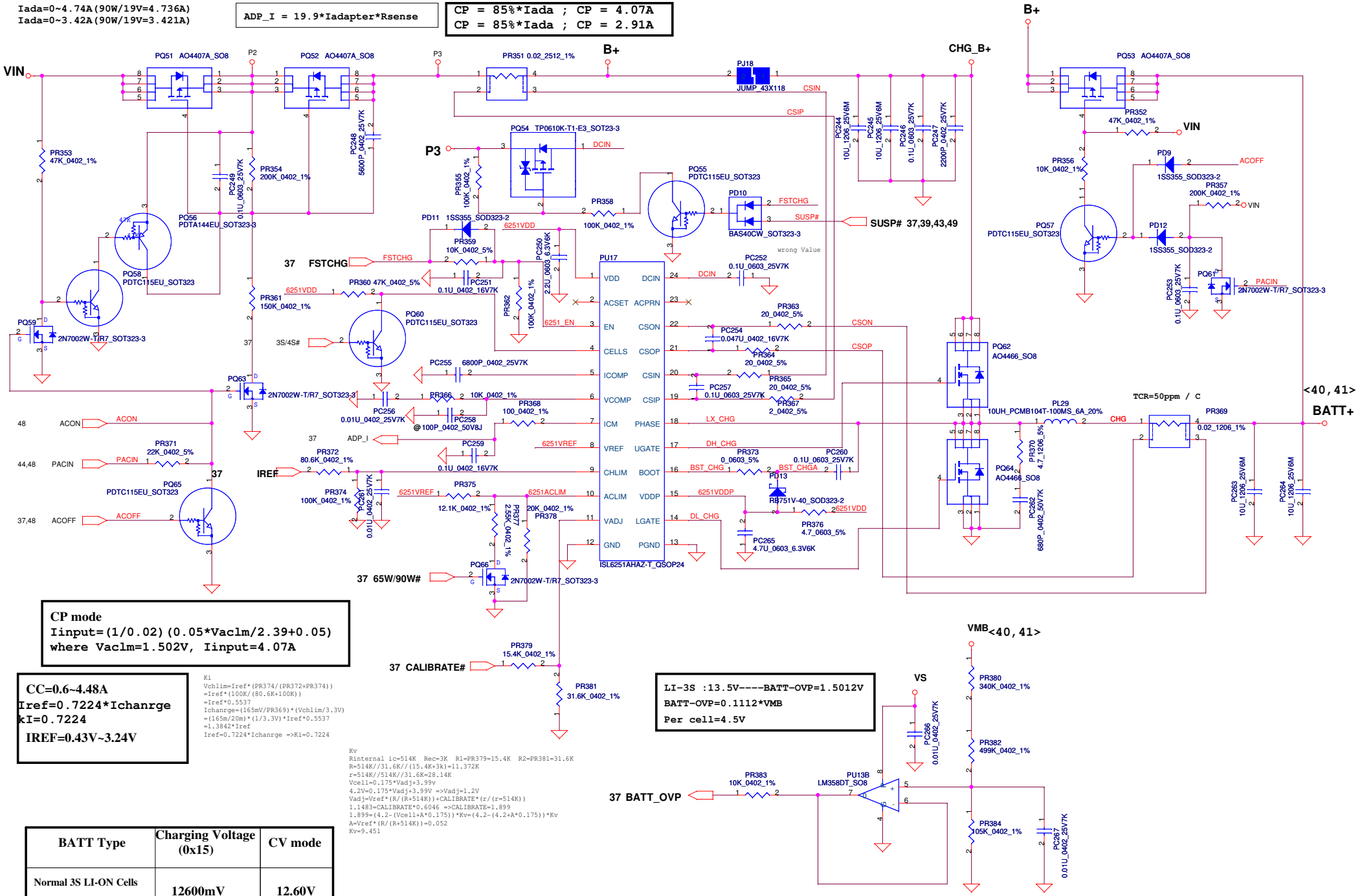
Iada=0~4.74A(90W/19V=4.736A)
Iada=0~3.42A(90W/19V=3.421A)

ADP_I = 19.9*Iadapter*Rsense

CP = 85%*Iada ; CP = 4.07A
CP = 85%*Iada ; CP = 2.91A



CP mode
Iinput=(1/0.02)(0.05*Vaclm/2.39+0.05)
where Vaclm=1.502V, Iinput=4.07A

CC=0.6~4.48A
Iref=0.7224*Ichanrge
kI=0.7224
IREF=0.43V~3.24V

Ki
Vchlim=Iref*(PR374/(PR372+PR374))
=Iref*(100K/(80.6K+100K))
=Iref*0.5537
Ichanrge=(165mV/PR369)*(Vchlim/3.3V)
=(165m/20m)*(1/3.3V)*Iref*0.5537
=1.3842*Iref
Iref=0.7224*Ichanrge =>Ki=0.7224

Kv
Rinternal ic=514K Rec=3K R1=PR379=15.4K R2=PR381=31.6K
R=514K//31.6K//((15.4K+3k)=11.372K
r=514K//514K//31.6K=28.14K
Vcell=0.175*Vadj+3.99v
4.2V=0.175*Vadj+3.99V =>Vadj=1.2V
Vadj=Vref*(R/(R+514K))+CALIBRATE*(r/(r=514K))
1.1483=CALIBRATE*0.6046 =>CALIBRATE=1.899
1.899=(4.2-(Vcell+A*0.175))*Kv=(4.2-(4.2+A*0.175))*Kv
A=Vref*(R/(R+514K))=0.052
Kv=9.451

LI-3S :13.5V----BATT-OVP=1.5012V
BATT-OVP=0.1112*VMB
Per cell=4.5V

BATT Type	Charging Voltage (0x15)	CV mode
Normal 3S LI-ON Cells	12600mV	12.60V

-

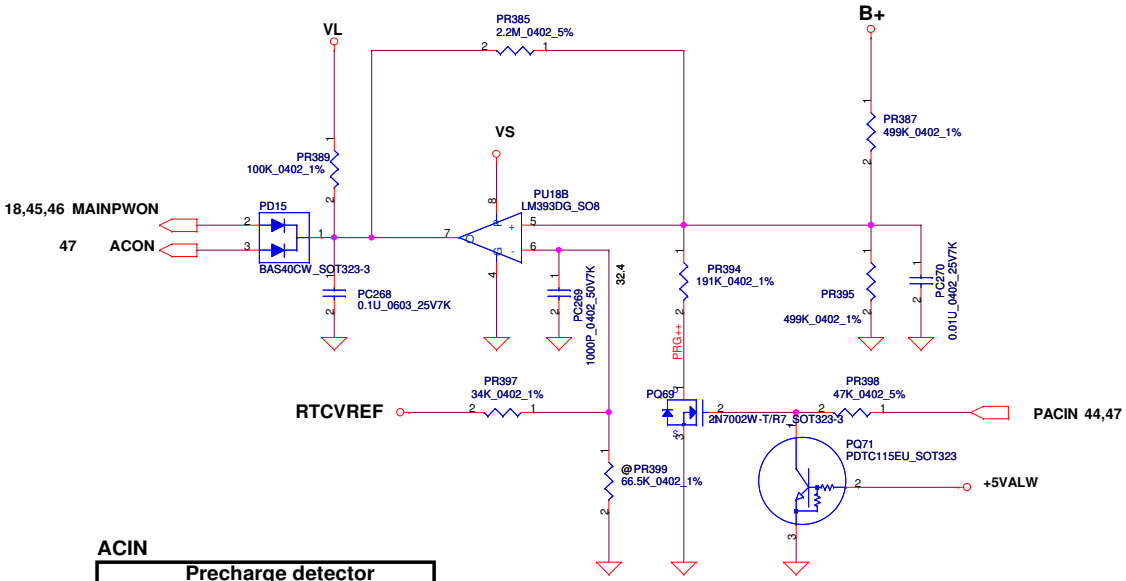
Security Classification	Compal Secret Data		
Issued Date	2007/09/20	Deciphered Date	2010/08/01

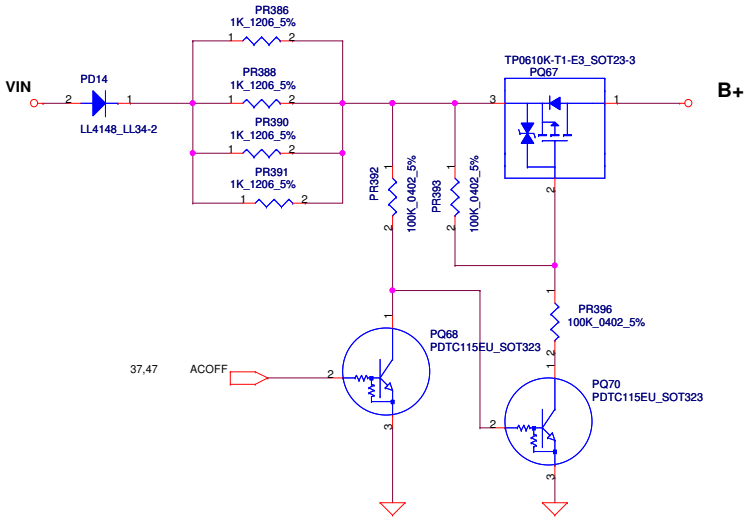
Compal Electronics, Inc.

Title: CHARGER

Size: Custom | Document Number: NEW70 M/B LA-5891P Schematic | Rev: 1.0

Date: Tuesday, December 29, 2009 | Sheet 47 of 59





ACIN

Precharge detector	Min.	typ.	Max
H-->L	14.589V	14.84V	15.243V
L-->H	15.562V	15.97V	16.388V

BATT ONLY

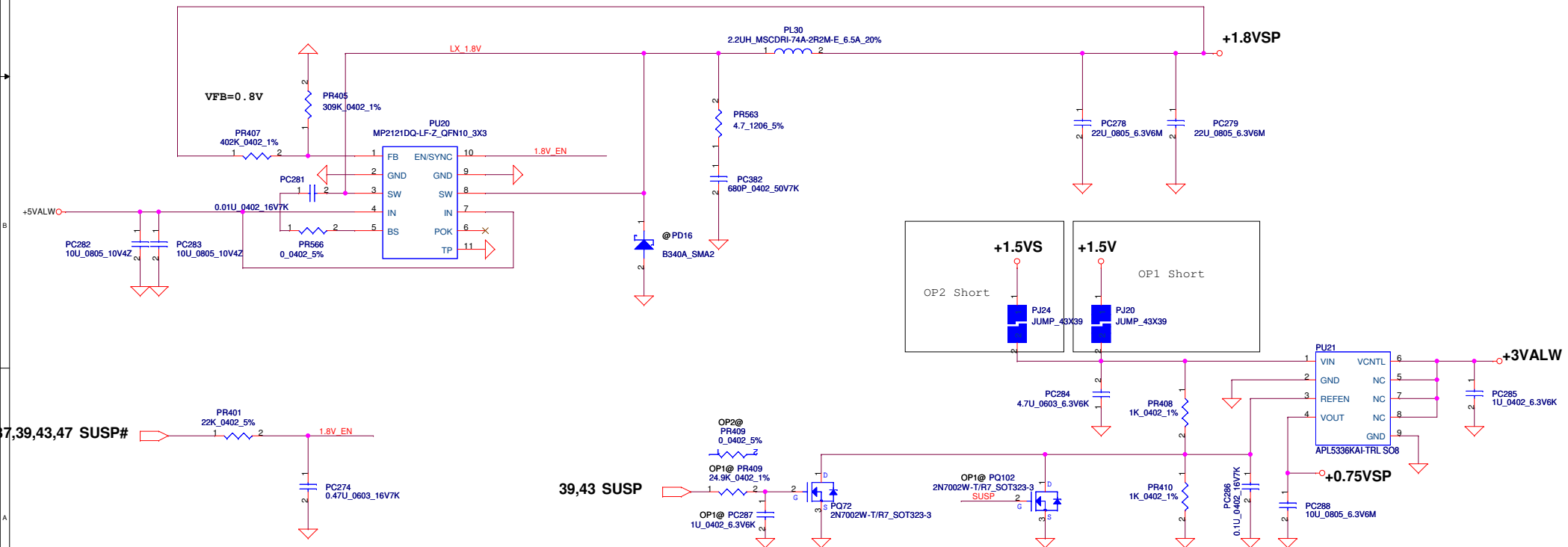
Precharge detector	Min.	typ.	Max
H-->L	6.138V	6.214V	6.359V
L-->H	7.196V	7.349V	7.505V

Security Classification	Compal Secret Data		
Issued Date	2007/09/20	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: **PRECHARGE**

Size	Document Number	Rev
Custom	NEW70 M/B LA-5891P Schematic	1.0
Date: Tuesday, December 29, 2009	Sheet 48 of 59	



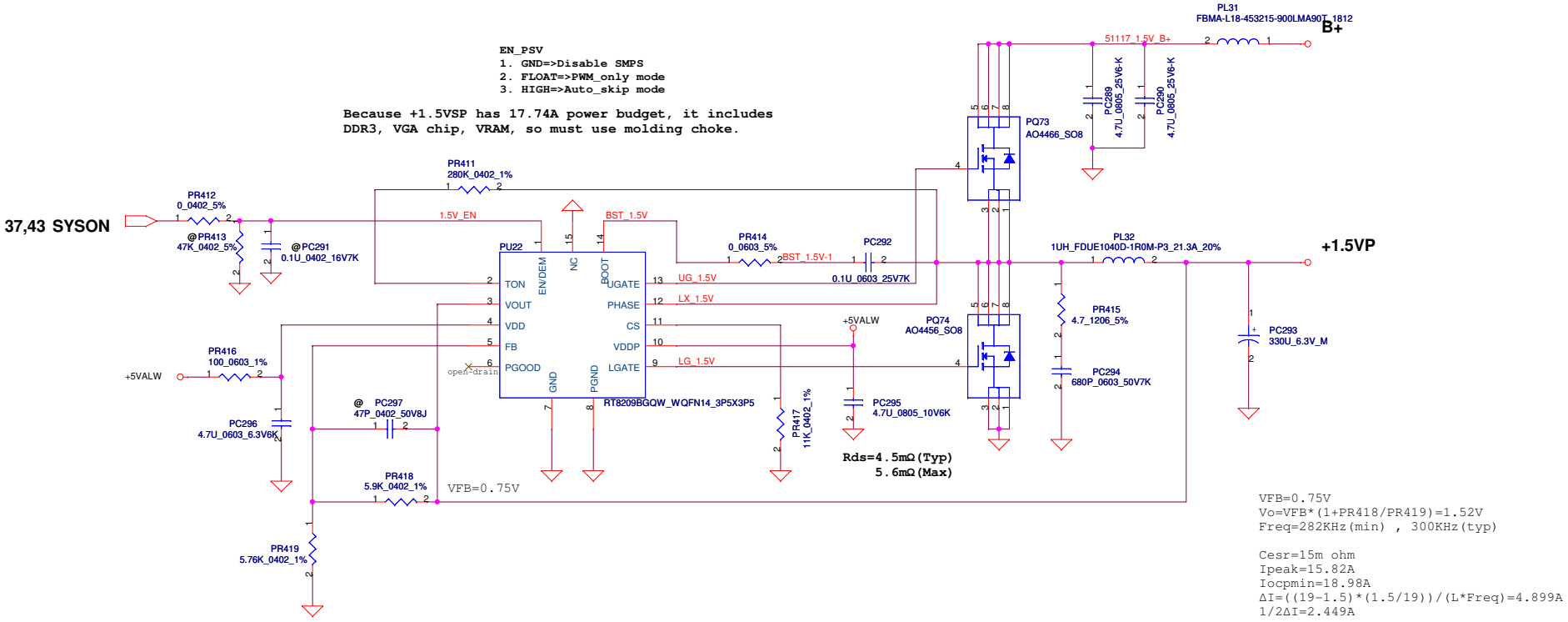
Security Classification	Compal Secret Data		
Issued Date	2007/09/20	Deciphered Date	2010/08/01

Compal Electronics, Inc.

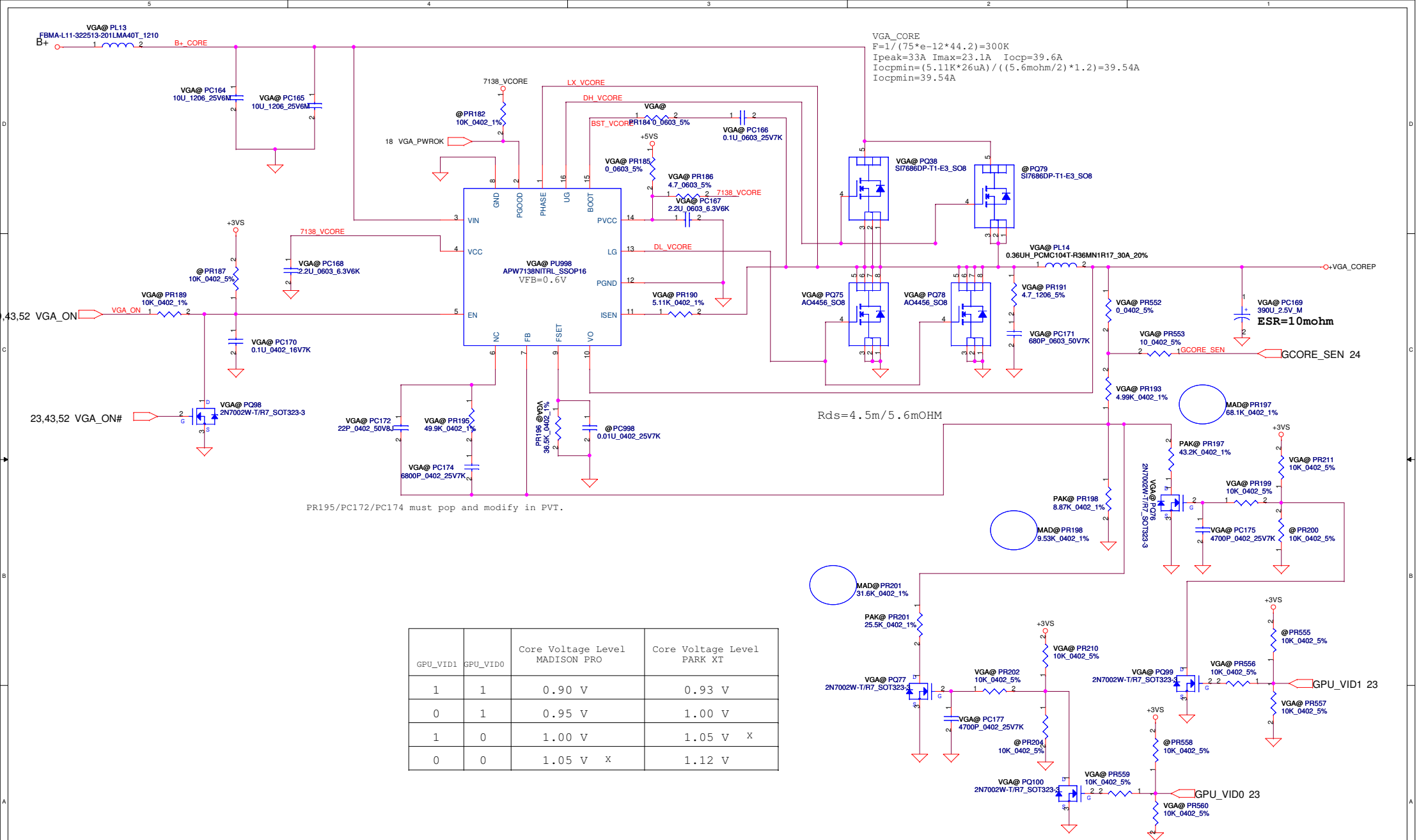
Title: **+1.8VSP/+0.75VSP**

Size	Document Number	Rev
Custom	NEW70 M/B LA-5891P Schematic	1.0

Date: Tuesday, December 29, 2009 | Sheet 49 of 59



Compal Electronics, Inc.	
Title	1.5VP
Size: Custom	Document Number: NEW70 M/B LA-5891P Schematic
Rev	1.0
Date: Tuesday, December 29, 2009	Sheet 50 of 59



GPU_VID1	GPU_VID0	Core Voltage Level MADISON PRO	Core Voltage Level PARK XT
1	1	0.90 V	0.93 V
0	1	0.95 V	1.00 V
1	0	1.00 V	1.05 V X
0	0	1.05 V X	1.12 V

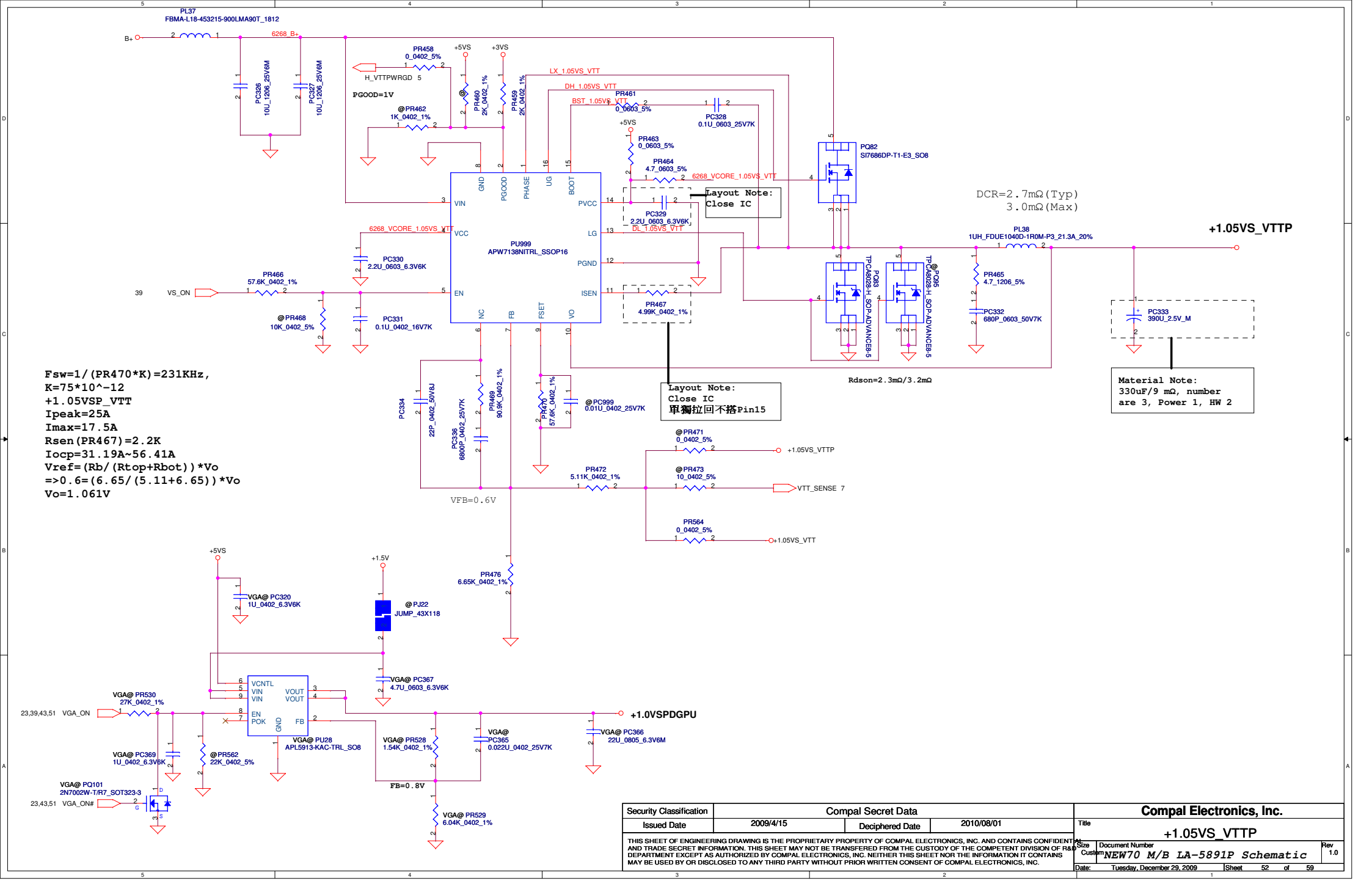
Security Classification	Compal Secret Data		
Issued Date	2007/12/18	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: VGA_COREP/+1.1VSDGPU

Size: Custom | Document Number: NEW70 M/B LA-5891P Schematic | Rev: 1.0

Date: Tuesday, December 29, 2009 | Sheet 51 of 59



Security Classification	Compal Secret Data		
Issued Date	2009/4/15	Deciphered Date	2010/08/01

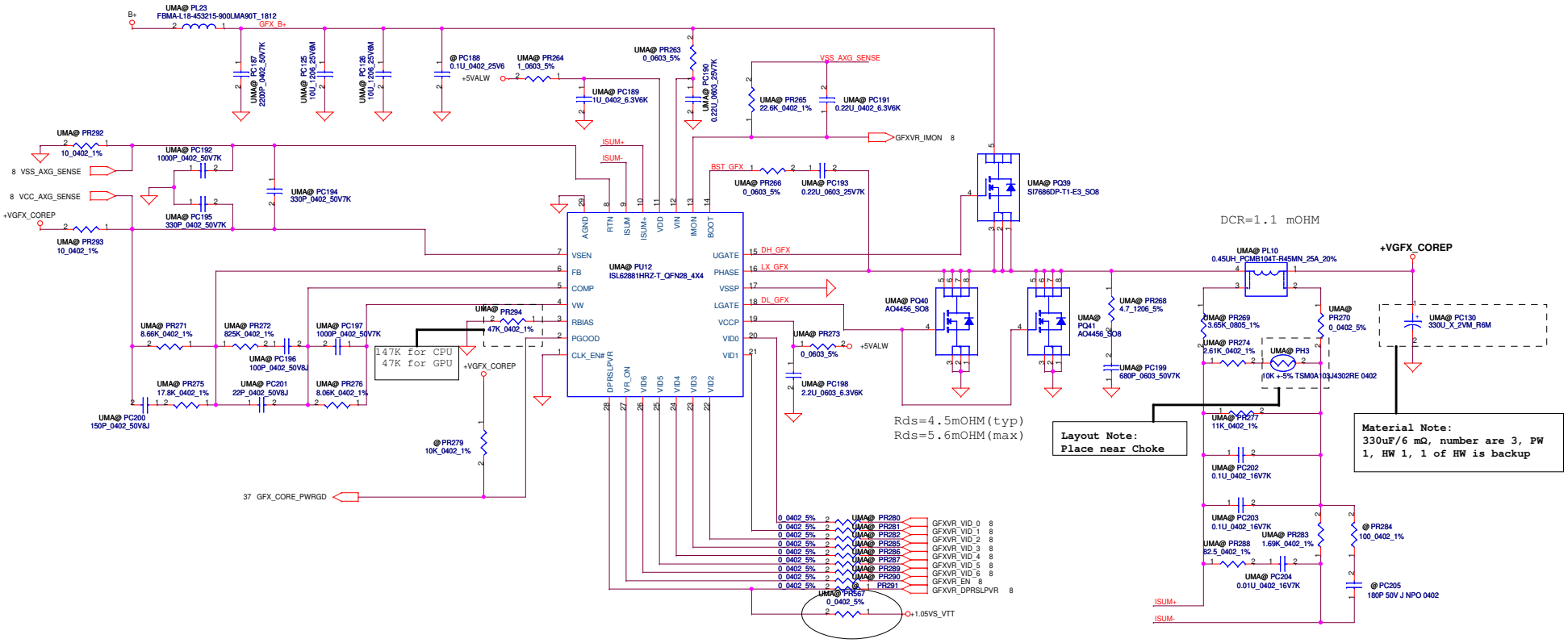
Compal Electronics, Inc.

Title: +1.05VS_VTTP

Size	Document Number	Rev
Custom	NEW70 M/B LA-5891P Schematic	1.0

Date: Tuesday, December 29, 2009 Sheet 52 of 59

Intel Auburndale CPU(Integrate Graphics) Ipeak=22A Imax=15A
OCP calculation : Assume DCR=1.1m ohm
G1=Rn/(Rn+Rsum)=0.617
where Rn=PR277 // (PR274+PH3)=5.875k ohm
Rsum=PR269=3.65k ohm
LL=2*Rdroop*G1*DCR/Ri= 6.96m V/A
where Rdroop=PR271=8.66k ohm, Ri=PR283=1.69k ohm
Iocp=OCP Threshold*Rdroop/LL=24.89A



2009-1214 common circiut modify.

Security Classification	Compal Secret Data		
Issued Date	2009/4/15	Deciphered Date	2010/08/01

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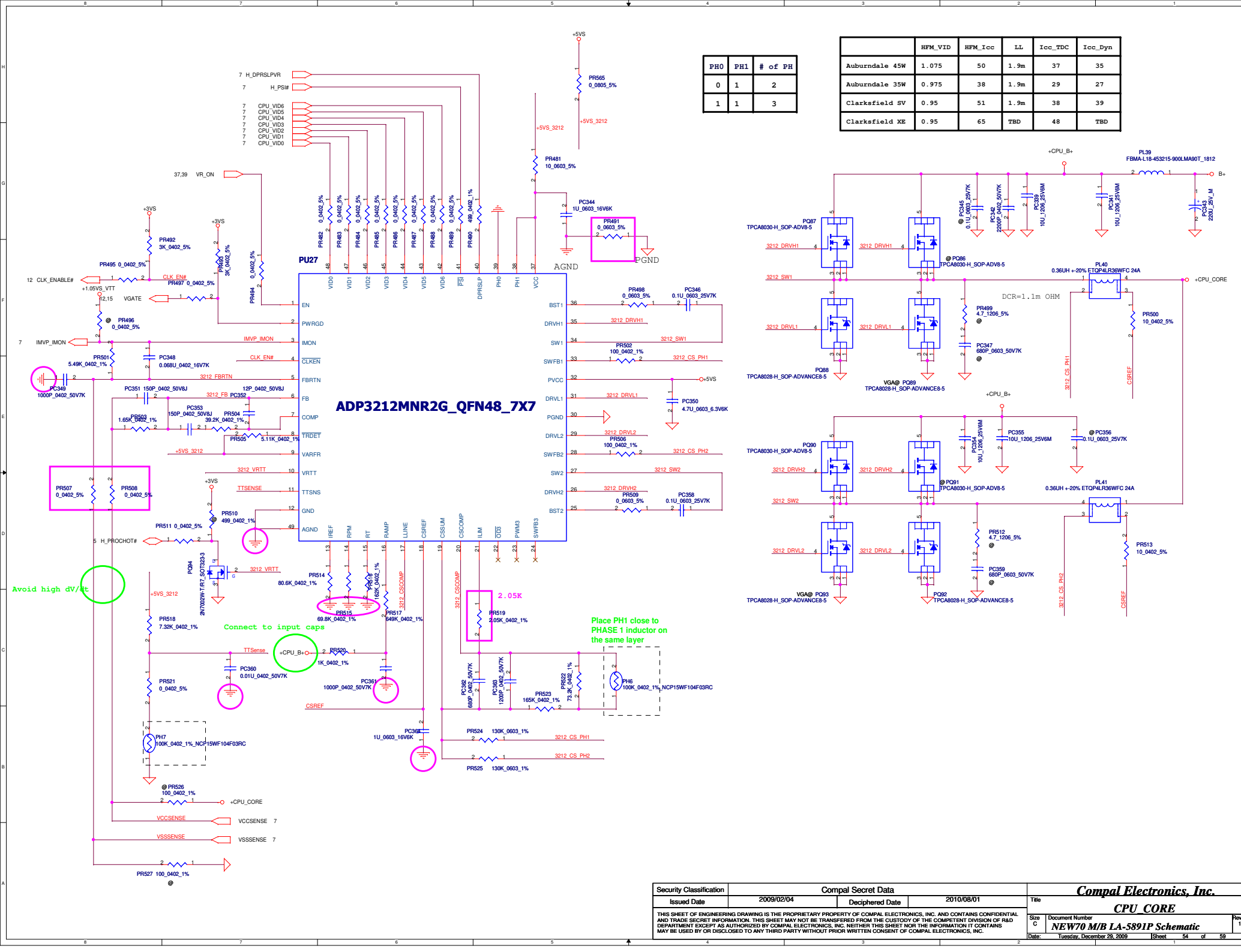
Compal Electronics, Inc.

Title: GFX_COREP

Size	Document Number	Rev
C	NEW70 M/B LA-5891P Schematic	1.0

Date: Tuesday, December 29, 2009 | Sheet 53 of 59



PH0	PH1	# of PH
0	1	2
1	1	3

	HFM_VID	HFM_Icc	LL	Icc_TDC	Icc_Dyn
Auburndale 45W	1.075	50	1.9m	37	35
Auburndale 35W	0.975	38	1.9m	29	27
Clarksfield SV	0.95	51	1.9m	38	39
Clarksfield XE	0.95	65	TBD	48	TBD

Security Classification	Compal Secret Data		
Issued Date	2009/02/04	Deciphered Date	2010/08/01

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Compal Electronics, Inc.			
Title	CPU_CORE		
Size C	Document Number NEW70 M/B LA-5891P Schematic		Rev 1.0
Date: Tuesday, December 29, 2009	Sheet 54 of 59		

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	For BOM unique.	For BOM unique.	0.1	46	Change PD8 from SC1SS355003(S DIO 1SS355) to SC100001K00(DIO 1SS355 SOD323 T/R-5K)	2009-1021	to DVT
2	For BOM unique.	For BOM unique.	0.1	54	Delete PQ86/PQ91 SB00000HL00(S TR TPCA8030-H 1N SOP). Add PQ87/PQ90 SB00000HL00(S TR TPCA8030-H 1N SOP).	2009-1021	to DVT
3	For UMA Arrandale CPU commond design.	For UMA Arrandale CPU, we just only pop 1 HS MOS and 1 LS MOS.	0.1	54	Delete PQ89/PQ93 SB00000GL00(S TR TPCA8028-H 1N SOP)	2009-1021	to DVT
4	For VTT Power rail commond design.	For VTT Power rail commond design, we pop 1 HS MOS and 1LS MOS.	0.1	52	Delete PQ95 SB00000GL00(S TR TPCA8028-H 1N SOP)	2009-1021	to DVT
5	CIS link error.	CIS link error.	0.1	54	Change PR500 from SD028100A00(S RES 1/16W 10 +-5% 0402) to SD028100A80(S RES 1/16W 10 +-5% 0402)	2009-1021	to DVT
6	BOM unique.	BOM unique.	0.1	47	Chnage PC265 from SE107475M80(S CER CAP 4.7U 6.3V M X5R 0603 to SE107475K80(S CER CAP 4.7U 6.3V K X5R 0603)	2009-1021	to DVT
7	BOM unique.	BOM unique.	0.1	49	Chnage PC284 from SE107475M80(S CER CAP 4.7U 6.3V M X5R 0603 to SE107475K80(S CER CAP 4.7U 6.3V K X5R 0603)	2009-1021	to DVT
8	BOM unique.	BOM unique.	0.1	54	Chnage PC350 from SE107475M80(S CER CAP 4.7U 6.3V M X5R 0603 to SE107475K80(S CER CAP 4.7U 6.3V K X5R 0603)	2009-1021	to DVT
9	BOM unique.(For Madison/Park SKU)	BOM unique.(For Madison/Park SKU)	0.1	52	Chnage PC367 from SE107475M80(S CER CAP 4.7U 6.3V M X5R 0603 to SE107475K80(S CER CAP 4.7U 6.3V K X5R 0603)	2009-1021	to DVT
10	BOM unique.	BOM unique.	0.1	46	Change PC225/PC227 from SE153106K80(S CER CAP 10U 25V K X6S 1206) to SE142106M80 (S CER CAP 10U 25V M X5R 1206)	2009-1021	to DVT
11	BOM unique.	BOM unique.	0.1	54	Change PC339/PC341 from SE153106K80(S CER CAP 10U 25V K X6S 1206) to SE142106M80 (S CER CAP 10U 25V M X5R 1206) Change PC354/PC355 from SE153106K80(S CER CAP 10U 25V K X6S 1206) to SE142106M80 (S CER CAP 10U 25V M X5R 1206)	2009-1021	to DVT
12	+1.05VS_VTTP Cost down 1 LS MOS. HW request.	+1.05VS_VTTP Cost down 1 LS MOS. Because +1.05VS_VTT has voltage drop issue, HW request, remote sense to close to PCH.	0.2	52	Delete PQ95 SB00000GL00(S TR TPCA8028-H 1N SOP) Delete PR471 SD028000080(S RES 0 0402 5%) Delete PR473 from SD034100A80(S RES 10 0402 5%) Add PR564 SD028000080(S RES 1/16W 0 0402 5%)	2009-1029	to DVT
13							
14	Adjust +1.05VS_VTTP OCP.	Because we remove a LS MOS, so OCP must adjust.	0.2	52	Change PR467 from SD000004O80(S RES 1/16W 2.2K +-1% 0402) to SD034499180(S RES 1/16W 4.99K 0402 1%)	2009-1029	to DVT
15	+1.8VSP2, Using MP2121 for 1.8V only.	No need to use LDO for +1.8V. Delete all PU19 circiut.	0.2	49	Delete PU19 SA00001NC00 (S IC APL5913-KAC-TRL SO 8P)	2009-1029	to DVT
16	+1.8VSP2, Using MP2121 for 1.8V only.	No need to use LDO for +1.8V. Delete all PU19 circiut.	0.2	49	Delete PR402 SD034150280, PR404 SD034120280. Delete PC273 SE075103K80 PC275 SE000000I10	2009-1029	to DVT
17	+1.8VSP2, Using MP2121 for 1.8V only.	No need to use LDO for +1.8V. Delete all PU19 circiut.	0.2	49	Delete PC272 SE107475K80, PC271 SE107105M80 Delete PR401 and PR403 SD028220280, PC274 SE026474K80	2009-1029	to DVT
18	+VGA_COREP, efficiency issue.	Increase Freq, decrease choke, to improve efficiency.	0.2	51	Change PR196 from SD034442280 to SD034365280. Change PL14 from SL200000V00 to SH000005680	2009-1029	to DVT
19	+VGA_COREP, OVP issue.	Becasue if PR199/PR202 pop 0ohm, it will cause OVP when VID change from 00 to 11)	0.2	51	Change PR199/PR202 from SD028000080 to SD028100280 (S RES 1/16W 10K 0402 5%)	2009-1029	to DVT
20	+VGA_COREP, cost issue.	Cost down.	0.2	51	Change PQ75/PQ78 from SB00000GL00(S TR TPCA8028-H 1N SOP) to SB000009F80(S TR AO4456 1N SO8)	2009-1029	to DVT
21	+VGA_COREP, satndard design.	+VGA_COREP, satndard design, pop 1HS MOS and 2LS MOS, so remove one HS MOS PQ79.	0.2	51	Delete PQ79 SB000008L80 (S TR SI7686DP-T1-E3 1N POWERPAK SO8)	2009-1029	to DVT
22	+GFX_COREP, spike issue.	Because +GFX_COREP has spike voltage issue, add schottky diode across GFXVR_EN and VS_ON to solve it.	0.2	51	Add PD17 SCS00000Z00 (S SCH DIO RB751V-40 SOD-323)	2009-1029	to DVT
23	+VGA_COREP, OCP caaculation erroe issue.	Because VGA_CORE has 2 LS MOS, APW7138 detect LS Rdson, so when caculate OCP, Rdson must reduce 1/2.	0.2	51	Change PR190 from SD034649180 to SD034511180 (S RES 1/16W 5.11K 0402 1%)	2009-1029	to DVT

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	CPU choke TOHO quality issue.	Because TOHO has quality issue before, change to Panasonic choke.	0.2	54	Change PL40/PL41 from SHSH00000F000 S COIL 0.36UH +-20% SF-I104-R36 23A to SH000005680 S COIL 0.36UH +-20% PCMC104T-R36MN1R17	2009-1029	to DVT
2	+VGA_COREP, voltage change.	ATI updated Park output voltage.	0.2	51	Change PR197 from SD034649280 to SD034432280.	2009-1029	to DVT
3	+VGA_COREP, voltage change.	ATI updated Park output voltage.	0.2	51	Chnage PR198 from SD034953180 to SD034887180.	2009-1029	to DVT
4	+VGA_COREP, voltage change.	ATI updated Park output voltage.	0.2	51	CHange PR201 from SD034316280 to SD034255280.	2009-1029	to DVT
5	+VGA_COREP, initial state unknow.	When VGA_CORE start up, but VBIOS doesn't ready, the VID is unknow, add pull down R.	0.2	51	Add PR557/PR560 SD028100280(S RES 1/16W 10K 0402 5%)	2009-1029	to DVT
6	+1.0VSPDGPU,adjust power sequence.	Because HW request that adjust power sequence, we will follow the value which given by HW.	0.2	52	Change PC369 from SE076104K80 to SE000000K80 (S CER CAP 1U 0402 X7R)	2009-1029	to DVT
7	+1.0VSPDGPU,adjust power sequence.	Because HW request that adjust power sequence, we will follow the value which given by HW.	0.2	52	Change PR530 from SD028150380 to SD034270280 (S RES 1/16W 27K 0402 1%)	2009-1029	to DVT
8	+1.0VSPDGPU,adjust power sequence.	Because HW request that adjust power sequence, we will follow the value which given by HW.	0.2	52	Delete PR562 SD028220280 (S RES 1/16W 22K +-5% 0402)	2009-1029	to DVT
9	+0.75VSP,adjust power sequence.	Because HW request that adjust power sequence, we will follow the value which given by HW.	0.2	49	Change PR409 SD028000080 to SD034249280(24.9K 0402 1%) Change PC287 from SE076104K80 to SE000000K80	2009-1029	to DVT
10	=1.8VSP, voltage too small.	Because +1.8VSP drop in HW side, increase +1.8VSP.	0.2	49	Change PR405 from SD034316380(S RES 1/16W 316K +-1% 0402) to SD034309380(S RES 1/16W 309K 0402 1%)	2009-1029	to DVT
11	+GFX_COREP, spike voltage issue.	Because GFX_COREP has spike voltage issue, originally we add a schottcky diode to solve it, but Intel's command is that do not add it, because of overdriving, so delete it now.	0.3	53	Delete PD17 SCS00000Z00(S SCH DIO RB751V-40 SOD-323)	2009-1104	to DVT
12	+GFX_COREP, EMI request.	EMI request to add snubber.	0.3	53	Add PR268 SD001470B80(S RES 1/4W 4.7 +-5% 1206) Add PC199 SE025681K80(S CER CAP 680P 50V K X7R 0603)	2009-1104	to DVT
13	+1.05VS_VTTP, EMI request.	EMI request to add snubber.	0.3	52	Add PR465 SD001470B80(S RES 1/4W 4.7 +-5% 1206) Add PC332 SE025681K80(S CER CAP 680P 50V K X7R 0603)	2009-1104	to DVT
14	+VGA_COREP, EMI request.	EMI request to add snubber.	0.3	51	Add PR191 SD001470B80(S RES 1/4W 4.7 +-5% 1206) Add PC171 SE025681K80(S CER CAP 680P 50V K X7R 0603)	2009-1104	to DVT
15							
16	+1.5VP, EMI request.	EMI request to add snubber.	0.3	50	Add PR415 SD001470B80(S RES 1/4W 4.7 +-5% 1206) Add PC294 SE025681K80(S CER CAP 680P 50V K X7R 0603)	2009-1104	to DVT
17	Charger, EMI request.	EMI request to add snubber.	0.3	47	Add PR370 SD001470B80(S RES 1/4W 4.7 +-5% 1206) Add PC262 SE074681K80 (S CER CAP 680P 50V K X7R 0402)	2009-1104	to DVT
18	CPU_COREP, transient, load line modify.	CPU_COREP, transient, load line modify.	0.3	54	Change PR524/PR525 from SD014120380 to SD014130380. Change PR501 from SD034536180 to SD034549180 Change PC362 from SE074391K80 to SE074681K80 Change PL40/PL41 from SH000005680 to SH12036BM00.	2009-1104	to DVT
19	+VSBP, EMI request.	EMI request to add cap to reduce EMI noise on B+	0.3	45	Add PC221 SE000005280 S CER CAP .22U 25V K X7R 0603. Add PC222 SE042104K80 S CER CAP .1U 25V K X7R 0603	2009-1104	to DVT
20	+1.8VSP BOM error.	Loss +1.8VSP enable circiut.	0.3	49	Add PR401 SD014220280 S RES 1/16W 22K 0402 5% Add PC274 SE026474K80 S CER CAP 0.47U 16V K X7R 0603	2009-1104	to DVT
21	+VGA_COREP, output voltage change.	Because ATI change Park output voltage, we saperate Park and Madison by PAK@ and MAD@. And Change Madison X63 BOM.	0.4	51	Change PR197 from SD034432280 to SD034681280. Chnage PR198 from SD034887180 to SD034953180. Change PR201 SD034255280 to SD034316280.	2009-1113	to DVT
22	+CPU_COREP, power measure.	Because HW want to measure CPU_CORE IC power loss, Add 0805 R to saperate +5VS.	0.4	54	Add PR565 SD002000080 S RES 1/8W 0 +-5% 0805	2009-1113	to DVT

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	+CPU_COREP, IMON design change.	Intel release IMON RC time constant new request, change PC348 to 0.068u to meet spec.	0.4	54	Change PC348 from SE076103K80 S CER CAP .01U 16V K X7R 0402 to SE000003J80 S CER CAP 0.068U 16V K X7R 0402	2009-1113	to DVT
2	+CPU_COREP, cost issue.	SF000000G80 will cost up, change to SF22004M210.	0.4	54	Change PC343 from SF000000G80 to SF22004M210.	2009-1113	to DVT
3	+3V/+5V cost issue.	Because Nippon cost up thier OS-CON cap, so we change Nippon cap to Sanyo cap by sourcer request.	0.5	46	Change PC233/PC237 from SF22001M300 S ELE CAP 220U 6.3V M F60(6.3X5.7) PXC to SF22001M200 S ELE CAP 220U 6.3V M B C6 SVPC ESR15	2009-1118	to DVT
4	+1.05VS_VTTP issue.	+1.05VS_VTTP choke unique to +1.5VP.	0.5	52	Change PL38 from SH000008V80 S COIL 1UH +-20% PCMB103E-1R0MS 20A to SH000009U00 S COIL 1UH +-20% FDUE1040D-1R0M=P3 21.3A	2009-1118	to DVT
5	+VGA_COREP 2nd source issue.	In order to phase in 2nd source of APW7138, must add Pin6 components to meet ISL6268 reqirement.	0.6	51	Add PC172 SE071220J80 S CER CAP 22P 50V J NPO 0402 Add PC174 SE075682K80 S CER CAP 6800P 25V K X7R 0402 Add PR195 SD034909280 S RES 1/16W 90.9K 0402 1%	2009-1208	to PVT
6	+VGA_COREP 2nd source issue.	In order to phase in 2nd source of APW7138, must add Pin6 components to meet ISL6268 reqirement.	0.6	51	Change location PU23 to PU998.	2009-1208	to PVT
7	+1.05VS_VTTP 2nd source issue.	In order to phase in 2nd source, change ISL6268 to APW7138.	0.6	52	Change PU26 from SA00001HT80 S IC ISL6268CAZ-T SSOP 16P to PU999 SA00002O600 S IC APW7138NITRL SSOP 16P	2009-1208	to PVT
8	+1.05VS_VTTP 2nd source issue.	APW7138 needn't pop PC335.	0.6	52	Delete PC335 SE075103K80 S CER CAP .01U 25V K X7R 0402 and change location to PC999.	2009-1208	to PVT
9	HDD LED flash issue.	HDD LED will flash when plug in adapter, because +3VS rise a little. HW request add PC224 to solve it.	0.6	45	Add PC224 SE000000K80 S CER CAP 1U 6.3V K X5R 0402	2009-1208	to PVT
10	HDD LED flash issue.	If add PC224, must change PR330 from 0 to 1K to avoid SPOK pin fail. that is add a current limit R on SPOK pin.	0.6	45	Chnage PR330 from SD028000080 to SD028100180.	2009-1208	to PVT
11	BOM error.	+1.8VSP choke use wrong material.	0.6	49	Change PL30 from SH000006I80 S COIL 2.2UH +-20% PCMC063T -2R2MN 8A to SH000009Q00 S COIL 2.2UH 20% MSCDRI-74A-2R2M-E 6.5A	2009-1208	to PVT
12							
13							
14							
15							
16							
17							
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Compal Electronics, Inc.			
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A --> B Change List

1012:----------
Page 29,30 Update F1,F2 symbol to SP04301P120(F_SMD1812P110TF)
Page 36,38 C789,C788,C684 symbol update (have pin define)
Page 31, U3 P/N change from SA00001RM00 to SA00003O900
1102:----------
Page 7,8 C97,C675,C134,C136,C251,C268,C541,C667 symbol update from SGA00002380 to SGA00002U00
Page 23. Add C609 0.1u_0402(SE076104K80) R739 24K_0402(SD034240280) fix +3VSDGPU Ramp up issue
Page 17,35 Add 1 more USB trace to 3G/B connector from PCH USB20_P10 & USB20_N10
1103:----------
Page 43 R200 change symbol from 22_0402_5% to 22_0603_5%
Page 39 SW1,SW4 BOM structure change to @
Page 36 C789.2 power source +3VS change to +3VALW
1104:----------
Page 8, Add C797,C798,C799,C800 0.1u_0402 at between +1.5V&+1.5V_1(Intel suggest)
Page 15,37 U41.F3 modify net from GPIO62 to susclk
Page 37 Add R740(@) close U32.123
1105:----------
Page 8 R98 change from 4.7K_0402_5% to 330ohm_0402_5% (Intel feekback VGFX_CORE issue solution)
1109:----------
Page 23 Change R717,R718,R720,R509 BOM structure from VGA@ to @ (Madison&Park prodution remove JTAG option2)
Page 24 Change R64 BOM structure from @ to VGA@ (Madison&Park prodution remove JTAG option2)
Page 23 Remove and short R729 (A2VDD)
Page 23 Change C600,C172,C599 BOM structure from VGA@ to @ (+A2VDD)
Page 23 Remove and short L6 (+A2VDDQ)
Page 26 Remove and short R730,R731,R732,R733,R734,R735,R736,R737,R738, (DPB,DPC,DPD power source)
Page 37 Add R508 100K_0402 Pull down to GND(EC E51TXD_P80DATA)(fix Intel WLAN Card reset issue)
RF request:----------
Page 35 Add C801 (SE071470J80 47P_0402) and C173(SE000005T80 10U_0603)(+3VS_WWAN)
Page 23 Remove R508 (100_0402) change to C802(@) (12P_0402_50V8J)(SE071120J80) (VGA_CLK_27M)
Page 29 Add two shunt C804,C803 12P_0402_50V8J(SE071120J80)(P31.DDC to HDMI conn)
Page 29 Add two shunt C805,C806 22P_0402_50V8J(SE071220J80)(P29.LCD Conn)
pop R403(47_0402) and C516 (22P_0402)(CLK_PCI_LPC)
pop R163 (10_0402)and C319 (10P_0402) (CLK_BUF_ICH_14M)
EMI request:----------
Page 36 POP D26, CM1293-04SO(SC300000O00)
Page 38,40,41 POP D18,D19,D10,D9,D11,D28,D30 PJDLC05C(SCA00001100)
1110:----------
Page 38 Add Q53(ACIN_LED#)
1111:----------
Page 40 C775,C776,C777,C778 change Symbol from SE093475K80(4.7U_0805) to SE107475M80(4.7U_0603)
Page 38 R341,R343 100_0402_5% change to 680_0402_5%(BLUE LED Bright)
Page 38 R342,R344 300_0402_5% change to 3.9K_0402_5%(Orange LED Bright)
1113:----------
Page 8 R98 change from 330_0402_5% to 470_0402_5%(SD028470080)
Page 23 Change back R717,R718,R720,R509 BOM structure from @ to VGA@ (Madison&Park prodution remove JTAG option2)
Page 24 Change back R64 BOM structure from VGA@ to @ (Madison&Park prodution remove JTAG option2)
1116:----------
Page 13 U41 change P/N from SA00003N700 to SA00003N7B0
Page 34 T16 change P/N from SP050006C00 to SP050006B00
1117:----------
Page 58 Add HW PIR

B --> C Change List

1209:----------
R679 change BOM structure to @
D13,D15 change BOM structure to @
Change R717,R718,R720,R509 BOM structure from VGA@ to @ (Madison&Park prodution remove JTAG option2)
Change R64 BOM structure from @ to VGA@ (Madison&Park prodution remove JTAG option2)
Add R729 0_0402(SD028000080,@)
Add R730 0_0402(SD028000080,@) LOCAL_DIM for Panel new feature
Add R731 0_0402(SD028000080,@) COLOR_ENG_EN for Panel new feature
Add R732 100K_0402(SD028100380)LOCAL_DIM PD to GND
Add R733 100K_0402(SD028100380)COLOR_ENG_EN PD to GND
Q53 change BOM structure to @
ADD Q54 2N7002DWH_SOT363-6(SB00000AR10) for AC PLUG HDD LED flash issue
DEL U16 for AC PLUG HDD LED flash issue
C97,C134,C136,C251,C541,C268,C675,C667 symbol update from SGA00002U00 to SGA00001Q80
C775,C776,C777,C778 change P/N SE107475M80 to SE107475K80(4.7U_0603_6.3V6K)
R272(100K PU +3VS) change BOM structure to @
Add U32.85 WWAN_LED# (input)
Add U32.17 MINI1_LED# (input)
ADD R734 PD to GND (fix CPT Panel Flash issue)

1211:----------
ADD C807,C808 1000P_0402(SE074102K80) LAN EMI
ADD C610 0.1U_0402 Y5V(SE070104Z80) VGFX_CORE EMI
ADD C809 C810 0.1U_0402 Y5V(SE070104Z80) +1.5V EMI
1211B:----------
Add U32.36 WLAN_LED# (output)
Add U32.91 3G_LED# (output)
Add U32.85 WWAN_LED# (input)
1214:----------
ADD R735 For U24 power source +3VS (POP)
ADD R736 For U24 power source +5VS (@)
1215:----------
ADD R737 asmedia CLK-
ADD R738 asmedia CLK+
U24 PN change to SA00000U500 (74AHC1G125GW_SOT353-5)
1216:----------
C465 change BOM structure to @(3G 150U)
R41 change BOM structure to @(CRT DET)
Q20 change BOM structure to @(CRT DET)
R343,R341 change to 2.2K_0402_5%(SD028220180) (LED)
R334 change to 249K_0402_1%(SD034249380)
1217:----------
R253 2.2K_0402_5% change to @
R252 2.2K_0402_5% change to UMAHD@
R343 change to 2.2K_0402_5%(7080@) 680_0402_5%(90@)
R344 change to 3.9K_0402_5%(7080@) 680_0402_5%(90@)
R341 change to 2.2K_0402_5%(7080@) 680_0402_5%(90@)
R342 change to 3.9K_0402_5%(7080@) 680_0402_5%(90@)
1219:
R382 change to 18K_0402(SD028180280)(Board ID)
R389 ADD 100K_0402_5%(SD028100380) PH +3VALW(Board ID)
1223:
R157 change to R167 10K_0402_5% (GPIO66: L:6L H:8L)
GPIO21 define to Project ID (L:NEW50/70/80/90 H:NEW71/91)

C --> MP Change List

1228:
MB PCB P/N (DA80000H700)change to (DAZ0C900100)
Q5,Q9,Q16,Q19,Q21,Q22,Q26,Q27,Q35,Q40,Q47,Q54 change SB00000AR10 to SB00000D900
DEL D10 (Int. MIC ESD Diode PASS Can remove)
R382 change to 18K_0402_5%(SD028180280 Board ID rev0.3)
DEL R667,R668(SD028000080) USb common mode choke
DEL R167,(SD028100280)(GPIO66 PH 8L,PD 6L) 10K_0402_5%
ADD R157 (SD028100280)(GPIO66 PH 8L,PD 6L) 10K_0402_5%
ADD R389 (SD028100380)(Board ID)100K_0402_5%
ADD L68(SM070001600 12ohm bead) USB common mode choke
Modify U24 Symbol

0104:
ADD R350 100K_0402_5%(SD028100380)(3G PH +3VS_WWAN)
0107:
Q5,Q9,Q16,Q19,Q21,Q22,Q26,Q27,Q35,Q40,Q47,Q54 change SB00000D900 to SB00000DH00

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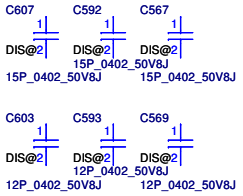
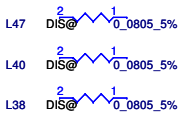
CRT Option Components

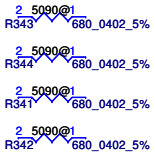


15P_0402_50V8J: SE071150J80
12P_0402_50V8J: SE071120J80

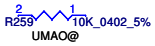


0_0805_5%: SD002000080

NEW90 LED Option



PCH SKU Option



GPIO19

VGA

U34
PARK@
216-0774007 A11 PARK XT M2

PARK XT M2 A11: SA00003MC10

PCB

ZZZ
LA-5891P REV1 M/B

LA-5891P MB Rev0: DA80000H700
LA-5891P MB Rev1: DA80000H710
LA-5891P MB with Small Board Rev1: DAZ0C900100

X76

ZZZ
X761@
X76198BOL01

X76198BOL01 VRAM 512M SAM NEW70
Samsung : SA000035700 (S IC D3 64MX16 K4W1G1646E-HC12 FBGA 96P)

ZZZ
X762@
X76198BOL02

X76198BOL02 VRAM 512M HYN NEW70
Hynix : SA000032400 (S IC D3 64MX16 H5TQ1G63BFR-12C FBGA 1.5V)

ZZZ
X763@
X76198BOL03

X76198BOL03 VRAM 1G SAM NEW70
Samsung : SA000035700 (S IC D3 64MX16 K4W1G1646E-HC12 FBGA 96P)

ZZZ
X764@
X76198BOL04

X76198BOL04 VRAM 1G HYN NEW70
Hynix : SA000032400 (S IC D3 64MX16 H5TQ1G63BFR-12C FBGA 1.5V)

ZZZ
X765@
X76198BOL05

X76198BOL05 VRAM 512M AMD NEW70
AMD :SA00003PF10
(S IC D3 64M16/800 23EY2387MB-12 PG-TFBGA 96P 1.5V)

ZZZ
X766@
X76198BOL06

X76198BOL06 VRAM 1G AMD NEW70
AMD :SA00003PF10
(S IC D3 64M16/800 23EY2387MB-12 PG-TFBGA 96P 1.5V)

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