

Compal confidential

Schematics Document

Mobile Merom uFCPGA with Satna Rosa Platform

2007-08-02

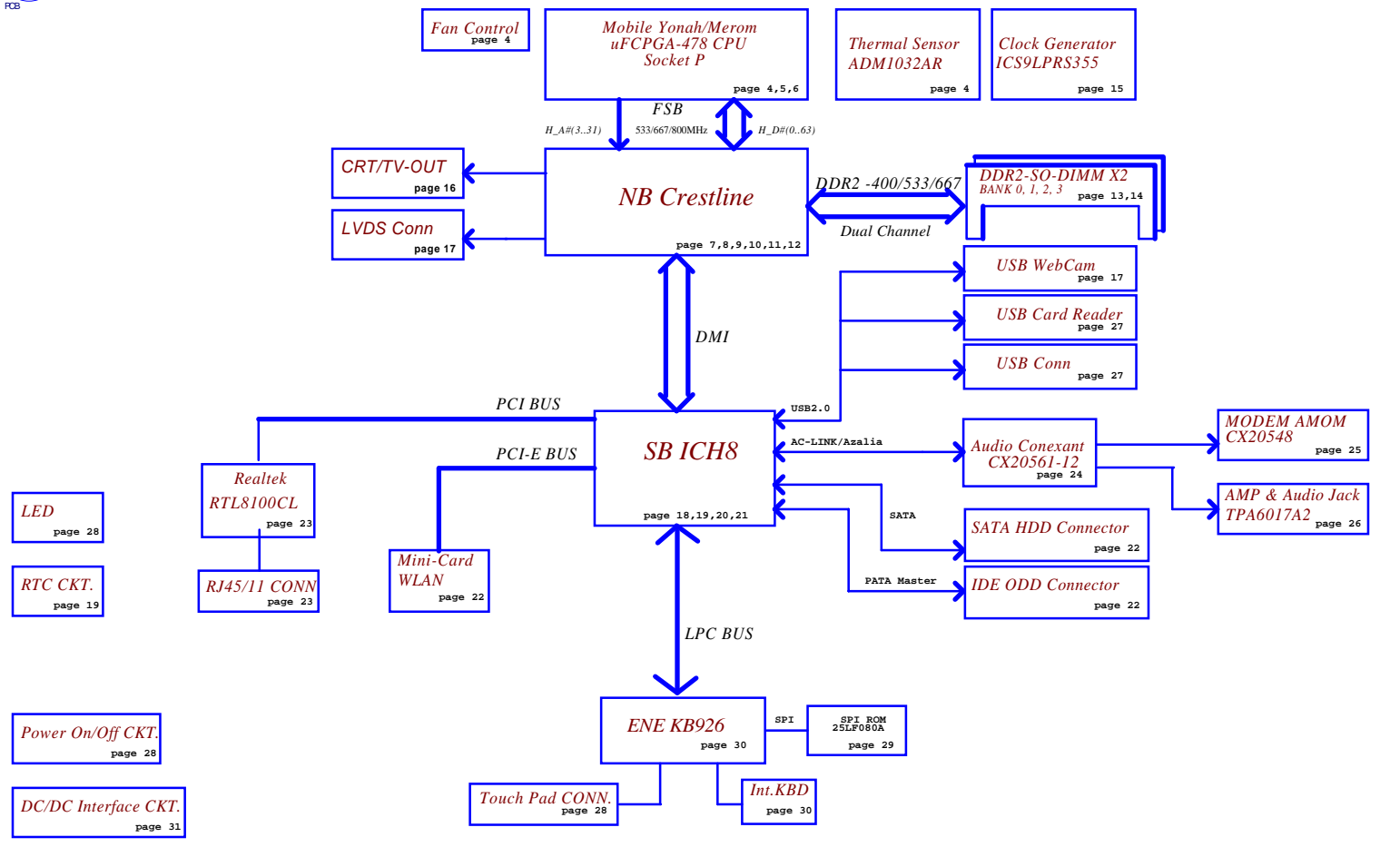
REV: 0.2

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Issued Date	2007/03/26	Deciphered Date	2006/07/26	Cover Sheet		
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LEON 1.0 (Merom +Crestline+ICH8)



PCB



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Block Diagram

Voltage Rails

power plane State	+B	+5VALW +3VALW	+1.8V	+5VS +3VS +1.5VS +1.25VS +0.9V +VCCP +CPU_CORE
s0	O	O	O	O
s1	O	O	O	O
s3	O	O	O	X
s5 s4/AC	O	O	X	X
s5 s4/ Battery only	O	X	X	X
s5 s4/AC & Battery don't exist	X	X	X	X

Symbol Note :

 : means Digital Ground

 : means Analog Ground

@ : means just reserve , no build

DEBUG@ : means just reserve for debug.

External PCI Devices

DEVICE	IDSEL #	REQ/GNT #	PIRQ
LAN	AD22	0	A

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	10100000
DDR SO-DIMM 1	A4	10100100
CLOCK GENERATOR (EXT.)	D2	11010010

SMBUS Control Table

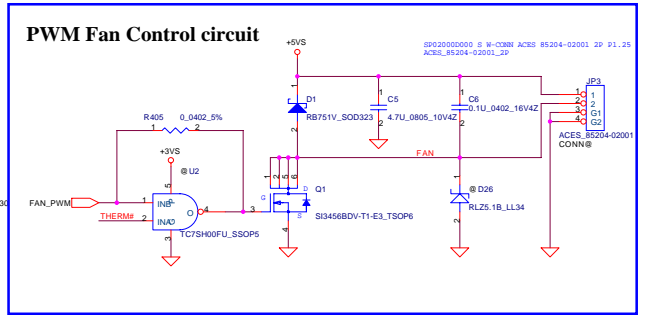
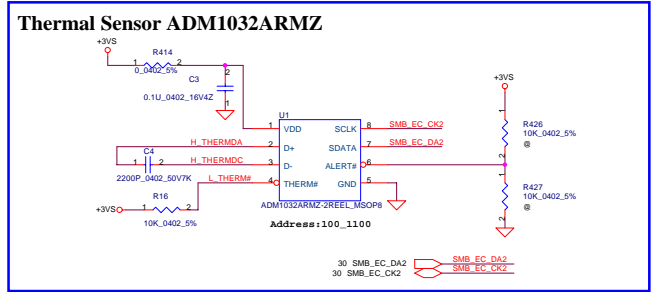
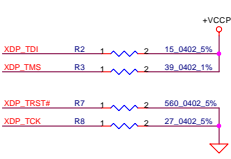
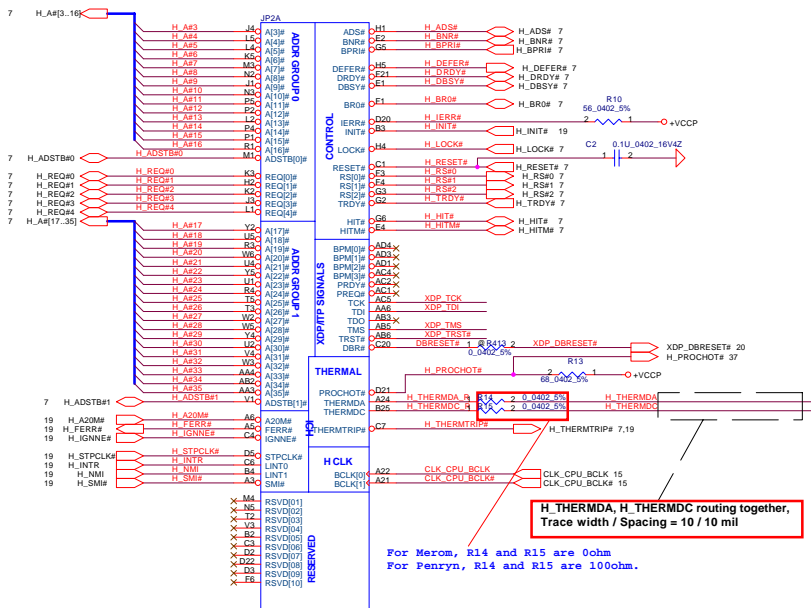
	SOURCE	INVERTER	BATT	SERIAL EEPROM	THERMAL SENSOR (CPU) ADML022	SODIMM	CLK CHIP	MINI CARD	LCD
SMB_EC_CK1 SMB_EC_DA1	KB925	X	V	V	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB925	X	X	X	V	X	X	X	X
SMB_CK_CLK1 SMB_CR_DAT1	ICH8	X	X	X	X	V	V	V	X
LCD_CLK LCD_DAT	Crestline	X	X	X	X	X	X	X	V

BOM: 43151732L01(965GM) & 443151732L02(960GML) with card reader

BOM: 43151732L03(965GM) & 43151732L04(960GML) without card reader

Jump-Short: PJP?

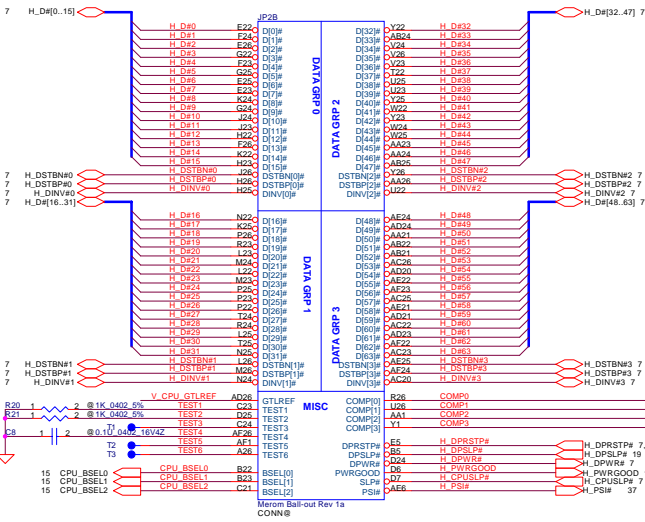
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H_THERMDA, H_THERMDC routing together,
Trace width / Spacing = 10 / 10 mil

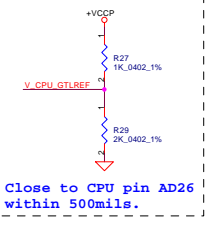
For Merom, R14 and R15 are 0ohm
For Penryn, R14 and R15 are 100ohm.

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2007/03/26	Deciphered Date	2006/03/10	Title	Merom(13)-AGTL+XDP
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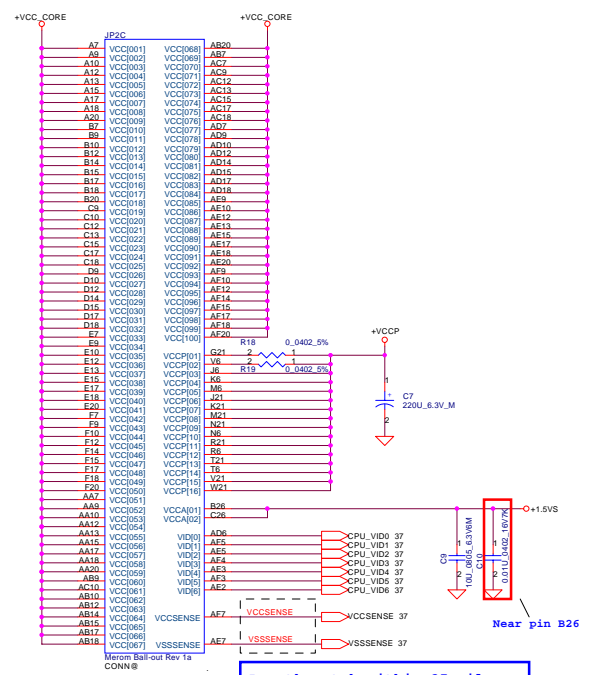


layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

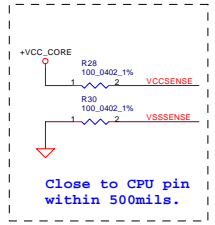
CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0



Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP[0, 2] trace width is 18 mils. COMP[1,3] trace width is 4 mils.

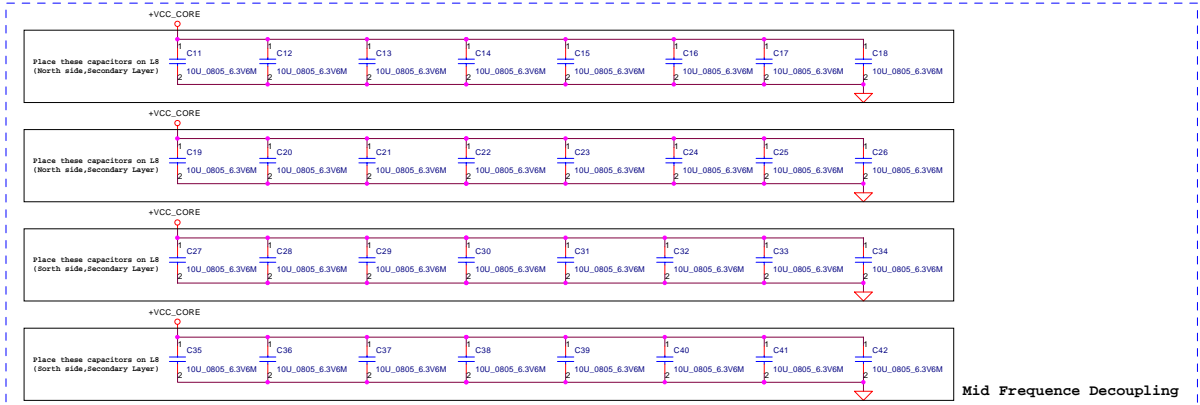


Length match within 25 mils. The trace width/space/other is 20/7/25.



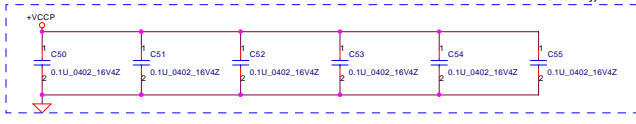
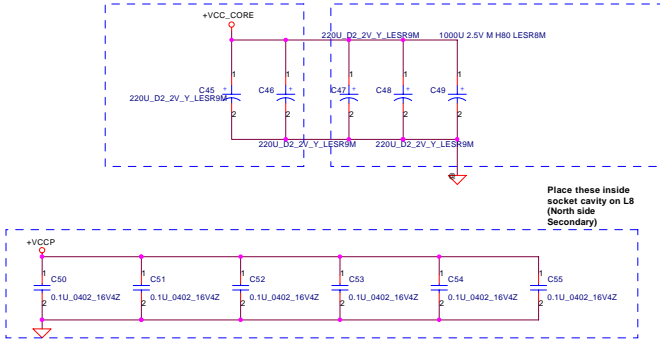
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JP2D			
A4	VSS1001	VSS1080	P6
A5	VSS1002	VSS1083	P21
A6	VSS1003	VSS1084	P22
A11	VSS1004	VSS1085	B2
A14	VSS1005	VSS1086	B22
A16	VSS1006	VSS1087	B22
A19	VSS1007	VSS1088	T1
A22	VSS1008	VSS1089	T1
AF2	VSS1009	VSS1090	T4
B6	VSS1010	VSS1091	T7
B11	VSS1011	VSS1092	T26
B13	VSS1012	VSS1093	T17
B16	VSS1013	VSS1094	U6
B19	VSS1014	VSS1095	U2
B21	VSS1015	VSS1096	U24
C2	VSS1016	VSS1097	U5
C4	VSS1017	VSS1098	U2
C8	VSS1018	VSS1099	U22
C11	VSS1019	VSS1100	U25
C14	VSS1020	VSS1101	W1
C16	VSS1021	VSS1102	W4
C19	VSS1022	VSS1103	W22
C2	VSS1023	VSS1104	W2
C22	VSS1024	VSS1105	X3
C25	VSS1025	VSS1106	X6
D1	VSS1026	VSS1107	X2
D4	VSS1027	VSS1108	X24
D8	VSS1028	VSS1109	Y2
D11	VSS1029	VSS1110	Y24
D13	VSS1030	VSS1111	AA8
D16	VSS1031	VSS1112	AA11
D19	VSS1032	VSS1113	AA14
D23	VSS1033	VSS1114	AA16
D26	VSS1034	VSS1115	AA19
E3	VSS1035	VSS1116	AA22
E6	VSS1036	VSS1117	AA25
E8	VSS1037	VSS1118	AB1
E11	VSS1038	VSS1119	AB4
E14	VSS1039	VSS1120	AB7
E16	VSS1040	VSS1121	AB11
E19	VSS1041	VSS1122	AB13
E21	VSS1042	VSS1123	AB16
E24	VSS1043	VSS1124	AB19
F4	VSS1044	VSS1125	AB23
F8	VSS1045	VSS1126	AB26
F11	VSS1046	VSS1127	AC2
F16	VSS1047	VSS1128	AC6
F19	VSS1048	VSS1129	AC11
F22	VSS1049	VSS1130	AC14
F25	VSS1050	VSS1131	AC16
G2	VSS1051	VSS1132	AC19
G4	VSS1052	VSS1133	AC21
G1	VSS1053	VSS1134	AC24
G3	VSS1054	VSS1135	AD2
G8	VSS1055	VSS1136	AD5
H4	VSS1056	VSS1137	AD8
H6	VSS1057	VSS1138	AD11
H21	VSS1058	VSS1139	AD13
H24	VSS1059	VSS1140	AD16
J2	VSS1060	VSS1141	AD19
J6	VSS1061	VSS1142	AD22
J22	VSS1062	VSS1143	AD25
K5	VSS1063	VSS1144	AE1
K1	VSS1064	VSS1145	AE4
K4	VSS1065	VSS1146	AE7
K8	VSS1066	VSS1147	AE8
K23	VSS1067	VSS1148	AE11
K26	VSS1068	VSS1149	AE14
L3	VSS1069	VSS1150	AE16
L6	VSS1070	VSS1151	AE19
L21	VSS1071	VSS1152	AE23
L24	VSS1072	VSS1153	AE26
M2	VSS1073	VSS1154	AF2
M5	VSS1074	VSS1155	AF5
M22	VSS1075	VSS1156	AF8
M26	VSS1076	VSS1157	AF11
N1	VSS1077	VSS1158	AF13
N4	VSS1078	VSS1159	AF16
N23	VSS1079	VSS1160	AF19
N26	VSS1080	VSS1161	AF21
P1	VSS1081	VSS1162	AZ2
		VSS1163	AZ5

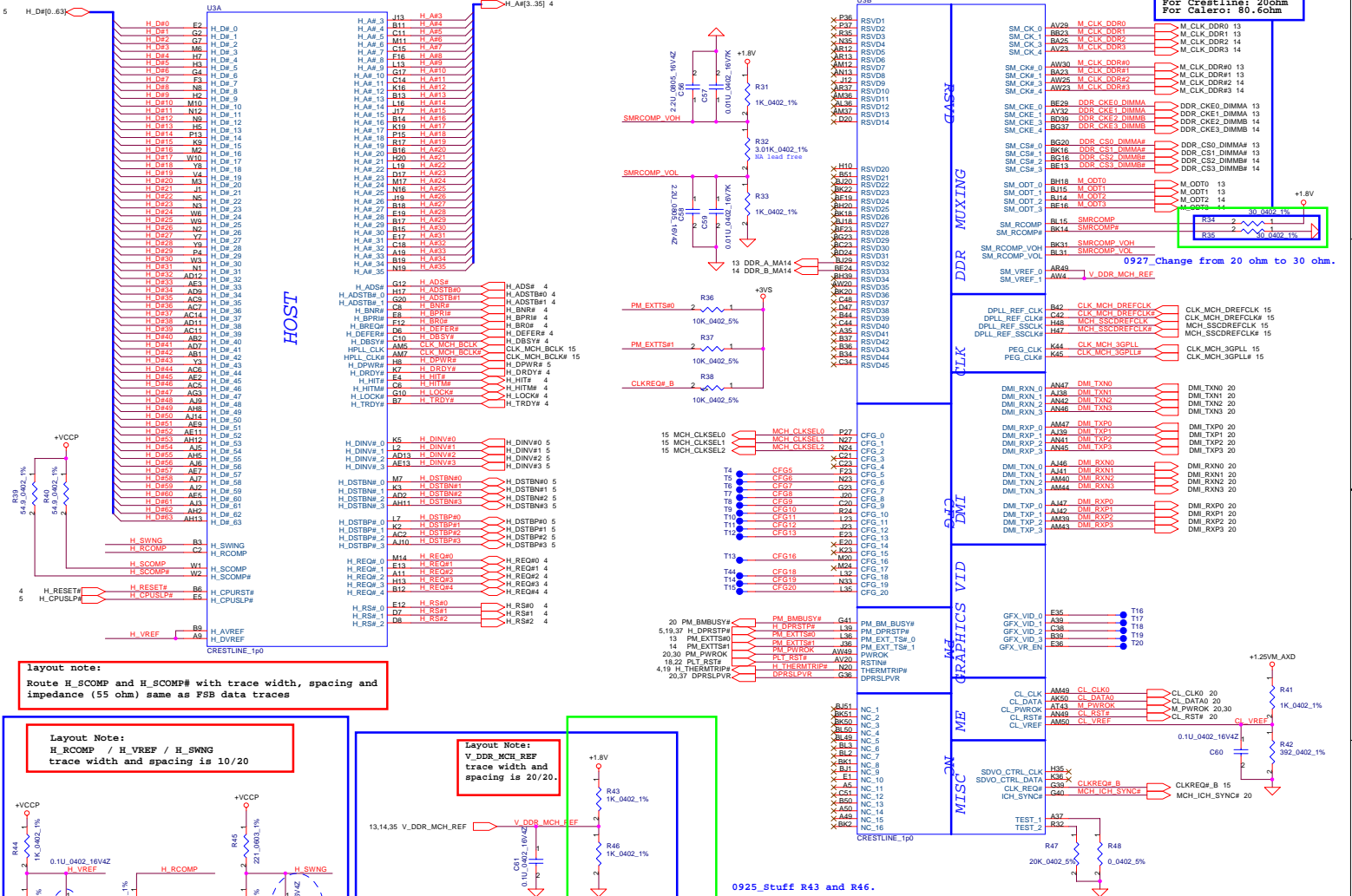


Mid Frequency Decoupling

Near CPU CORE regulator ESR <= 1.5m ohm Capacitor > 1980uF



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For Crestline: 20ohm
For Calero: 80, 60ohm

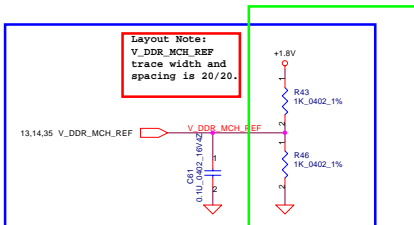
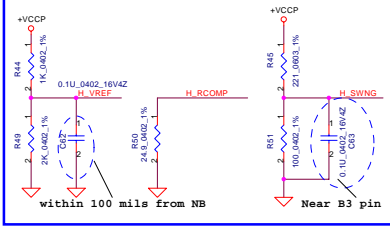
0927_Change from 20 ohm to 30 ohm.

layout note:
Route H_SCOMP and H_SCOMP# with trace width, spacing and impedance (55 ohm) same as #8 data traces

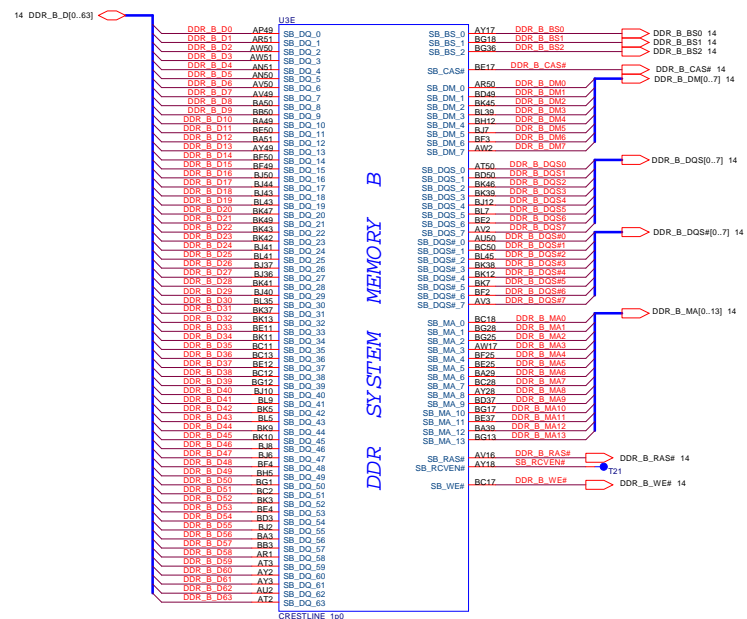
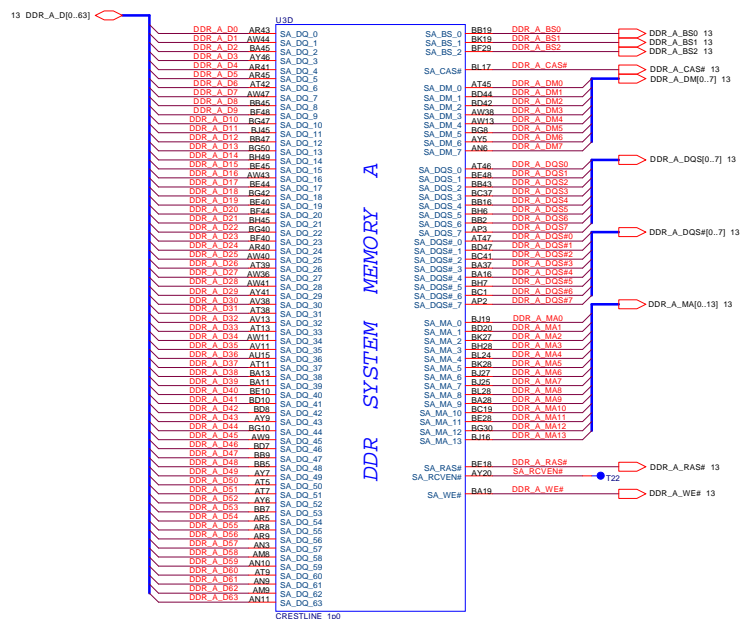
Layout Note:
H_RCMP / H_VREF / H_SWNG trace width and spacing is 10/20

Layout Note:
V_DDR_MCH_REF trace width and spacing is 20/20.

0925_Stuff R43 and R46.



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CRESTLINE_1p0

CRESTLINE_1p0

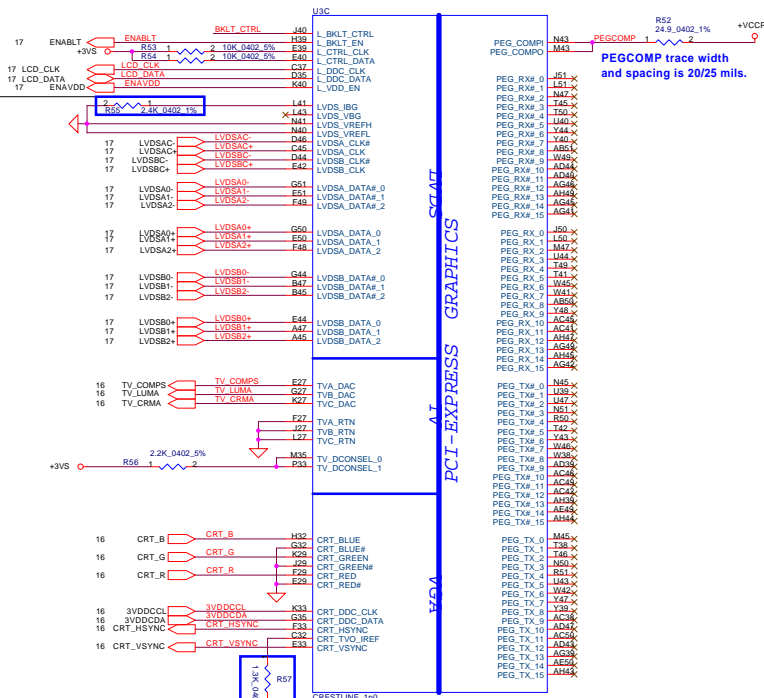
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Strap Pin Table

CFG[2:0] FSB Freq select	010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	Reserved
CFG7 (CPU Strap)	0 = Reserved 1 = Mobile CPU *
CFG8 (Low power PCIe)	0 = Normal mode 1 = Low Power mode *
CFG9 (PCIe Graphics Lane Reversal)	0 = Reverse Lane 1 = Normal Operation *
CFG[11:10]	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation(Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
SDVO_CTRLDATA	0 = No SDVO Device Present * 1 = SDVO Device Present
CFG19 (DMI Lane Reversal)	0 = Normal Operation (Lane number in Order) * 1 = Reverse Lane
CFG20 (PCIe/SDVO concurrent)	0 = Only PCIe or SDVO is operational. * 1 = PCIe/SDVO are operating simu.

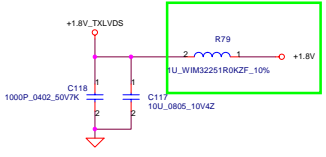
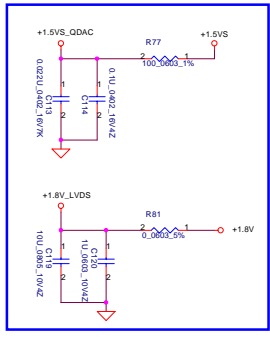
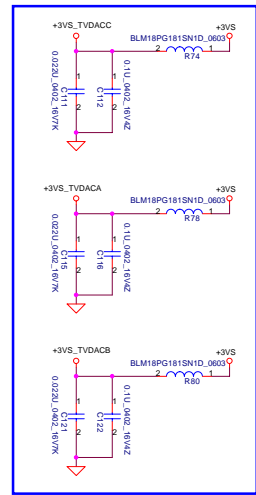
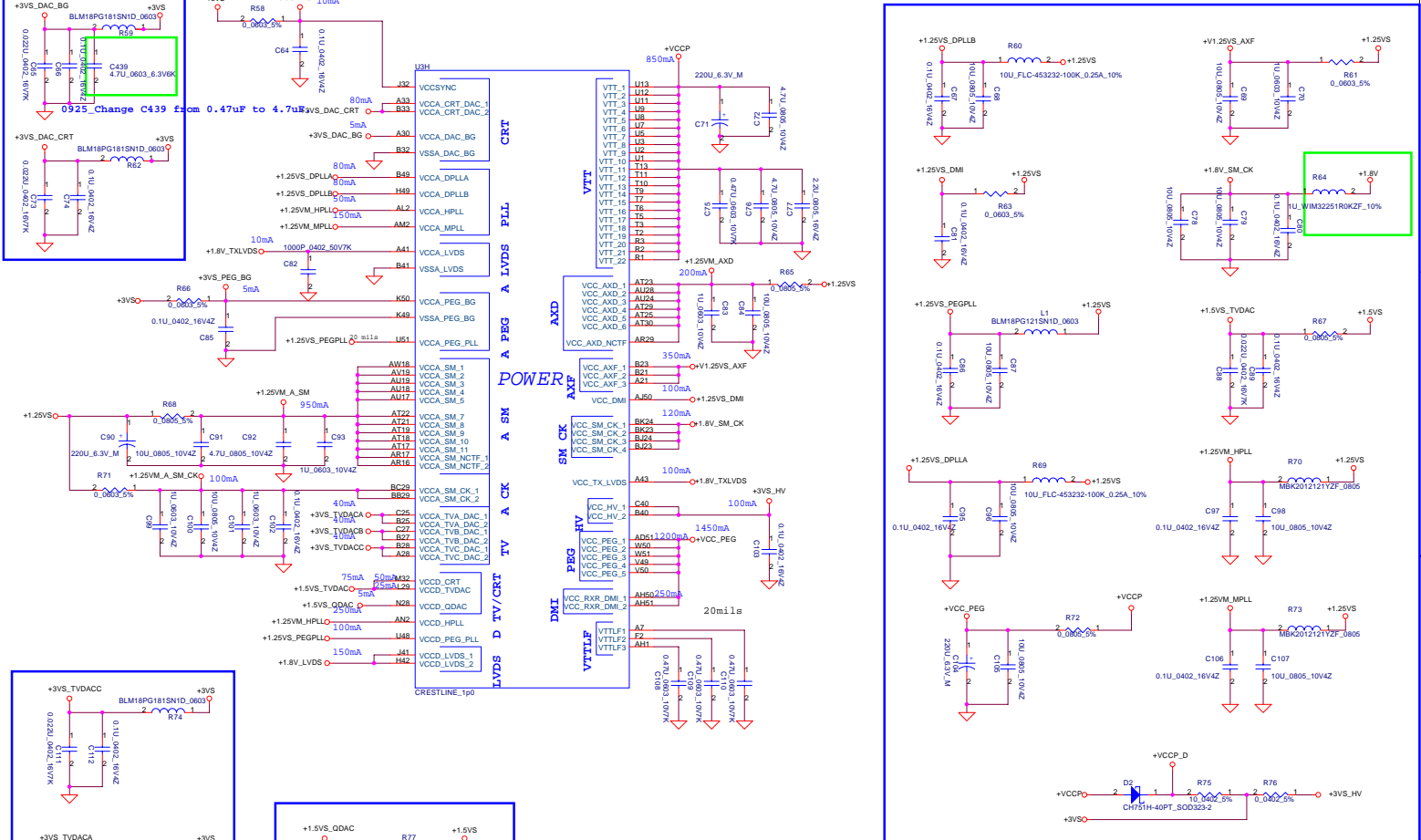
CFG[17:3] have internal pull up
CFG[19:18] have internal pull down

For Crestline: 2.4kohm
For Calero: 1.5kohm



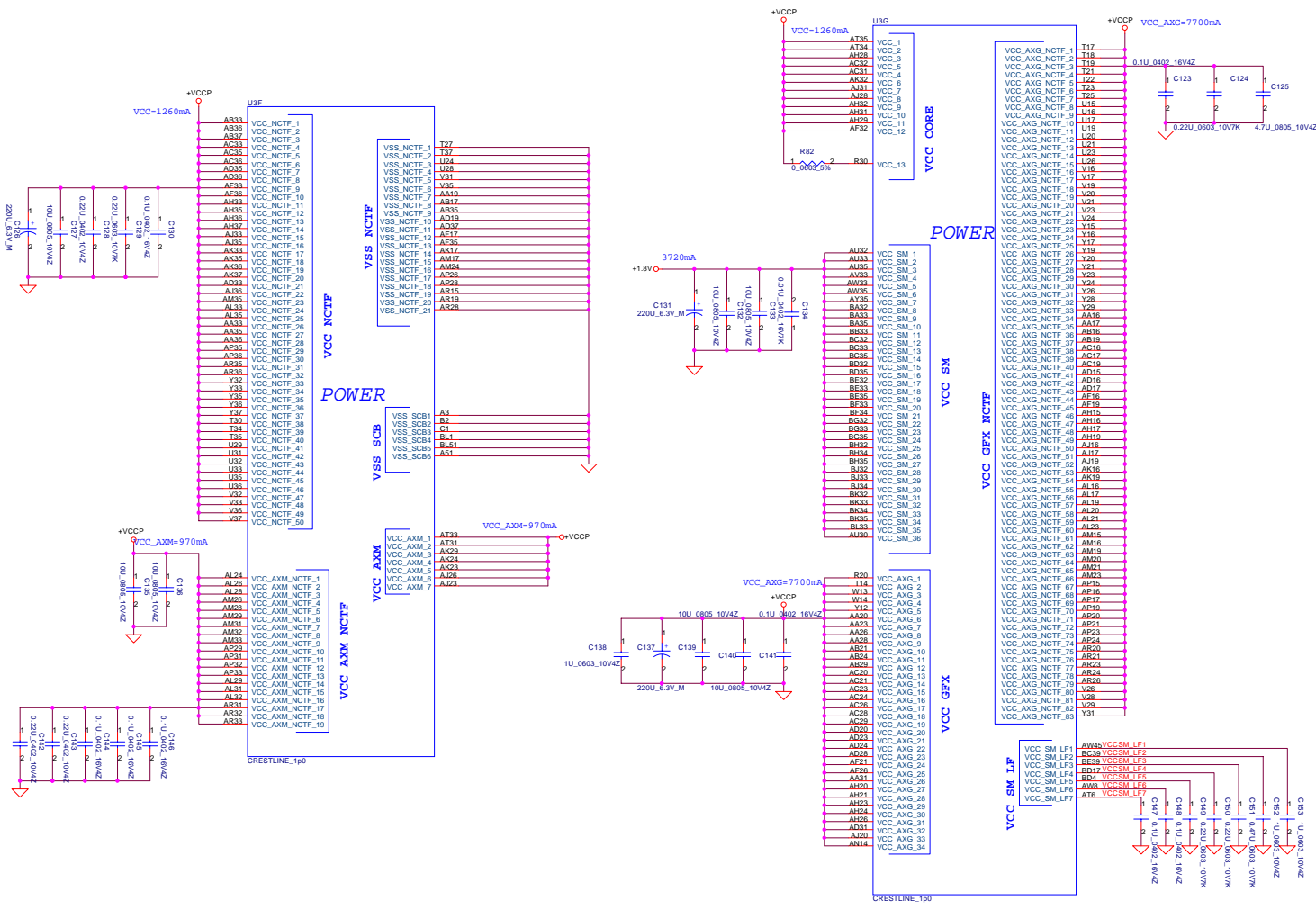
For Crestline: 1.3kohm
For Calero: 255ohm

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1022_Change R64, R79 from 0 ohm to 1uH/400mA inductor.

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Compal Electronics, Inc.
CRESTLINE((5/6)-PWR/GND

Rev 0.3

U31			
A13	VSS_1	AW24	
A15	VSS_2	AW23	
A17	VSS_3	AW22	
A2	VSS_4	AW21	
AA21	VSS_5	AW20	
AA24	VSS_6	AW19	
AA25	VSS_7	AW18	
AB20	VSS_8	AW17	
AB23	VSS_9	AW16	
AB26	VSS_10	AW15	
AB28	VSS_11	AW14	
AB31	VSS_12	AW13	
AC10	VSS_13	AW12	
AC13	VSS_14	AW11	
AC1	VSS_15	AW10	
AC2	VSS_16	AW9	
AC43	VSS_17	AW8	
AD1	VSS_18	AW7	
AD21	VSS_19	AW6	
AD26	VSS_20	AW5	
AD29	VSS_21	AW4	
AD3	VSS_22	AW3	
AD41	VSS_23	AW2	
AD49	VSS_24	AW1	
AD5	VSS_25		
AD5	VSS_26		
AD50	VSS_27		
AE10	VSS_28		
AE14	VSS_29		
AE1	VSS_30		
AE1	VSS_31		
AE1	VSS_32		
AF23	VSS_33		
AF24	VSS_34		
AF24	VSS_35		
AF31	VSS_36		
AG2	VSS_37		
AG38	VSS_38		
AG43	VSS_39		
AG47	VSS_40		
AH3	VSS_41		
AH3	VSS_42		
AH3	VSS_43		
AH41	VSS_44		
AH7	VSS_45		
AI3	VSS_46		
AJ11	VSS_47		
AJ24	VSS_48		
AJ21	VSS_49		
AJ24	VSS_50		
AJ29	VSS_51		
AJ32	VSS_52		
AJ43	VSS_53		
AJ45	VSS_54		
AJ45	VSS_55		
AK20	VSS_56		
AK21	VSS_57		
AK28	VSS_58		
AK28	VSS_59		
AK31	VSS_60		
AK51	VSS_61		
AL1	VSS_62		
AM11	VSS_63		
AM13	VSS_64		
AM3	VSS_65		
AM4	VSS_66		
AM41	VSS_67		
AN3	VSS_68		
AN3	VSS_69		
AN38	VSS_70		
AN38	VSS_71		
AN43	VSS_72		
AN7	VSS_73		
AN7	VSS_74		
AP48	VSS_75		
AP48	VSS_76		
AP50	VSS_77		
AR1	VSS_78		
AR2	VSS_79		
AR2	VSS_80		
AR44	VSS_81		
AR7	VSS_82		
AR7	VSS_83		
AT10	VSS_84		
AT14	VSS_85		
AT41	VSS_86		
AT6	VSS_87		
AU1	VSS_88		
AU23	VSS_89		
AU2	VSS_90		
AU3	VSS_91		
AU36	VSS_92		
AU49	VSS_93		
AU4	VSS_94		
AV38	VSS_95		
AV48	VSS_96		
AW1	VSS_97		
AW12	VSS_98		
AW16	VSS_99		

VSS

CRESTLINE_1p0

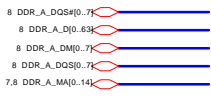
J31			
C46	VSS_199	W11	
C50	VSS_200	W39	
C7	VSS_201	W43	
D13	VSS_202	W47	
D24	VSS_203	W5	
D3	VSS_204	W7	
D32	VSS_205	W13	
D39	VSS_206	W2	
D45	VSS_207	W41	
D49	VSS_208	W46	
E10	VSS_209	W49	
E14	VSS_210	W50	
E24	VSS_211	W50	
E28	VSS_212	W50	
E47	VSS_213	W50	
F19	VSS_214	W50	
F36	VSS_215	W50	
F4	VSS_216	W50	
F40	VSS_217	W50	
F50	VSS_218	W50	
G1	VSS_219	W50	
G13	VSS_220	W50	
G16	VSS_221	W50	
G19	VSS_222	W50	
G24	VSS_223	W50	
G28	VSS_224	W50	
G30	VSS_225	W50	
G42	VSS_226	W50	
G46	VSS_227	W50	
G48	VSS_228	W50	
G4	VSS_229	W50	
H24	VSS_230	W50	
H24	VSS_231	W50	
H28	VSS_232	W50	
H4	VSS_233	W50	
H4	VSS_234	W50	
H45	VSS_235	W50	
J11	VSS_236	W50	
J16	VSS_237	W50	
J2	VSS_238	W50	
J24	VSS_239	W50	
J33	VSS_240	W50	
J36	VSS_241	W50	
J39	VSS_242	W50	
J43	VSS_243	W50	
K12	VSS_245	W50	
K47	VSS_246	W50	
L1	VSS_247	W50	
L17	VSS_248	W50	
L20	VSS_249	W50	
L24	VSS_250	W50	
L28	VSS_251	W50	
L3	VSS_252	W50	
L33	VSS_253	W50	
L48	VSS_254	W50	
M08	VSS_255	W50	
M2	VSS_256	W50	
M42	VSS_257	W50	
M48	VSS_258	W50	
M49	VSS_259	W50	
M5	VSS_260	W50	
M50	VSS_261	W50	
M9	VSS_262	W50	
N14	VSS_263	W50	
N17	VSS_264	W50	
N26	VSS_265	W50	
N32	VSS_266	W50	
N33	VSS_267	W50	
N39	VSS_268	W50	
N44	VSS_269	W50	
N49	VSS_270	W50	
N7	VSS_271	W50	
P13	VSS_272	W50	
P2	VSS_273	W50	
P23	VSS_274	W50	
P3	VSS_275	W50	
P30	VSS_276	W50	
P49	VSS_277	W50	
P59	VSS_278	W50	
P59	VSS_279	W50	
P67	VSS_280	W50	
P7	VSS_281	W50	
P72	VSS_282	W50	
P85	VSS_283	W50	
P90	VSS_284	W50	
V2	VSS_285	W50	
V3	VSS_286	W50	

VSS

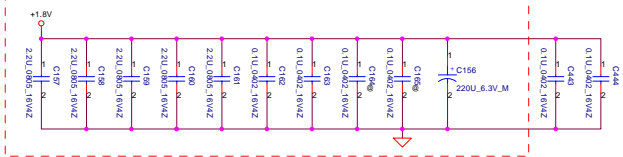
CRESTLINE_1p0

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Issued Date	2007/03/26	Deciphered Date	2006/03/10	Customer
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Date: Monday, October 22, 2007				Sheet 12 of 42

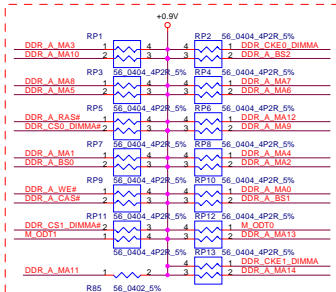
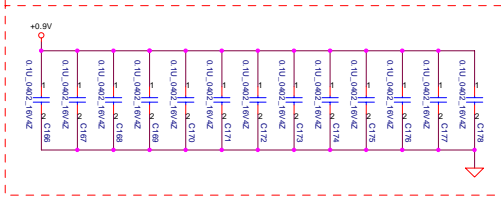
Compal Electronics, Inc.
CRESTLINE((6/6)-PWR/GND
 LA-3901P
 Rev 0.3



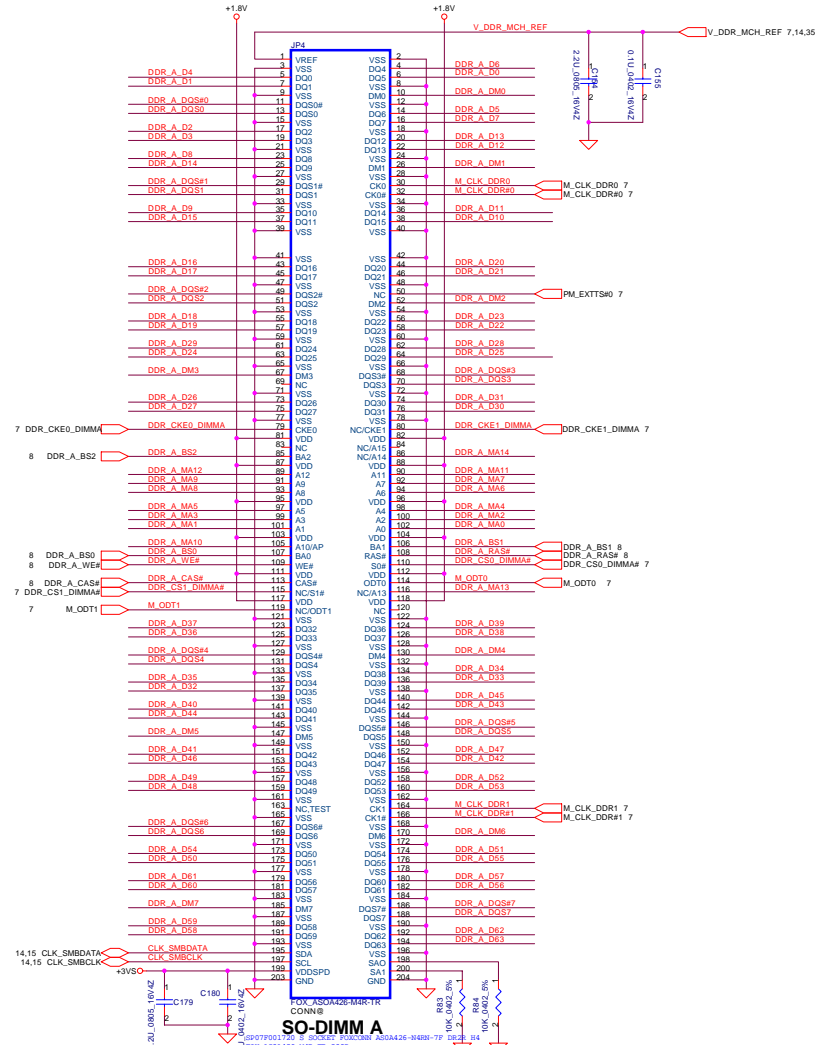
Layout Note:
Place near JP34



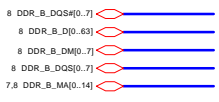
Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS



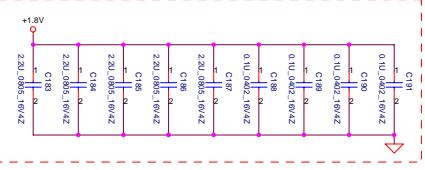
Layout Note:
Place these resistor closely JP34, all trace length Max=1.5"



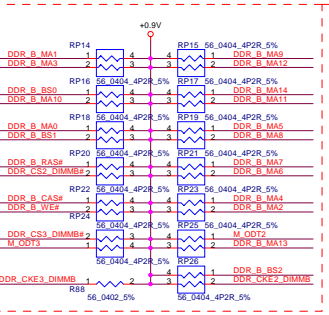
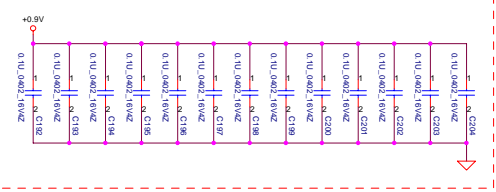
Security Classification				Compal Secret Data		Title	
Issued Date	2007/03/26	Deciphered Date	2006/03/10	DDR1-SODIMM SLOT			
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Size	Document Number	Rev					
Customer	LA-3901P	0.3					
Date	Monday, October 22, 2007	Sheet	13	of	42		



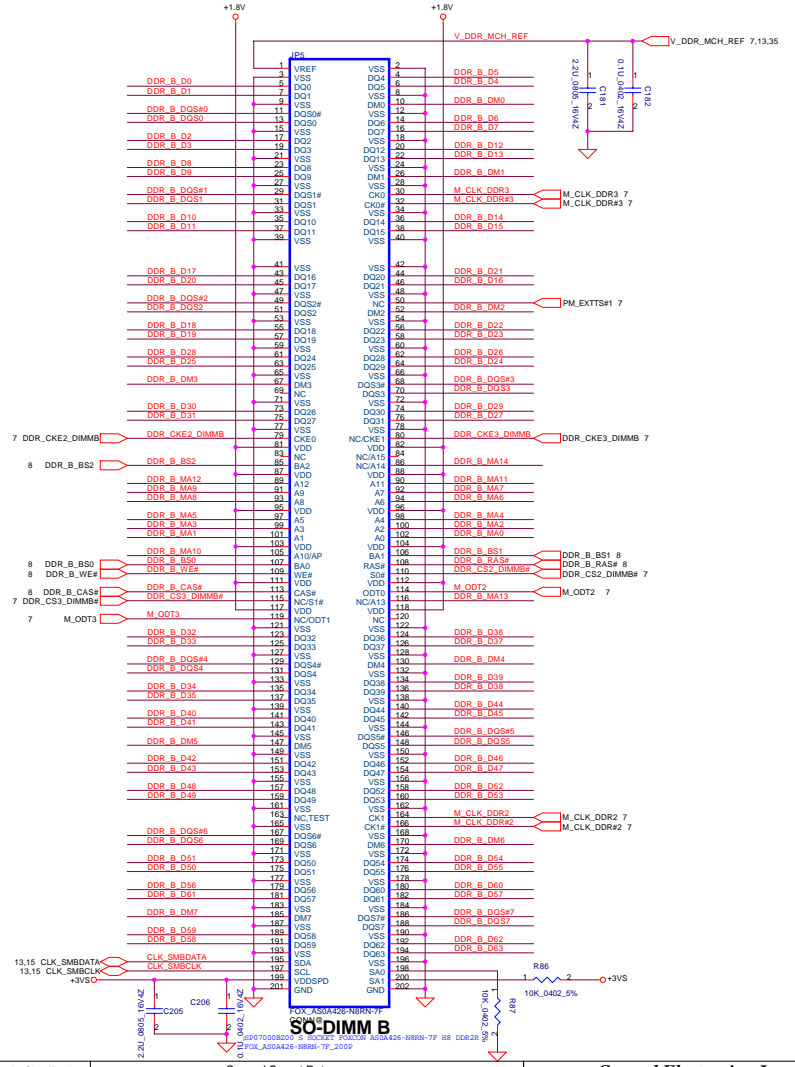
Layout Note:
Place near JP10



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V



Layout Note:
Place these resistor closely JP10, all trace length Max=1.5"



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Size	Document Number	Rev	0.3
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Compal Electronics, Inc.
DDR3-SODIMM SLOT2

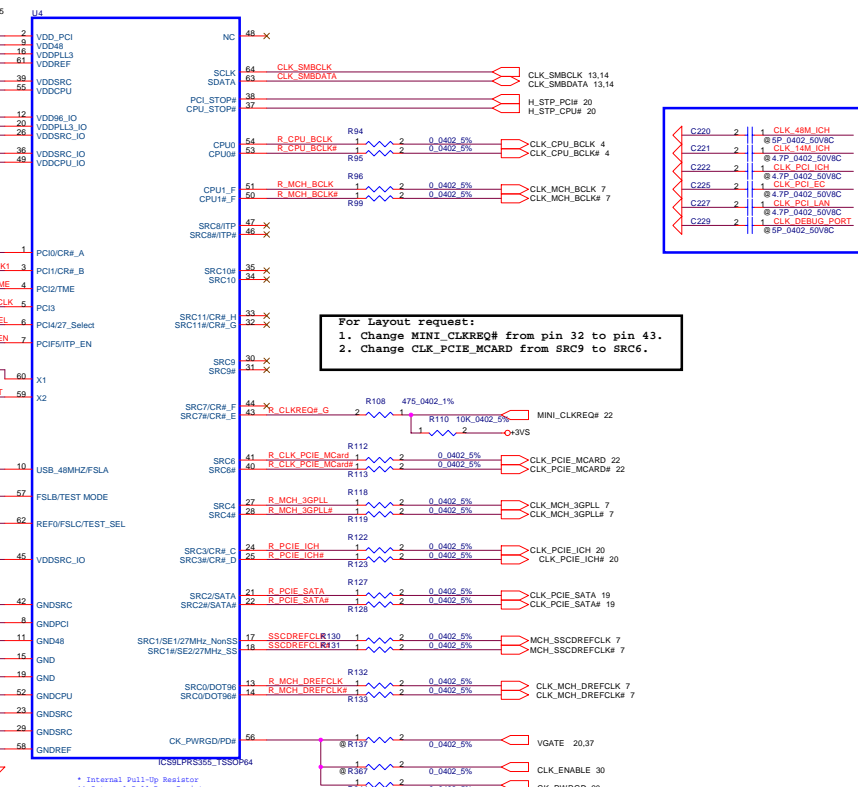
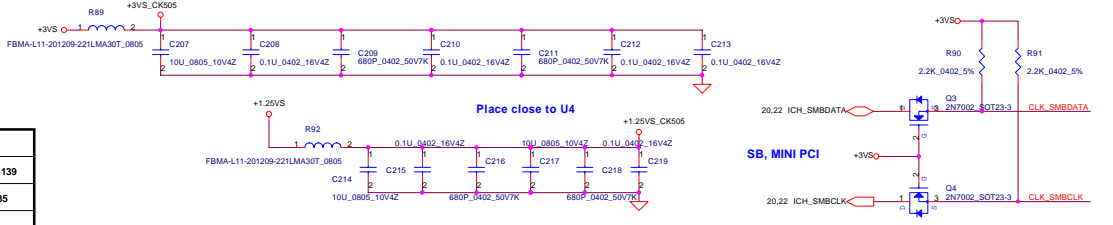
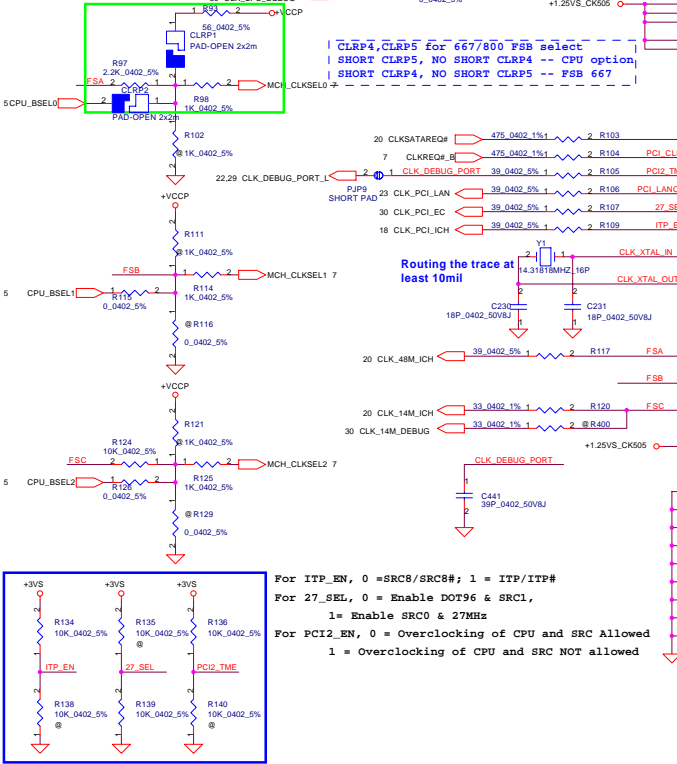
LA-3981P

FSLC CLKSEL2	FSLB CLKSEL1	FSLA CLKSEL0	CPU MHz	SRC MHz	PCI MHz
0	0	1	133	100	33.3
0	1	0	200	100	33.3
0	1	1	166	100	33.3

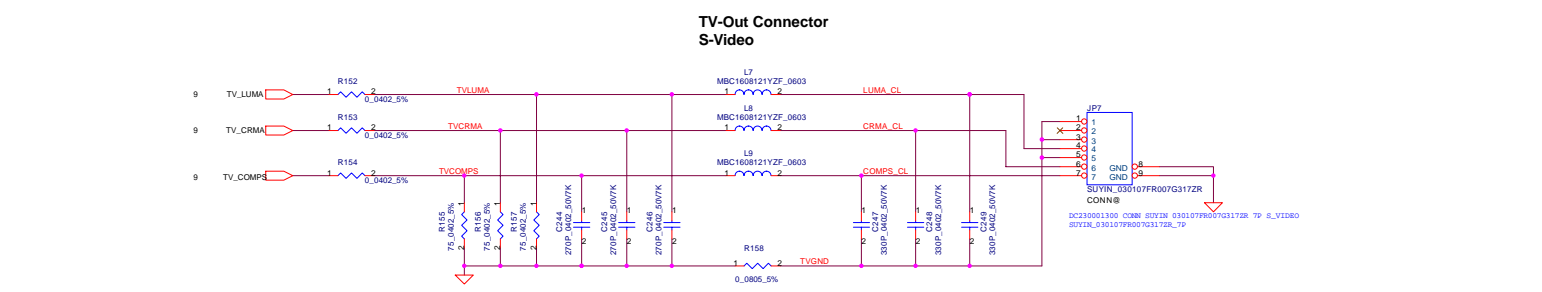
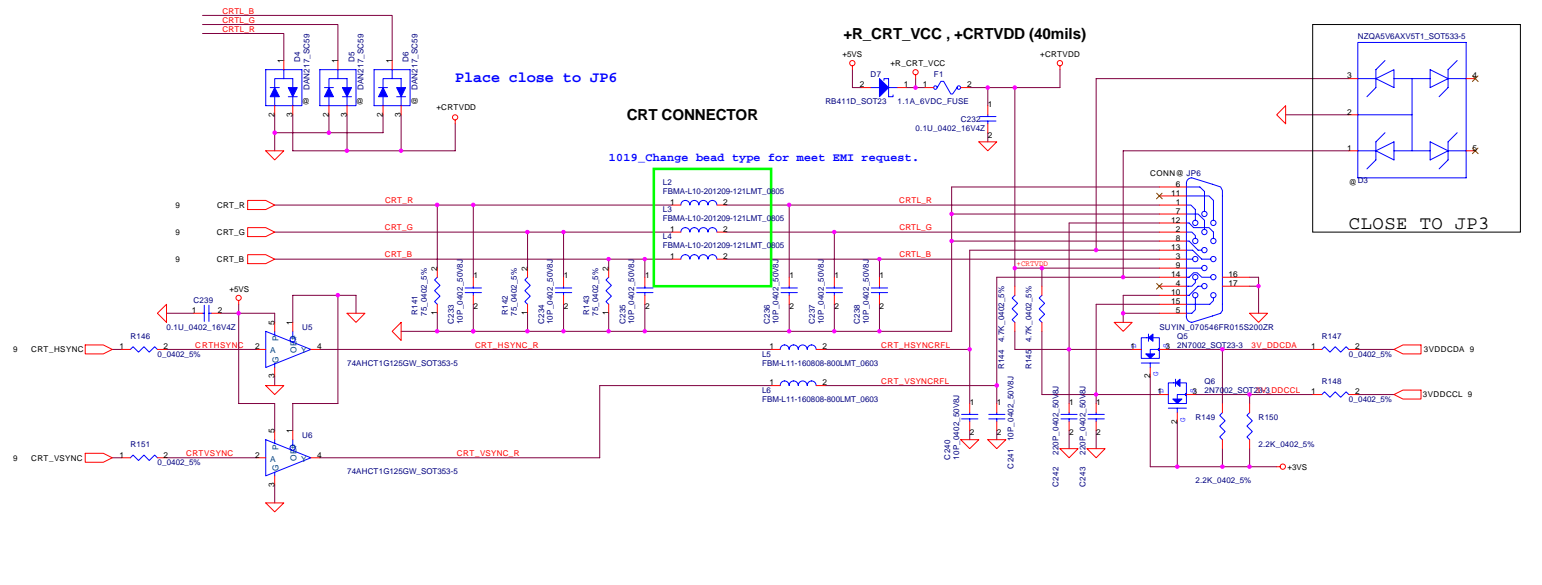
FSB Frequency Select:

CPU Driven	Stuff	R107	R113	R1083
*(Default)	No Stuff	R1074	R1066	R1098 R1113 R1128 R1139
	Stuff	R1086	R1139	R1135 R1074 R1139 R1135
667MHz	No Stuff	R1083	R1107	R1128 R1113 R1098
	Stuff	R1135	R1139	
800MHz	No Stuff	R1083	R1086	R1098 R1128 R1074 R1107 R1113

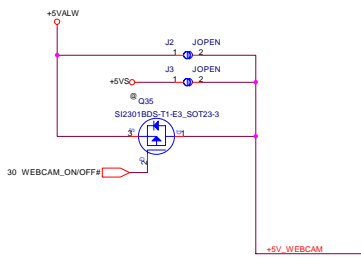
1019_Change CLR1 and CLR2 type like the same as PJP4.



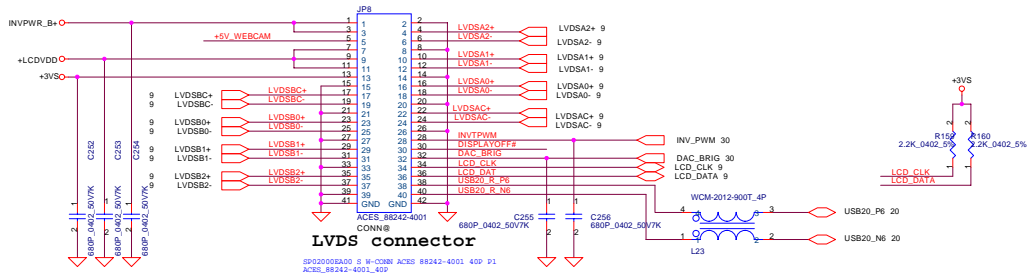
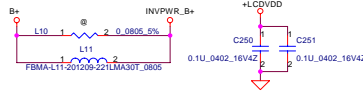
Security Classification	Compal Secret Data	Issued Date	Deciphered Date	2007/03/26	2006/03/10	Title
						Compal Electronics, Inc.
						Clock generator
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						Document Number
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						Date
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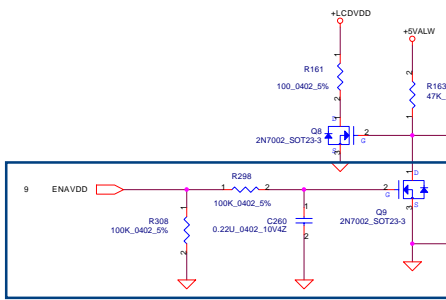
Security Classification	Compal Secret Data		
Issued Date	2007/03/26	Deciphered Date	2006/07/26
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Compal Electronics, Inc. CRT & TVout Connector			Title CRT & TVout Connector
Size Document Number LA-3981P			Rev 0.3
Date: Monday, October 22, 2007			Sheet 16 of 42



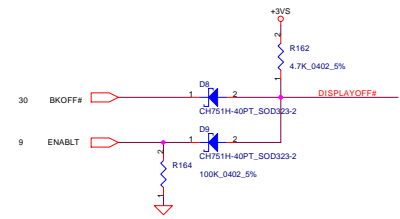
LVDS CONN



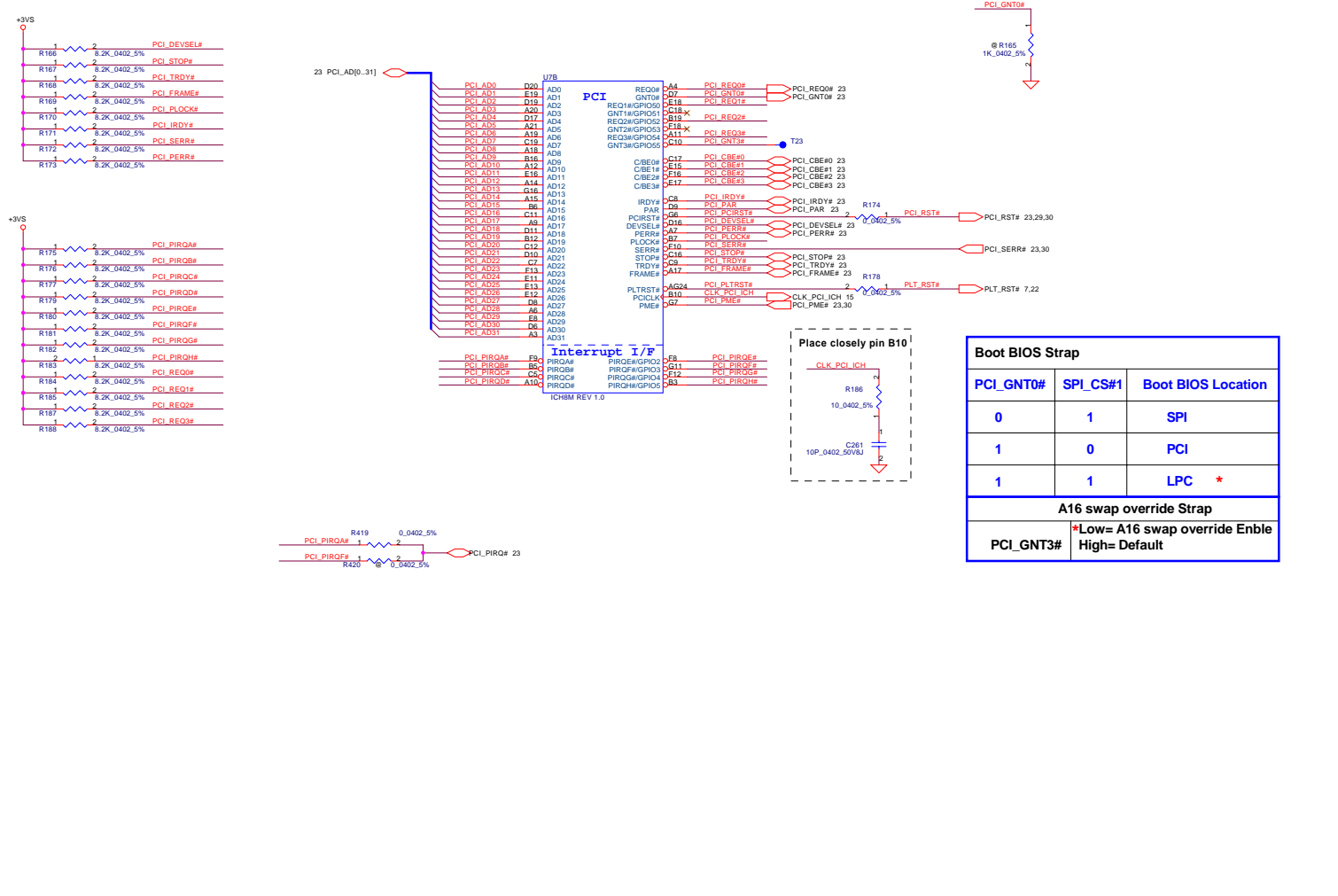
LVDS connector
 ACES_86242-4001
 CONN18
 680P_0402_50V7K C255
 680P_0402_50V7K C256
 WCM-2012-900T_4P
 L23
 USB20_P6 20
 USB20_N6 20



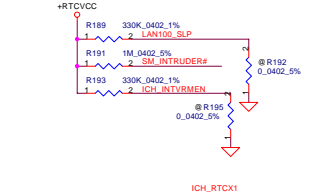
Avoid Panel display garbage after power on.



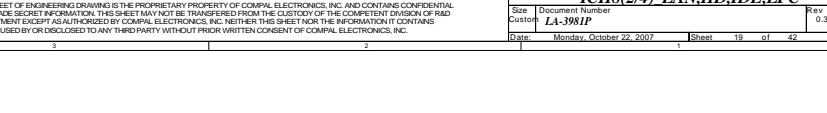
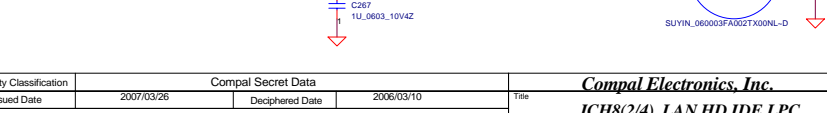
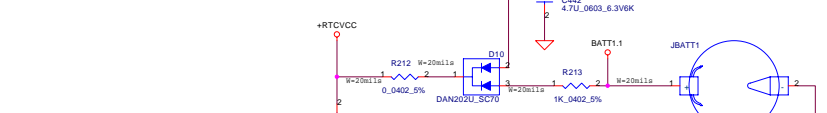
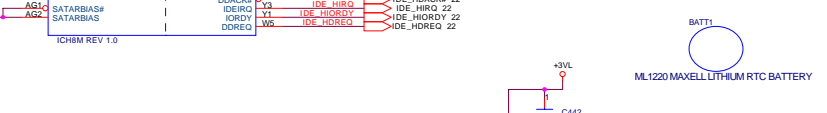
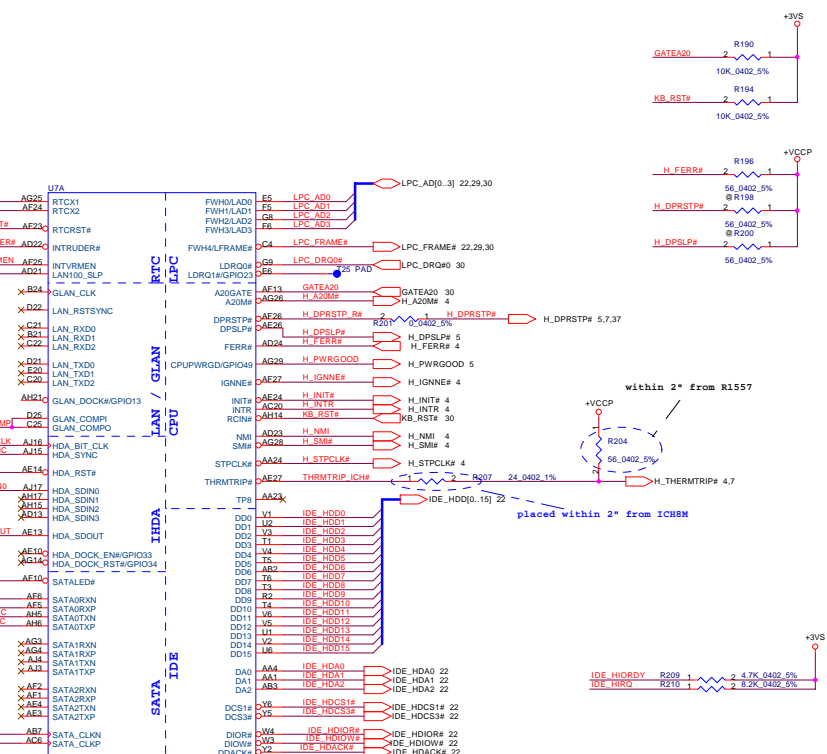
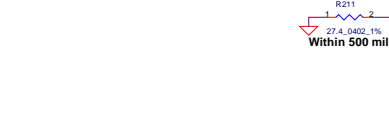
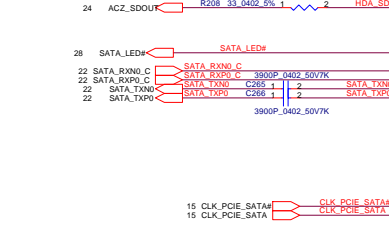
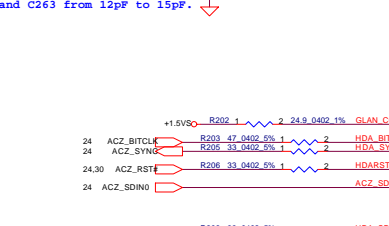
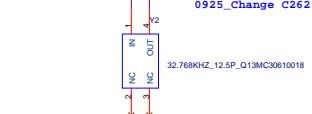
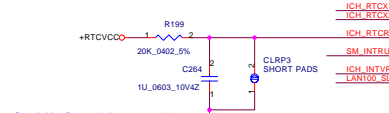
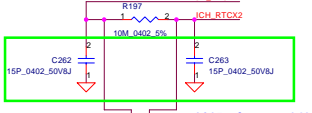
Security Classification		Compal Secret Data		Title	
Issued Date	2007/03/26	Deciphered Date	2006/07/26	LCD CONN.	
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				LA-3981P	Rev
Date	Monday, October 22, 2007	Sheet	18	of	42

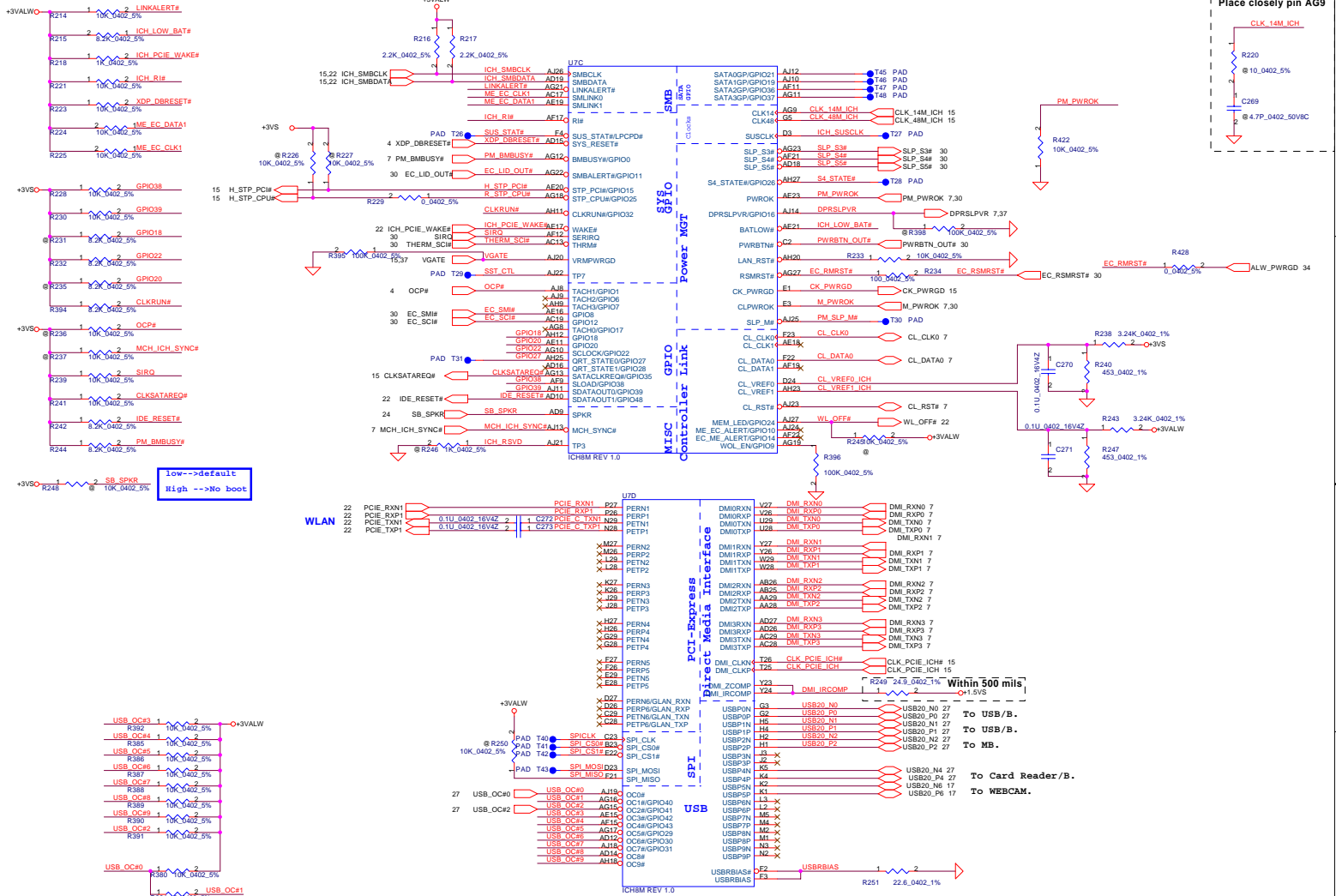


ICH8M Internal VR Enable Strap (Internal VR for VccSus1.05, VccSus1.5, VccCLL1.5)	
ICH_INTVRMEN	Low = Internal VR Disabled High = Internal VR Enabled(Default)
ICH8M LAN100 SLP Strap (Internal VR for VccLAN1.05 and VccCLL1.05)	
ICH_LAN100_SLP	Low = Internal VR Disabled High = Internal VR Enabled(Default)

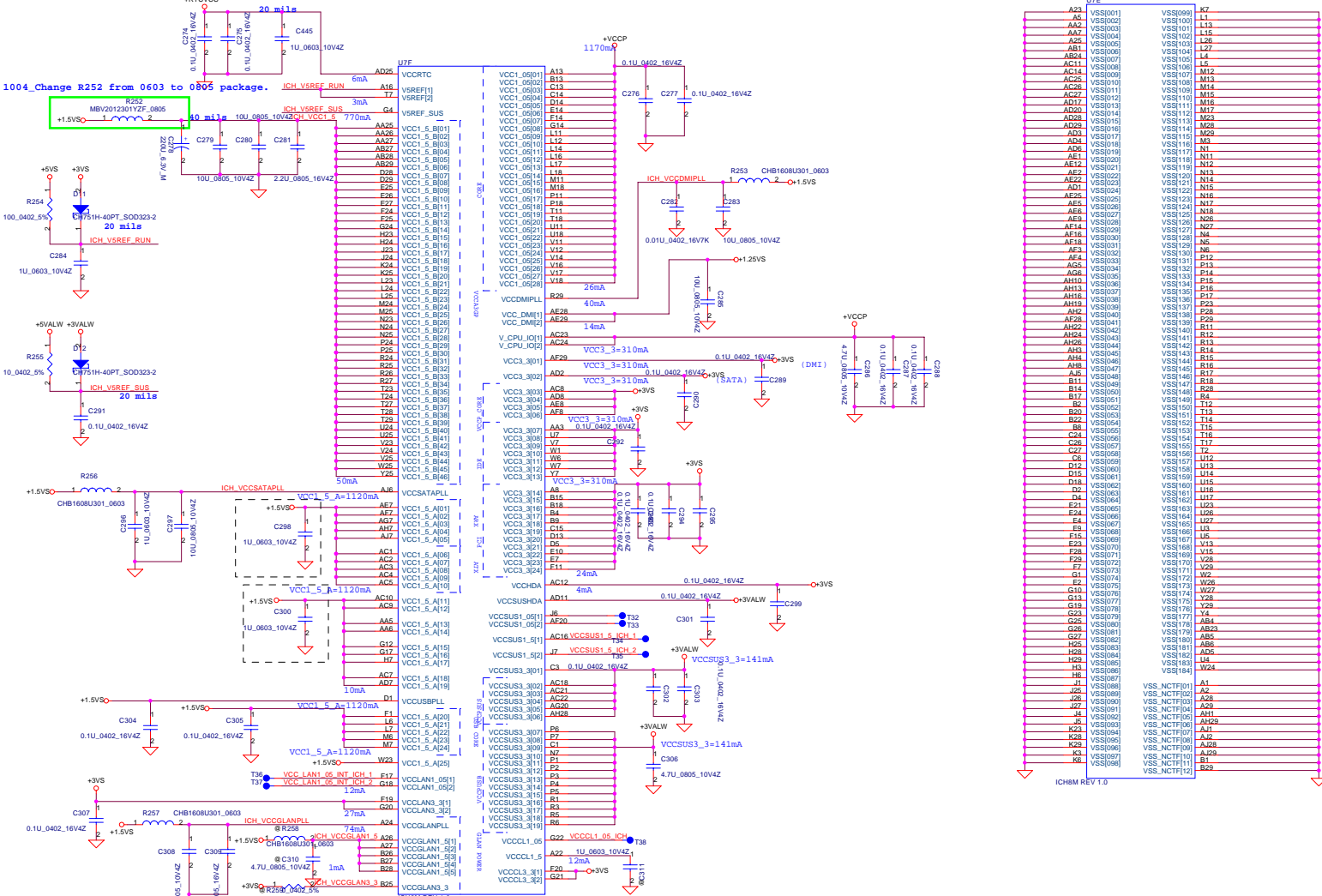


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Issued Date	2007/03/26	Deciphered Date	2006/03/10	Size	Document Number
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				Date	Monday, October 22, 2007
				Sheet	18 of 42

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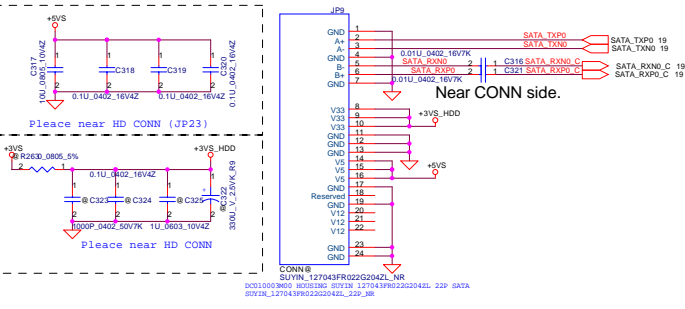


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Size	Document Number	Rev	
Customer	LA-3901P	ICH8(3/4) PM,USB,GPIO	
Date	Monday, October 22, 2007	Sheet	29 of 42

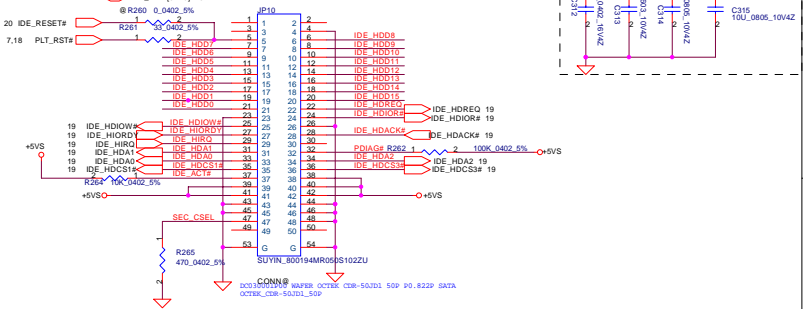


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Issued Date	2007/03/26	Deciphered Date	2006/03/10	Customer
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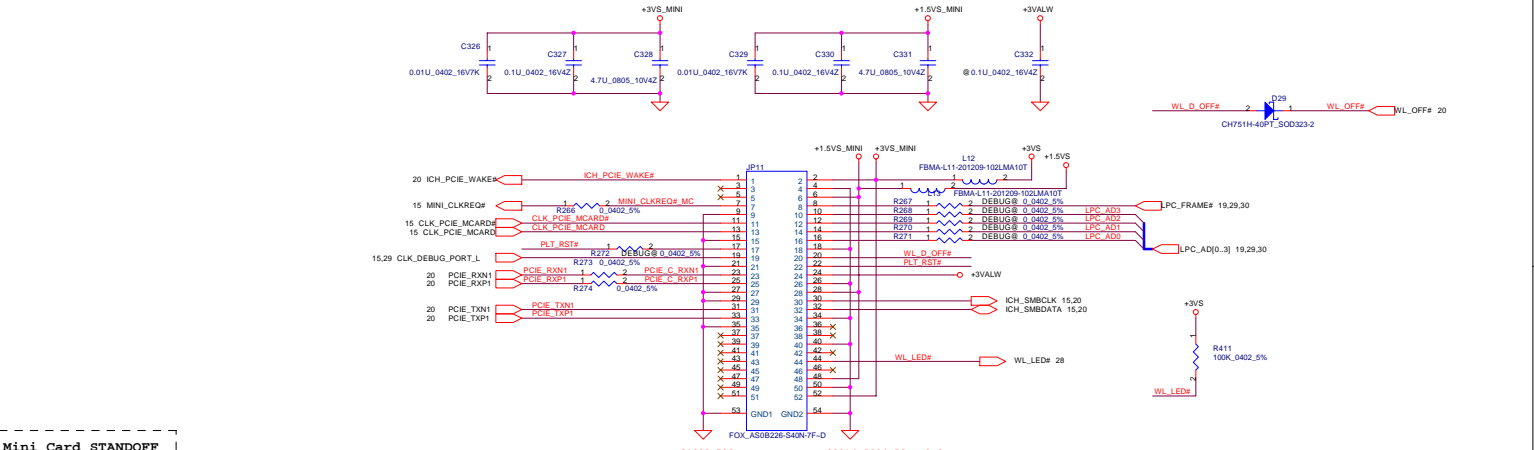
HDD Connector



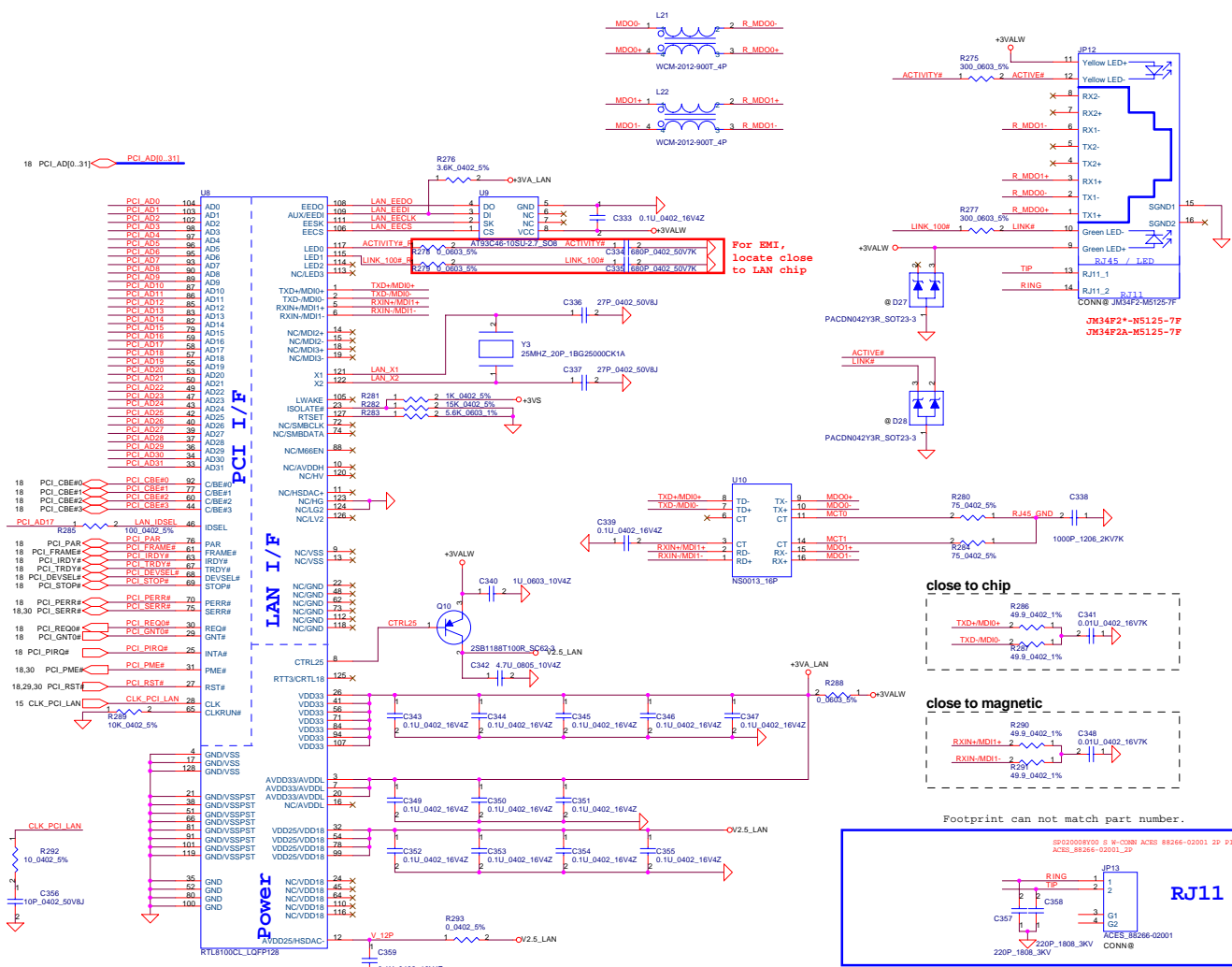
CD-ROM Connector



Mini-Express Card---WLAN



Security Classification		Compal Secret Data		Title	
Issued Date		Deciphered Date		HDD/ODD/Mini Card CONN.	
2007/03/26		2007/08/29		LA-3981P	
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				Monday, October 22, 2007	0.3
				Sheet	22 of 42



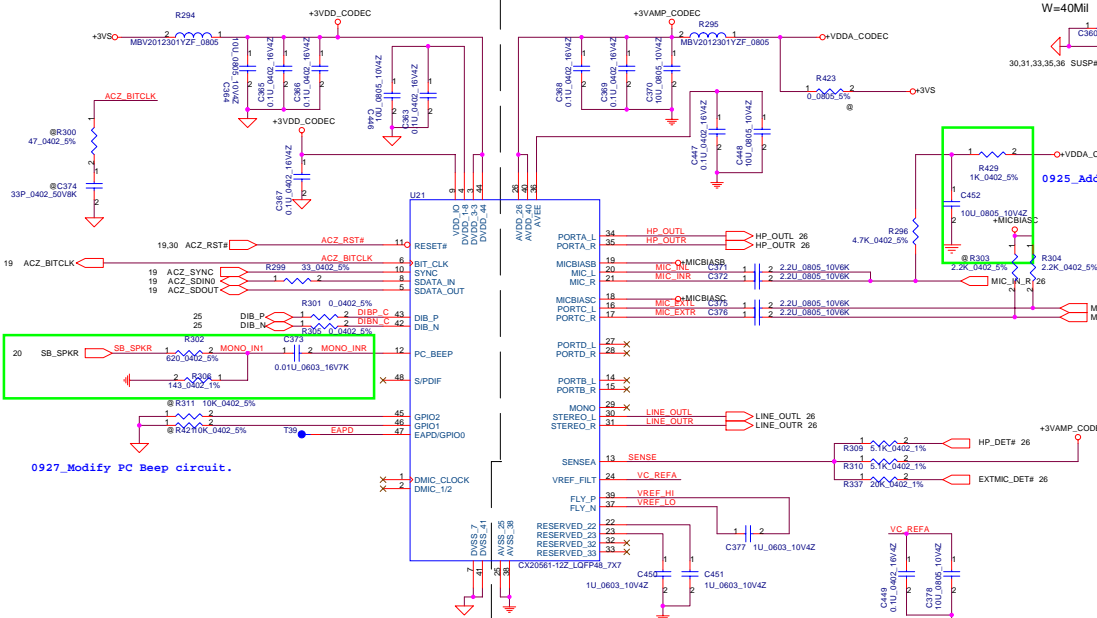
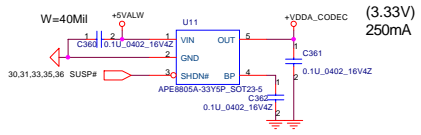
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Issued Date	2007/03/26	Deciphered Date	2007/08/29	LAN-8100CL	
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Date	Monday, October 22, 2007	Sheet	23	of	42

In order for the modem wake on ring feature to function, the CODEC must be powered by a rail that is not removed when the system is in standby.

AUDIO CODEC

For Layout:
Place decoupling caps near the power pins of SmartAMC device.

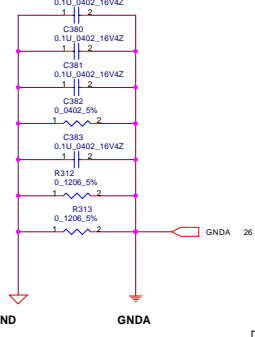
CODEC POWER



0927_Modify PC Bleep circuit.

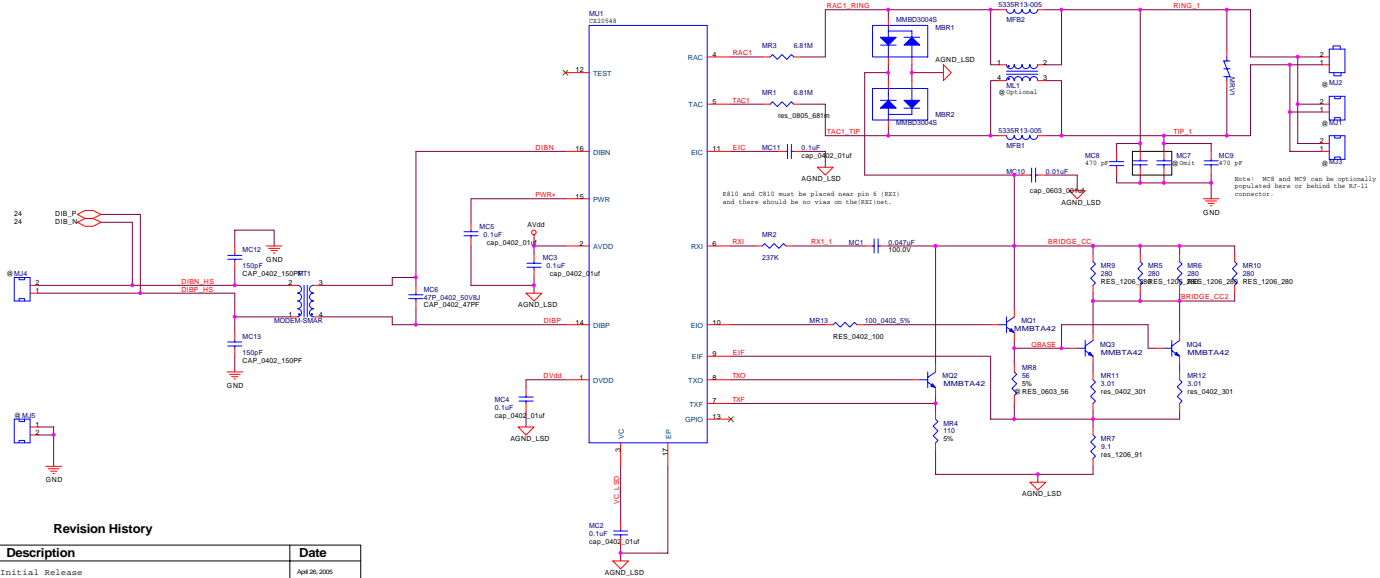
0925_Add LPF to reduce INT. MIC noise.

DIGITAL ANALOG



HP_DET#	MIC_DET	LINEOUT	PORT-A <Earphone OUT>	MIC	EQ
0 (LOW)	0 (LOW)	OFF	ON	ON	Disable
0 (LOW)	NC	OFF	ON	OFF	Disable
NC	0 (LOW)	ON	OFF	ON	Enable
NC	NC	ON	OFF	OFF	Enable

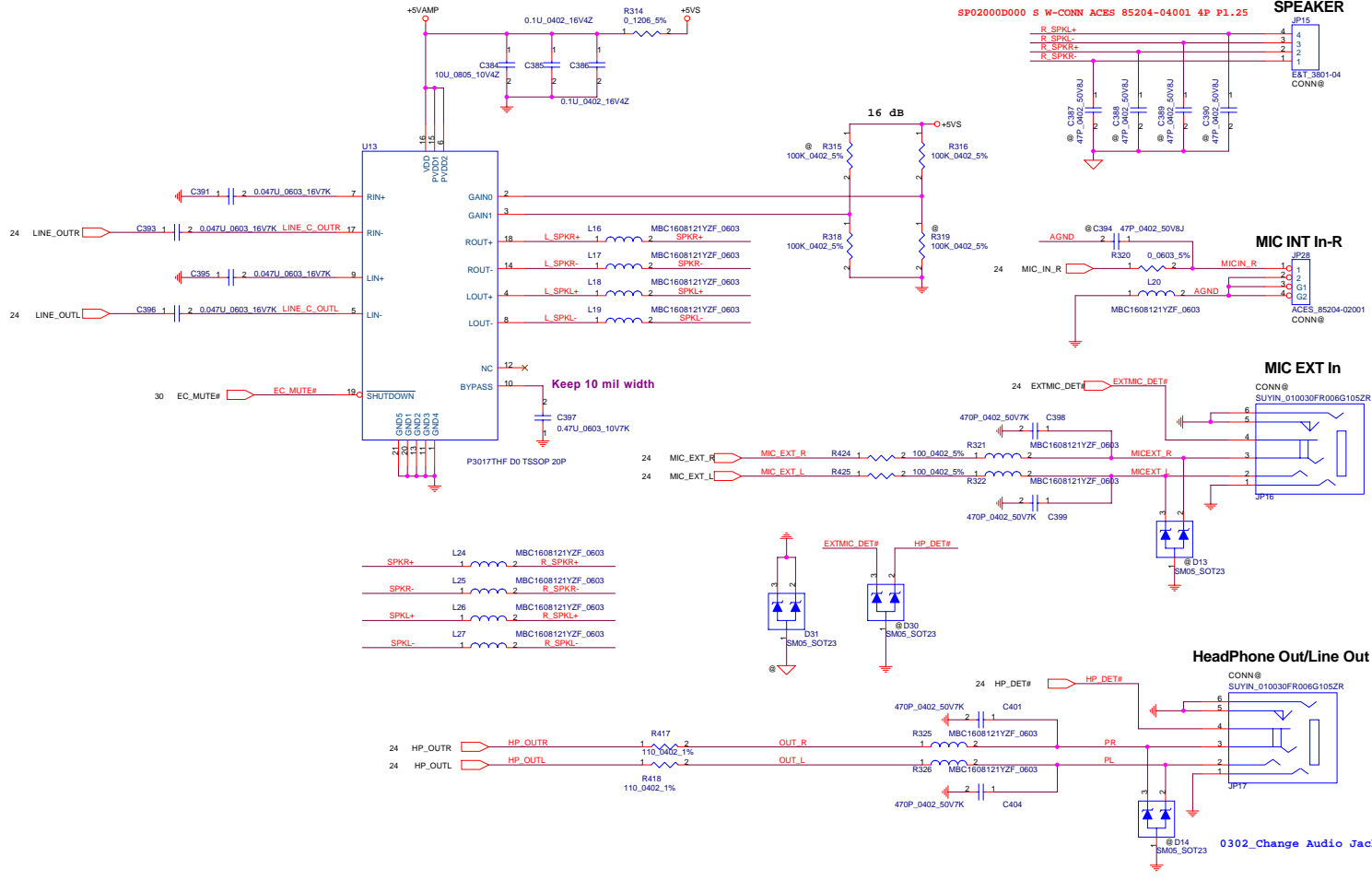
Security Classification		Compal Secret Data		Title	
Issued Date	2007/03/26	Deciphered Date	2006/03/10	AMOM codec	
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				LA-3981P	Rev 0.3
				Date	Monday, October 22, 2007
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Revision History

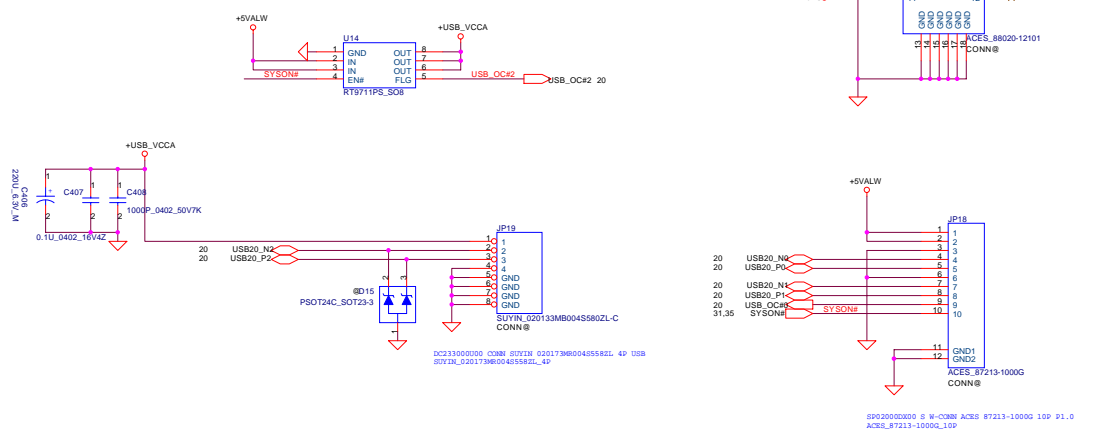
REV	Description	Date
0	Initial Release	April 26, 2005
1	No changes to schematic. PCB updated to -003. Updated footprints and corrected via spacing errors.	April 18, 2005
2	Changed MC8 and MC9 pads. No schematic changes. PCB updated to -005.	November 3, 2005
3	Added MR11 and MR12. PCB updated to -007.	November 15, 2005
4	Added MR13. PCB updated to -009.	January 3, 2006
4.01	AVL update only.	April 20, 2006

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Doc No	LA-391P	Rev	0.3	Date: Monday, October 22, 2007 Sheet 25 of 42		



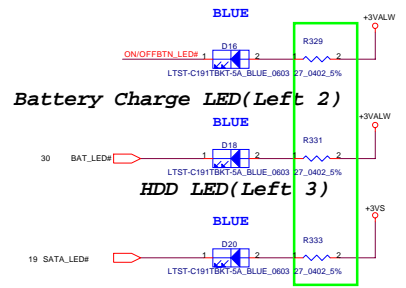
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Issued Date	2007/03/26	Deciphered Date	2007/08/29	AMP & Audio Jack
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USB Port

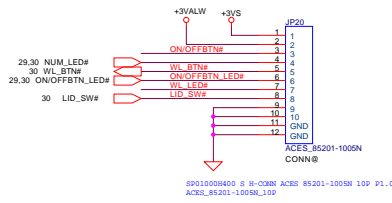


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Issued Date	2007/03/26	Deciphered Date	2006/07/26	USB CONN.	
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Size	Document Number	Rev		0.3	
	LA-398IP				
Date:	Monday, October 22, 2007	Sheet	27	of	42

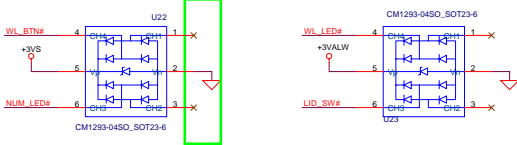
POWER LED(Left 1)



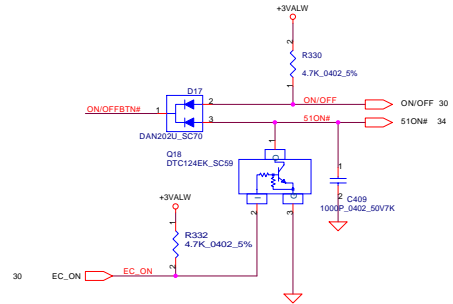
M/BtoS/B



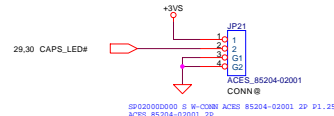
1005_Disconnect ON/OFFBTN# and ON/OFFBTN_LED# from U22.



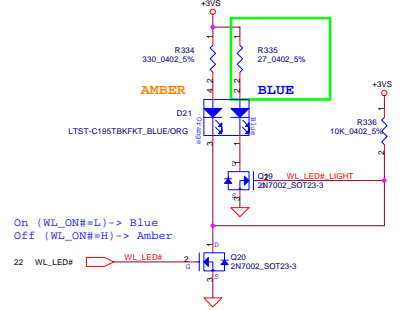
Power ON/OFF



M/B to SB(Caps Lock LED)

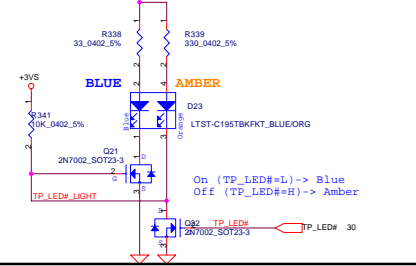


Wireless ON/OFF LED(Left 4)

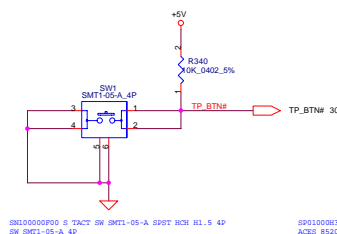


D21, D25, D23 Footprint can not match part number.

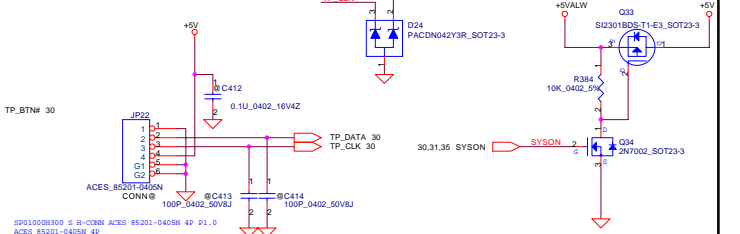
TouchPAD ON/OFF LED



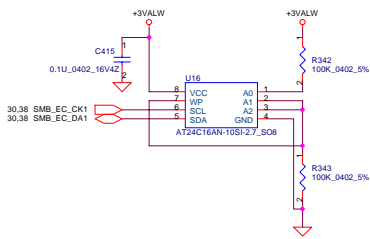
TP ON/OFF



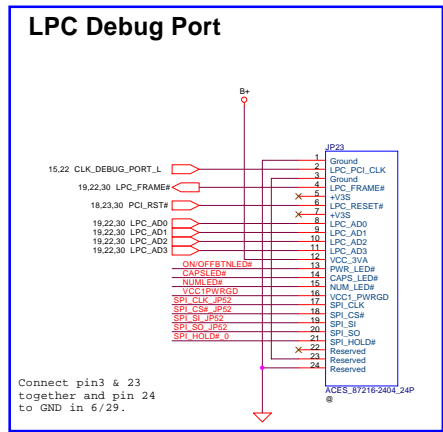
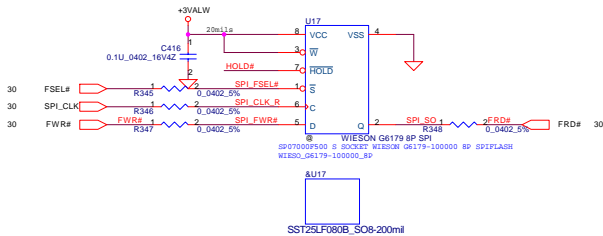
T/P Board



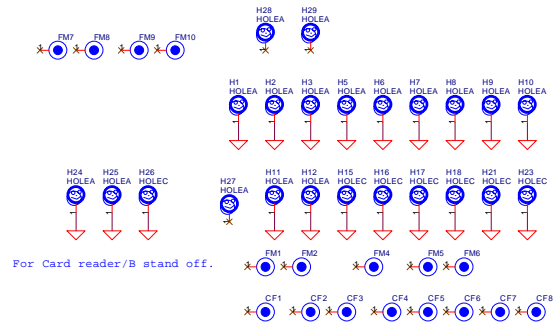
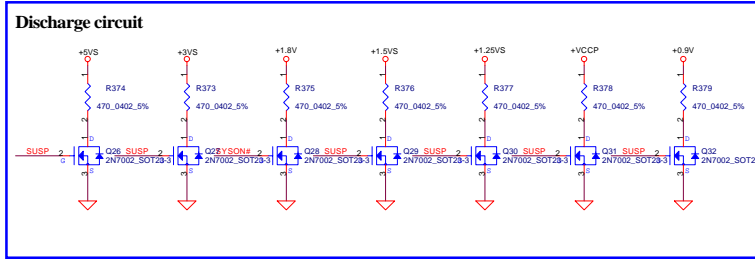
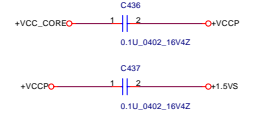
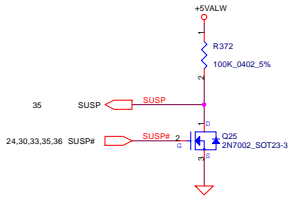
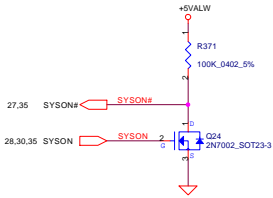
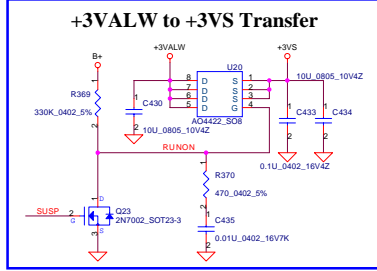
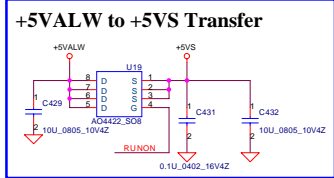
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Issued Date	2007/03/26	Deciphered Date	2006/07/26	Title
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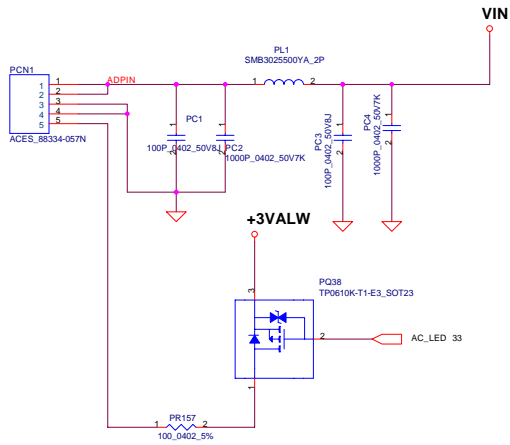
SPI ROM



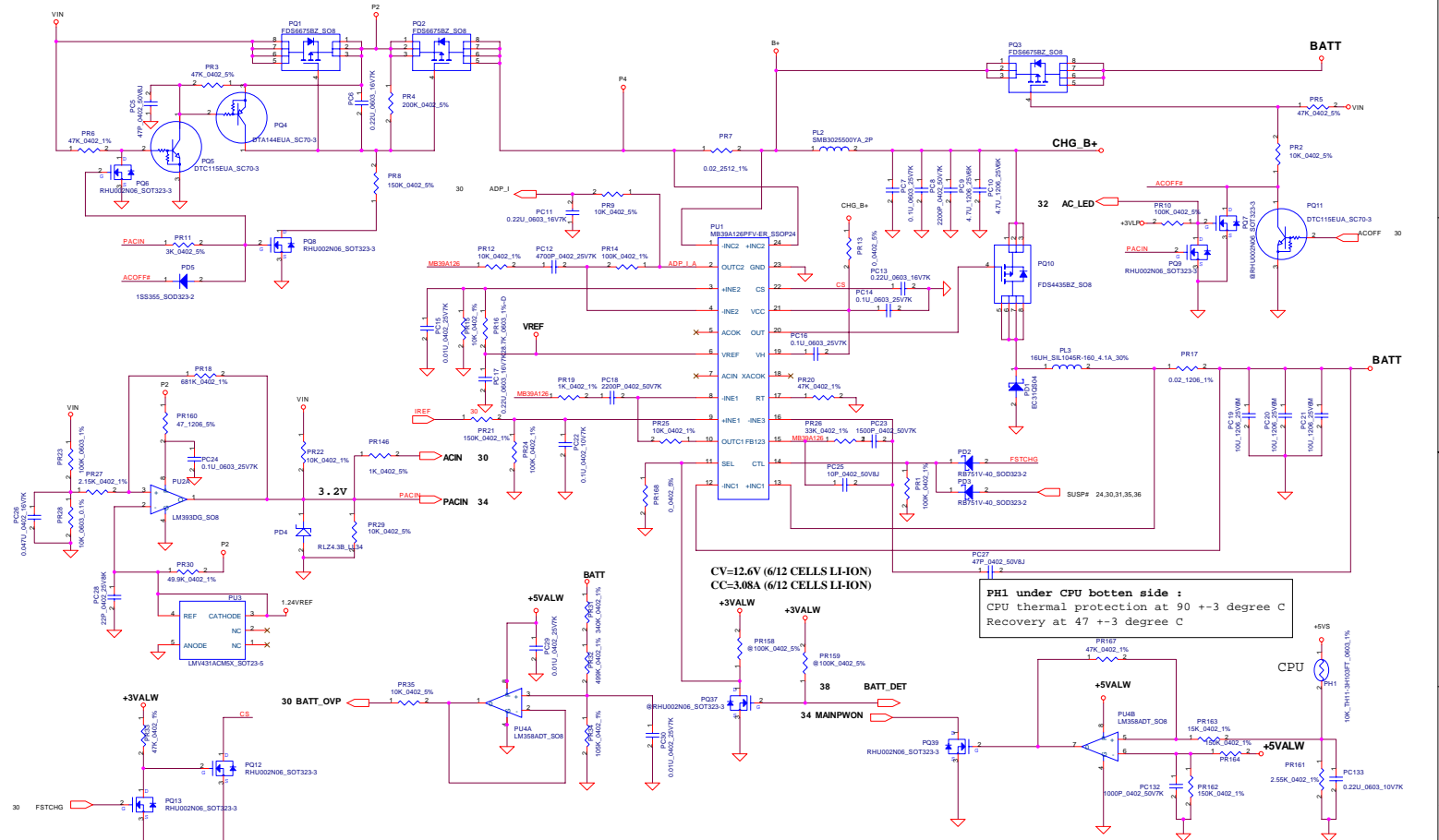
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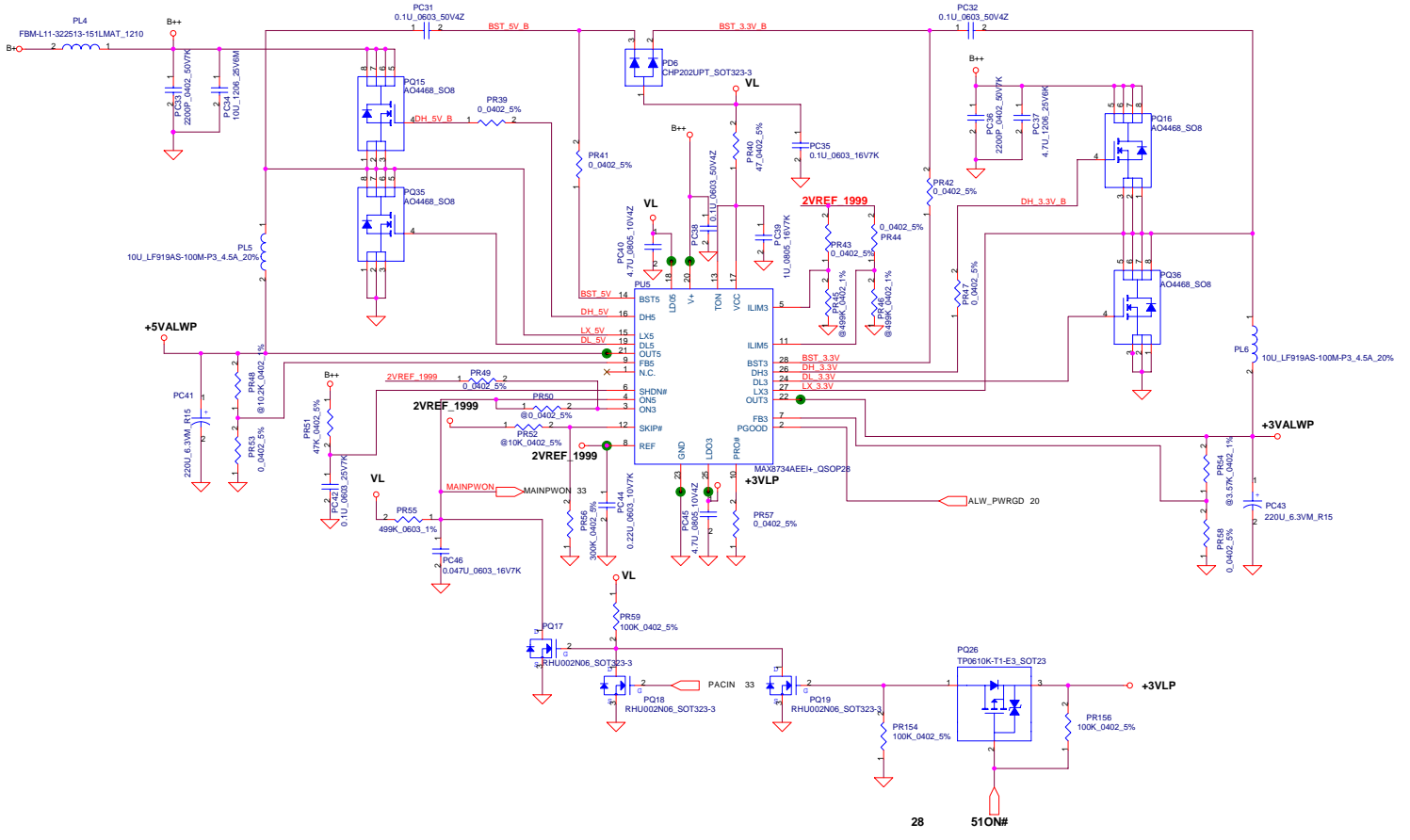


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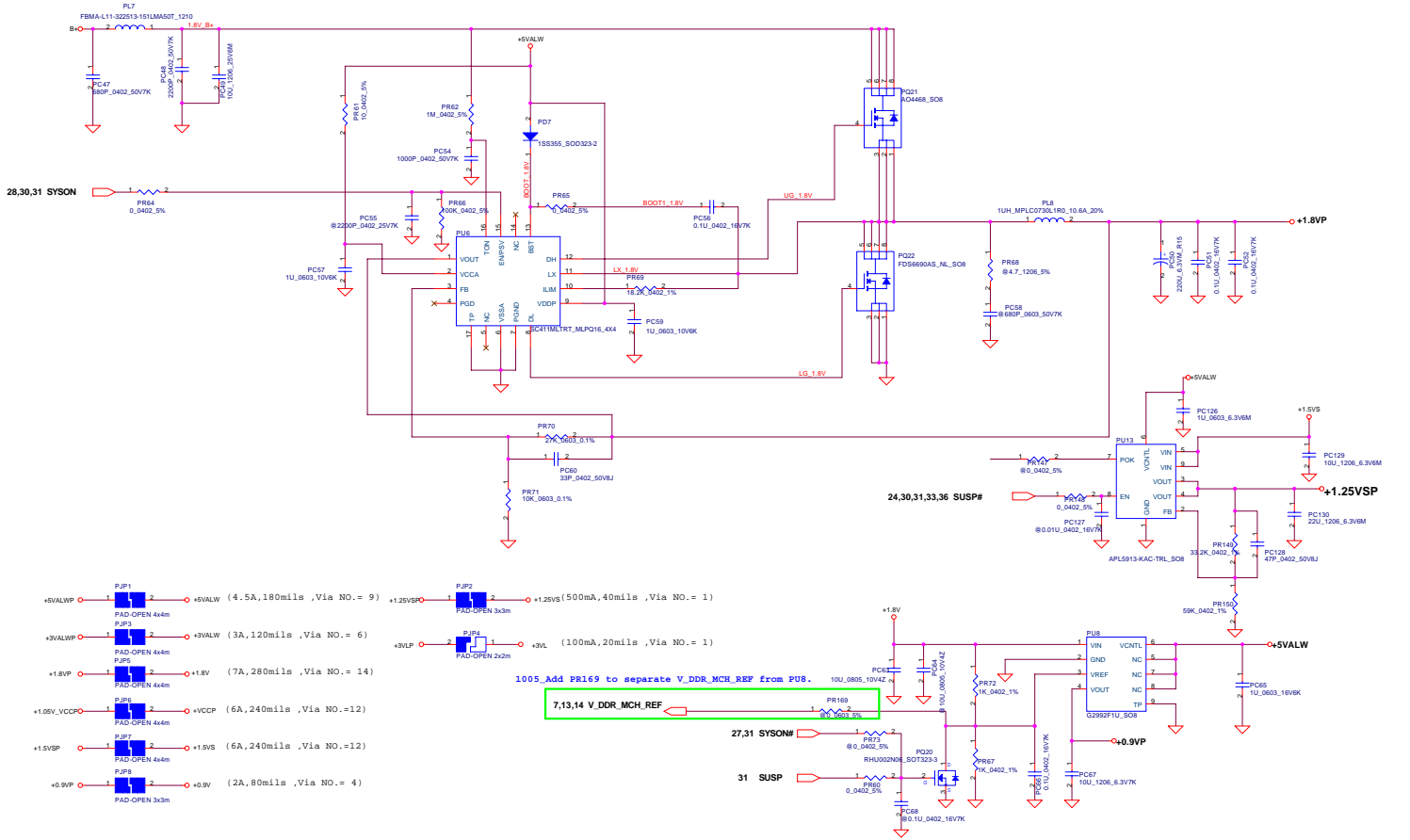
PH1 under CPU bottom side :
 CPU thermal protection at 90 +/-3 degree C
 Recovery at 47 +/-3 degree C

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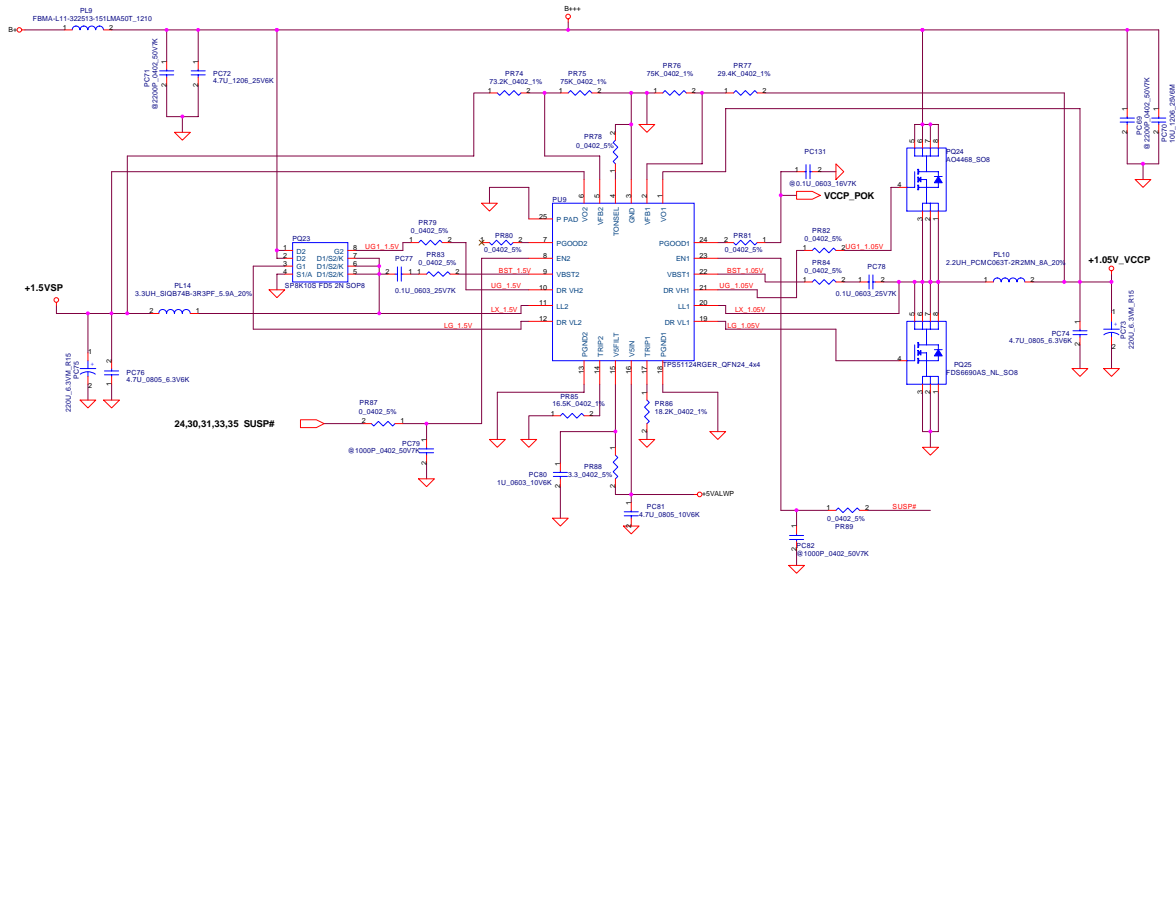
28 510N#

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Issued Date	<Issued_Date>	Deciphered Date	<Deciphered_Date>	Title: 3.3VALWP / 5VALWP	
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Size	Document Number	Rev			
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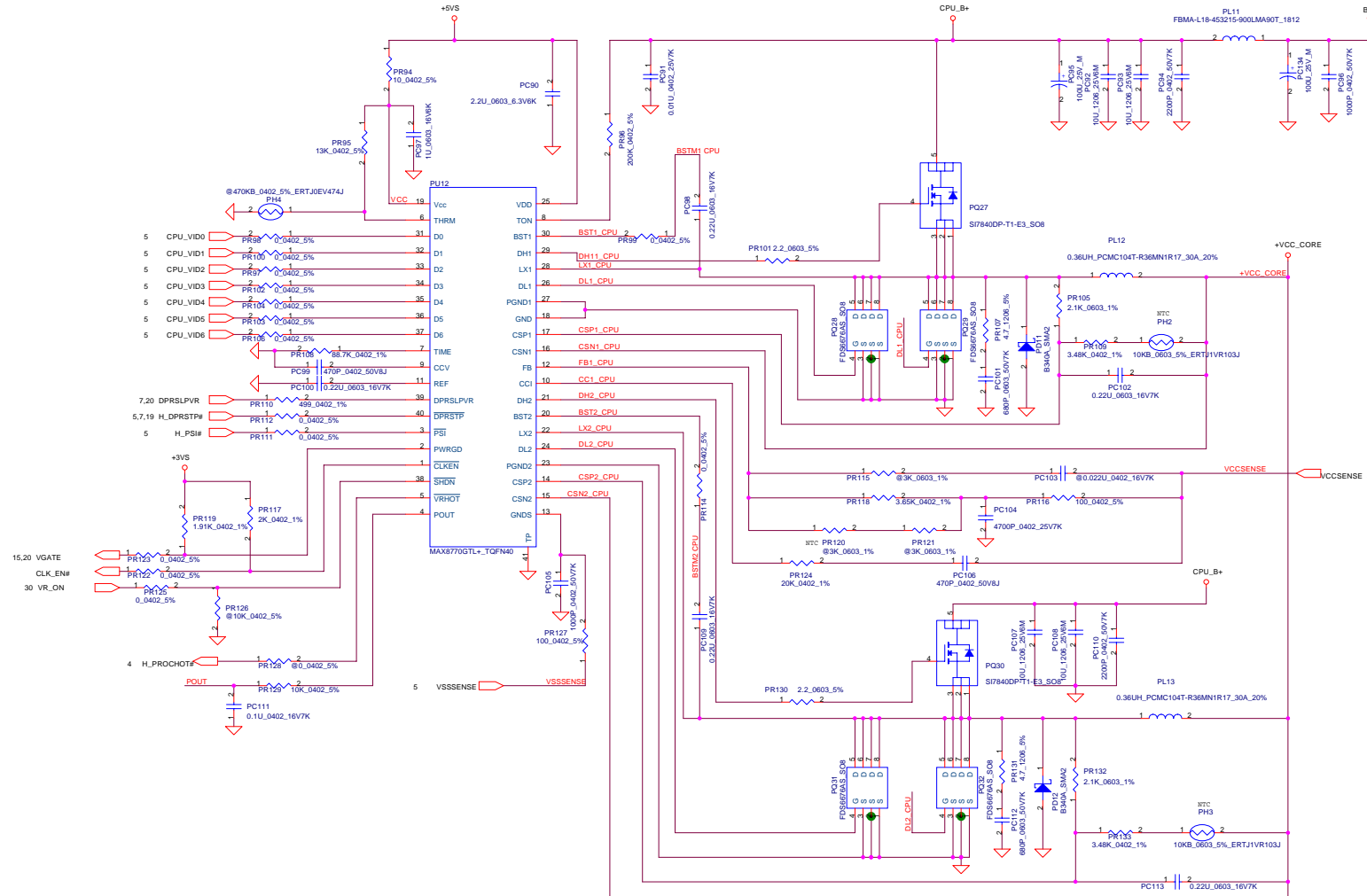


- +SVALWP PJP1 2 +SVALW (4.5A,180mils ,Via NO.= 9)
- +SVALWP PJP2 2 +SVALW (3A,120mils ,Via NO.= 6)
- +1.8VP PJP3 2 +1.8V (7A,280mils ,Via NO.= 14)
- +1.05V_VCCP PJP6 2 +VCCP (6A,240mils ,Via NO.=12)
- +1.5VSP PJP7 2 +1.5VS (6A,240mils ,Via NO.=12)
- +0.9VP PJP8 2 +0.9V (2A,80mils ,Via NO.= 4)
- +1.25VSP PJP2 2 +1.25VSP (500mA,40mils ,Via NO.= 1)
- +VLP PJP1 1 +VLP (100mA,20mils ,Via NO.= 1)

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Size	Document Number	Rev	03		
DATE	Monday, October 25, 2009	Issue	35	of	49

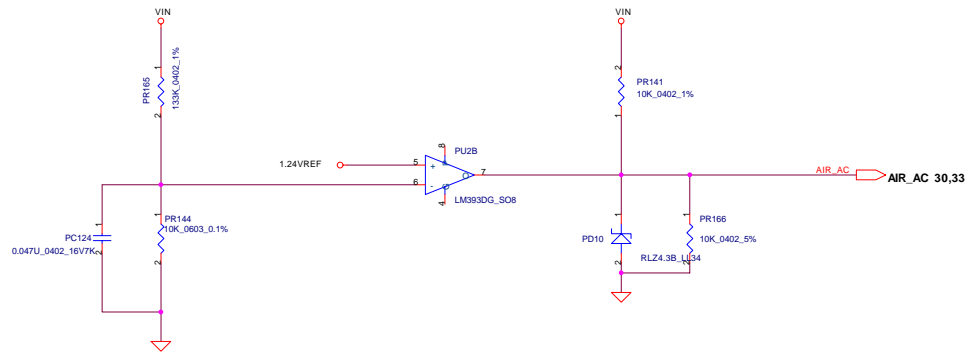
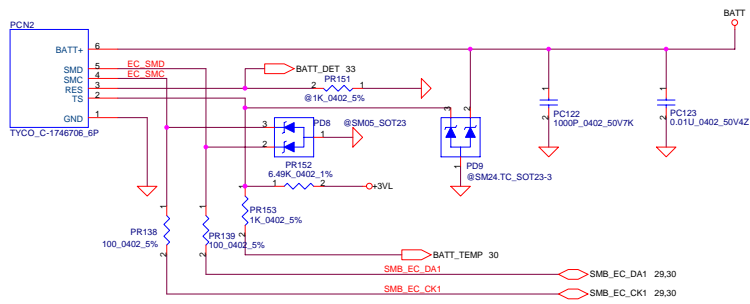


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Compal Electronics, Inc.		
File	+CPU CORE	
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Item	Reason for change	PG#	Modify List	Date	Phase
1			1009_FL8 change to 1uH.		
2					
3					
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					

Security Classification	Compal Secret Data		Title	
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Version Change List (P. I. R. List) for HW Circuit

Item	Change Item	Page	Date	Phase
1	Change C262 and C263 from 15pF to 12pF	19	7/16	DB --> SI
2	Reserved R245 and Add R422	20	7/16	DB --> SI
3	Add D29 prevent leakage issue	22	7/16	DB --> SI
4	Reserved diode D30 D31 for ESD	26	7/16	DB --> SI
5	Reserved R423 for coat down plan	24	7/24	DB --> SI
6	Remove Q12-Q17, R323 R324 R327 R328 R417 R418	26	7/30	DB --> SI
7	Change EXT MIC port B to port C	24	7/31	DB --> SI
8				DB --> SI
9				DB --> SI
10				DB --> SI
11				DB --> SI
12				DB --> SI
13				DB --> SI
14				DB --> SI
15				DB --> SI
16				DB --> SI
17				DB --> SI
18				DB --> SI
19				DB --> SI
20				DB --> SI
21				DB --> SI
22				DB --> SI
23				DB --> SI
24				DB --> SI
25				DB --> SI
26				DB --> SI
27				DB --> SI
28				DB --> SI
29				DB --> SI

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3

2

1

Rev 0.3

Version Change List (P. I. R. List) for HW Circuit

Item	Change Item	Page	Date	Phase	
1	Change R296 R337 R value	24	Follow conexant new design rule	8/6	SI --> FV
2	Add R424 R425 100ohm on MIC_EXT_R and MIC_EXT_L	26	Follow conexant new design rule	8/6	SI --> FV
3	Change PIRQ from F to A	18	Choose R419 then control PIRQ A	8/14	SI --> FV
4	Connect PCI_SERR# to EC GPIO pin.	18	Connect PCI_SERR# to EC GPIO pin.	8/31	SI --> FV
5	Modify PC BEEP circuit.	20	Modify PC BEEP circuit.	8/31	SI --> FV
6	For support Intel Penryn CPU.	04	Reserve R426 and R427 for support Intel Penryn CPU.	9/3	SI --> FV
7	For ESD request.	28	Add U22 and U23 for ESD request.	9/3	SI --> FV
8	For EMI request.	26	Add L24-L27	9/5	SI --> FV
9	Change C391, C393, C395, C396 from 0.47uF to 0.047uF.	26	Change C391, C393, C395, C396 from 0.47uF to 0.047uF	9/7	SI --> FV
10	Add R417 and R418 to fine-tune Vp-p.	26	Add R417 and R418 to fine-tune Vp-p.	9/7	SI --> FV
11	For ESD request.	20	Add U22 and U23 for ESD request.	9/7	SI --> FV
12					SI --> FV
13					SI --> FV
14					SI --> FV
15					SI --> FV
16					SI --> FV
17					SI --> FV
18					SI --> FV
19					SI --> FV
20					SI --> FV
21					SI --> FV
22					SI --> FV
23					SI --> FV
24					SI --> FV
25					SI --> FV
26					SI --> FV
27					SI --> FV
28					SI --> FV
29					SI --> FV
30					SI --> FV
31					SI --> FV
32					SI --> FV
33					SI --> FV
34					SI --> FV
35					SI --> FV
36					SI --> FV
37					SI --> FV
38					SI --> FV

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Version Change List (P. I. R. List) for HW Circuit

Item	Change item	Page		Date	Phase
1	Solve Vref miss when entry S3 mode.	7	Stuff R43 and R46.	9/25	PV --> MV
2	Solve wave ripple on CRT and TV.	10	Change C439 from 0.47uF to 4.7uF.	9/25	PV --> MV
3	Solve RTC timing too exceed.	18	Change C262 and C263 from 12pF to 15pF.	9/25	PV --> MV
4	Reduce INT.MIC noise.	24	Add LFP (R429 and C452).	9/25	PV --> MV
5	Solve S3 resume fail when use Micron DDR module.	35	Add PR169 to separate V_DDR_MCH_REF from P08.	10/05	PV --> MV
6	Solve pop noise when entry or resume from S3.	24	Modify FC Beep (C373, R302, R306) circuit.	9/27	PV --> MV
7	Solve EMI fail for Memory module.	7	Change R34/R35 from 20 ohm to 30 ohm.	9/27	PV --> MV
8	Fine-tune LED brightness.	28	Change R329, R331, R333, R335 from 33 ohm to 27 ohm.	9/27	PV --> MV
9	ICH 1.5V power rail 700mA current requirement.	21	Change R252 package from 0603 to 0805.	10/04	PV --> MV
10	Solve can not power on when stuff U22.	28	Disconnect ON/OFFBTN# and ON/OFFBTN_LED# from U22.	10/05	PV --> MV
11	For EMI request.	16	Change L2, L3, L4 to FBMA-L10-201209-121LMT_0805.	10/19	PV --> MV
12	To avoid too easy to open solder for CLR2.	15	Change CLR2P1 and CLR2P2 type like the same as PJP4.	10/19	PV --> MV
13	Solve acoustic noise issue.	10	Change R64, R79, R81 from 0 ohm to 1uH/400mA inductor.	10/22	PV --> MV

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