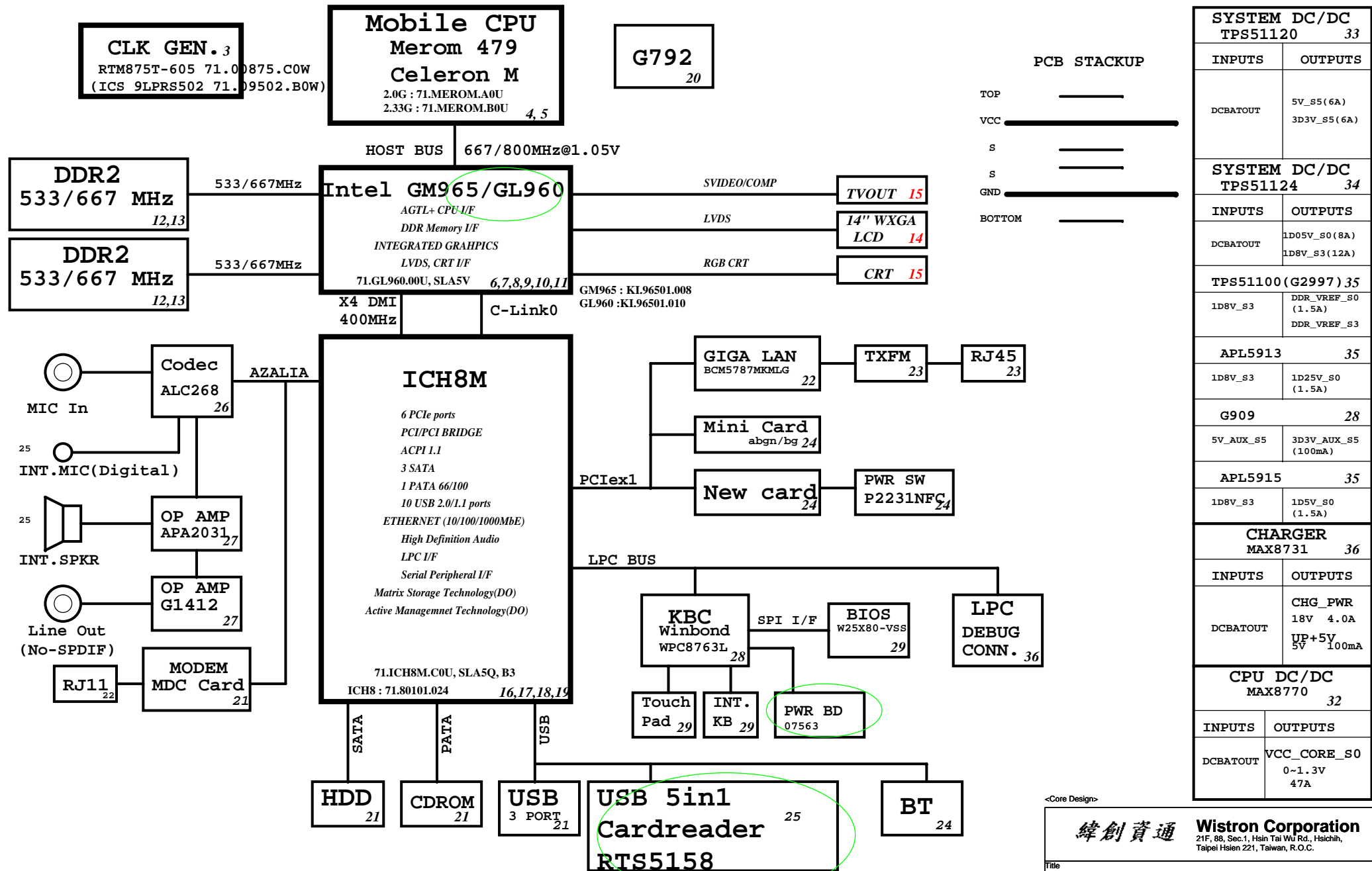


Calado Block Diagram

Project code: 91.4X401.001
 PCB P/N : 07227
 REVISION : -1



ICH8M Functional Strap Definitions

ICH8-M EDS 21762 2.0V1 page 16

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low. When TP3 not pulled low at rising edge of PWROK, sets bit1 of RPC.PC(Config Registers: offset 224h)
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#	PCIE config2 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#/ SPI_CS1#	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
INTVRMEN	Integrated VccSus1_05, VccSus1_5 and VccCL1_5 VRM Enable/Disable. Always sampled.	Enables integrated VccSus1_05, VccSus1_5 and VccCL1_5 VRM's when sampled high
LAN100_SLP	Integrated VccLAN1_05 and VccCL1_05 VRM Enable/Disable. Always sampled.	Enables integrated VccLAN1_05 and VccCL1_05 VRM's when sampled high
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH8 will disable the TCO timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	This signal has a weak internal pull-up. Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be used in manufacturing environments.

ICH8M Integrated Pull-up and Pull-down Resistors

ICH8-M EDS 21762 2.0V1

SIGNAL	Resistor Type/Value
HDA_BIT_CLK	PULL-DOWN 20K
HDA_RST#	NONE
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT[3:0]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K ?
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 10K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#	PULL-UP 20K
SPI_CLK	PULL-UP 20K
SPI_MOSI	PULL-UP 20K
SPI_MISO	PULL-UP 20K
TACH_[3:0]	PULL-UP 20K ?
SPKR	PULL-DOWN 20K
TP[3]	PULL-UP 20K
USB[9:0][P,N]	PULL-DOWN 15K
CL_RST#	PULL-UP 13K

Crestline Strapping Signals and Configuration

Crestline EDS 20954 1.0 page 7

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	001 = FSB533 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG[8:6]	Reserved	
	Low Power PCI Express	0 = Normal mode 1 = Low Power mode (Default)
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes,15->0,14->1 ect.. 1 = Normal operation(Default):Lane Numbered in order
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled 11 = Normal Operation (Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG[18:17]	Reserved	
CFG19	DMI Lane Reversal	0 = Normal operation (Default):lane Numbered in order 1 =Reverse Lane,4->0,3->1 ect...
CFG20	SDVO/PCIE Concurrent	0 = Only SDVO or PCIE x1 is operational (Default) 1 =SDVO and PCIE X1 are operating simultaneously via the PEG port
SDVOCRTL_DATA	SDVO Present	0 = No SDVO Card present (Default) 1= SDVO Card present

NOTE: All strap signals are sampled with respect to the leading edge of the Crestline GMCH PWROK in signal.

History

ICH8M IDE Integrated Series Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm
--	----------------------

USB Table

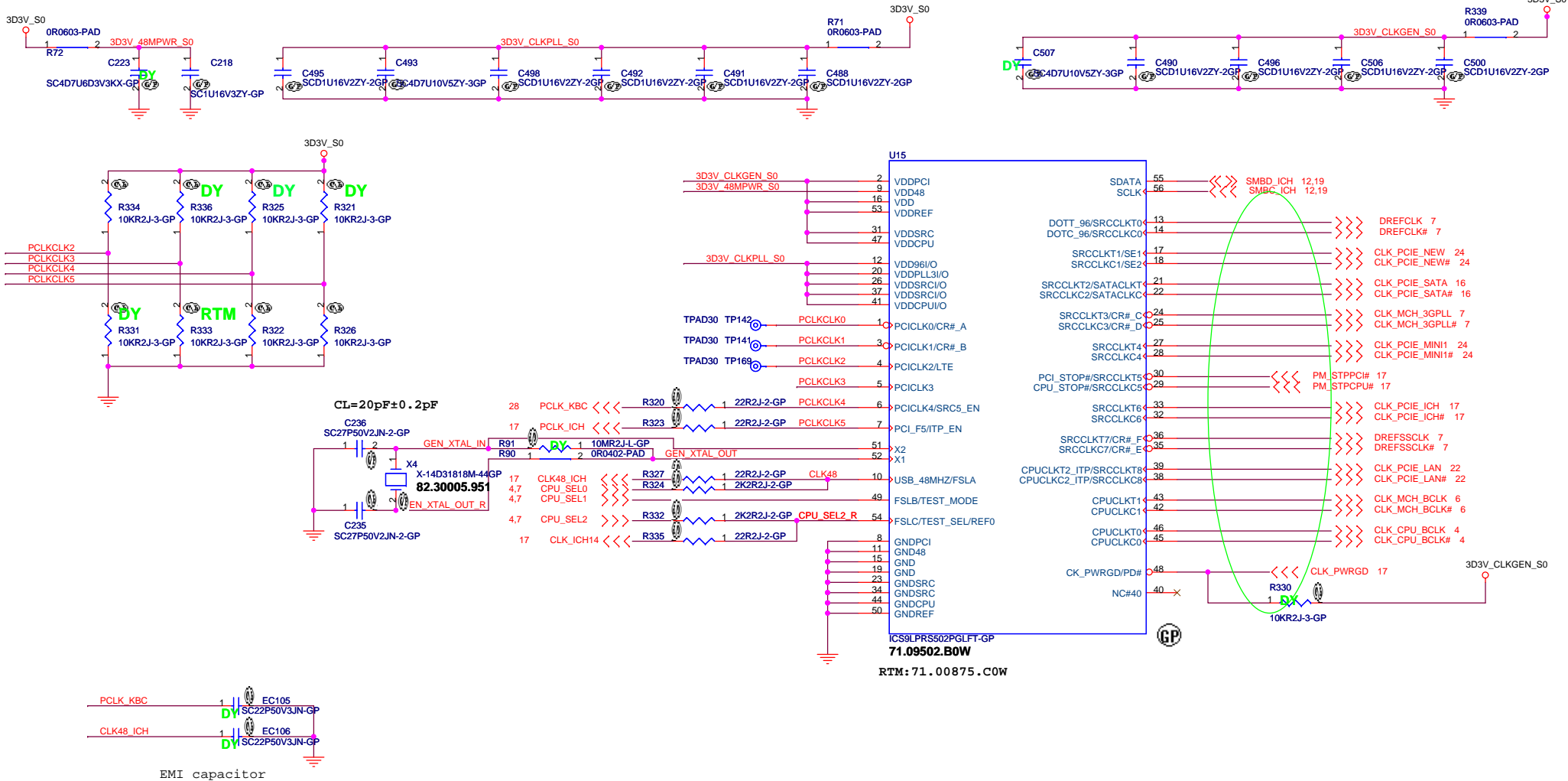
USB	
Pair	Device
0	USB1
1	NC
2	USB2
3	NC
4	USB3
5	BT
6	Cardreader
7	MINICARD
8	CCD
9	NEW1

PCIE Routing

LANE1	LAN Marvell
LANE2	MiniCard WLAN
LANE3	NewCard WLAN

<Core Design>

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		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Reference			
Size A3	Document Number	Rev	
	Volvi2	-1	
Date: Monday, September 10, 2007	Sheet 2 of	39	



ICS9LPR502HGLFT-GP setting table

PIN NAME	DESCRIPTION
PCI0/CR#_A	Byte 5, bit 7 0 = PCI0 enabled (default) 1 = CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair Byte 5, bit 6 0 = CR#_A controls SRC0 pair (default), 1 = CR#_A controls SRC2 pair
PCI1/CR#_B	Byte 5, bit 5 0 = PCI1 enabled (default) 1 = CR#_B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pair Byte 5, bit 4 0 = CR#_B controls SRC1 pair (default) 1 = CR#_B controls SRC4 pair
PCI2/TME	0 = Overclocking of CPU and SRC Allowed 1 = Overclocking of CPU and SRC NOT allowed
PCI4/SRC5_EN	0 = Pin29 as CPU_STOP#, pin 30 as PCI_STOP#. 1 = Pins29,30 as SRC-5 differential pair.
PCI_F5/ITP_EN	0 = SRC8/SRC# 1 = ITP/ITP#

RTM875T-605 setting table

PIN NAME	DESCRIPTION
PCI0/CR#_A	Byte 5, bit 7 0 = PCI0 enabled (default) 1 = CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair Byte 5, bit 6 0 = CR#_A controls SRC0 pair (default), 1 = CR#_A controls SRC2 pair
PCI1/CR#_B	Byte 5, bit 5 0 = PCI1 enabled (default) 1 = CR#_B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pair Byte 5, bit 4 0 = CR#_B controls SRC1 pair (default) 1 = CR#_B controls SRC4 pair
PCI2/TME	0 = Overclocking of CPU and SRC Allowed 1 = Overclocking of CPU and SRC NOT allowed
PCI3/SRC-5_EN	0 = Pin29 as CPU_STOP#, pin 30 as PCI_STOP#. 1 = Pins29,30 as SRC-5 differential pair.
PCI4/27M_SEL	0 = Pin17 as SRC-1, Pin18 as SRC-1#, Pin13 as DOT96, Pin14 as DOT96# 1 = Pin17 as 27MHz, Pin 18 as 27MHz_SS, Pin13 as SRC-0, Pin14 as SRC-0#
PCI_F5/ITP_EN	0 = SRC8/SRC# 1 = ITP/ITP#

SEL2	SEL1	SEL0	CPU	FSB
FSC	FSB	FSA		
1	0	1	100M	X
0	0	1	133M	X
0	1	1	166M	667M
0	1	0	200M	800M

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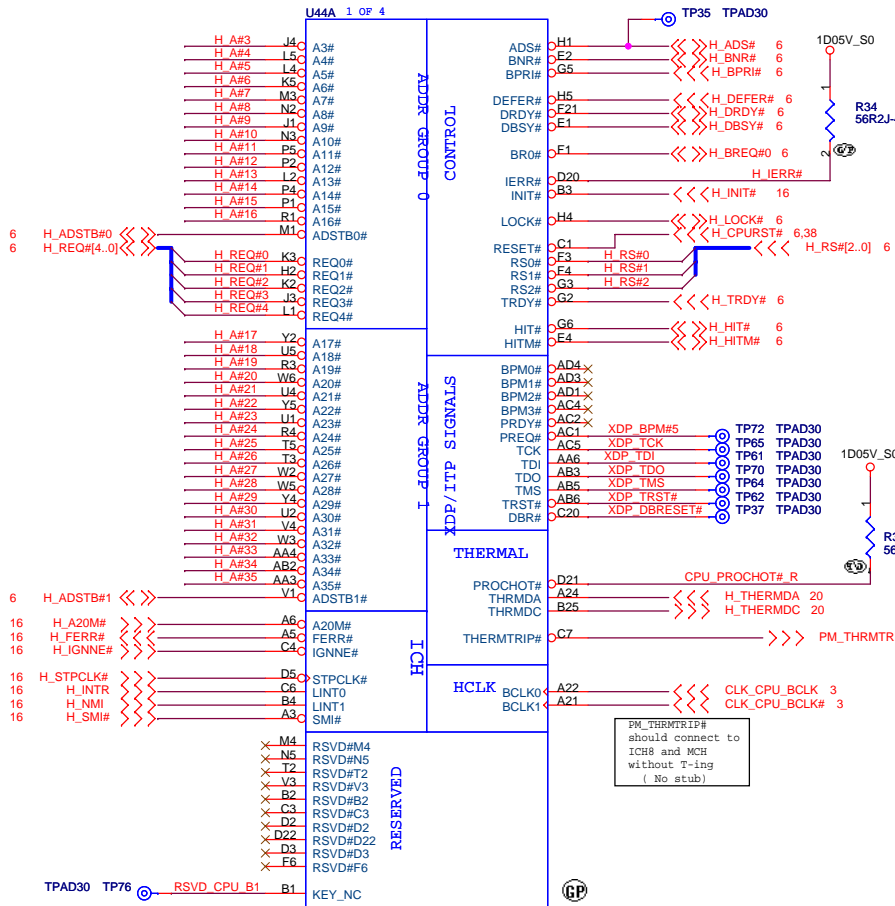
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Size Document Number **Calado** Rev -1

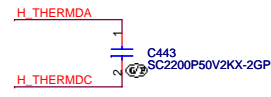
Date: Wednesday, September 12, 2007 Sheet 3 of 39

6 H_A#(35..3) <<<>> H_A#(35..3)

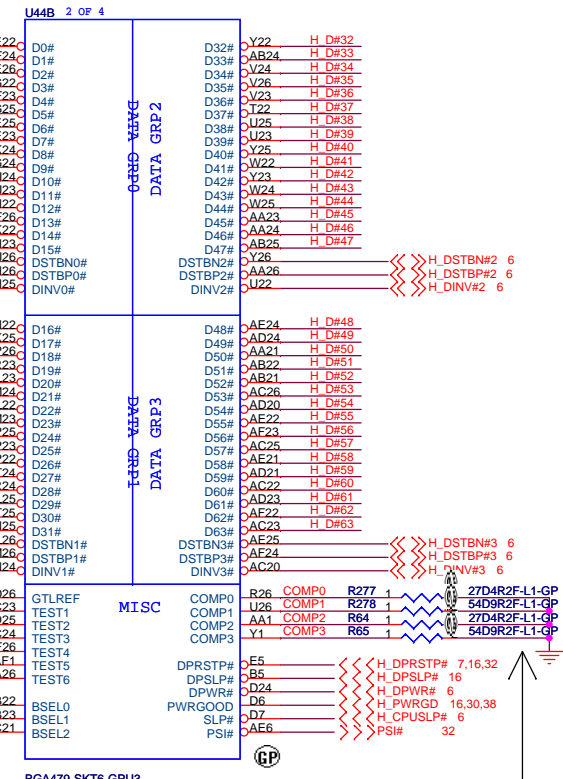
H_DINV#[3..0] <<>> H_DINV#[3..0] 6
H_DSTBN#[3..0] <<>> H_DSTBN#[3..0] 6
H_DSTBP#[3..0] <<>> H_DSTBP#[3..0] 6
H_D#(63..0) <<>> H_D#(63..0) 6



Place testpoint on H_IERR# with a GND 0.1" away



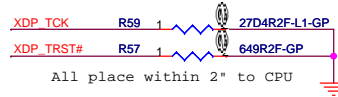
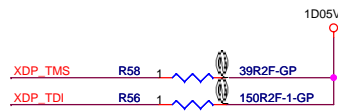
6 H_DSTBN#0
6 H_DSTBP#0
6 H_DINV#0



Layout Note: "CPU_GTLREF0" 0.5" max length.

Net "TEST4" as short as possible, make sure "TEST4" routing is reference to GND and away other noisy signals

Layout Note: Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5"
Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5"



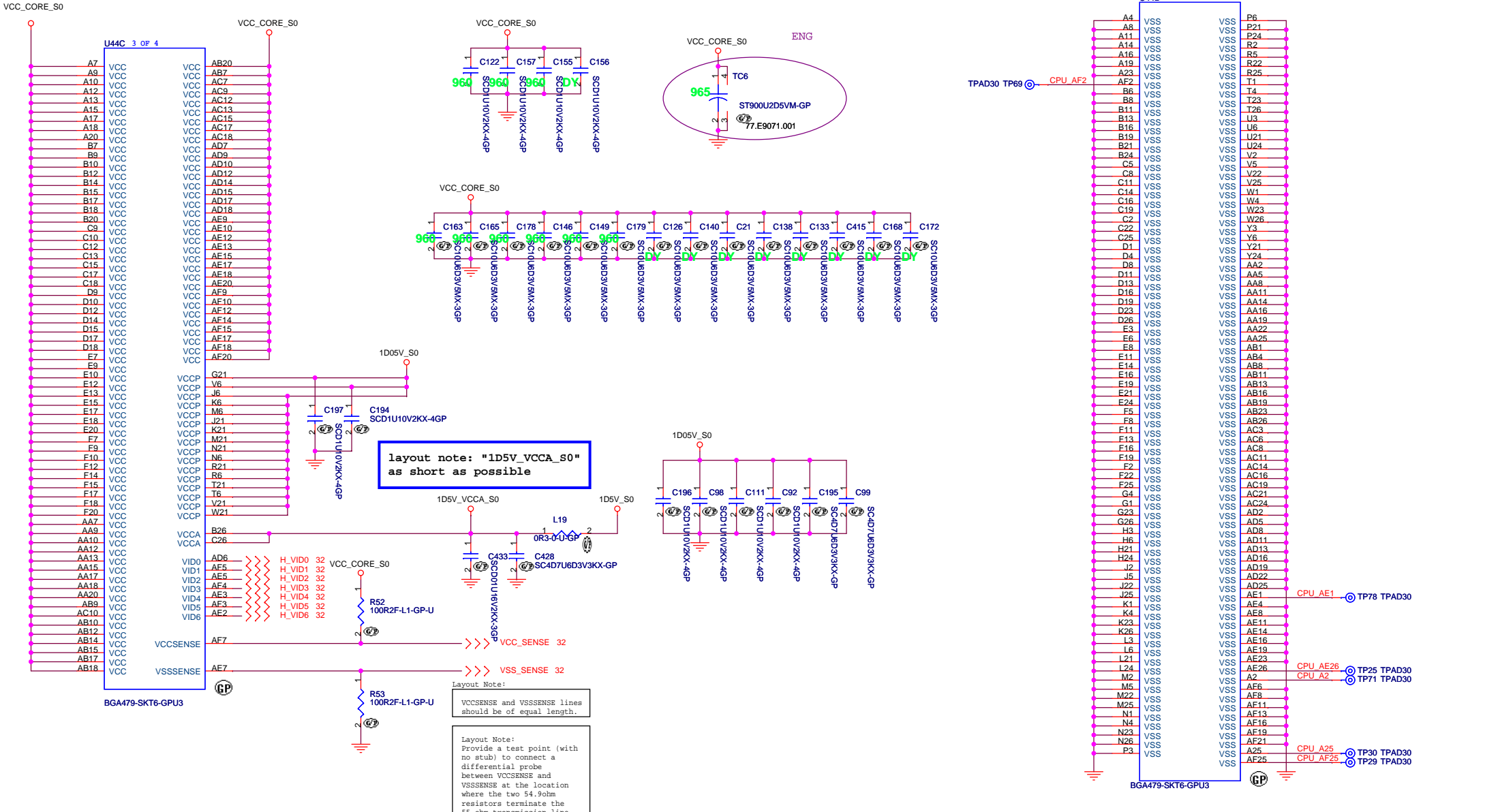
62.10079.001
2nd source: 62.10053.401

BGA479-SKT6-GPU3

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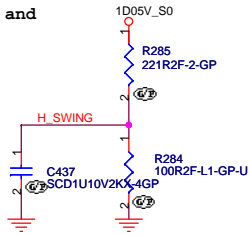
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Size	Document Number	Rev	
Calado		-1	
Date: Wednesday, September 12, 2007	Sheet 4	of 39	

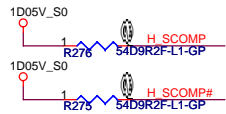


H_SWING routing Trace width and Spacing use 10 / 20 mil

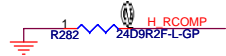
H_SWING Resistors and Capacitors close MCH 500 mil (MAX)



H_SCOMP and H_SCOMP# Resistors and Capacitors close MCH 500 mil (MAX)

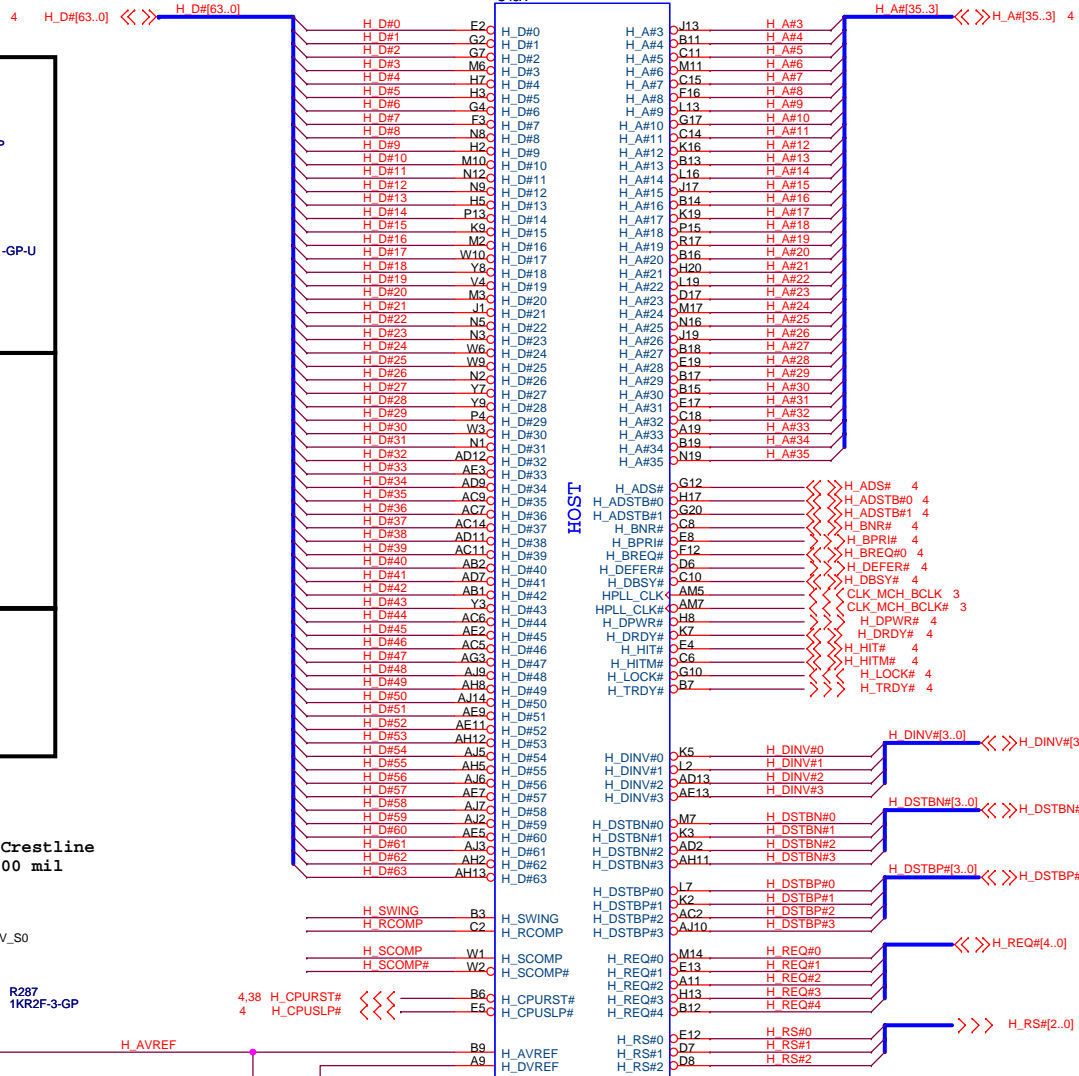
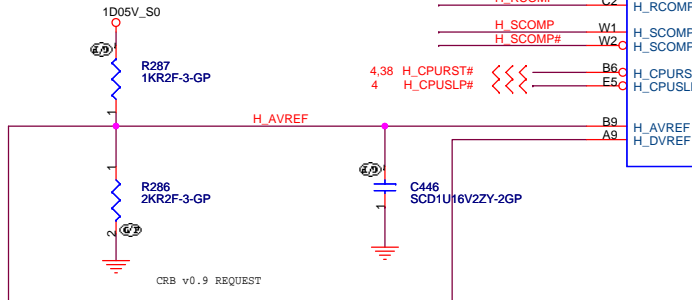


H_RCOMP routing Trace width and Spacing use 10 / 20 mil



Place them near to the chip (< 0.5")

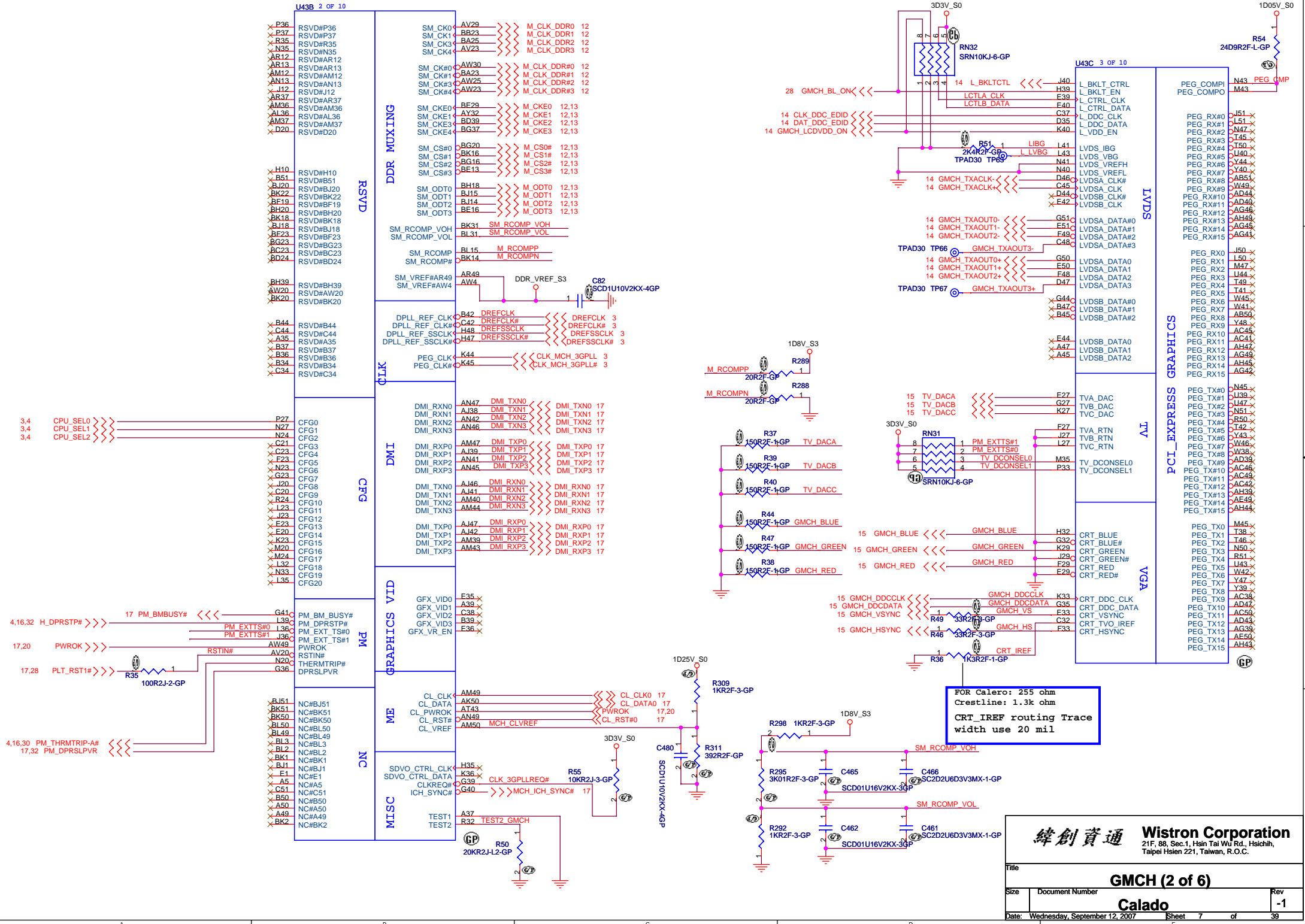
H_REF Decoupling Crestline close Crestline 100 mil



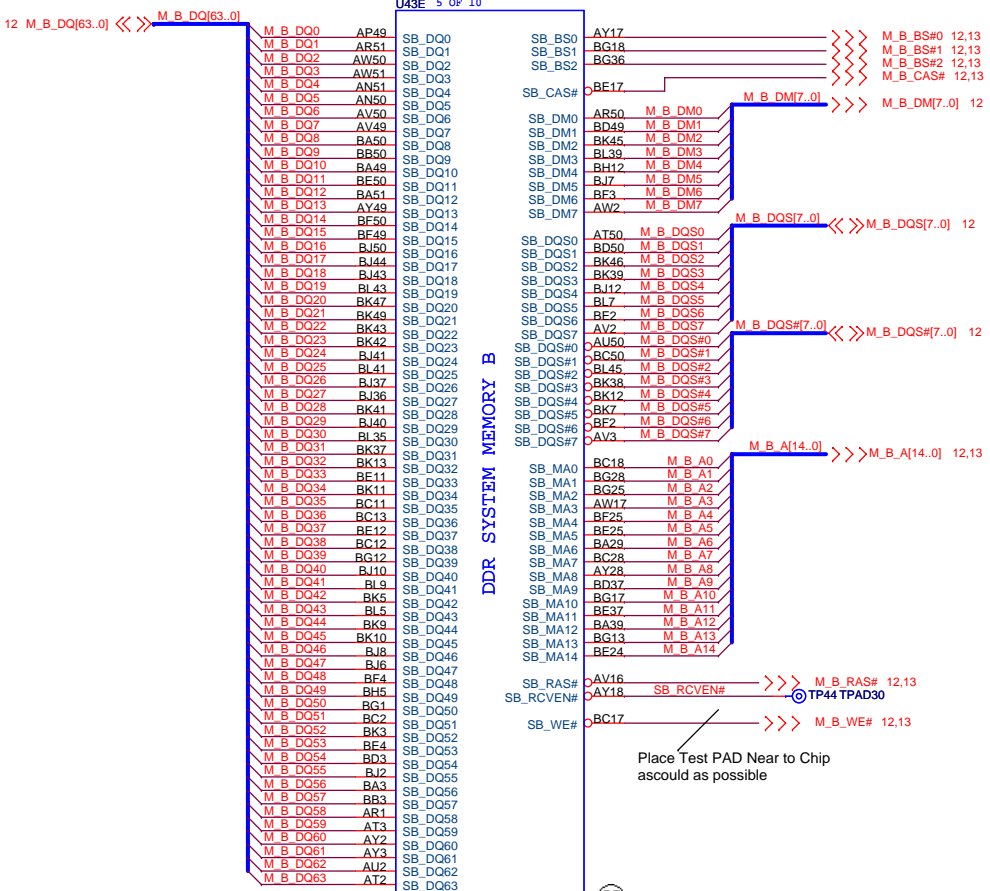
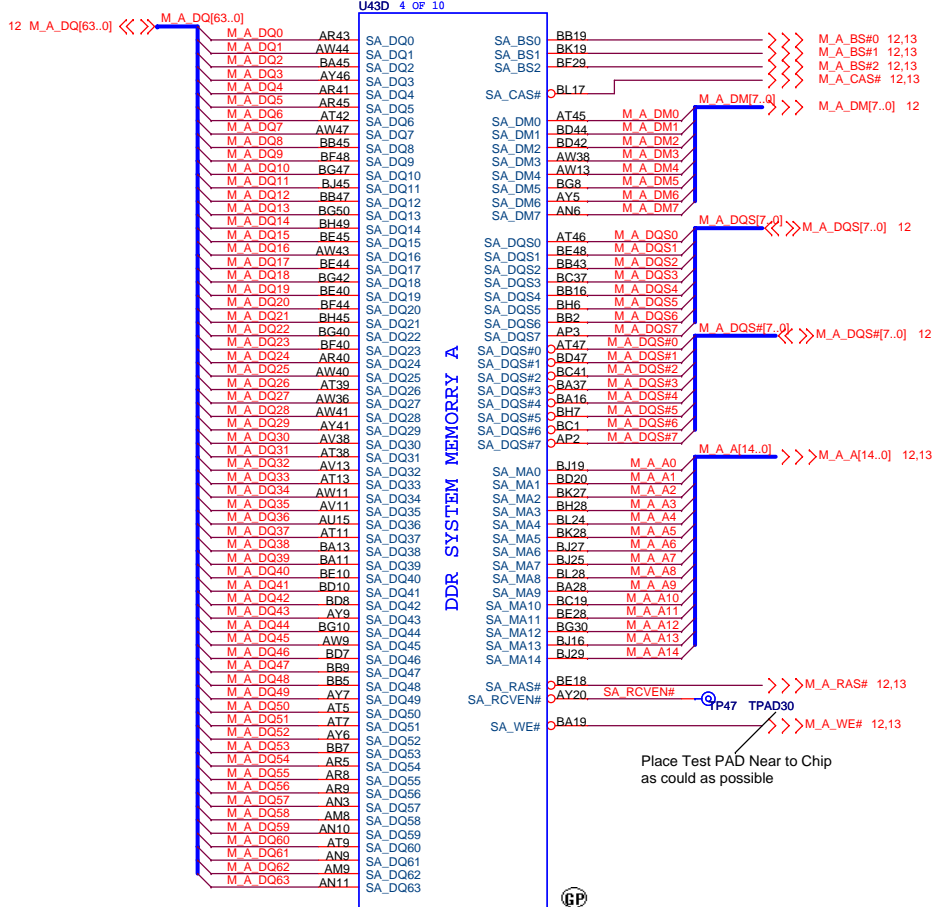
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Size	Document Number				Rev
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Date:	Wednesday, September 12, 2007	Sheet	6	of	39

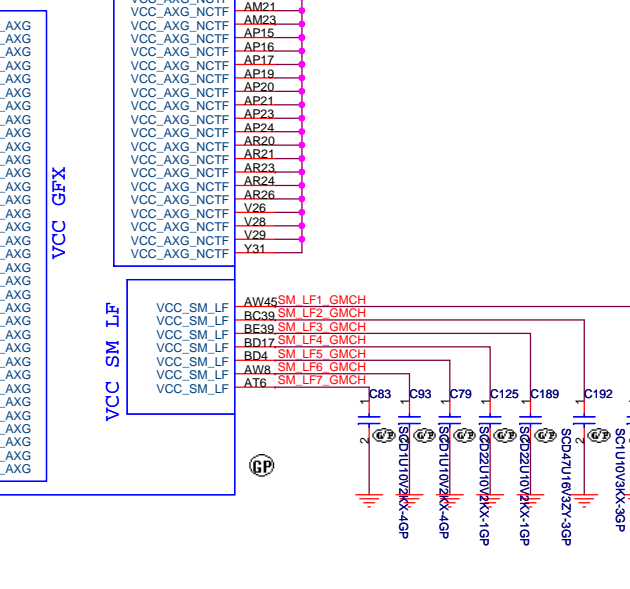
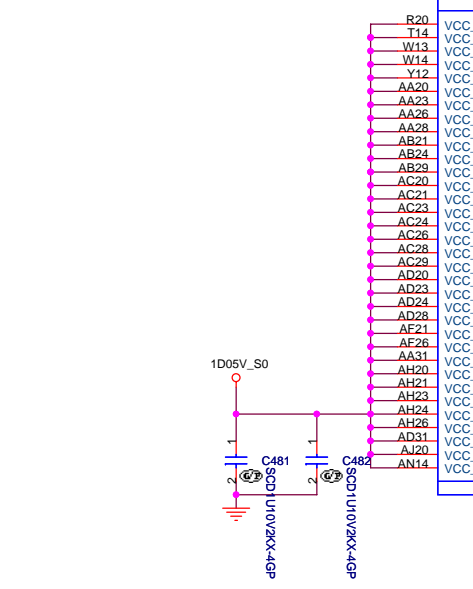
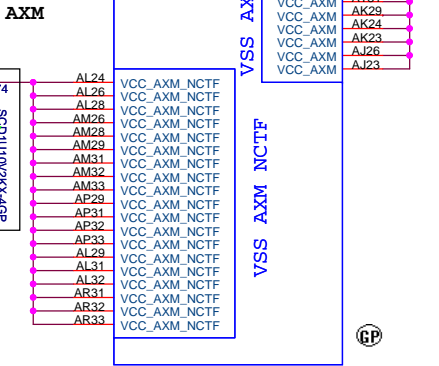
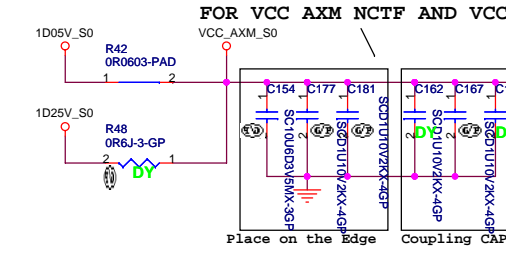
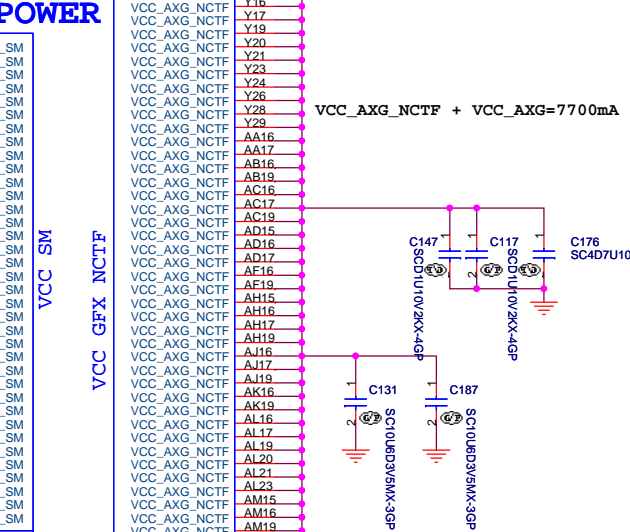
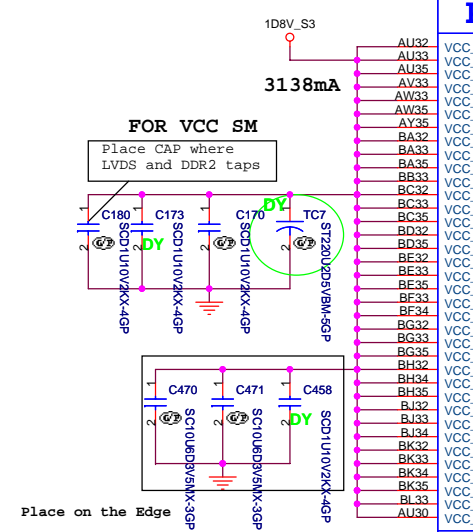
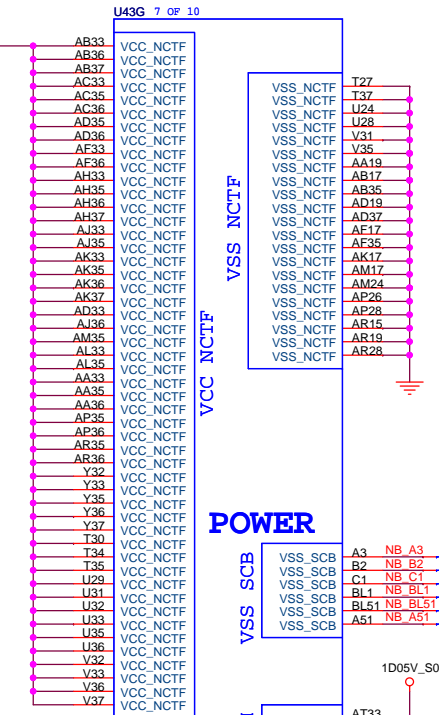
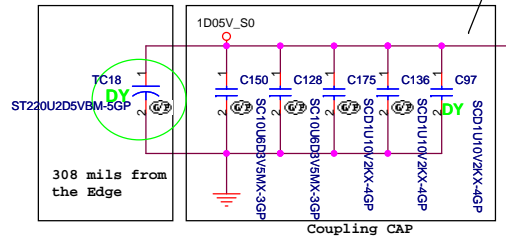
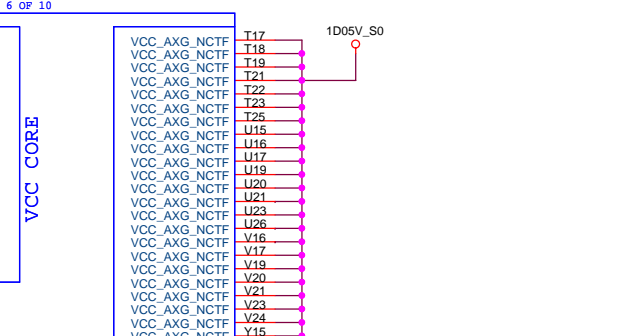
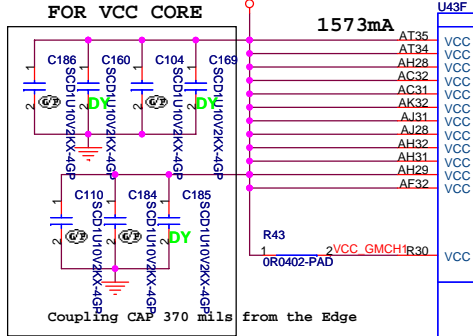


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Document Number	-1
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Date: Wednesday, September 12, 2007	Sheet 7 of 39

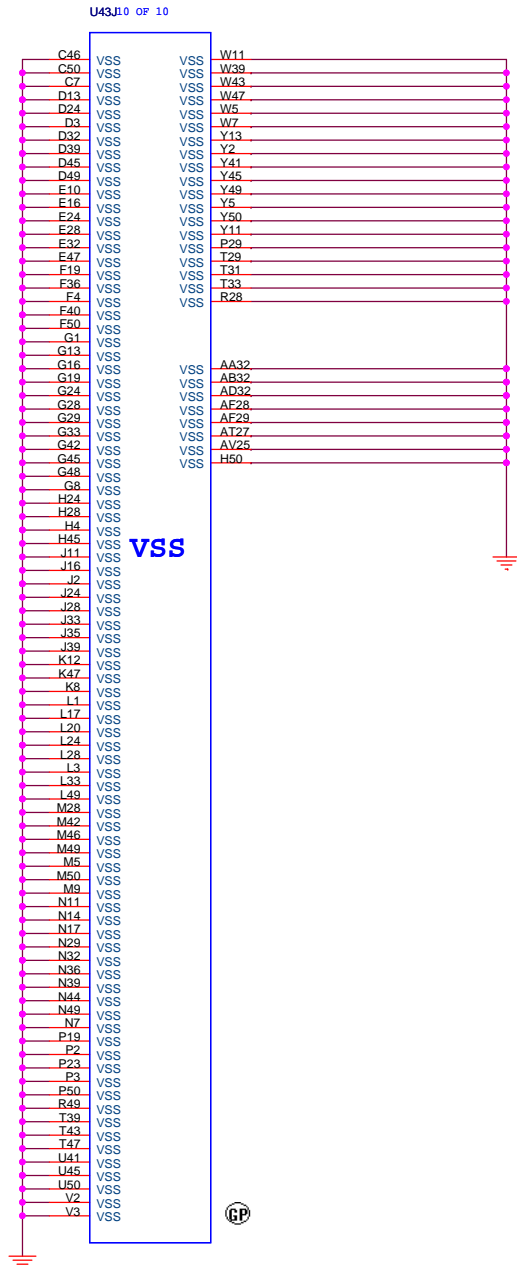
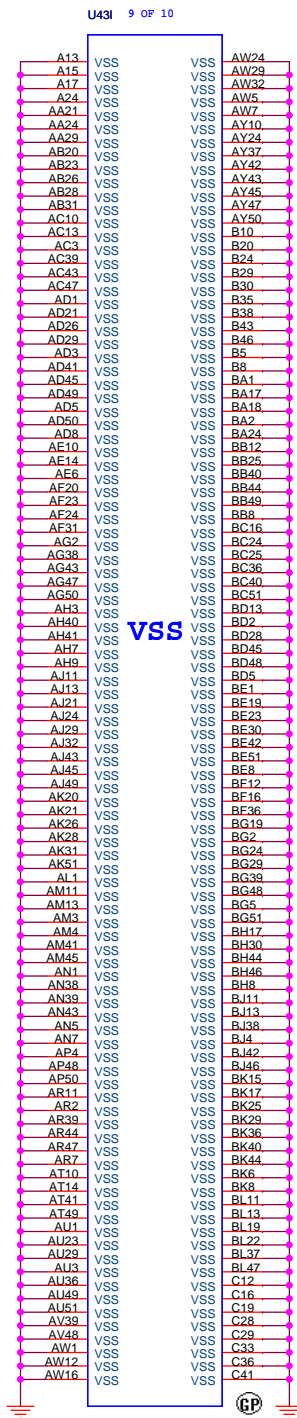


VCC_NCTF + VCC=1573mA

FOR VCC CORE AND VCC NCTF



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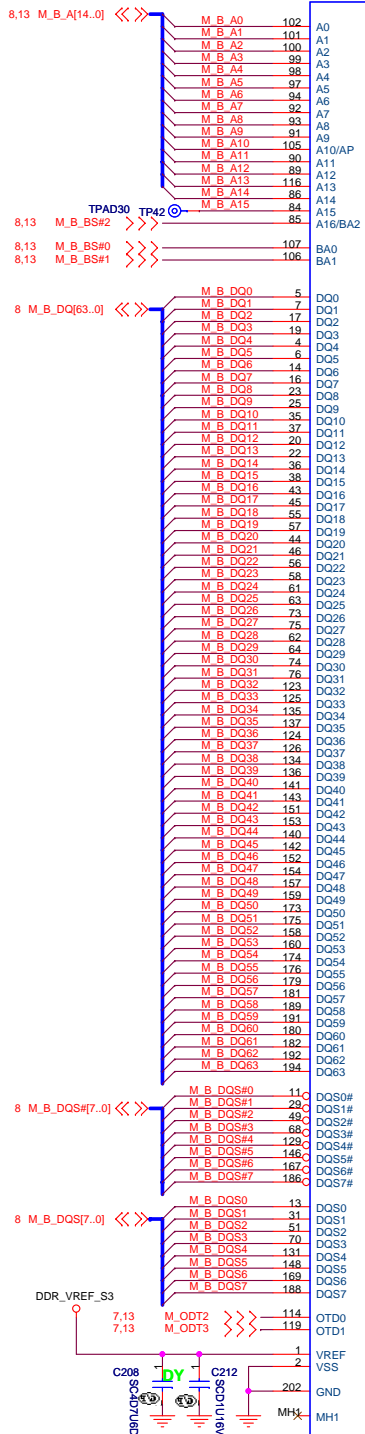


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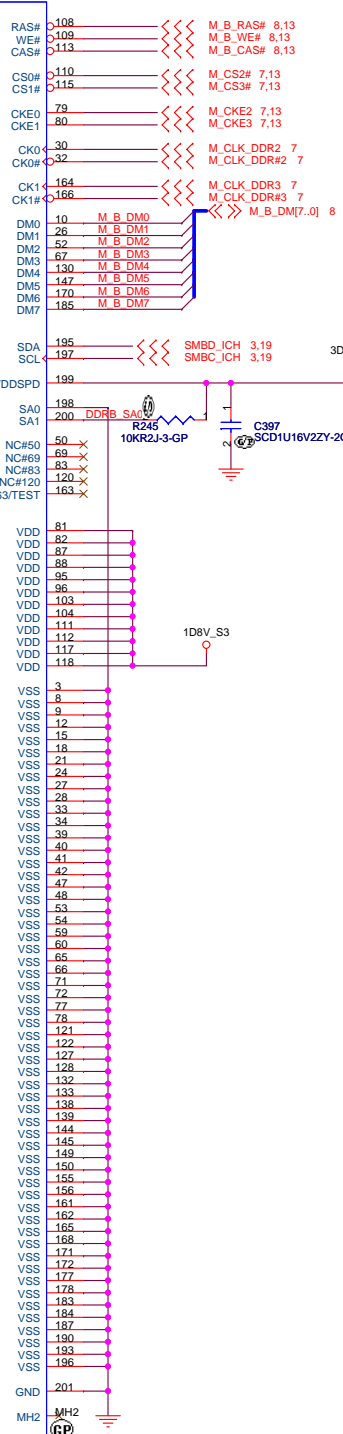
Size	Document Number	Rev
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Date: Monday, September 10, 2007 Sheet 11 of 39



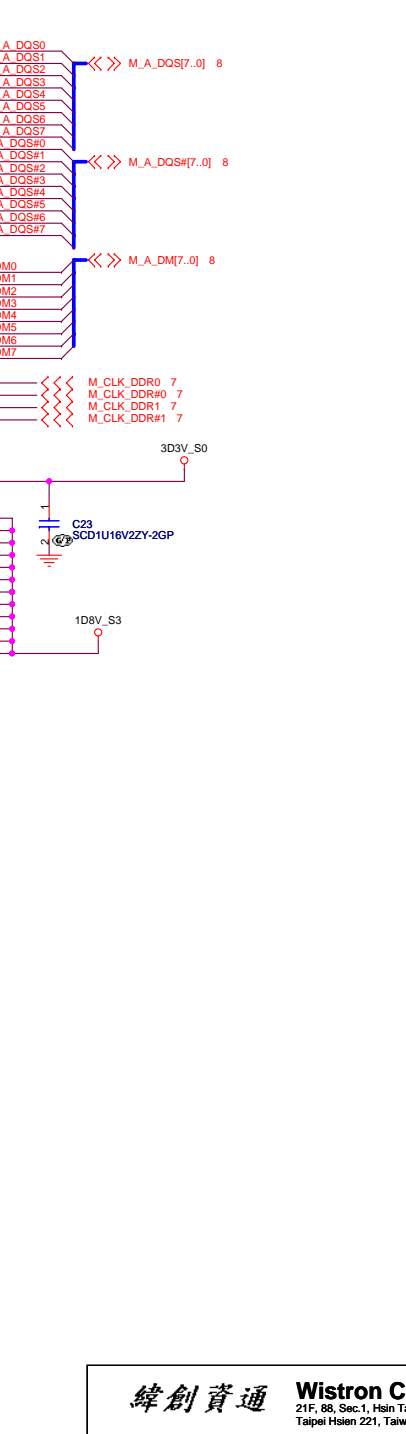
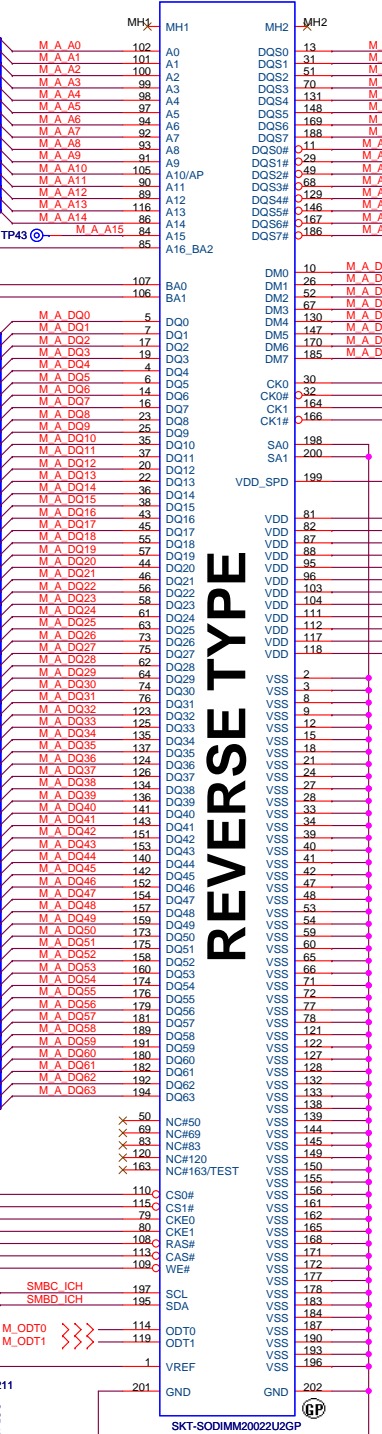
REVERSE TYPE

DDR2-200P-23-GP-U1
62.10017.A71
High 9.2mm



REVERSE TYPE

SKT-SODIMM2002U2GP
62.10017.691
High 5.2mm



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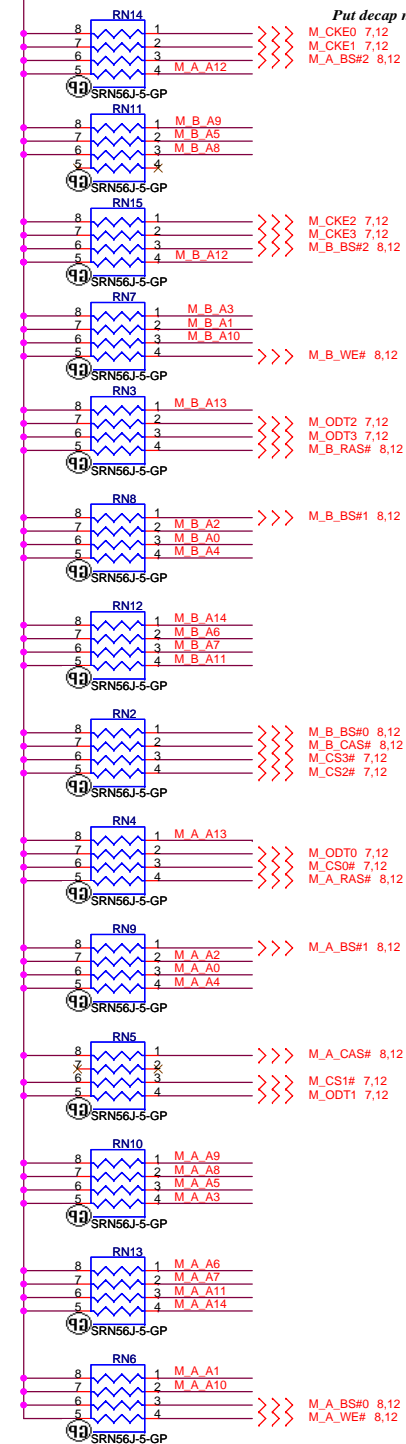
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Size	Document Number	Rev
	Calado	-1

Date: Wednesday, September 12, 2007 Sheet 12 of 39

PARALLEL TERMINATION

DDR_VREF_S0

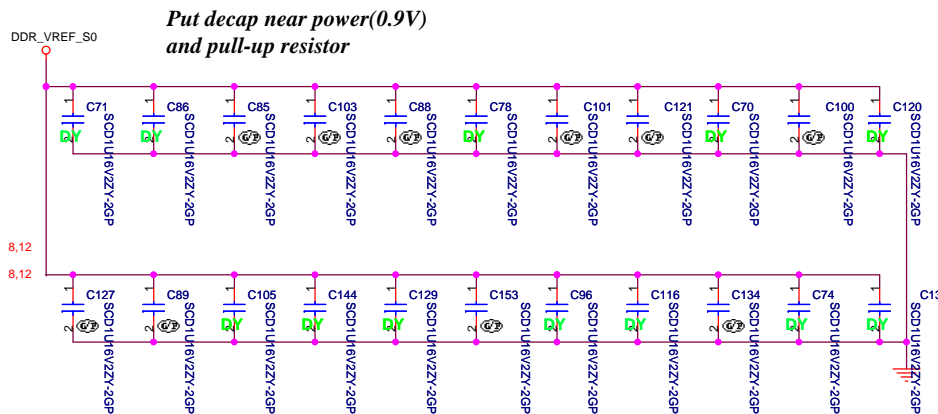


Put decap near power(0.9V) and pull-up resistor

M_A_A[14..0] <<> M_A_A[14..0] 8,12
M_B_A[14..0] <<> M_B_A[14..0] 8,12

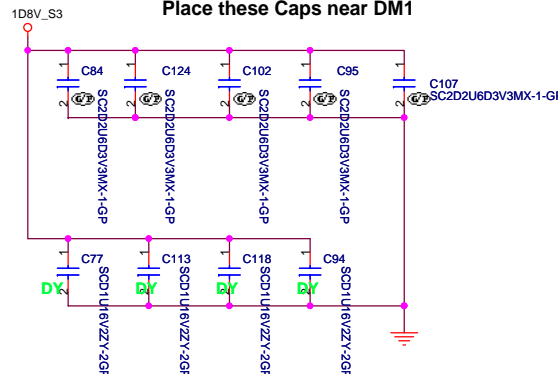
Decoupling Capacitor

DDR_VREF_S0

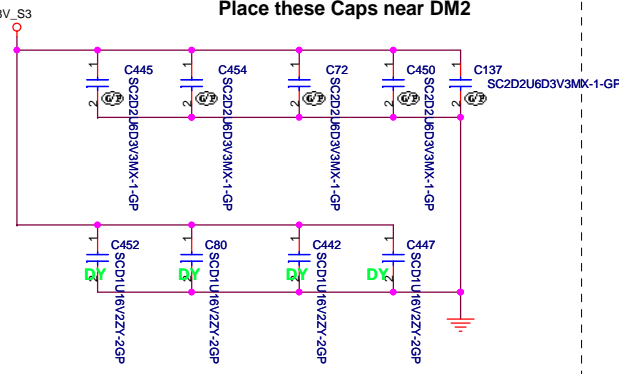


Put decap near power(0.9V) and pull-up resistor

Place these Caps near DM1



Place these Caps near DM2

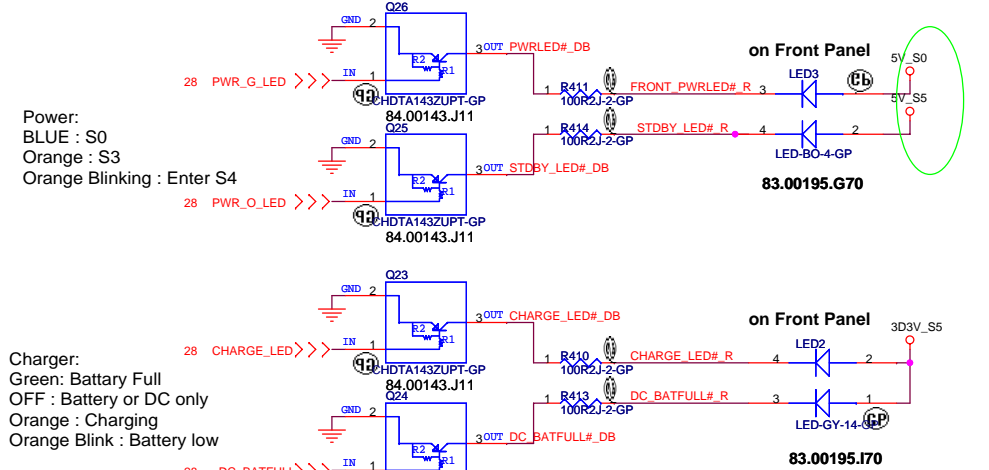
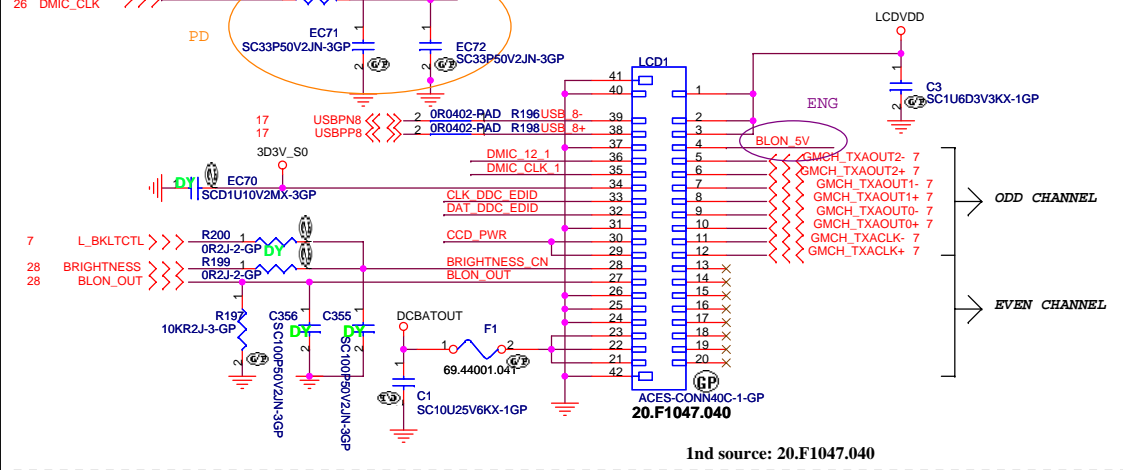


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Size	Document Number		Calado		Rev
					-1
Date:	Wednesday, September 12, 2007		Sheet	13	of 39

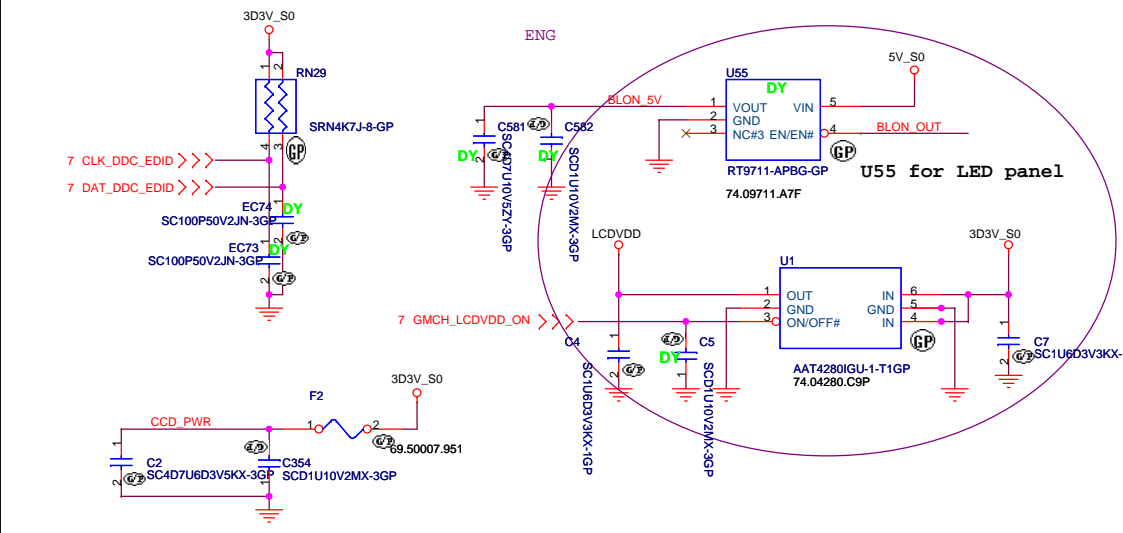
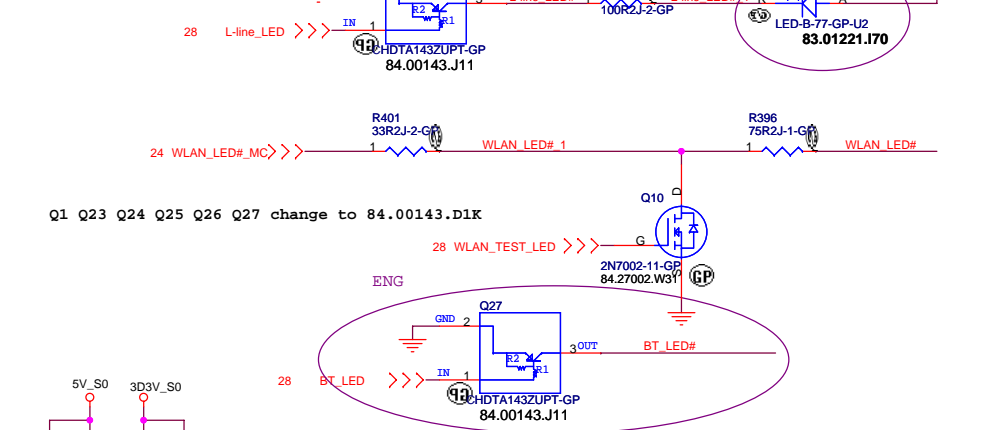
LCD/INVERTER CONN

LED

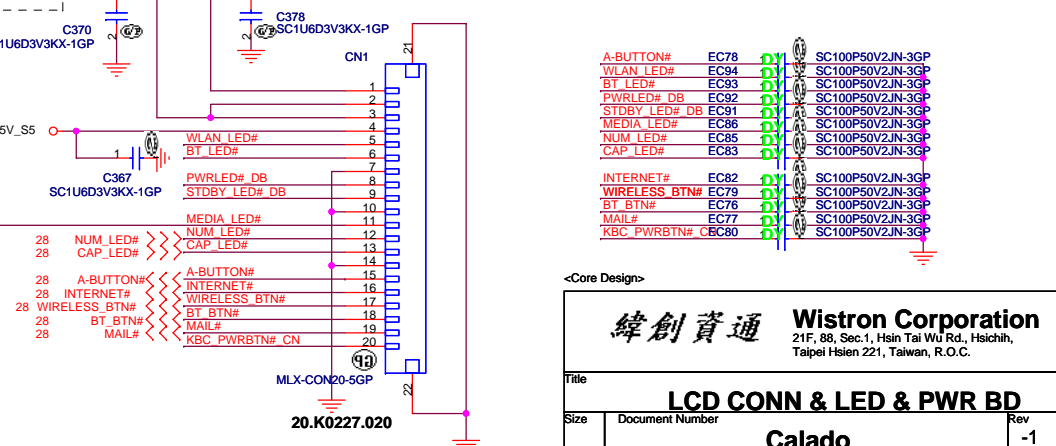
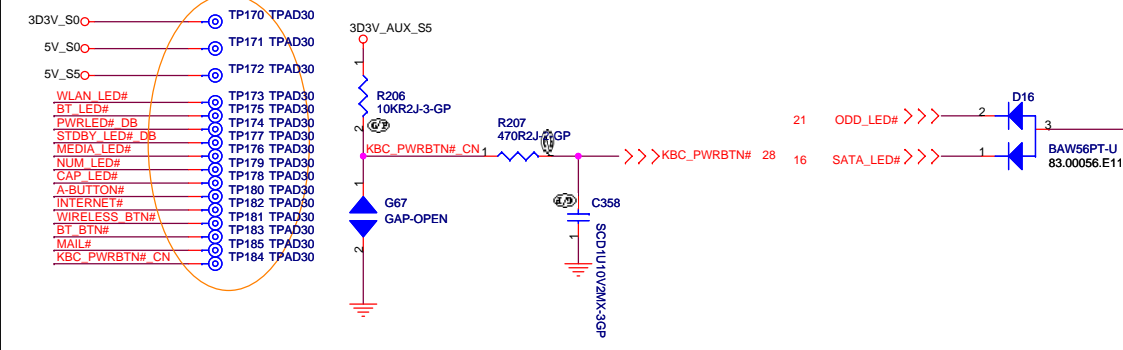


Power:
BLUE : S0
Orange : S3
Orange Blinking : Enter S4

Charger:
Green: Battery Full
OFF : Battery or DC only
Orange : Charging
Orange Blink : Battery low



PWR BD



<Core Design>

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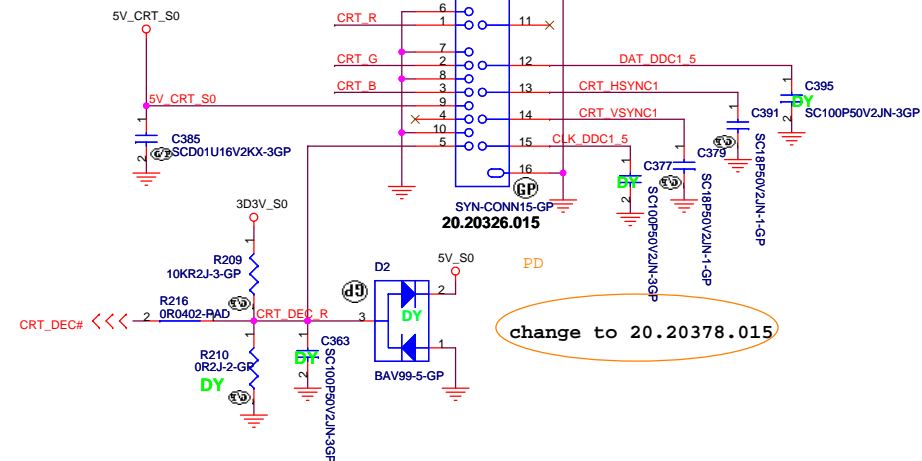
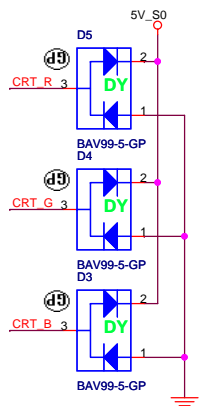
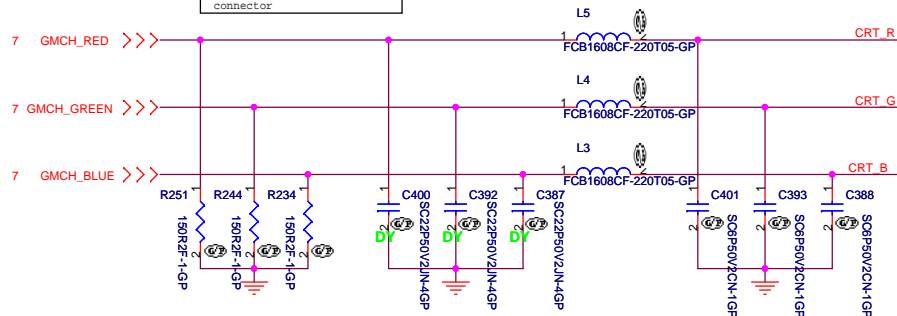
LCD CONN & LED & PWR BD

File _____
Size _____ Document Number _____ Rev -1
Date: Wednesday, September 12, 2007 Sheet 14 of 39

CRT I/F & CONNECTOR

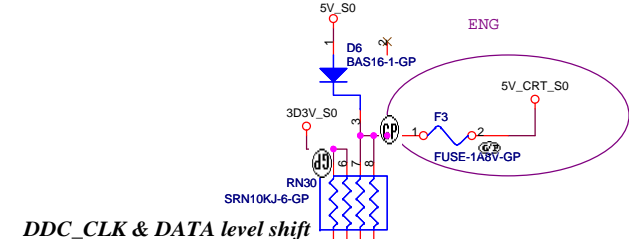
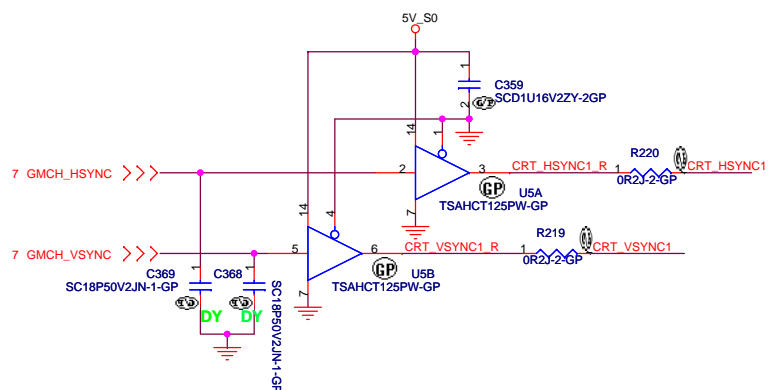
Layout Note:
Place these resistors
close to the CRT-out
connector

Ferrite bead impedance: 22 ohm@100MHz;
from 10 ohm change to 22 ohm for EMI

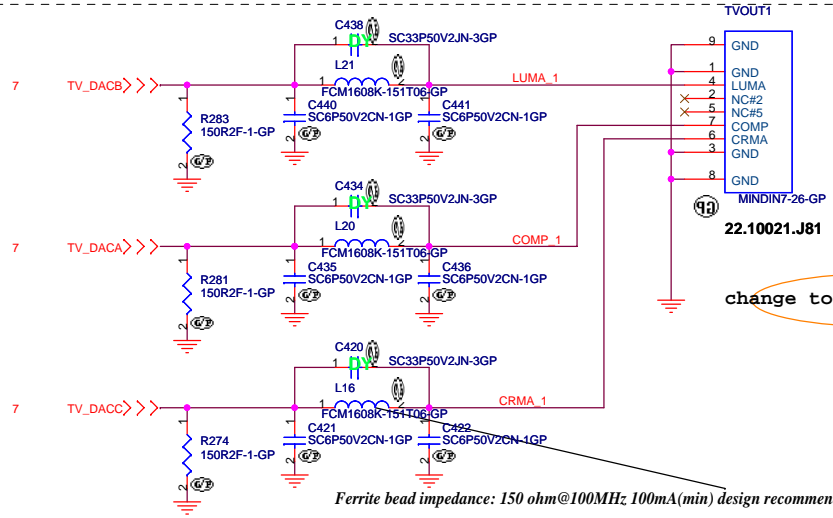


Layout Note:
* Must be a ground return path between this ground and the ground on
the VGA connector.
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT
CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

Hsync & Vsync level shift



TV CONN

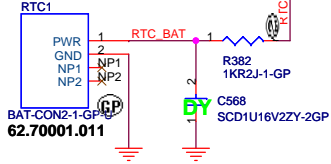


22.10021.J81
change to 22.10021.H61

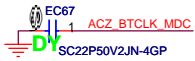
Ferrite bead impedance: 150 ohm@100MHz; 100mA(min) design recommend

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
CRT/TV Connector	
Size	Document Number
Calado	
Date: Thursday, September 13, 2007	Rev -1
Sheet 15	of 39

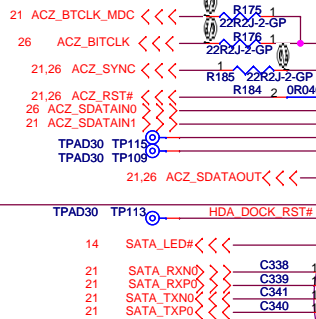
RTC circuitry



EMI capacitor



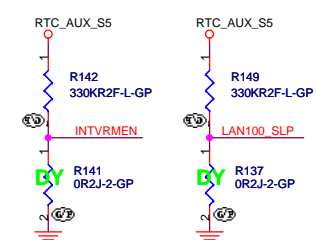
GLAN_COMP place within 500 mil of ICH8M



ENG

Place within 500 mils of ICH8 ball

Change to 24.9 1% ohm when use SATA HD



integrated VccSus1_05,VccSus1_5,VccCLL1_5		
INTVRMEN	High=Enable	Low=Disable
integrated VccLan1_05VccCLL1_05		
LAN100_SLP	High=Enable	Low=Disable

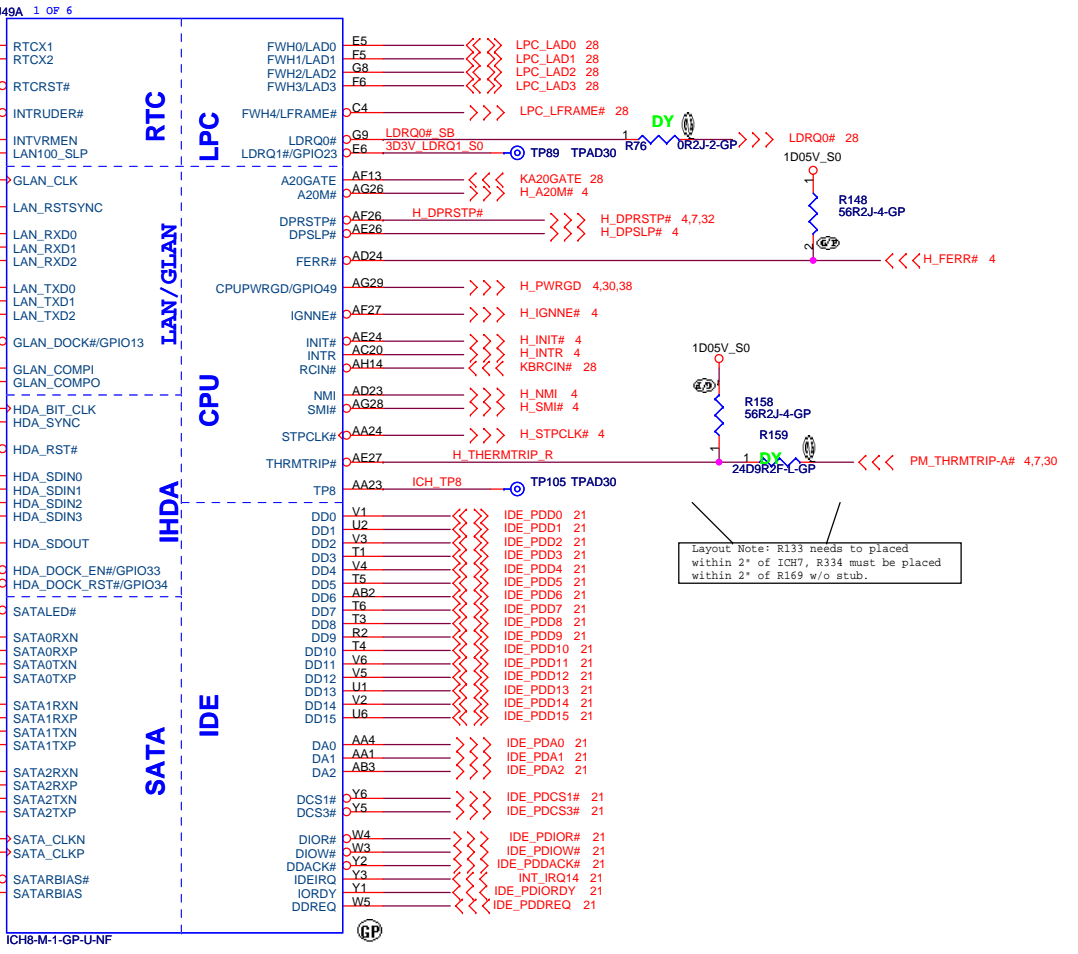
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

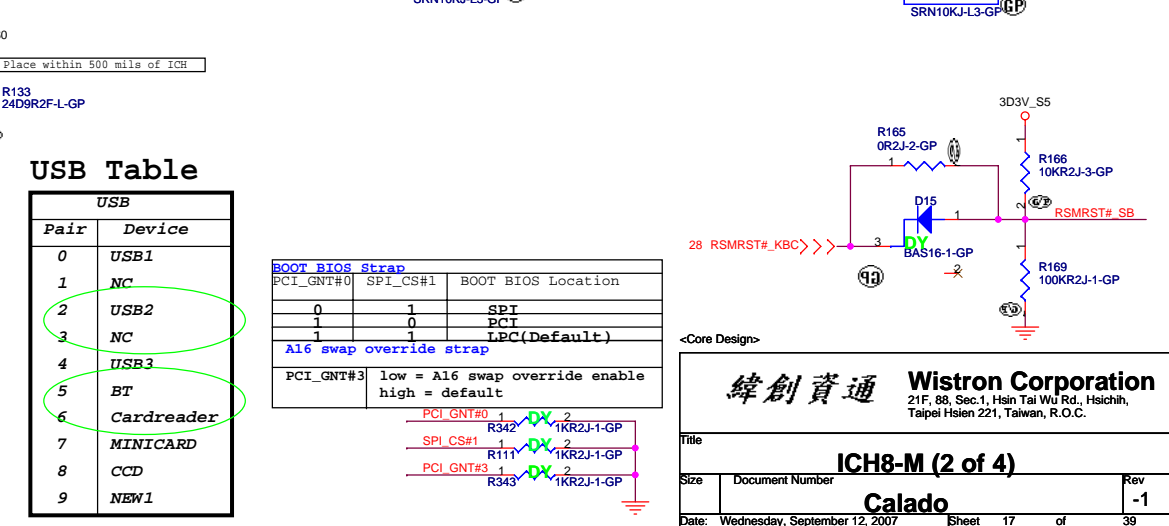
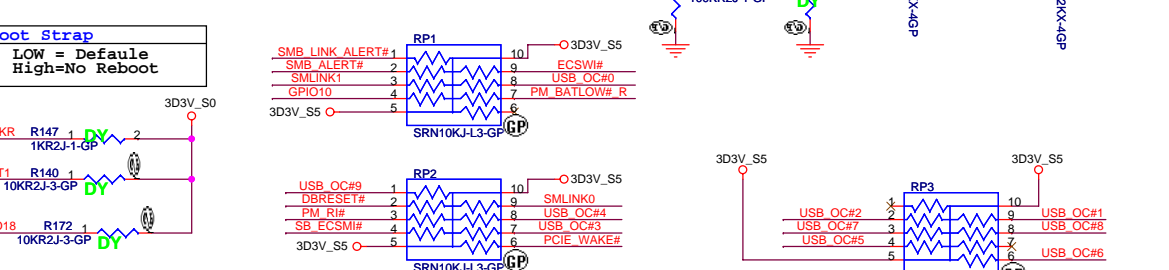
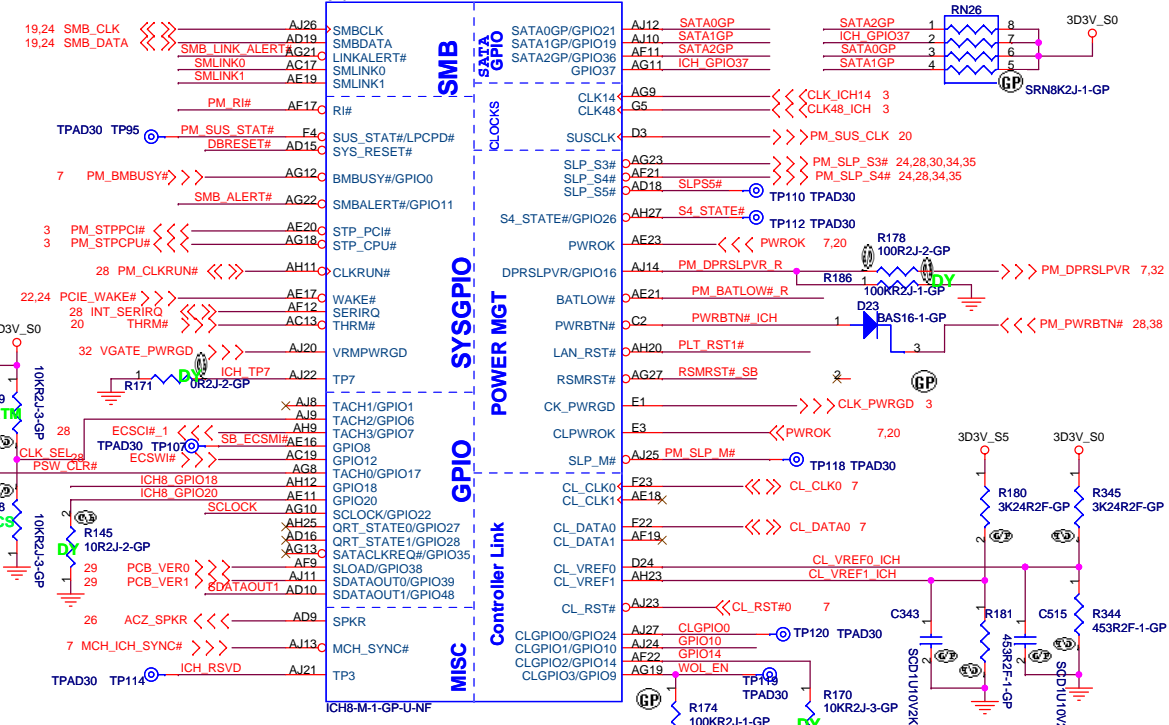
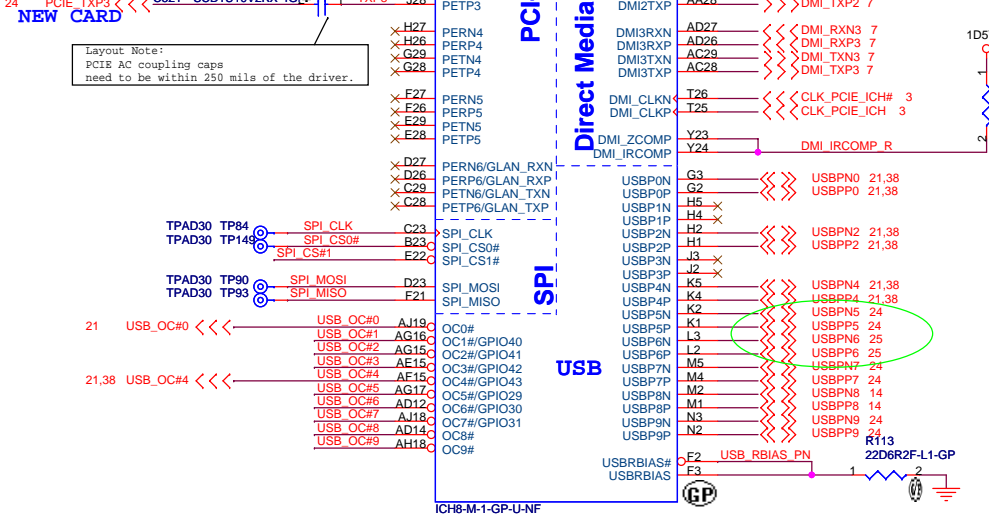
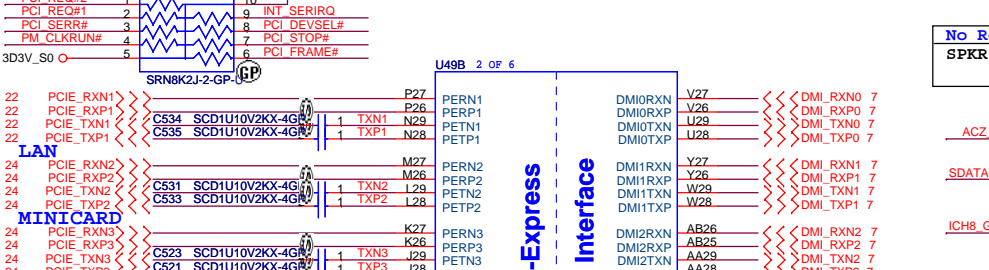
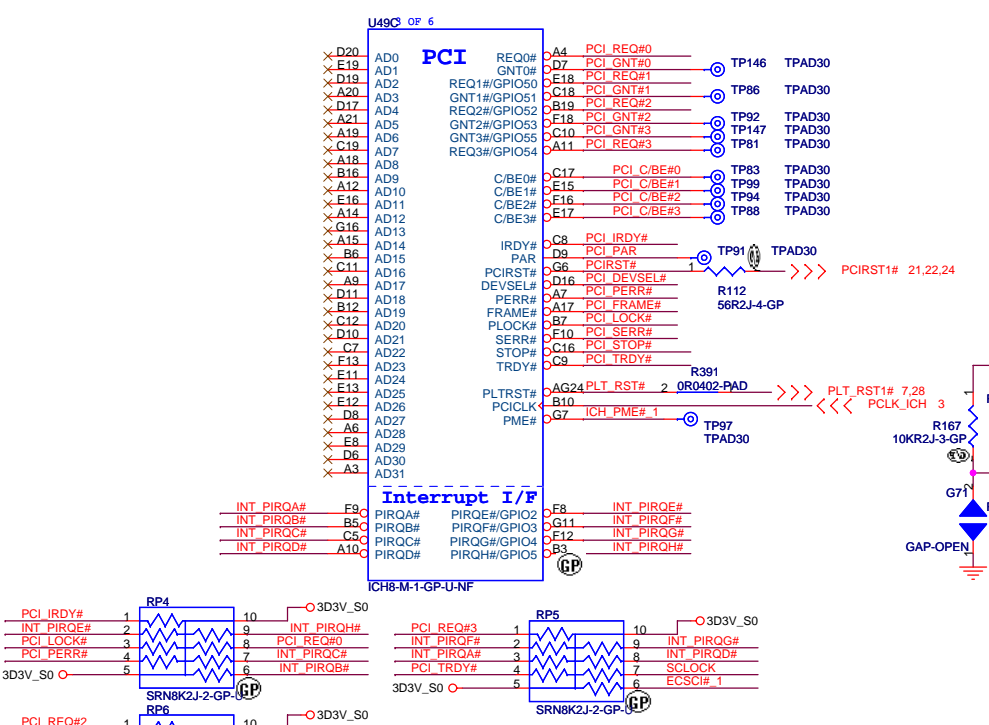
Title: **ICH8-M (1 of 4)**

Size: Document Number Rev: -1

Date: Wednesday, September 12, 2007 Sheet 16 of 39



Layout Note: R133 needs to be placed within 2" of ICH7, R334 must be placed within 2" of R169 w/o stub.



No Reboot Strap
SPKR LOW = Default High = No Reboot

USB Table

Pair	Device
0	USB1
1	NC
2	USB2
3	NC
4	USB3
5	BT
6	Cardreader
7	MINICARD
8	CCD
9	NEW1

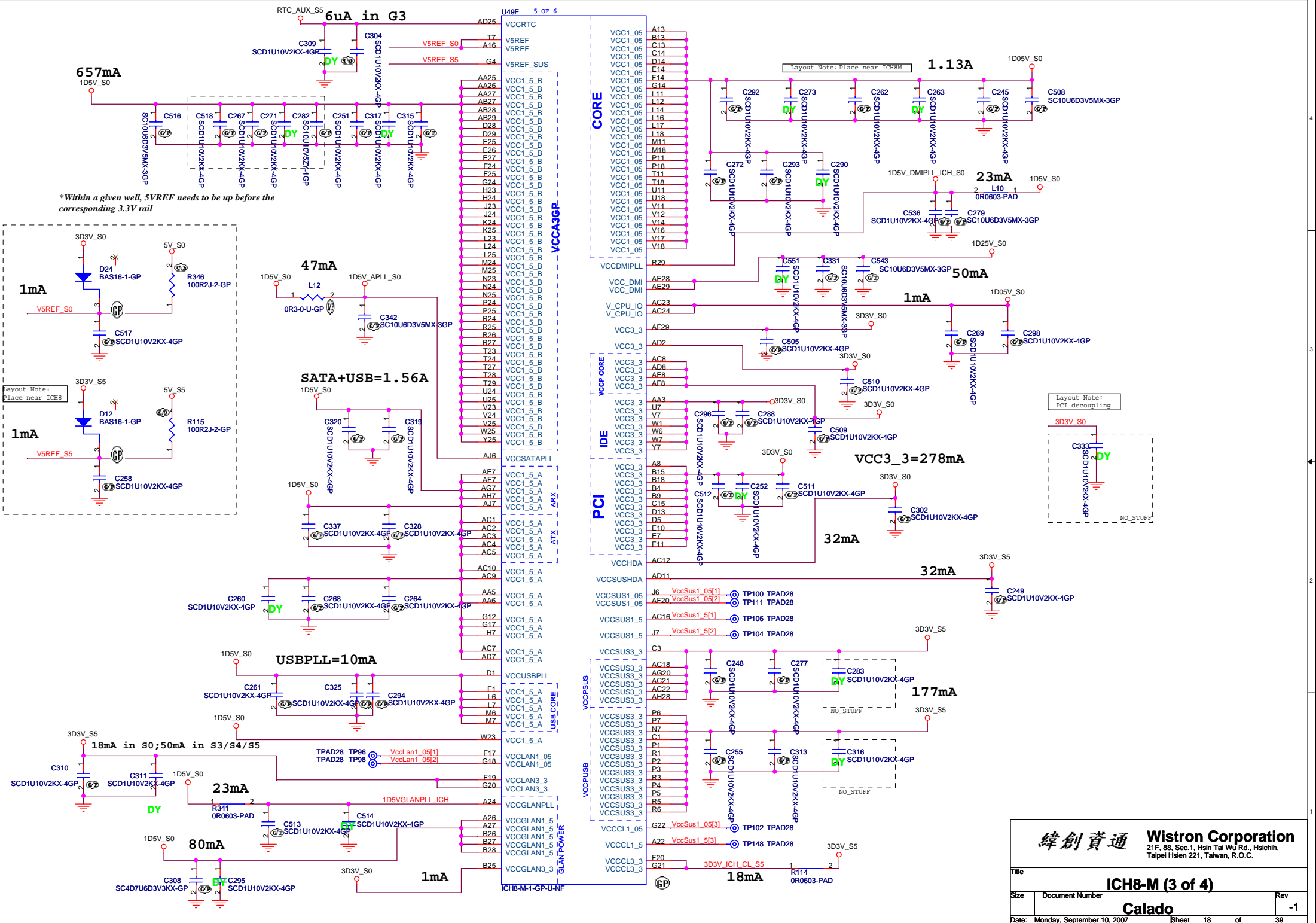
BOOT BIOS Strap			
PCI_GNT#0	SPI_CS#1	BOOT BIOS Location	
0	1	SPT	
1	0	PCI	
0	1	LPC(Default)	

A16 swap override strap
PCI_GNT#3 low = A16 swap override enable high = default

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ICH8-M (2 of 4)
Calado

File: _____
Size: _____ Document Number: _____ Rev: -1
Date: Wednesday, September 12, 2007 Sheet 17 of 39



*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail

Layout Note: Place near ICH8M

Layout Note: PCI decoupling

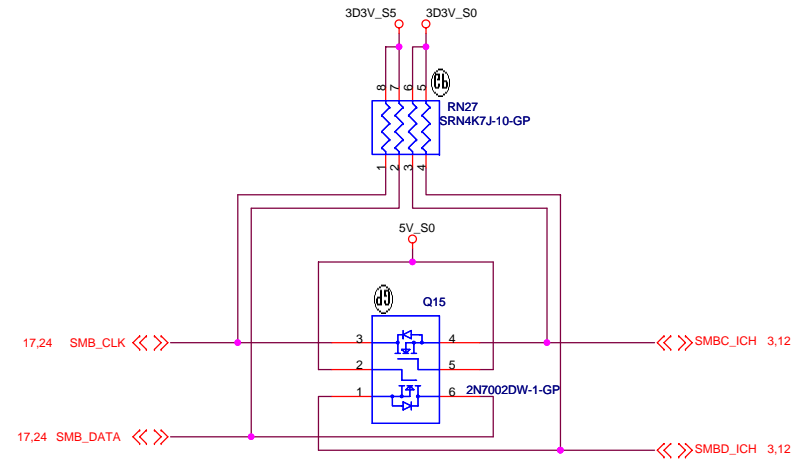
緯創資通 Wistron Corporation
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Title		
ICH8-M (3 of 4)		
Size	Document Number	Rev
		-1
Calado		
Date: Monday, September 10, 2007	Sheet 18 of	39

U49F 6 OF 6

A23	VSS	K7
A5	VSS	L1
AA2	VSS	L13
AA7	VSS	L15
A25	VSS	L26
AB1	VSS	L27
AB24	VSS	L4
AC11	VSS	L5
AC14	VSS	M12
AC25	VSS	M13
AC26	VSS	M14
AC27	VSS	M15
AD17	VSS	M16
AD20	VSS	M17
AD28	VSS	M23
AD29	VSS	M28
AD3	VSS	M29
AD4	VSS	M3
AD6	VSS	N1
AE1	VSS	N11
AE12	VSS	N12
AE2	VSS	N13
AE22	VSS	N14
AD1	VSS	N15
AE25	VSS	N16
AE5	VSS	N17
AE6	VSS	N18
AE9	VSS	N26
AF14	VSS	N27
AF16	VSS	N4
AF18	VSS	N5
AF3	VSS	N6
AF4	VSS	P12
AG5	VSS	P13
AG6	VSS	P14
AH10	VSS	P15
AH13	VSS	P16
AH16	VSS	P17
AH19	VSS	P23
AH2	VSS	P28
AE28	VSS	P29
AH22	VSS	R11
AH24	VSS	R12
AH26	VSS	R13
AH3	VSS	R14
AH4	VSS	R15
AH8	VSS	R16
AJ5	VSS	R17
B11	VSS	R18
B14	VSS	R28
B17	VSS	R4
B2	VSS	T12
B20	VSS	T13
B22	VSS	T14
B3	VSS	T15
C24	VSS	T16
C26	VSS	T17
C27	VSS	T2
C6	VSS	U12
D12	VSS	U13
D15	VSS	U14
D18	VSS	U15
D2	VSS	U16
D4	VSS	U17
E21	VSS	U23
E24	VSS	U26
E4	VSS	U27
E9	VSS	U3
F15	VSS	U5
E23	VSS	V13
F28	VSS	V15
F29	VSS	V28
F7	VSS	V29
G1	VSS	W2
E2	VSS	W26
G10	VSS	W27
G13	VSS	Y28
G19	VSS	Y29
G23	VSS	Y4
G25	VSS	AB4
G26	VSS	AB23
G27	VSS	AB5
H25	VSS	AB6
H28	VSS	AD5
H29	VSS	U4
H3	VSS	W24
H6	VSS	
J1	VSS	A1 SB A1 TP143TPAD30
J25	VSS_NCTF	A2 SB A2 TP144TPAD30
J26	VSS_NCTF	A28 SB A28 TP150TPAD30
J27	VSS_NCTF	A29 SB A29 TP151TPAD30
J4	VSS_NCTF	AJ28 SB AJ28 TP116TPAD30
J5	VSS_NCTF	AH1 SB AH1 TP159TPAD30
K23	VSS_NCTF	AH29 SB AH29 TP117TPAD30
K28	VSS_NCTF	AJ1 SB AJ1 TP160TPAD30
K29	VSS_NCTF	AJ2 SB AJ2 TP161TPAD30
K3	VSS_NCTF	AJ29 SB AJ29 TP121TPAD30
K6	VSS_NCTF	B1 SB B1 TP145TPAD30
	VSS_NCTF	B29 SB B29 TP152TPAD30

ICH8-M-1-GP-U-NF



Q12 connect SMLINK and SMBUS in S) for SMBus 2.0 compliance

SMBUS

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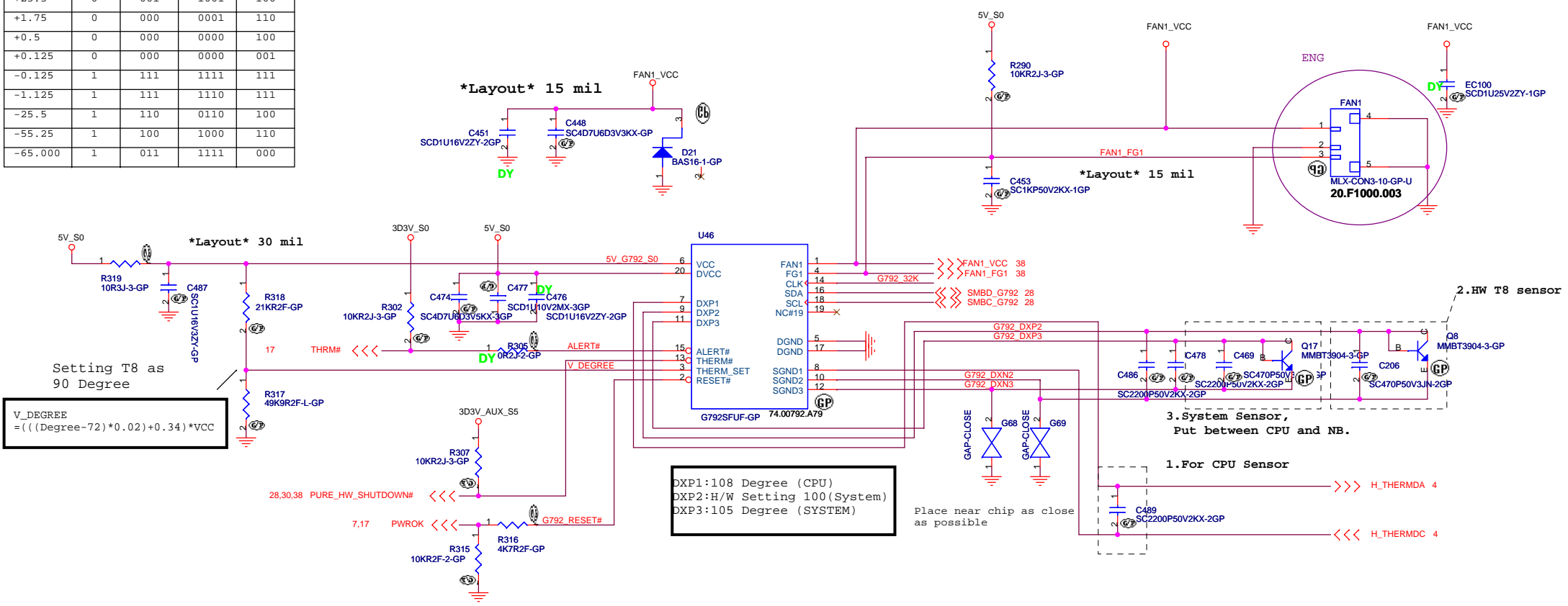
Title: ICH8-M (4 of 4)

Size: Document Number: Calado

Date: Wednesday, September 12, 2007 Sheet 19 of 39

Rev: -1

TEMP.	Digital Output Data Bits			
	Sign	MSB	LSB	EXT
+127.875	0	111	1111	111
+126.375	0	111	1110	011
+25.5	0	001	1001	100
+1.75	0	000	0001	110
+0.5	0	000	0000	100
+0.125	0	000	0000	001
-0.125	1	111	1111	111
-1.125	1	111	1110	111
-25.5	1	110	0110	100
-55.25	1	100	1000	110
-65.000	1	011	1111	000

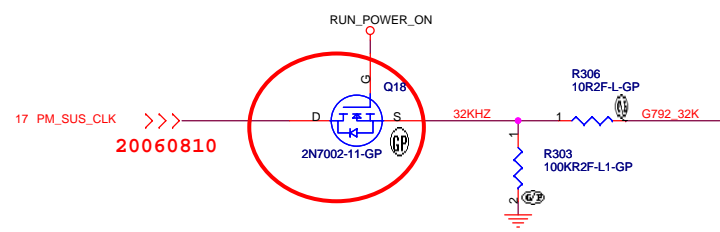


Setting T8 as 90 Degree

$$V_DEGREE = (((Degree - 72) * 0.02) + 0.34) * VCC$$

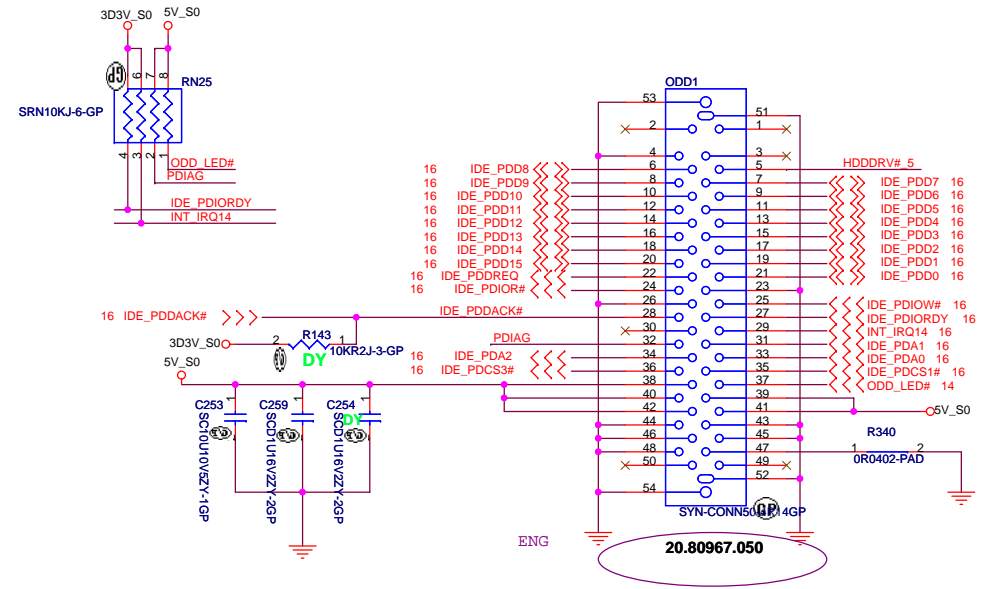
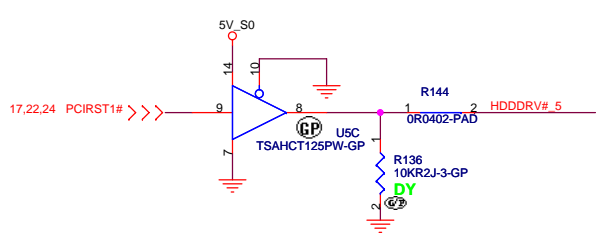
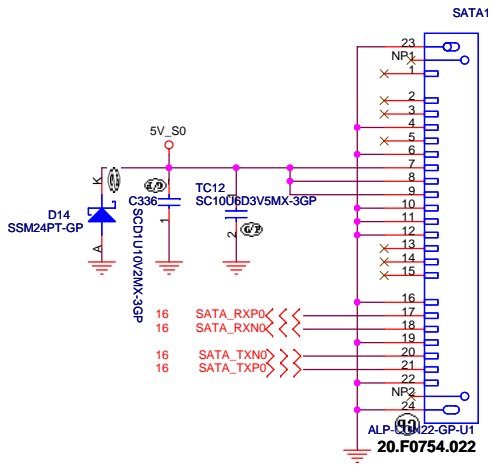
DXP1:108 Degree (CPU)
 DXP2:H/W Setting 100(System)
 DXP3:105 Degree (SYSTEM)

32K suspend clock output

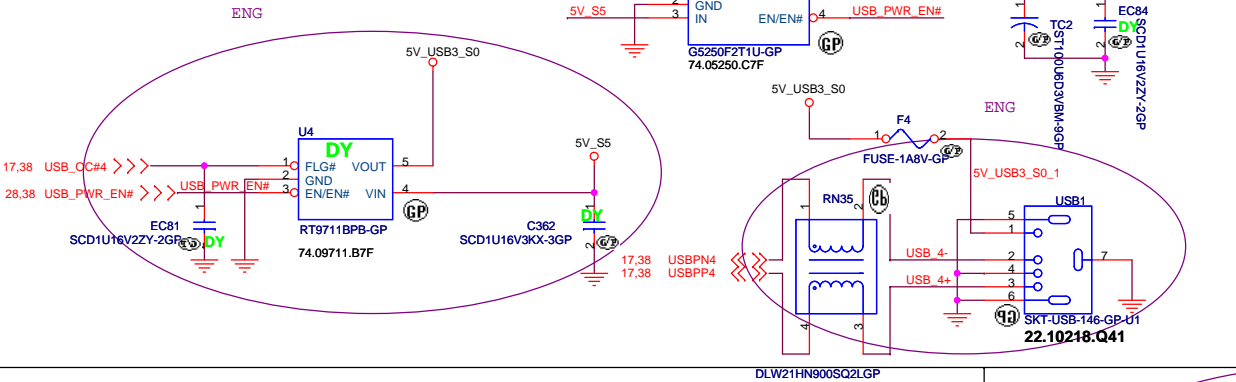


SATA HD Connector

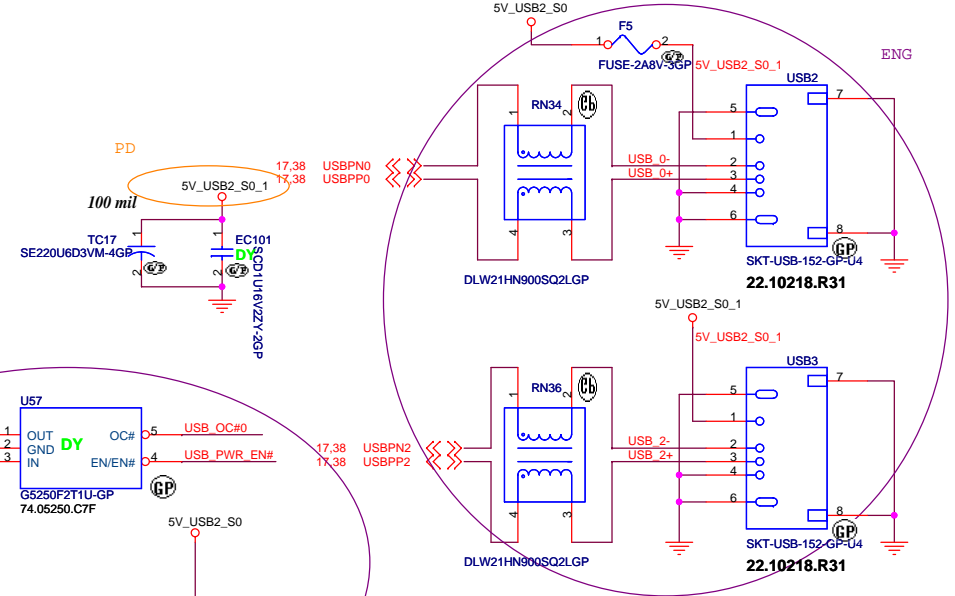
ODD Connector



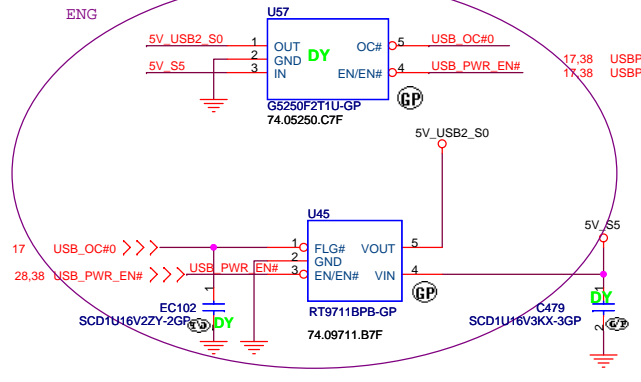
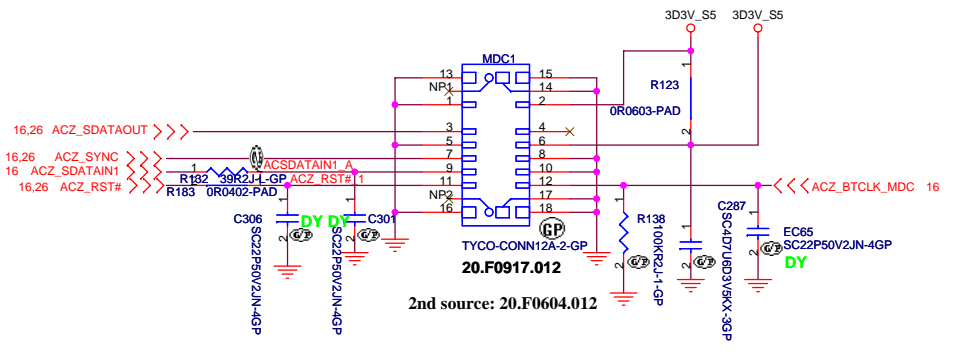
USB On Board CONN(RIGHT)

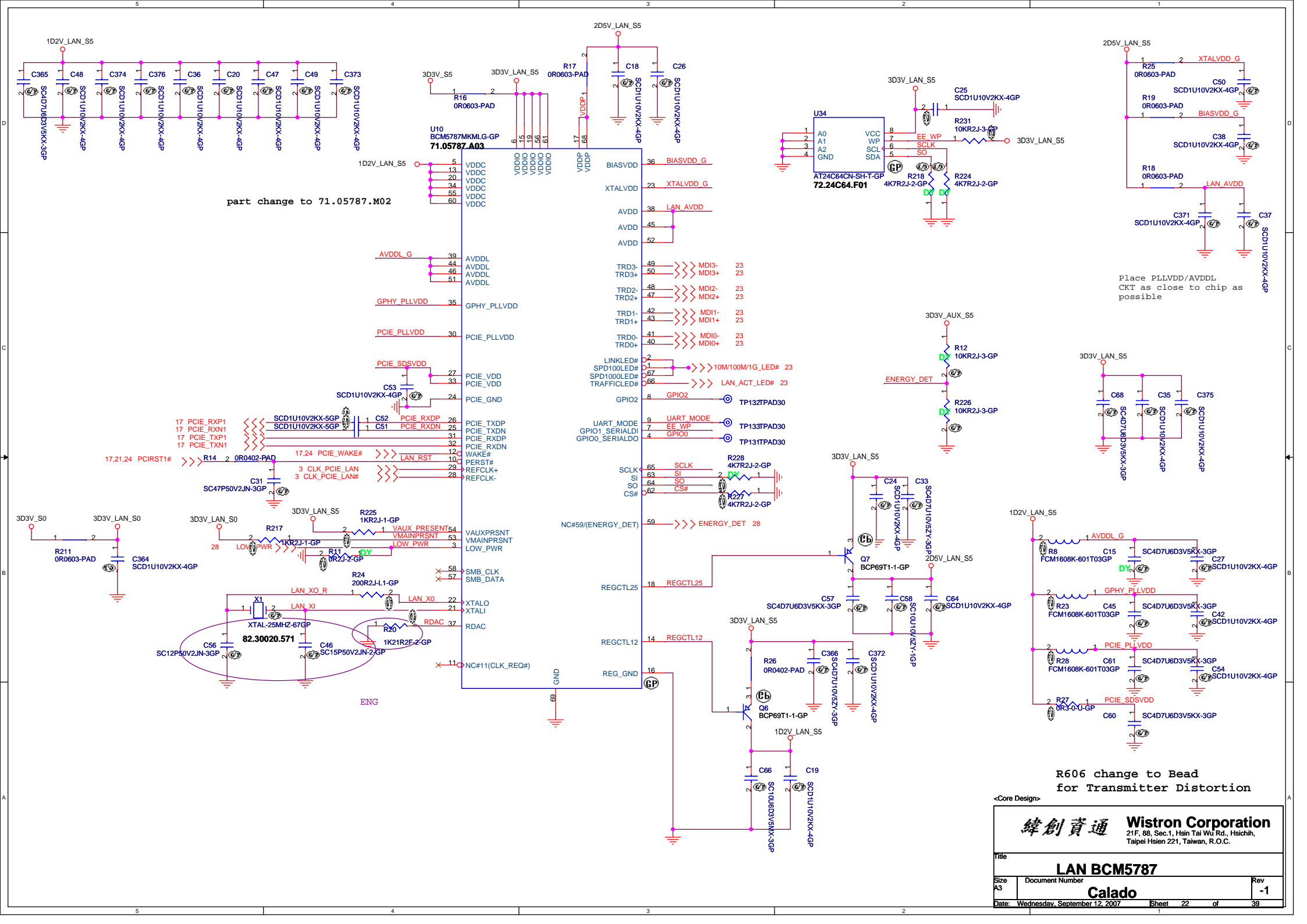


USB On Board CONN(LEFT)



MDC 1.5 CONN





part change to 71.05787.M02

Place PLLVDD/AVDDL CKT as close to chip as possible

R606 change to Bead for Transmitter Distortion

<Core Design>

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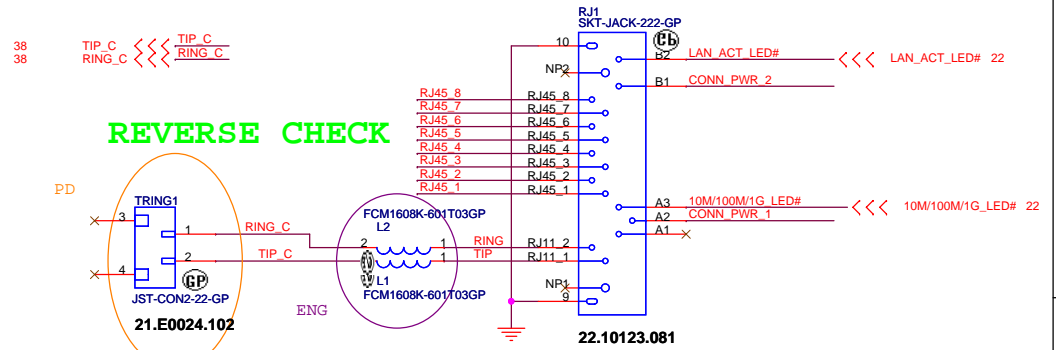
Title: LAN BCM5787

Size A3 Document Number Calado Rev -1

Date: Wednesday, September 12, 2007 Sheet 22 of 39

Voltage Rail	4401E	5789	5787
VDDIO_PCI	3D3V_LAN_S5	3D3V_S0	Don't Care
VDDC	1D8V_LAN_S5	1D2V_LAN_S5	
VDDIO	3D3V_LAN_S5	3D3V_LAN_S5	
VESD	3D3V_LAN_S5	3D3V_S0	Don't Care
VDDP	Don't Care	2D5V_S5	
3D3V_2D5V_S5	3D3V_S5	2D5V_S5	
1D8V_1D2V_S5	1D8V_LAN_S5	1D2V_S5	

LAN Connector

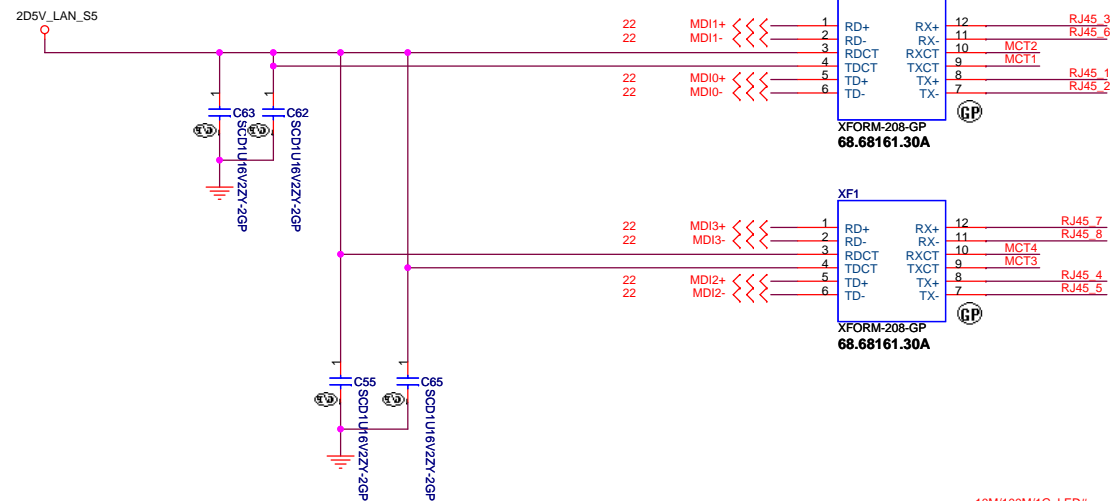


REVERSE CHECK

A3: Green
B2: YELLOW

LAN Link: Green(A3), behavior is the same for 10/100/1000 bits
LAN Data: Yellow(B2), when LAN is transferring data.

GIGA Lan Transformer

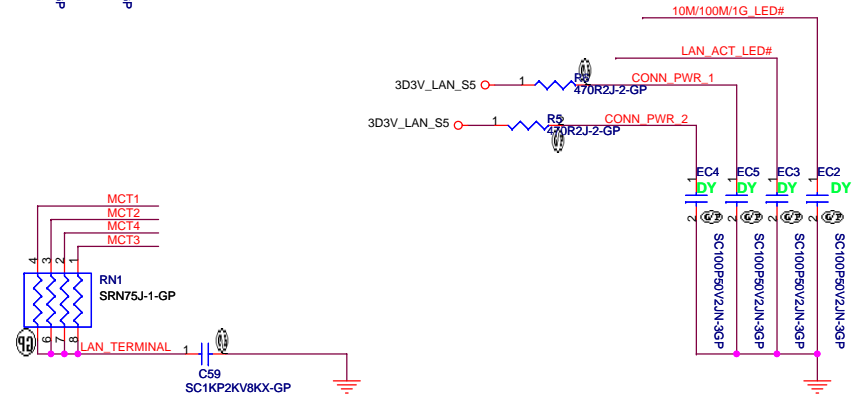


- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width, 12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat, except RJ-45 moat.

RJ11 signal must leave the other signal or power plane 100mil.

DOC_TIP,DOC_RING,TIP,RING:
W/S : 10/100 @ Surface layers
10/20 @ Inner layers

10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6



<Core Design>

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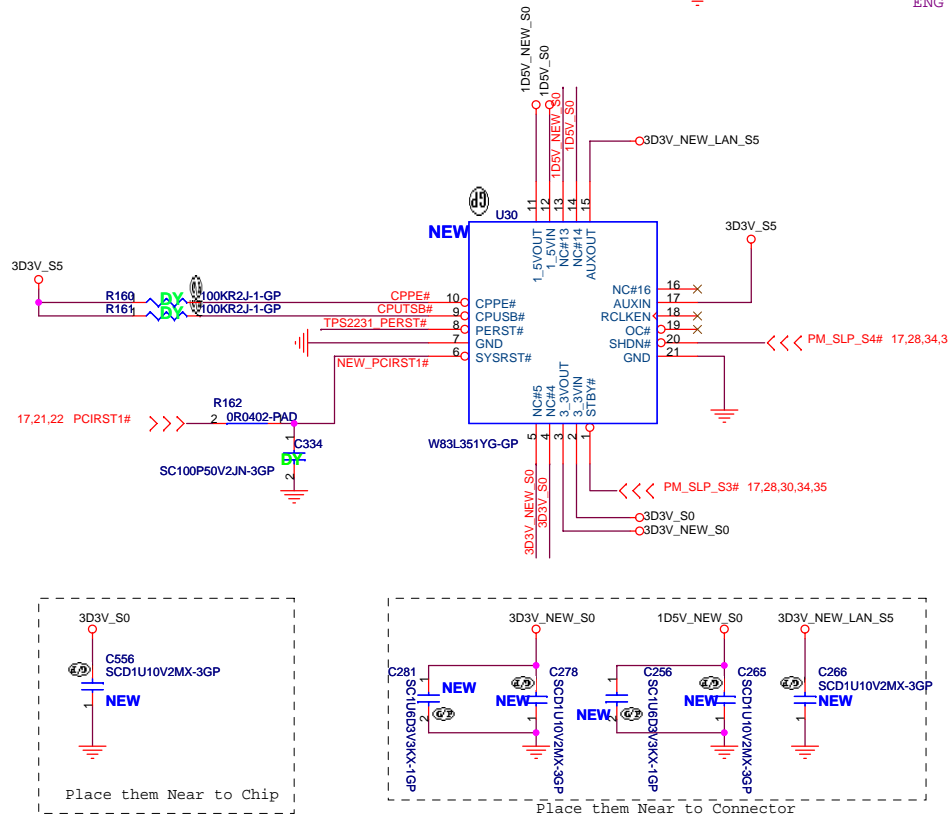
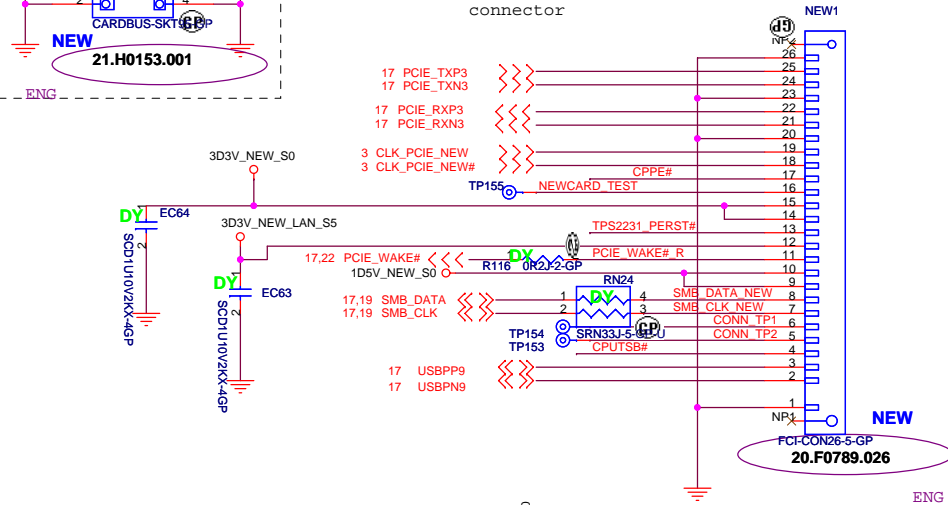
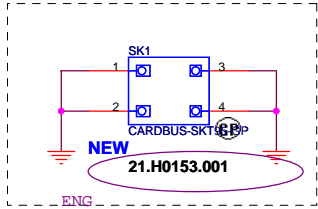
Title: **LAN Connector**

Size A3 Document Number **Calado** Rev -1

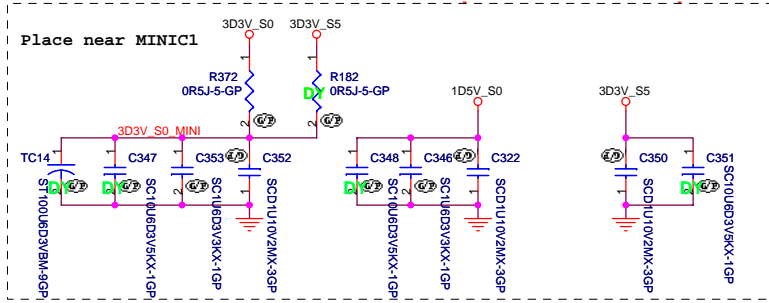
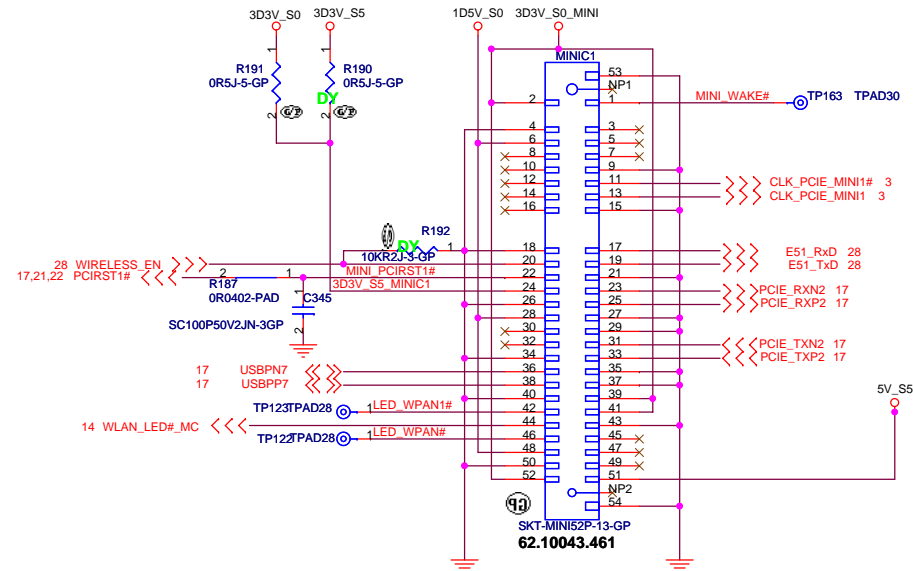
Date: Wednesday, September 12, 2007 Sheet 23 of 39

NEWCARD Connector

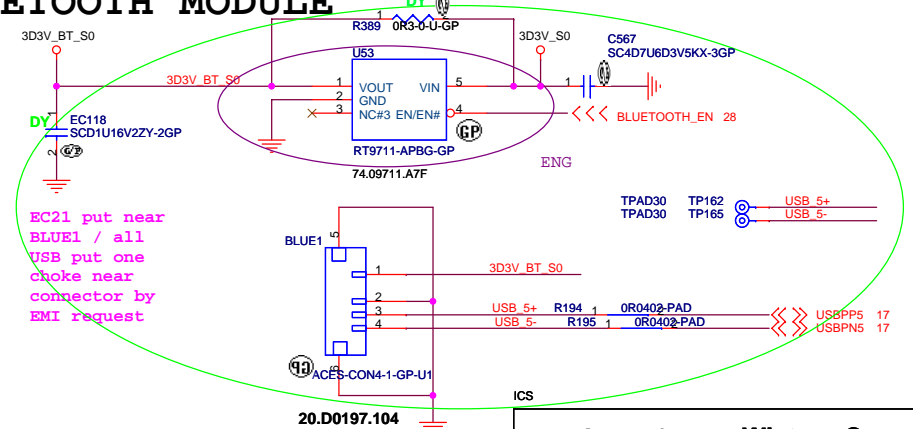
Reserve the symbol for bottom side connector



Mini Card Connector

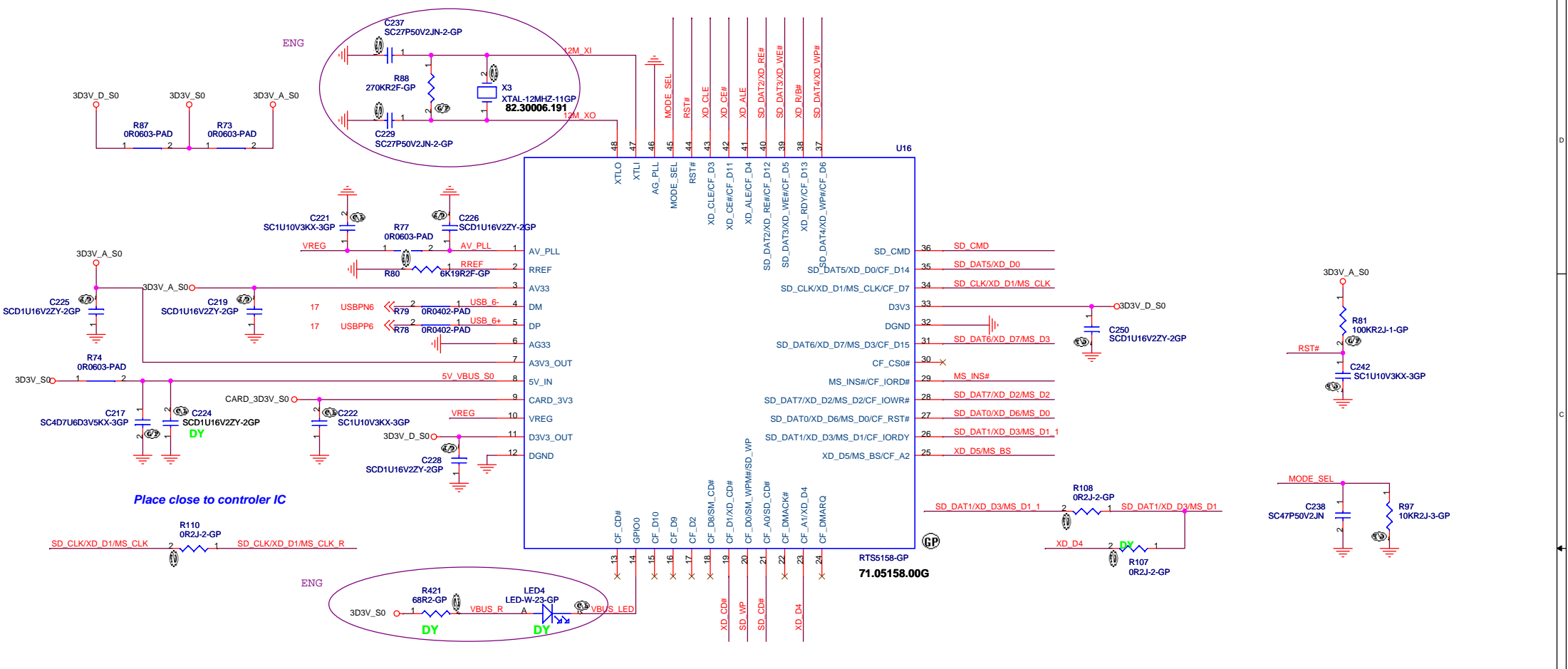


BLUETOOTH MODULE

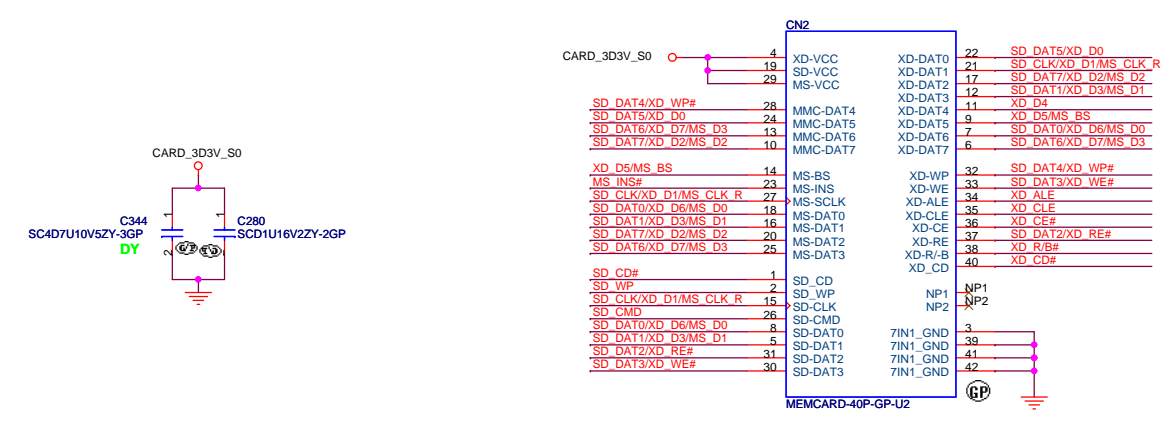


1st source: 20.D0197.104
2nd source: 20.F0984.004

Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: MINI CARD / NEW CARD/BT	
Size:	Document Number
Calado	
Date: Wednesday, September 12, 2007	Sheet 24 of 39



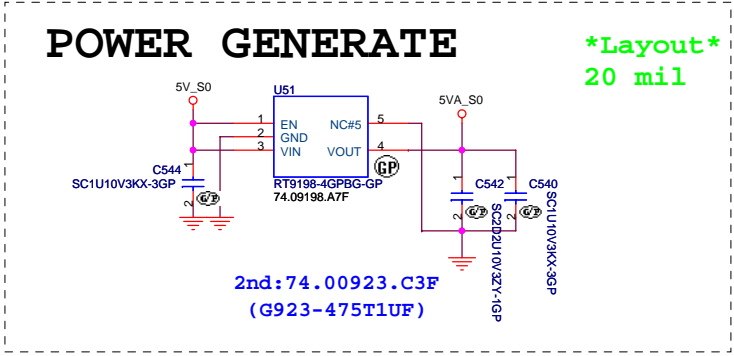
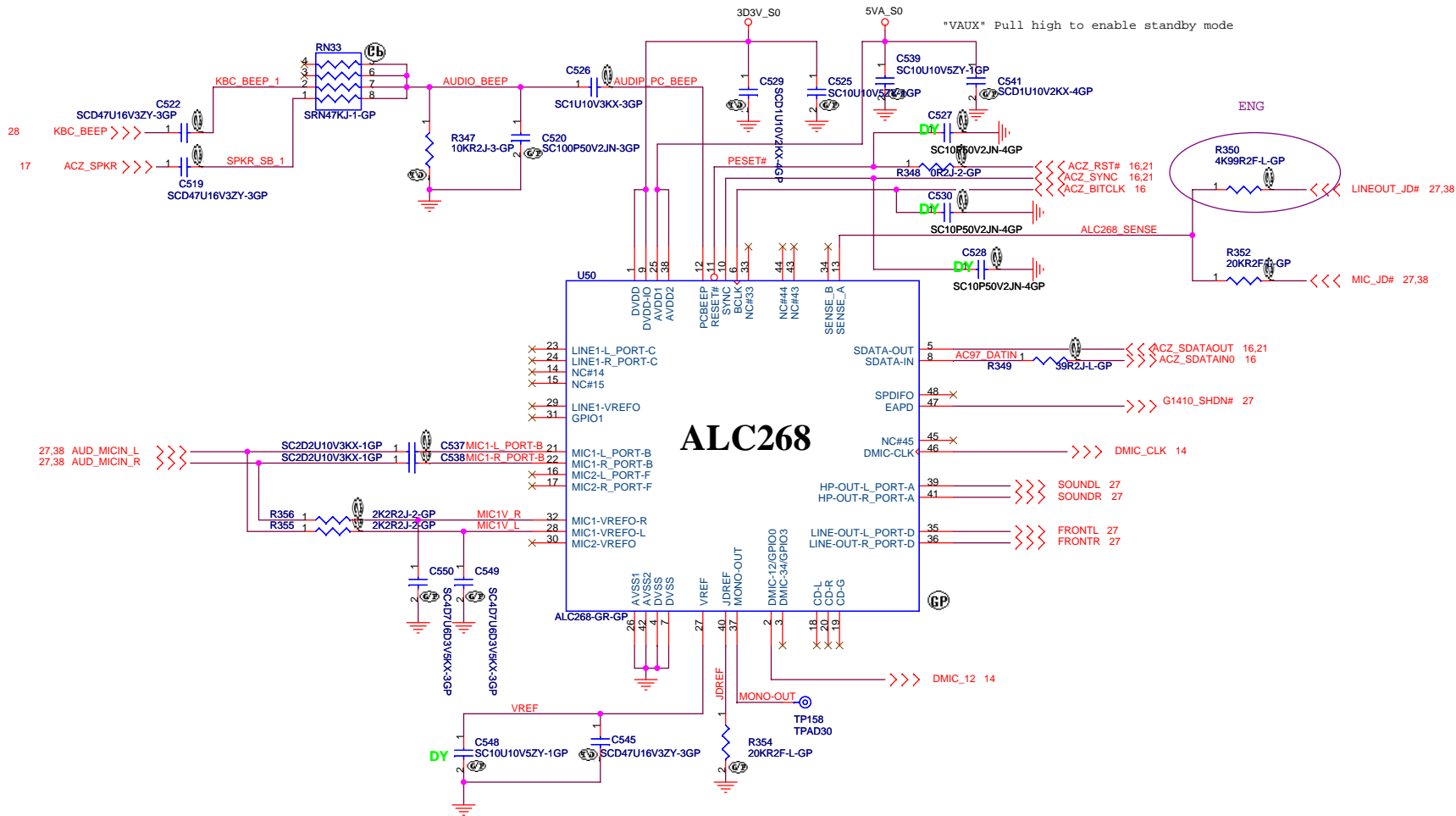
4 IN1 CARD-READER (SD/SD IO/MMC/MMC4.0/MS/MS PRO/XD)



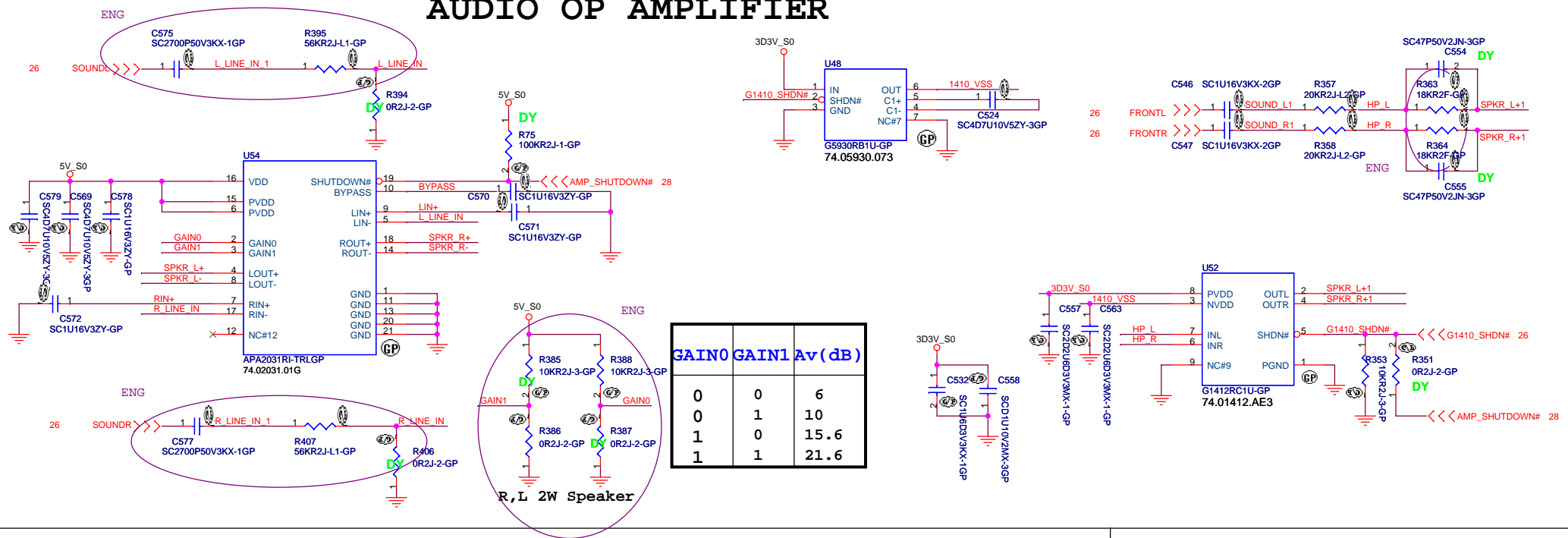
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title
USB Card Reader Controller - RTS5158

Size	Document Number	Rev
	Calado	-1
Date: Wednesday, September 12, 2007	Sheet 25 of 39	

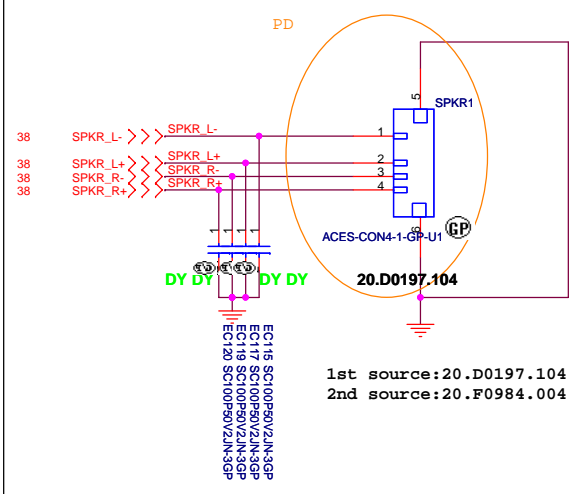


AUDIO OP AMPLIFIER



GAIN0	GAIN1	Av (dB)
0	0	6
0	1	10
1	0	15.6
1	1	21.6

Internal Speaker



1st source: 20.D0197.104
2nd source: 20.F0984.004

ICS

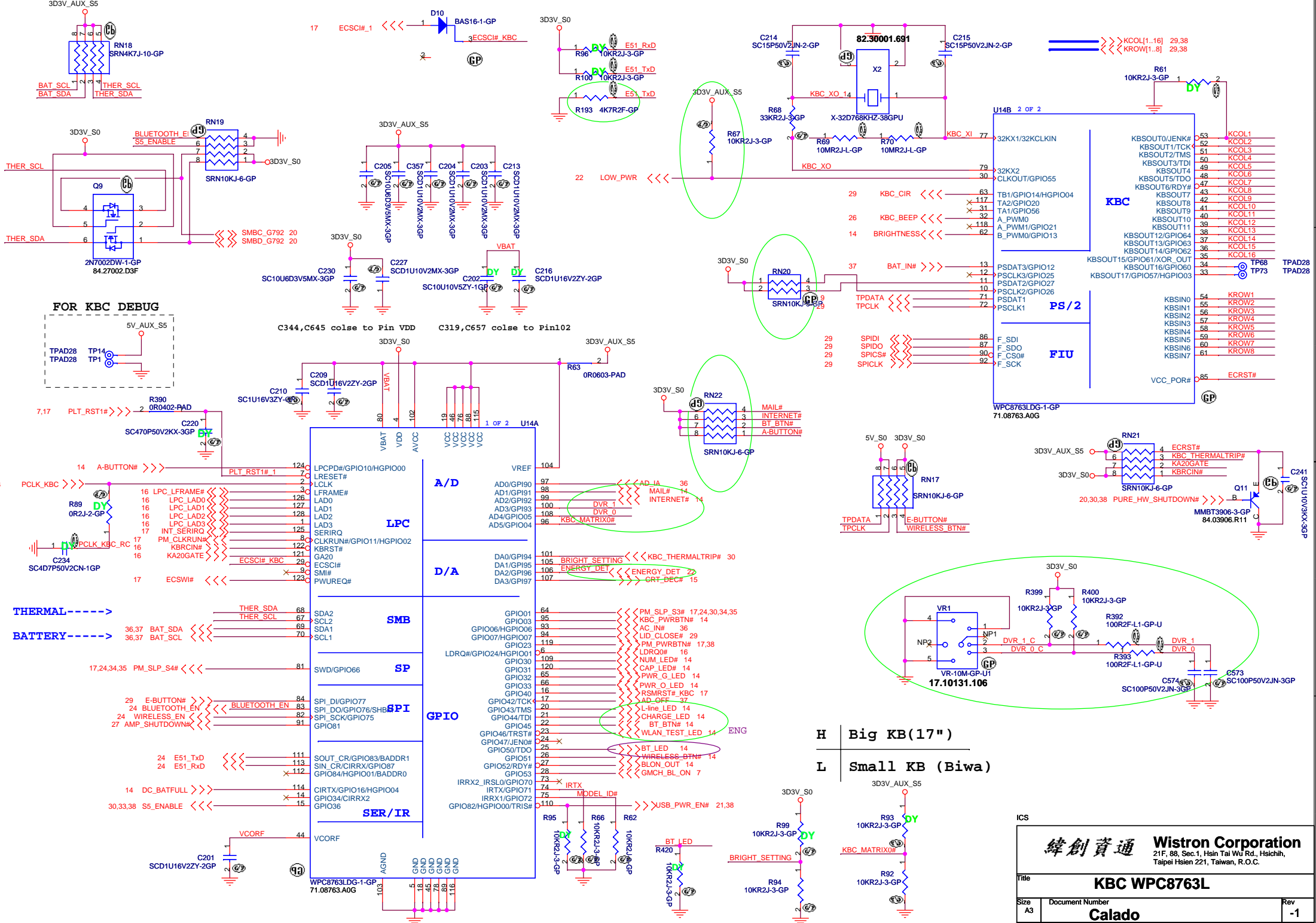
緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **AUDIO AMP AND JACK**

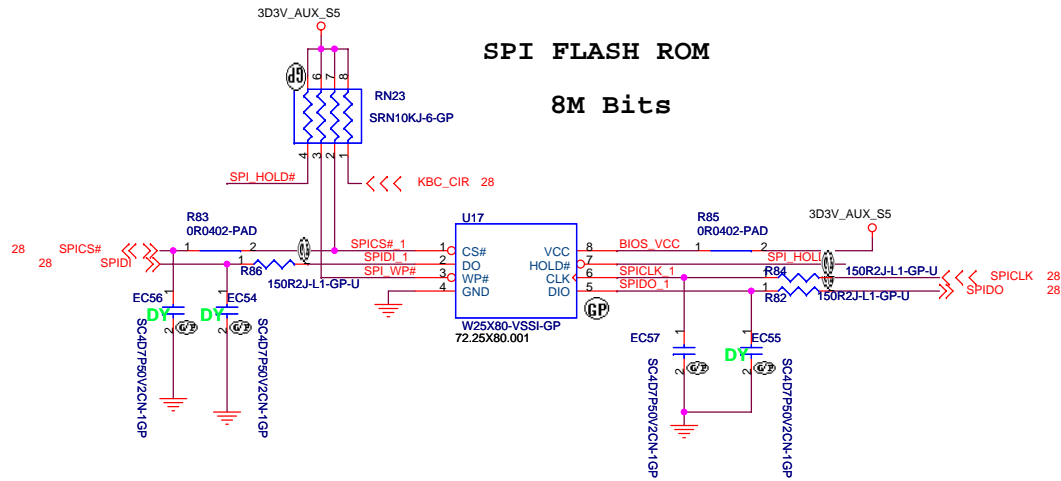
Size: Document Number

Rev: **-1**

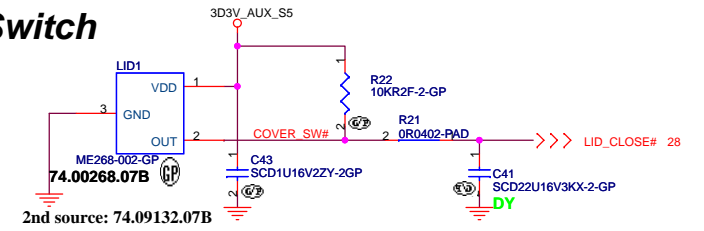
Date: Wednesday, September 12, 2007 Sheet 27 of 39



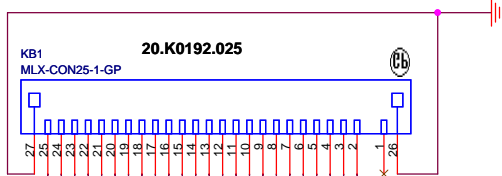
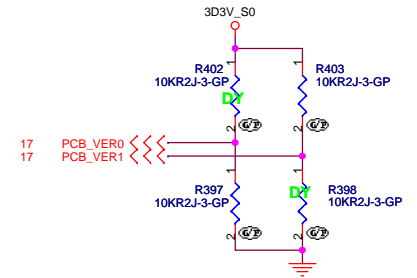
SPI FLASH ROM 8M Bits



Hall Switch



PlanarID
(1,0)
SA: 0,0
SB: 0,1
-1: 1,0
-2: 1,1

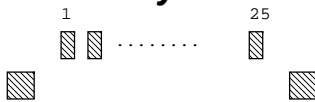


EMI Bypass cap.

KCOL16	EC14	1	SC220P50V2JN-3GP
KCOL15	EC15	1	SC220P50V2JN-3GP
KCOL14	EC17	1	SC220P50V2JN-3GP
KCOL13	EC18	1	SC220P50V2JN-3GP
KCOL8	EC24	1	SC220P50V2JN-3GP
KCOL7	EC25	1	SC220P50V2JN-3GP
KCOL6	EC26	1	SC220P50V2JN-3GP
KCOL5	EC27	1	SC220P50V2JN-3GP
KCOL4	EC28	1	SC220P50V2JN-3GP
KCOL3	EC29	1	SC220P50V2JN-3GP
KCOL2	EC30	1	SC220P50V2JN-3GP
KCOL1	EC31	1	SC220P50V2JN-3GP
KROW8	EC32	1	SC220P50V2JN-3GP
KROW7	EC33	1	SC220P50V2JN-3GP
KROW6	EC34	1	SC220P50V2JN-3GP
KROW5	EC35	1	SC220P50V2JN-3GP
KCOL12	EC19	1	SC220P50V2JN-3GP
KCOL11	EC20	1	SC220P50V2JN-3GP
KCOL10	EC21	1	SC220P50V2JN-3GP
KCOL9	EC22	1	SC220P50V2JN-3GP
KROW4	EC37	1	SC220P50V2JN-3GP
KROW3	EC38	1	SC220P50V2JN-3GP
KROW2	EC39	1	SC220P50V2JN-3GP
KROW1	EC40	1	SC220P50V2JN-3GP

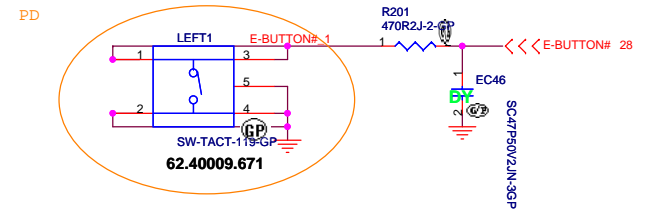
KROW1[.8] >>> KROW[1..8] 28,38
KCOL1[.16] >>> KCOL[1..16] 28,38

Internal KeyBoard CONN

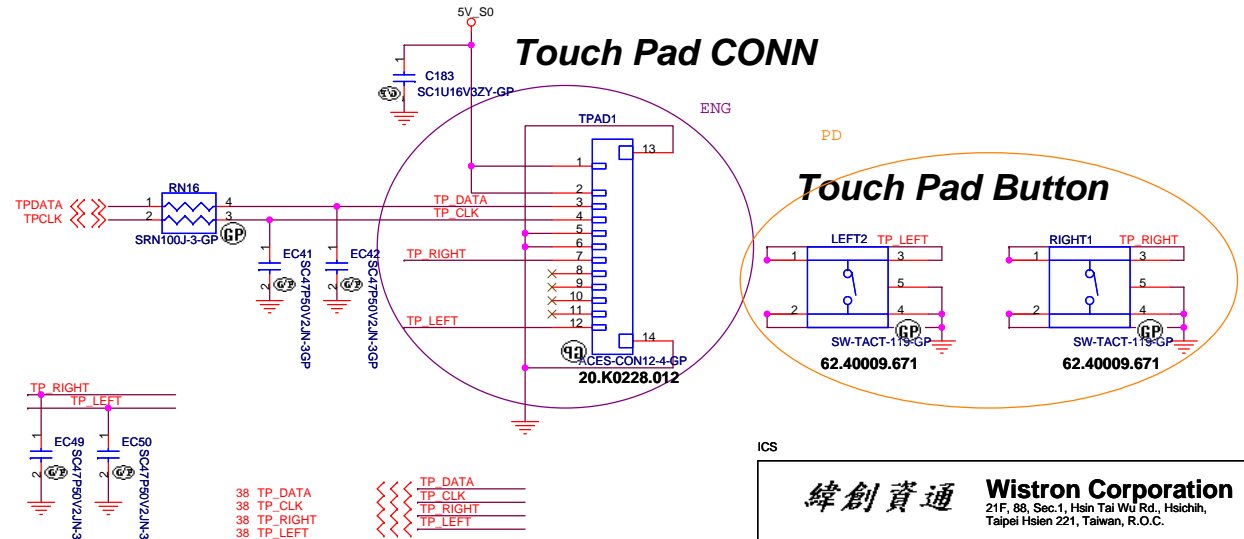


CHECK KB SPEC. AND PIN DEFINE

E-key



Touch Pad CONN



ICS

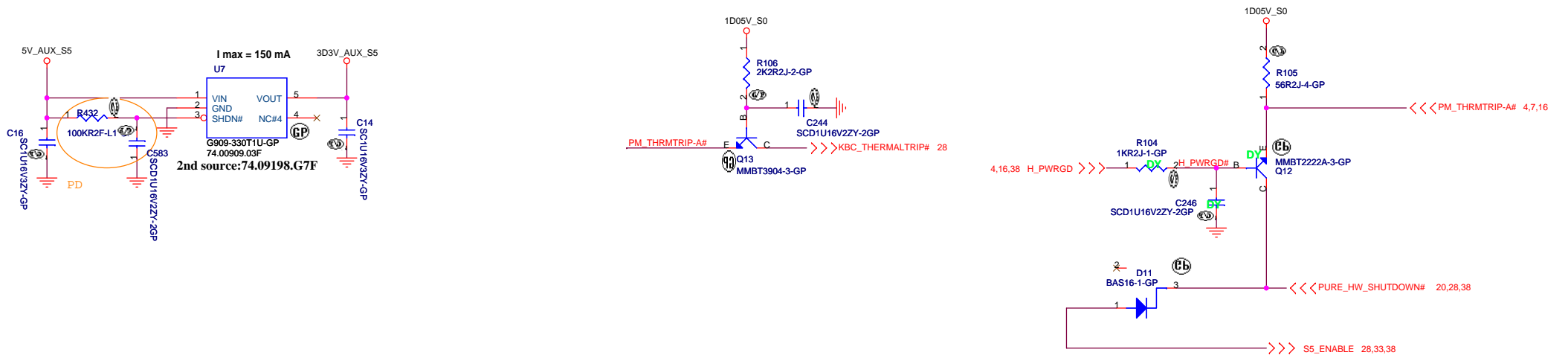
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **BUTTONS / KB / TOUCHPAD / BIOS**

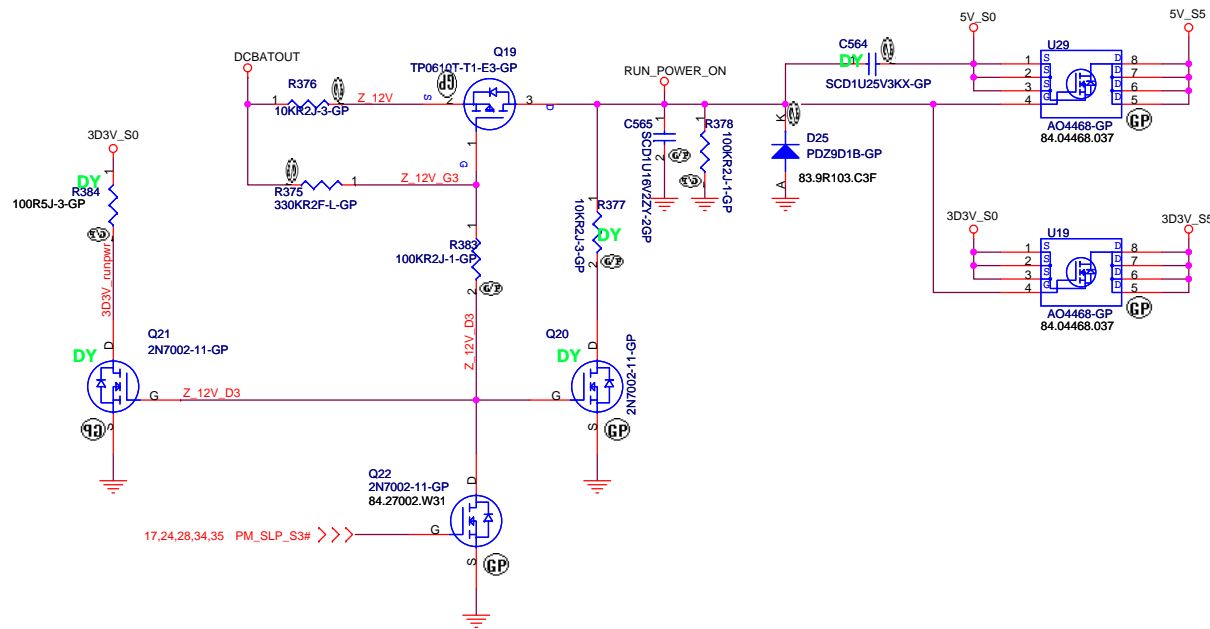
Size: Document Number Rev

Date: Wednesday, September 12, 2007 Sheet 29 of 39

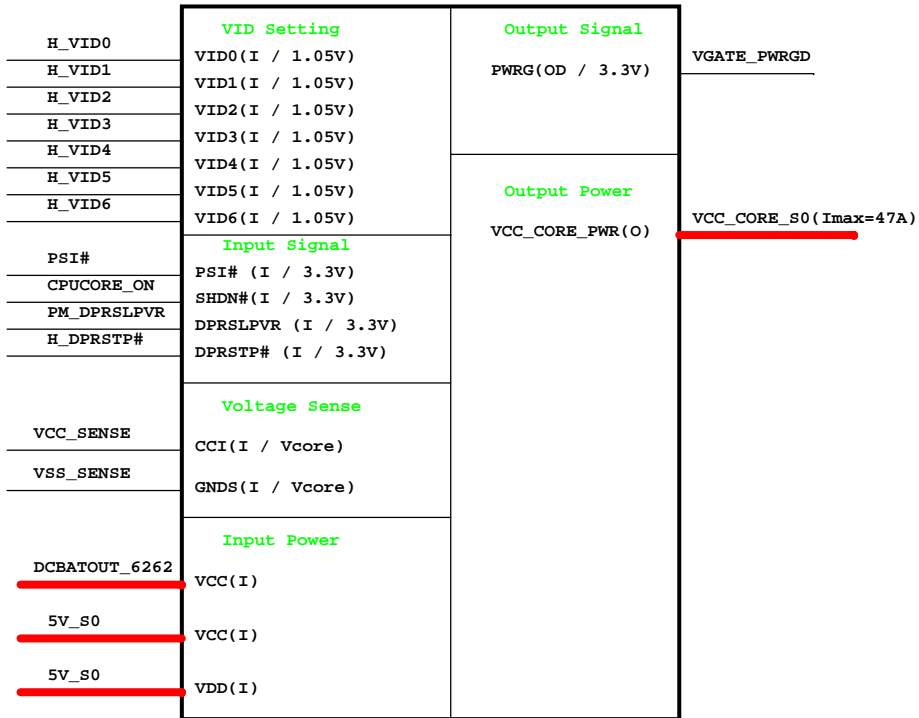
Calado -1



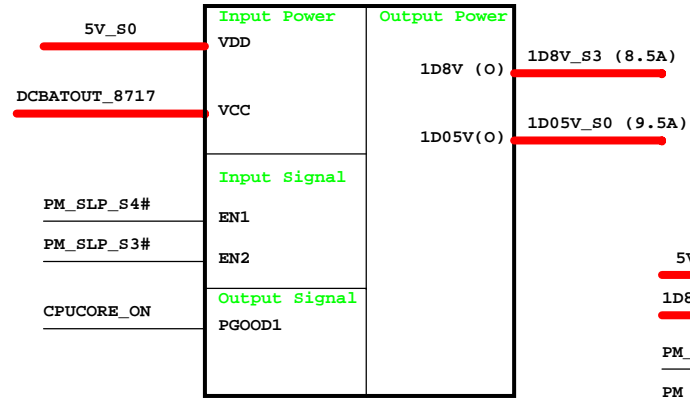
Run Power



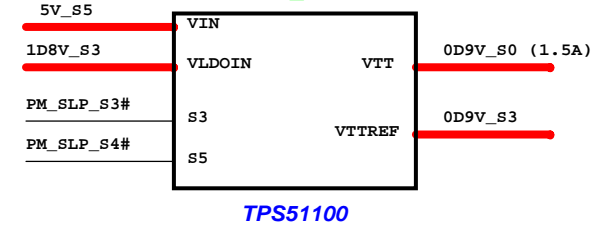
**CPU_CORE
MAX8770**



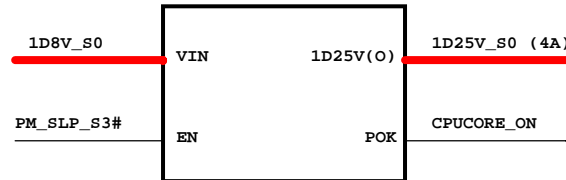
**TPS51124
1D8V/1D05V**



0D9V_S0

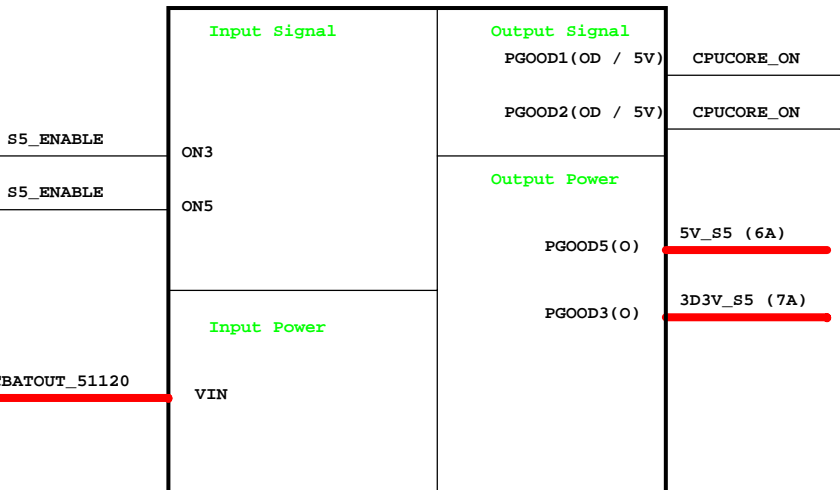


1D25V_S0

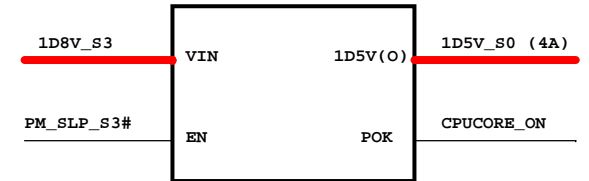


APL5913

**TPS51120
5V/3D3V**

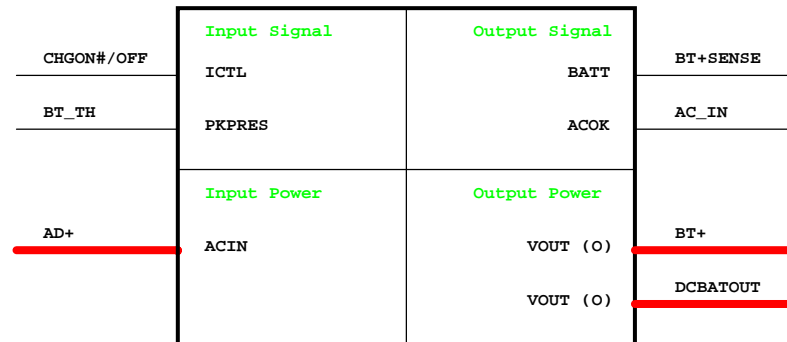


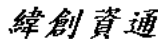
1D5V_S0

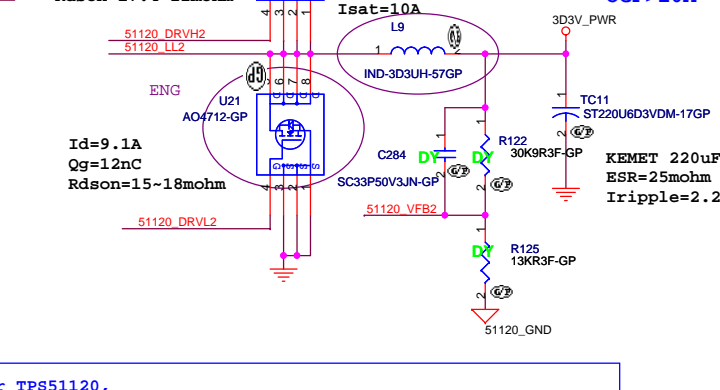
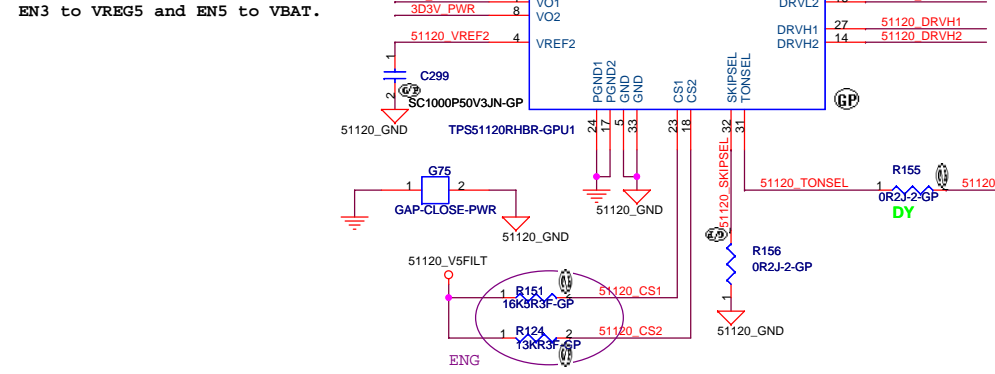
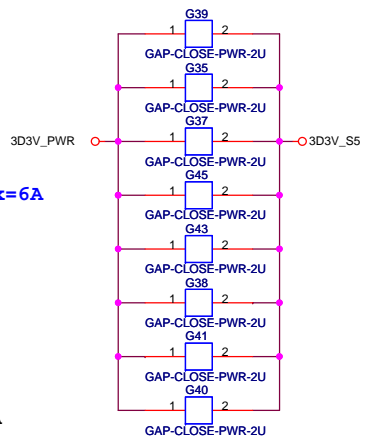
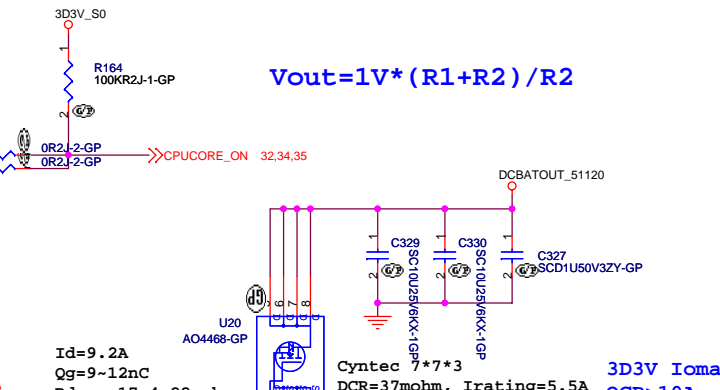
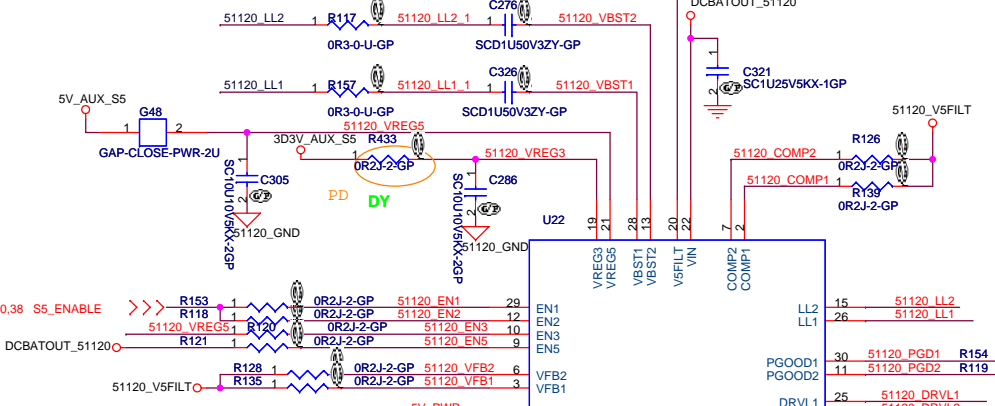
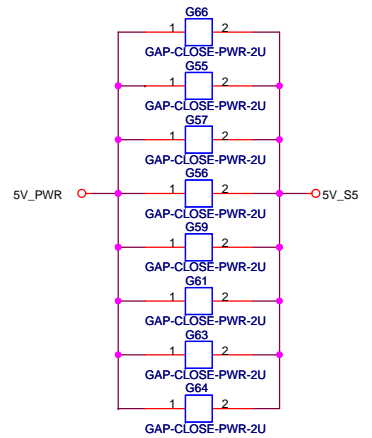
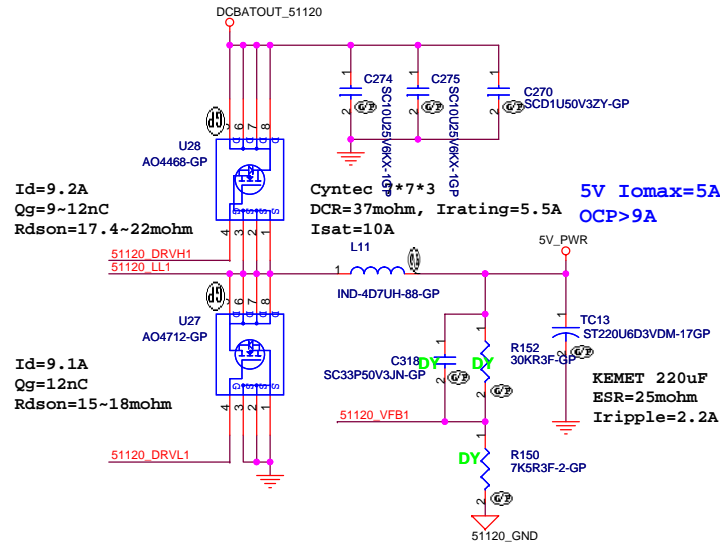
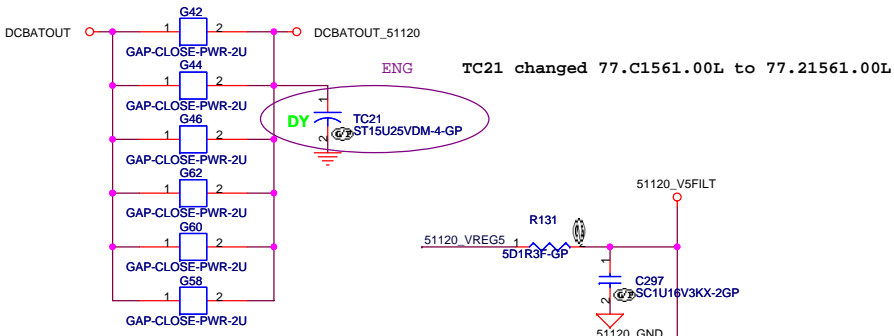


APL5915

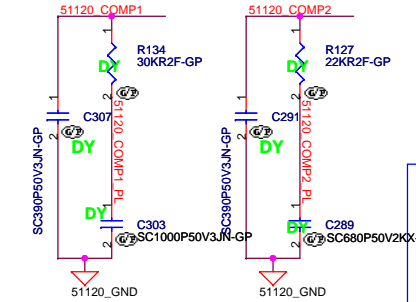
Charger MAX8731



 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Power Block Diagram	
Size A3	Document Number Calado
Date: Monday, September 10, 2007	Sheet 31 of 39



	GND	VREF2	FLOAT	V5FILT
SKIPSEL	AUTOSKIP	AUTOSKIP / FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	D-Cap MODE
TONSEL	380k/CH1 590k/CH2	290k/CH1 440k/CH2	220k/CH1 330k/CH2	180k/CH1 280k/CH2
VFB1	N/A	not use	ADJ.	5V Fixed Output
VFB2	N/A	not use	ADJ.	3.3V Fixed Output
EN1, EN2	switcher OFF	not use	Switcher ON	Switcher ON
EN3, EN5	LDO OFF	not use	LDO ON	VREG3 on



For TPS51120, Vout=5V

- If you use a 6.8uH inductor, the minimum ESR is 70m ohm.
- If you use a 4.7uH inductor, the minimum ESR is 48m ohm.
- If you use a 3.3uH inductor, the minimum ESR is 34m ohm.

Vout=3.3V

- If you use a 4.7uH inductor, the minimum ESR is 51m ohm.
- If you use a 3.3uH inductor, the minimum ESR is 36m ohm.
- If you use a 2.5uH inductor, the minimum ESR is 27m ohm.

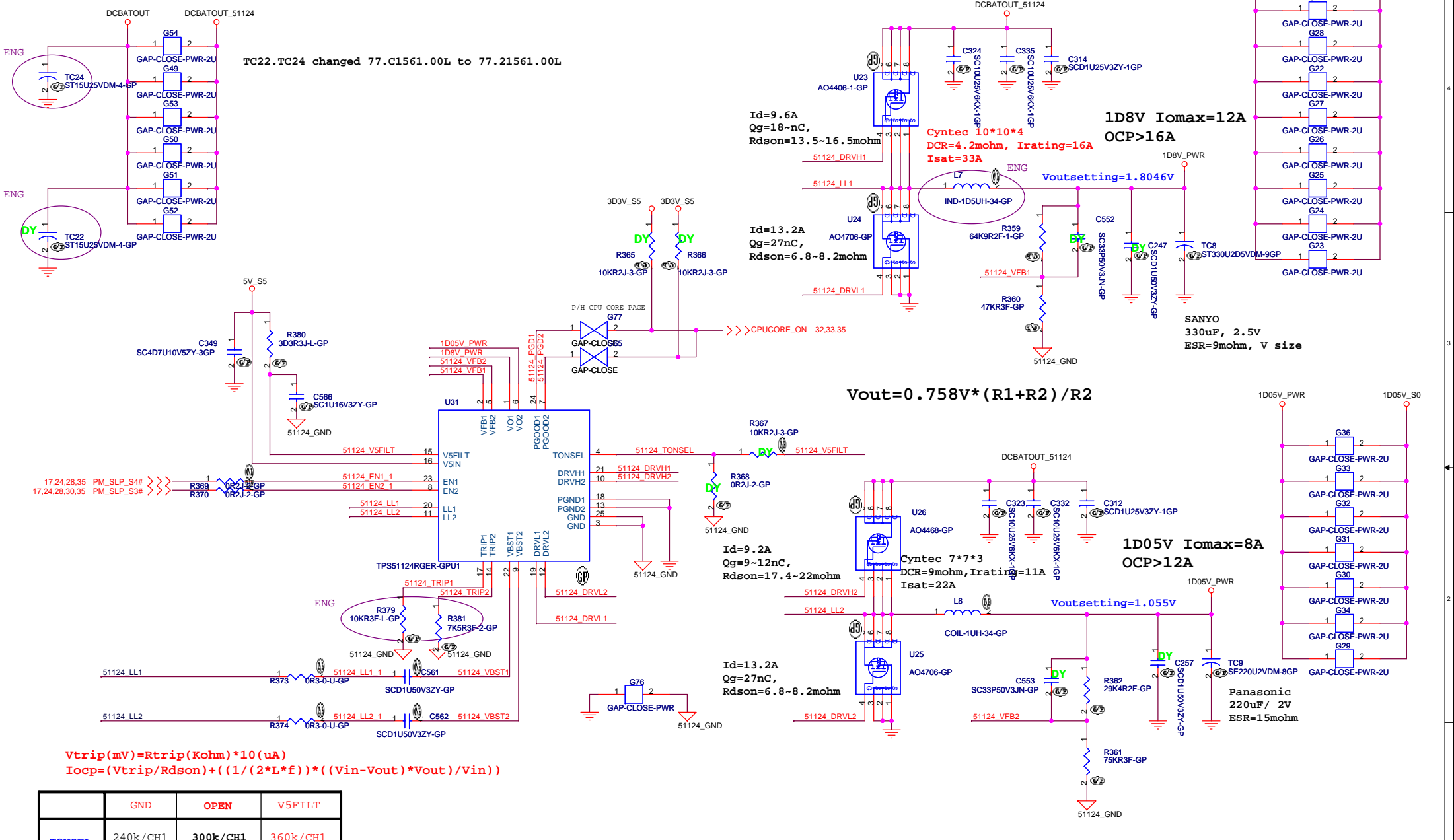
<Core Design>

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File: **TPS51120 5V 3D3V**

Size A3 Document Number **Calado** Rev -1

Date: Wednesday, September 12, 2007 Sheet 33 of 39



TC22.TC24 changed 77.C1561.00L to 77.21561.00L

Id=9.6A
Qg=18-nC,
Rdson=13.5~16.5mohm

1D8V Iomax=12A
OCP>16A

Id=13.2A
Qg=27nC,
Rdson=6.8~8.2mohm

Cyntec 10*10*4
DCR=4.2mohm, Irating=16A
Isat=33A

Voutsetting=1.8046V

SANYO
330uF, 2.5V
ESR=9mohm, V size

$$V_{out} = 0.758V * (R1 + R2) / R2$$

1D05V Iomax=8A
OCP>12A

Id=9.2A
Qg=9~12nC,
Rdson=17.4~22mohm

Cyntec 7*7*3
DCR=9mohm, Irating=11A
Isat=22A

Voutsetting=1.055V

Id=13.2A
Qg=27nC,
Rdson=6.8~8.2mohm

Panasonic
220uF / 2V
ESR=1.5mohm

$$V_{trip}(mV) = R_{trip}(Kohm) * 10(uA)$$

$$I_{ocp} = (V_{trip}/R_{dson}) + ((1/(2*L*f)) * ((V_{in} - V_{out}) * V_{out}) / V_{in})$$

	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2

ICS

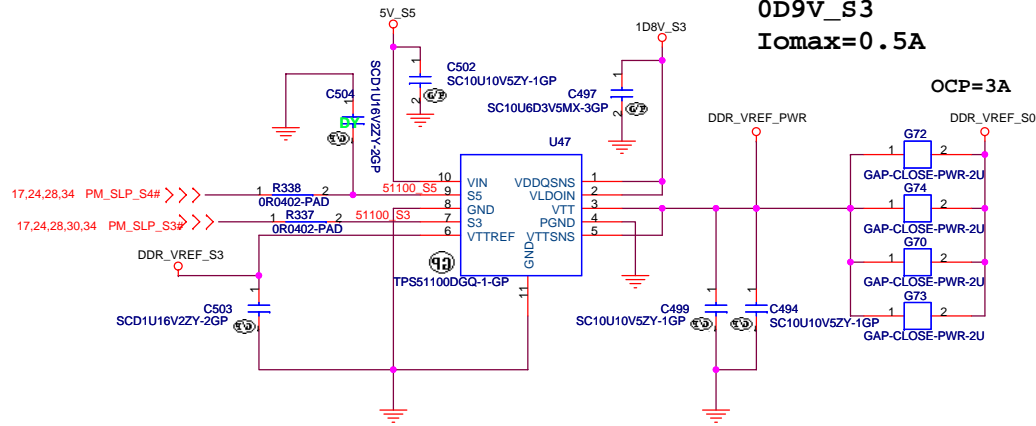
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **TPS51124 1D8V 1D05V**

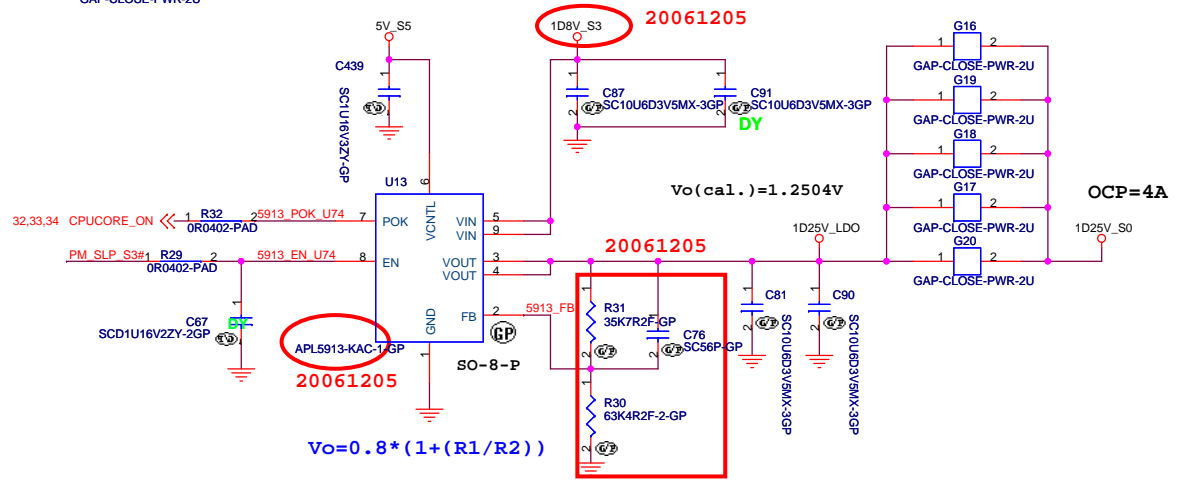
Size A3 Document Number **Calado** Rev -1

Date: Wednesday, September 12, 2007 Sheet 34 of 39

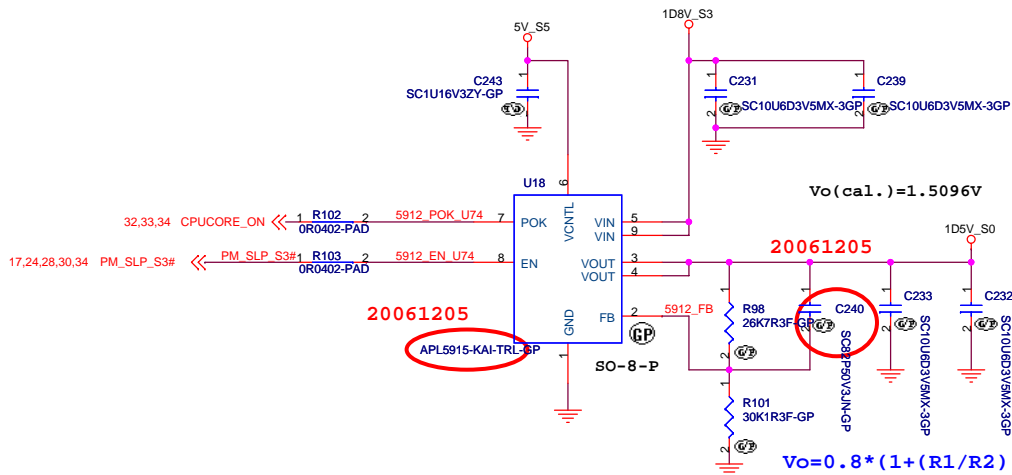
0D9V_S3
Iomax=0.5A

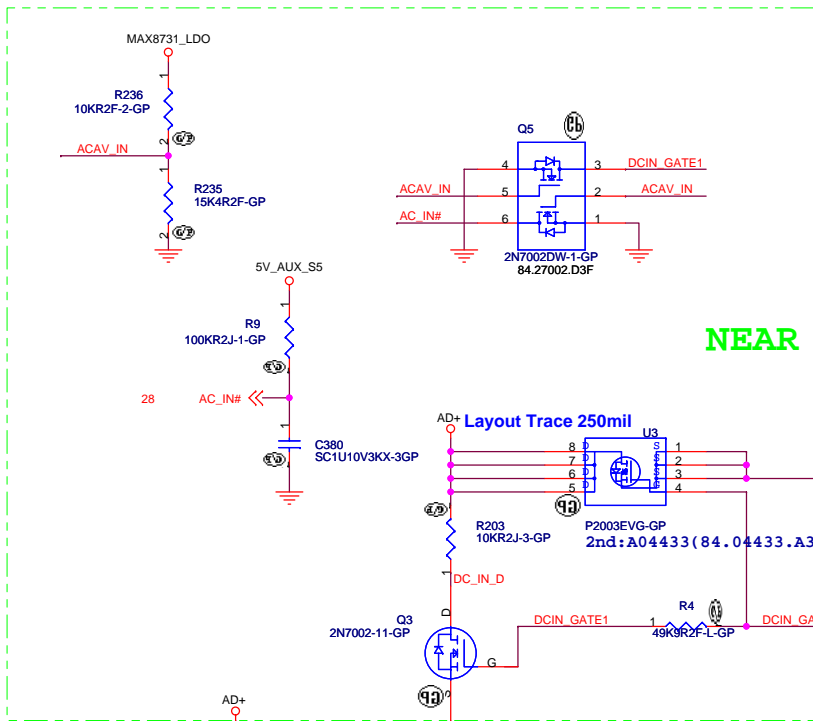


1D25V_S0
Iomax=2A

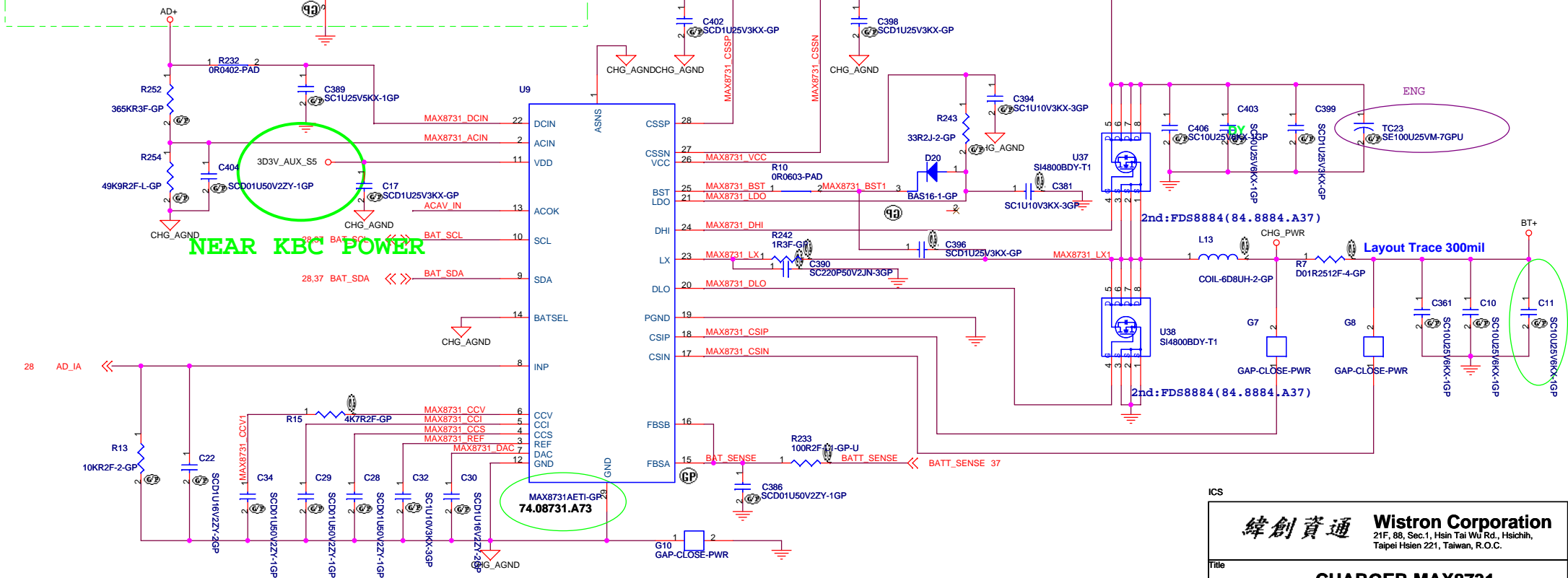


1D5V_S0
Iomax=1.5A
OCP>1.8A



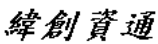


Adaptor In Soft-Start Circuit

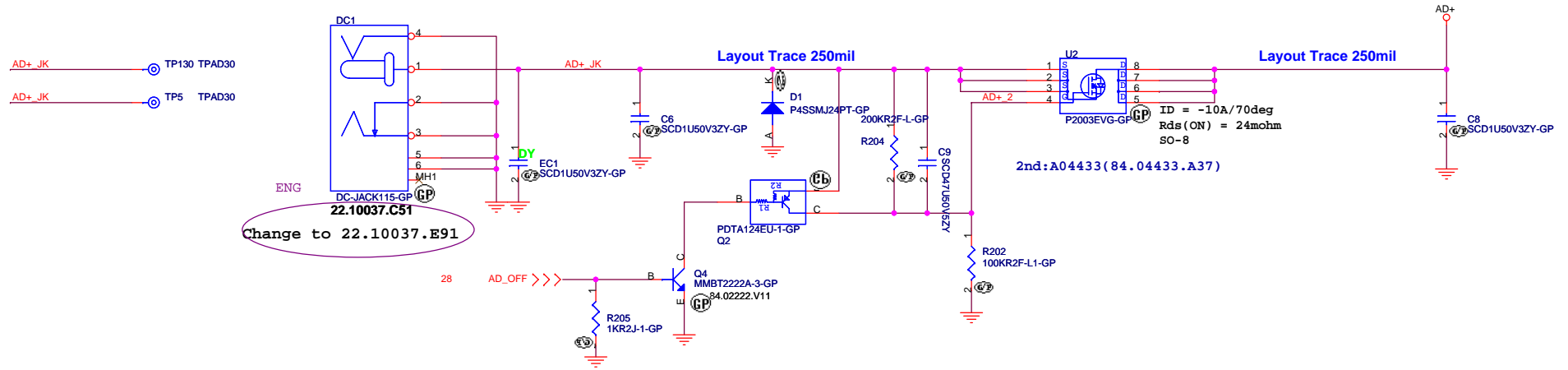


Need Check MAXIM Sming Use MAX8731 or MAX8731A

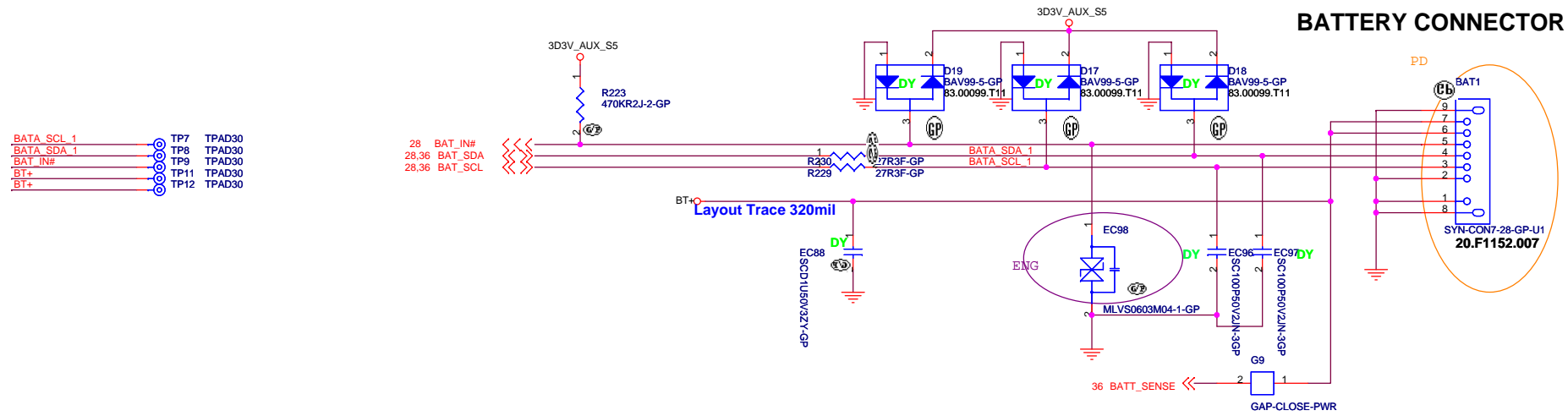
ICS

 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
CHARGER MAX8731	
Title	
Size A3	Document Number
Calado	
Date: Wednesday, September 12, 2007	Sheet 36 of 39
	Rev -1

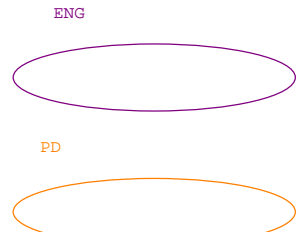
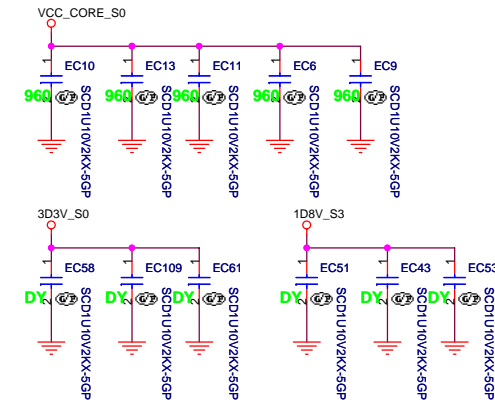
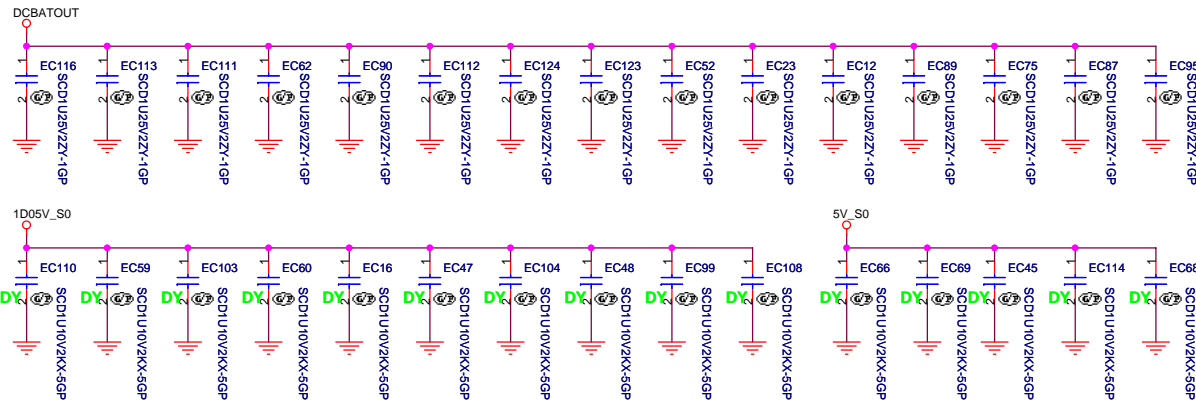
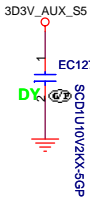
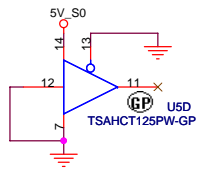
Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



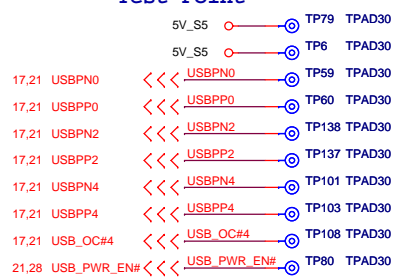
ICS	
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
AD/BATT CONN	
Size	Document Number
A3	Calado
Date: Wednesday, September 12, 2007	Sheet 37 of 39
Rev	-1



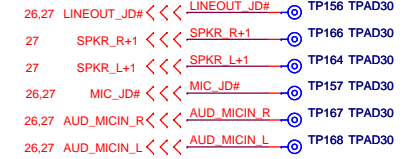
FAN CONN



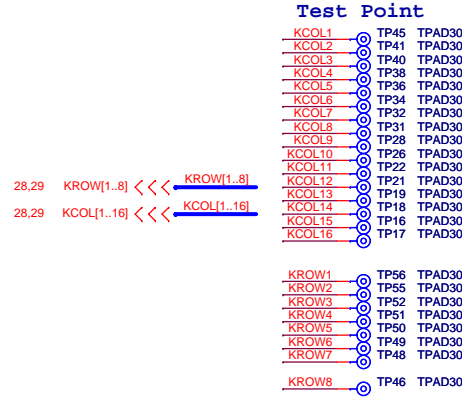
USB ZIF CONN



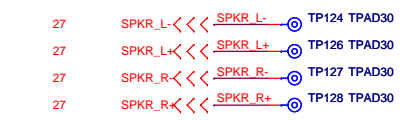
Audio Connector



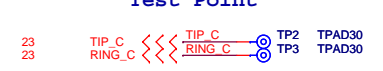
Internal KeyBoard CONN



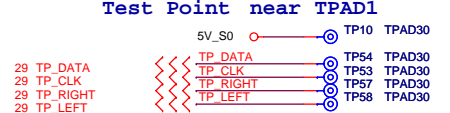
Internal Speaker



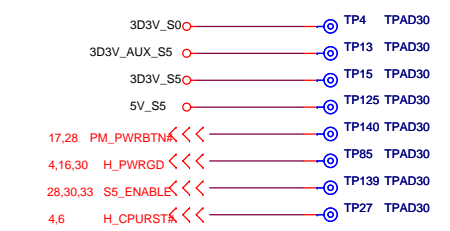
TRING CONN



Touch Pad CONN



Check test point

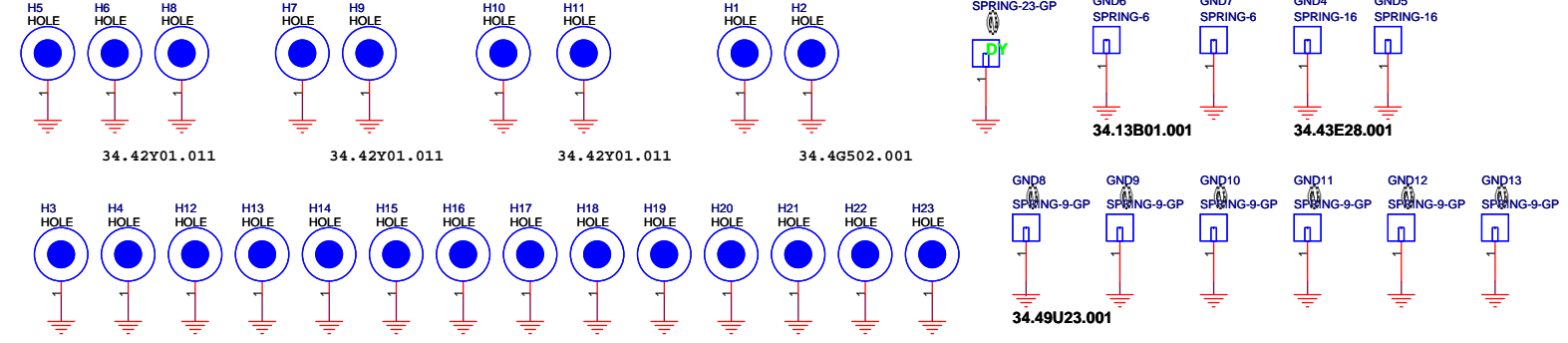


CPU

NB

MDC

MINI CARD



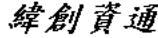
Test Point 放在 Dimm Door 打開可量測處

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Title: EMI/Spring/Boss
 Size: Document Number
 Date: Thursday, September 13, 2007
 Sheet 38 of 39

SA to SB
 1.TC6 change to 900U
 2.modify U42(change to G913 300mA) add R417 for TV CRT ripple.
 3.add Q27 for BT LED signal
 4.change LED1 to 83.01221.I70(right angle)
 5.add U55 BLON_5V for LED panel
 6.change U1 to 74.04280.C9P for source request
 7.add polyswitch F3 for safety.
 8.C338 C339 C341 C340 change to 0402 size for SATA signal.
 9.FAN1 change to 20.F1000.003 for ME.
 10.USB1 swap pin3 pin4 signal.
 11.USB2 USB3 change to 22.10218.R31 for ME.
 12.add polyswitch F4 F5 for safety.
 13.change U4 U45 to 74.09711.B7F ,U56 U57 74.05250.C7F for source request.
 14.R20 change to 1.21K for IEEE.
 15.C56 change to 12P for Oscillation report.
 16.U53 change to 74.09711.A7F for source request.
 17.NEW1 change to 20.F07890.026.SK1 change to 21.H0153.001 for ME
 18.add R421 LED4 for CardReader test.
 19.C237 C229 change to 27P for Oscillation report.
 20.R350 change to 4.99K for jack detection.
 21.R363 R364 change to 18K.R404 R405 change to 56 ohm for audio report.
 22.add AUD_AGND.L24 for audio noise.
 23.C575 C577 change to 2700p Cut frequency at 500HZ
 24.add BT_LED to KBC GPIO50.
 25.add TC19 TC20 TC21 TC22 TC23 TC24 for acoustic noise.
 26.C419 change to 1000p for power team.
 27.U21 change to 84.04712.037.L9 change to 68.3R310.20A for power team.
 28.R151 change to 16.5K.R124 change to 13K for OCP.
 29.L7 change to 68.1R510.10J for power team.
 30.R379 change to 10K.R381 change to 7.5K for OCP.
 31.BAT1 change to 20.80977.007 for ME.
 32.EC98 add 69.80007.031 for EC damaged.
 33.R402 change to 10K.R397 DY for planar ID.
 34.ODD1 change to 20.80967.050 for ME.
 35.add G79.G80 for power.
 36.R385.R386.R388.R387 change for Gain.R395.R407 change to 56K.
 37.add EC6.EC9.EC10.EC11.EC13 to 960 for EMI.
 38.add EC41.EC42.EC49.EC50.EC127 for EMI.
 39.add R423.R422 for EMI.
 40.add RN34.RN35.RN36 for EMI.
 41.remove Golden finger
 42.swap Touchpad pin define.
 43.change L1 L2 to 68.00084.371.
 44.change DC1 to 22.10037.E91 for ME.
 45.change TVOUT1 to 22.10021.F41 for ME.
 SB to -1
 1.add AFTE test point for power board Conn.
 2.add R432.C583 change G47 to R433 for 3D3V_AUX_S5 power option
 3.change to 0 ohm pad for R45.R41.R216.R391.R183.R184.R14.R162.
 R78.R79.R74.R87.R73.R77.R390.R21.R194.R187
 4.change SPKR1 to 20.D0197.104 for ME.
 5.change TRING1 to 21.E0024.102 for ME.
 6.remove D7.D8.D9 for EMI.
 7.add EC116.EC113.EC111.EC62.EC90.EC112.EC124.EC123.EC52.EC23.EC12.EC89.EC75.EC87.EC95.
 8.change R422.R423 to 33 ohm.add EC71.EC72 to 33P for EMI.
 9.add EC128.EC129 for EMI.
 10.change c419 to 78.10234.1BL for source OBSOLETED.
 11.change LEFT1.LEFT2.RIGHT1 to 62.40009.671 for ME.
 12.change TVOUT1 to 22.10021.H61 for ME.
 13.change BAT1 to 20.F1152.007 for ME.
 14.add D26 for EMI.
 15.change TC17 to 79.22710.3AL for USB droop test fial.
 16.change TC2.EC84 to 5V_USB3_S0_1,change TC17.EC101 to5V_USB2_S0_1 for UPT2 fail.
 17.add GND6.GND7.GND8.GND9.GND10.GND11.GND12.GND13 fot EMI.
 18.change CRT1 to 20.20378.015 for ME.
 19.del GND1.GND2.

ICS

 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Change List		
Size	Document Number	Rev
	Calado	-1
Date: Thursday, September 13, 2007		Sheet 39 of 39