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1. Overview

The M16C/26 group of single-chip microcomputers are built using the high-performance silicon gate CMOS process using a M16C/60 Series CPU core and are packaged in a 48-pin plastic molded QFP. These single-chip microcomputers operate using sophisticated instructions featuring a high level of instruction efficiency. With 1M bytes of address space, they are capable of executing instructions at high speed. In addition, this microcomputer contains a multiplier and DMAC which combined with fast instruction processing capability, makes it suitable for control of various OA, communication, and industrial equipment which requires high-speed arithmetic/logic operations.

1.1 Applications

Audio, cameras, office/communications/portable/industrial equipment, etc

Specifications written in this manual are believed to be accurate, but are not guaranteed to be entirely free of error. Specifications in this manual may be changed for functional or performance improvements. Please make sure your manual is the latest edition.

1.2 Performance Outline

Table 1.1 lists performance outline of M16C/26 group.

Table 1.1. Performance outline of M16C/26 group

Item		Performance
Number of basic instructions		91 instructions
Shortest instruction execution time		50 ns (f(BCLK)= 20MHz, V_{CC1}= 3.0V to 5.5V) 100 ns (f(BCLK)= 10MHz, V_{CC1}= 2.7V to 5.5V)
Memory capacity	ROM	(See the product list)
	RAM	(See the product list)
I/O port	$P1_5$ to $P1_7$, P6, P7, $P8_0$ to $P8_3$, $P8_5$ to $P8_7$, $P9_0$ to $P9_3$, P10	8bit x 3, 7bit x 1, 4bit x 1, 3bit x 1
Multifunction timer		Timer A:16 bits x 5 channels (TA0, TA1, TA2, TA3, TA4) Timer B:16 bits x 3 channels (TB0, TB1, TB2) Three-phase Motor Control Timer
Serial I/O		2 channels (UART0, UART1) UART, clock synchronous 1 channels (UART2) UART, clock synchronous, I^2C bus[1], or IEBus[2]
A/D converter		10 bits x 8 channels
DMAC		2 channels (trigger: 20 sources)
Watchdog timer		15 bits x 1 (with prescaler)
Interrupt		20 internal and 7 external sources, 4 software sources, 7 levels
Clock generation circuit		3 circuits (These circuits contain a built-in feedback resistor and external ceramic/quartz oscillator) • Main clock • Sub-clock • On-chip oscillator(main-clock oscillation stop detect function)
Power supply voltage		V_{CC}=3.0V to 5.5V (f(BCLK)=20MHz) V_{CC}=2.7V to 5.5V (f(BCLK)=10MHz)
Flash memory	Program/erase voltage	V_{CC}=2.7V to 5.5V
	Number of program/erase	100 times (all area) 1000times (program area) /10000 times[3] (data area)
Power consumption		16mA (V_{CC}=3V, f(BCLK)=20MHz) 25µA (f(BCLK)=f(X_{CIN})=32kHz on RAM) 1.8µA (V_{CC}=3V, f(X_{CIN})=32kHz, when wait mode) 0.7µA (V_{CC}=3V, when stop mode)
I/O characteristics	I/O withstand voltage	5.0V
	Output current	5mA
Operating ambient temperature		-20 to 85°C -40 to 85°C [3]
Device configuration		CMOS high performance silicon gate
Package		48-pin plastic mold QFP

Notes:
1. I^2C bus is a trademark of Koninklijke Philips Electronics N.V.
2. IEBus is a trademark of NEC Electronics Corporation.
3. See Table 1.3 for the number of program/erase and the operating ambient temperatue.

1.3 Block Diagram

Figure 1.1 is a block diagram of the M16C/26 group.

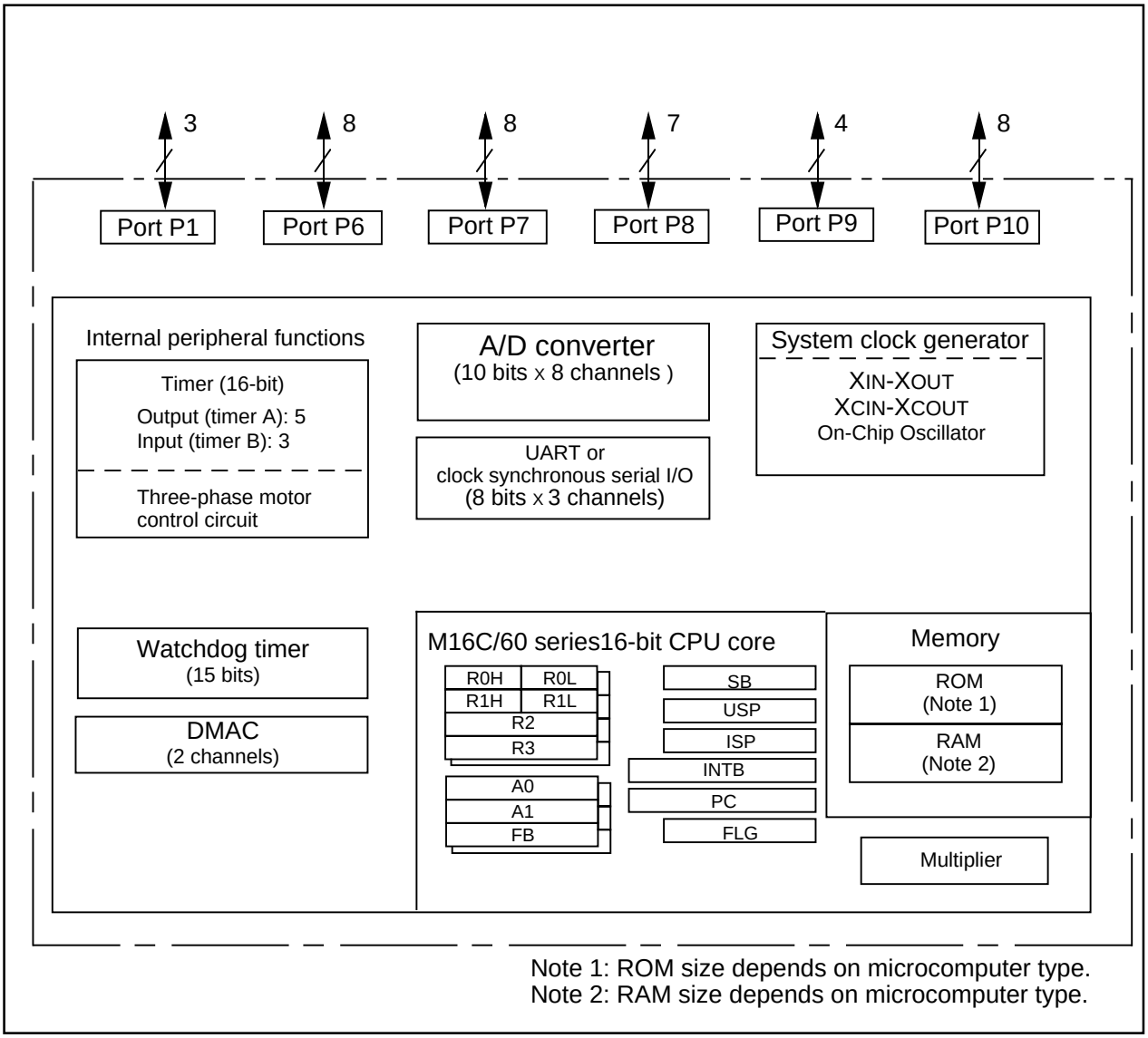


Figure 1.1. Block Diagram

1.4 Product List

Table 1.2 lists the M16C/26 group products, Figure 1.2 shows the type numbers, memory sizes and packages, Table 1.3 lists the product code, and Figure 1.3 shows the marking.

Table 1.2. Product List As of May 2004

Type No.	ROM capacity	RAM capacity	Package type	Remarks
M30262F3GP	24K + 4K byte	1K byte	48P6Q-A	Flash ROM Version
M30262F4GP	32K + 4K byte	1K byte		
M30262F6GP	48K + 4K byte	2K byte		
M30262F8GP	64K + 4K byte	2K byte		

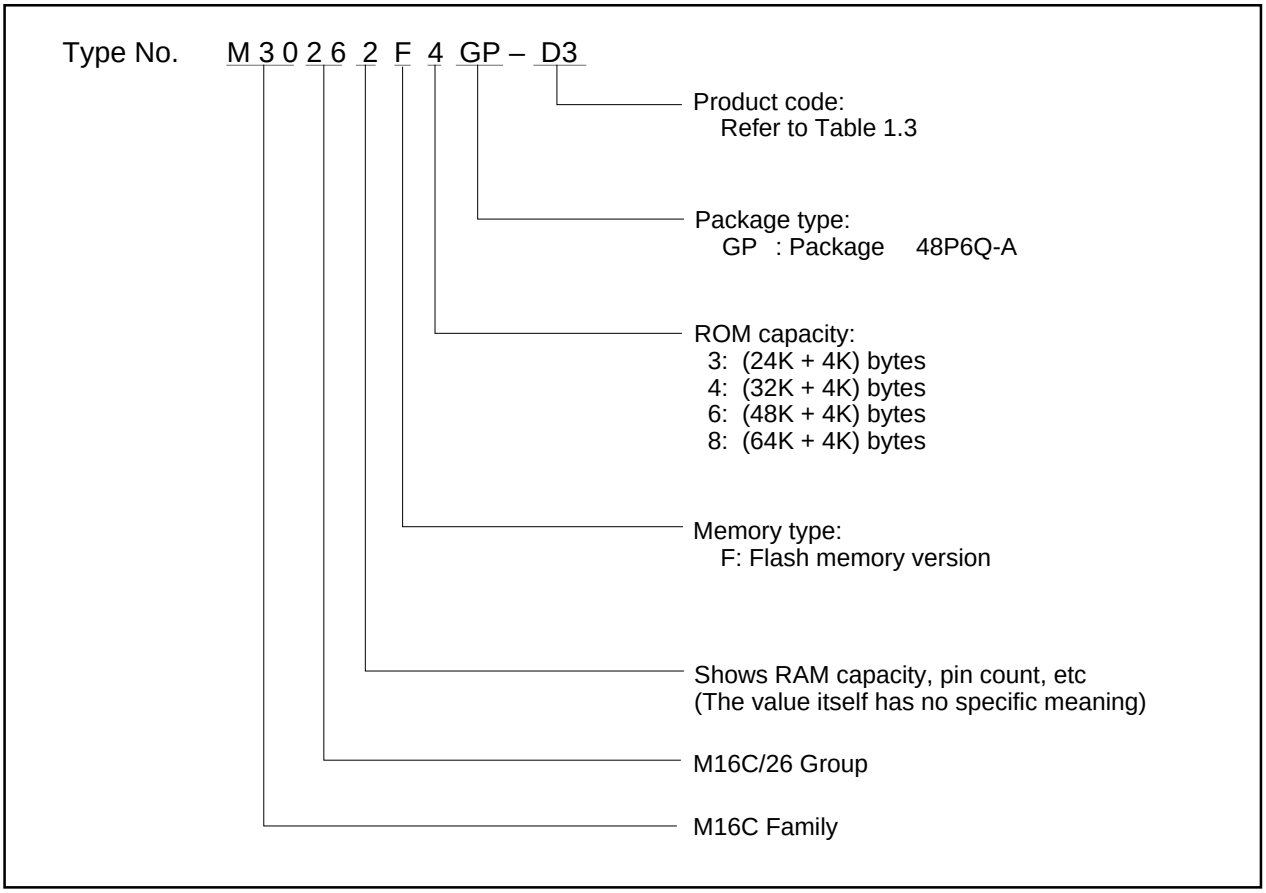


Figure 1.2. Type No., Memory Size, and Package

Table 1.3. Product code

Product Code	Package	Internal ROM (Program area)		Internal ROM (Data area)		Operating Ambient Temperature
		Program and Erase Endurance	Temperature Range	Program and Erase Endurance	Temperature Range	
D3	Lead-included	100	0°C to 60°C	100	0°C to 60°C	-40°C to 85°C
D5						-20°C to 85°C
D7		1,000		10,000	-40°C to 85°C	-40°C to 85°C
D9					-20°C to 85°C	-20°C to 85°C
U3	Lead-free	100		100	0°C to 60°C	-40°C to 85°C
U5						-20°C to 85°C
U7		1,000		10,000	-40°C to 85°C	-40°C to 85°C
U9					-20°C to 85°C	-20°C to 85°C

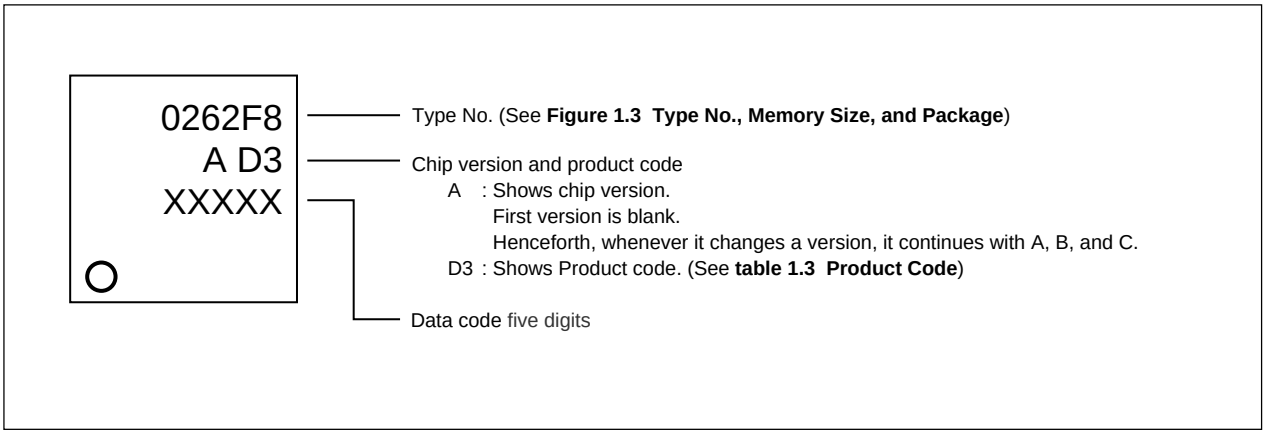


Figure 1.3. Marking Diagram of Flash Memory versionfor M16C/26 (Top View)

1.5 Pin Configuration

Figures 1.4 showd the pin configurations (top view).

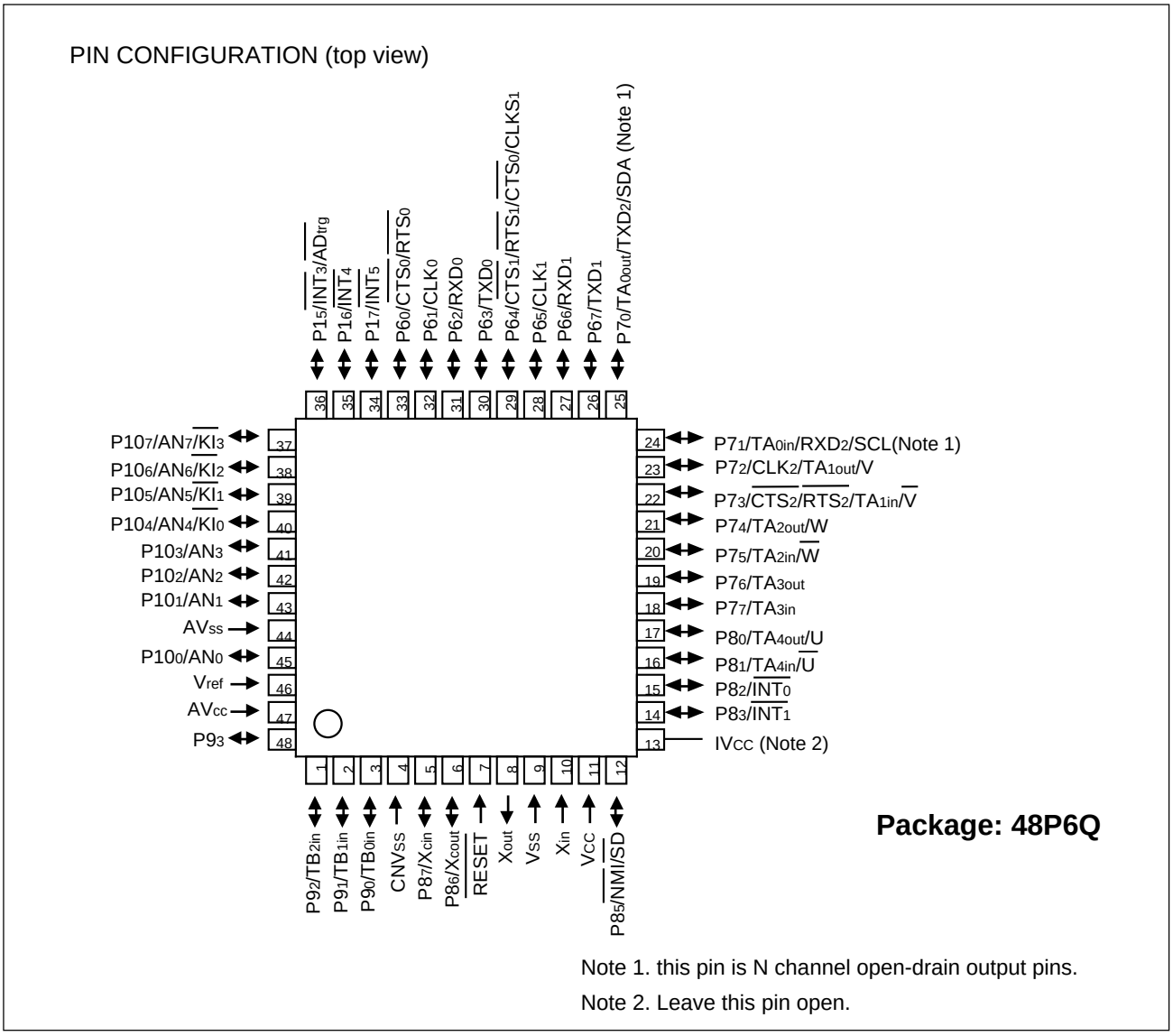


Figure 1.4. Pin Configuration (Top View)

1.6 Pin Description

Table 1.4 and 1.5 describe the available pins.

Table 1.4. Pin Description(1)

Pin name	Signal name	I/O type	Function
V_{CC},V_{SS}	Power supply input		Apply 2.7V to 5.5V to the V_{CC} pin, and 0V to the Vss pin.
CNV_{SS}	CNV_{SS}	Input	Connect this pin to Vss.
IV_{CC}	IV_{CC}		Leave this pin open.
$\overline{RESET}$	Reset input	Input	"L" on this input resets the microcomputer.
X_{IN} X_{OUT}	Clock input Clock output	Input Output	These pins are provided for the main clock generating circuit input/output. Connect a ceramic resonator or crystal between the X_{IN} and the X_{OUT} pins. To use an externally derived clock, input it to the X_{IN} pin and leave the X_{OUT} pin open.
AV_{CC}	Analog power supply input		This pin is a power supply input for the A/D converter. Connect this pin to V_{CC}.
AV_{SS}	Analog power supply input		This pin is a power supply input for the A/D converter. Connect this pin to V_{SS}.
V_{REF}	Reference Voltage input	Input	This pin is a reference voltage input for the A/D converter.
$P1_5$~$P1_7$	I/O port P1	Input/ output	This is an 3-bit CMOS I/O port. It has an input/output port direction register that allows the user to set each pin for input or output individually. When used for input, a pull-up resister option can be selected for the entire group of three pins. Additional software selectable secondary functions are: 1) $P1_5$ to $P1_7$ can be configured as external $\overline{INT}$ interrupt pins, and; 2) $P1_5$ can input a trigger for the A/D converter.
$P6_0$~$P6_7$	I/O port P6	Input/ output	This is an 8-bit CMOS I/O port. It has an input/output port direction register that allows the user to set each pin for input or output individually. When used for input, a pull-up resister option can be selected for the entire group of four pins. Pins in this port also function as UART0 and UART1 I/O.
$P7_0$~$P7_7$	I/O port P7	Input/ output	This is an 8-bit I/O port equivalent to P6. ($P7_0$ and $P7_1$ are N channel open-drain output) P7 can also function as I/O for timer A0 to A3, as selected by software. Additional programming options are: $P7_0$ to $P7_3$ can assume UART2 I/O capabilities, and $P7_2$ to $P7_5$ can function as output pins for the three-phase motor control timer.
$P8_0$~$P8_3$, $P8_5$~$P8_7$	I/O port P8	Input/ output	$P8_0$ to $P8_3$ and $P8_5$ to $P8_7$ are an 7-bit I/O port equivalent to P6.When used for input, a pull-up resister option can be selected for the entire group of four pins or three pins. Additional software-selectable secondary functions are: 1) $P8_0$ and $P8_1$ can act as either I/O for Timer A4, or as output pins for the three-phase motor control timer; 2) $P8_2$ to $P8_3$ can be configured as external $\overline{INT}$ interrupt pins; 3) $P8_5$ can be used as $\overline{NMI}$/$\overline{SD}$. $P8_5$ can not be used as I/O port while the three-phase motor control is enabled. Apply a stable "H" to $P8_5$ after setting the direction register for $P8_5$ to "0" when the three-phase motor control is enabled, and; 4) $P8_6$ and $P8_7$ can serve as I/O pins for the sub-clock generation circuit. In this latter case, a quartzoscillator must be connented between $P8_6$ (X_{COUT} pin) and $P8_7$ (X_{CIN} pin).

Table 1.7. Pin Description(2)

Pin name	Signal name	I/O type	Function
$P9_0$~$P9_3$	I/O port P9	Input/ output	This is an 4-bit I/O port equivalent to P6. Additional software-selectable secondary functions are: 1) $P9_0$ to $P9_2$ can act as Timer B0~B2 input pins.
$P10_0$~$P10_7$	I/O port P10	Input/ output	This is an 8-bit I/O port equivalent to P6. This port can also function as A/D converter input pins, as selected by software. Furthermore, $P10_4$ to $P10_7$ can also function as input pins for the key input interrupt function.

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU registers. The CPU has 13 registers. Of these, R0, R1, R2, R3, A0, A1 and FB comprise a register bank. There are two register banks.

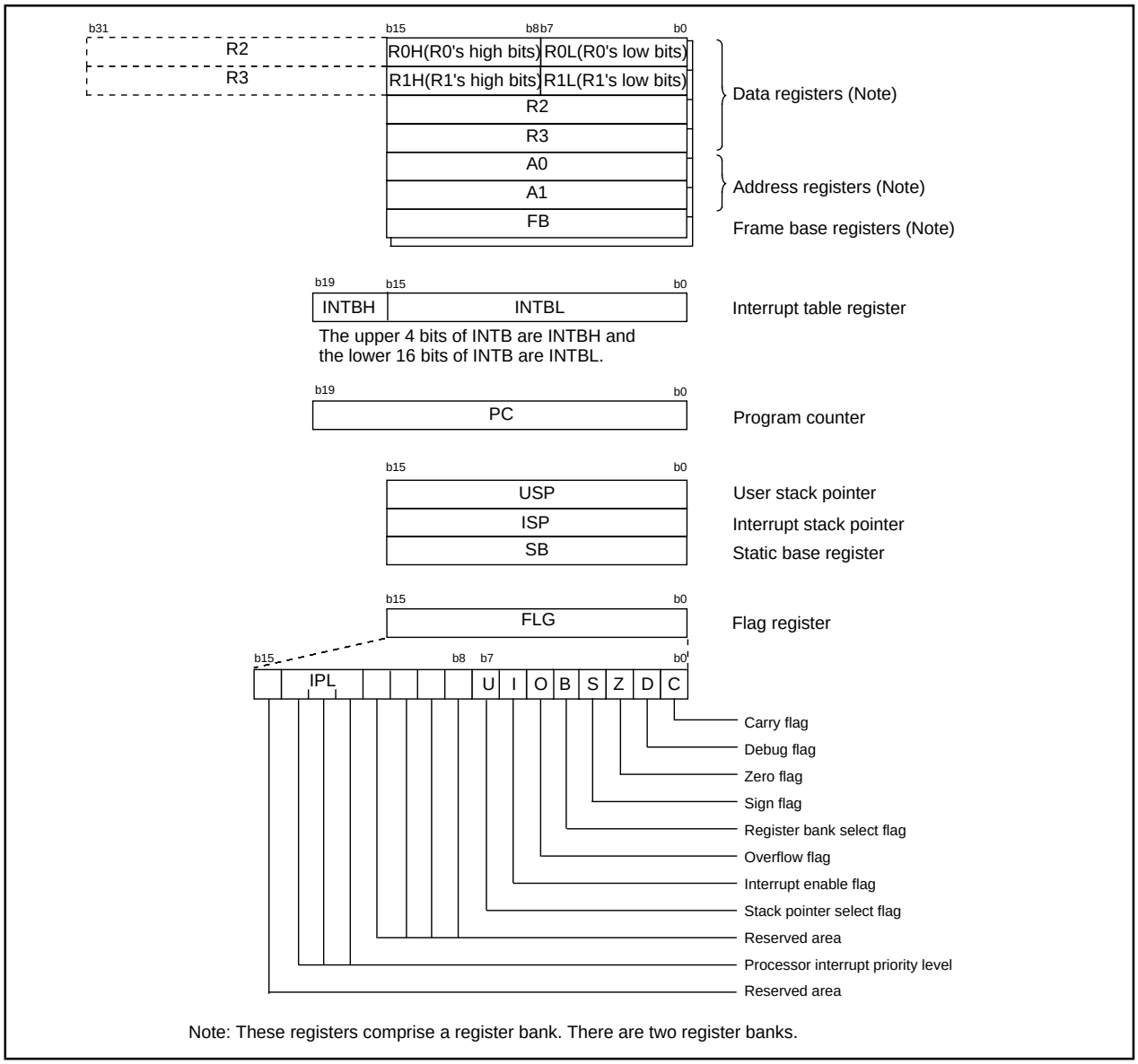


Figure 2.1. Central Processing Unit Register

2.1 Data Registers (R0, R1, R2 and R3)

The R0 register consists of 16 bits, and is used mainly for transfers and arithmetic/logic operations. R1 to R3 are the same as R0.

The R0 register can be separated between high (R0H) and low (R0L) for use as two 8-bit data registers. R1H and R1L are the same as R0H and R0L. Conversely, R2 and R0 can be combined for use as a 32-bit data register (R2R0). R3R1 is the same as R2R0.

2.2 Address Registers (A0 and A1)

The register A0 consists of 16 bits, and is used for address register indirect addressing and address register relative addressing. They also are used for transfers and logic/logic operations. A1 is the same as A0. In some instructions, registers A1 and A0 can be combined for use as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is configured with 16 bits, and is used for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is configured with 20 bits, indicating the start address of an interrupt vector table.

2.5 Program Counter (PC)

PC is configured with 20 bits, indicating the address of an instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

Stack pointer (SP) comes in two types: USP and ISP, each configured with 16 bits.

Your desired type of stack pointer (USP or ISP) can be selected by the U flag of FLG.

2.7 Static Base Register (SB)

SB is configured with 16 bits, and is used for SB relative addressing.

2.8 Flag Register (FLG)

FLG consists of 11 bits, indicating the CPU status.

2.8.1 Carry Flag (C Flag)

This flag retains a carry, borrow, or shift-out bit that has occurred in the arithmetic/logic unit.

2.8.2 Debug Flag (D Flag)

The D flag is used exclusively for debugging purpose. During normal use, it must be set to “0”.

2.8.3 Zero Flag (Z Flag)

This flag is set to “1” when an arithmetic operation resulted in 0; otherwise, it is “0”.

2.8.4 Sign Flag (S Flag)

This flag is set to “1” when an arithmetic operation resulted in a negative value; otherwise, it is “0”.

2.8.5 Register Bank Select Flag (B Flag)

Register bank 0 is selected when this flag is “0” ; register bank 1 is selected when this flag is “1”.

2.8.6 Overflow Flag (O Flag)

This flag is set to “1” when the operation resulted in an overflow; otherwise, it is “0”.

2.8.7 Interrupt Enable Flag (I Flag)

This flag enables a maskable interrupt.

Maskable interrupts are disabled when the I flag is “0”, and are enabled when the I flag is “1”. The I flag is cleared to “0” when the interrupt request is accepted.

2.8.8 Stack Pointer Select Flag (U Flag)

ISP is selected when the U flag is “0”; USP is selected when the U flag is “1”.

The U flag is cleared to “0” when a hardware interrupt request is accepted or an INT instruction for software interrupt Nos. 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is configured with three bits, for specification of up to eight processor interrupt priority levels from level 0 to level 7.

If a requested interrupt has priority greater than IPL, the interrupt is enabled.

2.8.10 Reserved Area

When write to this bit, write "0". When read, its content is indeterminate.

3. Memory

Figure 3.1 is a memory map of the M16C/26 group. The address space extends the 1M bytes from address 00000$_{16}$ to FFFFF$_{16}$.

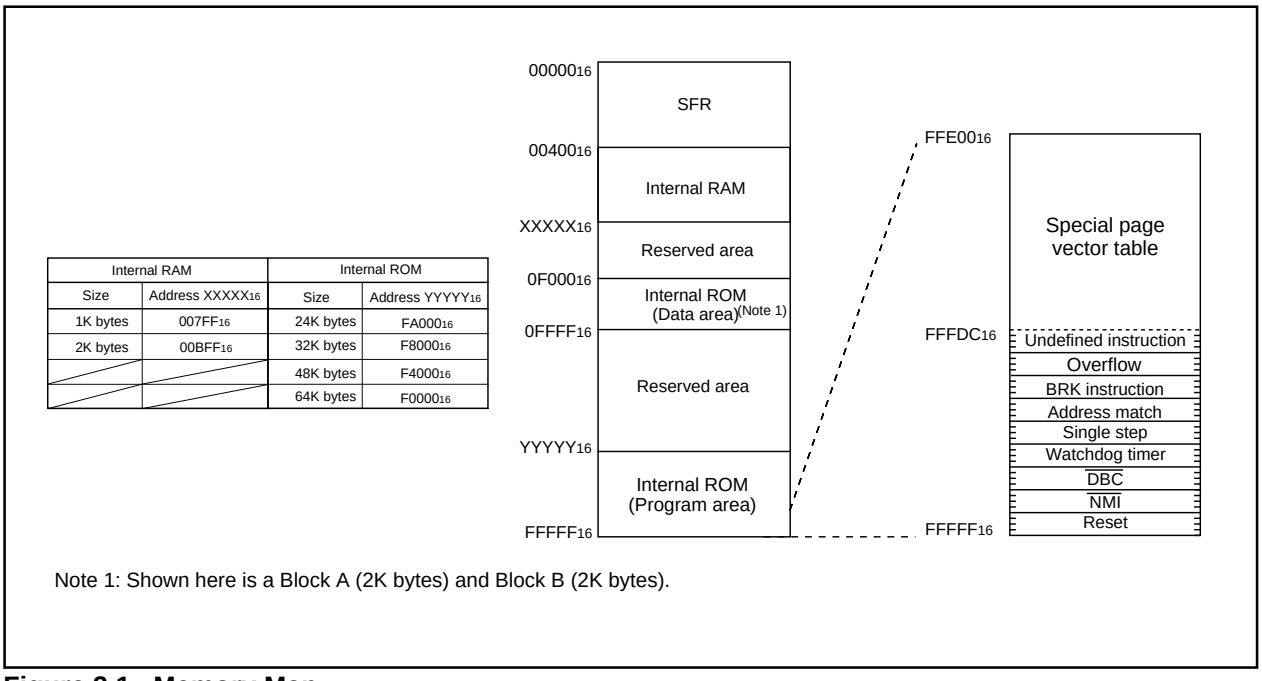
The internal ROM is allocated in a lower address direction beginning with address FFFFF$_{16}$. For example, a 32-Kbyte internal ROM is allocated to the addresses from F8000$_{16}$ to FFFFF$_{16}$.

The fixed interrupt vector table is allocated to the addresses from FFFDC$_{16}$ to FFFFF$_{16}$. Therefore, store the start address of each interrupt routine here.

The internal RAM is allocated in an upper address direction beginning with address 00400$_{16}$. For example, a 1-Kbytes internal RAM is allocated to the addresses from 00400$_{16}$ to 007FF$_{16}$. In addition to storing data, the internal RAM also stores the stack used when calling subroutines and when interrupts are generated.

The SRF is allocated to the addresses from 00000$_{16}$ to 003FF$_{16}$. Peripheral function control registers are located here. Of the SFR, any area which has no functions allocated is reserved for future use and cannot be used by users.

The special page vector table is allocated to the addresses from FFE00$_{16}$ to FFFDB$_{16}$. This vector is used by the JMPS or JSRS instruction. For details, refer to the “M16C/60 and M16C/20 Series Software Manual.”



Internal RAM		Internal ROM	
Size	Address XXXXX$_{16}$	Size	Address YYYYY$_{16}$
1K bytes	007FF$_{16}$	24K bytes	FA000$_{16}$
2K bytes	00BFF$_{16}$	32K bytes	F8000$_{16}$
		48K bytes	F4000$_{16}$
		64K bytes	F0000$_{16}$

Note 1: Shown here is a Block A (2K bytes) and Block B (2K bytes).

Figure 3.1. Memory Map

4. Special Function Register (SFR) Map

Address	Register	Symbol	After reset
0000$_{16}$			
0001$_{16}$			
0002$_{16}$			
0003$_{16}$			
0004$_{16}$	Processor mode register 0 (Note 2)	PM0	00$_{16}$
0005$_{16}$	Processor mode register 1	PM1	00001000$_2$
0006$_{16}$	System clock control register 0	CM0	01001000$_2$
0007$_{16}$	System clock control register 1	CM1	00100000$_2$
0008$_{16}$			
0009$_{16}$	Address match interrupt enable register	AIER	XXXXXX00$_2$
000A$_{16}$	Protect register	PRCR	XX000000$_2$
000B$_{16}$			
000C$_{16}$	Oscillation stop detection register (Note 3)	CM2	0X000000$_2$
000D$_{16}$			
000E$_{16}$	Watchdog timer start register	WDTS	XX$_{16}$
000F$_{16}$	Watchdog timer control register	WDC	00XXXXXX$_2$(Note 4)
0010$_{16}$	Address match interrupt register 0	RMAD0	00$_{16}$
0011$_{16}$			00$_{16}$
0012$_{16}$			X0$_{16}$
0013$_{16}$			
0014$_{16}$	Address match interrupt register 1	RMAD1	00$_{16}$
0015$_{16}$			00$_{16}$
0016$_{16}$			X0$_{16}$
0017$_{16}$			
0018$_{16}$			
0019$_{16}$	Voltage detection register 1 (Note 5)	VCR1	00001000$_2$
001A$_{16}$	Voltage detection register 2 (Note 5)	VCR2	00$_{16}$
001B$_{16}$			
001C$_{16}$			
001D$_{16}$			
001E$_{16}$	Processor mode register 2	PM2	XXX00000$_2$
001F$_{16}$	Voltage down detection interrupt register	D4INT	00$_{16}$
0020$_{16}$	DMA0 source pointer	SAR0	XX$_{16}$
0021$_{16}$			XX$_{16}$
0022$_{16}$			XX$_{16}$
0023$_{16}$			
0024$_{16}$	DMA0 destination pointer	DAR0	XX$_{16}$
0025$_{16}$			XX$_{16}$
0026$_{16}$			XX$_{16}$
0027$_{16}$			
0028$_{16}$	DMA0 transfer counter	TCR0	XX$_{16}$
0029$_{16}$			XX$_{16}$
002A$_{16}$			
002B$_{16}$			
002C$_{16}$	DMA0 control register	DM0CON	00000X00$_2$
002D$_{16}$			
002E$_{16}$			
002F$_{16}$			
0030$_{16}$	DMA1 source pointer	SAR1	XX$_{16}$
0031$_{16}$			XX$_{16}$
0032$_{16}$			XX$_{16}$
0033$_{16}$			
0034$_{16}$	DMA1 destination pointer	DAR1	XX$_{16}$
0035$_{16}$			XX$_{16}$
0036$_{16}$			XX$_{16}$
0037$_{16}$			
0038$_{16}$	DMA1 transfer counter	TCR1	XX$_{16}$
0039$_{16}$			XX$_{16}$
003A$_{16}$			
003B$_{16}$			
003C$_{16}$	DMA1 control register	DM1CON	00000X00$_2$
003D$_{16}$			
003E$_{16}$			
003F$_{16}$			

Note 1: The blank areas are reserved and cannot be accessed by users.
Note 2: The PM00 and PM01 bits do not change at software reset, watchdog timer reset and oscillation stop detection reset.
Note 3: The CM20, CM21, and CM27 bits do not change at oscillation stop detection reset.
Note 4: The WDC5 bit is “0” (cold start) immediately after power-on. It can only be set to “1” in a program. It is set to “0” when the input voltage at the V_{CC1} pin drops to Vdet2 or less while the VC25 bit in the VCR2 register is set to “1” (RAM retention limit detection circuit enable).
X : Nothing is mapped to this bit

Address	Register	Symbol	After reset
0040₁₆			
0041₁₆			
0042₁₆			
0043₁₆			
0044₁₆	INT3 interrupt control register	INT3IC	XX00X000₂
0045₁₆			
0046₁₆			
0047₁₆			
0048₁₆	INT5 interrupt control register	INT5IC	XX00X000₂
0049₁₆	INT4 interrupt control register	INT4IC	XX00X000₂
004A₁₆	UART2 Bus collision detection interrupt control register	BCNIC	XXXXX000₂
004B₁₆	DMA0 interrupt control register	DM0IC	XXXXX000₂
004C₁₆	DMA1 interrupt control register	DM1IC	XXXXX000₂
004D₁₆	Key input interrupt control register	KUPIC	XXXXX000₂
004E₁₆	A/D conversion interrupt control register	ADIC	XXXXX000₂
004F₁₆	UART2 transmit interrupt control register	S2TIC	XXXXX000₂
0050₁₆	UART2 receive interrupt control register	S2RIC	XXXXX000₂
0051₁₆	UART0 transmit interrupt control register	S0TIC	XXXXX000₂
0052₁₆	UART0 receive interrupt control register	S0RIC	XXXXX000₂
0053₁₆	UART1 transmit interrupt control register	S1TIC	XXXXX000₂
0054₁₆	UART1 receive interrupt control register	S1RIC	XXXXX000₂
0055₁₆	Timer A0 interrupt control register	TA0IC	XXXXX000₂
0056₁₆	Timer A1 interrupt control register	TA1IC	XXXXX000₂
0057₁₆	Timer A2 interrupt control register	TA2IC	XXXXX000₂
0058₁₆	Timer A3 interrupt control register	TA3IC	XXXXX000₂
0059₁₆	Timer A4 interrupt control register	TA4IC	XXXXX000₂
005A₁₆	Timer B0 interrupt control register	TB0IC	XXXXX000₂
005B₁₆	Timer B1 interrupt control register	TB1IC	XXXXX000₂
005C₁₆	Timer B2 interrupt control register	TB2IC	XXXXX000₂
005D₁₆	INT0 interrupt control register	INT0IC	XX00X000₂
005E₁₆	INT1 interrupt control register	INT1IC	XX00X000₂
005F₁₆			
0060₁₆			
0061₁₆			
0062₁₆			
0063₁₆			
0064₁₆			
0065₁₆			
0066₁₆			
0067₁₆			
0068₁₆			
0069₁₆			
006A₁₆			
006B₁₆			
006C₁₆			
006D₁₆			
006E₁₆			
006F₁₆			
0070₁₆			
0071₁₆			
0072₁₆			
0073₁₆			
0074₁₆			
0075₁₆			
0076₁₆			
0077₁₆			
0078₁₆			
0079₁₆			
007A₁₆			
007B₁₆			
007C₁₆			
007D₁₆			
007E₁₆			
007F₁₆			

Note :The blank areas are reserved and cannot be accessed by users.

X : Nothing is mapped to this bit

Address	Register	Symbol	After reset
0080₁₆			
0081₁₆			
0082₁₆			
0083₁₆			
0084₁₆			
0085₁₆			
0086₁₆			
≈			≈
01B0₁₆			
01B1₁₆			
01B2₁₆			
01B3₁₆	Flash memory control register 4 (Note 2)	FMR4	01000000₂
01B4₁₆			
01B5₁₆	Flash memory control register 1 (Note 2)	FMR1	0100XX0X₂
01B6₁₆			
01B7₁₆	Flash memory control register 0 (Note 2)	FMR0	XX000001₂
01B8₁₆			
01B9₁₆			
01BA₁₆			
01BB₁₆			
01BC₁₆			
01BD₁₆			
01BE₁₆			
01BF₁₆			
≈			≈
0250₁₆			
0251₁₆			
0252₁₆			
0253₁₆			
0254₁₆			
0255₁₆			
0256₁₆			
0257₁₆			
0258₁₆			
0259₁₆			
025A₁₆			
025B₁₆			
025C₁₆			
025D₁₆			
025E₁₆	Peripheral clock select register	PCLKR	00000011₂
025F₁₆			
≈			≈
0330₁₆			
0331₁₆			
0332₁₆			
0333₁₆			
0334₁₆			
0335₁₆			
0336₁₆			
0337₁₆			
0338₁₆			
0339₁₆			
033A₁₆			
033B₁₆			
033C₁₆			
033D₁₆			
033E₁₆			
033F₁₆			

Note 1: The blank areas are reserved and cannot be accessed by users.
Note 2: This register is included in the flash memory version.

X : Nothing is mapped to this bit

Address	Register	Symbol	After reset
0340₁₆			
0341₁₆			
0342₁₆	Timer A1-1 register	TA11	XX₁₆
0343₁₆			XX₁₆
0344₁₆	Timer A2-1 register	TA21	XX₁₆
0345₁₆			XX₁₆
0346₁₆	Timer A4-1 register	TA41	XX₁₆
0347₁₆			XX₁₆
0348₁₆	Three-phase PWM control register 0	INVC0	00₁₆
0349₁₆	Three-phase PWM control register 1	INVC1	00₁₆
034A₁₆	Three-phase output buffer register 0	IDB0	00₁₆
034B₁₆	Three-phase output buffer register 1	IDB1	00₁₆
034C₁₆	Dead time timer	DTT	XX₁₆
034D₁₆	Timer B2 interrupt occurrence frequency set counter	ICTB2	XX₁₆
034E₁₆			
034F₁₆			
0350₁₆			
0351₁₆			
0352₁₆			
0353₁₆			
0354₁₆			
0355₁₆			
0356₁₆			
0357₁₆			
0358₁₆			
0359₁₆			
035A₁₆			
035B₁₆			
035C₁₆			
035D₁₆			
035E₁₆			
035F₁₆	Interrupt cause select register	IFSR	00₁₆
0360₁₆			
0361₁₆			
0362₁₆			
0363₁₆			
0364₁₆			
0365₁₆			
0366₁₆			
0367₁₆			
0368₁₆			
0369₁₆			
036A₁₆			
036B₁₆			
036C₁₆			
036D₁₆			
036E₁₆			
036F₁₆			
0370₁₆			
0371₁₆			
0372₁₆			
0373₁₆			
0374₁₆	UART2 special mode register 4	U2SMR4	00₁₆
0375₁₆	UART2 special mode register 3	U2SMR3	000X0X0X₂
0376₁₆	UART2 special mode register 2	U2SMR2	X0000000₂
0377₁₆	UART2 special mode register	U2SMR	X0000000₂
0378₁₆	UART2 transmit/receive mode register	U2MR	00₁₆
0379₁₆	UART2 bit rate generator	U2BRG	XX₁₆
037A₁₆	UART2 transmit buffer register	U2TB	XXXXXXXX₂
037B₁₆			XXXXXXXX₂
037C₁₆	UART2 transmit/receive control register 0	U2C0	00001000₂
037D₁₆	UART2 transmit/receive control register 1	U2C1	00000010₂
037E₁₆	UART2 receive buffer register	U2RB	XXXXXXXX₂
037F₁₆			XXXXXXXX₂

Note : The blank areas are reserved and cannot be accessed by users.
X : Nothing is mapped to this bit

Address	Register	Symbol	After reset
038016	Count start flag	TABSR	0016
038116	Clock prescaler reset flag	CPSRF	0XXXXXXX2
038216	One-shot start flag	ONSF	0016
038316	Trigger select register	TRGSR	0016
038416	Up-down flag	UDF	0016
038516			
038616	Timer A0 register	TA0	XX16
038716			XX16
038816	Timer A1 register	TA1	XX16
038916			XX16
038A16	Timer A2 register	TA2	XX16
038B16			XX16
038C16	Timer A3 register	TA3	XX16
038D16			XX16
038E16	Timer A4 register	TA4	XX16
038F16			XX16
039016	Timer B0 register	TB0	XX16
039116			XX16
039216	Timer B1 register	TB1	XX16
039316			XX16
039416	Timer B2 register	TB2	XX16
039516			XX16
039616	Timer A0 mode register	TA0MR	0016
039716	Timer A1 mode register	TA1MR	0016
039816	Timer A2 mode register	TA2MR	0016
039916	Timer A3 mode register	TA3MR	0016
039A16	Timer A4 mode register	TA4MR	0016
039B16	Timer B0 mode register	TB0MR	00XX00002
039C16	Timer B1 mode register	TB1MR	00XX00002
039D16	Timer B2 mode register	TB2MR	00XX00002
039E16	Timer B2 special mode register	TB2SC	XXXXXX002
039F16			
03A016	UART0 transmit/receive mode register	U0MR	0016
03A116	UART0 bit rate generator	U0BRG	XX16
03A216	UART0 transmit buffer register	U0TB	XXXXXXXX2
03A316			XXXXXXXX2
03A416	UART0 transmit/receive control register 0	U0C0	000010002
03A516	UART0 transmit/receive control register 1	U0C1	000000102
03A616	UART0 receive buffer register	U0RB	XXXXXXXX2
03A716			XXXXXXXX2
03A816	UART1 transmit/receive mode register	U1MR	0016
03A916	UART1 bit rate generator	U1BRG	XX16
03AA16	UART1 transmit buffer register	U1TB	XXXXXXXX2
03AB16			XXXXXXXX2
03AC16	UART1 transmit/receive control register 0	U1C0	000010002
03AD16	UART1 transmit/receive control register 1	U1C1	000000102
03AE16	UART1 receive buffer register	U1RB	XXXXXXXX2
03AF16			XXXXXXXX2
03B016	UART transmit/receive control register 2	UCON	X00000002
03B116			
03B216			
03B316			
03B416			
03B516			
03B616			
03B716			
03B816	DMA0 request cause select register	DM0SL	0016
03B916			
03BA16	DMA1 request cause select register	DM1SL	0016
03BB16			
03BC16			
03BD16			
03BE16			
03BF16			

Note : The blank areas are reserved and cannot be accessed by users.
X : Nothing is mapped to this bit

Address	Register	Symbol	After reset
03C0₁₆	A/D register 0	AD0	XXXXXXXX₂
03C1₁₆			XXXXXXXX₂
03C2₁₆	A/D register 1	AD1	XXXXXXXX₂
03C3₁₆			XXXXXXXX₂
03C4₁₆	A/D register 2	AD2	XXXXXXXX₂
03C5₁₆			XXXXXXXX₂
03C6₁₆	A/D register 3	AD3	XXXXXXXX₂
03C7₁₆			XXXXXXXX₂
03C8₁₆	A/D register 4	AD4	XXXXXXXX₂
03C9₁₆			XXXXXXXX₂
03CA₁₆	A/D register 5	AD5	XXXXXXXX₂
03CB₁₆			XXXXXXXX₂
03CC₁₆	A/D register 6	AD6	XXXXXXXX₂
03CD₁₆			XXXXXXXX₂
03CE₁₆	A/D register 7	AD7	XXXXXXXX₂
03CF₁₆			XXXXXXXX₂
03D0₁₆			
03D1₁₆			
03D2₁₆			
03D3₁₆			
03D4₁₆	A/D control register 2	ADCON2	00₁₆
03D5₁₆			
03D6₁₆	A/D control register 0	ADCON0	00000XXX₂
03D7₁₆	A/D control register 1	ADCON1	00₁₆
03D8₁₆			
03D9₁₆			
03DA₁₆			
03DB₁₆			
03DC₁₆			
03DD₁₆			
03DE₁₆			
03DF₁₆			
03E0₁₆			
03E1₁₆	Port P1 register	P1	XX₁₆
03E2₁₆			
03E3₁₆	Port P1 direction register	PD1	00₁₆
03E4₁₆			
03E5₁₆			
03E6₁₆			
03E7₁₆			
03E8₁₆			
03E9₁₆			
03EA₁₆			
03EB₁₆			
03EC₁₆	Port P6 register	P6	XX₁₆
03ED₁₆	Port P7 register	P7	XX₁₆
03EE₁₆	Port P6 direction register	PD6	00₁₆
03EF₁₆	Port P7 direction register	PD7	00₁₆
03F0₁₆	Port P8 register	P8	XX₁₆
03F1₁₆	Port P9 register	P9	XX₁₆
03F2₁₆	Port P8 direction register	PD8	00X00000₂
03F3₁₆	Port P9 direction register	PD9	00₁₆
03F4₁₆	Port P10 register	P10	XX₁₆
03F5₁₆			
03F6₁₆	Port P10 direction register	PD10	00₁₆
03F7₁₆			
03F8₁₆			
03F9₁₆			
03FA₁₆			
03FB₁₆			
03FC₁₆	Pull-up control register 0	PUR0	00₁₆
03FD₁₆	Pull-up control register 1	PUR1	00₁₆
03FE₁₆	Pull-up control register 2	PUR2	00₁₆
03FF₁₆	Port control register	PCR	00₁₆

Note 1: The blank areas are reserved and cannot be accessed by users.

X : Nothing is mapped to this bit

5. Electrical Characteristics

5.1 Absolute Maximum Ratings

Table 16.1. Absolute Maximum Ratings

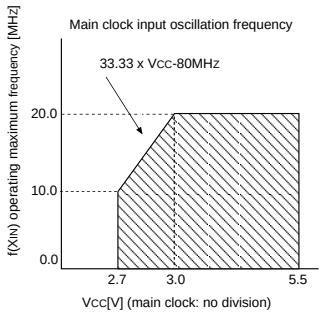
Symbol	Parameter		Condition	Rated value	Unit
V_{CC}	Supply voltage		V_{CC}=AV_{CC}	-0.3 to 6.5	V
AV_{CC}	Analog supply voltage		V_{CC}=AV_{CC}	-0.3 to 6.5	V
V_I	Input voltage	$\overline{RESET}$, CNV_{SS}, $P1_5$ to $P1_7$, $P6_0$ to $P6_7$, $P7_2$ to $P7_7$, $P8_0$ to $P8_3$, $P8_5$ to $P8_7$, $P9_0$ to $P9_3$, $P10_0$ to $P10_7$, V_{REF}, X_{IN}		-0.3 to V_{CC}+0.3	V
		$P7_0$, $P7_1$		-0.3 to 6.5	V
V_O	Output voltage	$P1_5$ to $P1_7$, $P6_0$ to $P6_7$, $P7_2$ to $P7_7$, $P8_0$ to $P8_3$, $P8_5$ to $P8_7$, $P9_0$ to $P9_3$, $P10_0$ to $P10_7$, X_{OUT}		-0.3 to V_{CC}+0.3	V
		$P7_0$, $P7_1$		-0.3 to 6.5	V
P_d	Power dissipation		Topr=25 °C	300	mW
T_{opr}	Operating ambient temperature			-20 to 85 / -40 to 85	°C
T_{stg}	Storage temperature			-65 to 150	°C

5.2 Recommended Operating Conditions

Table 1.26.2. Recommended Operating Conditions (Note 1)

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
VCC	Supply voltage		2.7		5.5	V
AVcc	Analog supply voltage			VCC		V
Vss	Supply voltage			0		V
AVss	Analog supply voltage			0		V
VIH	HIGH input voltage	$\overline{RESET}$, CNVSS, XIN, P15 to P17, P60 to P67, P72 to P77, P80 to P83, P85 to P87, P90 to P93, P100 to P107	0.8VCC		VCC	V
		P70 , P71	0.8VCC		6.5	V
VIL	LOW input voltage	$\overline{RESET}$, CNVSS, XIN, P15 to P17, P60 to P67, P70 to P77, P80 to P83, P85 to P87, P90 to P93, P100 to P107	0		0.2VCC	V
IOH (peak)	HIGH peak output current	P15 to P17, P60 to P67, P72 to P77, P80 to P83, P85 to P87, P90 to P93, P100 to P107			-10.0	mA
IOH (avg)	HIGH average output current	P15 to P17, P60 to P67, P72 to P77, P80 to P83, P85 to P87, P90 to P93, P100 to P107			-5.0	mA
IOL (peak)	LOW peak output current	P15 to P17, P60 to P67, P72 to P77, P80 to P83, P85 to P87, P90 to P93, P100 to P107			10.0	mA
IOL (avg)	LOW average output current	P15 to P17, P60 to P67, P72 to P77, P80 to P83, P85 to P87, P90 to P93, P100 to P107			5.0	mA
f (XIN)	Main clock input oscillation frequency (Note 4)	VCC=3.0 to 5.5V	0		20	MHz
		VCC=2.7 to 3.0V	0		33.33 X VCC-80	MHz
f (XCIN)	Sub-clock oscillation frequency			32.768	50	kHz
f (Ring)	On-chip oscillation frequency			1		MHz
f (BCLK)	CPU operation clock		0		20	MHz

Note 1: Referenced to VCC = 2.7 to 5.5V at Topr = -20 to 85 °C / -40 to 85 °C unless otherwise specified.
Note 2: The mean output current is the mean value within 100ms.
Note 3: The total IOL (peak) for all ports must be 80mA max. The total IOL (peak) for all ports must be -80mA max.
Note 4: Relationship between main clock oscillation frequency and supply voltage.



5.3 A/D Conversion Characteristics

Table 16.3. A/D Conversion Characteristics (Note 1)

Symbol	Parameter		Measuring condition		Standard Min.	Standard Typ.	Standard Max.	Unit
–	Resolution		V_{REF} =V_{CC}				10	Bits
INL	Integral non-linearity error	10 bit	V_{REF}=V_{CC}=5V	AN_0 to AN_7 input			±3	LSB
			V_{REF}=V_{CC}=3.3V	AN_0 to AN_7 input			±5	LSB
		8 bit	V_{REF} =V_{CC}=3.3V				±2	LSB
–	Absolute accuracy	10 bit	V_{REF}=V_{CC}=5V	AN_0 to AN_7 input			±3	LSB
			V_{REF}=V_{CC}=3.3V	AN_0 to AN_7 input			±5	LSB
		8 bit	V_{REF} =V_{CC}=3.3V				±2	LSB
DNL	Differential non-linearity error						±1	LSB
–	Offset error						±3	LSB
–	Gain error						±3	LSB
R_{LADDER}	Ladder resistance		V_{REF} =V_{CC}		10		40	kΩ
t_{CONV}	Conversion time(10bit), Sample & hold function available		V_{REF} =V_{CC}=5V, $ø_{AD}$=10MHz		3.3			µs
t_{CONV}	Conversion time(8bit), Sample & hold function available		V_{REF} =V_{CC}=5V, $ø_{AD}$=10MHz		2.8			µs
t_{SAMP}	Sampling time				0.3			µs
V_{REF}	Reference voltage				2.0		V_{CC}	V
V_{IA}	Analog input voltage				0		V_{REF}	V

Note 1: Referenced to V_{CC}=AV_{CC}=V_{REF}=3.3 to 5.5V, V_{SS}=AV_{SS}=0V at Topr = -20 to 85 °C / -40 to 85 °C unless otherwise specified.
Note 2: AD operation clock frequency ($Ø_{AD}$ frequency) must be 10 MHz or less. And divide the f_{AD} if V_{CC} is less than 4.2V, and make $Ø_{AD}$ frequency equal to or lower than f_{AD}/2.
Note 3: A case without sample & hold function turn $Ø_{AD}$ frequency into 250 kHz or more in addition to a limit of Note 2.
A case with sample & hold function turn $Ø_{AD}$ frequency into 1MHz or more in addition to a limit of Note 2.

5.4 Flash Memory Version Electrical Characteristics

Table 16.4. Flash Memory Version Electrical Characteristics (Note 1) 100E/W cycle products (D3, D5, U3, U5))

Symbol	Parameter		Standard			Unit
			Min.	Typ. (Note 2)	Max	
–	Erase/Write cycle (Note 3)		100(Note 4)			cycle
–	Word program time (Vcc=5.0V, Topr=25°C)			75	600	µs
–	Block erase time	2Kbyte block		0.2	9	s
		8Kbyte block		0.4	9	s
		16Kbyte block		0.7	9	s
		32Kbyte block		1.2	9	s
td(SR-ES)	Time delay from Suspend Request until Erase Suspend				8	ms
–	Data retention time (Note 5)		20			year

Table 16.5. Flash Memory Version Electrical Characteristics (Note 6) 10000 E/W cycle products (D7, D9, U7, U9) [blockA and block B(Note 7)]

Symbol	Parameter	Standard			Unit
		Min.	Typ. (Note 2)	Max	
–	Erase/Write cycle (Note 3, 8, 9)	10000(Note 4,10)			cycle
–	Word program time (Vcc=5.0V, Topr=25°C)		100		µs
–	Block erase time(Vcc=5.0V, Topr=25°C) (2Kbyte block)		0.3		s
td(SR-ES)	Time delay from Suspend Request until Erase Suspend			8	ms

Note 1: When not otherwise specified, Vcc = 2.7 to5.5V; Topr = 0 to 60 °C.
Note 2: VCC = 5V; TOPR = 25 °C.
Note 3: Definition of E/W cycle: Each block may be written to a variable number of times - up to a maximum of the total number of distinct word addresses - for every block erase. Performing multiple writes to the same address before an erase operation is prohibited.
Note 4: Maximum number of E/W cycles for which opration is guaranteed.
Note 5: Topr = 55°C.
Note 6: When not otherwise specified, Vcc = 2.7 to 5.5V; Topr = -40 to 85°C (D7, U7) / -20 to 85°C (D9, U9).
Note 7: Table18.5 applies for Block A or B E/W cycles > 1000. Otherwise, use Table 18.4.
Note 8: To reduce the number of E/W cycles, a block erase should ideally be performed after writing as many different word addresses (only one time each) as possible. It is important to track the total number of block erases.
Note 9: Should erase error occur during block erase, attempt to execute clear status register command, then clock erase command at least three times until erase error disappears.
Note 10: When Block A or B E/W cycles exceed 100 (D7, D9, U7, U9), select one wait state per block access. When FMR 17 is set to "1", one wait state is inserted per access to Block A or B - regardless of the value of PM17. Wait state insertion during access to all other blocks, as well as to internal RAM, is controlled by PM17 - regardless of the setting of FMR17.
Note 11: Customers desiring E/W failure rate information should contact their Renesas technical support representative.

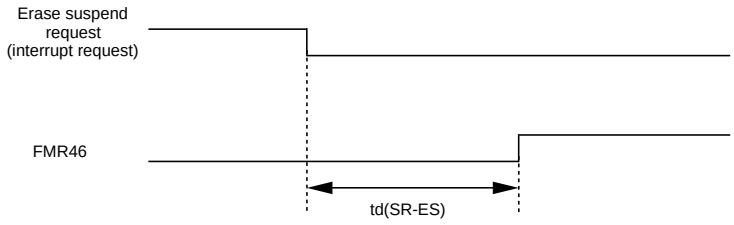


Table 16.6. Flash Memory Version Program/Erase Voltage and Read Operation Voltage Characteristics (at Topr = 0 to 60°C)

Flash program, erase voltage	Flash read operation voltage
Vcc = 2.7 V to 5.5 V	Vcc=2.7 to 5.5 V

5.5 Low Voltage Detection Circuit Electrical Charactristics

Table 16.7. Low Voltage Detection Circuit Electrical Characteristics (Note 1, Note 4)

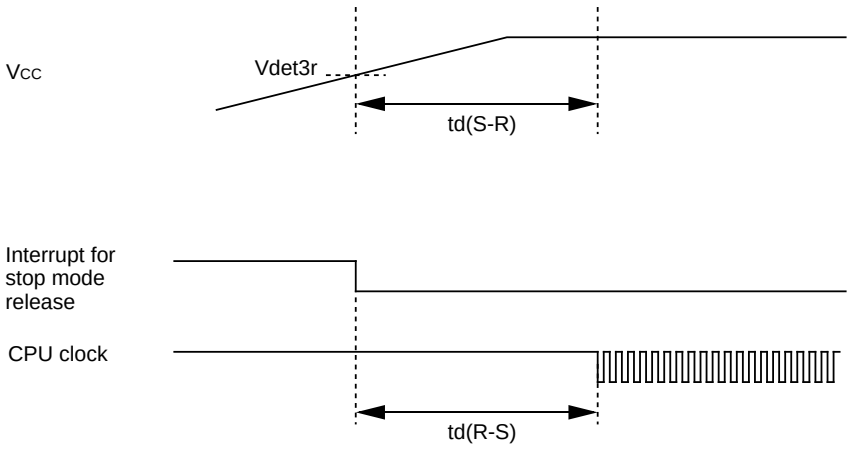
Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max.	
Vdet4	Voltage down detection voltage (Note 1)	VCC1=0.8 to 5.5V	3.3	3.8	4.4	V
Vdet3	Reset level detection voltage (Notes 1, 2)		2.2	2.8	3.6	V
Vdet3s	Low voltage reset retention voltage		0.8			V
Vdet3r	Low voltage reset release voltage (Note 3)		2.2	2.9	4.0	V

Note 1: Vdet4 > Vdet3
Note 2: Where reset level detection voltage is less than 2.7 V, if the supply power voltage is greater than the reset level detection voltage, the operation at f(BCLK) ≤ 10MHz is guaranteed.
Note 3: Vdet3r > Vdet3 is not guaranteed.
Note 4: The low voltage detection circuit is designed to use when VCC is set to 5V.

Table 16.8. Power Supply Circuit Timing Characteristics

Symbol	Parameter	Measuring condition	Standard			Unit
			Min.	Typ.	Max.	
td(P-R)	Time for internal power supply stabilization during powering-on	VCC1=2.7 to 5.5V			2	ms
td(R-S)	STOP release time				150	µs
td(W-S)	Low power dissipation mode wait mode release time				150	µs
td(M-L)	Time for internal power supply stabilization when main clock oscillation starts				50	µs
td(S-R)	Hardware reset 2 release wait time	VCC1=Vdet3r to 5.5V		6 (Note)	20	ms
td(E-A)	Low voltage detection circuit operation start time	VCC1=2.7 to 5.5V			20	µs

Note : When VCC = 5V



5.6 Electrical Charactristics (VCC=5V)

VCC = 5V

Table 16.9. Electrical Characteristics (Note 1)

Symbol	Parameter		Measuring condition	Standard			Unit
				Min.	Typ.	Max.	
VOH	HIGH output voltage P15 to P17, P60 to P67,P72 to P77,P80 to P83, P85 to P87,P90 to P93, P100 to P107		IOH=-5mA	VCC-2.0		VCC	V
VOH	HIGH output voltage P15 to P17, P60 to P67,P72 to P77,P80 to P83, P85 to P87,P90 to P93, P100 to P107		IOH=-200µA	VCC-0.3		VCC	V
VOH	HIGH output voltage XOUT	HIGHPOWER	IOH=-1mA	VCC-2.0		VCC	V
		LOWPOWER	IOH=-0.5mA	VCC-2.0		VCC	
	HIGH output voltage XCOUT	HIGHPOWER	With no load applied		2.5		V
		LOWPOWER	With no load applied		1.6		
VOL	LOW output voltage P15 to P17, P60 to P67,P72 to P77,P80 to P83, P85 to P87,P90 to P93, P100 to P107		IOL=5mA			2.0	V
VOL	LOW output voltage P15 to P17, P60 to P67,P72 to P77,P80 to P83, P85 to P87,P90 to P93, P100 to P107		IOL=200µA			0.45	V
VOL	LOW output voltage XOUT	HIGHPOWER	IOL=1mA			2.0	V
		LOWPOWER	IOL=0.5mA			2.0	
	LOW output voltage XCOUT	HIGHPOWER	With no load applied		0		V
		LOWPOWER	With no load applied		0		
VT+-VT-	Hysteresis TA0IN to TA4IN, TB0IN to TB2IN, INT0 to INT1,INT3 to INT5,NMI, ADTRG, SCL, SDA, RxD0 to RxD2, CTS0 to CTS2, CLK0 to CLK2, TA2OUT to TA4OUT, KI0 to KI3			0.2		1.0	V
VT+-VT-	Hysteresis RESET			0.2		2.5	V
IIH	HIGH input current P15 to P17, P60 to P67, P70 to P77, P80 to P83, P85 to P87, P90 to P93, P100 to P107, XIN, RESET, CNVss		VI=5V			5.0	µA
IIL	LOW input current P15 to P17, P60 to P67, P70 to P77, P80 to P83, P85 to P87, P90 to P93, P100 to P107, XIN, RESET, CNVss		VI=0V			-5.0	µA
RPULLUP	Pull-up resistance P15 to P17, P60 to P67,P72 to P77,P80 to P83, P85 to P87,P90 to P93, P100 to P107		VI=0V	30	50	170	kΩ
RIXIN	Feedback resistance XIN				1.5		MΩ
RIXCIN	Feedback resistance XCIN				15		MΩ
VRAM	RAM retention voltage		At stop mode	2.0			V

Note 1: Referenced to VCC=4.2 to 5.5V, VSS=0V at Topr = -20 to 85 °C / -40 to 85 °C, f(BCLK)=20MHz unless otherwise specified.

VCC = 5V

Table 16.10. Electrical Characteristics (2) (Note 1)

Symbol	Parameter		Measuring condition		Standard			Unit
					Min.	Typ.	Max.	
ICC	Power supply current (VCC=3.0 to 5.5V)	In single-chip mode, the output pins are open and other pins are VSS	Mask ROM	f(BCLK)=20MHz, No division		16	19	mA
				No division, On-chip oscillation		T.B.D		mA
			Flash memory Program	f(BCLK)=10MHz, VCC=5.0V		T.B.D		mA
			Flash memory Erase	f(BCLK)=10MHz, VCC=5.0V		T.B.D		mA
			Flash memory	f(BCLK)=32kHz, Low power dissipation mode, RAM(Note 3)		25		µA
				f(BCLK)=32kHz Low power dissipation mode, Flash memory(Note 3)		420		µA
				On-chip oscillation, Wait mode		T.B.D		µA
			Flash memory	f(BCLK)=32kHz, Wait mode (Note 2), Oscillation capacity High		7.5		µA
				f(BCLK)=32kHz, Wait mode(Note 2), Oscillation capacity Low		2.0		µA
				Stop mode, Topr=25°C		0.8	3.0	µA

Note 1: Referenced to VCC==4.2 to 5.5V, VSS=0V at Topr = -20 to 85 °C / -40 to 85 °C, f(BCLK)=20MHz unless otherwise specified.
Note 2: With one timer operated using fC32.
Note 3: This indicates the memory in which the program to be executed exists.

5.7 Timing Requirements (VCC=5V)

VCC = 5V

(VCC = 5V, VSS = 0V, at Topr = – 20 to 85°C / – 40 to 85°C unless otherwise specified)

Table 16.11. External Clock Input (XIN input)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t_c	External clock input cycle time	50		ns
$t_{w(H)}$	External clock input HIGH pulse width	25		ns
$t_{w(L)}$	External clock input LOW pulse width	25		ns
t_r	External clock rise time		15	ns
t_f	External clock fall time		15	ns

VCC = 5V

Timing Requirements

(VCC = 5V, VSS = 0V, at Topr = – 20 to 85°C / – 40 to 85°C unless otherwise specified)

Table 16.12. Timer A Input (Counter Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	100		ns
$t_{w(TAH)}$	TAiIN input HIGH pulse width	40		ns
$t_{w(TAL)}$	TAiIN input LOW pulse width	40		ns

Table 16.13. Timer A Input (Gating Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	400		ns
$t_{w(TAH)}$	TAiIN input HIGH pulse width	200		ns
$t_{w(TAL)}$	TAiIN input LOW pulse width	200		ns

Table 16.14. Timer A Input (External Trigger Input in One-shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	200		ns
$t_{w(TAH)}$	TAiIN input HIGH pulse width	100		ns
$t_{w(TAL)}$	TAiIN input LOW pulse width	100		ns

Table 16.15. Timer A Input (External Trigger Input in Pulse Width Modulation Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(TAH)}$	TAiIN input HIGH pulse width	100		ns
$t_{w(TAL)}$	TAiIN input LOW pulse width	100		ns

Table 16.16. Timer A Input (Counter Increment/decrement Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(UP)}$	TAiOUT input cycle time	2000		ns
$t_{w(UPH)}$	TAiOUT input HIGH pulse width	1000		ns
$t_{w(UPL)}$	TAiOUT input LOW pulse width	1000		ns
$t_{su(UP-TIN)}$	TAiOUT input setup time	400		ns
$t_{h(TIN-UP)}$	TAiOUT input hold time	400		ns

Table 16.17. Timer A Input (Two-phase Pulse Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	800		ns
$t_{su(TAIN-TAOUT)}$	TAiOUT input setup time	200		ns
$t_{su(TAOUT-TAIN)}$	TAiIN input setup time	200		ns

VCC = 5V

Timing Requirements

(VCC = 5V, VSS = 0V, at Topr = – 20 to 85°C / – 40 to 85°C unless otherwise specified)

Table 16.18. Timer B Input (Counter Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time (counted on one edge)	100		ns
$t_{w(TBH)}$	TBiIN input HIGH pulse width (counted on one edge)	40		ns
$t_{w(TBL)}$	TBiIN input LOW pulse width (counted on one edge)	40		ns
$t_{c(TB)}$	TBiIN input cycle time (counted on both edges)	200		ns
$t_{w(TBH)}$	TBiIN input HIGH pulse width (counted on both edges)	80		ns
$t_{w(TBL)}$	TBiIN input LOW pulse width (counted on both edges)	80		ns

Table 16.19. Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time	400		ns
$t_{w(TBH)}$	TBiIN input HIGH pulse width	200		ns
$t_{w(TBL)}$	TBiIN input LOW pulse width	200		ns

Table 16.20. Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time	400		ns
$t_{w(TBH)}$	TBiIN input HIGH pulse width	200		ns
$t_{w(TBL)}$	TBiIN input LOW pulse width	200		ns

Table 16.21. A/D Trigger Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(AD)}$	$\overline{\text{ADTRG}}$ input cycle time (trigger able minimum)	1000		ns
$t_{w(ADL)}$	$\overline{\text{ADTRG}}$ input LOW pulse width	125		ns

Table 16.22. Serial I/O

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	200		ns
$t_{w(CKH)}$	CLKi input HIGH pulse width	100		ns
$t_{w(CKL)}$	CLKi input LOW pulse width	100		ns
$t_{d(C-Q)}$	TxDi output delay time		80	ns
$t_{h(C-Q)}$	TxDi hold time	0		ns
$t_{su(D-C)}$	RxDi input setup time	30		ns
$t_{h(C-D)}$	RxDi input hold time	90		ns

Table 16.23. External Interrupt $\overline{\text{INTi}}$ Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{\text{INTi}}$ input HIGH pulse width	250		ns
$t_{w(INL)}$	$\overline{\text{INTi}}$ input LOW pulse width	250		ns

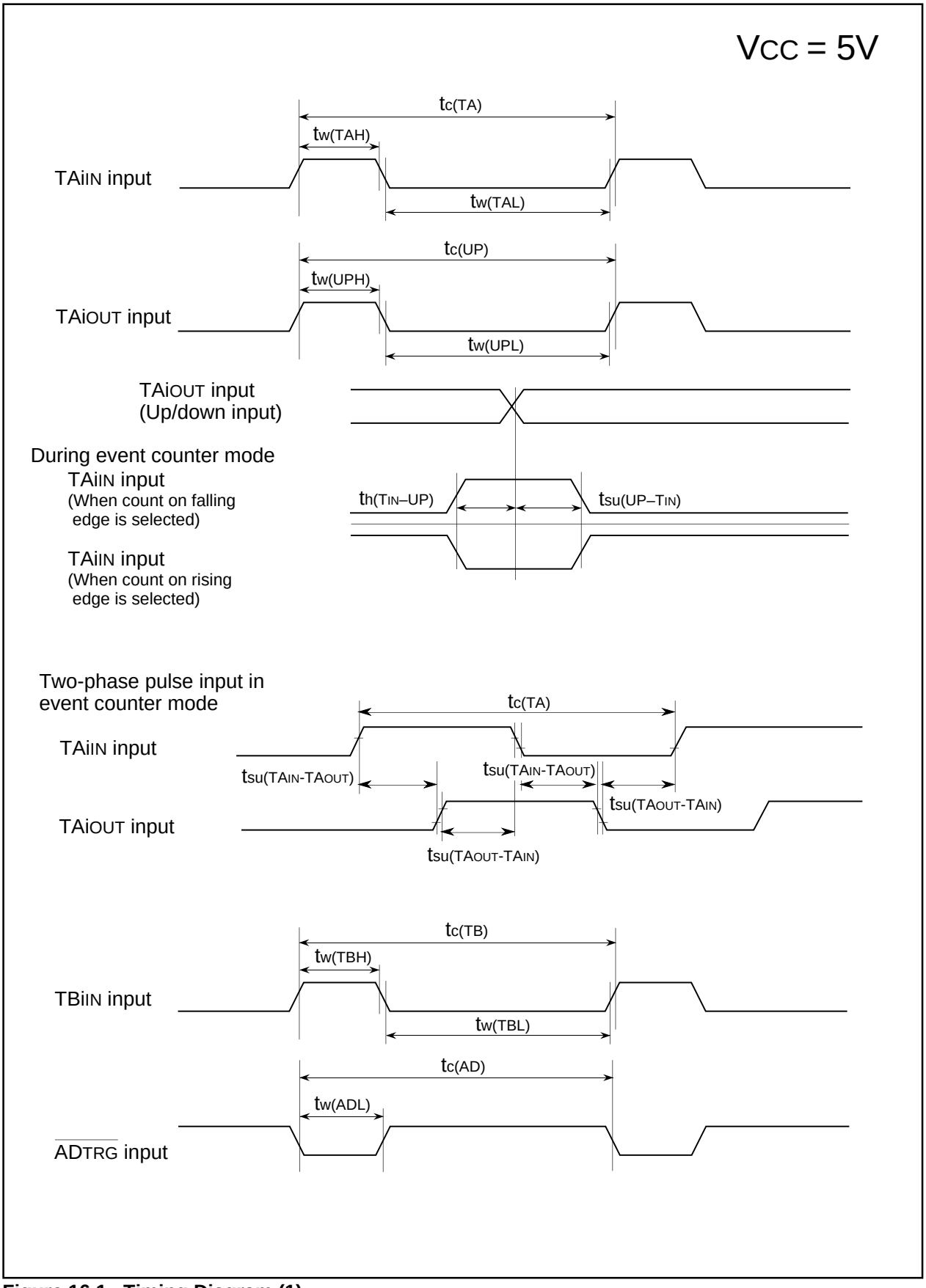


Figure 16.1. Timing Diagram (1)

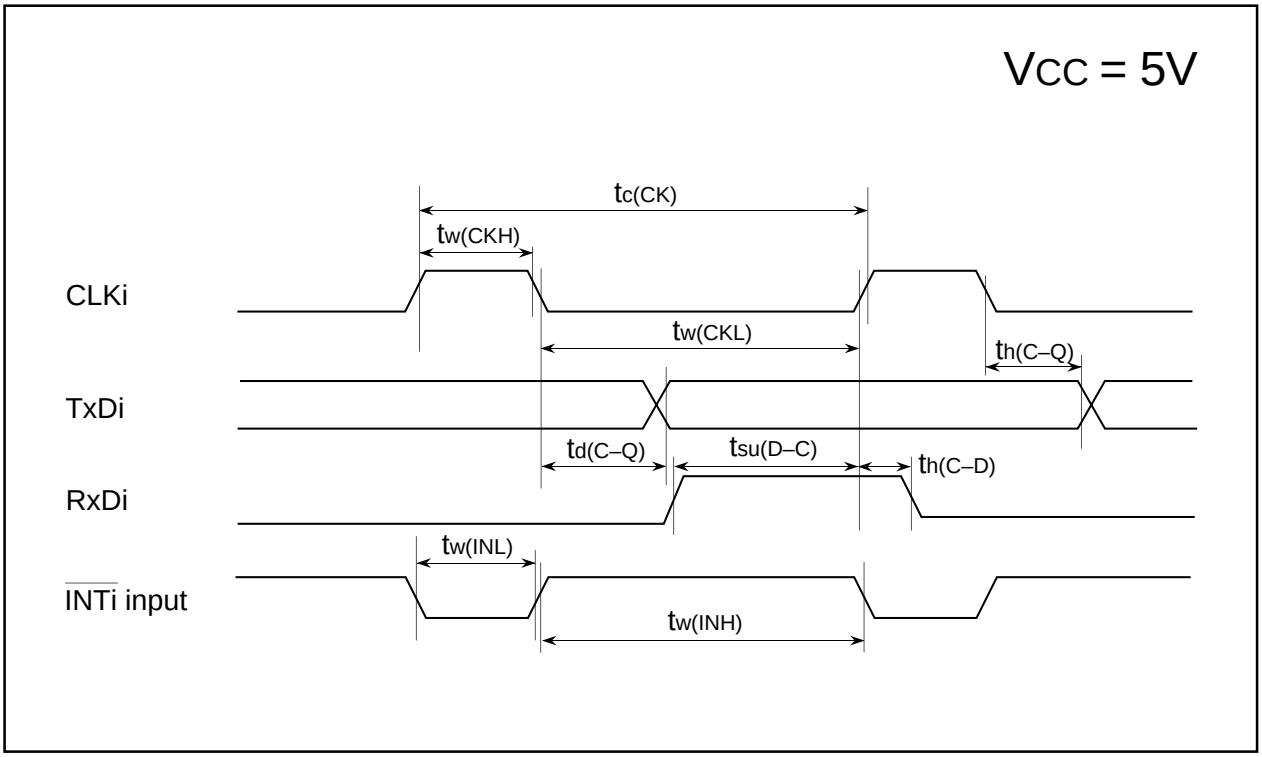


Figure 16.2. Timing Diagram (2)

VCC = 3V

5.8 Electrical Charactristics (VCC=3V)

Table 16.24. Electrical Characteristics (Note)

Symbol	Parameter		Measuring condition	Standard			Unit
				Min.	Typ.	Max.	
VOH	HIGH output voltage P15 to P17, P60 to P67, P72 to P77, P80 to P83, P85 to P87, P90 to P93, P100 to P107		IOH=-1mA	VCC-0.5		VCC	V
VOH	HIGH output voltage XOUT	HIGHPOWER	IOH=-0.1mA	VCC-0.5		VCC	V
		LOWPOWER	IOH=-50µA	VCC-0.5		VCC	
	HIGH output voltage XCOUT	HIGHPOWER	With no load applied		2.5		V
		LOWPOWER	With no load applied		1.6		
VOL	LOW output voltage P15 to P17, P60 to P67, P72 to P77, P80 to P83, P85 to P87, P90 to P93, P100 to P107		IOL=1mA			0.5	V
VOL	LOW output voltage XOUT	HIGHPOWER	IOL=0.1mA			0.5	V
		LOWPOWER	IOL=50µA			0.5	
	LOW output voltage XCOUT	HIGHPOWER	With no load applied		0		V
		LOWPOWER	With no load applied		0		
VT+-VT-	Hysteresis TA0IN to TA4IN, TB0IN to TB2IN, INT0 to INT1, INT3 to INT5, NMI, ADTRG, SCL, SDA, RxD0 to RxD2, CTS0 to CTS2, CLK0 to CLK2, TA2OUT to TA4OUT, KI0 to KI3			0.2		0.8	V
VT+-VT-	Hysteresis RESET			0.2		1.8	V
IIH	HIGH input current P15 to P17, P60 to P67, P70 to P77, P80 to P83, P85 to P87, P90 to P93, P100 to P107, XIN, RESET, CNVss		VI=3V			4.0	µA
IIL	LOW input current P15 to P17, P60 to P67, P70 to P77, P80 to P83, P85 to P87, P90 to P93, P100 to P107, XIN, RESET, CNVss		VI=0V			-4.0	µA
RPULLUP	Pull-up resistance P15 to P17, P60 to P67, P72 to P77, P80 to P83, P85 to P87, P90 to P93, P100 to P107		VI=0V	50	100	500	kΩ
RfXIN	Feedback resistance XIN				3.0		MΩ
RfXCIN	Feedback resistance XCIN				25		MΩ
VRAM	RAM retention voltage		At stop mode	2.0			V

Note 1 : Referenced to VCC=2.7 to 3.3V, VSS=0V at Topr = -20 to 85 °C / -40 to 85 °C, f(BCLK)=10MHz unless otherwise specified.

VCC = 3V

Table 16.25. Electrical Characteristics (2) (Note 1)

Symbol	Parameter		Measuring condition		Standard			Unit
					Min.	Typ.	Max.	
ICC	Power supply current (VCC=2.7 to 3.6V)	In single-chip mode, the output pins are open and other pins are VSS	Flash memory	f(BCLK)=10MHz, No division		8	13	mA
				No division, On-chip oscillation		T.B.D		mA
			Flash memory Program	f(BCLK)=10MHz, VCC1=3.0V		T.B.D		mA
			Flash memory Erase	f(BCLK)=10MHz, VCC1=3.0V		T.B.D		mA
			Flash memory	f(BCLK)=32kHz, Low power dissipation mode, RAM(Note 3)		25		µA
				f(BCLK)=32kHz, Low power dissipation mode, Flash memory(Note 3)		420		µA
				On-chip oscillation, Wait mode		T.B.D		µA
			Flash memory	f(BCLK)=32kHz, Wait mode (Note 2), Oscillation capacity High		6.0		µA
				f(BCLK)=32kHz, Wait mode (Note 2), Oscillation capacity Low		1.8		µA
				Stop mode, Topr=25°C		0.7	3.0	µA

Note 1: Referenced to VCC=2.7 to 3.3V, VSS=0V at Topr = -20 to 85 °C / -40 to 85 °C, f(BCLK)=10MHz unless otherwise specified.
Note 2: With one timer operated using fC32.
Note 3: This indicates the memory in which the program to be executed exists.

VCC = 3V

5.9 Timing Requirements (VCC=3V)

Timing Requirements

(VCC = 3V, VSS = 0V, at Topr = – 20 to 85°C / – 40 to 85°C unless otherwise specified)

Table 16.26. External Clock Input (XIN input)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t_c	External clock input cycle time	100		ns
$t_{w(H)}$	External clock input HIGH pulse width	40		ns
$t_{w(L)}$	External clock input LOW pulse width	40		ns
t_r	External clock rise time		18	ns
t_f	External clock fall time		18	ns

VCC = 3V

Timing Requirements

(VCC = 3V, VSS = 0V, at Topr = – 20 to 85°C / – 40 to 85°C unless otherwise specified)

Table 16.27. Timer A Input (Counter Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	150		ns
$t_{w(TAH)}$	TAiIN input HIGH pulse width	60		ns
$t_{w(TAL)}$	TAiIN input LOW pulse width	60		ns

Table 16.28. Timer A Input (Gating Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	600		ns
$t_{w(TAH)}$	TAiIN input HIGH pulse width	300		ns
$t_{w(TAL)}$	TAiIN input LOW pulse width	300		ns

Table 16.29. Timer A Input (External Trigger Input in One-shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	300		ns
$t_{w(TAH)}$	TAiIN input HIGH pulse width	150		ns
$t_{w(TAL)}$	TAiIN input LOW pulse width	150		ns

Table 16.30. Timer A Input (External Trigger Input in Pulse Width Modulation Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(TAH)}$	TAiIN input HIGH pulse width	150		ns
$t_{w(TAL)}$	TAiIN input LOW pulse width	150		ns

Table 16.31. Timer A Input (Counter Increment/decrement Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(UP)}$	TAiOUT input cycle time	3000		ns
$t_{w(UPH)}$	TAiOUT input HIGH pulse width	1500		ns
$t_{w(UPL)}$	TAiOUT input LOW pulse width	1500		ns
$t_{su(UP-TIN)}$	TAiOUT input setup time	600		ns
$t_{h(TIN-UP)}$	TAiOUT input hold time	600		ns

Table 1.6.32. Timer A Input (Two-phase Pulse Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	2		µs
$t_{su(TAIN-TAOUT)}$	TAiOUT input setup time	500		ns
$t_{su(TAOUT-TAIN)}$	TAiIN input setup time	500		ns

VCC = 3V

Timing Requirements

(VCC = 3V, VSS = 0V, at Topr = – 20 to 85°C / – 40 to 85°C unless otherwise specified)

Table 16.33. Timer B Input (Counter Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time (counted on one edge)	150		ns
$t_{w(TBH)}$	TBiIN input HIGH pulse width (counted on one edge)	60		ns
$t_{w(TBL)}$	TBiIN input LOW pulse width (counted on one edge)	60		ns
$t_{c(TB)}$	TBiIN input cycle time (counted on both edges)	300		ns
$t_{w(TBH)}$	TBiIN input HIGH pulse width (counted on both edges)	120		ns
$t_{w(TBL)}$	TBiIN input LOW pulse width (counted on both edges)	120		ns

Table 16.34. Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time	600		ns
$t_{w(TBH)}$	TBiIN input HIGH pulse width	300		ns
$t_{w(TBL)}$	TBiIN input LOW pulse width	300		ns

Table 16.35. Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time	600		ns
$t_{w(TBH)}$	TBiIN input HIGH pulse width	300		ns
$t_{w(TBL)}$	TBiIN input LOW pulse width	300		ns

Table 16.36. A/D Trigger Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(AD)}$	$\overline{ADTRG}$ input cycle time (trigger able minimum)	1500		ns
$t_{w(ADL)}$	$\overline{ADTRG}$ input LOW pulse width	200		ns

Table 16.37. Serial I/O

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	300		ns
$t_{w(CKH)}$	CLKi input HIGH pulse width	150		ns
$t_{w(CKL)}$	CLKi input LOW pulse width	150		ns
$t_{d(C-Q)}$	TxDi output delay time		160	ns
$t_{h(C-Q)}$	TxDi hold time	0		ns
$t_{su(D-C)}$	RxDi input setup time	50		ns
$t_{h(C-D)}$	RxDi input hold time	90		ns

Table 16.38. External Interrupt $\overline{INTi}$ Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ input HIGH pulse width	380		ns
$t_{w(INL)}$	$\overline{INTi}$ input LOW pulse width	380		ns

Vcc = 3V

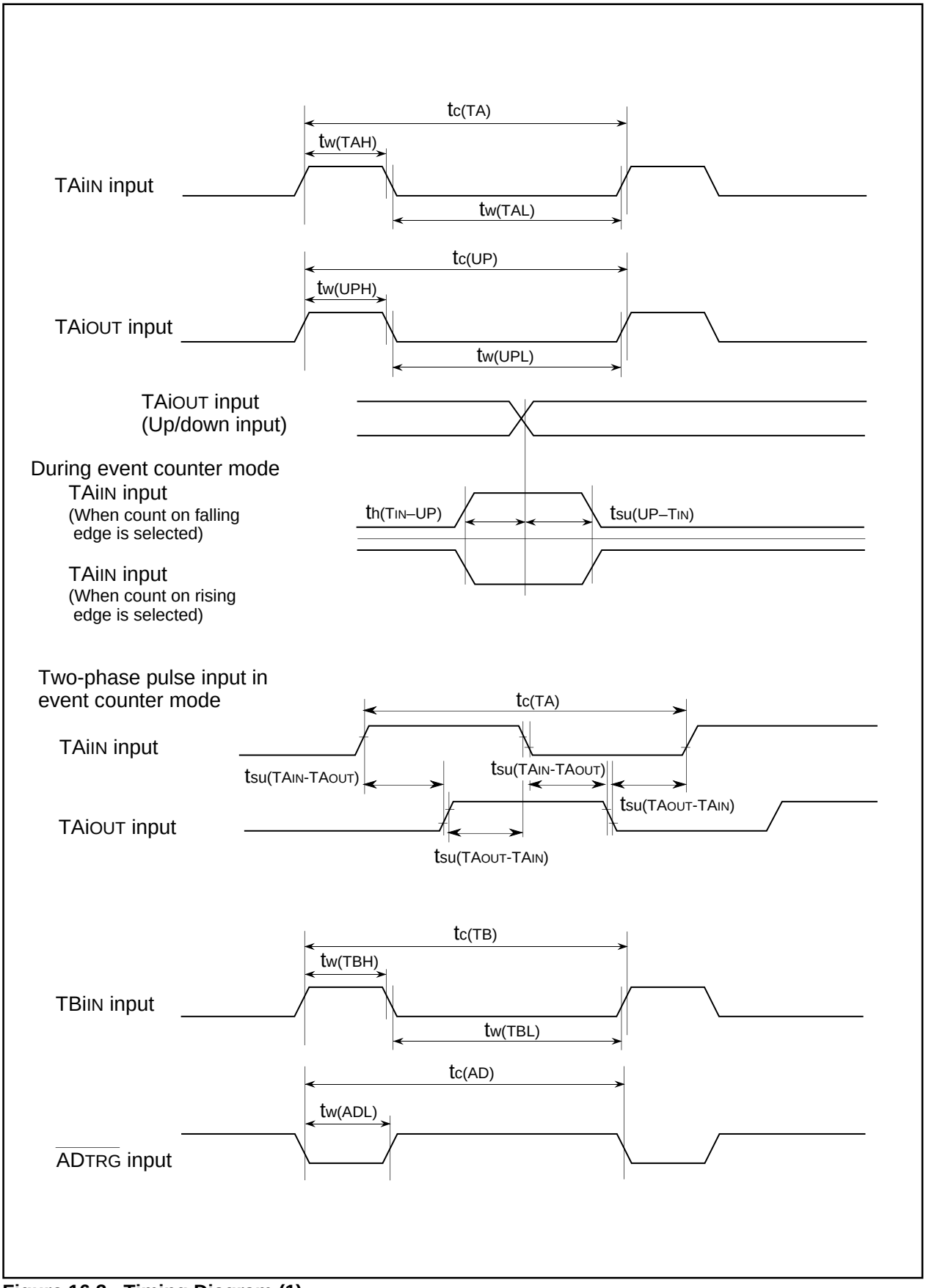


Figure 16.3. Timing Diagram (1)

Vcc = 3V

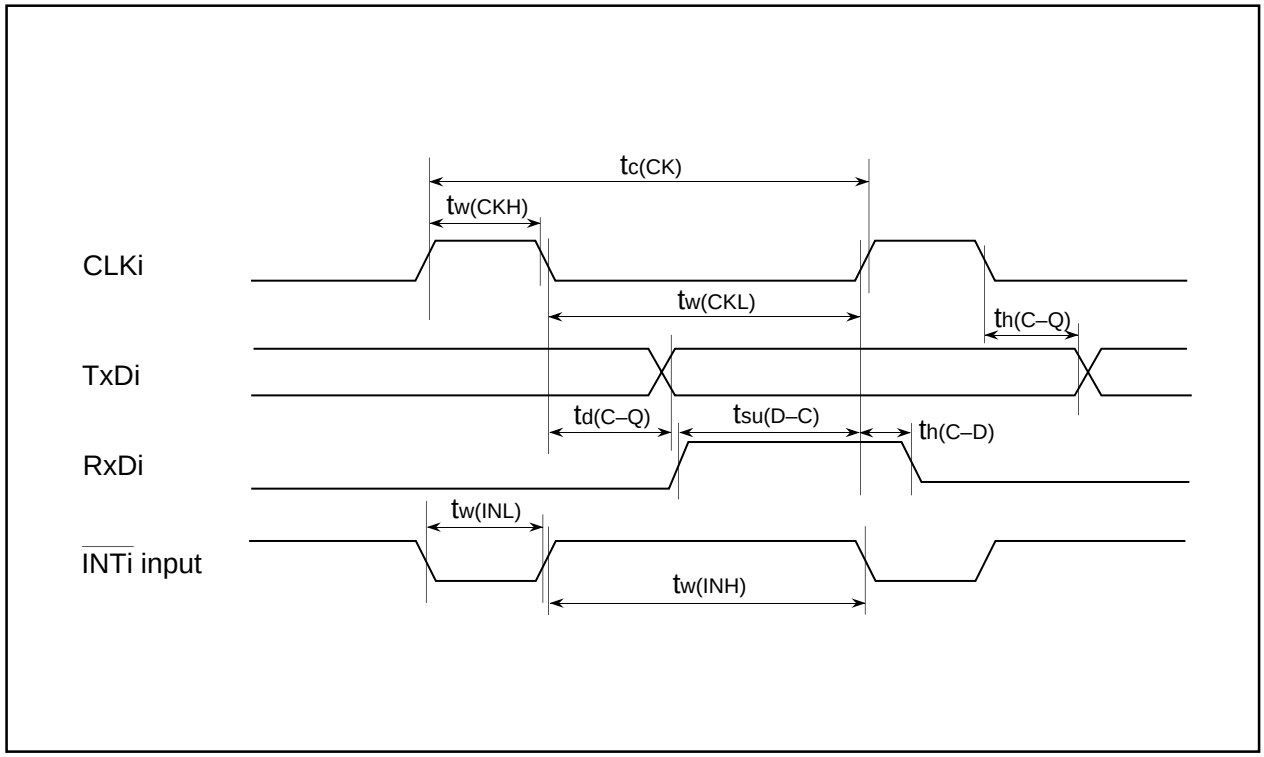


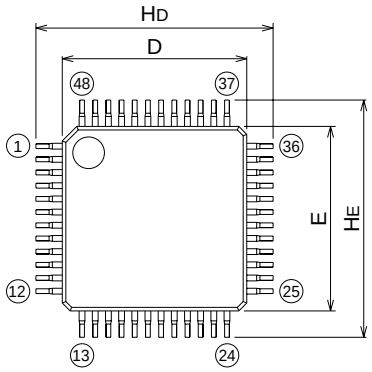
Figure 16.4. Timing Diagram (2)

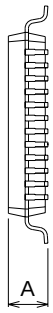
6. Package

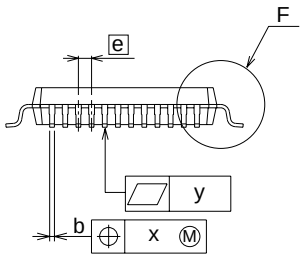
48P6Q-A Recommended

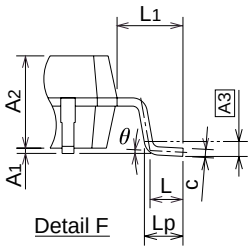
Plastic 48pin 7×7mm body LQFP

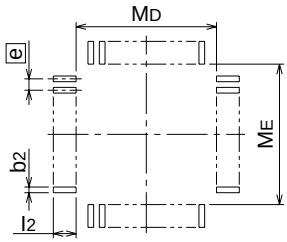
EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
LQFP48-P-77-0.50	–	–	Cu Alloy











Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	1.7
A1	0	0.1	0.2
A2	–	1.4	–
b	0.17	0.22	0.27
c	0.105	0.125	0.175
D	6.9	7.0	7.1
E	6.9	7.0	7.1
e	–	0.5	–
HD	8.8	9.0	9.2
HE	8.8	9.0	9.2
L	0.35	0.5	0.65
L1	–	1.0	–
Lp	0.45	0.6	0.75
A3	–	0.25	–
x	–	–	0.08
y	–	–	0.1
θ	0°	–	8°
b2	–	0.225	–
l2	1.0	–	–
MD	–	7.4	–
ME	–	7.4	–

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