SERVICE MANUAL

DVD 5.1 HOME THEATRE SYSTEM

H-HT5115-N
DA918PA

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1. PRECAUTIONS

1-1 Safety Precautions

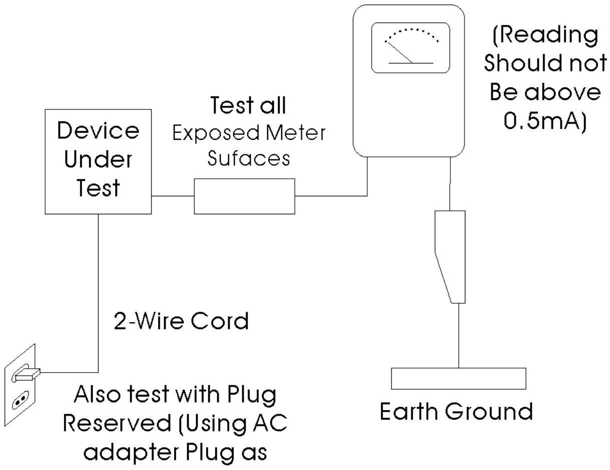
1) Before returning an instrument to the customer, always make a safety check of the entire instrument, including, but not limited to, the following items:

(1) Be sure that no built-in protective devices are defective or have been defeated during servicing.
(1) Protective shields are provided to protect both the technician and the customer. Correctly replace all missing protective shields, including any remove for servicing convenience.
(2) When reinstalling the chassis and/or other assembly in the cabinet, be sure to put back in place all protective devices, including, but not limited to, nonmetallic control knobs, insulating fish papers, adjustment and compartment covers/shields, and isolation resistor/capacitor networks. Do not operate this instrument or permit it to be operated without all protective devices correctly installed and functioning.

(2) Be sure that there are no cabinet opening through which adults or children might be able to insert their fingers and contact a hazardous voltage. Such openings include, but are not limited to, excessively wide cabinet ventilation slots, and an improperly fitted and/or incorrectly secured cabinet back cover.

(3) Leakage Current Hot Check-With the instrument completely reassembled, plug the AC line cord directly into a 120V AC outlet. (Do not use an isolation transformer during this test.) Use a leakage current tester or a metering system that complies with American National Standards institute (ANSI) C101.1 Leakage.

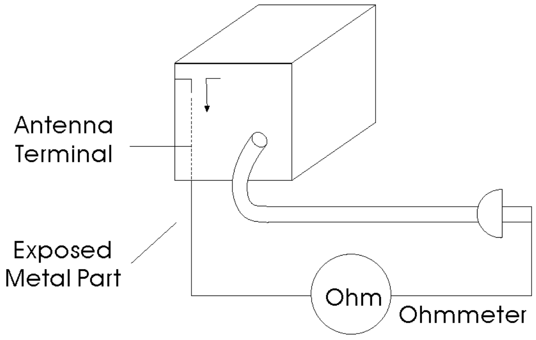
Current for Appliances and underwriters Laboratories (UL) 1270 (40.7). With the instrument's AC switch first in the ON position and then in the OFF position, measure from a known earth ground (metal water pipe, conduit, etc.) to all exposed metal parts of the instrument (antennas, handle brackets, metal cabinets, screwheads, metallic overlays, control shafts, etc.), especially and exposed metal parts that offer an electrical return path to the chassis.
Any current measured must not exceed 0.5mA.
Reverse the instrument power cord plug in the outlet and repeat the test.



AC Leakage Test

Any measurements not within the limits specified herein indicate a potential shock hazard that must be eliminated before returning the instrument to the customer.

(4) Insulation Resistance Test Cold Check-(1) Unplug the power supply cord and connect a jumper wore between the two prongs of the plug. (2) Turn on the power switch of the instrument. (3) Measure the resistance with an ohmmeter between the jumpered AC plug and all exposed metallic cabinet parts on the instrument, such as screwheads, antenna, control shafts, handle brackets, etc. When an exposed metallic part has a return path to the chassis, the reading should be between 1 and 5.2 megohm. When there is no return path to the chassis, the reading must be infinite. If the reading is not within the limits specified, there is the possibility of a shock hazard, and the instrument must be re-pared and rechecked before it is returned to the customer.



Insulation Resistance Test

2) Read and comply with all caution and safety related notes non or inside the cabinet, or on the chassis.

3) Design Alteration Warning-Do not alter of add to the mechanical or electrical design of this instrument. Design alterations and additions, including but not limited to, circuit modifications and the addition of items such as auxiliary audio output connections, might alter the safety characteristics of this instrument and create a hazard to the user. Any design alterations or additions will make you, the service, responsible for personal injury or property damage resulting there from.

4) Observe original lead dress. Take extra care to assure correct lead dress in the following areas: (1) near sharp edges, (2) near thermally hot parts (be sure that leads and components do not touch thermally hot parts), (3) the AC supply, (4) high voltage, and (5) antenna wiring. Always inspect in all areas for pinched, out-of-place, or frayed wiring. Do not change spacing between a component and the printed-circuit board, Check the AC power cord for damage.

5) Components, parts, and/or wiring that appear to have overheated or that are otherwise damaged should be replaced with components, parts and/or wiring that meet original specifications. Additionally determine the cause of overheating and/or damage and, if necessary, take corrective action to remove and potential safety hazard.

6) Product Safety Notice-Some electrical and mechanical parts have special safety-related characteristics which are often not evident from visual inspection, nor can the protection they give necessarily be obtained by replacing them with components rated for higher voltage, wattage, etc. Parts that have special safety characteristics are identified by shading, an (⚡) or a (⚠) on schematics and parts lists. Use of a substitute replacement that does not have the same safety characteristics as the recommended replacement part might created shock, fire and/or other hazards. Product safety is under review continuously and new instructions are issued whenever appropriate.

1-2 Servicing Precautions

CAUTION: Before servicing Instruments covered by this service manual and its supplements, read and follow the Safety Precautions section of this manual.

Note: If unforeseen circument create conflict between the following servicing precautions and any of the safety precautions, always follow the safety precautions. Remember; Safety First

1-2-1 General Serving Precautions

(1) a. Always unplug the instrument's AC power cord from the AC power source before (1) removing or reinstalling any component, circuit board, module or any other instrument assembly. (2) disconnecting any instrument electrical plug or other electrical connection. (3) connecting a test substitute in parallel with an electrolytic capacitor in the instrument.

b. Do not defeat any plug/socket B+ voltage interlocks with which instruments covered by this service manual might be equipped.

c. Do not apply AC power to this instrument and/or any of its electrical assemblies unless all solid-state device heat sinks are correctly installed.

d. Always connect a test instrument's ground lead to the instrument chassis ground before connecting the test instrument positive lead. Always remove the test instrument ground lead last.

Note: Refer to the Safety Precautions section ground lead last.

(2) The service precautions are indicated or printed on the cabinet, chassis or components. When servicing, follow the printed or indicated service precautions and service materials.

(3) The components used in the unit have a specified flame resistance and dielectric strength. When replacing components, use components which have the same ratings, by (⚡) or by (⚠) in the circuit diagram are important for safety or for the characteristics of the unit. Always replace them with the exact replacement components.

(4) An insulation tube or tape is sometimes used and some components are raised above the printed wiring board for safety. The internal wiring is sometimes clamped to prevent contact with heating components. Install such elements as they were.

(5) After servicing, always check that the removed screws, components, and wiring have been installed correctly and that the portion around the serviced part has not been damaged and so on. Further, check the insulation between the blades of the attachment plus and accessible conductive parts.

1-2-2 Insulation Checking Procedure

Disconnect the attachment plug from the AC outlet and turn the power ON. Connect the insulation resistance meter (500V) to the blades of the attachment plug. The insulation resistance between each blade of the attachment plug and accessible conductive parts (see note) should be more than 1 Megohm.

Note: Accessible conductive parts include metal panels, input terminals, earphone jacks, etc.

1-3 ESD Precautions

Electrostatically Sensitive Devices (ESD)

Some semiconductor (solid static electricity) devices can be damaged easily by static electricity.
Such compo9nents commonly are called Electrostatically Sensitive Devices (ESD). Examples of typical ESD devices are integrated circuits and some field-effect transistors and semiconductor chip components. The following techniques of component damage caused by static electricity.

(1) immediately before handling any semiconductor components or semiconductor-equipped assembly, drain off any electrostatic charge on your body by touching a known earth ground. Alternatively, obtain and wear a commercially available discharging wrist strap device, which should be removed for potential shock reasons prior to applying power to the unit under test.

(2) after removing an electrical assembly equipped with ESD devices, place the assembly on a conductive surface such as aluminum foil, to prevent electrostatic charge buildup or exposure of the assembly.

(3) Use only a grounded-tip soldering iron to solder or unsolder ESD device.

(4) Use only an anti-static solder removal devices. Some solder removal devices not classified as “anti-static” can generate electrical charges sufficient to damage ESD devices.

(5) Do not use freon-propelled chemicals. These can generate electrical charges sufficient to damage ESD devices.

(6) Do not remove a replacement ESD device from its protective package until immediately before you are ready to install it. (Most replacement ES devices are packaged with leads electrically shorted together by conductive foam, aluminum foil or comparable conductive materials).

(7) Immediately before removing the protective materials from the leads of a replacement ES device touch the protective material to the chassis or circuit assembly into which the device will be installed.

CAUTION: Be sure no power is applied to the chassis or circuit, and observe all other safety precautions.

(8) Minimize bodily motions when handling unpackaged replacement ESD devices. (Otherwise harmless motion such as the brushing together of your clothes fabric or the lifting of your foot from a carpeted floor can generate static electricity sufficient to damage an ESD device).

MT1389J

Desktop DVD Player SOC
General Datasheet

Version 1.0

Specifications are subject to change without notice

Revision History

Revised date	Contents of revision	Reason for revision	Page	Remarks
2009 6 18	1st Release			Ver 1.0

Contents of Specifications

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1 Applications

This present specifications are applied to IC MT1389J.

2 Type

MT1389J

3 Usage

Single Chip IC for DVD Player

4 Structure

0.13um CMOS process, Silicon material, Monolithic IC, 128pin LQFP, 3.3/1.2 Dual operation voltages.

5 Function

5-1 General Description

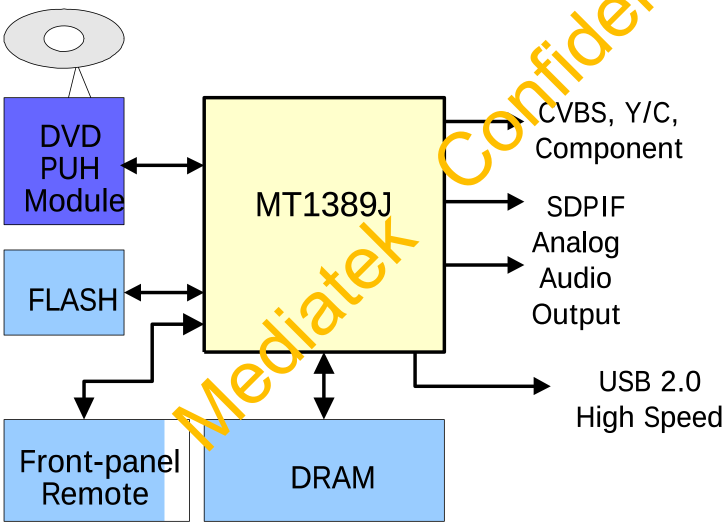
MediaTek MT1389J is a cost-effective DVD system-on-chip (SOC) which incorporates advanced features like MPEG-4 video decoder, high quality TV encoder and state-of-art de-interlace processing. The MT1389J enables consumer electronics manufacturers to build high quality, USB2.0, MS/SD/MMC reader, feature-rich DVD players, portable DVD players or any other home entertainment audio/video devices.

World-Leading Technology: Based on MediaTek's world-leading DVD player SOC architecture, the MT1389J is the New generation of the DVD player SOC. It integrates the MediaTek 3rd generation front-end digital RF amplifier and the Servo/MPEG AV decoder. To save power consumption for Earth, MediaTek use the .13um Process to decrease the power consumption.

Rich Feature for High Valued Product: To enrich the feature of DVD player, the MT1389 equips a simplified MPEG-4 advanced simple profile (ASP) video decoder to fully support the DivX[1] Home Theater profile. It makes the MT1389-based DVD player be capable of playback MPEG-4 content which become more and more popular.

Incredible Audio/Video Quality: The progressive scan of the MT1389J utilized advanced motion-adaptive de-interlace algorithm to achieve the best movie/video playback. The 108MHz/12-bit video DAC provides users a whole new viewing experience. Built-in 6ch audio DACs and 2ch audio ADCs could give the variable function solutions.

High Performance Memory Storage Device: As the core of Portable DVD players need more capability to support current multimedia contents. The MT1389J provides the interface for the 3-in-1 card reader, which supports Memory-Stick, Secure Digital Memory Card, and MultiMediaCard, to connect with the mainstream digital camera FLASH cards. For the USB application, we adopt **USB2.0 High speed** specification to reach rich-contents transference. **USB 2.0 High speed** will support for high-speed devices. **USB 2.0 High Speed** is suitable for high-performance devices such as high-density storage devices. In addition, **USB 2.0 High Speed** supports old USB 1.0/1.1 software and peripherals, offering impressive and even better compatibility to customers



DVD Player System Diagram Using MT1389J

Key Features

- RF/Servo/MPEG Integration
- DivX Home Theater Level MPEG4 ASP Video decoder
- Support DivX Ultra
- High Performance Audio Processor
- Progressive Scan
- 108MHz/12-bit, 4 CH TV Encoder
- Internal 6CH Audio DAC
- Internal 2CH Audio ADC
- USB2.0 High Speed (Host)
- 3-in-1 MS/SD/MMC reader

Applications

Standard DVD Players

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[1] DivX is a trademark of DivXNetworks

[2] **USB High Speed** : 480Mbit/sec. USB Full Speed : 12Mbit/sec.

5-2 Key Features

- RF/Servo/MPEG Integration
- Embedded 6ch Audio DAC
- Embedded 2ch Audio ADC for Karaoke
- High Performance Audio Processor
- High Performance Progressive Video Processor
- Support DivX Ultra
- High Quality 108MHz/12-bit, 4 CH TV Encoder
- USB 2.0 High-Speed

5-3 Applications

- Standard DVD Players
- DVD Players Home Theater Application
- Portable DVD Players
- TV/DVD Combo Systems

5-4 General Feature lists

■ Super Integration DVD player single chip

- High performance analog RF amplifier
- Servo controller and data channel processing
- MPEG-1/MPEG-2/JPEG video
- Dolby AC-3/DTS Decoder
- Unified memory architecture
- Versatile video scaling & quality enhancement
- OSD & Sub-picture
- Built-in clock generator
- Built-in high quality TV encoder
- Built-in progressive video processor
- Audio effect post-processor
- Built-in 5.1-ch Audio DAC
- Built-in 2-ch Audio ADC for Karaoke
- USB 2.0 High-Speed
- MS/SD/MMC 3-in-1 card reader

■ Speed Performance on Servo/Channel Decoding

- DVD-ROM up to 4XS
- CD-ROM up to 24XS

■ Channel Data Processor

- Digital data slicer for small jitter capability
- Built-in high performance data PLL for channel data demodulation
- EFM/EFM+ data demodulation
- Enhanced channel data frame sync protection & DVD-ROM sector sync protection

■ Servo Control and Spindle Motor Control

- Programmable frequency error gain and phase error gain of spindle PLL to control spindle motor on CLV and CAV mode
- Built-in ADCs and DACs for digital servo control
- Provide 2 general PWM
- Tray control can be PWM output or digital output

■ Embedded Micro controller

- Built-in 8032 micro controller
- Built-in internal 373 and 8-bit programmable lower address port
- 1024-bytes on-chip RAM
- Up to 8M bytes FLASH-programming interface
- Supports 5/3.3-Volt. FLASH interface
- Supports power-down mode
- Supports additional serial port

■ DVD-ROM/CD-ROM Decoding Logic

- High-speed ECC logic capable of correcting one error per each P-codeword or Q-codeword
- Automatic sector Mode and Form detection
- Automatic sector Header verification
- Decoder Error Notification Interrupt that signals various decoder errors
- Provide error correction acceleration

■ Buffer Memory Controller

- Supports 16Mb/32Mb/64Mb/128Mb SDRAM
- Supports 16-bit SDRAM data bus
- Provides the self-refresh mode SDRAM
- Block-based sector addressing

■ Video Decode

- Decodes MPEG1 video and MPEG2 main level, main profile video (720/480 and 720x576)
- Decodes MPEG-4 Advanced Simple Profile
- Support DivX 3.11/4.x/5.x Home Theater Profile
- Support DivX Ultra
- Smooth digest view function with I, P and B picture decoding
- Baseline, extended-sequential and progressive JPEG image decoding
- Support CD-G titles

■ Video/OSD/SPU/HLI Processor

- Arbitrary ratio vertical/horizontal scaling of video, from 0.25X to 256X
- 65535/256/16/4/2-color bitmap format OSD,
- 256/16 color RLC format OSD
- Automatic scrolling of OSD image

■ Audio Effect Processing

- Dolby Digital (AC-3) decoding
- DTS decoding
- MPEG-1 layer 1/layer 2 audio decoding
- High Definition Compatible Digital (HDCD)
- Windows Media Audio (WMA)
- Dolby ProLogic II
- Concurrent multi-channel
- IEC 60958/61937 output
  - PCM / bit stream / mute mode
  - Custom IEC latency up to 2 frames
- Pink noise and white noise generator
- Karaoke functions
  - Microphone echo
  - Microphone tone control
  - Vocal mute/vocal assistant

  - Key shift up to +/- 8 keys
  - Chorus/Flanger/Harmony/Reverb
- Channel equalizer
- 3D surround processing include virtual surround and speaker separation

TV Encoder

- Four 108MHz/12bit DACs
- Support NTSC, PAL-BDGHINM, PAL-60
- Support 525p, 625p progressive TV format
- Automatically turn off unconnected channels
- Support Macrovision 7.1 L1, Macrovision 525P and 625P
- CGMS-A/WSS
- Closed Caption

Progressive Scan Video

- Automatic detect film or video source
- Advanced Motion adaptive de-interlace
- Minimum external memory requirement

Serial Flash Interface

- Supports 4Mb/8Mb/16Mb/32Mb/64Mb SPI interface Serial Flash

External Interface

- USB2.0 High Speed (Host)
- Memory-Stick, Secure Digital Memory Card, and MultiMediaCard Interface

Outline

- 128-pin LQFP package
- 3.3/1.2-Volt. Dual operating voltages

General Feature – Third Party Proprietary Right

1. Dolby License

Supply of this Implementation of Dolby technology does not convey a license nor imply a right under any patent, or any other industrial or intellectual property right of Dolby Laboratories, to use this Implementation in any finished end-user or ready-to-use final product. It is hereby notified that a license for such use is required from Dolby Laboratories.

2. Macrovision License

This device is protected by U.S. patent numbers 4,631,603, 4,577,216, 4,819,098 and other intellectual property rights.

3. DTS License

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4. Microsoft License

This product included technology owned by Microsoft Corporation and cannot be used or distributed without a license from Microsoft GP.

5-5 Pin Definitions

Abbreviations:

- SR: Slew Rate
- PU: Pull Up
- PD: Pull Down
- SMT: Schmitt Trigger
- 4mA~16mA: Output buffer driving strength.

Pin	Main	Alt.	Type	Description
Analog Interface (62)				
123	RFIP		Analog Input	AC coupled DVD RF signal input RFIP
124	RFIN	OPOUT	Analog Input	1) AC coupled DVD RF signal input RFIN 2) GPI36
125	RFG	OPINP	Analog Input	Main beam, RF AC input path
126	RFH	OPINN	Analog Input	Main beam, RF AC input path
127	RFA		Analog Input	RF main beam input A
128	RFB		Analog Input	RF main beam input B
1	RFC		Analog Input	RF main beam input C
2	RFD		Analog Input	RF main beam input D
3	RFE		Analog Input	RF sub beam input E
4	RFF		Analog Input	RF sub beam input E
5	AVDD12_2		Analog power	Analog 1.2V power
6	AVDD33_1		Analog Power	Analog 3.3V power
7	XTALI		Input	27MHz crystal input

Pin	Main	Alt.	Type	Description
8	XTALO		Output	27MHz crystal output
9	AGND33		Analog Ground	Analog Ground
10	V20		Analog output	Reference voltage 2.0V
11	V14		Analog output	Reference voltage 1.4V
12	REXT	GPO5	Analog Input	1) Current reference input. It generates reference current for RF path. Connect an external 15K resistor to this pin and AVSS 2) GPO5
13	MDI1		Analog Input	Laser power monitor input
14	LDO1		Analog Output	Laser driver output
15	LDO2		Analog Output	Laser driver output
16	AVDD33_2		Analog Power	Analog 3.3V power
17	DMO		Analog Output	Disk motor control output. PWM output
18	FMO		Analog Output	Feed motor control. PWM output
19	TRAY_OPEN		Analog Output	Tray PWM output/Tray open output
20	TRAY_CLOSE		Analog Output	Tray PWM output/Tray close output
21	TRO		Analog Output	Tracking servo output. PDM output of tracking servo compensator
22	FOO		Analog Output	Focus servo output. PDM output of focus servo compensator
23	FG	GPIO2	Analog	1) Motor Hall sensor input 2) GPIO2
24	USB_DM		Analog Inout	USB port DMINUS analog pin
25	USB_DP		Analog Inout	USB port DPLUS analog pin
26	VDD33_USB		USB Power	USB Power pin 3.3V

Pin	Main	Alt.	Type	Description
27	VSS33_USB		USB Ground	USB ground pin
28	PAD_VRT		Analog Inout	USB generating reference current
29	VDD12_USB		USB Power	USB Power pin 1.2V
96	DACVDDC		Power	3.3V power pin for video DAC circuitry
97	VREF	GPO14	Analog	1) Bandgap reference voltage 2) GPO14
98	FS		Analog	Full scale adjustment (suggest to use 560 ohm)
99	DACVSSC		Ground	Ground pin for video DAC circuitry
100	CVBS		Analog	Analog CVBS or C
101	DACVDDB		Power	3.3V power pin for video DAC circuitry
102	Y/G		Analog	Green, Y, SY, or CVBS
103	B/CB/PB		Analog	Blue, CB/PB, or SC
104	R/CR/PR		Analog	Red, CR/PR, CVBS, or SY
105	AADVSS		Ground	Ground pin for 2ch audio ADC circuitry
106	AKIN2	GPIO19	Analog	1) Audio ADC input 2 2) Audio Mute 3) MCDATA 4) SPDIF 5) GPIO19
107	ADVCM	GPIO20	Analog	1) 2ch audio ADC reference voltageC 2) GPIO20
108	AKIN1	GPIO21	Analog	1) Audio ADC input 1 2) Audio Mute 3) AS_DATA3 4) GPIO21
109	AADVDD		Power	3.3V power pin for 2ch audio ADC circuitry
110	ADACVSS2		Ground	Ground pin for audio DAC circuitry
111	ADACVSS1		Ground	Ground pin for audio DAC circuitry
112	ARF / LFE	GPIO	Analog Output	1) AUDIO DAC LFE channel output 2) ACLK 3) GPIO_LFE
113	ARS	GPIO	Analog Output	1) AUDIO DAC RS channel output 2) ABCK 3) GPIO_ARS
114	AR	GPIO0	Analog Output	1) AUDIO DAC right channel output 2) RXD2 3) ASDATA2 4) GPIO_AR
115	AVCM		Analog	Audio DAC reference voltage

Pin	Main	Alt.	Type	Description
116	AL	GPIO1	Analog Output	1) AUDIO DAC left channel output 2) TXD2 3) ASDATA1 4) GPIO_AL
117	ALS	GPIO	Analog Output	1) AUDIO DAC LS channel output 2) ALRCK 3) GPIO_ALS
118	ALF /CENTER	GPIO	Analog Output	1) AUDIO DAC CENTER channel output 2) Audio Mute 3) ASDATA0 4) GPIO_CENTER
119	ADACVDD1		Analog Power	3.3V power pin for audio DAC circuitry
120	ADACVDD2		Analog Power	3.3V power pin for audio DAC circuitry
121	AVDD12_1		Analog Power	Analog 1.2V power
122	AGND12		Analog Ground	Analog Ground
General Power/Ground (7)				
56, 87	DVDD12		Power	1.2V power pin for internal digital circuitry
81	DVSS12		Ground	1.2V Ground pin for internal digital circuitry
51, 71,84	DVDD33		Power	3.3V power pin for internal digital circuitry
50	DVSS33		Ground	3.3V Ground pin for internal digital circuitry
Micro Controller , Flash Interface and GPIO(11)				
30	SF_CS_		InOut 8mA, SR PU, SMT	Serial Flash Chip Select
31	SF_DO		InOut 8mA, SR PD, SMT	Serial Flash Dout
32	SF_DI		InOut 8mA, SR PU, SMT	Serial Flash Din

Pin	Main	Alt.	Type	Description
33	SF_CK		InOut 8mA, SR PD, SMT	Serial Flash Clock
34	UP1_6	SCL	InOut 4mA, SR PU, SMT	1) Microcontroller port 1-6 2) SD_D1 set D 3) MS_D1 set D 4) RXD3 5) I^{2}C SCK
35	UP1_7	SDA	InOut 4mA, SR PU, SMT	1) Microcontroller port 1-7 2) SD_D2 set D 3) MS_D2 set D 4) TXD3 5) I^{2}C SDA
37	GPIO6		InOut 4mA, PU	1) Microcontroller port 3-5 (Internal Pull-Up) 2) SD_D0 set B/D/E/F 3) SD_D2 set C 4) MS_D0 set B/D/E 5) MS_D2 set C 6) TXD1 7) ASDATA2 8) GPIO6
38	PRST#		Input PU, SMT	Power on reset input, active low
39	IR		Input SR, SMT	IR control signal input
40	GPIO3	INT#	InOut 8mA, SR SMT	1) INT_ 2) Microcontroller port 3-1 (Internal Pull-Up) 3) SD_CLK set D/F 4) MS_CLK set B/D/E 5) TXD4 6) GPIO3
41	GPIO4		InOut 4mA, PD	1) Microcontroller port 3-4 (Internal Pull-Up) 2) MS_BS set B 3) YCLK 4) ASDATA0 5) ALRCK 6) GPIO4
Dram Interface (37) (Sorted by position)				
52	RD0		InOut, 2mA	DRAM data 0
53	RD1		InOut 2mA	DRAM data 1
54	RD2		InOut 2mA	DRAM data 2

Pin	Main	Alt.	Type	Description
55	RD3		InOut 2mA	DRAM data 3
57	RD4		InOut 2mA	DRAM data 4
58	RD5		InOut 2mA	DRAM data 5
59	RD6		InOut 2mA	DRAM data 6
60	RD7		InOut 2mA	DRAM data 7
61	DQM0		InOut 2mA, PD	Data mask 0
62	RD15		InOut 2mA	DRAM data 15
63	RD14		InOut 2mA	DRAM data 14
64	RD13		InOut 2mA	DRAM data 13
65	RD12		InOut 2mA	DRAM data 12
66	RD11		InOut 2mA	DRAM data 11
67	RD10		InOut 2mA	DRAM data 10
68	RD9		InOut 2mA	DRAM data 9
69	RD8		InOut 2mA	DRAM data 8
70	DQM1		InOut 2mA, PD	Data mask 1
72	RCLK		InOut 4mA, PD	Dram clock
73	RA11		InOut 2mA, PD	DRAM address bit 11

Pin	Main	Alt.	Type	Description
74	RA9		InOut 2mA, PD	DRAM address 9
75	RA8		InOut 2mA, PD	DRAM address 8
76	RA7		InOut 2mA, PD	DRAM address 7
77	RA6		InOut 2mA, PD	DRAM address 6
78	RA5		InOut 2mA, PD	DRAM address 5
79	RA4		InOut 2mA, PD	DRAM address 4
80	RWE#		Output 2mA, PD	DRAM Write enable, active low
82	CAS#		Output 2mA, PD	DRAM column address strobe, active low
83	RAS#		Output 2mA, PD	DRAM row address strobe, active low
85	BA0		InOut 2mA, PD	DRAM bank address 0
86	BA1		InOut 2mA, PD	DRAM bank address 1
88	RA10		InOut 2mA, PD	DRAM address 10
89	RA0		InOut 2mA, PD	DRAM address 0
90	RA1		InOut 2mA, PD	DRAM address 1
91	RA2		InOut 2mA, PD	DRAM address 2
92	RA3		InOut 2mA, PD	DRAM address 3

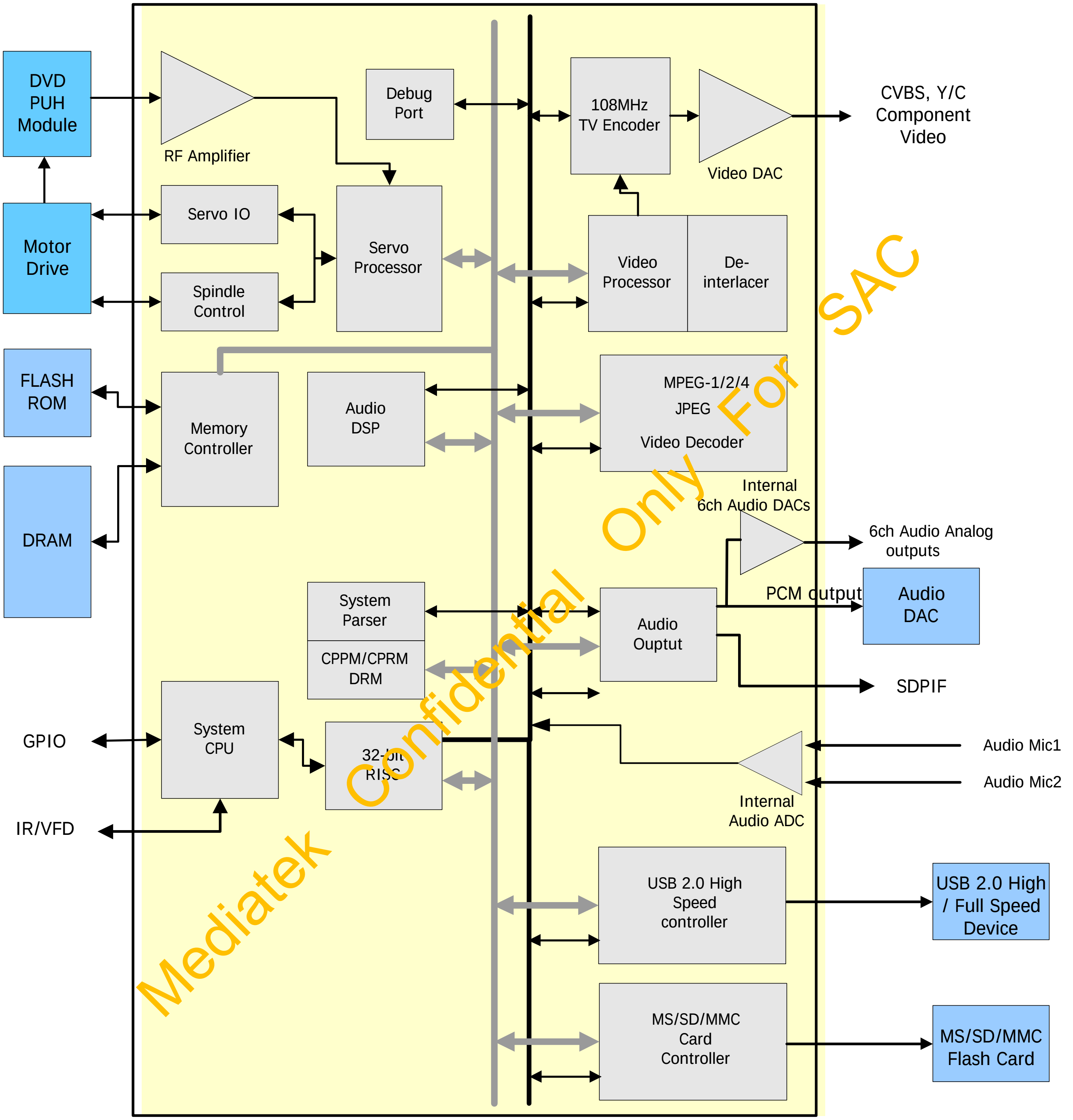
Pin	Main	Alt.	Type	Description
45	GPIO7	CKE	InOut 4mA, PD	1) Dram Clock Enable 2) SD_CLK set A/C 3) MS_CLK set A/C 4) Y4/Y3 5) ACLK 6) ASDATA1 7) MCDATA 8) Microcontroller port 1-4 (Internal Pull-Up) 9) GPIO 7
GPIO (11)				
44	GPIO8		InOut 4mA, PD	1) SD_CLK set E 2) SD_CMD set A/C 3) MS_BS set A/C 4) Y5/Y2 5) ASDATA2 6) ACLK 7) MCDATA 8) Microcontroller port 1-5 (Internal Pull-Up) 9) GPIO8
43	GPIO9		InOut 4mA, PD	1) SD_CMD set E 2) SD_D0 set A/C 3) MS_D0 set A/C 4) Y6/Y1 5) ASDATA3 6) ABCK 7) GPIO9
94	GPIO10		InOut 4mA, PD	1) SD_D3 set D 2) MS_D3 set D 3) GPIO10
36	GPIO11		InOut 4mA, PU	1) SD_D1 set C 2) SD_CMD set B/D/F 3) MS_BS set D/E 4) ABCK 5) ASDATA0 6) Audio Mute 7) RXD1/ RXD4 8) Microcontroller port 3-0 (Internal Pull-Up) 9) GPIO11
93	SPDIF	GPIO12	InOut 2mA, PD	1) SPDIF output 2) GPIO12
42	GPIO13		InOut 4mA, PD	1) SD_CLK set B 2) SD_D3 set C 3) MS_D3 set C 4) Y7/Y0 5) ALRCK 6) Audio Mute 7) GPIO13

Pin	Main	Alt.	Type	Description
46	GPIO29		InOut 4mA, PD	1) SD_D0 set G 2) MS_D0 set F 3) Y3/Y4 4) GPIO29
47	GPIO30		InOut 4mA, PU	1) SD_CMD set G 2) MS_BS set F 3) Y2/Y5 4) AS_DATA3 5) GPIO30
48	GPIO31		InOut 4mA, PU	1) SD_CLK set G 2) MS_CLK set F 3) Y1/Y6 4) AS_DATA3 5) GPIO31
49	GPIO32		InOut 4mA, PD	1) Y0/Y7 2) GPIO32
95	GPIO33		InOut 4mA, PD	1) GPIO33

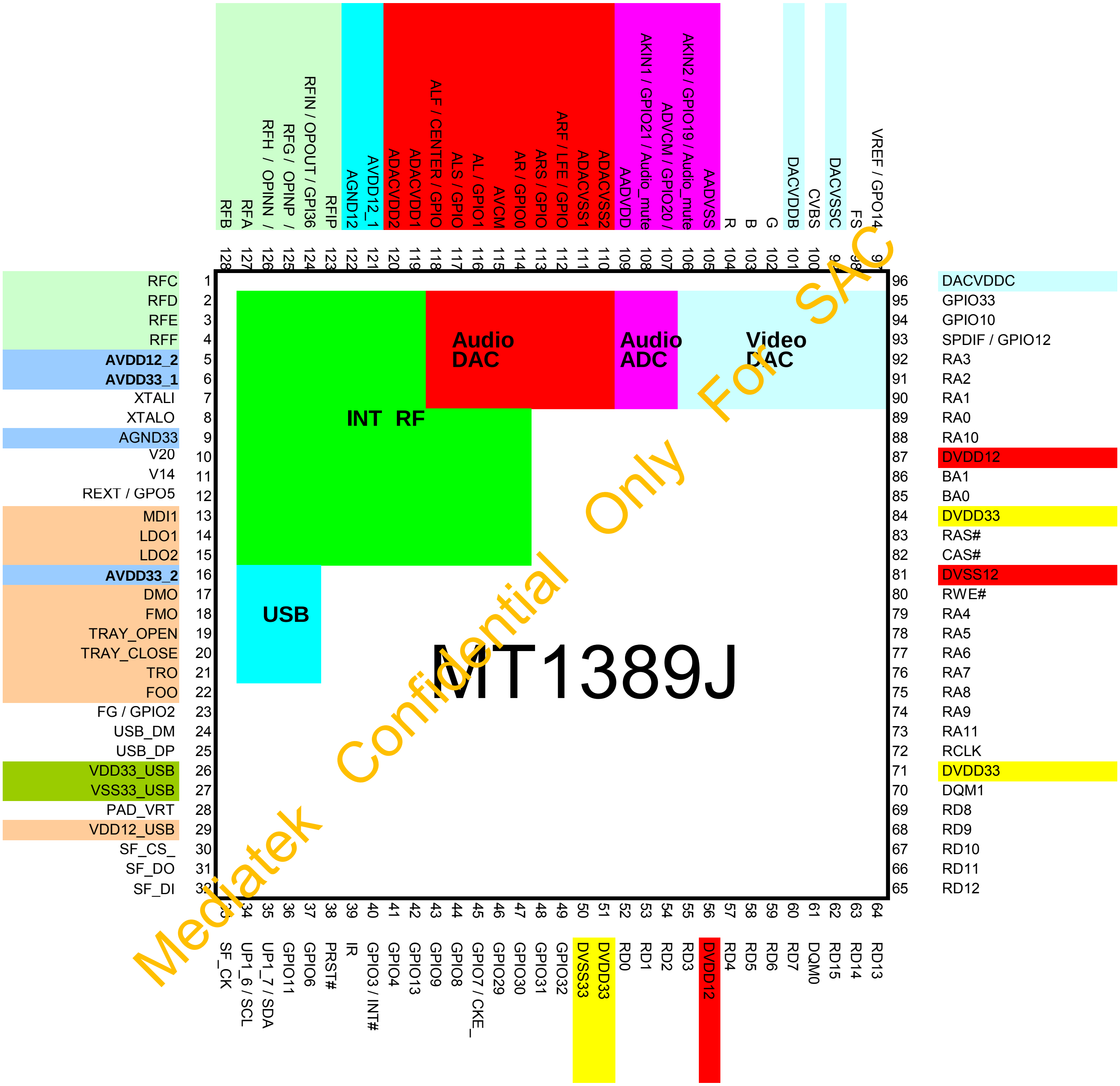
Note:

1. The Main column is the main function, Alt. means alternative function.
2. The multi-function GPIO pins are set to green characters.

5-6 Functional Block



6 Pin Assignment



7 Absolute Maximum Ratings

Symbol	Parameters	Value	Unit
VDD3	3.3V Supply voltage	-0.3 to 3.6	V
VDD2	1.2V Supply voltage	-0.3 to 2.1	V
VDDA	Analog Supply voltage	-0.3 to 3.6	V
V_{IN}(3.3V)	Input Voltage (3.3V IO)	-0.3 to 3.63	V
V_{IN}(5V-tolerance)	Input Voltage (5V-tolerance IO)	-0.3 to 5.5	V
V_{OUT}	Output Voltage	-0.3 to VDD3+0.3	V
T_{STG}	Storage Temperature	-45 to 150	°C

8 Recommend Operation Condition

Symbol	Parameters	Min	Typ	Max	Unit
T_{OP}	Operating Temperature	0		70	°C
T_J	Junction Operation Temp.	0	25	115	°C
VDD3	3.3V Supply voltage	3.1	3.3	3.6	V
VDD2	1.2V Supply voltage	1.15	1.25	1.35	V
VDDA	Analog Supply voltage	3.1	3.3	3.6	V
V_{IH} (3.3V)	Input voltage high (3.3V IO)	2.0	-	-	V
V_{IL} (3.3V)	Input voltage low (3.3V IO)	-	-	0.8	V
I_{IH}	High level input current			10	UA
I_{IL}	Low level input current	-10			UA
P_D	Power dissipation		1.5		W
P_{DOWN}	Power down mode			0.1	W
fclk	Input frequency of clock		27		MHz

9 Electrical Characteristics

9-1 DC Characteristics

Symbol	Parameters	Min	Typ	Max	Unit
V_{OH} (3.3V)	Output voltage high (3.3V IO) (*I_{OH} = 2 ~ 16mA)	2.4	-	-	V
V_{OL} (3.3V)	Output voltage low (3.3V IO) (*I_{OL} = 2 ~ 16mA)	-	-	0.4	V
Rpu	Pull-up Resistance	40	75	190	KΩ
Rpd	Pull-down Resistance	40	75	190	KΩ
FOO_{OFF}	Offset voltage between FOO zero output and V_{REF}	-50	0	50	mV
TRO_{OFF}	Offset voltage between TRO zero output and V_{REF}	-40	0	40	mV
DMO_{OFF}	Offset voltage between DMO zero output and V_{REF}	-30	0	30	mV

Note * : The driving current of some IO pad are programmable according to the different application and environment . All setting will be defined according to the F/W progress and test result.

9-2 Built-in Audio-DAC Characteristics

Note *: All parameters is measured on MediaTek's DVD player reference DVD board, the actual performance depends on different PCB design.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{out}	Output swing level: Digital i/p level =0 dBFS , ADACVDD =3.3V (V_{out} = 1.0 * ADACVDD / 3.3)	0.9	1.0	1.1	V_P
Ro	Output impedance @ 1kHz		50	100	
R_{L_min}	Minimum resister load	5			K
C_{L_max}	Maximum capacitor load			20	PF
S/(THD+N)	S/(THD+N) @ 0 dBFS; f_{in} = 1kHz; Fs = 48kHz, A-weighted		83		dBr(A)
DR	Dynamic Range		83		dBr(A)
SNR	Signal to noise ratio; A-weighted		90		dBr(A)
Channel Separation	Close-talk of Left and Right Channel		85		dB

9-3 Built-in Audio-ADC Characteristics

Test Condition:

DSP MIC1 Gain = 0 (0)	MIC threshold=0
DSP MIC2 Gain = 0dB.(2000)	Apwin output Z= 600

Echo level = 0 dB

Measure SPDIF output.

CIC filter right shift 3 bit

Test signal : 1K Hz sin wave	Vpp(V)
Max Input (with output THD+N <60 dbfs)	2.9
DC bias level	1.3
Test signal : 1K Hz sin wave	
Input (Vpp)	Output THD+N(dBFs)
3V	-45
2.828V	-65
2.75V	-65.6
2.5V	-66
2V	-66.5
1.5V	-66.7
1V	-66.6
0.5V	-67.8

Test signal : 2.828 Vpp	
Input frequency:	Amp(dBFS)
1 KHz	-0.544
4KHz	-0.574
8khz	-0.66
16KHz	-0.981
20KHz	-1.24
22KHz	-2.44

9-4 Built-in Video-DAC Specifications

Input Codes for Video Application:

	NTSC	NTSC w/setup	525_I	525_I w/setup	525_P
WHITE (235)	Programable, Current setting: 3297	Programable, Current setting: 3297	Programable, Current setting: 3297	Programable, Current setting: 3297	Programable, Current setting: 3290
BLACK (16)	960	1120	960	1120	1008
PEDESTAL	960	960	960	960	1008
SYNC TIP	64	64	64	64	64

	525_P w/s	PAL	625_I	625_P	RGB
WHITE (235)	---	Programable, Current setting: 3290	Programable, Current setting: 3290	Programable, Current setting: 3290	Programable, Current setting: 2282
BLACK (16)	---	1008	1008	1008	0
PEDESTAL	---	1008	1008	1008	-
SYNC TIP	---	64	64	64	-

9-5 Video Output Voltage Level:

High Impedance Mode:

I_{OUT} (max) = 19.4152 / R_{REF}, R_{REF} = 2.2 KOhm

V_{OUT} (max) = R_{LOAD} * I_{OUT} (max) = 1.3237 V, R_{LOAD} = 150 Ohm

V_{OUT} = D_{IN} / 4095 * V_{OUT} (max) = D_{IN} * R_{LOAD} * 0.0047412 / R_{REF}

Low Impedance Mode:

I_{OUT} (max) = 19.4152 / R_{REF}, R_{REF} = 560 Ohm

V_{OUT} (max) = R_{LOAD} * I_{OUT} (max) = 1.3 V, R_{LOAD} = 37.5 Ohm (75 Ohm || 75 Ohm)

V_{OUT} = D_{IN} / 4095 * V_{OUT} (max) = D_{IN} * R_{LOAD} * 0.0047412 / R_{REF}

9-6 Video DAC DC Electrical Characteristics
(Operating Free-Air Temperature, AVDD 3.3V, DVDD = 3.3V).

Analog Output	MIN	TYP	MAX	UNIT
Full Scale Output Current CVBS/Y/C/R/G/B (low impedance mode)	33.6	34.6	34.9	mA
Full Scale Output Current CVBS/Y/C/R/G/B (high impedance mode)	8.40	8.65	8.73	mA
LSB current CVBS/Y/C/R/G/B (low impedance mode)	32.8	33.8	34.1	uA
LSB current CVBS/Y/C/R/G/B (high impedance mode)	8.20	8.45	8.52	uA
DAC-to-DAC Mis-Matching	--	1.28	--	%

Output Compliance	0	--	1.35	V
DAC Output Delay	--	1.5	10	ns
DAC Rise/Fall Time	--	2.1	5	
Voltage Reference				
Reference Voltage Output		1.27		V
Reference Input Current		2.267		MA
Static Performance				
DAC Resolution		12		Bits
DNL Differential Non-Linearity	+/-0.2	*/-0.25	+/-0.3	LSB
INL Integral Non-Linearity	+/-0.35	*/-0.4	+/-0.49	LSB
Dynamic Performance				
Differential Gain		0.8	1.5	%
Differential Phase		0.6	1.5	□
S/N Ratio	70			dB
Power Supply				
Supply Voltage	3.0	3.3	3.6	V

9-7 RF specification

Item	Designator	Conditions	Min	Typ	Max	Unit
3.3V POWER			3.00	3.30	3.60	Volts
Power Down Mode		Enable power down	10	27	50	mA
		Chip Reset	90	151	200	mA
Reference Voltage	V20	Force current =0A	1.85	1.99	2.15	Volts
Reference Voltage	V14	Force current =0A	1.25	1.39	1.55	Volts
APC1(CD)	MDI1	0Ah=10 ;APC1 on MDI1=180mV	166	184	202	mV
	LDO1	0Ah=00 ;APC1 off	3.00	3.28		V
	MDI1→LDO1	0Ah=10; APC1 on	212	254	295	V/V
APC2(DVD)	MDI2	0Bh=10 ;APC2 on MDI2=180mV	166	184	202	mV
	LDO2	0Bh=00 ;APC2 off	3.00	3.28		V
	MDI2→LDO2	0Bh=10; APC2 on High gain	210	265	298	V/V

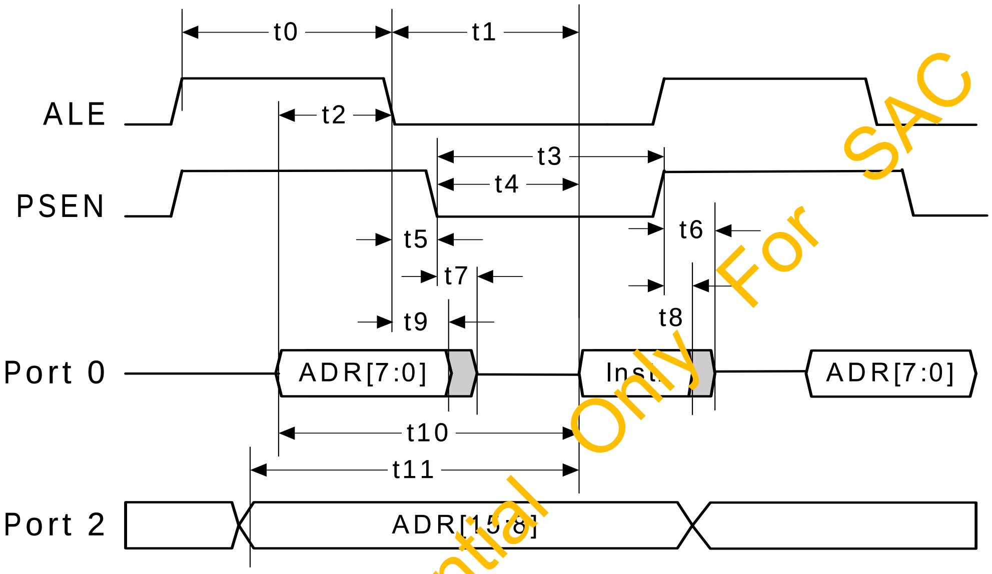
Item	Designator	Conditions	Min	Typ	Max	Unit
Focusing Error Gain	MA → FEO	05h=30; low gain With 10KHz Sin Input	7.5	10.3	11.5	dB
Focusing Error Frequency Response	MA → FEO	05h=7C; low gain With 10KHz, 300KHz Sin Input R=G(10kHz)-G(300Khz)	16	23.9		dB
Focusing Error Common Mode Gain	MA → FEO MB → FEO	05h=3F; low gain With 10KHz Sin Input		-34	-20	dB
Focusing Error H/L Gain	MA → FEO	Toggle 05h bit5 : FELG With 10KHz Sin Input	2.75	2.99	3.25	V/V
Focusing Error offset Adjustment step	Input Floating Measure FEO	Toggle 4Dh : FEOS[6:0]	65	103	140	mV
Focusing Error THD	MA → FEO	05h=7C; low gain With 10KHz Sin Input	30	54		dB
Central Servo Gain	MA → CSO	06h=F0; low gain With 10KHz Sin Input	12.5	14.1	15.5	dB
Central Servo Frequency Response	MA → CSO	06h=FF; low gain With 10KHz, 300KHz Sin Input R=G(10kHz)-G(300Khz)	14	21.4		dB
Central Servo Common Mode Gain	MA → CSO MB → CSO	06h=F0; low gain With 10KHz Sin Input		-30	-10	dB
Central Servo H/L Gain	MA → CSO	Toggle 06h bit5 : CSOLG With 10KHz Sin Input	2.75	2.97	3.25	V/V
Central Servo offset Adjustment step	Input Floating Measure CSO	Toggle 4Eh : CSOOS[6:0]	65	108	140	mV
Central Servo THD	MA → CSO	06h=F0; low gain With 10KHz Sin Input	30	53		dB
Tracking Error Gain	MA → TEO	07h=70; low gain With 10KHz Sin Input	13	15	17	dB
Tracking Error Frequency Response	MA → TEO	07h=70; low gain With 10KHz, 300KHz Sin Input R=G(10kHz)-G(300Khz)	16	24.2		dB

Item	Designator	Conditions	Min	Typ	Max	Unit
Tracking Error Common Mode Gain	MA → TEO MB → TEO	07h=7F; low gain With 10KHz Sin Input		-22	-10	dB
Tracking Error H/L Gain	MA → TEO	Toggle 07h bit6, 5 With 10KHz Sin Input	4	5.8	8	V/V
Tracking Error offset Adjustment step	Input Floating Measure TEO	Toggle 4Fh : TEOS[6:0]	65	110	140	mV
Tracking Error THD	MA → TEO	07h=7F; low gain With 10KHz Sin Input	30	42		dB
RFL Gain	MA → LVL	08h=60; low gain With 10KHz Sin Input	-6.5	-4.6	-3.5	dB
RFL Frequency Response	MA → LVL	08h=7F; low gain With 10KHz, 300KHz Sin Input R=G(10kHz)-G(300Khz)	14	22.7		dB
RFL H/L Gain I	MA → LVL	Toggle 09h bit1 : LVLATN With 10KHz Sin Input	0.3	0.52	0.7	V/V
RFL H/L Gain II	SA → LVL	Toggle 09h bit2 : SBADHG With 10KHz Sin Input	2.5	2.77	3.1	V/V
RFL offset Adjustment step	Input Floating Measure LVL	Toggle 50h : LVLOS[6:0]	65	113	140	mV
RFL THD	MA → LVL	08h=7F; low gain With 10KHz Sin Input	30	44		dB

9-8 Micro Controller Interface

Parameter	Symbol	Min.	Max.	Units
Oscillator Frequency	1/Tf	0	23.3	MHz
ALE Pulse Width	T0	1.5Tf-5		ns
ALE Low to Valid Instruction	T1		2.5Tf-20	ns
ALE Low to PSEN Low	T5	0.5Tf-5		ns
Address Valid to ALE Low	T2	0.5Tf-5		ns
Address Hold After ALE Low	T9	0.5Tf-5		ns
PSEN Pulse Width	T3	2.0Tf-5		ns
PSEN Low to Valid Instruction	T4		2.0Tf-20	ns

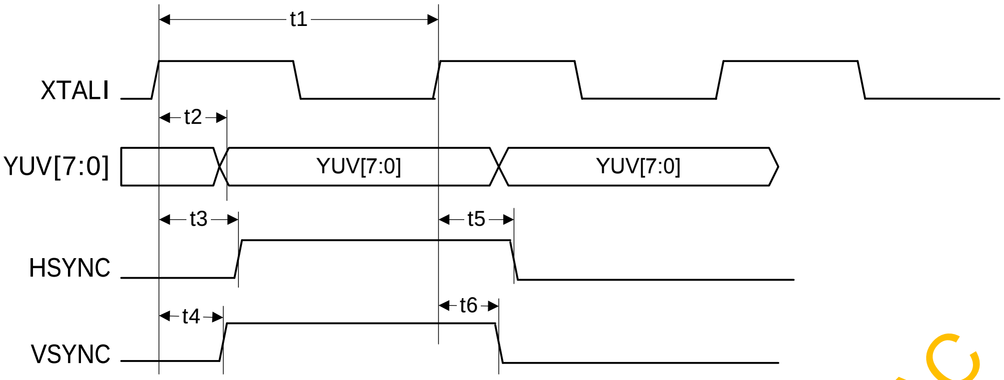
Input Instruction Hold After PSEN high	T8	0		ns
Input Instruction Float After PSEN high	T6		1.0Tf-5	ns
Port 0 Address to Valid Instruction	T10		3.0Tf-20	ns
Port 2 Address to Valid Instruction	T11		3.5Tf-20	ns
PSEN Low to Address Float	T7		0	ns



Program Memory Read Cycle Timing Diagram

9-9 Digital Video Output Interface

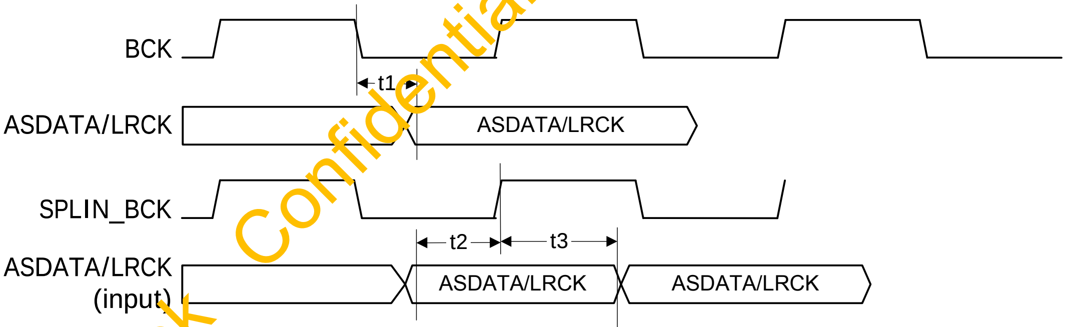
Parameter	Symbol	Min	Typ	Max	Units
Oscillator Frequency	1/T1		27		MHz
YUV digital output delay	T2			15	ns
HSYNC Rising delay	T3			15	ns
VSYNC Rising delay	T4			15	ns
HSYNC Falling delay	T5			20	ns
VSYNC Falling delay	T6			20	ns



Digital Video Output Interface Timing Diagram

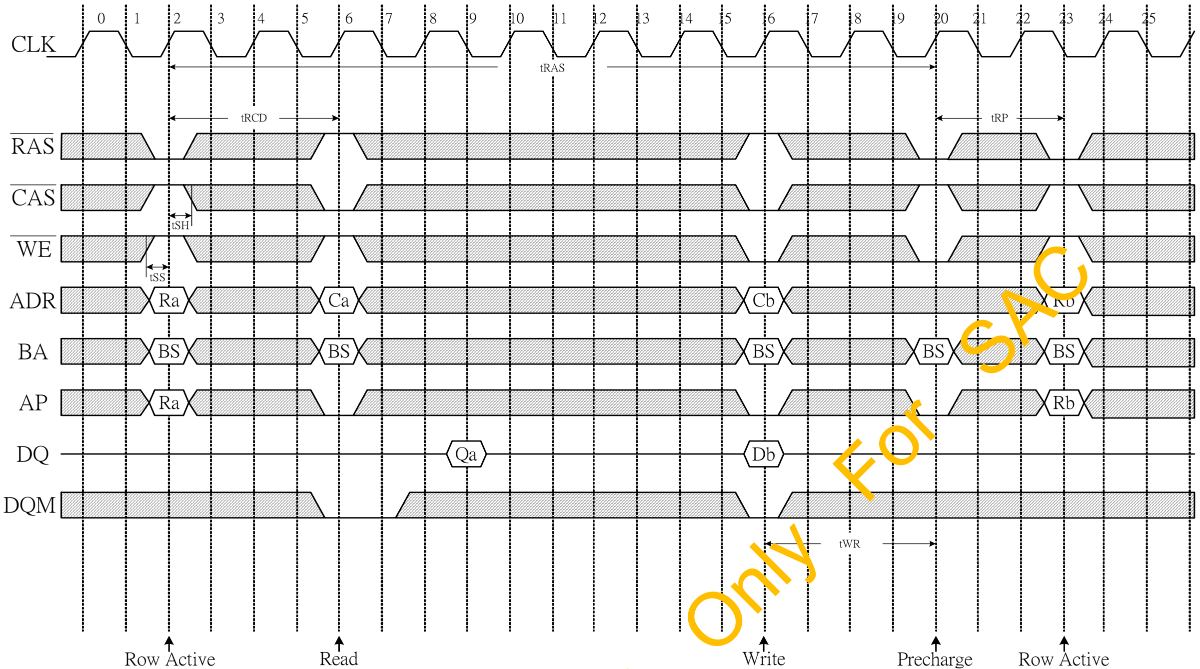
9-10 SPDIF I/O Interface

Parameter	Symbol	Min	Typ	Max	Units
BCK negative edge to ASDATA valid	T1	1.0		3.0	ns
ASDATA/LRCK input setup	T2			3.0	ns
ASDATA/LRCK input hold	T3	1.2			ns



SPDIF Input/Output Timing Diagram

9-11 DRAM Interface



Parameter		Symbol	-6		-7		-75		Units
			Min	Max	Min	Max	Min	Max	
CLK cycle time	CAS latency = 3	tCC	7.5	-	7.5	-	7.5	-	ns
SDRAM input setup time		tSS	1.5		1.75		1.75		ns
SDRAM input hold time		tSH	1		1		1		ns
Active to Precharge command period		tRAS	42	100K	49	100K	52	100K	ns
Precharge to Active command period		tRP	18		20		20		ns
Active to read/write command delay		tRCD	18		20		20		ns
Write recovery time	CL = 3	tWR	6		7		7.5		ns

FREQUENCY vs. AC PARAMETER RELATIONSHIP TABLE

-6T

(Unit: number of clock)

Frequency	CAS Latency	tRAS	tRP	tRCD	tWR
		42ns	18ns	18ns	6ns/10ns
133MHz (7.5ns)	3	6	3	3	1
125MHz (8ns)	2	6	3	3	1
100MHz (10ns)	2	5	2	2	1

-7T

(Unit: number of clock)

Frequency	CAS Latency	tRAS	tRP	tRCD	tWR
		49ns	20ns	20ns	7ns/10ns
133MHz (7.5ns)	3	7	3	3	1
125MHz (8ns)	3	6	3	3	1
100MHz (10ns)	2	5	2	2	1

-7.5T

(Unit: number of clock)

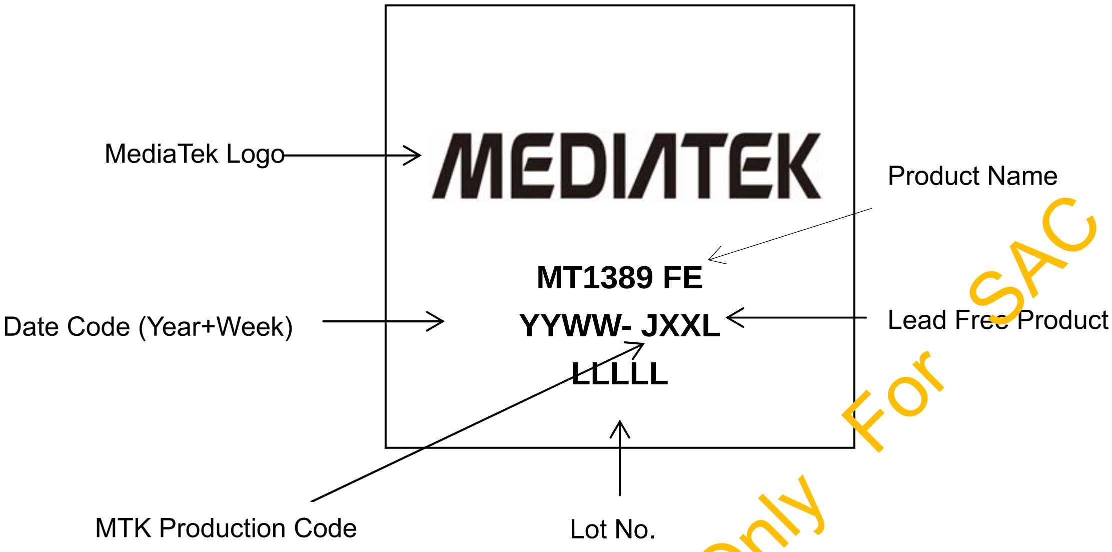
Frequency	CAS Latency	tRAS	tRP	tRCD	tWR
		45ns	20ns	20ns	7.5ns/10ns
133MHz (7.5ns)	3	6	3	3	1
125MHz (8ns)	3	6	3	3	1
100MHz (10ns)	2	5	2	2	1

-8T

(Unit: number of clock)

Frequency	CAS Latency	tRAS	tRP	tRCD	tWR
		48ns	20ns	20ns	8ns/10ns
125MHz (8ns)	3	6	3	3	1
100MHz (10ns)	3	5	2	2	1

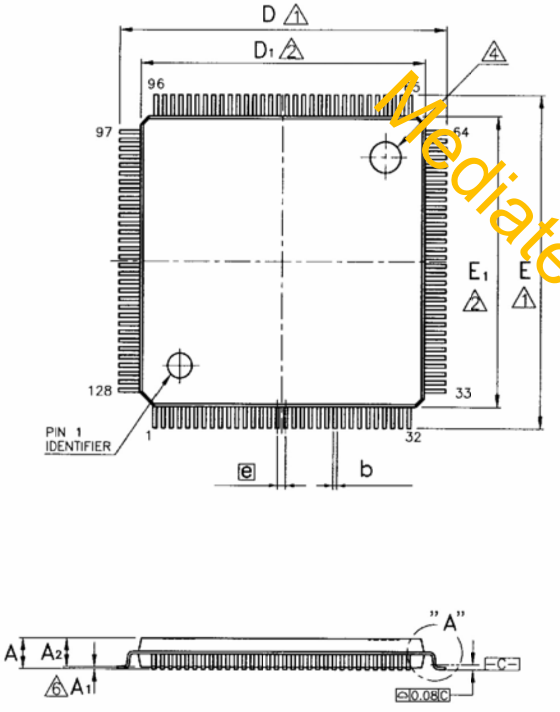
10 Marking on Devices

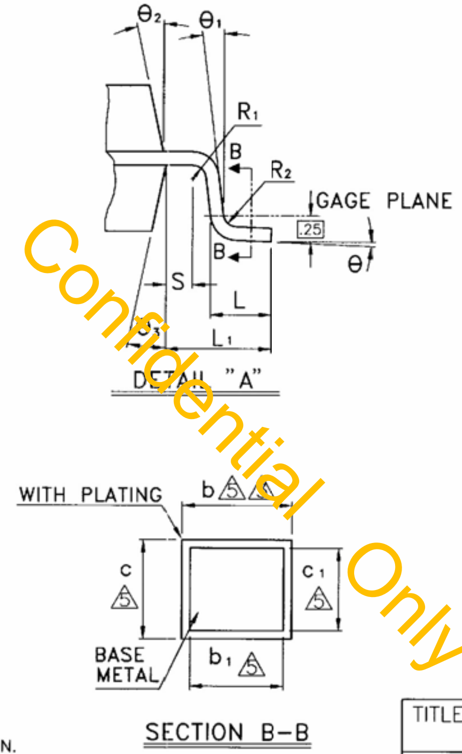


11 Package Description

11-1 Package Outline Dimension

The bend lead are controlled under the criteria 0.075mm (2.5mil).





Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.60	—	—	0.063
A_1	0.05	—	—	0.002	—	—
A_2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.13	0.18	0.23	0.005	0.007	0.009
b_1	0.13	0.16	0.19	0.005	0.006	0.007
c	0.09	—	0.20	0.004	—	0.008
c_1	0.09	—	0.16	0.004	—	0.006
D	15.85	16.00	16.15	0.624	0.630	0.636
D_1	13.90	14.00	14.10	0.547	0.551	0.555
E	15.85	16.00	16.15	0.624	0.630	0.636
E_1	13.90	14.00	14.10	0.547	0.551	0.555
e	0.40 BSC			0.016 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 REF			0.039 REF		
R_1	0.08	—	—	0.003	—	—
R_2	0.08	—	0.20	0.003	—	0.008
S	0.20	—	—	0.008	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
$θ_1$	0°	—	—	0°	—	—
$θ_2$	12°TYP			12°TYP		
$θ_3$	12°TYP			12°TYP		

NOTE :

1. TO BE DETERMINED AT SEATING PLANE -C- .
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.
4. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
5. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.25 mm FROM THE LEAD TIP.
6. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
7. CONTROLLING DIMENSION : MILLIMETER.
8. REFERENCE DOCUMENT : JEDEC MS-026.

APPROVED
BY:
DATE

TITLE: 128LD LQFP(14x14x1.4mm) PACKAGE OUTLINE -Cu L/F,FOOTPRINT 2.0mm			
L/F MATERIAL: C7025 1/2H			
APPR.		DWG NO.	D128-SW1
R&D		REV NO.	A
Q.M		SCALE	
CHK.		DATE	JAN 20,'97
DEN.	J.F.C	SHT NO.	1/1
SILICONWARE PRECISION INDUSTRIES CO., LTD.			

REV NO	DESCRIPTION	DATE

COPY
CONTROLLED

11-2 Weight of the chip

0.65g

11-3 Material and Finish of Lead Terminals

For Lead-free Package, Materials of terminal is Sn(98%) and Bi (2%) and thickness is 300~600u inch, similar as SnPb.

11-4 Package Material

Lead frame: Cu

Epoxy: 1033BF

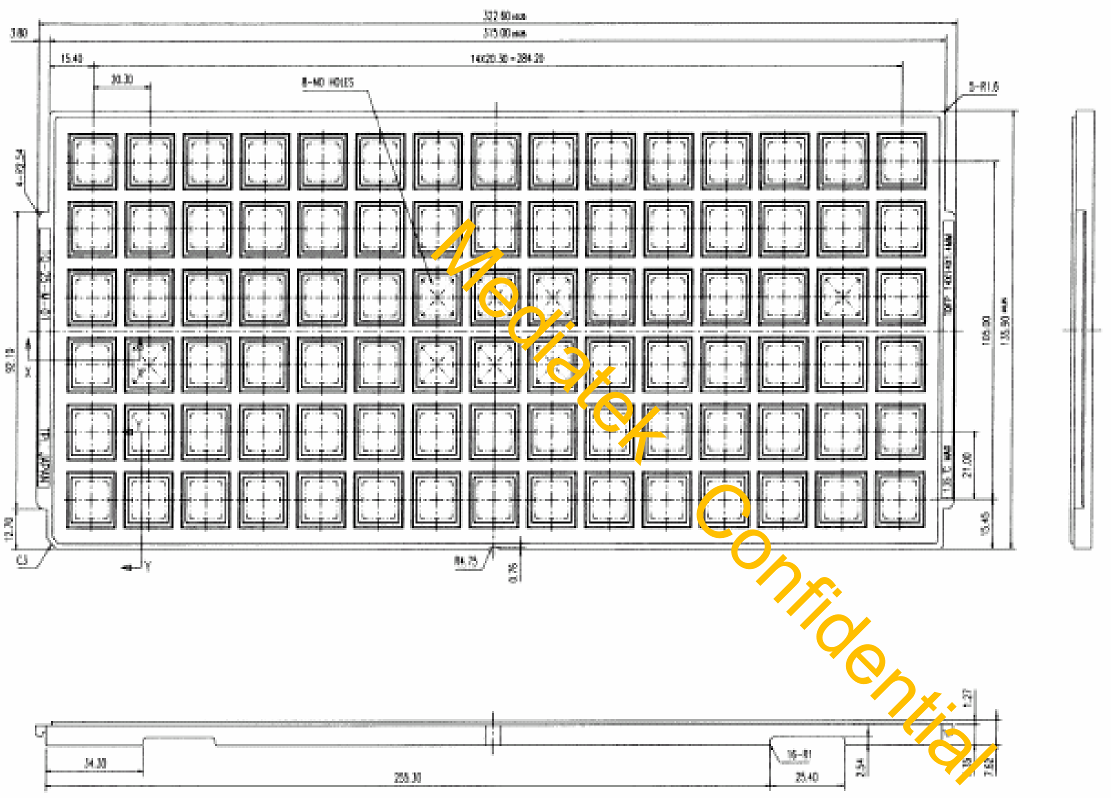
Molding compound: G700

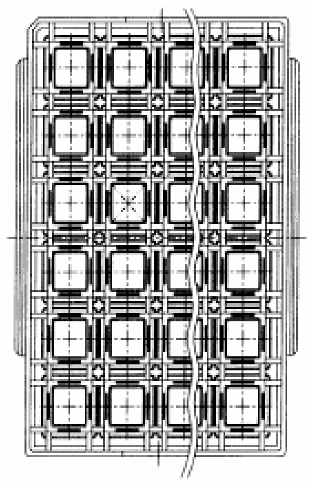
12 Packing Description

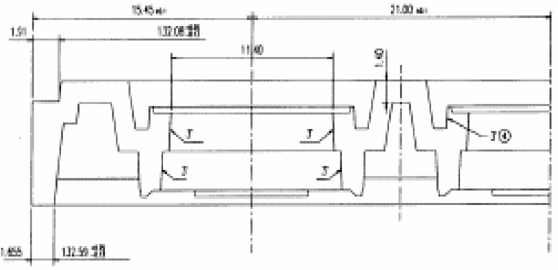
Package	Pin / Ball count	EA / Tray	Tray / Box	Full Box Q'ty	Box / Carton	Full carton Q'ty
LQFP	128	90	10	900	6	5400

12-1 Tray Description

40ea/ Hard Tray (150°C resistance).

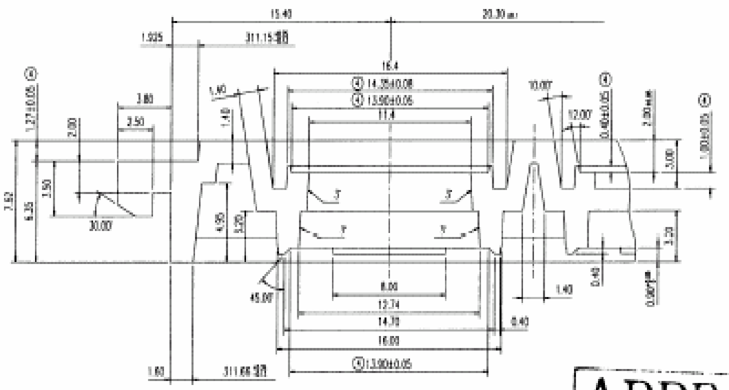






SECTION Y-Y (5:1)

NOTE :
1. HEAT RESISTANCE UP TO 24 HOURS 135°C.
2. SURFACE ELECTRICAL RESISTIVITY IS LESS THAN 10^{12} OM/SQ
3. COLOR : BLACK.
4. WARPAGE : LESS THAN 0.76mm.
5. GENERAL TOLERANCE X.X = ±0.5
X.XX = ±0.25
X.XXX = ±0.13



SECTION X-X (5:1)

APPROVED
BY:
Check By:

TITLE: TQFP 14X14X1.4MM JEDEC TRAY TQ-25-M-01			
APPR.	David Lou	DWG NO.	T0051-1-03
DM.	G. L. Wang	REV NO.	4
CHK.	Johnson Shieh	DATE	1999.8.20
DEN.	Leon	SHT NO.	1/1
TOKYO PRINTING INK MFG. CO., LTD			

REV NO	WORD ON → NEW ON	SIGN	DATE
④		B. S. Chiu	2004.11.16
3	CHANGE TOOLING		

12-2 Desiccants

Size: 110*120 mm.

Weight: 66g

12-3 Aluminum Foil Bag

Size: 250*500 mm.

Thickness: 0.12 +/- 0.005 mm.

Surface impedance: 10^{8}-10^{12} Ohm/SQ

12-4 Box Description

Material: 3 Layer B corrugated paper.

Strength: 1176000 PA.

Box size: 355(L)*157(W)*90.5(H) mm.

Printing: Black (words, warning, index)

12-5 Side Plank

Material: 5 Layer AB corrugated paper

Strength: 1793400 PA.

Size: 405(L)*237(W) mm.

Fixture: 3 pieces of EPE (recyclable material).

Thickness: 20 mm.

12-6 Carton Description

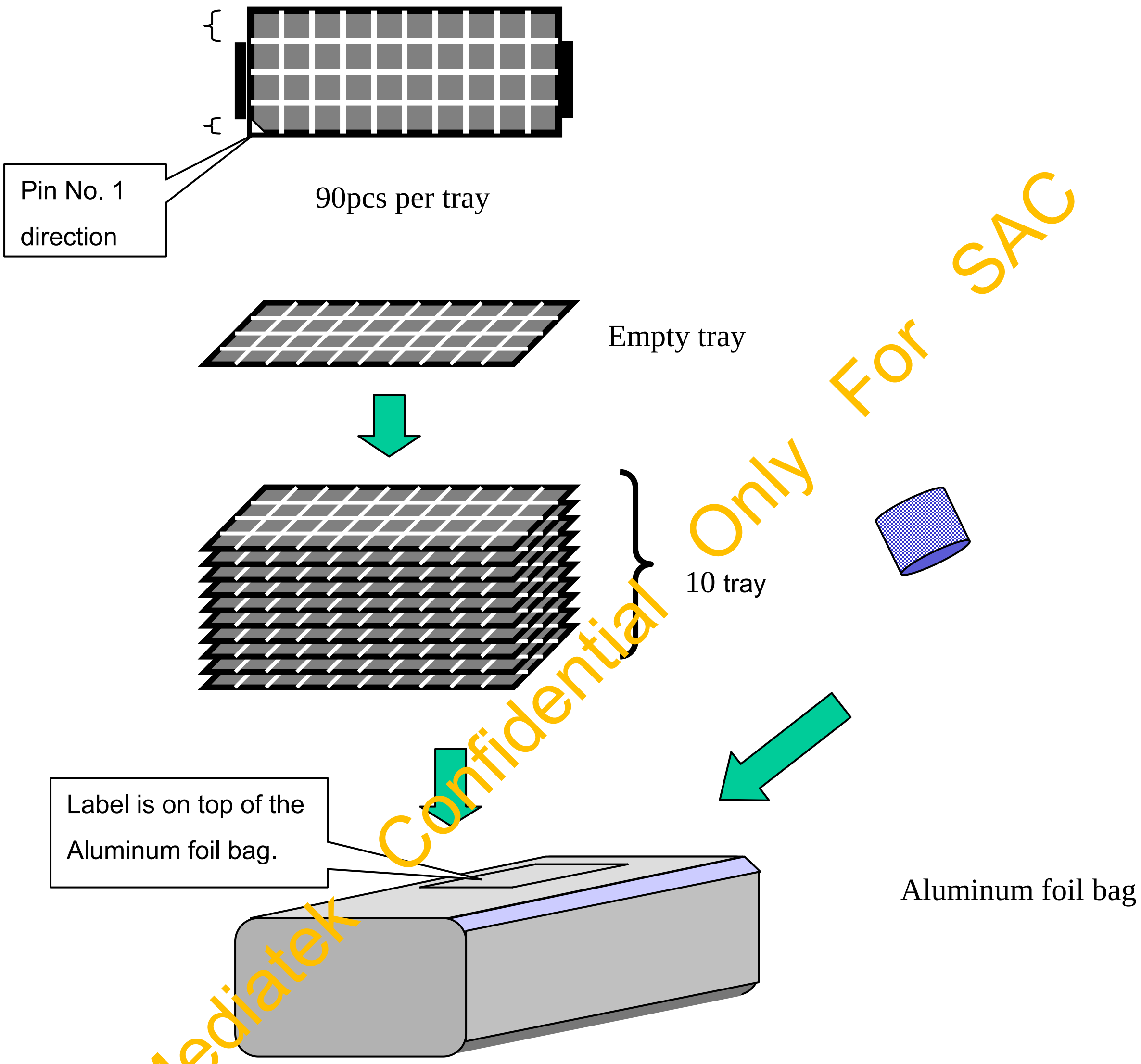
Material: 5 Layer AB corrugated paper.

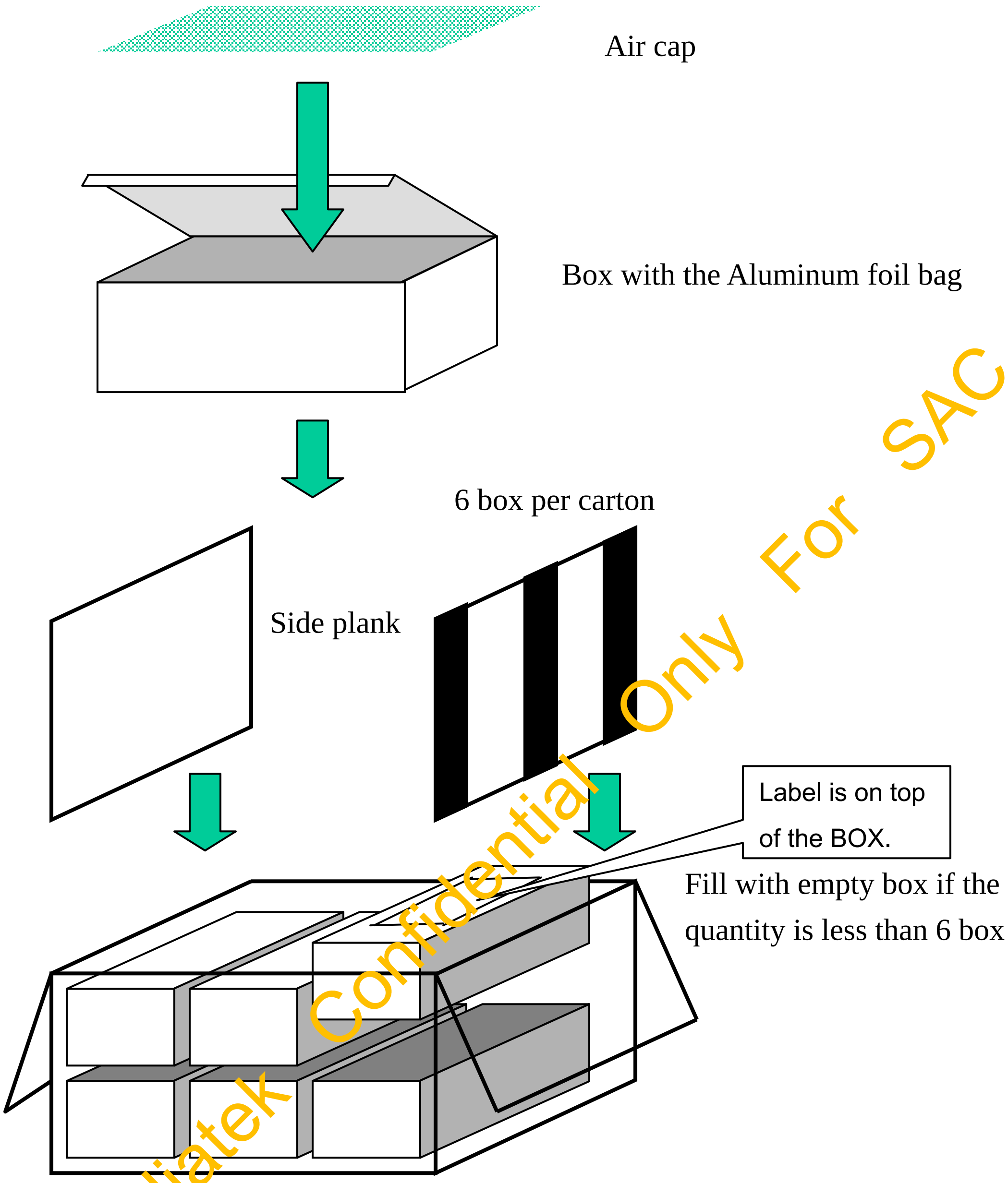
Strength: 1793400 PA.

Carton size: 558(L)*428(W)*264(H) mm.

Printing: Black (words, warning, index)

12-7 Packing Flow




Air cap
Box with the Aluminum foil bag
6 box per carton
Side plank
Label is on top of the BOX.
Fill with empty box if the quantity is less than 6 box

13 Solder-Reflow Condition

13-1 Reflow Condition

MediaTek can guarantee 3 times IR reflow based on the reflow profile (Figure 1).

Average ramp-up rate (Ts to peak): 3 °C /sec. max.

Preheat & Soak: Pb-Free 150~200 °C (SnPb Eutectic 100~150 °C) for 60~120 seconds

Liquidous temperature maintained above Pb-Free 217 °C (SnPb Eutectic 183 °C) for 60~150 seconds

Time within 5 °C of specified classification temperature: Pb-Free 30 seconds (SnPb Eutectic 20 seconds)

Note:

Reflow profiles in this document are for classification/preconditioning and ***are not meant to specify board assembly profiles.*** Actual board assembly profiles should be developed based on specific process needs and board designs and should not exceed the parameters in Table 1.

For example, if Tc is 260 °C and time tp is 30 seconds, this means the following for the supplier and user.

For a supplier: The peak temperature must be at least 260 °C. The time above 255 °C must be at least 30 seconds.

For a user: The peak temperature must not exceed 260 °C. The time above 255 °C must not exceed 30 seconds.

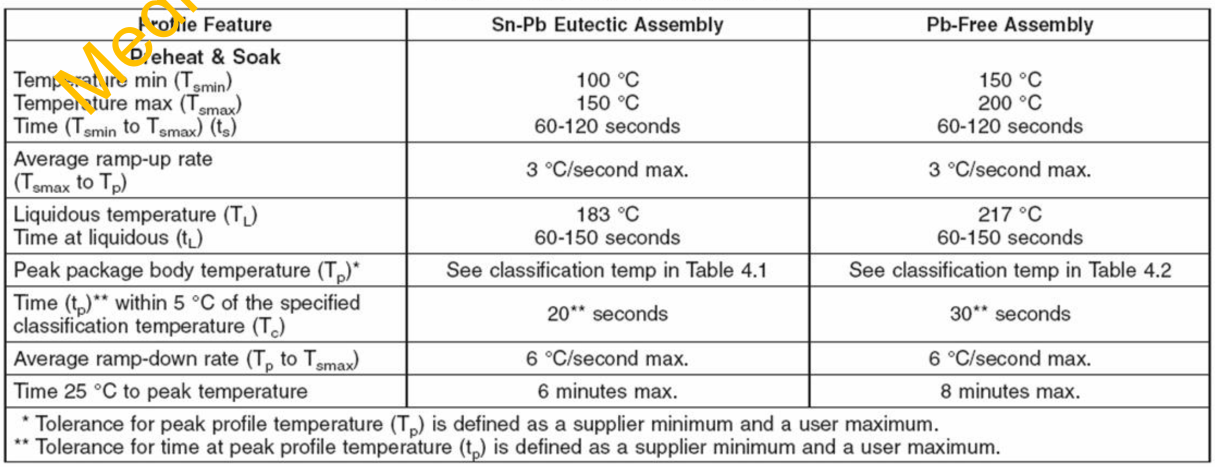
Peak temperature: Defined in Table 2-1 and Table 2-2.

Ramp-down rate: 6 °C /sec. max.

Time 25 °C to peak temperature: Pb-Free: 8 minutes max. (SnPb Eutectic 6 minutes max.)

Time between reflows: 5 minutes minimum and 60 minutes maximum

Table 1 Classification Reflow Profiles



Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_p)	3 °C/second max.	3 °C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body temperature (T_p)*	See classification temp in Table 4.1	See classification temp in Table 4.2
Time (t_p)** within 5 °C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

* Tolerance for peak profile temperature (T_p) is defined as a supplier minimum and a user maximum.
** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.

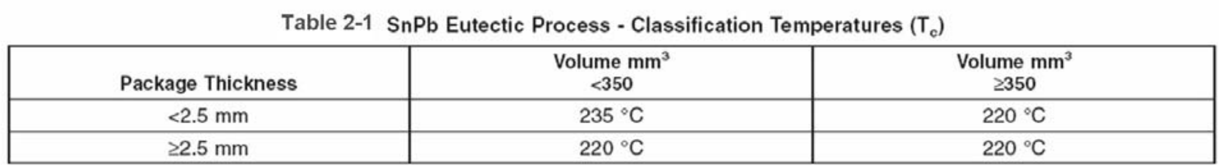


Table 2-1 SnPb Eutectic Process - Classification Temperatures (T_c)

Package Thickness	Volume mm³ <350	Volume mm³ ≥350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

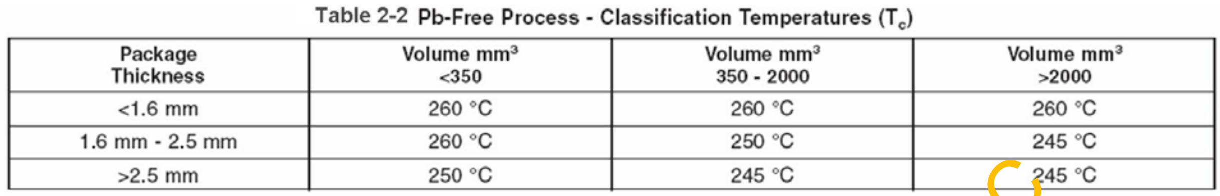


Table 2-2 Pb-Free Process - Classification Temperatures (T_c)

Package Thickness	Volume mm³ <350	Volume mm³ 350 - 2000	Volume mm³ >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm - 2.5 mm	260 °C	250 °C	245 °C
>2.5 mm	250 °C	245 °C	245 °C

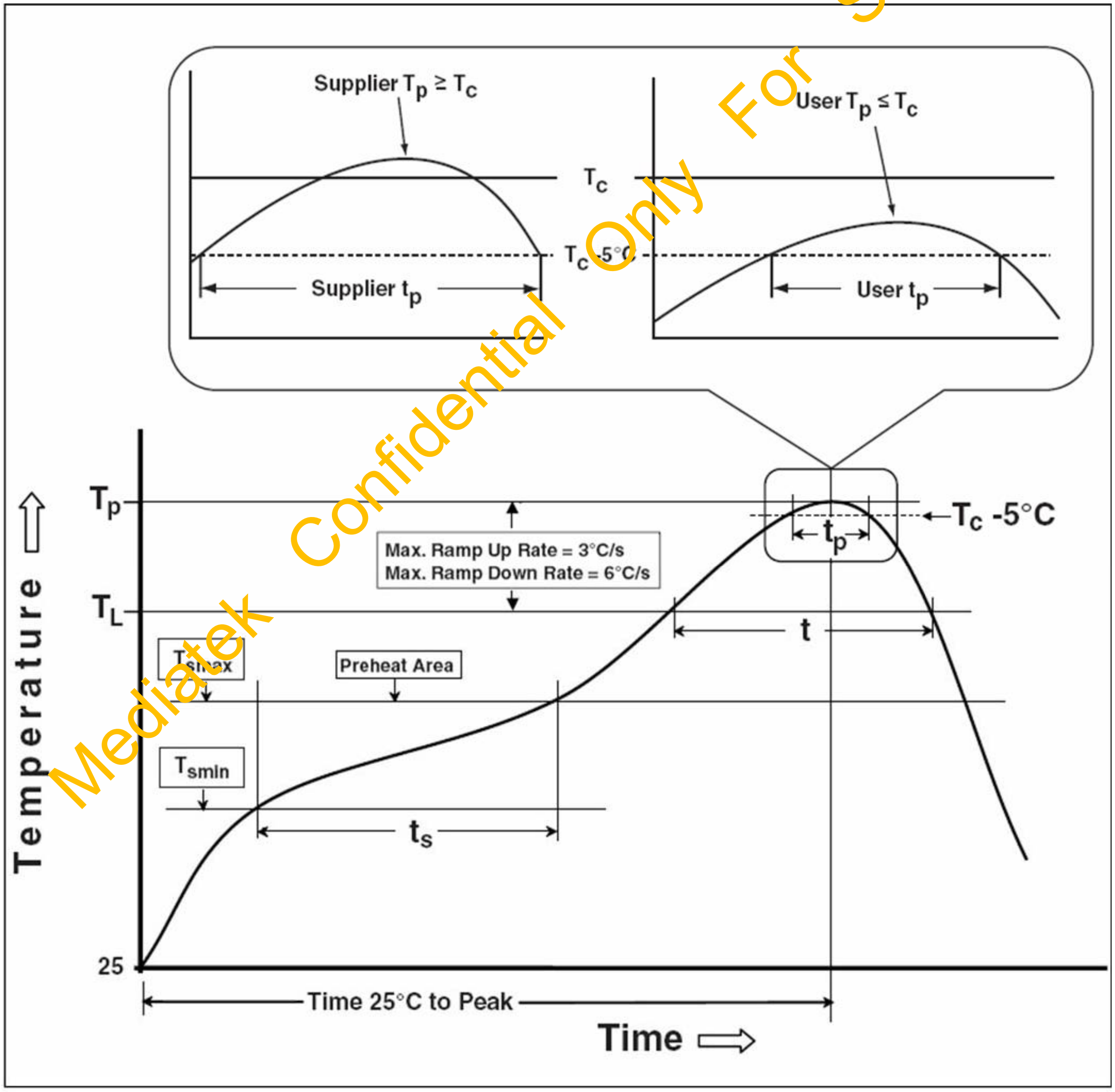


Figure 1 Classification Profile

13-2 Pre-process and Heat Treatment

Procedure: (MRT L3)

[Package opening] → [Baking] → [Humidification] → [Reflow]

A. Conditions between each step of procedure

Be lift for duration of 2 hours or longer at temperature of 30 °C or lower and a humidity of 60% R.H. or lower.

B. Baking 125 °C, 24 hours.

C. Humidification: 30 °C, 60% R.H., 192 Hours

D. Reflow: 3 x 260 °C

14 Manual Solder Condition

The specimen should be in the as-delivered condition. Set the soldering iron at a temperature of 300 +/- 10 °C (at the iron bit). Place the iron and flux-cored solder in parallel with each and every terminal/lead on the back of the board for a duration which does not exceed 5 seconds without applying any mechanical stress on the component body.

It can also be applied under 350 +/- 10 °C at the iron bit within 3 seconds, please treat it carefully under such condition.

The chip can’t do DIP soldering.

15 Storage Condition

15-1 Storage Duration

A. Notice the Sealing time.

B. 12 monthly and storage condition: <= 40°C , <= 90% R.H.

C. Warehouse control: First in and First out.

15-2 After Open the Bag

A. SMT: Should finish the SMT process within 168 hours

B. Check the humidity check card: The value should < 20% (blue), if the value >= 30% (red), it means the IC has got moisture.

C. Factory environment control: <= 30°C, <= 60% R.H.

16 Other

If a doubt related to the present specifications arises, the problem will be solved based on discussion between the both parties.

Purpose

Eon Silicon Solution Inc. (hereinafter called “Eon”) is going to provide its products’ top marking on ICs with < cFeon > from January 1st, 2009, and without any change of the part number and the compositions of the ICs. Eon is still keeping the promise of quality for all the products with the same as that of Eon delivered before. Please be advised with the change and appreciate your kindly cooperation and fully support Eon’s product family.

Eon products’ New Top Marking

cFeon

cFeon Top Marking Example:

cFeon

Part Number: XXXX-XXX
Lot Number: XXXXX
Date Code: XXXXX

Continuity of Specifications

There is no change to this data sheet as a result of offering the device as an Eon product. Any changes that have been made are the result of normal data sheet improvement and are noted in the document revision summary, where supported. Future routine revisions will occur when appropriate, and changes will be noted in a revision summary.

Continuity of Ordering Part Numbers

Eon continues to support existing part numbers beginning with “Eon” and “cFeon” top marking. To order these products, during the transition please specify “Eon top marking” or “cFeon top marking” on your purchasing orders.

For More Information

Please contact your local sales office for additional information about Eon memory solutions.

EN25F16
16 Megabit Serial Flash Memory with 4Kbytes Uniform Sector

FEATURES

- Single power supply operation
  - Full voltage range: 2.7-3.6 volt
- Serial Interface Architecture
  - SPI Compatible: Mode 0 and Mode 3
- 16 Mbit Serial Flash
  - 16 M-bit/2048 K-byte/8192 pages
  - 256 bytes per programmable page
- High performance
  - 100MHz clock rate
- Low power consumption
  - 12 mA typical active current
  - 1 µA typical power down current
- Uniform Sector Architecture:
  - 512 sectors of 4-Kbyte
  - 32 blocks of 64-Kbyte
  - Any sector or block can be erased individually
- Software and Hardware Write Protection:
  - Write Protect all or portion of memory via software
  - Enable/Disable protection with WP# pin
- High performance program/erase speed
  - Page program time: 1.3ms typical
  - Sector erase time: 90ms typical
  - Block erase time 400ms typical
  - Chip erase time: 7 Seconds typical
- Lockable 128 byte OTP security sector
- Minimum 100K endurance cycle
- Package Options
  - 8 pins SOP 200mil body width
  - 8 contact VDFN
  - 8 pins PDIP
  - All Pb-free packages are RoHS compliant
- Industrial temperature Range

GENERAL DESCRIPTION

The EN25F16 is a 16M-bit (2048K-byte) Serial Flash memory, with advanced write protection mechanisms, accessed by a high speed SPI-compatible bus. The memory can be programmed 1 to 256 bytes at a time, using the Page Program instruction.

The EN25F16 is designed to allow either single Sector/Block at a time or full chip erase operation. The EN25F16 can be configured to protect part of the memory as the software protected mode. The device can sustain a minimum of 100K program/erase cycles on each sector or block.

Figure.1 CONNECTION DIAGRAMS

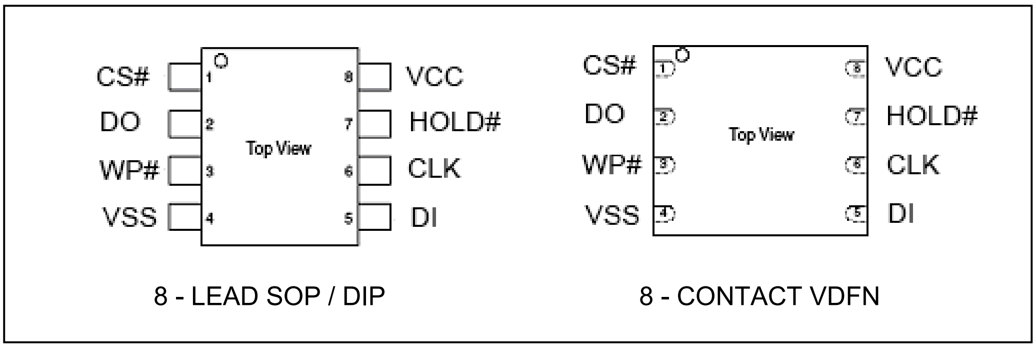
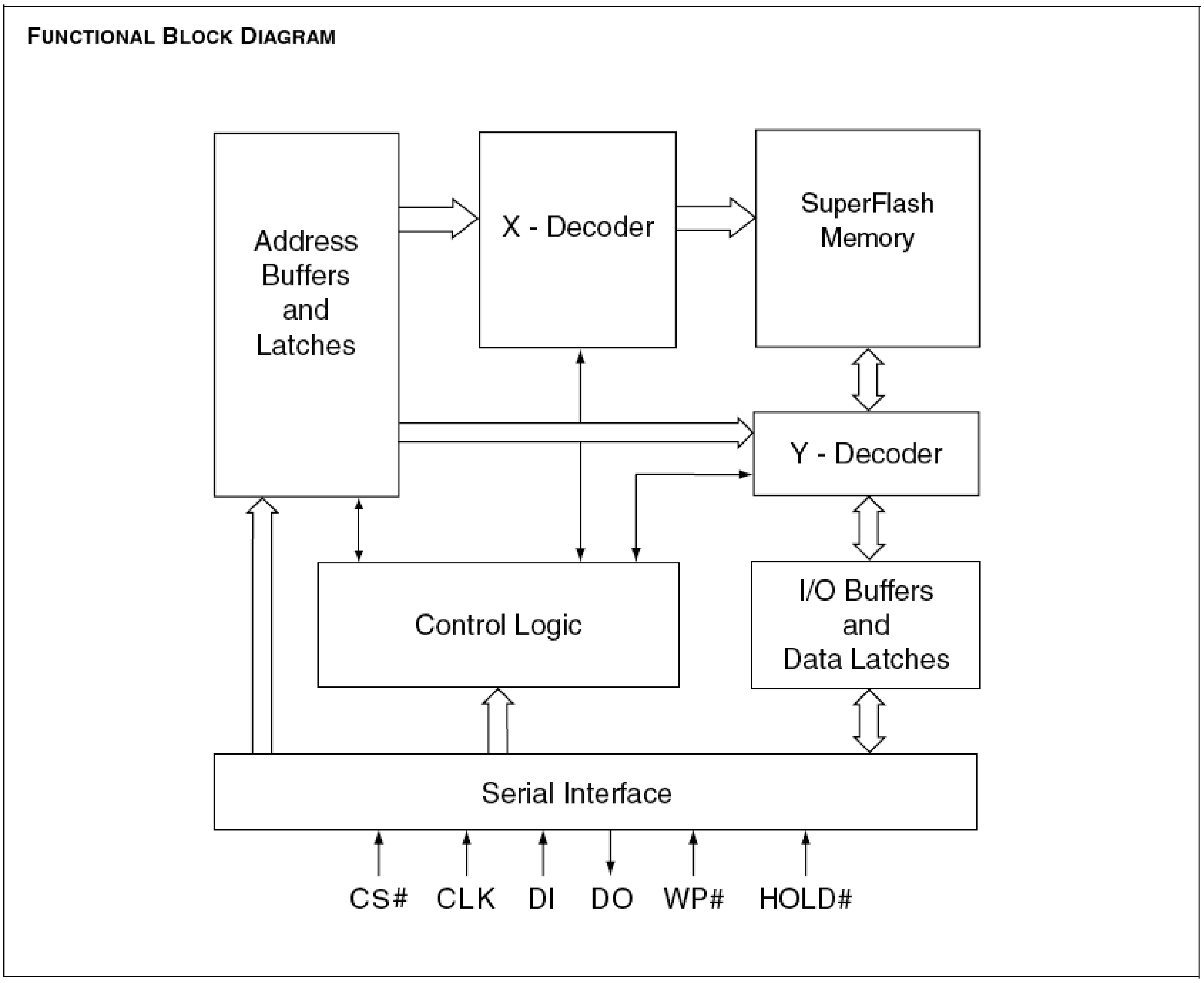


Figure 2. BLOCK DIAGRAM



SIGNAL DESCRIPTION

Serial Data Input (DI)
The SPI Serial Data Input (DI) pin provides a means for instructions, addresses and data to be serially written to (shifted into) the device. Data is latched on the rising edge of the Serial Clock (CLK) input pin.

Serial Data Output (DO)
The SPI Serial Data Output (DO) pin provides a means for data and status to be serially read from (shifted out of) the device. Data is shifted out on the falling edge of the Serial Clock (CLK) input pin.

Serial Clock (CLK)
The SPI Serial Clock Input (CLK) pin provides the timing for serial input and output operations. ("See SPI Mode")

Chip Select (CS#)
The SPI Chip Select (CS#) pin enables and disables device operation. When CS# is high the device is deselected and the Serial Data Output (DO) pin is at high impedance. When deselected, the devices power consumption will be at standby levels unless an internal erase, program or status register cycle is in progress. When CS# is brought low the device will be selected, power consumption will increase to active levels and instructions can be written to and data read from the device. After power-up, CS# must transition from high to low before a new instruction will be accepted.

Hold (HOLD#)
The HOLD pin allows the device to be paused while it is actively selected. When HOLD is brought low, while CS# is low, the DO pin will be at high impedance and signals on the DI and CLK pins will be ignored (don't care). The hold function can be useful when multiple devices are sharing the same SPI signals.

Write Protect (WP#)
The Write Protect (WP#) pin can be used to prevent the Status Register from being written. Used in conjunction with the Status Register's Block Protect (BP0, BP1and BP2) bits and Status Register Protect (SRP) bits, a portion or the entire memory array can be hardware protected.

Table 1. PIN Names

Symbol	**Pin Name**
CLK	Serial Clock Input
DI	Serial Data Input
DO	Serial Data Output
CS#	Chip Enable
WP#	Write Protect
HOLD#	Hold Input
Vcc	Supply Voltage (2.7-3.6V)
Vss	Ground

MEMORY ORGANIZATION

The memory is organized as:

- 2,097,152 bytes
- Uniform Sector Architecture
  32 blocks of 64-Kbyte
  512 sectors of 4-Kbyte
- 8192 pages (256 bytes each)

Each page can be individually programmed (bits are programmed from 1 to 0). The device is Sector, Block or Chip Erasable but not Page Erasable.

Table 2. Uniform Block Sector Architecture

Block	Sector	Address range	
31	511	1FF000	1FFFFF
	⋮	⋮	⋮
	496	1F0000	1F0FFF
30	495	1EF000	1EFFFF
	⋮	⋮	⋮
	480	1E0000	1E0FFF
29	479	1DF000	1DFFFF
	⋮	⋮	⋮
	464	1D0000	1D0FFF
28	463	1CF000	1CFFFF
	⋮	⋮	⋮
	448	1C0000	1C0FFF
27	447	1BF000	1BFFFF
	⋮	⋮	⋮
	432	1B0000	1B0FFF
26	431	1AF000	1AFFFF
	⋮	⋮	⋮
	416	1A0000	1A0FFF
25	415	19F000	19FFFF
	⋮	⋮	⋮
	400	190000	190FFF
24	399	18F000	18FFFF
	⋮	⋮	⋮
	384	180000	180FFF
23	383	17F000	17FFFF
	⋮	⋮	⋮
	368	170000	170FFF
22	367	16F000	16FFFF
	⋮	⋮	⋮
	352	160000	160FFF
21	351	15F000	15FFFF
	⋮	⋮	⋮
	336	150000	150FFF
20	335	14F000	14FFFF
	⋮	⋮	⋮
	320	140000	140FFF
19	319	13F000	13FFFF
	⋮	⋮	⋮
	304	130000	130FFF
18	303	12F000	12FFFF
	⋮	⋮	⋮
	288	120000	120FFF
17	287	11F000	11FFFF
	⋮	⋮	⋮
	272	110000	110FFF
16	271	10F000	10FFFF
	⋮	⋮	⋮
	256	100000	100FFF
15	255	0FF000h	0FFFFFh
	⋮	⋮	⋮
	240	0F0000h	0F0FFFh

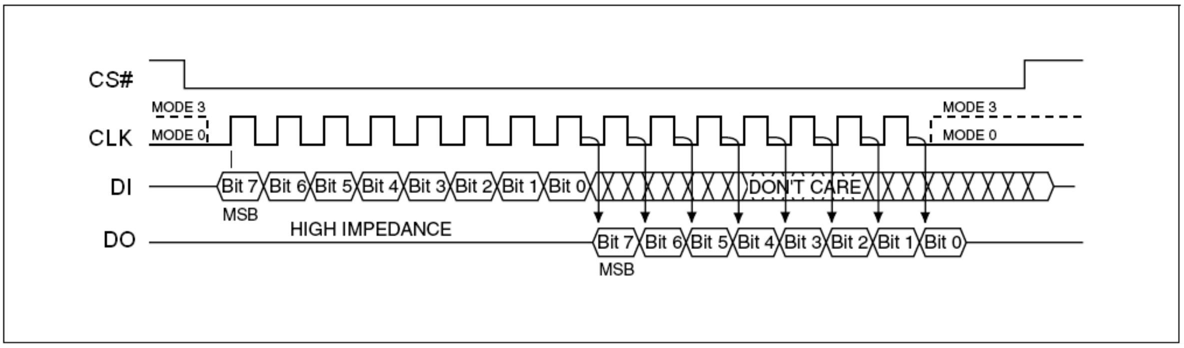
14	239	0EF000h	0EFFFFh
	⋮	⋮	⋮
	224	0E0000h	0E0FFFh
13	223	0DF000h	0DFFFFh
	⋮	⋮	⋮
	208	0D0000h	0D0FFFh
12	207	0CF000h	0CFFFFh
	⋮	⋮	⋮
	192	0C0000h	0C0FFFh
11	191	0BF000h	0BFFFFh
	⋮	⋮	⋮
	176	0B0000h	0B0FFFh
10	175	0AF000h	0AFFFFh
	⋮	⋮	⋮
	160	0A0000h	0A0FFFh
9	159	09F000h	09FFFFh
	⋮	⋮	⋮
	144	090000h	090FFFh
8	143	08F000h	08FFFFh
	⋮	⋮	⋮
	128	080000h	080FFFh
7	127	07F000h	07FFFFh
	⋮	⋮	⋮
	112	070000h	070FFFh
6	111	06F000h	06FFFFh
	⋮	⋮	⋮
	96	060000h	060FFFh
5	95	05F000h	05FFFFh
	⋮	⋮	⋮
	80	050000h	050FFFh
4	79	04F000h	04FFFFh
	⋮	⋮	⋮
	64	040000h	040FFFh
3	63	03F000h	03FFFFh
	⋮	⋮	⋮
	48	030000h	030FFFh
2	47	02F000h	02FFFFh
	⋮	⋮	⋮
	32	020000h	020FFFh
1	31	01F000h	01FFFFh
	⋮	⋮	⋮
	16	010000h	010FFFh
0	15	00F000h	00FFFFh
	⋮	⋮	⋮
	4	004000h	004FFFh
	3	003000h	003FFFh
	2	002000h	002FFFh
	1	001000h	001FFFh
	0	000000h	000FFFh

OPERATING FEATURES

SPI Modes

The EN25F16 is accessed through an SPI compatible bus consisting of four signals: Serial Clock (CLK), Chip Select (CS#), Serial Data Input (DI) and Serial Data Output (DO). Both SPI bus operation Modes 0 (0,0) and 3 (1,1) are supported. The primary difference between Mode 0 and Mode 3, as shown in Figure 3, concerns the normal state of the CLK signal when the SPI bus master is in standby and data is not being transferred to the Serial Flash. For Mode 0 the CLK signal is normally low. For Mode 3 the CLK signal is normally high. In either case data input on the DI pin is sampled on the rising edge of the CLK. Data output on the DO pin is clocked out on the falling edge of CLK.

Figure 3. SPI Modes



Page Programming

To program one data byte, two instructions are required: Write Enable (WREN), which is one byte, and a Page Program (PP) sequence, which consists of four bytes plus data. This is followed by the internal Program cycle (of duration t_{PP}).

To spread this overhead, the Page Program (PP) instruction allows up to 256 bytes to be programmed at a time (changing bits from 1 to 0), provided that they lie in consecutive addresses on the same page of memory.

Sector Erase, Block Erase and Chip Erase

The Page Program (PP) instruction allows bits to be reset from 1 to 0. Before this can be applied, the bytes of memory need to have been erased to all 1s (FFh). This can be achieved a sector at a time, using the Sector Erase (SE) instruction, a block at a time using the Block Erase (BE) instruction or throughout the entire memory, using the Chip Erase (CE) instruction. This starts an internal Erase cycle (of duration t_{SE} t_{BE} or t_{CE}). The Erase instruction must be preceded by a Write Enable (WREN) instruction.

Polling During a Write, Program or Erase Cycle

A further improvement in the time to Write Status Register (WRSR), Program (PP) or Erase (SE, BE or CE) can be achieved by not waiting for the worst case delay (t_W, t_{PP}, t_{SE}, t_{BE} or t_{CE}). The Write In Progress (WIP) bit is provided in the Status Register so that the application program can monitor its value, polling it to establish when the previous Write cycle, Program cycle or Erase cycle is complete.

Active Power, Stand-by Power and Deep Power-Down Modes

When Chip Select (CS#) is Low, the device is enabled, and in the Active Power mode. When Chip Select (CS#) is High, the device is disabled, but could remain in the Active Power mode until all internal cycles have completed (Program, Erase, Write Status Register). The device then goes into the Stand-by Power mode. The device consumption drops to I_{CC1}.

The Deep Power-down mode is entered when the specific instruction (the Enter Deep Power-down Mode (DP) instruction) is executed. The device consumption drops further to I_{CC2}. The device remains in this mode until another specific instruction (the Release from Deep Power-down Mode and Read Device ID (RDI) instruction) is executed.

All other instructions are ignored while the device is in the Deep Power-down mode. This can be used as an extra software protection mechanism, when the device is not in active use, to protect the device from inadvertent Write, Program or Erase instructions.

Status Register. The Status Register contains a number of status and control bits that can be read or set (as appropriate) by specific instructions.

WIP bit. The Write In Progress (WIP) bit indicates whether the memory is busy with a Write Status Register, Program or Erase cycle.

WEL bit. The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch.

BP2, BP1, BP0 bits. The Block Protect (BP2, BP1, BP0) bits are non-volatile. They define the size of the area to be software protected against Program and Erase instructions.

SRP bit / OTP_LOCK bit The Status Register Protect (SRP) bit is operated in conjunction with the Write Protect (WP#) signal. The Status Register Protect (SRP) bit and Write Protect (WP#) signal allow the device to be put in the Hardware Protected mode. In this mode, the non-volatile bits of the Status Register (SRP, BP2, BP1, BP0) become read-only bits.

In OTP mode, this bit is served as OTP_LOCK bit, user can read/program/erase OTP sector as normal sector while OTP_LOCK value is equal 0, after OTP_LOCK is programmed with 1 by WRSR command, the OTP sector is protected from program and erase operation. The OTP_LOCK bit can only be programmed once.

Note : In OTP mode, the WRSR command will ignore any input data and program OTP_LOCK bit to 1, user must clear the protect bits before enter OTP mode and program the OTP code, then execute WRSR command to lock the OTP sector before leaving OTP mode.

Write Protection

Applications that use non-volatile memory must take into consideration the possibility of noise and other adverse system conditions that may compromise data integrity. To address this concern the EN25F16 provides the following data protection mechanisms:

- Power-On Reset and an internal timer (t_{PUW}) can provide protection against inadvertent changes while the power supply is outside the operating specification.
- Program, Erase and Write Status Register instructions are checked that they consist of a number of clock pulses that is a multiple of eight, before they are accepted for execution.
- All instructions that modify data must be preceded by a Write Enable (WREN) instruction to set the Write Enable Latch (WEL) bit . This bit is returned to its reset state by the following events:
  - Power-up
  - Write Disable (WRDI) instruction completion or Write Status Register (WRSR) instruction completion or Page Program (PP) instruction completion or Sector Erase (SE) instruction completion or Block Erase (BE) instruction completion or Chip Erase (CE) instruction completion
- The Block Protect (BP2, BP1, BP0) bits allow part of the memory to be configured as read-only. This is the Software Protected Mode (SPM).
- The Write Protect (WP#) signal allows the Block Protect (BP2, BP1, BP0) bits and Status Register Protect (SRP) bit to be protected. This is the Hardware Protected Mode (HPM).
- In addition to the low power consumption feature, the Deep Power-down mode offers extra software protection from inadvertent Write, Program and Erase instructions, as all instructions are ignored except one particular instruction (the Release from Deep Power-down instruction).

Table 3. Protected Area Sizes Sector Organization

Status Register Content			Memory Content			
BP2 Bit	**BP1 Bit**	**BP0 Bit**	**Protect Areas**	**Addresses**	**Density(KB)**	**Portion**
0	0	0	None	None	None	None
0	0	1	RFU	RFU	RFU	RFU
0	1	0				
0	1	1				
1	0	0				
1	0	1				
1	1	0				
1	1	1	All	000000h-1FFFFFh	2048KB	All

Note: RFU = Reserved for future use

Hold Function

The Hold (HOLD) signal is used to pause any serial communications with the device without resetting the clocking sequence. However, taking this signal Low does not terminate any Write Status Register, Program or Erase cycle that is currently in progress.

To enter the Hold condition, the device must be selected, with Chip Select (CS#) Low. The Hold condition starts on the falling edge of the Hold (HOLD) signal, provided that this coincides with Serial Clock (CLK) being Low (as shown in Figure 4.).

The Hold condition ends on the rising edge of the Hold (HOLD) signal, provided that this coincides with Serial Clock (CLK) being Low.

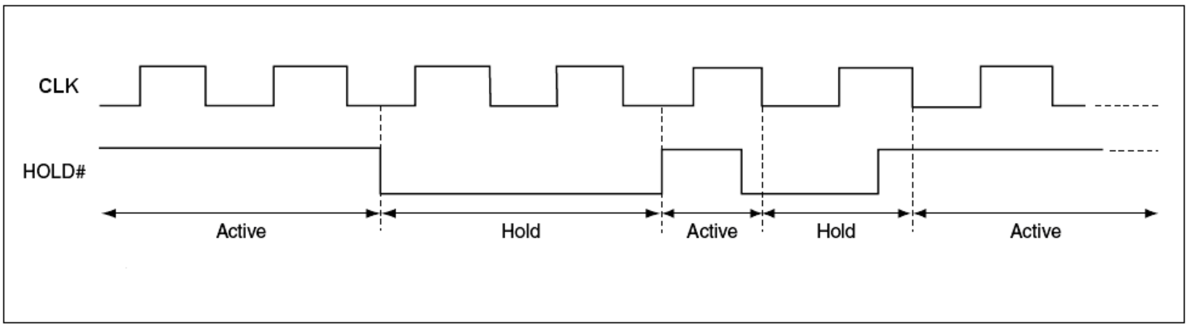
If the falling edge does not coincide with Serial Clock (CLK) being Low, the Hold condition starts after Serial Clock (CLK) next goes Low. Similarly, if the rising edge does not coincide with Serial Clock (CLK) being Low, the Hold condition ends after Serial Clock (CLK) next goes Low. (This is shown in Figure 4.).

During the Hold condition, the Serial Data Output (DO) is high impedance, and Serial Data Input (DI) and Serial Clock (CLK) are Don't Care.

Normally, the device is kept selected, with Chip Select (CS#) driven Low, for the whole duration of the Hold condition. This is to ensure that the state of the internal logic remains unchanged from the moment of entering the Hold condition.

If Chip Select (CS#) goes High while the device is in the Hold condition, this has the effect of resetting the internal logic of the device. To restart communication with the device, it is necessary to drive Hold (HOLD) High, and then to drive Chip Select (CS#) Low. This prevents the device from going back to the Hold condition.

Figure 4. Hold Condition Waveform



INSTRUCTIONS

All instructions, addresses and data are shifted in and out of the device, most significant bit first. Serial Data Input (DI) is sampled on the first rising edge of Serial Clock (CLK) after Chip Select (CS#) is driven Low. Then, the one-byte instruction code must be shifted in to the device, most significant bit first, on Serial Data Input (DI), each bit being latched on the rising edges of Serial Clock (CLK).

The instruction set is listed in Table 4. Every instruction sequence starts with a one-byte instruction code. Depending on the instruction, this might be followed by address bytes, or by data bytes, or by both or none. Chip Select (CS#) must be driven High after the last bit of the instruction sequence has been shifted in. In the case of a Read Data Bytes (READ), Read Data Bytes at Higher Speed (Fast_Read), Read Status Register (RDSR) or Release from Deep Power-down, and Read Device ID (RDI) instruction, the shifted-in instruction sequence is followed by a data-out sequence. Chip Select (CS#) can be driven High after any bit of the data-out sequence is being shifted out.

In the case of a Page Program (PP), Sector Erase (SE), Block Erase (BE), Chip Erase (CE), Write Status Register (WRSR), Write Enable (WREN), Write Disable (WRDI) or Deep Power-down (DP) instruction, Chip Select (CS#) must be driven High exactly at a byte boundary, otherwise the instruction is rejected, and is not executed. That is, Chip Select (CS#) must driven High when the number of clock pulses after Chip Select (CS#) being driven Low is an exact multiple of eight. For Page Program, if at any time the input byte is not a full byte, nothing will happen and WEL will not be reset.

In the case of multi-byte commands of Page Program (PP), and Release from Deep Power Down (RES) minimum number of bytes specified has to be given, without which, the command will be ignored.

In the case of Page Program, if the number of byte after the command is less than 4 (at least 1 data byte), it will be ignored too. In the case of SE and BE, exact 24-bit address is a must, any less or more will cause the command to be ignored.

All attempts to access the memory array during a Write Status Register cycle, Program cycle or Erase cycle are ignored, and the internal Write Status Register cycle, Program cycle or Erase cycle continues unaffected.

Table 4. Instruction Set

Instruction Name	Byte 1 Code	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	n-Bytes
Write Enable	06h						
Write Disable / Exit OTP mode	04h						
Read Status Register	05h	(S7-S0)(1)					continuous(2)
Write Status Register	01h	S7-S0					
Read Data	03h	A23-A16	A15-A8	A7-A0	(D7-D0)	(Next byte)	continuous
Fast Read	0Bh	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	(Next Byte) continuous
Page Program	02h	A23-A16	A15-A8	A7-A0	D7-D0	Next byte	continuous
Sector Erase	20h	A23-A16	A15-A8	A7-A0			
Block Erase	D8h/ 52h	A23-A16	A15-A8	A7-A0			
Chip Erase	C7h/ 60h						
Deep Power-down	B9h						
Release from Deep Power-down, and read Device ID	ABh	dummy	dummy	dummy	(ID7-ID0)		(3)
Release from Deep Power-down							

Manufacturer/ Device ID	90h	dummy	dummy	00h	(M7-M0)	(ID7-ID0)	(4)
				01h	(ID7-ID0)	(M7-M0)	
Read Identification	9Fh	(M7-M0)	(ID15-ID8)	(ID7-ID0)	(5)		
Enter OTP mode	3Ah						

Notes:
1. Data bytes are shifted with Most Significant Bit first. Byte fields with data in parenthesis "( )" indicate data being read from the device on the DO pin.
2. The Status Register contents will repeat continuously until CS# terminate the instruction.
3. The Device ID will repeat continuously until CS# terminate the instruction.
4. The Manufacturer ID and Device ID bytes will repeat continuously until CS# terminate the instruction.
   00h on Byte 4 starts with MID and alternate with DID, 01h on Byte 4 starts with DID and alternate with MID.
5. (M7-M0) : Manufacturer, (ID15-ID8) : Memory Type, (ID7-ID0) : Memory Capacity

Table 5. Manufacturer and Device Identification

OP Code	(M7-M0)	(ID15-ID0)	(ID7-ID0)
ABh			14h
90h	1Ch		14h
9Fh	1Ch	3115h	

Write Enable (WREN) (06h)

The Write Enable (WREN) instruction (Figure 5) sets the Write Enable Latch (WEL) bit. The Write Enable Latch (WEL) bit must be set prior to every Page Program (PP), Sector Erase (SE), Block Erase (BE), Chip Erase (CE) and Write Status Register (WRSR) instruction.
The Write Enable (WREN) instruction is entered by driving Chip Select (CS#) Low, sending the instruction code, and then driving Chip Select (CS#) High.

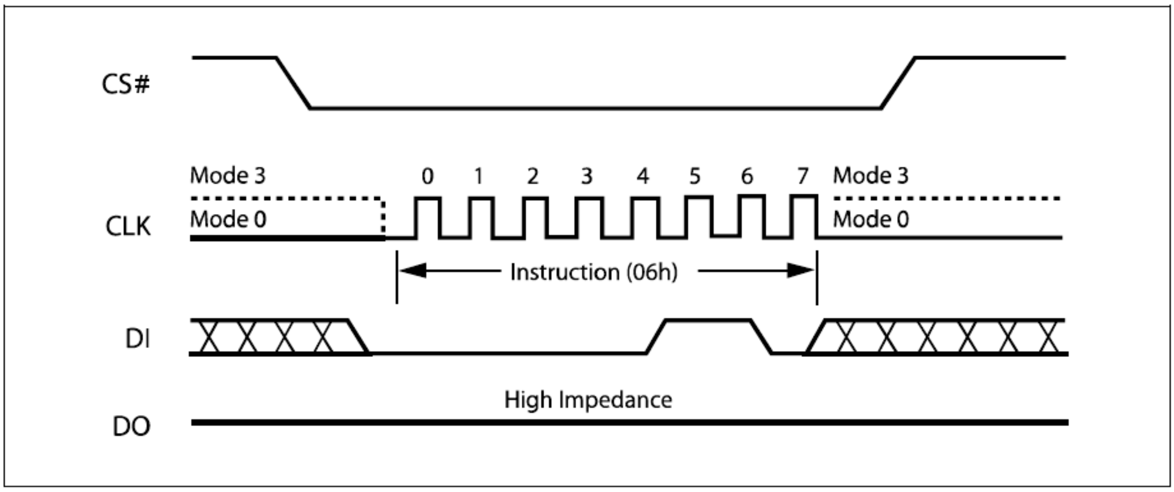


Figure 5. Write Enable Instruction Sequence Diagram

Write Disable (WRDI) (04h)

The Write Disable instruction (Figure 6) resets the Write Enable Latch (WEL) bit in the Status Register to a 0 or exit from OTP mode to normal mode. The Write Disable instruction is entered by driving Chip Select (CS#) low, shifting the instruction code "04h" into the DI pin and then driving Chip Select (CS#) high. Note that the WEL bit is automatically reset after Power-up and upon completion of the Write Status Register, Page Program, Sector Erase, Block Erase (BE) and Chip Erase instructions.

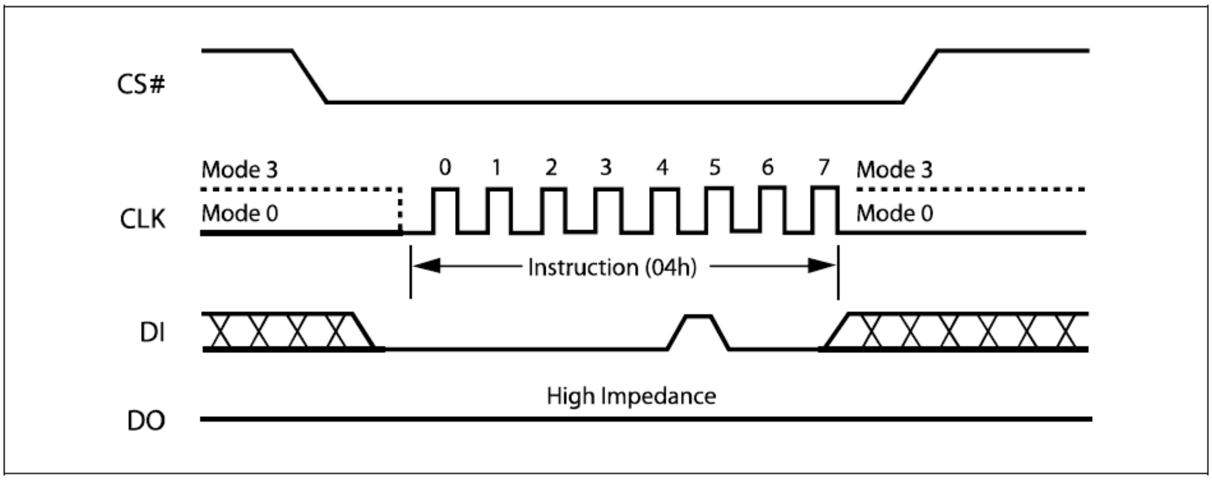


Figure 6. Write Disable Instruction Sequence Diagram

Read Status Register (RDSR) (05h)

The Read Status Register (RDSR) instruction allows the Status Register to be read. The Status Register may be read at any time, even while a Program, Erase or Write Status Register cycle is in progress. When one of these cycles is in progress, it is recommended to check the Write In Progress (WIP) bit before sending a new instruction to the device. It is also possible to read the Status Register continuously, as shown in Figure 7.

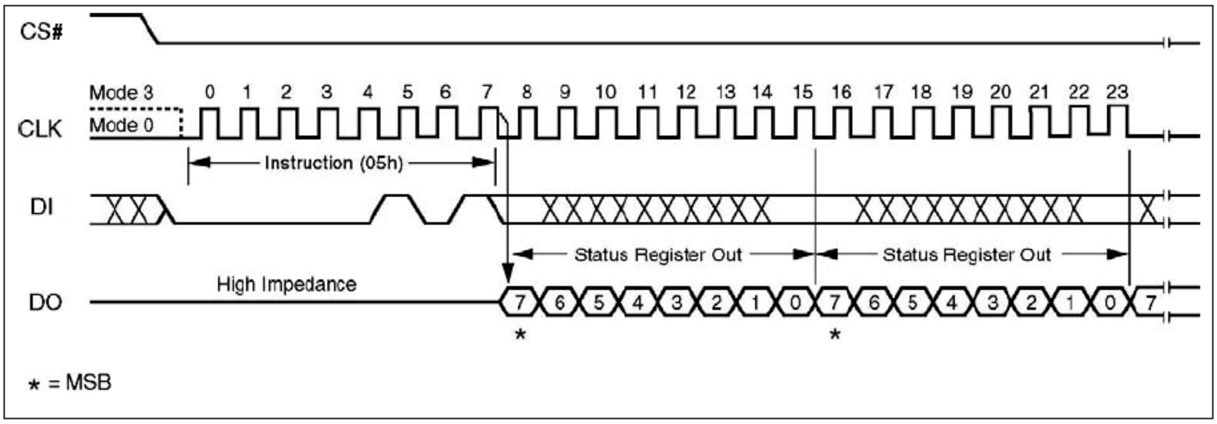


Figure 7. Read Status Register Instruction Sequence Diagram

Table 6. Status Register Bit Locations

S7		S6	S5	S4	S3	S2	S1	S0
SRP Status Register Protect	OTP_LOCK bit (note 1)	Reserved bits	Reserved bits	BP2 (Block Protected bits)	BP1 (Block Protected bits)	BP0 (Block Protected bits)	WEL (Write Enable Latch)	WIP (Write In Progress bit)
1 = status register write disable	1 = OTP sector is protected			(note 2)	(note 2)	(note 2)	1 = write enable 0 = not write enable	1 = write operation 0 = not in write operation
Non-volatile bit				Non-volatile bit	Non-volatile bit	Non-volatile bit	volatile bit	volatile bit

Note

1. In OTP mode, SRP bit is served as OTP_LOCK bit.
2. See the table “Protected Area Sizes Sector Organization”.

The status and control bits of the Status Register are as follows:

WIP bit. The Write In Progress (WIP) bit indicates whether the memory is busy with a Write Status Register, Program or Erase cycle. When set to 1, such a cycle is in progress, when reset to 0 no such cycle is in progress.

WEL bit. The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch. When set to 1 the internal Write Enable Latch is set, when set to 0 the internal Write Enable Latch is reset and no Write Status Register, Program or Erase instruction is accepted.

BP2, BP1, BP0 bits. The Block Protect (BP2, BP1, BP0) bits are non-volatile. They define the size of the area to be software protected against Program and Erase instructions. These bits are written with the Write Status Register (WRSR) instruction. When one or both of the Block Protect (BP2, BP1, BP0) bits is set to 1, the relevant memory area (as defined in Table 3.) becomes protected against Page Program (PP) Sector Erase (SE) and , Block Erase (BE), instructions. The Block Protect (BP2, BP1, BP0) bits can be written provided that the Hardware Protected mode has not been set. The Chip Erase (CE) instruction is executed if, and only if, all Block Protect (BP2, BP1, BP0) bits are 0.

Reserved bit. Status register bit locations 5 and 6 are reserved for future use. Current devices will read 0 for these bit locations. It is recommended to mask out the reserved bit when testing the Status Register. Doing this will ensure compatibility with future devices.

SRP bit / OTP_LOCK bit. The Status Register Protect (SRP) bit is operated in conjunction with the Write Protect (WP#) signal. The Status Register Write Protect (SRP) bit and Write Protect (WP#) signal allow the device to be put in the Hardware Protected mode (when the Status Register Protect (SRP) bit is set to 1, and Write Protect (WP#) is driven Low). In this mode, the non-volatile bits of the Status Register (SRP, BP2, BP1, BP0) become read-only bits and the Write Status Register (WRSR) instruction is no longer accepted for execution.

In OTP mode, this bit is served as OTP_LOCK bit, user can read/program/erase OTP sector as normal sector while OTP_LOCK value is equal 0, after OTP_LOCK is programmed with 1 by WRSR command, the OTP sector is protected from program and erase operation. The OTP_LOCK bit can only be programmed once.

Note : In OTP mode, the WRSR command will ignore any input data and program OTP_LOCK bit to 1, user must clear the protect bits before enter OTP mode and program the OTP code, then execute WRSR command to lock the OTP sector before leaving OTP mode.

Write Status Register (WRSR) (01h)

The Write Status Register (WRSR) instruction allows new values to be written to the Status Register. Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded and executed, the device sets the Write Enable Latch (WEL).

The Write Status Register (WRSR) instruction is entered by driving Chip Select (CS#) Low, followed by the instruction code and the data byte on Serial Data Input (DI).

The instruction sequence is shown in Figure 8. The Write Status Register (WRSR) instruction has no effect on S6, S5, S1 and S0 of the Status Register. S6 and S5 are always read as 0. Chip Select (CS#) must be driven High after the eighth bit of the data byte has been latched in. If not, the Write Status Register (WRSR) instruction is not executed. As soon as Chip Select (CS#) is driven High, the self-timed Write Status Register cycle (whose duration is t_W) is initiated. While the Write Status Register cycle is in progress, the Status Register may still be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Write Status Register cycle, and is 0 when it is completed. When the cycle is completed, the Write Enable Latch (WEL) is reset.

The Write Status Register (WRSR) instruction allows the user to change the values of the Block Protect (BP2, BP1, BP0) bits, to define the size of the area that is to be treated as read-only, as defined in Table 3.. The Write Status Register (WRSR) instruction also allows the user to set or reset the Status Register Protect (SRP) bit in accordance with the Write Protect (WP#) signal. The Status Register Protect (SRP) bit and Write Protect (WP#) signal allow the device to be put in the Hardware Protected

Mode (HPM). The Write Status Register (WRSR) instruction is not executed once the Hardware Protected Mode (HPM) is entered.

NOTE : In the OTP mode, WRSR command will ignore input data and program OTP_LOCK bit to 1.

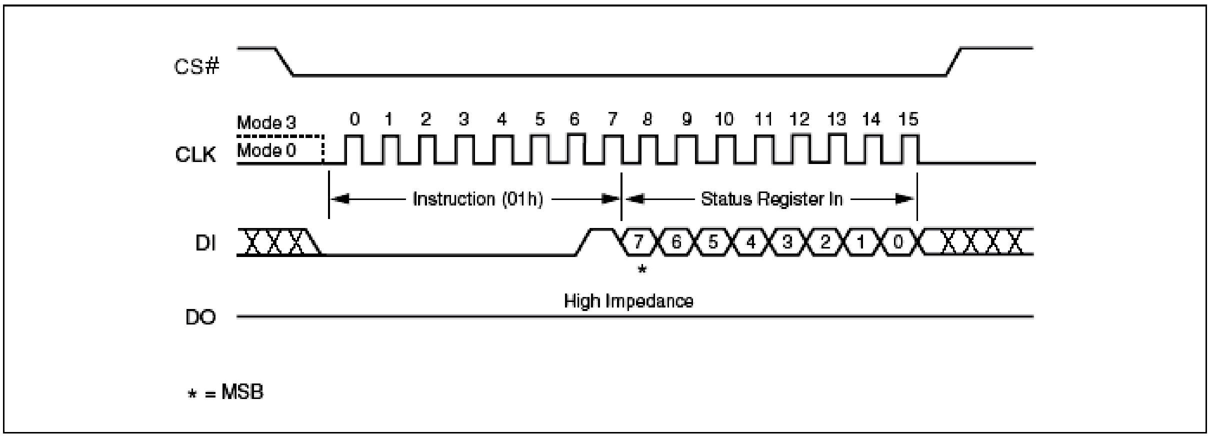


Figure 8. Write Status Register Instruction Sequence Diagram

Read Data Bytes (READ) (03h)

The device is first selected by driving Chip Select (CS#) Low. The instruction code for the Read Data Bytes (READ) instruction is followed by a 3-byte address (A23-A0), each bit being latched-in during the rising edge of Serial Clock (CLK). Then the memory contents, at that address, is shifted out on Serial Data Output (DO), each bit being shifted out, at a maximum frequency f_R, during the falling edge of Serial Clock (CLK).

The instruction sequence is shown in Figure 9. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The whole memory can, therefore, be read with a single Read Data Bytes (READ) instruction. When the highest address is reached, the address counter rolls over to 000000h, allowing the read sequence to be continued indefinitely.

The Read Data Bytes (READ) instruction is terminated by driving Chip Select (CS#) High. Chip Select (CS#) can be driven High at any time during data output. Any Read Data Bytes (READ) instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

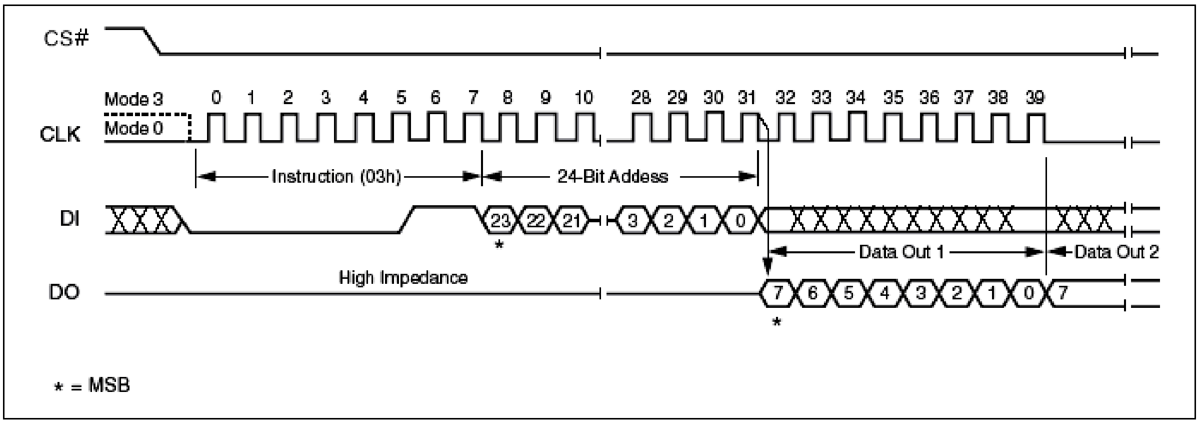


Figure 9. Read Data Instruction Sequence Diagram

Read Data Bytes at Higher Speed (FAST_READ) (0Bh)

The device is first selected by driving Chip Select (CS#) Low. The instruction code for the Read Data Bytes at Higher Speed (FAST_READ) instruction is followed by a 3-byte address (A23-A0) and a dummy byte, each bit being latched-in during the rising edge of Serial Clock (CLK). Then the memory contents, at that address, is shifted out on Serial Data Output (DO), each bit being shifted out, at a maximum frequency F_R, during the falling edge of Serial Clock (CLK).

The instruction sequence is shown in Figure 10. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The whole memory can, therefore, be read with a single Read Data Bytes at Higher Speed (FAST_READ) instruction. When the highest address is reached, the address counter rolls over to 000000h, allowing the read sequence to be continued indefinitely.
The Read Data Bytes at Higher Speed (FAST_READ) instruction is terminated by driving Chip Select (CS#) High. Chip Select (CS#) can be driven High at any time during data output. Any Read Data Bytes at Higher Speed (FAST_READ) instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

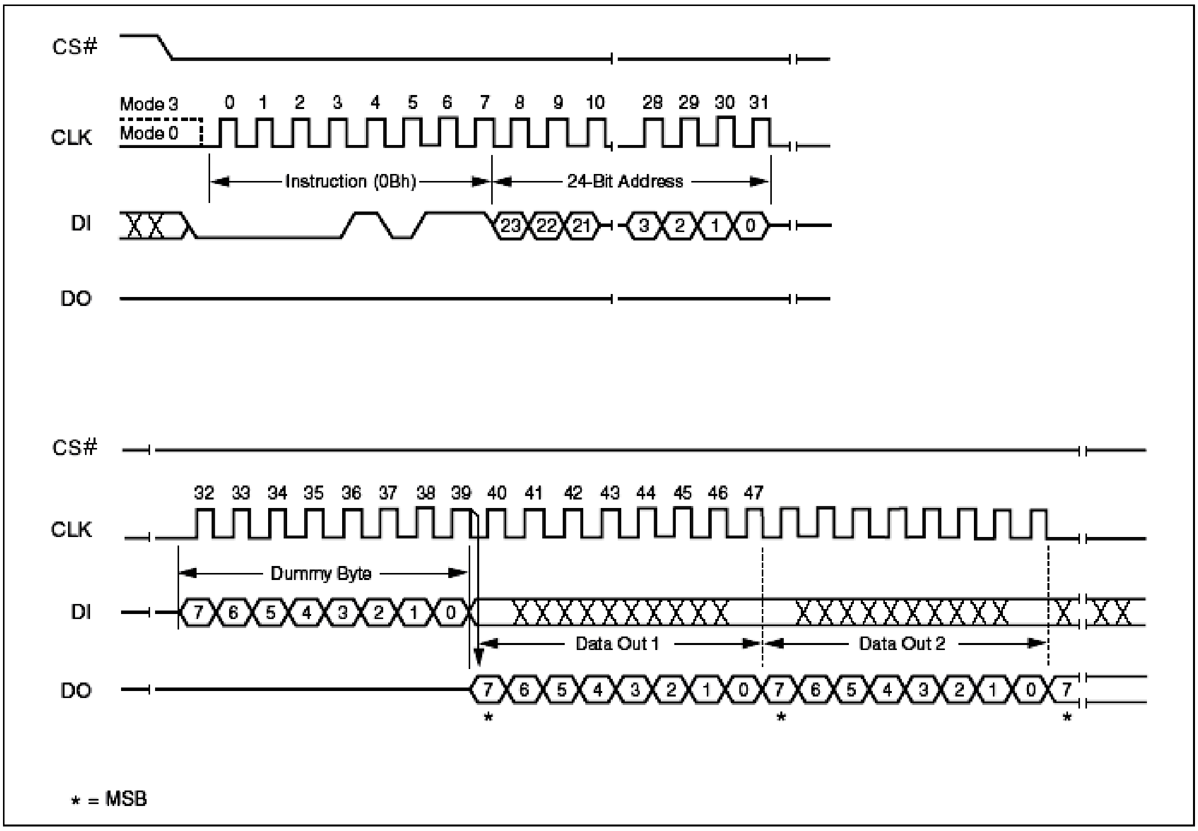


Figure 10. Fast Read Instruction Sequence Diagram

Page Program (PP) (02h)

The Page Program (PP) instruction allows bytes to be programmed in the memory. Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded, the device sets the Write Enable Latch (WEL).

The Page Program (PP) instruction is entered by driving Chip Select (CS#) Low, followed by the instruction code, three address bytes and at least one data byte on Serial Data Input (DI). If the 8 least significant address bits (A7-A0) are not all zero, all transmitted data that goes beyond the end of the current page are programmed from the start address of the same page (from the address whose 8 least significant bits (A7-A0) are all zero). Chip Select (CS#) must be driven Low for the entire duration of the sequence.
The instruction sequence is shown in Figure 11. If more than 256 bytes are sent to the device, previously latched data are discarded and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 Data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page.

Chip Select (CS#) must be driven High after the eighth bit of the last data byte has been latched in, otherwise the Page Program (PP) instruction is not executed.

As soon as Chip Select (CS#) is driven High, the self-timed Page Program cycle (whose duration is t_{PP}) is initiated. While the Page Program cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

A Page Program (PP) instruction applied to a page which is protected by the Block Protect (BP2, BP1, BP0) bits (see Table 3) is not executed.

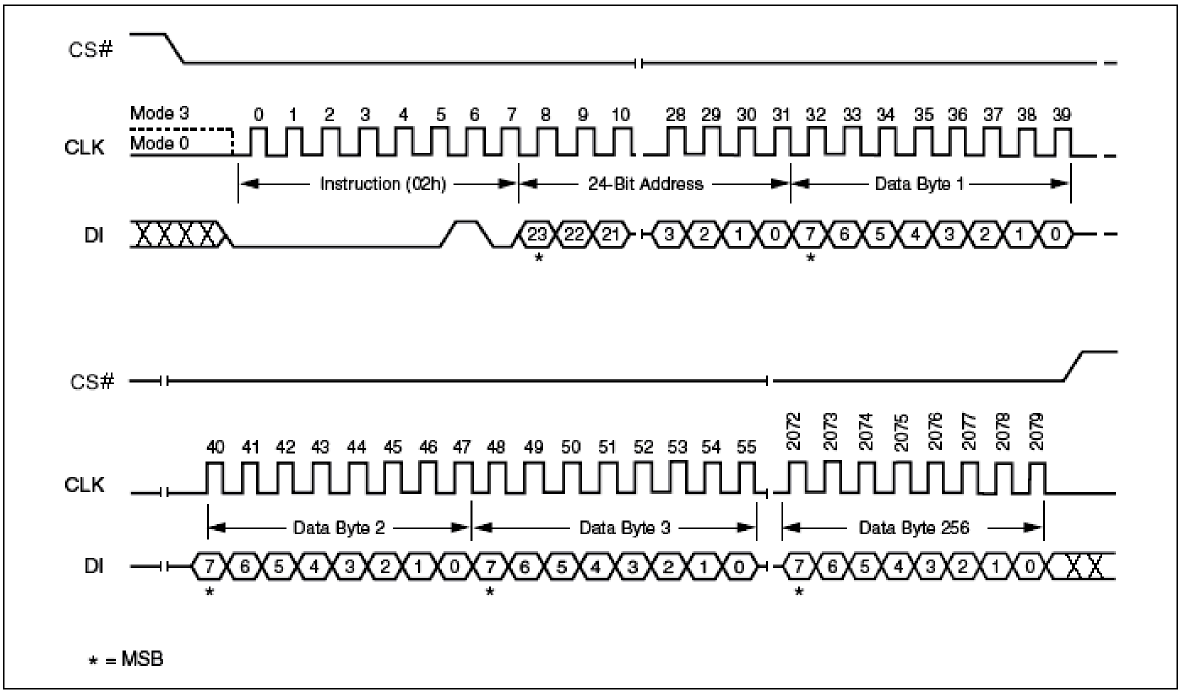


Figure 11. Page Program Instruction Sequence Diagram

Sector Erase (SE) (20h)

The Sector Erase (SE) instruction sets to 1 (FFh) all bits inside the chosen sector. Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded, the device sets the Write Enable Latch (WEL).

The Sector Erase (SE) instruction is entered by driving Chip Select (CS#) Low, followed by the instruction code, and three address bytes on Serial Data Input (DI). Any address inside the Sector (see Table 2) is a valid address for the Sector Erase (SE) instruction. Chip Select (CS#) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in Figure 12. Chip Select (CS#) must be driven High after the eighth bit of the last address byte has been latched in, otherwise the Sector Erase (SE) instruction is not executed. As soon as Chip Select (CS#) is driven High, the self-timed Sector Erase cycle (whose duration is t_{SE}) is initiated. While the Sector Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Sector Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

A Sector Erase (SE) instruction applied to a sector which is protected by the Block Protect (BP2, BP1, BP0) bits (see Table 3) is not executed.

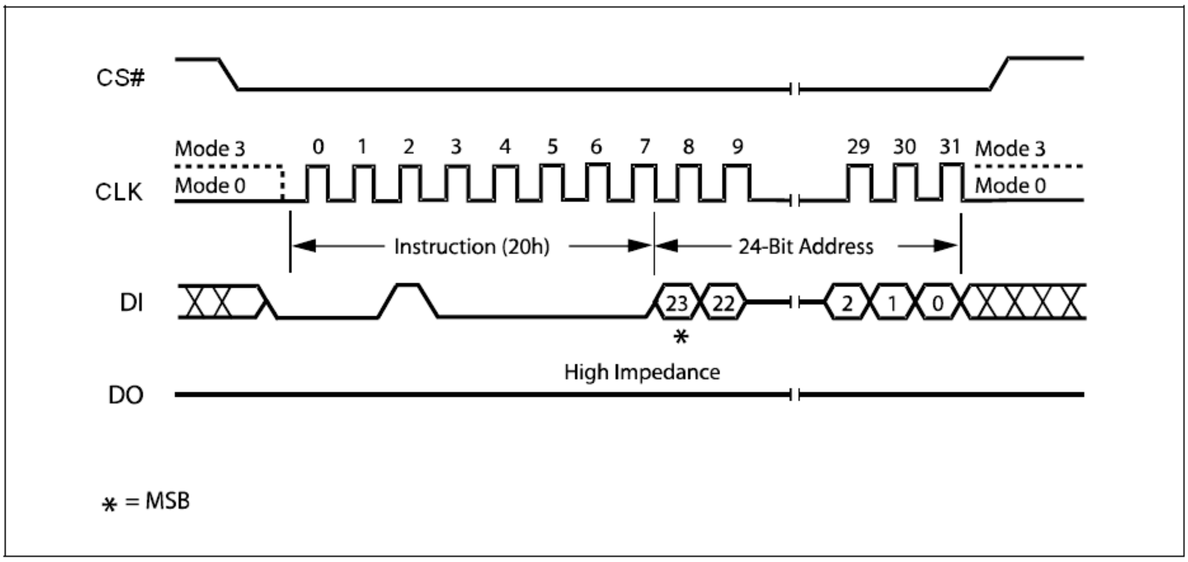


Figure 12. Sector Erase Instruction Sequence Diagram

Block Erase (BE) (D8h/52h)

The Block Erase (BE) instruction sets to 1 (FFh) all bits inside the chosen block. Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded, the device sets the Write Enable Latch (WEL).

The Block Erase (BE) instruction is entered by driving Chip Select (CS#) Low, followed by the instruction code, and three address bytes on Serial Data Input (DI). Any address inside the Block (see Table 2) is a valid address for the Block Erase (BE) instruction. Chip Select (CS#) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in Figure 13. Chip Select (CS#) must be driven High after the eighth bit of the last address byte has been latched in, otherwise the Block Erase (BE) instruction is not executed. As soon as Chip Select (CS#) is driven High, the self-timed Block Erase cycle (whose duration is t_{SE}) is initiated. While the Block Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Block Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

A Block Erase (BE) instruction applied to a block which is protected by the Block Protect (BP2, BP1, BP0) bits (see Table 3) is not executed.

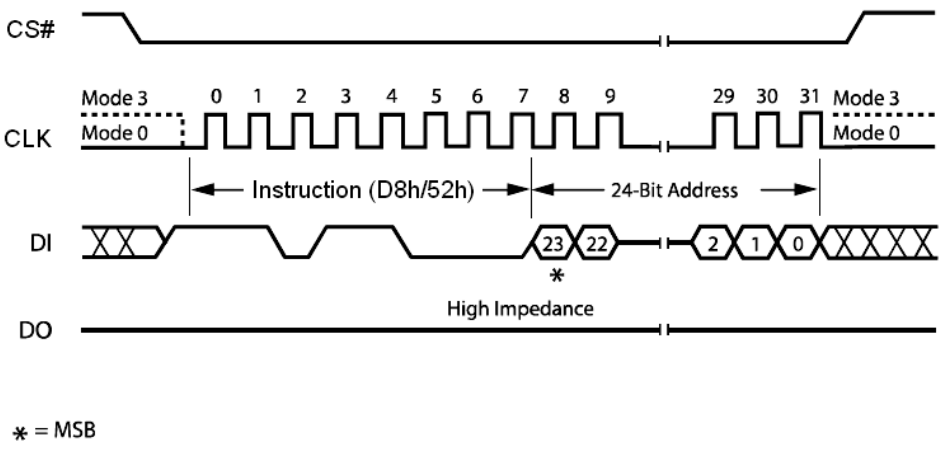


Figure 13 Block Erase Instruction Sequence Diagram

Chip Erase (CE) (C7h/60h)

The Chip Erase (CE) instruction sets all bits to 1 (FFh). Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded, the device sets the Write Enable Latch (WEL).

The Chip Erase (CE) instruction is entered by driving Chip Select (CS#) Low, followed by the instruction code on Serial Data Input (DI). Chip Select (CS#) must be driven Low for the entire duration of the sequence.
The instruction sequence is shown in Figure 14. Chip Select (CS#) must be driven High after the eighth bit of the instruction code has been latched in, otherwise the Chip Erase instruction is not executed. As soon as Chip Select (CS#) is driven High, the self-timed Chip Erase cycle (whose duration is t_{CE}) is initiated. While the Chip Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Chip Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.
The Chip Erase (CE) instruction is executed only if all Block Protect (BP2, BP1, BP0) bits are 0. The Chip Erase (CE) instruction is ignored if one, or more, sectors are protected.

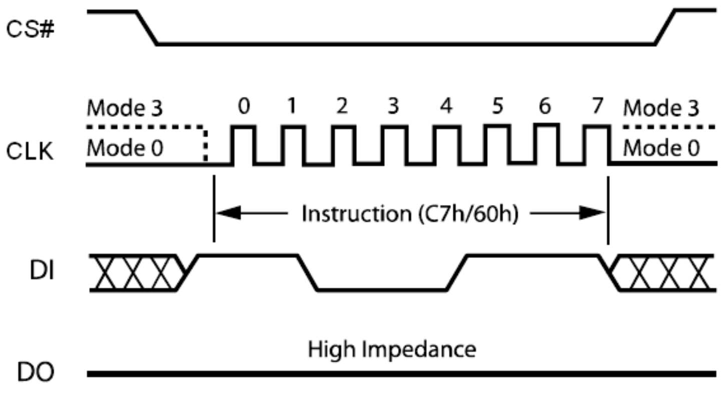


Figure 14. Chip Erase Instruction Sequence Diagram

Deep Power-down (DP) (B9h)

Executing the Deep Power-down (DP) instruction is the only way to put the device in the lowest consumption mode (the Deep Power-down mode). It can also be used as an extra software protection mechanism, while the device is not in active use, since in this mode, the device ignores all Write, Program and Erase instructions.

Driving Chip Select (CS#) High deselects the device, and puts the device in the Standby mode (if there is no internal cycle currently in progress). But this mode is not the Deep Power-down mode. The Deep Power-down mode can only be entered by executing the Deep Power-down (DP) instruction, to reduce the standby current (from ICC1 to ICC2, as specified in Table 9.).

Once the device has entered the Deep Power-down mode, all instructions are ignored except the Release from Deep Power-down and Read Device ID (RDI) instruction. This releases the device from this mode. The Release from Deep Power-down and Read Device ID (RDI) instruction also allows the Device ID of the device to be output on Serial Data Output (DO).
The Deep Power-down mode automatically stops at Power-down, and the device always Powers-up in the Standby mode. The Deep Power-down (DP) instruction is entered by driving Chip Select (CS#) Low, followed by the instruction code on Serial Data Input (DI). Chip Select (CS#) must be driven Low for the entire duration of the sequence.
The instruction sequence is shown in Figure 15.Chip Select (CS#) must be driven High after the eighth bit of the instruction code has been latched in, otherwise the Deep Power-down (DP) instruction is not executed. As soon as Chip Select (CS#) is driven High, it requires a delay of t_{DP} before the supply current is reduced to ICC2 and the Deep Power-down mode is entered.
Any Deep Power-down (DP) instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

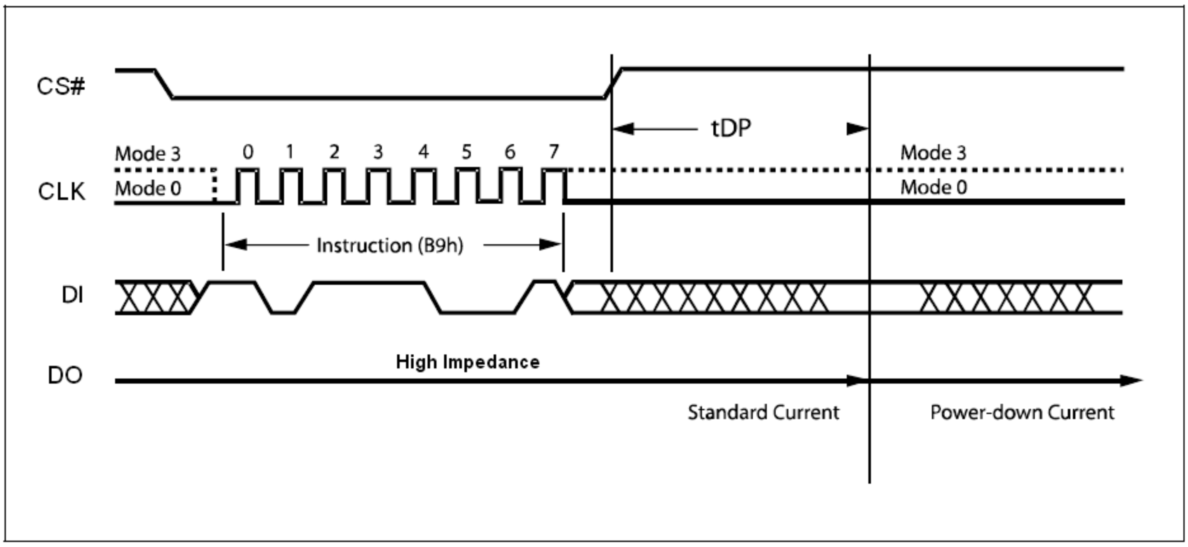


Figure 15. Deep Power-down Instruction Sequence Diagram

Release from Deep Power-down and Read Device ID (RDI)

Once the device has entered the Deep Power-down mode, all instructions are ignored except the Release from Deep Power-down and Read Device ID (RDI) instruction. Executing this instruction takes the device out of the Deep Power-down mode.
Please note that this is not the same as, or even a subset of, the JEDEC 16-bit Electronic Signature that is read by the Read Identifier (RDID) instruction. The old-style Electronic Signature is supported for reasons of backward compatibility, only, and should not be used for new designs. New designs should, instead, make use of the JEDEC 16-bit Electronic Signature, and the Read Identifier (RDID) instruction.

When used only to release the device from the power-down state, the instruction is issued by driving the CS# pin low, shifting the instruction code “ABh” and driving CS# high as shown in Figure 16. After the time duration of t_{RES1} (See AC Characteristics) the device will resume normal operation and other instructions will be accepted. The CS# pin must remain high during the t_{RES1} time duration.

When used only to obtain the Device ID while not in the power-down state, the instruction is initiated by driving the CS# pin low and shifting the instruction code "ABh" followed by 3-dummy bytes. The Device ID bits are then shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in Figure 17. The Device ID value for the EN25F16 are listed in Table 5. The Device ID can be read continuously. The instruction is completed by driving CS# high.

When Chip Select (CS#) is driven High, the device is put in the Stand-by Power mode. If the device was not previously in the Deep Power-down mode, the transition to the Stand-by Power mode is immediate. If the device was previously in the Deep Power-down mode, though, the transition to the Standby Power mode is delayed by t_{RES2}, and Chip Select (CS#) must remain High for at least t_{RES2} (max), as specified in Table 11. Once in the Stand-by Power mode, the device waits to be selected, so that it can receive, decode and execute instructions.

Except while an Erase, Program or Write Status Register cycle is in progress, the Release from Deep Power-down and Read Device ID (RDI) instruction always provides access to the 8bit Device ID of the device, and can be applied even if the Deep Power-down mode has not been entered.

Any Release from Deep Power-down and Read Device ID (RDI) instruction while an Erase, Program or Write Status Register cycle is in progress, is not decoded, and has no effect on the cycle that is in progress.

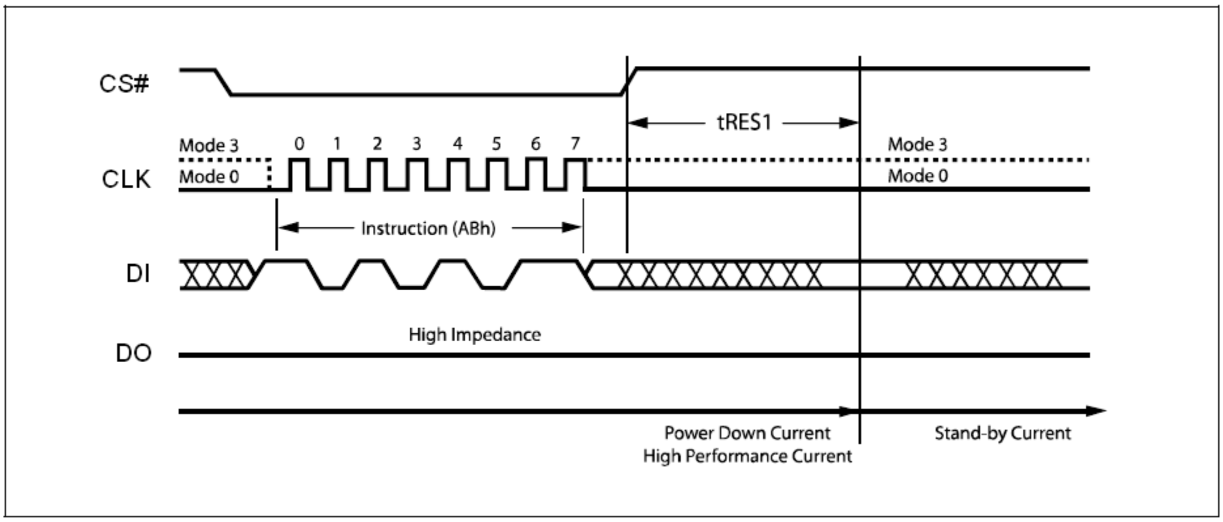


Figure 16. Release Power-down Instruction Sequence Diagram

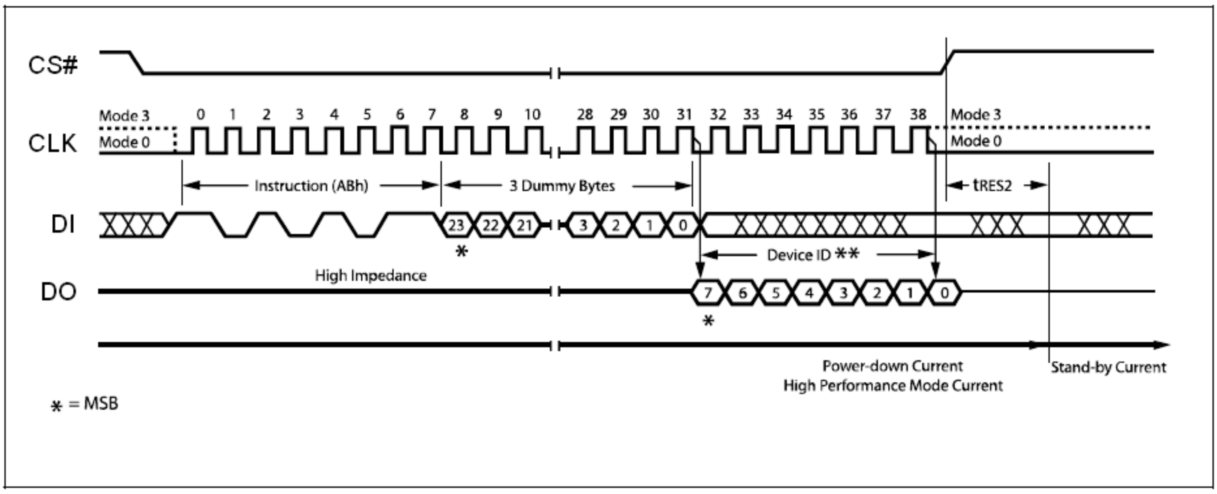


Figure 17. Release Power-down / Device ID Instruction Sequence Diagram

Read Manufacturer / Device ID (90h)

The Read Manufacturer/Device ID instruction is an alternative to the Release from Power-down / Device ID instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID.
The Read Manufacturer/Device ID instruction is very similar to the Release from Power-down / Device ID instruction. The instruction is initiated by driving the CS# pin low and shifting the instruction code "90h" followed by a 24-bit address (A23-A0) of 000000h. After which, the Manufacturer ID for Eon (1Ch) and the Device ID are shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in Figure 18. The Device ID values for the EN25F16 are listed in Table 5. If the 24-bit address is initially set to 000001h the Device ID will be read first

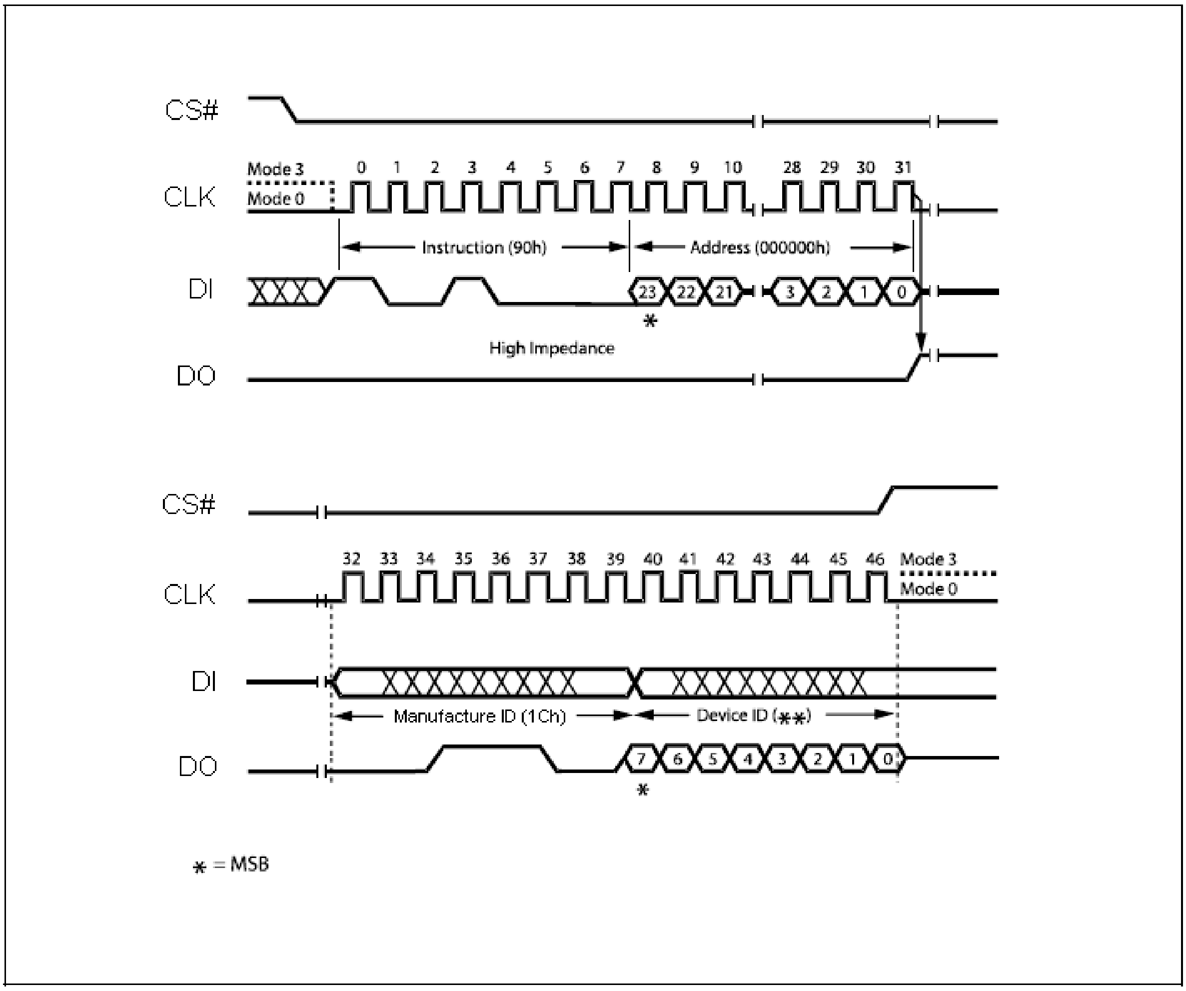


Figure 18. Read Manufacturer / Device ID Diagram

Read Identification (RDID)(9Fh)

The Read Identification (RDID) instruction allows the 8-bit manufacturer identification to be read, followed by two bytes of device identification. The device identification indicates the memory type in the first byte , and the memory capacity of the device in the second byte .
Any Read Identification (RDID) instruction while an Erase or Program cycle is in progress, is not decoded, and has no effect on the cycle that is in progress. The Read Identification (RDID) instruction should not be issued while the device is in Deep Power down mode.
The device is first selected by driving Chip Select Low. Then, the 8-bit instruction code for the instruction is shifted in. This is followed by the 24-bit device identification, stored in the memory, being shifted out on Serial Data Output, each bit being shifted out during the falling edge of Serial Clock. The

instruction sequence is shown in Figure 19. The Read Identification (RDID) instruction is terminated by driving Chip Select High at any time during data output.

When Chip Select is driven High, the device is put in the Standby Power mode. Once in the Standby Power mode, the device waits to be selected, so that it can receive, decode and execute instructions.

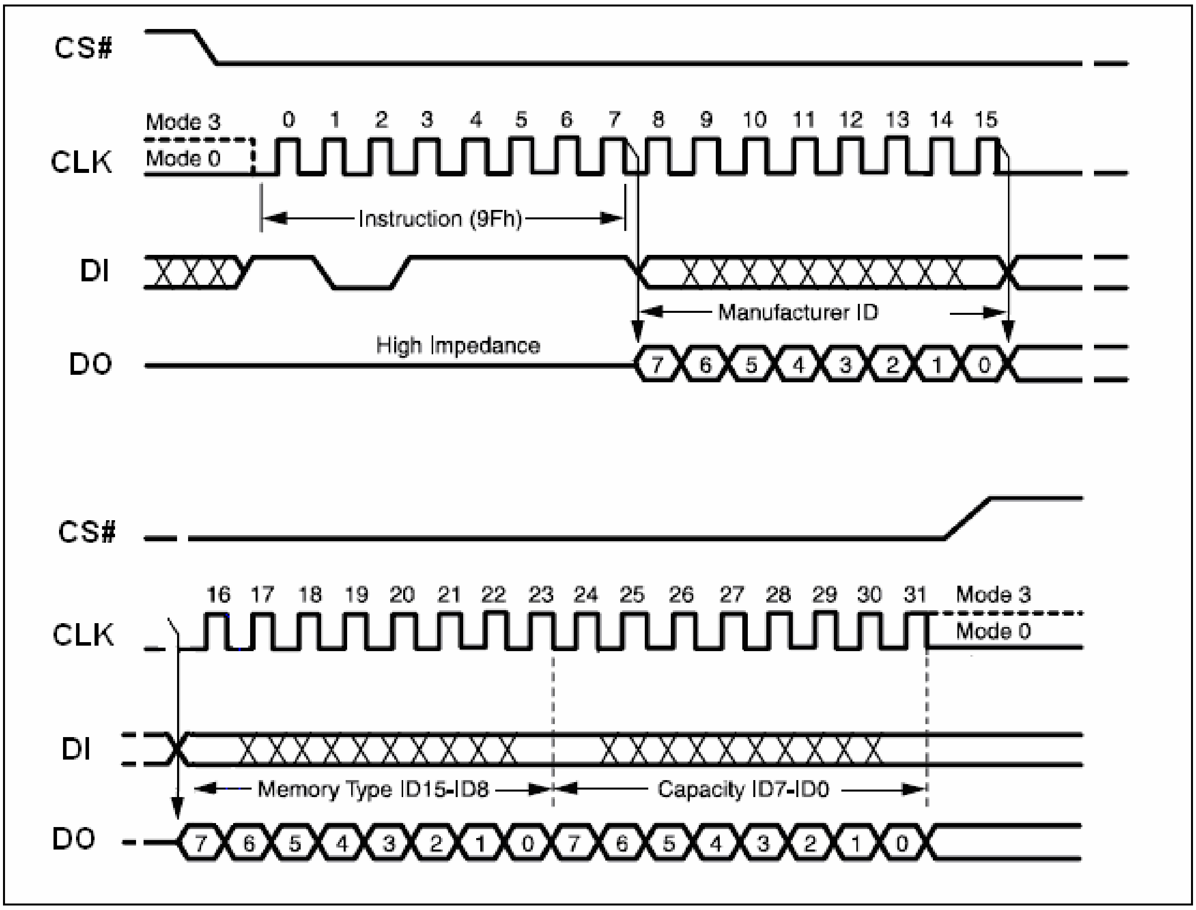


Figure 19. Read Identification (RDID)

Enter OTP Mode (3Ah)

This Flash has an extra 128 bytes OTP sector, user must issue ENTER OTP MODE command to read, program or erase OTP sector. After entering OTP mode, the OTP sector is mapping to sector 511, **SRP bit** becomes OTP_LOCK bit and can be read with RDSR command. Program / Erase command will be disabled when OTP_LOCK is ‘1’

WRSR command will ignore the input data and program LOCK_BIT to 1.
User must clear the protect bits before enter OTP mode.
OTP sector can only be program and erase when LOCK_BIT equal ‘0’ and BP [2:0] = ‘000’. In OTP mode, user can read other sectors, but program/erase other sectors only allowed when OTP_LOCK equal ‘0’.
User can use WRDI (04h) command to exit OTP mode.

Table 7. OTP Sector Address

Sector	Sector Size	Address Range
511	128 byte	1FF000 – 1FF07Fh

Note: The OTP sector is mapping to sector 511

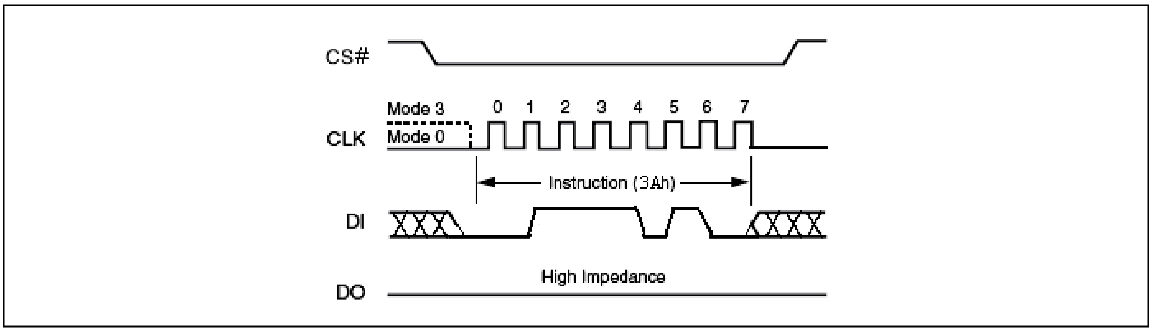


Figure 20. Enter OTP Mode

Power-up Timing

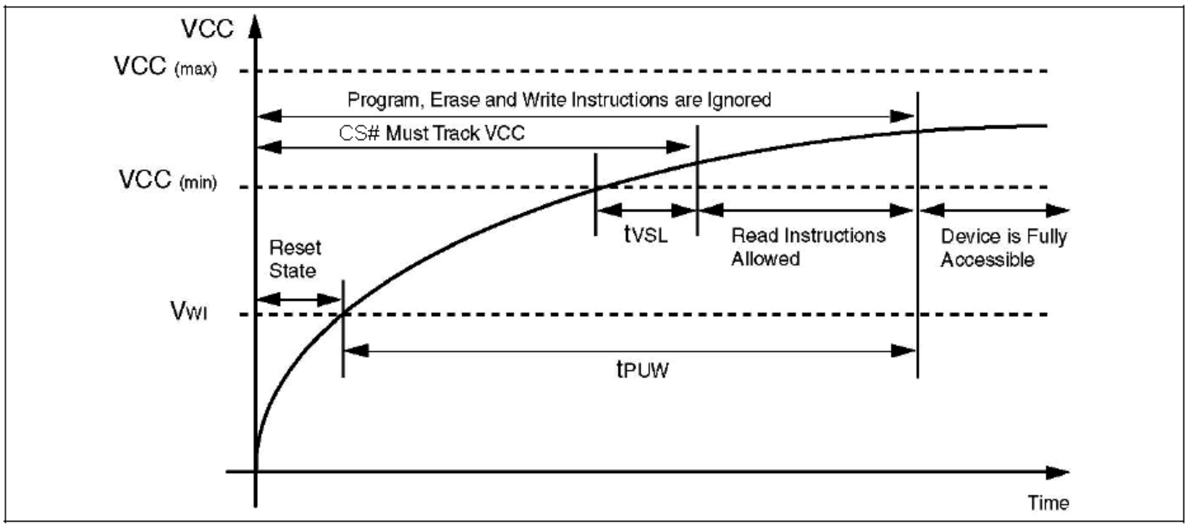


Figure 21. Power-up Timing

Table 8. Power-Up Timing and Write Inhibit Threshold

Symbol	Parameter	Min.	Max.	Unit
t_{VSL}(1)	V_{CC}(min) to CS# low	10		µs
t_{PUW}(1)	Time delay to Write instruction	1	10	ms
VWI(1)	Write Inhibit Voltage	1	2 .5	V

Note:
1.The parameters are characterized only.
2. VCC (max.) is 3.6V and VCC (min.) is 2.7V

INITIAL DELIVERY STATE

The device is delivered with the memory array erased: all bits are set to 1 (each byte contains FFh). The Status Register contains 00h (all Status Register bits are 0).

Table 9. DC Characteristics

(T_a = - 40°C to 85°C; V_{CC} = 2.7-3.6V)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
I_{LI}	Input Leakage Current			± 2	μA
I_{LO}	Output Leakage Current			± 2	μA
I_{CC1}	Standby Current	CS# = V_{CC}, V_{IN} = V_{SS} or V_{CC}		5	μA
I_{CC2}	Deep Power-down Current	CS# = V_{CC}, V_{IN} = V_{SS} or V_{CC}		5	μA
I_{CC3}	Operating Current (READ)	CLK = 0.1 V_{CC} / 0.9 V_{CC} at 100MHz, DQ = open		25	mA
		CLK = 0.1 V_{CC} / 0.9 V_{CC} at 75MHz, DQ = open		20	mA
I_{CC4}	Operating Current (PP)	CS# = V_{CC}		28	mA
I_{CC5}	Operating Current (WRSR)	CS# = V_{CC}		18	mA
I_{CC6}	Operating Current (SE)	CS# = V_{CC}		25	mA
I_{CC7}	Operating Current (BE)	CS# = V_{CC}		25	mA
V_{IL}	Input Low Voltage		– 0.5	0.2 V_{CC}	V
V_{IH}	Input High Voltage		0.7V_{CC}	V_{CC}+0.4	V
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –100 μA	V_{CC}-0.2		V

Table 10. AC Measurement Conditions

Symbol	Parameter	Min.	Max.	Unit
C_L	Load Capacitance	20/30		pF
	Input Rise and Fall Times		5	ns
	Input Pulse Voltages	0.2V_{CC} to 0.8V_{CC}		V
	Input Timing Reference Voltages	0.3V_{CC} to 0.7V_{CC}		V
	Output Timing Reference Voltages	V_{CC} / 2		V

Notes:

1. C_L = 20 pF when CLK=100MHz, C_L = 30 pF when CLK=75MHz,

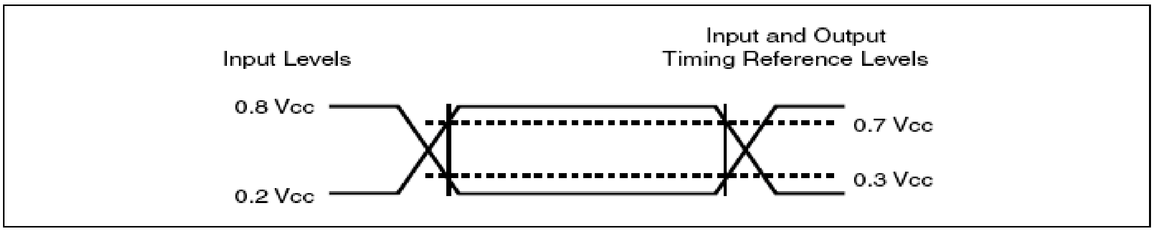


Figure 22. AC Measurement I/O Waveform

Table 11.100MHz AC Characteristics

(T_a = - 40°C to 85°C; V_{CC} = 2.7-3.6V)

Symbol	Alt	Parameter	Min	Typ	Max	Unit
F_R	f_C	Serial Clock Frequency for: FAST_READ, PP, SE, BE, DP, RES, WREN, WRDI, WRSR	D.C.		100	MHz
f_R		Serial Clock Frequency for READ, RDSR, RDID	D.C.		66	MHz
t_{CH} [1]		Serial Clock High Time	4			ns
t_{CL} [1]		Serial Clock Low Time	4			ns
t_{CLCH} [2]		Serial Clock Rise Time (Slew Rate)	0.1			V / ns
t_{CHCL} [2]		Serial Clock Fall Time (Slew Rate)	0.1			V / ns
t_{SLCH}	t_{CSS}	CS# Active Setup Time	5			ns
t_{CHSH}		CS# Active Hold Time	5			ns
t_{SHCH}		CS# Not Active Setup Time	5			ns
t_{CHSL}		CS# Not Active Hold Time	5			ns
t_{SHSL}	t_{CSH}	CS# High Time	100			ns
t_{SHQZ} [2]	t_{DIS}	Output Disable Time			6	ns
t_{CLQX}	t_{HO}	Output Hold Time	0			ns
t_{DVCH}	t_{DSU}	Data In Setup Time	2			ns
t_{CHDX}	t_{DH}	Data In Hold Time	5			ns
t_{HLCH}		HOLD# Low Setup Time (relative to CLK)	5			ns
t_{HHCH}		HOLD# High Setup Time (relative to CLK)	5			ns
t_{CHHH}		HOLD# Low Hold Time (relative to CLK)	5			ns
t_{CHHL}		HOLD# High Hold Time (relative to CLK)	5			ns
t_{HLQZ} [2]	t_{HZ}	HOLD# Low to High-Z Output			6	ns
t_{HHQX} [2]	t_{LZ}	HOLD# High to Low-Z Output			6	ns
t_{CLQV}	t_V	Output Valid from CLK			8	ns
t_{WHSL} [3]		Write Protect Setup Time before CS# Low	20			ns
t_{SHWL} [3]		Write Protect Hold Time after CS# High	100			ns
t_{DP} [2]		CS# High to Deep Power-down Mode			3	µs
t_{RES1} [2]		CS# High to Standby Mode without Electronic Signature read			3	µs
t_{RES2} [2]		CS# High to Standby Mode with Electronic Signature read			1.8	µs
t_W		Write Status Register Cycle Time		10	15	ms
t_{PP}		Page Programming Time		1.3	5	ms
t_{SE}		Sector Erase Time		0.09	0.3	s
t_{BE}		Block Erase Time		0.4	2	s
t_{CE}		Chip Erase Time		7	35	s

Note: 1. $t_{CH} + t_{CL}$ must be greater than or equal to 1/ f_C

2. Value guaranteed by characterization, not 100% tested in production.

3. Only applicable as a constraint for a Write status Register instruction when Status Register Protect Bit is set at 1.

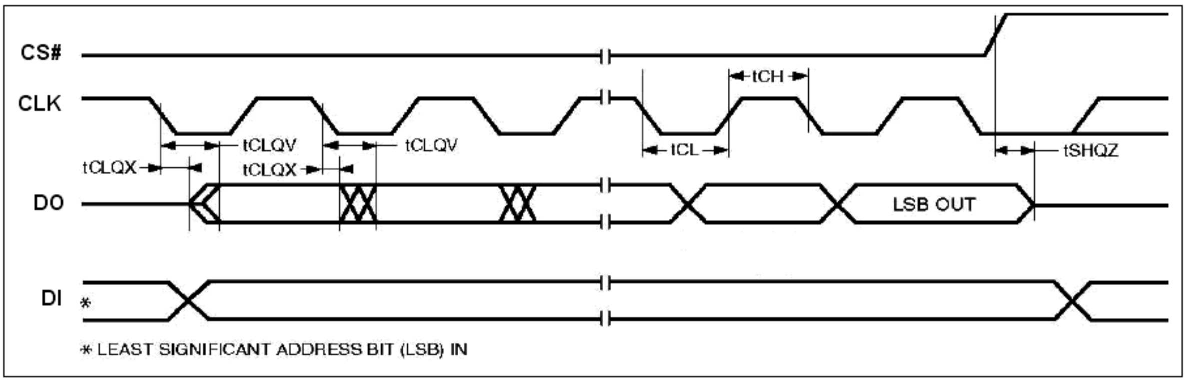


Figure 23. Serial Output Timing

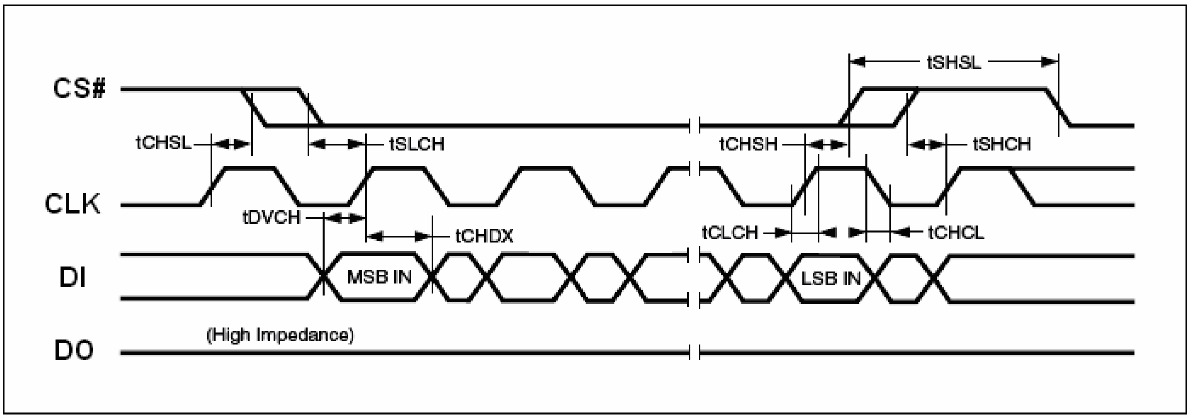


Figure 24. Input Timing

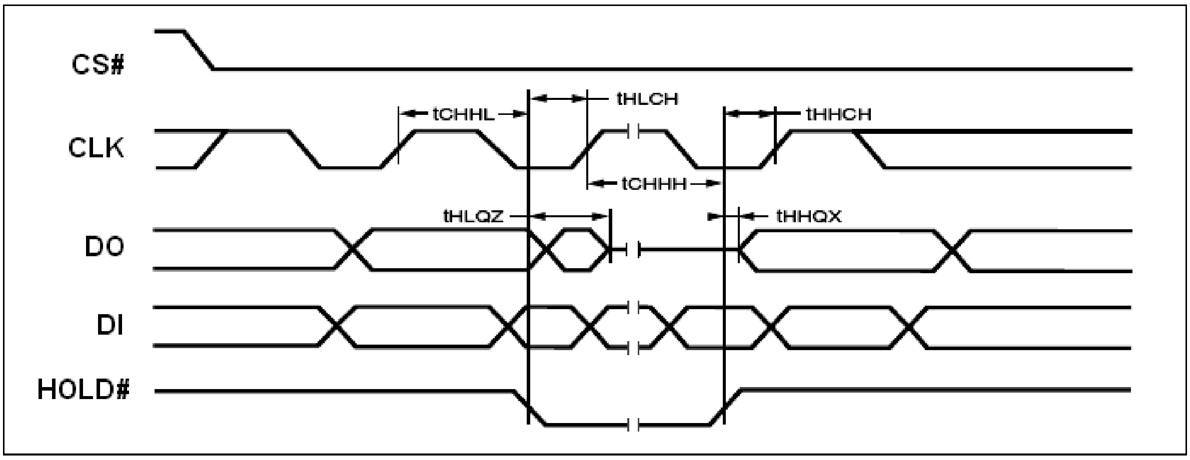


Figure 25. Hold Timing

ABSOLUTE MAXIMUM RATINGS

Stresses above the values so mentioned above may cause permanent damage to the device. These values are for a stress rating only and do not imply that the device should be operated at conditions up to or above these values. Exposure of the device to the maximum rating values for extended periods of time may adversely affect the device reliability.

Parameter	Value	Unit
Storage Temperature	-65 to +150	°C
Plastic Packages	-65 to +125	°C
Output Short Circuit Current[1]	200	mA
Input and Output Voltage (with respect to ground) [2]	-0.5 to +4.0	V
Vcc	-0.5 to +4.0	V

Notes:

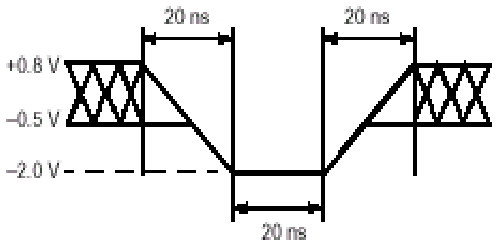
1. No more than one output shorted at a time. Duration of the short circuit should not be greater than one second.
2. Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, inputs may undershoot V_{ss} to –1.0V for periods of up to 50ns and to –2.0 V for periods of up to 20ns. See figure below. Maximum DC voltage on output and I/O pins is V_{cc} + 0.5 V. During voltage transitions, outputs may overshoot to V_{cc} + 1.5 V for periods up to 20ns. See figure below.

RECOMMENDED OPERATING RANGES [1]

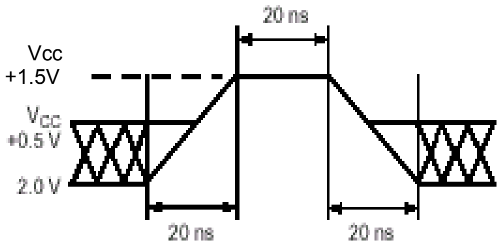
Parameter	Value	Unit
Ambient Operating Temperature Industrial Devices	-40 to 85	°C
Operating Supply Voltage Vcc	Full: 2.7 to 3.6	V

Notes:

1. Recommended Operating Ranges define those limits between which the functionality of the device is guaranteed.



Maximum Negative Overshoot Waveform



Maximum Positive Overshoot Waveform

Table 12. DATA RETENTION and ENDURANCE

Parameter Description	Test Conditions	Min	Unit
Data Retention Time	150°C	10	Years
	125°C	20	Years
Erase/Program Endurance	-40 to 85 °C	100k	cycles

Table 13. CAPACITANCE

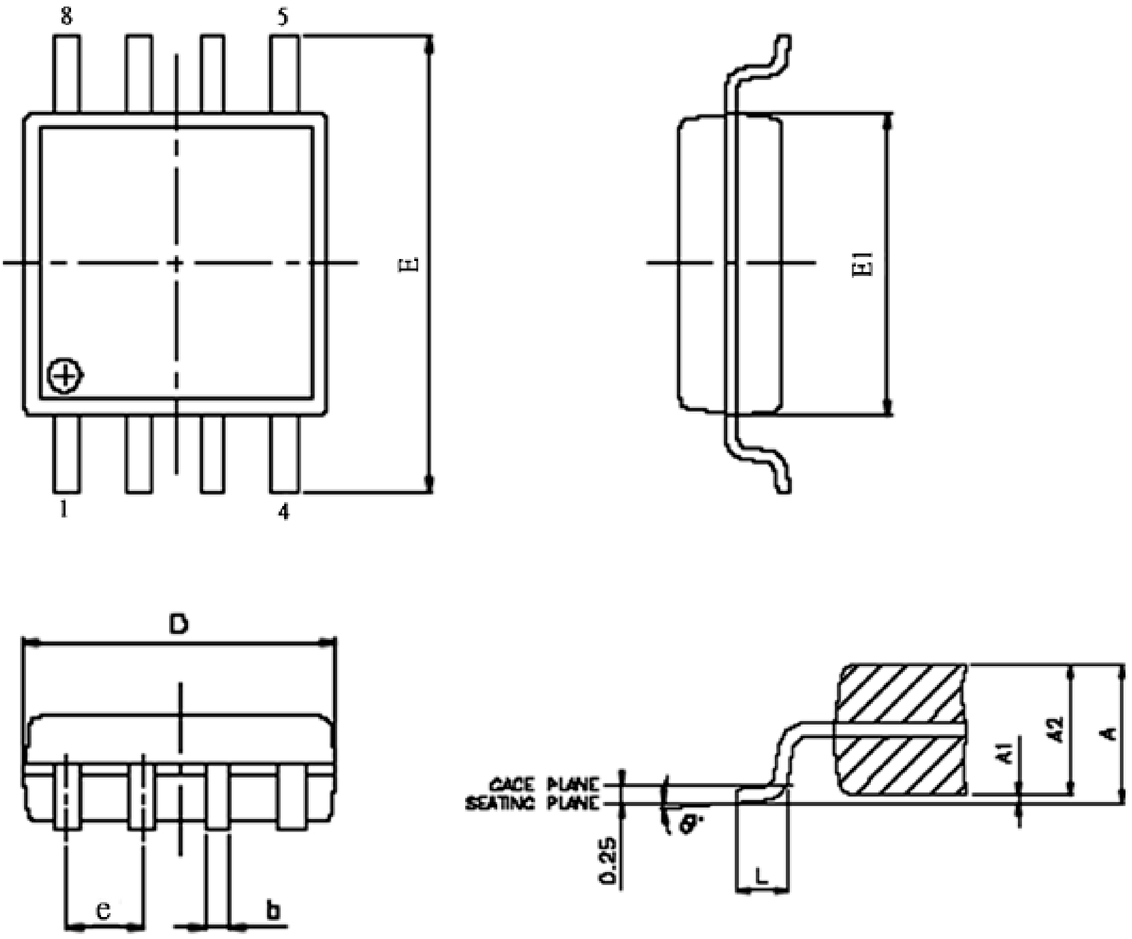
(V_{CC} = 2.7-3.6V)

Parameter Symbol	Parameter Description	Test Setup	Typ	Max	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0$		6	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0$		8	pF

Note : Sampled only, not 100% tested, at T_A = 25°C and a frequency of 20MHz.

PACKAGE MECHANICAL

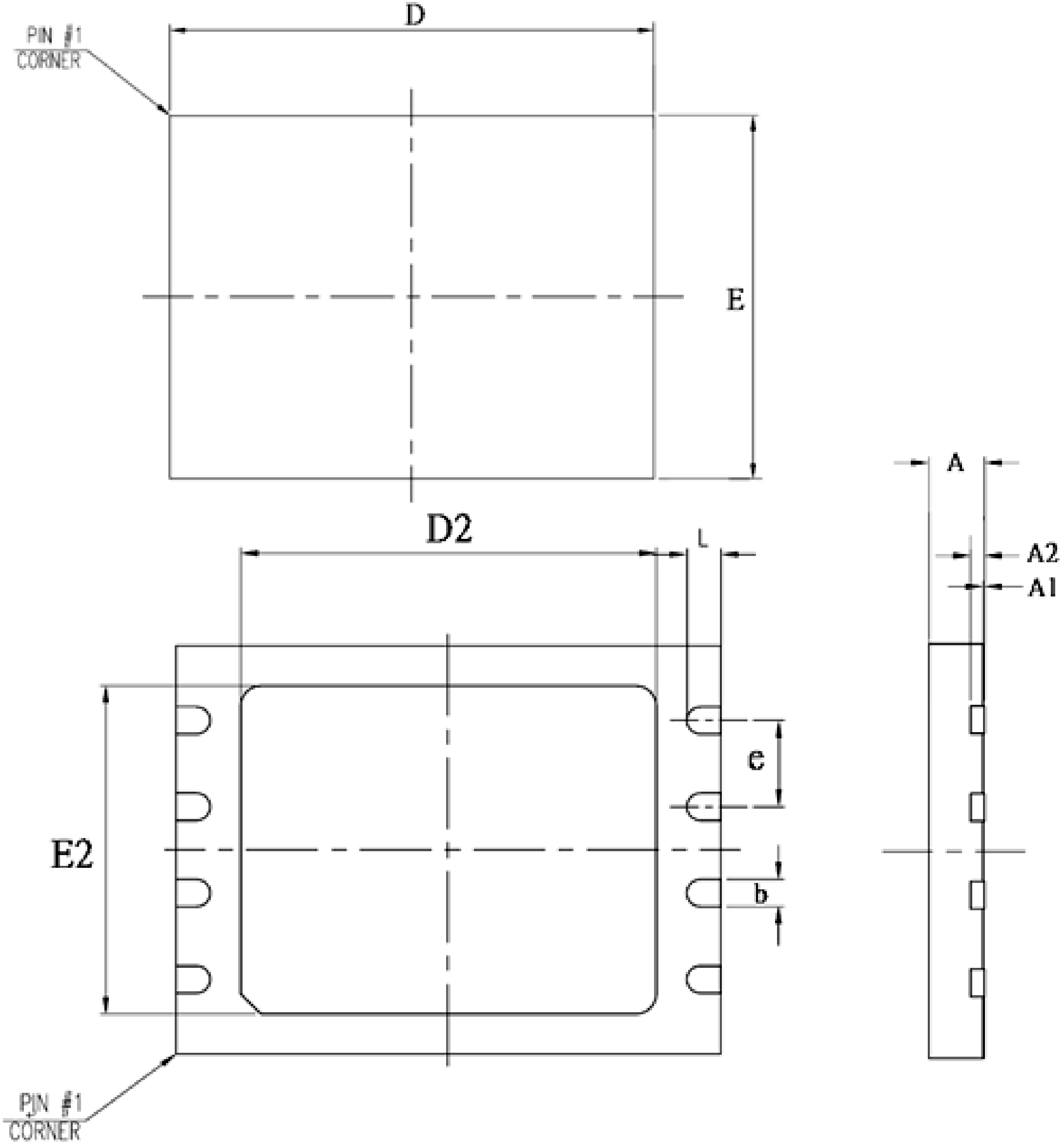
Figure 26. SOP 200 mil (official name = 208 mil)



SYMBOL	DIMENSION IN MM		
	MIN.	NOR	MAX
A	1.75	1.975	2.20
A1	0.05	0.15	0.25
A2	1.70	1.825	1.95
D	5.15	5.275	5.40
E	7.70	7.90	8.10
E1	5.15	5.275	5.40
e	- - -	1.27	- - -
b	0.35	0.425	0.50
L	0.5	0.65	0.80
θ	0^0	4^0	8^0

Note : 1. Coplanarity: 0.1 mm
2. Max. allowable mold flash is 0.15 mm
at the pkg ends, 0.25 mm between leads.

Figure 27. VDFN8 (5x6mm)

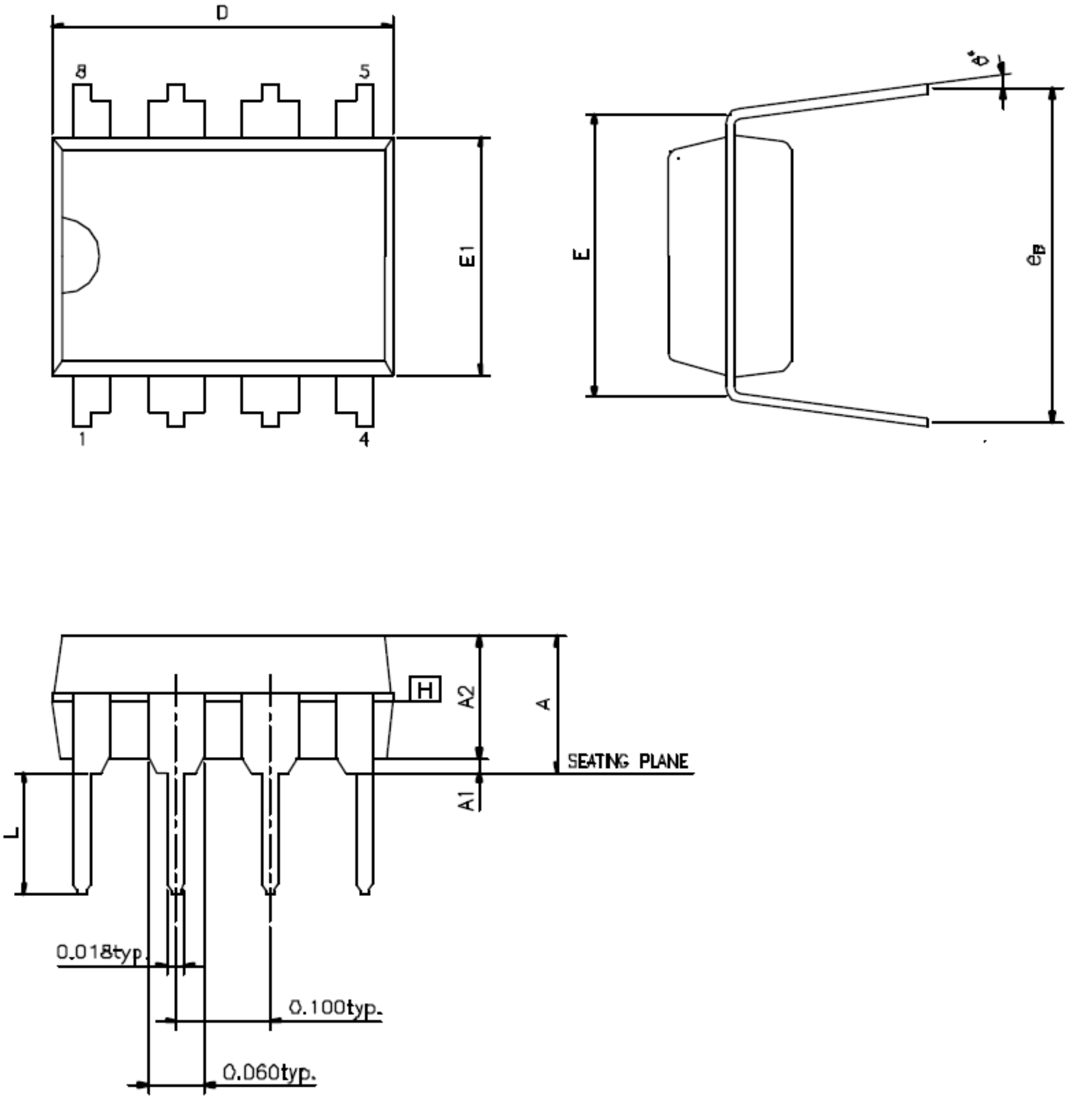


Controlling dimensions are in millimeters (mm).

SYMBOL	DIMENSION IN MM		
	MIN.	NOR	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.04
A2	- - -	0.20	- - -
D	5.90	6.00	6.10
E	4.90	5.00	5.10
D2	3.30	3.40	3.50
E2	3.90	4.00	4.10
e	- - -	1.27	- - -
b	0.35	0.40	0.45
L	0.55	0.60	0.65

Note : 1. Coplanarity: 0.1 mm

Figure 28. PDIP8



SYMBOL	DIMENSION IN INCH		
	MIN.	NOR	MAX
A	- - -	- - -	0.210
A1	0.015	- - -	- - -
A2	0.125	0.130	0.135
D	0.355	0.365	0.400
E	0.300	0.310	0.320
E1	0.245	0.250	0.255
L	0.115	0.130	0.150
e_B	0.310	0.350	0.375
Θ^0	0	7	15

ORDERING INFORMATION

EN25F16 - 100 H I P

PACKAGING CONTENT
(Blank) = Conventional
P = RoHS compliant

TEMPERATURE RANGE
I = Industrial (-40°C to +85°C)

PACKAGE
H = 8-pin 200mil SOP
W = 8-pin VDFN
Q = 8-pin PDIP

SPEED
100 = 100 Mhz

BASE PART NUMBER
EN = Eon Silicon Solution Inc.
25F = 3V Serial 4KByte Uniform-Sector FLASH
16 = 16 Megabit (2048K x 8)

Revisions List

Revision No	Description	Date
A	Preliminary draft	2007/05/02
B	1. Correct the extra OTP sector from 256 bytes to 512 bytes on page 1 and 22. 2. Correct the OTP sector is mapping to sector from 255 to 511 on page 22. 3. Update the Table 6. Status Register Bit Locations on page 12. 4. Modify the Figure 17 on page 20 for the starting point of t_{RES2} 5. Modify the Figure 18 on page 21 (1) revise the manufacture ID to 1Ch (2) the number of clock count to cover the manufacture ID should be 31 to 38 and the last clock to clock out device ID is 46. 6. Modify the Figure 19 in page 22, the clock count to cover the device ID should be from 15 to 31 7. Change Table 10. 100MHz AC Characteristics t_{CLQV} from 6 ns to 8 ns on page 25	2008/03/10
C	Remove C grade option of temperature range on page 1 and page 34	2008/06/23
D	1. Add Eon products' New top marking "cFeon" information on page 1. 2. Add the description "Serial Interface Architecture "and modify active current (typical) from 5mA to 12mA on page 2. 3. List the Note 4 for 90h command in Table 4 on page 12. 4. Update Table 6. Status Register Bit Locations on page 13. 5. Add Table 7. OTP Sector Address on page 23. 6. Add Note " Vcc (max) is 3.6V and Vcc (min) is 2.7V " in Table 8 on page 24. 7. Modify I_{CC3} from "Q = open" to " DQ = open " in Table 9 on page 25 8. Correct the typo "tCLH to tCH" 、 "tCLL to tCL"、"tHHQZ to tHHQX" in Table 11 and Table 12 on page 26 and 27. 9. Modify Storage Temperature from "-65 to + 125" to "-65 to +150" on page 29 10.Delete Latch up Characteristics Table from version C. 11.Modify official name from 209mil to 208mil and delete dimension " c " in Figure 26 on page 31. 12. Modify Figure 28. VDFN8 (5x6mm) dimension A from 0.80 to 0.75 on page 32.	2008/12/18
E	1. Update Page program, Sector erase and Block erase time parameter on page2, 26 and 27. 2. Modify Icc4, Icc5, Icc6 and Icc7 on page 25.	2009/01/20
F	1 Modify Chip erase time (typical) from 18 s to 7s on page 2 and 25 2. Change OTP security sector from 512 byte to 128 byte and update table 7 on page 2 and 22. 3. Remove the Protected Area Sizes definition of BP2、BP1 and BP0 = 001 to 110 in table 3 on page 9. 4. Remove 16 pin SOP 300mil package information from version E 5. Remove speed 75MHz information from version E. 6. Update the VDFN package (D2 from 4.23mm to 3.4mm) on page 30 and 32.	2009/03/16

Revision History

Revision 1.0 (13 Dec. 2001)
- Original

Revision 1.1 (10 Jan. 2002)
- Add -6 spec

Revision 1.2 (30 Jan. 2002)
- Delete Page44 PACKING DIMENSION 54-LEAD TSOP(II) SDRAM (400mil) (1:4).

Revision 1.3 (26 Apr. 2002)
- tRFC : 60ns. (Page5)

Revision 1.4 (21 Oct. 2002)
- Add -5, Delete -8. (P1,4~7)

Revision 1.5 (24 Dec. 2002)
- Delete -5 spec (AC/DC). (page 1,4~7)

Revision 1.6 (13 Feb. 2003)
- Change Icc5 / Icc3p /Icc3ps : Icc5=130mA-->Icc5=180mA / Icc3p=5mA-->Icc3p=10mA / Icc3ps=5mA-->Icc3ps=10mA (page 4)

Revision 1.7 (03 Mar. 2003)
- tRAS = 45ns --> tRAS = 42ns. (page 5,7)

Revision 1.8 (30 Jul. 2003)
- DQM with clock suspended(Full Page Read) needs modified to describe “Full Page”. (page 17)

Revision 1.9 (22 Oct. 2003)
- Modify refresh period. (page 1,13,23,40,41)

Revision 2.0 (17 Dec. 2003)
- Delete “The write burst length is programmed using A9
- Test mode use A7~A8
- Vendor specific options use A9, A10~A11 and A12~BA0

Revision 2.1 (21Jul. 2004)
- Correct typing error→ Page18(tCCD→tCDL), Page22(Note4, Note6), Page23(Note8→Note6), Page29(Note3, Note4)
- Correct plot1.2 clock suspended during read(Page17)
- Correct plot1.2 read interrupted by precharge(Page22)Delete -5 spec (AC/DC). (page 1,4~7)

Revision 2.2 (21 Jan. 2005)
- Add pb-free product number(Page1,7)

Revision 2.3 (17 Mar. 2005)
- Add Pb-free to ordering information
- Modify P8 for bank precharge state to idle state

Revision 2.4 (12 Jul. 2005)
- Rename Pb to Non-Pb-free on ordering info.
- Modify ICC1; ICC2N; ICC3N; 1CC4; ICC5 spec

Revision 2.5 (30 Sep. 2005)
- Add –5T speed grade spec

Revision 2.6 (11 Nov. 2005)
- Modify tCC and tSAC spec
-5T : tCC = 7ns → tCC = 10ns
tSAC = 5ns → tSAC = 6ns
-6T : tCC = 8ns → tCC = 10ns

Revision 2.7 (19Jun. 2006)
- Add BRSW mode

Revision 2.8 (06 Jul. 2006)
- Modify some description for BRSW.

Revision 2.9 (08 Dec. 2006)
- Add BGA type to ordering information

Revision 3.0 (16 Mar. 2007)
- Delete the mark of BGA package in packing diemension

Revision 3.1 (31 Jul. 2007)
- Modify Icc2N test condition (/CS <= VIH ➔ /CS >= VIH)

Revision 3.2 (09 Oct. 2007)
- Modify tSHZ timing

Revision 3.3 (05 May. 2008)
- Add Revision History
- Rename A13, A12 to BA0, BA1
- Delete frequency vs. AC parameter relationship table

SDRAM

1M x 16 Bit x 4 Banks

Synchronous DRAM

FEATURES

- JEDEC standard 3.3V power supply
- LVTTL compatible with multiplexed address
- Four banks operation
- MRS cycle with address key programs
  - CAS Latency (2 & 3)
  - Burst Length (1, 2, 4, 8 & full page)
  - Burst Type (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- DQM for masking
- Auto & self refresh
- 15.6 μs refresh interval

ORDERING INFORMATION

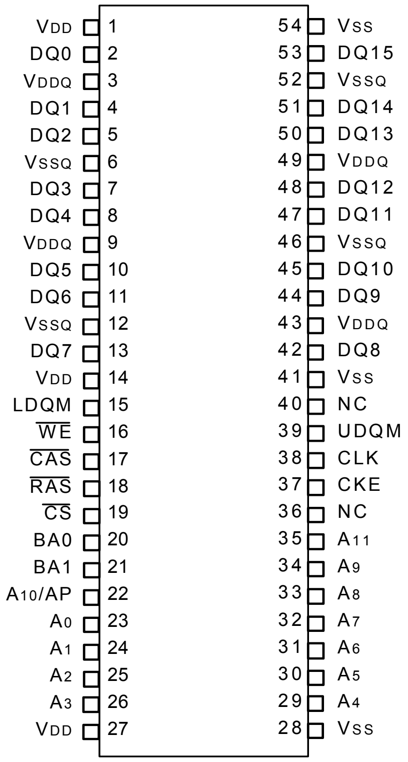
PRODUCT NO.	MAX FREQ.	PACKAGE	Comments
M12L64164A-5TG	200MHz	54 TSOP II	Pb-free
M12L64164A-6TG	166MHz	54 TSOP II	Pb-free
M12L64164A-7TG	143MHz	54 TSOP II	Pb-free
M12L64164A-5BG	200MHz	54 VBGA	Pb-free
M12L64164A-6BG	166MHz	54 VBGA	Pb-free
M12L64164A-7BG	143MHz	54 VBGA	Pb-free

GENERAL DESCRIPTION

The M12L64164A is 67,108,864 bits synchronous high data rate Dynamic RAM organized as 4 x 1,048,576 words by 16 bits. Synchronous design allows precise cycle controls with the use of system clock I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable burst length and programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

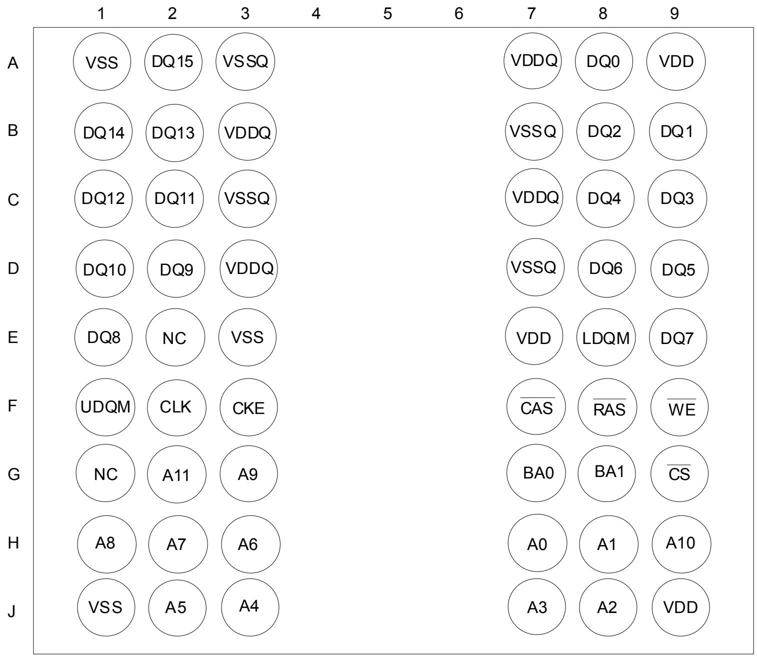
PIN ASSIGNMENT

Top View



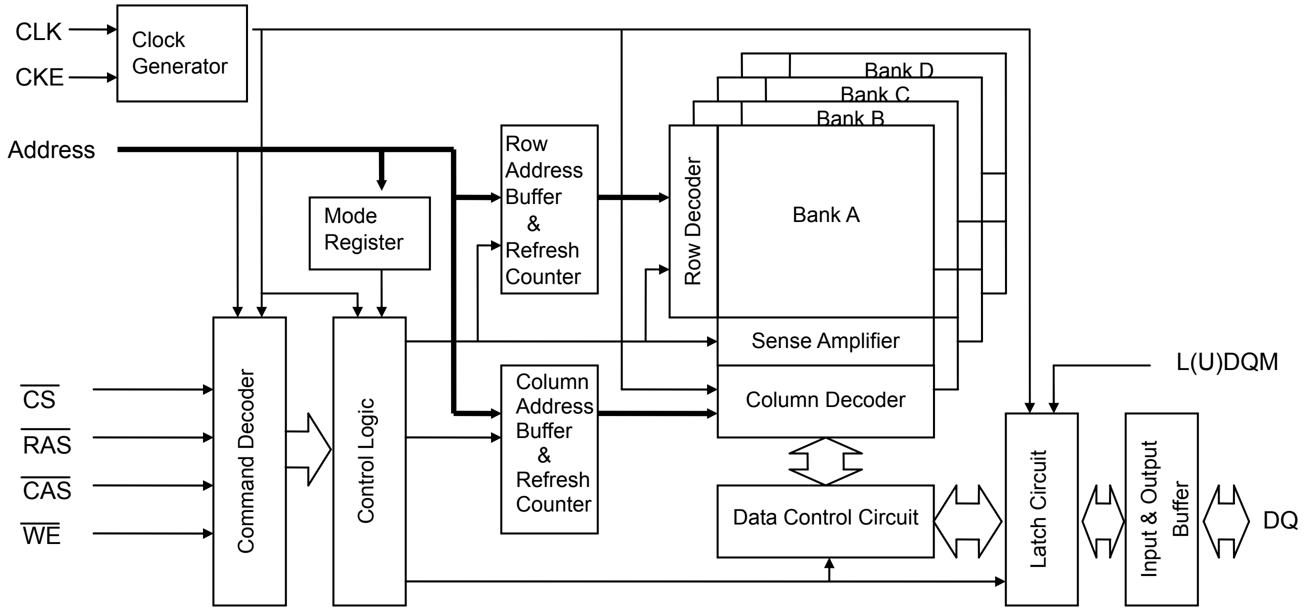
VDD	1	54	Vss
DQ0	2	53	DQ15
VDDQ	3	52	VSSQ
DQ1	4	51	DQ14
DQ2	5	50	DQ13
VSSQ	6	49	VDDQ
DQ3	7	48	DQ12
DQ4	8	47	DQ11
VDDQ	9	46	VSSQ
DQ5	10	45	DQ10
DQ6	11	44	DQ9
VSSQ	12	43	VDDQ
DQ7	13	42	DQ8
VDD	14	41	Vss
LDQM	15	40	NC
$\overline{WE}$	16	39	UDQM
$\overline{CAS}$	17	38	CLK
$\overline{RAS}$	18	37	CKE
$\overline{CS}$	19	36	NC
BA0	20	35	A11
BA1	21	34	A9
A10/AP	22	33	A8
A0	23	32	A7
A1	24	31	A6
A2	25	30	A5
A3	26	29	A4
VDD	27	28	Vss

54 Ball FVBGA (8mmx8mm)



	1	2	3	4	5	6	7	8	9
A	VSS	DQ15	VSSQ				VDDQ	DQ0	VDD
B	DQ14	DQ13	VDDQ				VSSQ	DQ2	DQ1
C	DQ12	DQ11	VSSQ				VDDQ	DQ4	DQ3
D	DQ10	DQ9	VDDQ				VSSQ	DQ6	DQ5
E	DQ8	NC	VSS				VDD	LDQM	DQ7
F	UDQM	CLK	CKE				$\overline{CAS}$	$\overline{RAS}$	$\overline{WE}$
G	NC	A11	A9				BA0	BA1	$\overline{CS}$
H	A8	A7	A6				A0	A1	A10
J	VSS	A5	A4				A3	A2	VDD

FUNCTIONAL BLOCK DIAGRAM



PIN FUNCTION DESCRIPTION

PIN	NAME	INPUT FUNCTION
CLK	System Clock	Active on the positive going edge to sample all inputs
$\overline{\text{CS}}$	Chip Select	Disables or enables device operation by masking or enabling all inputs except CLK , CKE and L(U)DQM
CKE	Clock Enable	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior new command. Disable input buffers for power down in standby.
A0 ~ A11	Address	Row / column address are multiplexed on the same pins. Row address : RA0~RA11, column address : CA0~CA7
BA1 , BA0	Bank Select Address	Selects bank to be activated during row address latch time. Selects bank for read / write during column address latch time.
$\overline{\text{RAS}}$	Row Address Strobe	Latches row addresses on the positive going edge of the CLK with $\overline{\text{RAS}}$ low. Enables row access & precharge.
$\overline{\text{CAS}}$	Column Address Strobe	Latches column address on the positive going edge of the CLK with $\overline{\text{CAS}}$ low. Enables column access.
$\overline{\text{WE}}$	Write Enable	Enables write operation and row precharge. Latches data in starting from $\overline{\text{CAS}}$, $\overline{\text{WE}}$ active.
L(U)DQM	Data Input / Output Mask	Makes data output Hi-Z, t_{SHZ} after the clock and masks the output. Blocks data input when L(U)DQM active.
DQ0 ~ DQ15	Data Input / Output	Data inputs / outputs are multiplexed on the same pins.
VDD / VSS	Power Supply / Ground	Power and ground for the input buffers and the core logic.
VDDQ / VSSQ	Data Output Power / Ground	Isolated power supply and ground for the output buffers to provide improved noise immunity.
NC	No Connection	This pin is recommended to be left No Connection on the device.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to V_{SS}	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	1	W
Short circuit current	I_{OS}	50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATING are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITION

Recommended operating conditions (Voltage referenced to VSS = 0V, TA = 0 to 70 °C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	NOTE
Supply voltage	V_{DD}, V_{DDQ}	3.0	3.3	3.6	V	
Input logic high voltage	V_{IH}	2.0		V_{DD}+0.3	V	1
Input logic low voltage	V_{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output logic low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{IL}	-5	-	5	μA	3
Output leakage current	I_{OL}	-5	-	5	μA	4

Note: 1. $V_{IH(max)}$ = 4.6V AC for pulse width $\leq$ 10ns acceptable.
2. $V_{IL(min)}$ = -1.5V AC for pulse width $\leq$ 10ns acceptable.
3. Any input 0V $\leq V_{IN} \leq V_{DD}$ + 0.3V, all other pins are not under test = 0V.
4. D_{out} is disabled , 0V $\leq V_{OUT} \leq V_{DD}$.

CAPACITANCE (VDD = 3.3V, TA = 25 °C , f = 1MHZ)

PARAMETER	SYMBOL	MIN	MAX	UNIT
Input capacitance (A0 ~ A11, BA0 ~ BA1)	C_{IN1}	2	4	pF
Input capacitance (CLK, CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ & L(U)DQM)	C_{IN2}	2	4	pF
Data input/output capacitance (DQ0 ~ DQ15)	C_{OUT}	2	6	pF

DC CHARACTERISTICS

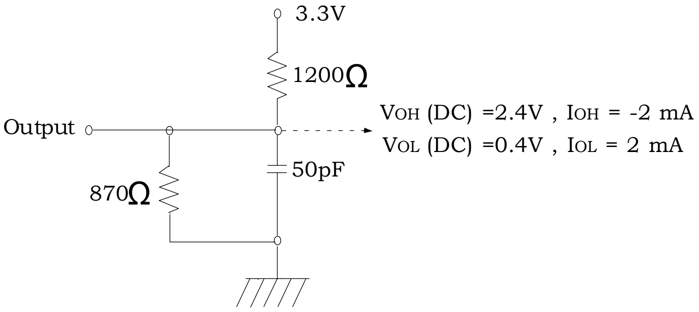
Recommended operating condition unless otherwise noted，TA = 0 to 70 ℃

<table>
<tr><th rowspan="2">PARAMETER</th><th rowspan="2">SYMBOL</th><th rowspan="2">TEST CONDITION</th><th colspan="3">VERSION</th><th rowspan="2">UNIT</th><th rowspan="2">NOTE</th></tr>
<tr><th>-5</th><th>-6</th><th>-7</th></tr>
<tr><td>Operating Current
(One Bank Active)</td><td>I_{CC1}</td><td>Burst Length = 1, $t_{RC} \geq t_{RC(min)}$, I_{OL} = 0 mA,
tcc = tcc(min)</td><td>100</td><td>85</td><td>85</td><td>mA</td><td>1,2</td></tr>
<tr><td rowspan="2">Precharge Standby Current in power-down mode</td><td>I_{CC2P}</td><td>CKE $\leq V_{IL(max)}$, tcc = tcc(min)</td><td colspan="3">2</td><td rowspan="2">mA</td><td rowspan="2"></td></tr>
<tr><td>I_{CC2PS}</td><td>CKE & CLK $\leq V_{IL(max)}$, tcc = ∞</td><td colspan="3">1</td></tr>
<tr><td rowspan="2">Precharge Standby Current in non power-down mode</td><td>I_{CC2N}</td><td>CKE $\geq V_{IH(min)}$, $\overline{CS} \geq V_{IH(min)}$, tcc = tcc(min)
Input signals are changed one time during 2CLK</td><td colspan="3">20</td><td rowspan="2">mA</td><td rowspan="2"></td></tr>
<tr><td>I_{CC2NS}</td><td>CKE $\geq V_{IH(min)}$, CLK $\leq V_{IL(max)}$, tcc = ∞
input signals are stable</td><td colspan="3">10</td></tr>
<tr><td rowspan="2">Active Standby Current in power-down mode</td><td>I_{CC3P}</td><td>CKE $\leq V_{IL(max)}$, tcc = tcc(min)</td><td colspan="3">10</td><td rowspan="2">mA</td><td rowspan="2"></td></tr>
<tr><td>I_{CC3PS}</td><td>CKE & CLK $\leq V_{IL(max)}$, tcc = ∞</td><td colspan="3">10</td></tr>
<tr><td rowspan="2">Active Standby Current in non power-down mode
(One Bank Active)</td><td>I_{CC3N}</td><td>CKE $\geq V_{IH}$(min), $\overline{CS} \geq V_{IH}$(min), t_{CC}=15ns
Input signals are changed one time during 2clks
All other pins ≥ V_{DD}-0.2V or ≤ 0.2V</td><td colspan="3">30</td><td>mA</td><td></td></tr>
<tr><td>I_{CC3NS}</td><td>CKE $\geq V_{IH(min)}$, CLK $\leq V_{IL(max)}$, tcc = ∞
input signals are stable</td><td colspan="3">25</td><td>mA</td><td></td></tr>
<tr><td>Operating Current
(Burst Mode)</td><td>I_{CC4}</td><td>I_{OL} = 0 mA, Page Burst, All Bank active
Burst Length = 4, CAS Latency = 3</td><td>180</td><td>150</td><td>140</td><td>mA</td><td>1,2</td></tr>
<tr><td>Refresh Current</td><td>I_{CC5}</td><td>$t_{RC} \geq t_{RC(min)}$, t_{CC} = tcc(min)</td><td>180</td><td>150</td><td>140</td><td>mA</td><td></td></tr>
<tr><td>Self Refresh Current</td><td>I_{CC6}</td><td>CKE $\leq$ 0.2V</td><td colspan="3">1</td><td>mA</td><td></td></tr>
</table>

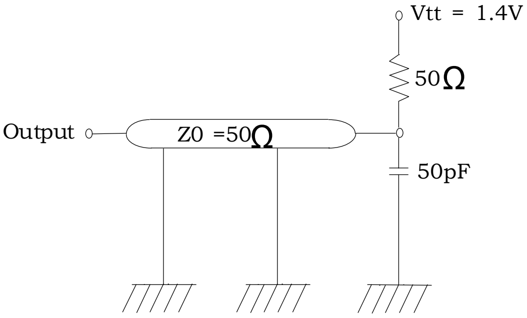
Note : 1. Measured with outputs open.
2. Input signals are changed one time during 2 CLKS.

AC OPERATING TEST CONDITIONS (VDD = 3.3V ± 0.3V ，TA = 0 to 70 °C)

PARAMETER	VALUE	UNIT
Input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall-time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC Output Load Circuit



(Fig. 2) AC Output Load Circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

PARAMETER		SYMBOL	VERSION			UNIT	NOTE
			-5	-6	-7		
Row active to row active delay		$t_{RRD(min)}$	10	12	14	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		$t_{RCD(min)}$	15	18	20	ns	1
Row precharge time		$t_{RP(min)}$	15	18	20	ns	1
Row active time		$t_{RAS(min)}$	38	40	42	ns	1
		$t_{RAS(max)}$	100			us	
Row cycle time	@ Operating	$t_{RC(min)}$	53	58	63	ns	1
	@ Auto refresh	$t_{RFC(min)}$	55	60	70	ns	1,5
Last data in to col. address delay		$t_{CDL(min)}$	1			CLK	2
Last data in to row precharge		$t_{RDL(min)}$	2			CLK	2
Last data in to burst stop		$t_{BDL(min)}$	1			CLK	2
Col. address to col. address delay		$t_{CCD(min)}$	1			CLK	3
Number of valid Output data	CAS latency = 3		2			ea	4
	CAS latency = 2		1				

Note : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete with.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.
5. A new command may be given t_{RFC} after self refresh exit.

AC CHARACTERISTICS (AC operating condition unless otherwise noted)

PARAMATER		SYMBOL	-5		-6		-7		UNIT	NOTE
			MIN	MAX	MIN	MAX	MIN	MAX		
CLK cycle time	CAS latency = 3	t_{CC}	5	1000	6	1000	7	1000	ns	1
	CAS latency = 2		10		10		10			
CLK to valid output delay	CAS latency = 3	t_{SAC}		4.5		5.5		6	ns	1,2
	CAS latency = 2			6		6		6		
Output data hold time	CAS latency = 3	t_{OH}	2.0		2.5		2.5		ns	2
	CAS latency = 2		2.0		2.5		2.5			
CLK high pulsh width		t_{CH}	2.5		2.5		2.5		ns	3
CLK low pulsh width		t_{CL}	2.5		2.5		2.5		ns	3
Input setup time		t_{SS}	1.5		1.5		1.5		ns	3
Input hold time		t_{SH}	1		1		1		ns	3
CLK to output in Low-Z		t_{SLZ}	0		0		0		ns	2
CLK to output in Hi-Z	CAS latency = 3	t_{SHZ}		4.5		5.5		6	ns	-
	CAS latency = 2			6		6		6		

Note :
1. Parameters depend on programmed CAS latency.
2. If clock rising time is longer than 1ns. (tr/2 - 0.5) ns should be considered.
3. Assumed input rise and fall time (tr & tf) =1ns.
   If tr & tf is longer than 1ns. transient time compensation should be considered.
   i.e., [(tr + tf)/2 – 1] ns should be added to the parameter.

SIMPLIFIED TRUTH TABLE

COMMAND			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0 BA1	A10/AP	A11 A9~A0	Note
Register	Mode Register set		H	X	L	L	L	L	X	OP CODE			1,2
Refresh	Auto Refresh		H	H	L	L	L	H	X	X			3
	Self Refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X	X				3
Bank Active & Row Addr.			H	X	L	L	H	H	X	V	Row Address		
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	X	V	L	Column Address (A0~A7)	4
	Auto Precharge Enable										H		4,5
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	X	V	L	Column Address (A0~A7)	4
	Auto Precharge Enable										H		4,5
Burst Stop			H	X	L	H	H	L	X	X			6
Precharge	Bank Selection		H	X	L	L	H	L	X	V	L	X	
	All Banks									X	H		
Clock Suspend or Active Power Down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No Operating Command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V = Valid , X = Don't Care. H = Logic High , L = Logic Low)

Note :
1.OP Code : Operating Code
A0~A11 & BA0, BA1 : Program keys. (@ MRS)
2.MRS can be issued only at all banks precharge state.
A new command can be issued after 2 CLK cycles of MRS.
3.Auto refresh functions are as same as CBR refresh of DRAM.
The automatical precharge without row precharge of command is meant by "Auto".
Auto/self refresh can be issued only at all banks idle state.
4.BA0, BA1 : Bank select addresses.
If both BA0 and BA1 are "Low" at read ,write , row active and precharge ,bank A is selected.
If both BA0 is "Low" and BA1 is "High" at read ,write , row active and precharge ,bank B is selected.
If both BA0 is "High" and BA1 is "Low" at read ,write , row active and precharge ,bank C is selected.
If both BA0 and BA1 are "High" at read ,write , row active and precharge ,bank D is selected
If A10/AP is "High" at row precharge , BA0 and BA1 is ignored and all banks are selected.
5.During burst read or write with auto precharge. new read/write command can not be issued.
Another bank read/write command can be issued after the end of burst.
New row active of the associated bank can be issued at tRP after the end of burst.
6.Burst stop command is valid at every burst length.
7.DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (write DQM latency is 0), but makes Hi-Z state the data-out of 2 CLK cycles after.(Read DQM latency is 2)

MODE REGISTER FIELD TABLE TO PROGRAM MODES

Register Programmed with MRS

Address	BA0, BA1	A11~A10/AP	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Function	RFU	RFU	W.B.L	TM		CAS Latency			BT	Burst Length		

Test Mode		
A8	**A7**	**Type**
0	0	Mode Register Set
0	1	Reserved
1	0	Reserved
1	1	Reserved

Write Burst Length	
A9	Length
0	Burst
1	Single Bit

CAS Latency			
A6	**A5**	**A4**	**Latency**
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2
0	1	1	3
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

Burst Type	
A3	**Type**
0	Sequential
1	Interleave

Burst Length				
A2	**A1**	**A0**	**BT = 0**	**BT = 1**
0	0	0	1	1
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserved	Reserved
1	0	1	Reserved	Reserved
1	1	0	Reserved	Reserved
1	1	1	Full Page	Reserved

Full Page Length : 256

POWER UP SEQUENCE

1.Apply power and start clock, Attempt to maintain CKE = ”H”, DQM = ”H” and the other pin are NOP condition at the inputs.
2. Maintain stable power , stable clock and NOP input condition for a minimum of 200us.
3. Issue precharge commands for all banks of the devices.
4. Issue 2 or more auto-refresh commands.
5. Issue mode register set command to initialize the mode register.
cf.) Sequence of 4 & 5 is regardless of the order.

The device is now ready for normal operation.

Note : 1. RFU(Reserved for future use) should stay “0” during MRS cycle.

2. If A9 is high during MRS cycle, “Burst Read Single Bit Write” function will be enabled.

3. The full column burst (256 bit) is available only at sequential mode of burst type.

BURST SEQUENCE (BURST LENGTH = 4)

Initial Adrress		Sequential				Interleave			
A1	**A0**								
0	0	0	1	2	3	0	1	2	3
0	1	1	2	3	0	1	0	3	2
1	0	2	3	0	1	2	3	0	1
1	1	3	0	1	2	3	2	1	0

BURST SEQUENCE (BURST LENGTH = 8)

Initial			Sequential								Interleave							
A2	**A1**	**A0**																
0	**0**	**0**	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**
0	**0**	**1**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**0**	**1**	**0**	**3**	**2**	**5**	**4**	**7**	**6**
0	**1**	**0**	**2**	**3**	**4**	**5**	**6**	**7**	**0**	**1**	**2**	**3**	**0**	**1**	**6**	**7**	**4**	**5**
0	**1**	**1**	**3**	**4**	**5**	**6**	**7**	**0**	**1**	**2**	**3**	**2**	**1**	**0**	**7**	**6**	**5**	**4**
1	**0**	**0**	**4**	**5**	**6**	**7**	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**0**	**1**	**2**	**3**
1	**0**	**1**	**5**	**6**	**7**	**0**	**1**	**2**	**3**	**4**	**5**	**4**	**7**	**6**	**1**	**0**	**3**	**2**
1	**1**	**0**	**6**	**7**	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**4**	**5**	**2**	**3**	**0**	**1**
1	**1**	**1**	**7**	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**

DEVICE OPERATIONS

CLOCK (CLK)

The clock input is used as the reference for all SDRAM operations. All operations are synchronized to the positive going edge of the clock. The clock transitions must be monotonic between V_{IL} and V_{IH}. During operation with CKE high all inputs are assumed to be in valid state (low or high) for the duration of setup and hold time around positive edge of the clock for proper functionality and Icc specifications.

CLOCK ENABLE(CKE)

The clock enable (CKE) gates the clock onto SDRAM. If CKE goes low synchronously with clock (set-up and hold time same as other inputs), the internal clock suspended from the next clock cycle and the state of output and burst address is frozen as long as the CKE remains low. All other inputs are ignored from the next clock cycle after CKE goes low. When all banks are in the idle state and CKE goes low synchronously with clock, the SDRAM enters the power down mode from the next clock cycle. The SDRAM remains in the power down mode ignoring the other inputs as long as CKE remains low. The power down exit is synchronous as the internal clock is suspended. When CKE goes high at least “1CLK + t_{SS}” before the high going edge of the clock, then the SDRAM becomes active from the same clock edge accepting all the input commands.

BANK ADDRESSES (BA0,BA1)

This SDRAM is organized as four independent banks of 1,048,576 words x 16 bits memory arrays. The BA0 and BA1 inputs are latched at the time of assertion of $\overline{RAS}$ and $\overline{CAS}$ to select the bank to be used for the operation. The banks addressed BA0 and BA1 are latched at bank active, read, write, mode register set and precharge operations.

ADDRESS INPUTS (A0~A11)

The 20 address bits are required to decode the 1,048,576 word locations are multiplexed into 12 address input pins (A0~A11). The 12 row addresses are latched along with $\overline{RAS}$ and BA0,BA1 during bank active command. The 8 bit column addresses are latched along with $\overline{CAS}$, $\overline{WE}$ and BA0,BA1 during read or with command.

NOP and DEVICE DESELECT

When $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ are high, The SDRAM performs no operation (NOP). NOP does not initiate any new operation, but is needed to complete operations which require more than single clock cycle like bank activate, burst read, auto refresh, etc. The device deselect is also a NOP and is entered by asserting $\overline{CS}$ high. $\overline{CS}$ high disables the command decoder so that $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and all the address inputs are ignored.

POWER-UP

1. Apply power and start clock, Attempt to maintain CKE = “H”, DQM = “H” and the other pins are NOP condition at the inputs.
2. Maintain stable power, stable clock and NOP input condition for minimum of 200us.
3. Issue precharge commands for both banks of the devices.
4. Issue 2 or more auto-refresh commands.
5. Issue a mode register set command to initialize the mode register.
   cf.) Sequence of 4 & 5 is regardless of the order.

   The device is now ready for normal operation.

MODE REGISTER SET (MRS)

The mode register stores the data for controlling the various operating modes of SDRAM. It programs the CAS latency, burst type, burst length, test mode and various vendor specific options to make SDRAM useful for variety of different applications. The default value of the mode register is not defined, therefore the mode register must be written after power up to operate the SDRAM. The mode register is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (The SDRAM should be in active mode with CKE already high prior to writing the mode register). The state of address pins A0~A11 and BA0,BA1 in the same cycle as $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ going low is the data written in the mode register. Two clock cycles is required to complete the write in the mode register. The mode register contents can be changed using the same command and clock cycle requirements during operation as long as all banks are in the idle state. The mode register is divided into various fields into depending on functionality. The burst length field uses A0~A2, burst type uses A3, CAS latency (read latency from column address) use A4~A6, vendor specific options or test mode use A7~A8, A10/AP~A11 and BA0,BA1. The write burst length is programmed using A9. A7~A8, A10/AP~A11 and BA0, BA1 must be set to low for normal SDRAM operation. Refer to the table for specific codes for various burst length, burst type and CAS latencies.

DEVICE OPERATIONS (Continued)

BANK ACTIVATE

The bank activate command is used to select a random row in an idle bank. By asserting low on $\overline{RAS}$ and $\overline{CS}$ with desired row and bank address, a row access is initiated. The read or write operation can occur after a time delay of $t_{RCD\ (min)}$ from the time of bank activation. t_{RCD} is the internal timing parameter of SDRAM, therefore it is dependent on operating clock frequency. The minimum number of clock cycles required between bank activate and read or write command should be calculated by dividing $t_{RCD\ (min)}$ with cycle time of the clock and then rounding of the result to the next higher integer. The SDRAM has four internal banks in the same chip and shares part of the internal circuitry to reduce chip area, therefore it restricts the activation of four banks simultaneously. Also the noise generated during sensing of each bank of SDRAM is high requiring some time for power supplies to recover before another bank can be sensed reliably. $t_{RRD\ (min)}$ specifies the minimum time required between activating different bank. The number of clock cycles required between different bank activation must be calculated similar to t_{RCD} specification. The minimum time required for the bank to be active to initiate sensing and restoring the complete row of dynamic cells is determined by $t_{RAS\ (min)}$. Every SDRAM bank activate command must satisfy $t_{RAS\ (min)}$ specification before a precharge command to that active bank can be asserted. The maximum time any bank can be in the active state is determined by $t_{RAS\ (max)}$ and $t_{RAS\ (max)}$ can be calculated similar to t_{RCD} specification.

BURST READ

The burst read command is used to access burst of data on consecutive clock cycles from an active row in an active bank. The burst read command is issued by asserting low on $\overline{CS}$ and $\overline{RAS}$ with $\overline{WE}$ being high on the positive edge of the clock. The bank must be active for at least $t_{RCD\ (min)}$ before the burst read command is issued. The first output appears in CAS latency number of clock cycles after the issue of burst read command. The burst length, burst sequence and latency from the burst read command is determined by the mode register which is already programmed. The burst read can be initiated on any column address of the active row. The address wraps around if the initial address does not start from a boundary such that number of outputs from each I/O are equal to the burst length programmed in the mode register. The output goes into high-impedance at the end of burst, unless a new burst read was initiated to keep the data output gapless. The burst read can be terminated by issuing another burst read or burst write in the same bank or the other active bank or a precharge command to the same bank. The burst stop command is valid at every page burst length.

BURST WRITE

The burst write command is similar to burst read command and is used to write data into the SDRAM on consecutive clock cycles in adjacent addresses depending on burst length and burst sequence. By asserting low on $\overline{CS}$, $\overline{CAS}$ and $\overline{WE}$ with valid column address, a write burst is initiated. The data inputs are provided for the initial address in the same clock cycle as the burst write command. The input buffer is deselected at the end of the burst length, even though the internal writing can be completed yet. The writing can be complete by issuing a burst read and DQM for blocking data inputs or burst write in the same or another active bank. The burst stop command is valid at every burst length. The write burst can also be terminated by using DQM for blocking data and procreating the bank t_{RDL} after the last data input to be written into the active row. See DQM OPERATION also.

DQM OPERATION

The DQM is used mask input and output operations. It works similar to $\overline{OE}$ during operation and inhibits writing during write operation. The read latency is two cycles from DQM and zero cycle for write, which means DQM masking occurs two cycles later in read cycle and occurs in the same cycle during write cycle. DQM operation is synchronous with the clock. The DQM signal is important during burst interrupts of write with read or precharge in the SDRAM. Due to asynchronous nature of the internal write, the DQM operation is critical to avoid unwanted or incomplete writes when the complete burst write is required. Please refer to DQM timing diagram also.

PRECHARGE

The precharge is performed on an active bank by asserting low on clock cycles required between bank activate and clock cycles required between bank activate and $\overline{CS}$, $\overline{RAS}$, $\overline{WE}$ and A10/AP with valid BA0, BA1 of the bank to be procharged. The precharge command can be asserted anytime after $t_{RAS\ (min)}$ is satisfy from the bank active command in the desired bank. t_{RP} is defined as the minimum number of clock cycles required to complete row precharge is calculated by dividing tRP with clock cycle time and rounding up to the next higher integer. Care should be taken to make sure that burst write is completed or DQM is used to inhibit writing before precharge command is asserted. The maximum time any bank can be active is specified by $t_{RAS\ (max)}$. Therefore, each bank activate command. At the end of precharge, the bank enters the idle state and is ready to be activated again. Entry to power-down, Auto refresh, Self refresh and Mode register set etc. is possible only when all banks are in idle state.

DEVICE OPERATIONS (Continued)

AUTO PRECHARGE

The precharge operation can also be performed by using auto precharge. The SDRAM internally generates the timing to satisfy $t_{RAS\ (min)}$ and "t_{RP}" for the programmed burst length and CAS latency. The auto precharge command is issued at the same time as burst write by asserting high on A10/AP, the bank is precharge command is asserted. Once auto precharge command is given, no new commands are possible to that particular bank until the bank achieves idle state.

BOTH BANKS PRECHARGE

Both banks can be precharged at the same time by using Precharge all command. Asserting low on $\overline{CS}$, $\overline{RAS}$, and $\overline{WE}$ with high on A10/AP after all banks have satisfied $t_{RAS\ (min)}$ requirement, performs precharge on all banks. At the end of t_{RP} after performing precharge all, all banks are in idle state.

AUTO REFRESH

The storage cells of SDRAM need to be refreshed every 64ms to maintain data. An auto refresh cycle accomplishes refresh of a single row of storage cells. The internal counter increments automatically on every auto refresh cycle to refresh all the rows. An auto refresh command is issued by asserting low on $\overline{CS}$, $\overline{RAS}$ and $\overline{CAS}$ with high on CKE and $\overline{WE}$. The auto refresh command can only be asserted with both banks being in idle state and the device is not in power down mode (CKE is high in the previous cycle). The time required to complete the auto refresh operation is specified by $t_{RFC\ (min)}$. The minimum number of clock cycles required can be calculated by driving t_{RFC} with clock cycle time and them rounding up to the next higher integer. The auto refresh command must be followed by NOP's until the auto refresh operation is completed. The auto refresh is the preferred refresh mode when the SDRAM is being used for normal data transactions. The auto refresh cycle can be performed once in 15.6us.

SELF REFRESH

The self refresh is another refresh mode available in the SDRAM. The self refresh is the preferred refresh mode for data retention and low power operation of SDRAM. In self refresh mode, the SDRAM disables the internal clock and all the input buffers except CKE. The refresh addressing and timing is internally generated to reduce power consumption. The self refresh mode is entered from all banks idle state by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and CKE with high on $\overline{WE}$. Once the self refresh mode is entered, only CKE state being low matters, all the other inputs including clock are ignored to remain in the refresh.
The self refresh is exited by restarting the external clock and then asserting high on CKE. This must be followed by NOP's for a minimum time of t_{RFC} before the SDRAM reaches idle state to begin normal operation.

COMMANDS

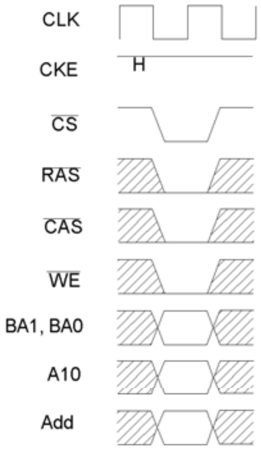


Fig. 1 Mode register set command

Mode register set command

($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ = Low)

The M12L64164A has a mode register that defines how the device operates. In this command, A0 through A11, BA0 and BA1 are the data input pins. After power on, the mode register set command must be executed to initialize the device.

The mode register can be set only when all banks are in idle state. During 2CLK (t_{RSC}) following this command, the M12L64164A cannot accept any other commands.

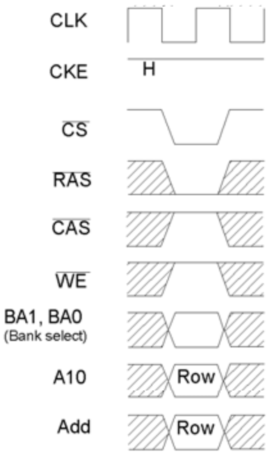


Fig. 2 Row address stroble and bank active command

Activate command

($\overline{CS}$, $\overline{RAS}$ = Low, $\overline{CAS}$, $\overline{WE}$ = High)

The M12L64164A has four banks, each with 4,096 rows.

This command activates the bank selected by BA1 and BA0 (BS) and a row address selected by A0 through A11.

This command corresponds to a conventional DRAM's $\overline{RAS}$ falling.

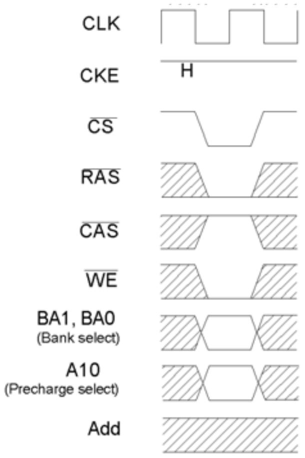


Fig. 3 Precharge command

Precharge command

($\overline{CS}$, $\overline{RAS}$, $\overline{WE}$ = Low, $\overline{CAS}$ = High)

This command begins precharge operation of the bank selected by BA1 and BA0 (BS). When A10 is High, all banks are precharged, regardless of BA1 and BA0. When A10 is Low, only the bank selected by BA1 and BA0 is precharged.

After this command, the M12L64164A can't accept the activate command to the precharging bank during t_{RP} (precharge to activate command period).

This command corresponds to a conventional DRAM's $\overline{RAS}$ rising.

Write command

($\overline{\text{CS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$ = Low, $\overline{\text{RAS}}$ = High)

If the mode register is in the burst write mode, this command sets the burst start address given by the column address to begin the burst write operation. The first write data in burst can be input with this command with subsequent data on following clocks.

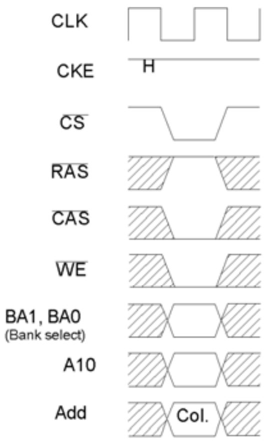


Fig. 4 Column address and write command

Read command

($\overline{\text{CS}}$, $\overline{\text{CAS}}$ = Low, $\overline{\text{RAS}}$, $\overline{\text{WE}}$ = High)

Read data is available after $\overline{\text{CAS}}$ latency requirements have been met.

This command sets the burst start address given by the column address.

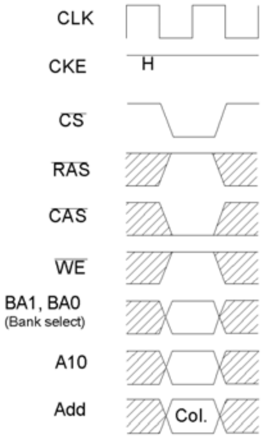


Fig. 5 Column address and read command

CBR (auto) refresh command

($\overline{\text{CS}}$, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ = Low, $\overline{\text{WE}}$, CKE = High)

This command is a request to begin the CBR refresh operation. The refresh address is generated internally.

Before executing CBR refresh, all banks must be precharged.

After this cycle, all banks will be in the idle (precharged) state and ready for a row activate command.

During t_{RC} period (from refresh command to refresh or activate command), the M12L64164A cannot accept any other command.

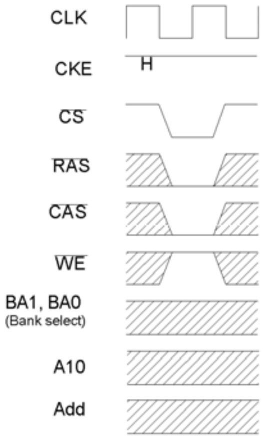


Fig. 6 Auto refresh command

Self refresh entry command

($\overline{\text{CS}}$, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, CKE = Low , $\overline{\text{WE}}$ = High)

After the command execution, self refresh operation continues while CKE remains low. When CKE goes to high, the M12L64164A exits the self refresh mode.

During self refresh mode, refresh interval and refresh operation are performed internally, so there is no need for external control.
Before executing self refresh, all banks must be precharged.

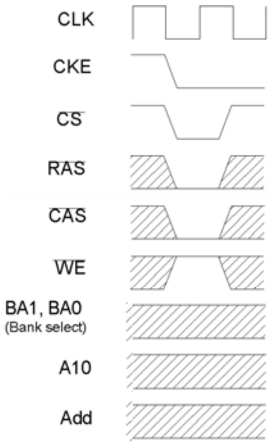


Fig. 7 Self refresh entry command

Burst stop command

($\overline{\text{CS}}$, $\overline{\text{WE}}$ = Low, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ = High)

This command terminates the current burst operation.
Burst stop is valid at every burst length.

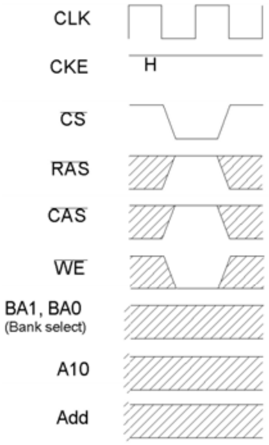


Fig. 8 Burst stop command

No operation

($\overline{\text{CS}}$ = Low , $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$ = High)

This command is not a execution command. No operations begin or terminate by this command.

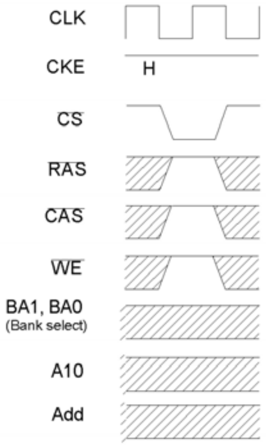
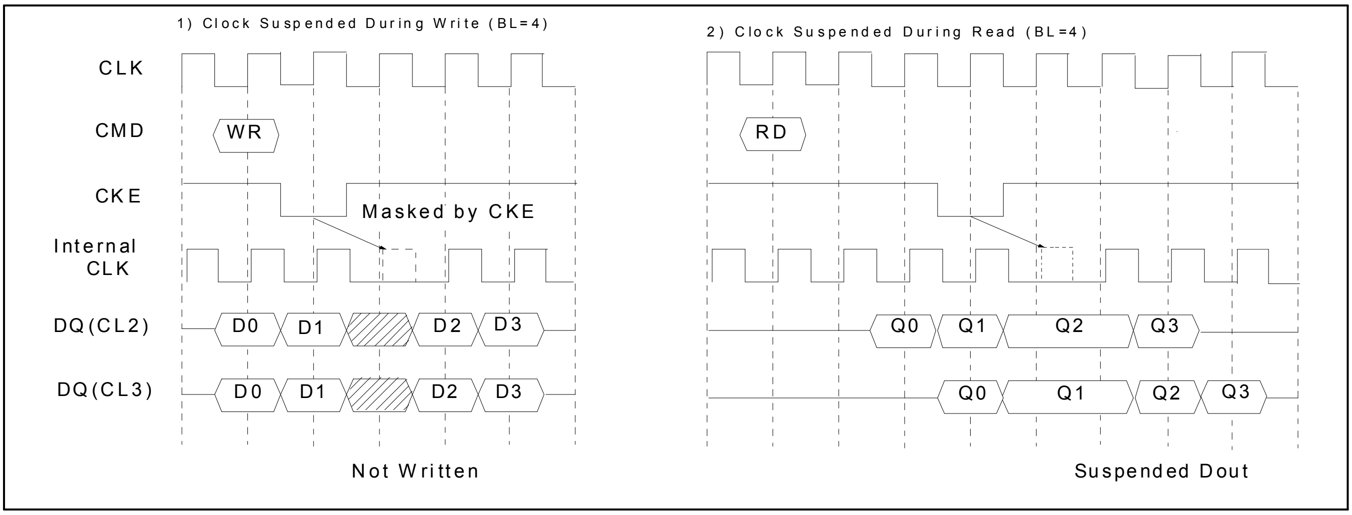


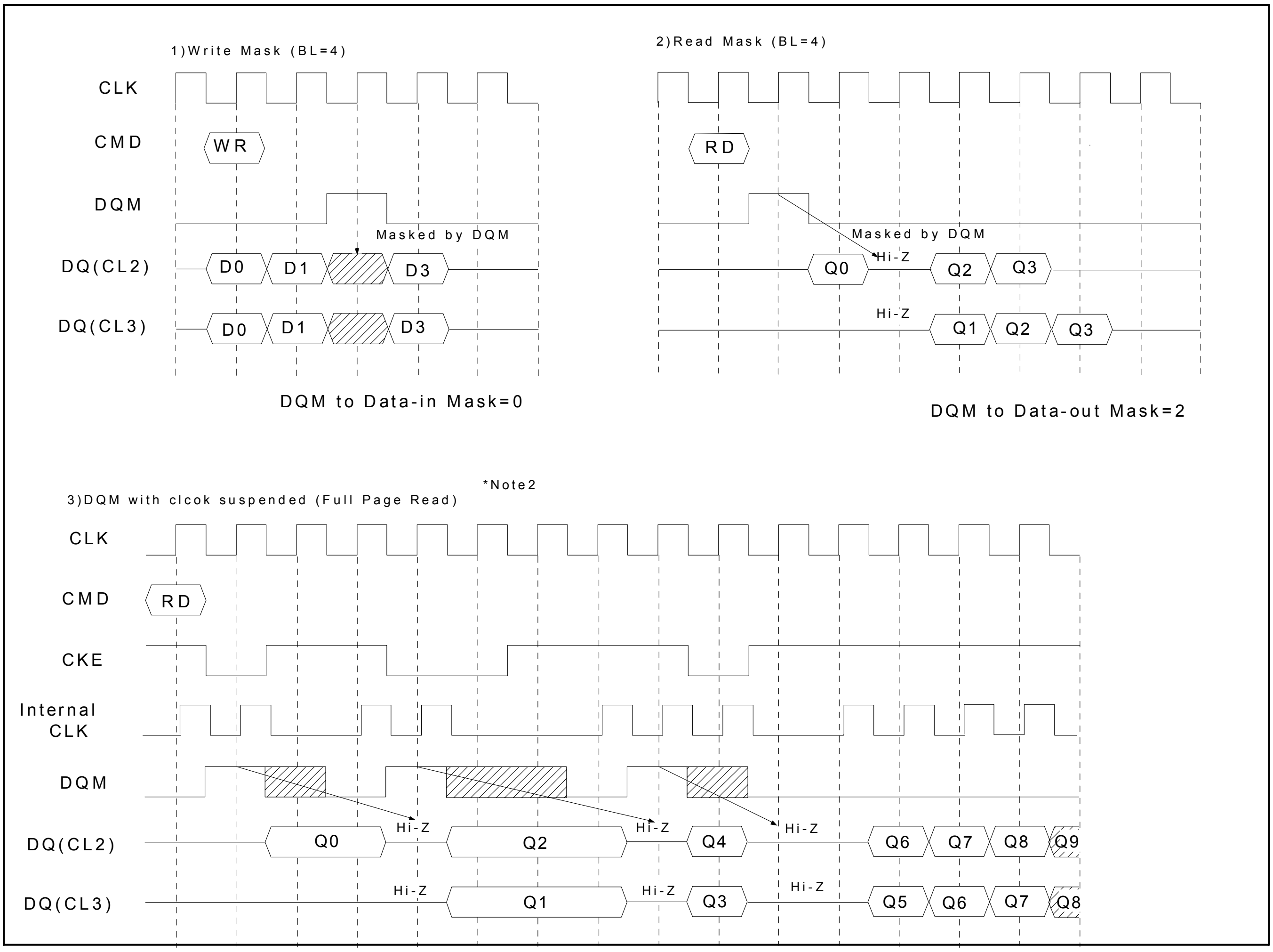
Fig. 9 No operation

BASIC FEATURE AND FUNCTION DESCRIPTIONS

1. CLOCK Suspend

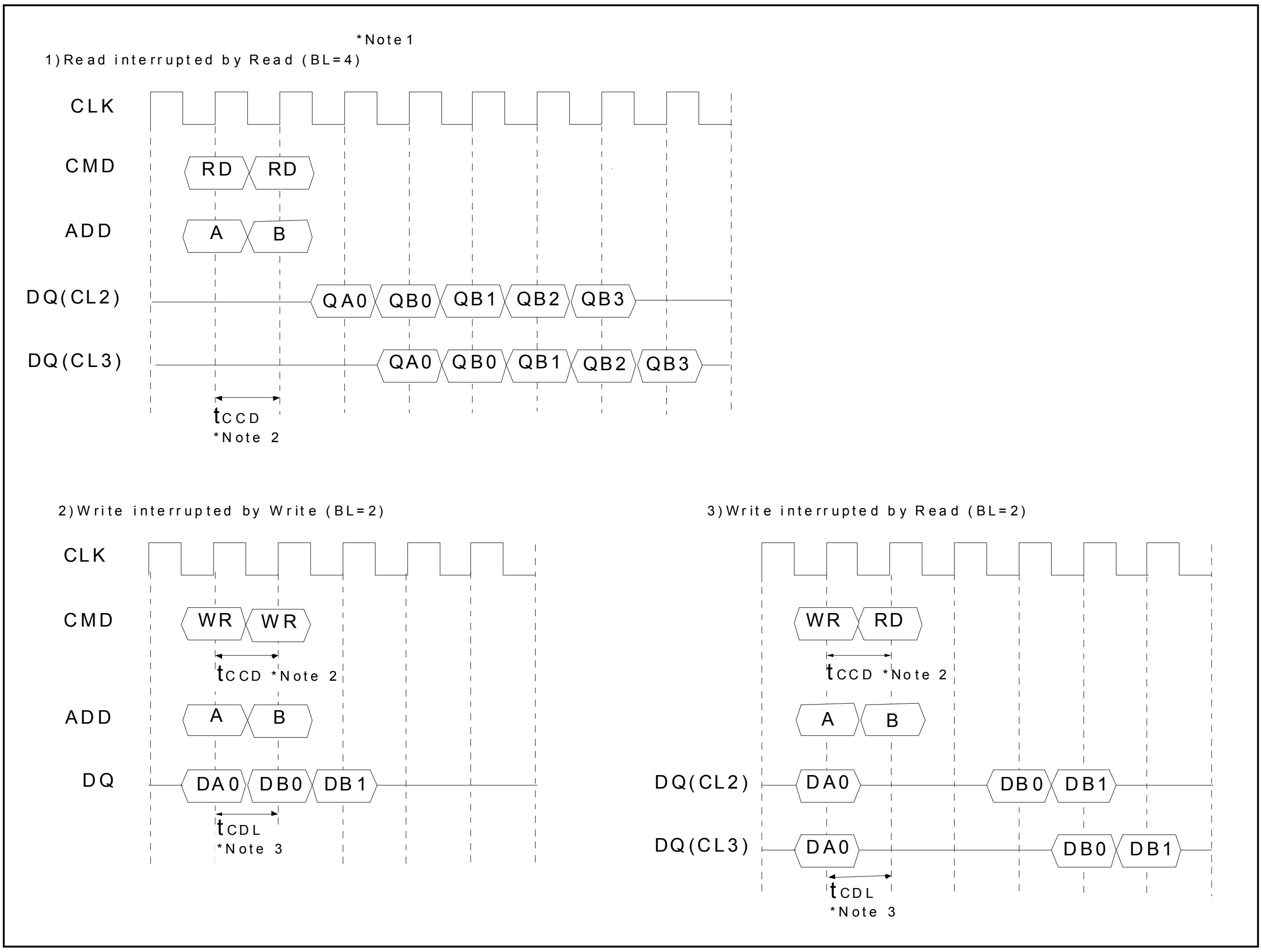


2. DQM Operation



*Note :1. CKE to CLK disable/enable = 1CLK.
2. DQM masks data out Hi-Z after 2CLKs which should masked by CKE ”L”.
3. DQM masks both data-in and data-out.

3. $\overline{\text{CAS}}$ Interrupt (I)

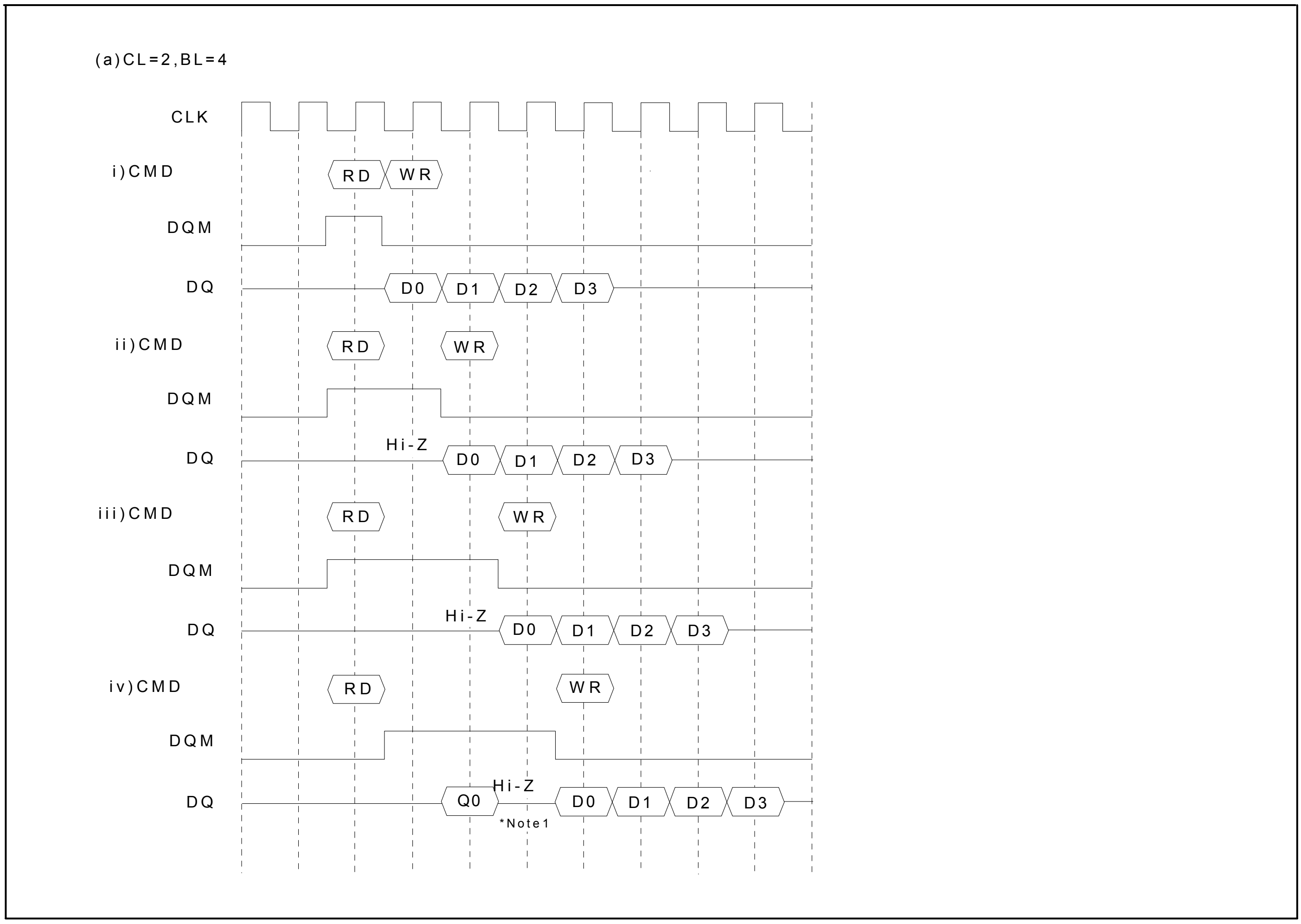


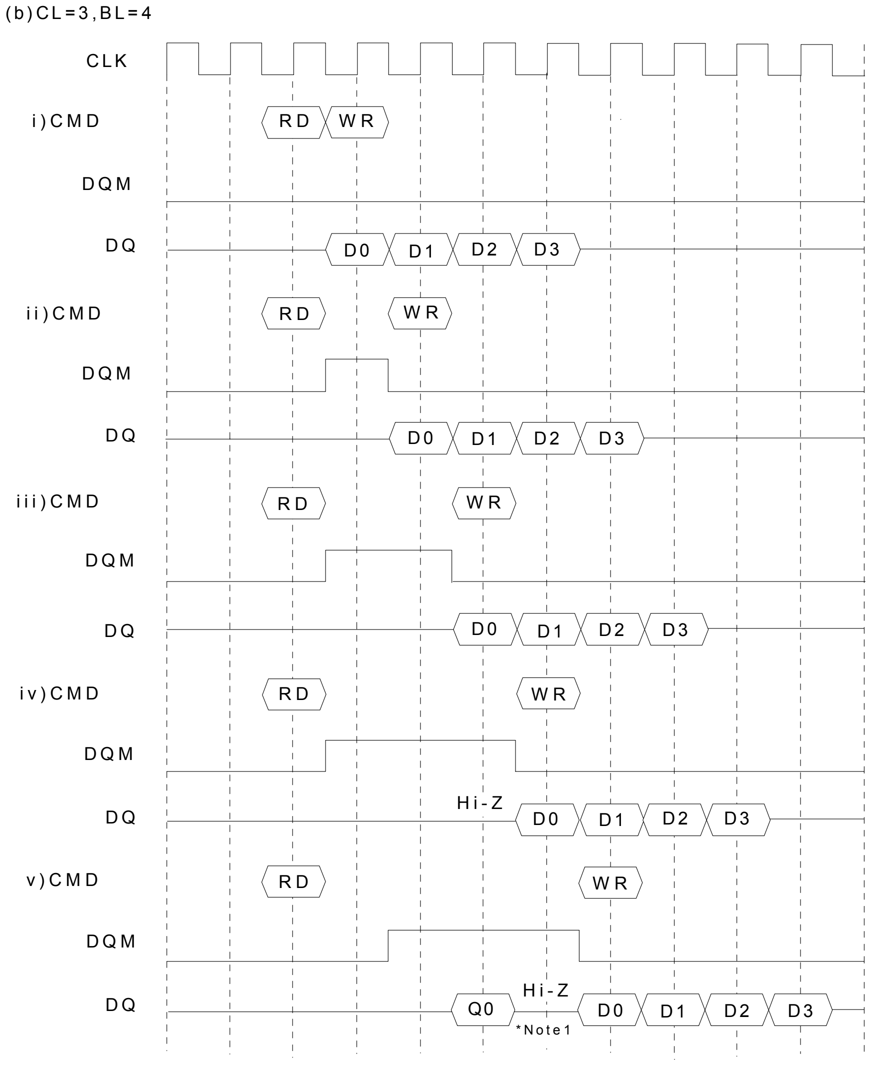
*Note : 1. By “interrupt” is meant to stop burst read/write by external before the end of burst.
By " $\overline{\text{CAS}}$ interrupt ", to stop burst read/write by $\overline{\text{CAS}}$ access; read and write.

2. t_{CCD} : $\overline{\text{CAS}}$ to $\overline{\text{CAS}}$ delay. (=1CLK)

3. t_{CDL} : Last data in to new column address delay. (=1CLK)

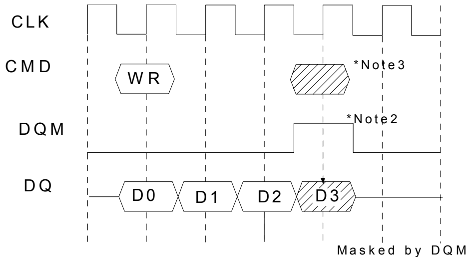
4. $\overline{\text{CAS}}$ Interrupt (II) : Read Interrupted by Write & DQM





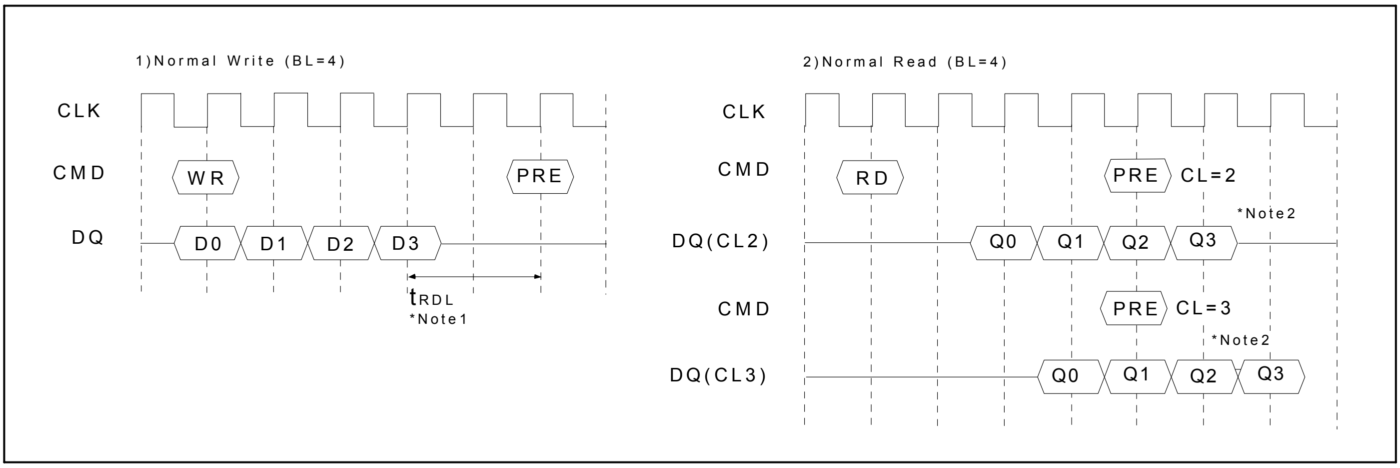
*Note : 1. To prevent bus contention, there should be at least one gap between data in and data out.

5. Write Interrupted by Precharge & DQM

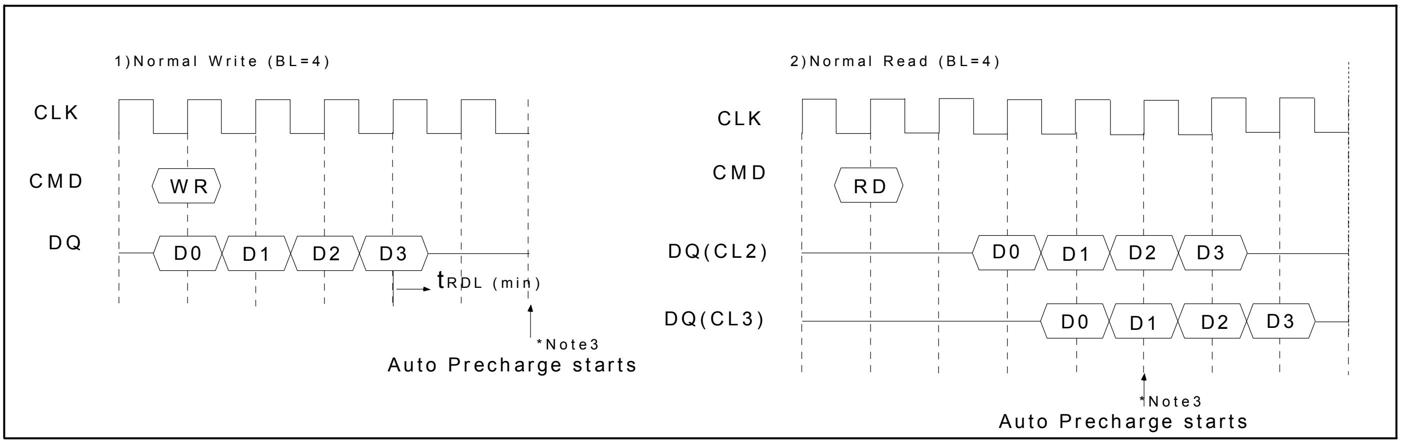


*Note : 1. To prevent bus contention, DQM should be issued which makes at least one gap between data in and data out.
2. To inhibit invalid write, DQM should be issued.
3. This precharge command and burst write command should be of the same bank, otherwise it is not precharge interrupt but only another bank precharge of four banks operation.

6. Precharge

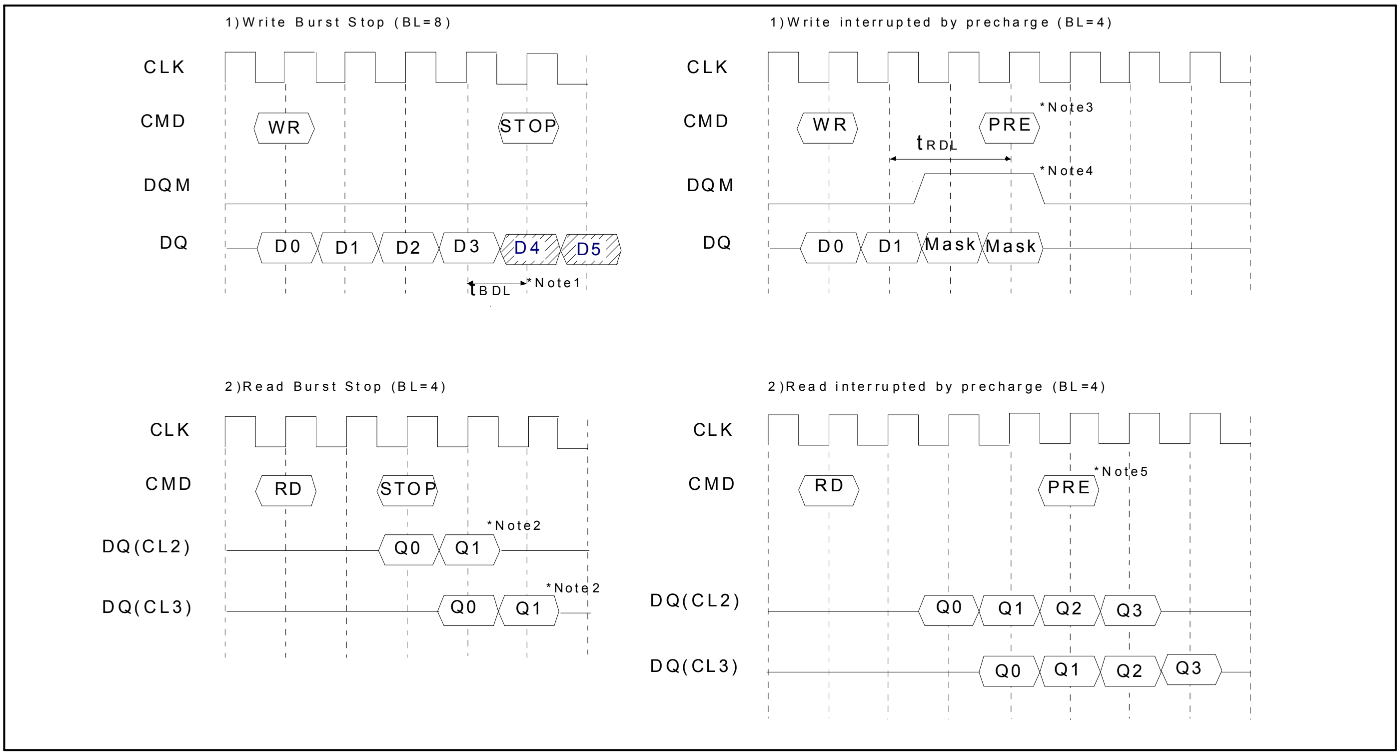


7. Auto Precharge

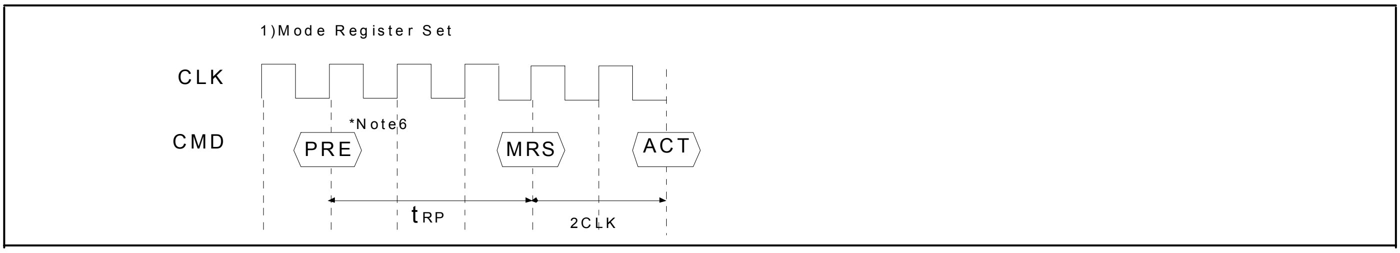


*Note : 1. t_{RDL} : Last data in to row precharge delay.
2. Number of valid output data after row precharge : 1,2 for CAS Latency = 2,3 respectively.
3. The row active command of the precharge bank can be issued after t_{RP} from this point.
The new read/write command of other activated bank can be issued from this point.
At burst read/write with auto precharge, CAS interrupt of the same/another bank is illegal.

8. Burst Stop & Interrupted by Precharge

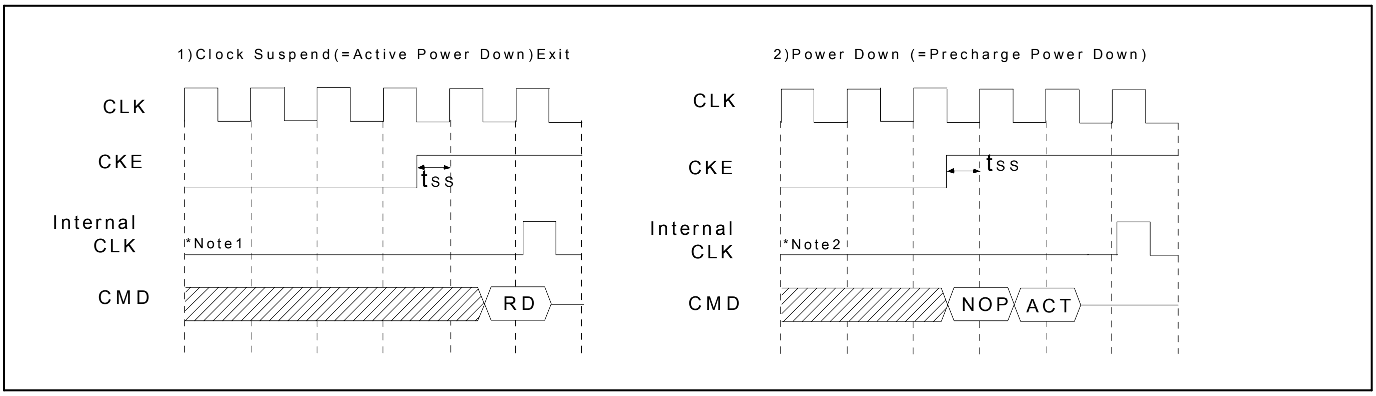


9. MRS

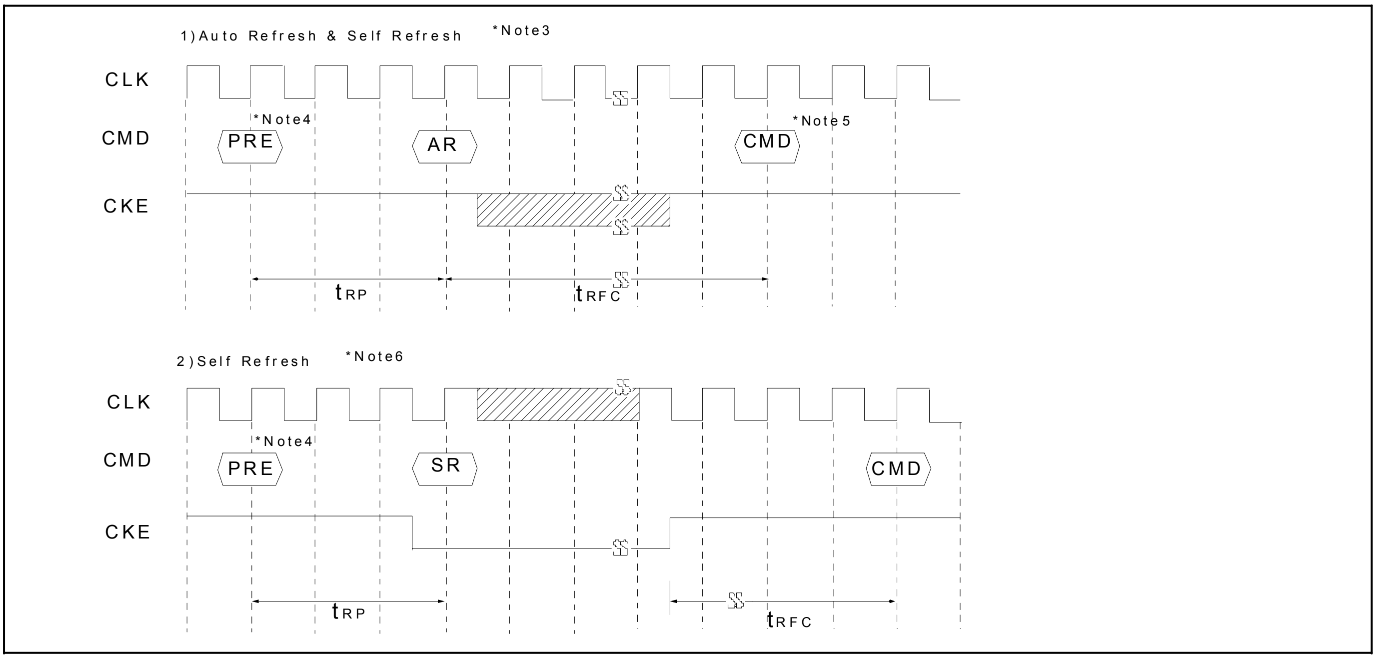


*Note: 1. tBDL : 1 CLK ; Last data in to burst stop delay.
Read or write burst stop command is valid at every burst length.
2. Number of valid output data after burst stop : 1,2 for CAS latency = 2,3 respectiviely.
3. Write burst is terminated. tRDL determinates the last data write.
4. DQM asserted to prevent corruption of locations D2 and D3.
5. Precharge can be issued here or earlier (satisfying tRAS min delay) with DQM.
6. PRE : All banks precharge, if necessary.
MRS can be issued only at all banks precharge state.

10. Clock Suspend Exit & Power Down Exit



11. Auto Refresh & Self Refresh



*Note :
1. Active power down : one or more banks active state.
2. Precharge power down : all banks precharge state.
3. The auto refresh is the same as CBR refresh of conventional DRAM.
   No precharge commands are required after auto refresh command.
   During t_{RFC} from auto refresh command, any other command can not be accepted.
4. Before executing auto/self refresh command, all banks must be idle state.
5. MRS, Bank Active, Auto/Self Refresh, Power Down Mode Entry.
6. During self refresh entry, refresh interval and refresh operation are performed internally.
   After self refresh entry, self refresh mode is kept while CKE is low.
   During self refresh entry, all inputs expect CKE will be don’t cared, and outputs will be in Hi-Z state.
   For the time interval of t_{RFC} from self refresh exit command, any other command can not be accepted.

12. About Burst Type Control

Basic MODE	Sequential Counting	At MRS A3 = “0”. See the BURST SEQUENCE TABLE. (BL = 4,8) BL = 1, 2, 4, 8 and full page.
	Interleave Counting	At MRS A3 = “1”. See the BURST SEQUENCE TABLE. (BL = 4,8) BL = 4, 8 At BL =1, 2 interleave Counting = Sequential Counting
Random MODE	Random Column Access t_{CCD} = 1 CLK	Every cycle Read/Write Command with random column address can realize Random Column Access. That is similar to Extended Data Out (EDO) Operation of conventional DRAM.

13. About Burst Length Control

Basic MODE	1	At MRS A210 = “000” At auto precharge . t_{RAS} should not be violated.
	2	At MRS A210 = “001” At auto precharge . t_{RAS} should not be violated.
	4	At MRS A210 = “010”
	8	At MRS A210 = “011”
	Full Page	At MRS A210 = “111” At the end of the burst length , burst is warp-around.
Random MODE	Burst Stop	t_{BDL} = 1, Valid DQ after burst stop is 1, 2 for CAS latency 2, 3 respectively. Using burst stop command, any burst length control is possible.
Interrupt MODE	$\overline{\text{RAS}}$ Interrupt (Interrupted by Precharge)	Before the end of burst. Row precharge command of the same bank stops read /write burst with auto precharge. t_{RDL} = 1 with DQM , Valid DQ after burst stop is 1, 2 for CAS latency 2, 3 respectively. During read/write burst with auto precharge, $\overline{\text{RAS}}$ interrupt can not be issued.
	$\overline{\text{CAS}}$ Interrupt	Before the end of burst, new read/write stops read/write burst and starts new read/write burst. During read/write burst with auto precharge, $\overline{\text{CAS}}$ interrupt can not be issued.

FUNCTION TURTH TABLE (TABLE 1)

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA	ADDR	ACTION	Note
IDLE	H	X	X	X	X	X	NOP	
	L	H	H	H	X	X	NOP	
	L	H	H	L	X	X	ILLEGAL	2
	L	H	L	X	BA	CA, A10/AP	ILLEGAL	2
	L	L	H	H	BA	RA	Row (&Bank) Active ; Latch RA	
	L	L	H	L	BA	A10/AP	NOP	4
	L	L	L	H	X	X	Auto Refresh or Self Refresh	5
	L	L	L	L	OP code	OP code	Mode Register Access	5
Row Active	H	X	X	X	X	X	NOP	
	L	H	H	H	X	X	NOP	
	L	H	H	L	X	X	ILLEGAL	2
	L	H	L	H	BA	CA, A10/AP	Begin Read ; latch CA ; determine AP	
	L	H	L	L	BA	CA, A10/AP	Begin Write ; latch CA ; determine AP	
	L	L	H	H	BA	RA	ILLEGAL	2
	L	L	H	L	BA	A10/AP	Precharge	
	L	L	L	X	X	X	ILLEGAL	
Read	H	X	X	X	X	X	NOP (Continue Burst to End → Row Active)	
	L	H	H	H	X	X	NOP (Continue Burst to End → Row Active)	
	L	H	H	L	X	X	Term burst → Row active	
	L	H	L	H	BA	CA, A10/AP	Term burst, New Read, Determine AP	
	L	H	L	L	BA	CA, A10/AP	Term burst, New Write, Determine AP	3
	L	L	H	H	BA	RA	ILLEGAL	2
	L	L	H	L	BA	A10/AP	Term burst, Precharge timing for Reads	
	L	L	L	X	X	X	ILLEGAL	
Write	H	X	X	X	X	X	NOP (Continue Burst to End → Row Active)	
	L	H	H	H	X	X	NOP (Continue Burst to End → Row Active)	
	L	H	H	L	X	X	Term burst → Row active	
	L	H	L	H	BA	CA, A10/AP	Term burst, New Read, Determine AP	3
	L	H	L	L	BA	CA, A10/AP	Term burst, New Write, Determine AP	3
	L	L	H	H	BA	RA	ILLEGAL	2
	L	L	H	L	BA	A10/AP	Term burst, Precharge timing for Writes	3
	L	L	L	X	X	X	ILLEGAL	
Read with Auto Precharge	H	X	X	X	X	X	NOP (Continue Burst to End → Row Active)	
	L	H	H	H	X	X	NOP (Continue Burst to End → Row Active)	
	L	H	H	L	X	X	ILLEGAL	
	L	H	L	X	BA	CA, A10/AP	ILLEGAL	
	L	L	H	X	BA	RA, RA10	ILLEGAL	2
	L	L	L	X	X	X	ILLEGAL	
Write with Auto Precharge	H	X	X	X	X	X	NOP (Continue Burst to End → Row Active)	
	L	H	H	H	X	X	NOP (Continue Burst to End → Row Active)	
	L	H	H	L	X	X	ILLEGAL	
	L	H	L	X	BA	CA, A10/AP	ILLEGAL	
	L	L	H	X	BA	RA, RA10	ILLEGAL	2
	L	L	L	X	X	X	ILLEGAL	

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA	ADDR	ACTION	Note
Read with Auto Precharge	H	X	X	X	X	X	NOP → Idle after tRP	
	L	H	H	H	X	X	NOP → Idle after tRP	
	L	H	H	L	X	X	ILLEGAL	2
	L	H	L	X	BA	CA	ILLEGAL	2
	L	L	H	H	BA	RA	ILLEGAL	2
	L	L	H	L	BA	A10/AP	NOP → Idle after tRPL	4
	L	L	L	X	X	X	ILLEGAL	
Row Activating	H	X	X	X	X	X	NOP → Row Active after tRCD	
	L	H	H	H	X	X	NOP → Row Active after tRCD	
	L	H	H	L	X	X	ILLEGAL	2
	L	H	L	X	BA	CA	ILLEGAL	2
	L	L	H	H	BA	RA	ILLEGAL	2
	L	L	H	L	BA	A10/AP	ILLEGAL	2
	L	L	L	X	X	X	ILLEGAL	
Refreshing	H	X	X	X	X	X	NOP → Idle after tRFC	
	L	H	H	X	X	X	NOP → Idle after tRFC	
	L	H	L	X	X	X	ILLEGAL	
	L	L	H	X	X	X	ILLEGAL	
	L	L	L	X	X	X	ILLEGAL	
Mode Register Accessing	H	X	X	X	X	X	NOP → Idle after 2clocks	
	L	H	H	H	X	X	NOP → Idle after 2clocks	
	L	H	H	L	X	X	ILLEGAL	
	L	H	L	X	X	X	ILLEGAL	
	L	L	X	X	X	X	ILLEGAL	

Abbreviations :
RA = Row Address
BA = Bank Address
NOP = No Operation Command
CA = Column Address
AP = Auto Precharge

*Note :
1. All entries assume the CKE was active (High) during the precharge clock and the current clock cycle.
2. Illegal to bank in specified state ; Function may be legal in the bank indicated by BA, depending on the state of the bank.
3. Must satisfy bus contention, bus turn around, and/or write recovery requirements.
4. NOP to bank precharge or in idle state. May precharge bank indicated by BA (and A10/AP).
5. Illegal if any bank is not idle.

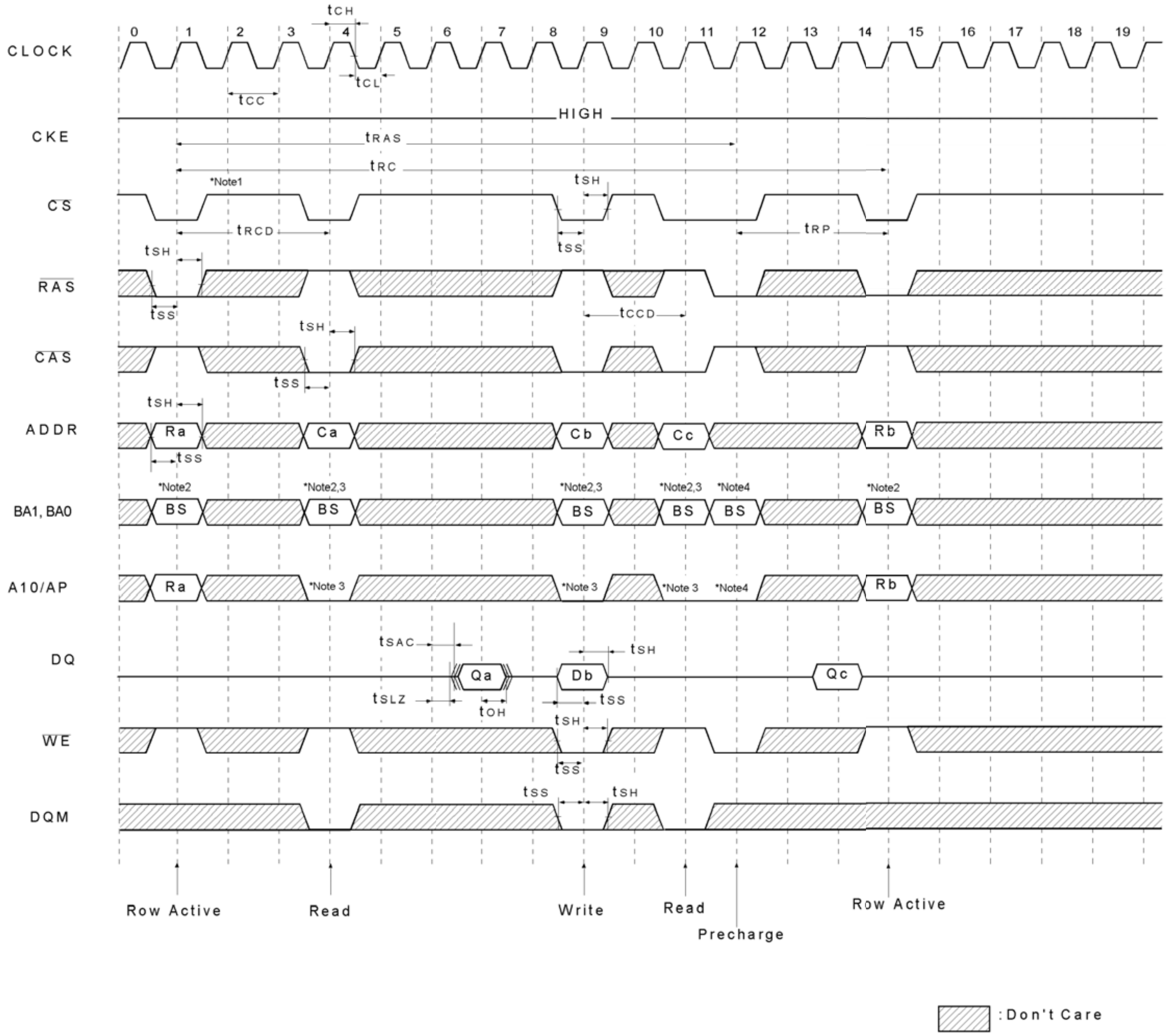
FUNCTION TRUTH TABLE (TABLE2)

Current State	CKE (n-1)	CKE n	$\overline{\text{CS}}$	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	ADDR	ACTION	Note
Self Refresh	H	X	X	X	X	X	X	INVALID	
	L	H	H	X	X	X	X	Exit Self Refresh → Idle after tRFC (ABI)	6
	L	H	L	H	H	H	X	Exit Self Refresh → Idle after tRFC (ABI)	6
	L	H	L	H	H	L	X	ILLEGAL	
	L	H	L	H	L	X	X	ILLEGAL	
	L	H	L	L	X	X	X	ILLEGAL	
	L	L	X	X	X	X	X	NOP (Maintain Self Refresh)	
All Banks Precharge Power Down	H	X	X	X	X	X	X	INVALID	
	L	H	H	X	X	X	X	Exit Self Refresh → ABI	7
	L	H	L	H	H	H	X	Exit Self Refresh → ABI	7
	L	H	L	H	H	L	X	ILLEGAL	
	L	H	L	H	L	X	X	ILLEGAL	
	L	H	L	L	X	X	X	ILLEGAL	
	L	L	X	X	X	X	X	NOP (Maintain Low Power Mode)	
All Banks Idle	H	H	X	X	X	X	X	Refer to Table1	
	H	L	H	X	X	X	X	Enter Power Down	8
	H	L	L	H	H	H	X	Enter Power Down	8
	H	L	L	H	H	L	X	ILLEGAL	
	H	L	L	H	L	X	X	ILLEGAL	
	H	L	L	L	H	H	RA	Row (& Bank) Active	
	H	L	L	L	H	H	X	NOP	
	H	L	L	L	L	L	X	Enter Self Refresh	8
	H	L	L	L	L	L	OP Code	Mode Register Access	
	L	L	X	X	X	X	X	NOP	
Any State other than Listed above	H	H	X	X	X	X	X	Refer to Operations in Table 1	
	H	L	X	X	X	X	X	Begin Clock Suspend next cycle	9
	L	H	X	X	X	X	X	Exit Clock Suspend next cycle	9
	L	L	X	X	X	X	X	Maintain Clock Suspend	

Abbreviations **:** ABI = All Banks Idle, RA = Row Address

*Note : 6.CKE low to high transition is asynchronous.
7.CKE low to high transition is asynchronous if restart internal clock.
A minimum setup time 1CLK + t_{SS} must be satisfy before any command other than exit.
8.Power down and self refresh can be entered only from the all banks idle state.
9.Must be a legal command.

Single Bit Read-Write-Read Cycle (Same Page) @ CAS Latency = 3,Burst Length = 1



Note : 1. All input expect CKE & DQM can be don't care when $\overline{CS}$ is high at the CLK high going edge.

2. Bank active @ read/write are controlled by BA0, BA1.

BA0	BA1	Active & Read/Write
0	0	Bank A
0	1	Bank B
1	0	Bank C
1	1	Bank D

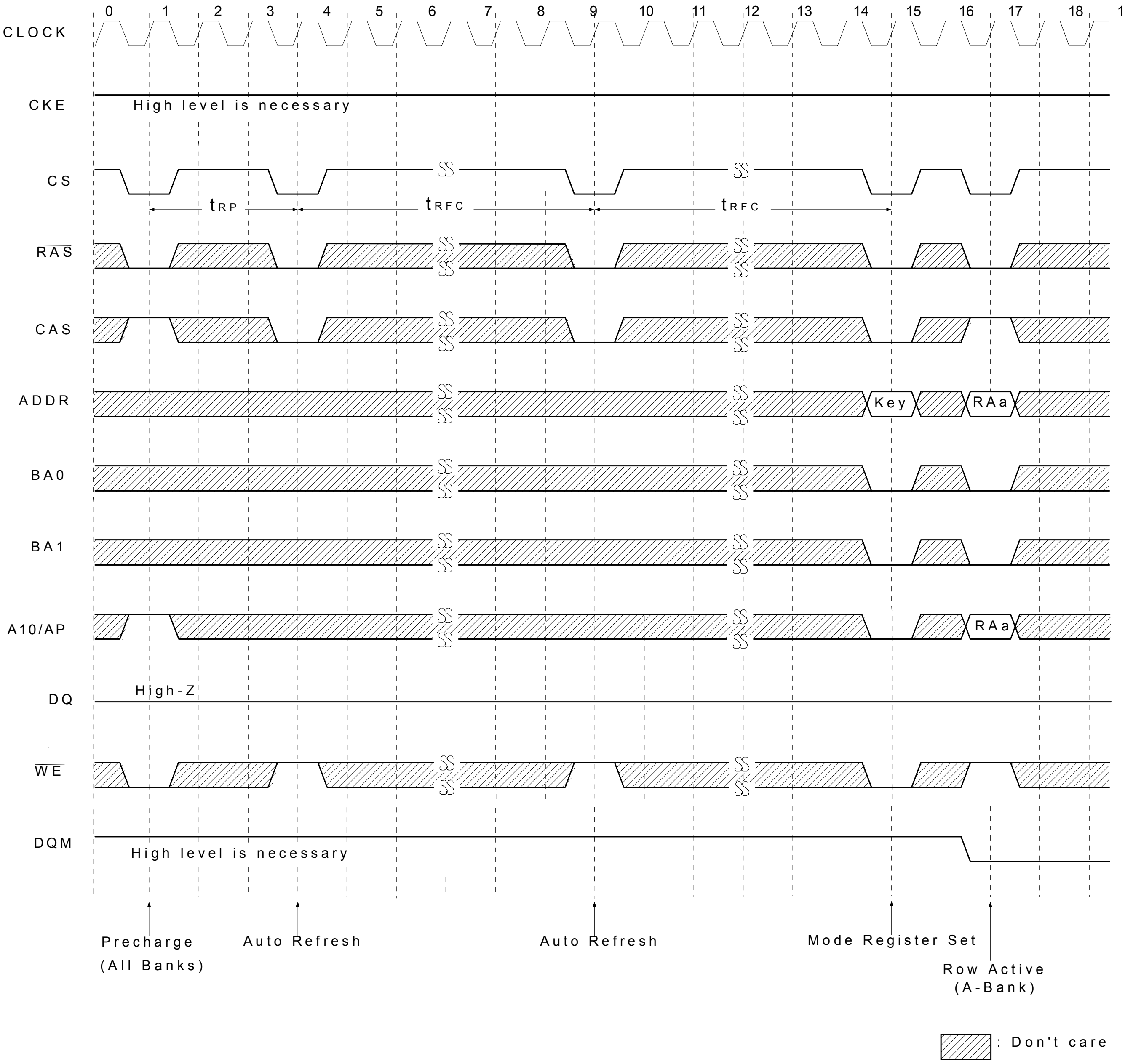
3. Enable and disable auto precharge function are controlled by A10/AP in read/write command

A10/AP	BA0	BA1	Operating
0	0	0	Disable auto precharge, leave A bank active at end of burst.
	0	1	Disable auto precharge, leave B bank active at end of burst.
	1	0	Disable auto precharge, leave C bank active at end of burst.
	1	1	Disable auto precharge, leave D bank active at end of burst.
1	0	0	Enable auto precharge , precharge bank A at end of burst.
	0	1	Enable auto precharge , precharge bank B at end of burst.
	1	0	Enable auto precharge , precharge bank C at end of burst.
	1	1	Enable auto precharge , precharge bank D at end of burst.

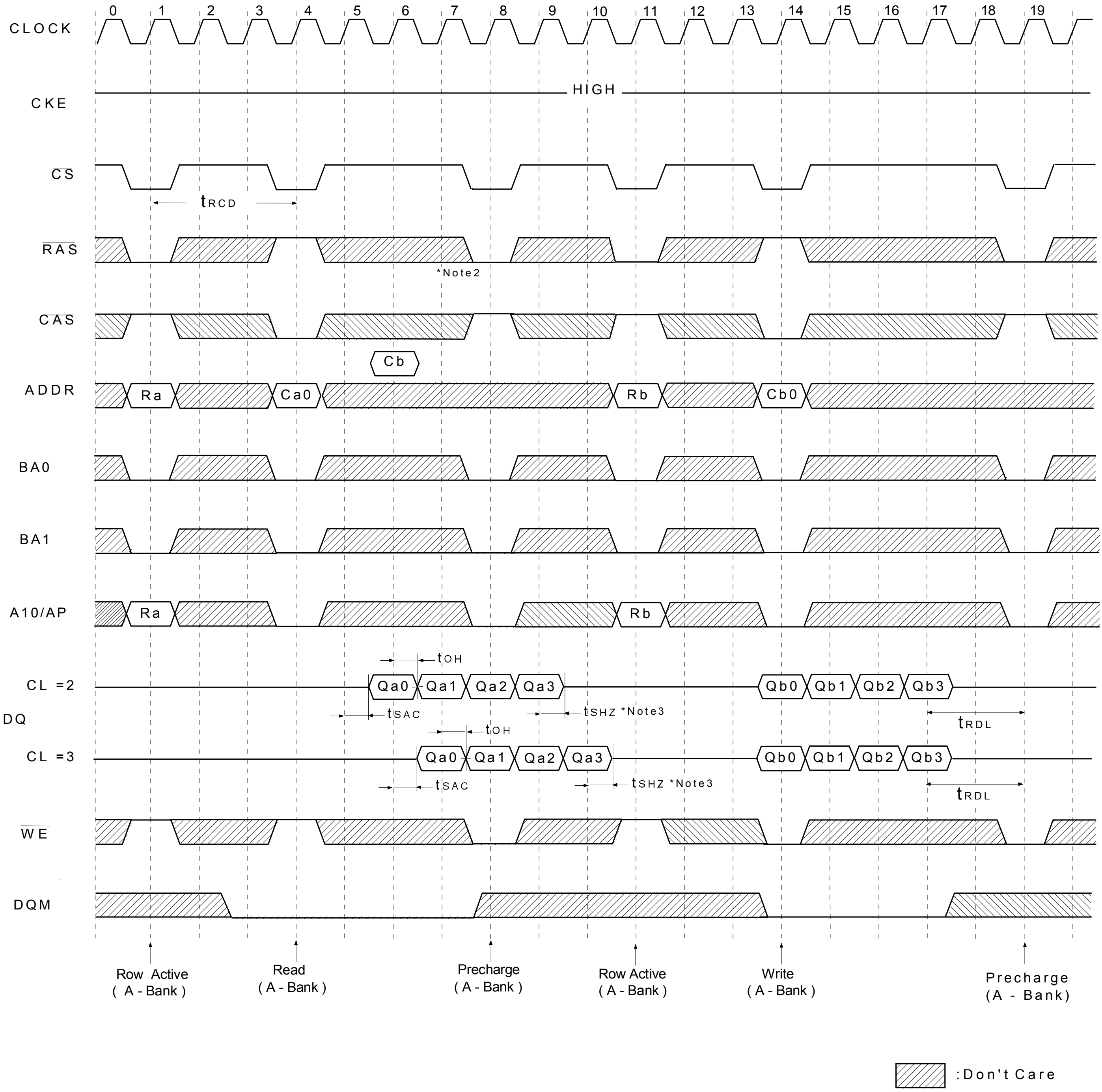
4. A10/AP and BA0, BA1 control bank precharge when precharge is asserted.

A10/AP	BA0	BA1	Precharge
0	0	0	Bank A
0	0	1	Bank B
0	1	0	Bank C
0	1	1	Bank D
1	X	X	All Banks

Power Up Sequence



Read & Write Cycle at Same Bank @ Burst Length = 4

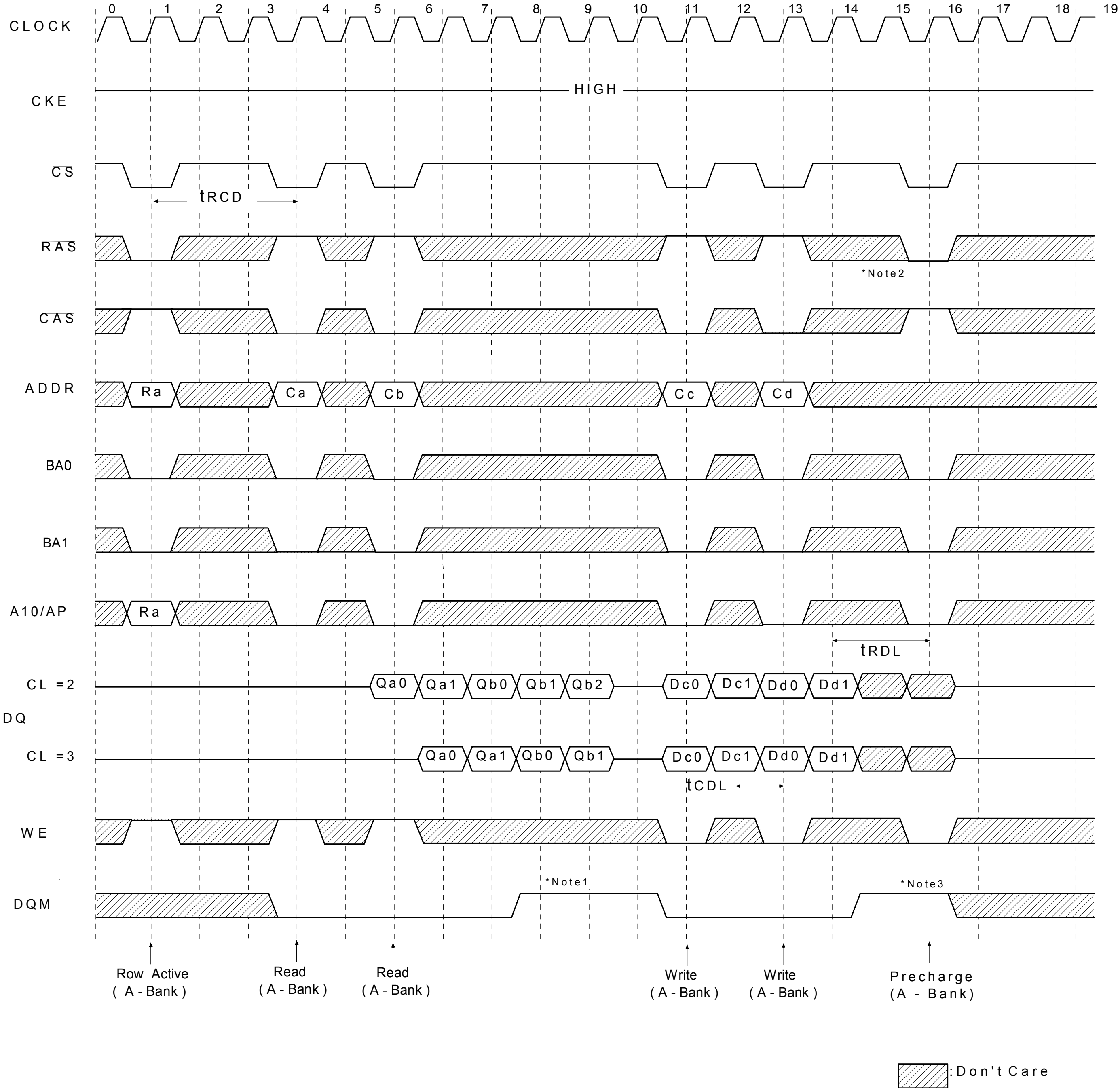


*Note : 1. Minimum row cycle times is required to complete internal DRAM operation.

2. Row precharge can interrupt burst on any cycle. [CAS Latency-1] number of valid output data is available after Row precharge. Last valid output will be Hi-Z (t_{SHZ}) after the clock.

3. Output will be Hi-Z after the end of burst. (1,2,4,8 & Full page bit burst)

Page Read & Write Cycle at Same Bank @ Burst Length = 4

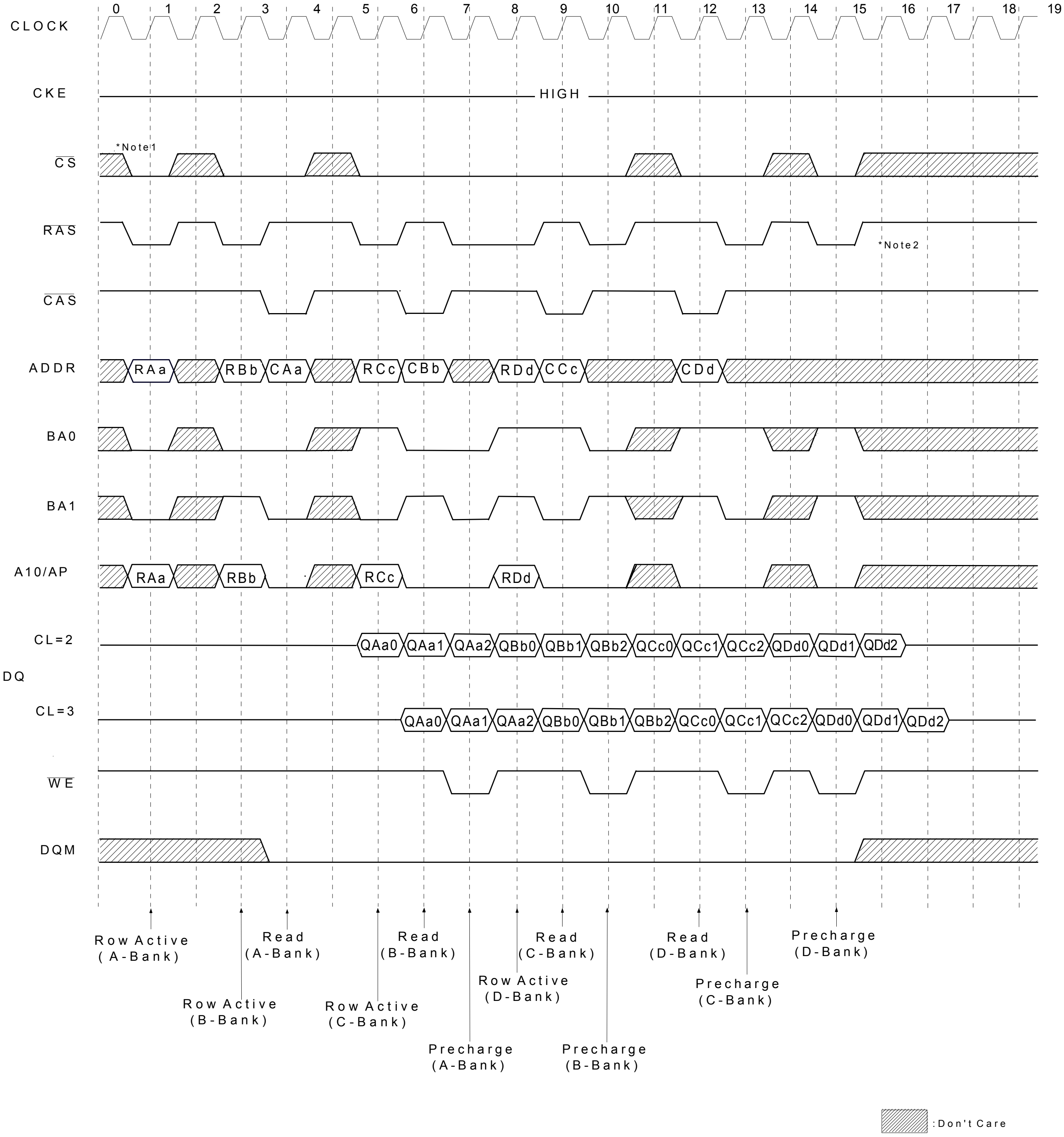


Note : 1. To Write data before burst read ends. DQM should be asserted three cycle prior to write command to avoid bus contention.

2. Row precharge will interrupt writing. Last data input , t_{RDL} before row precharge , will be written.

3. DQM should mask invalid input data on precharge command cycle when asserting precharge before end of burst. Input data after Row precharge cycle will be masked internally.

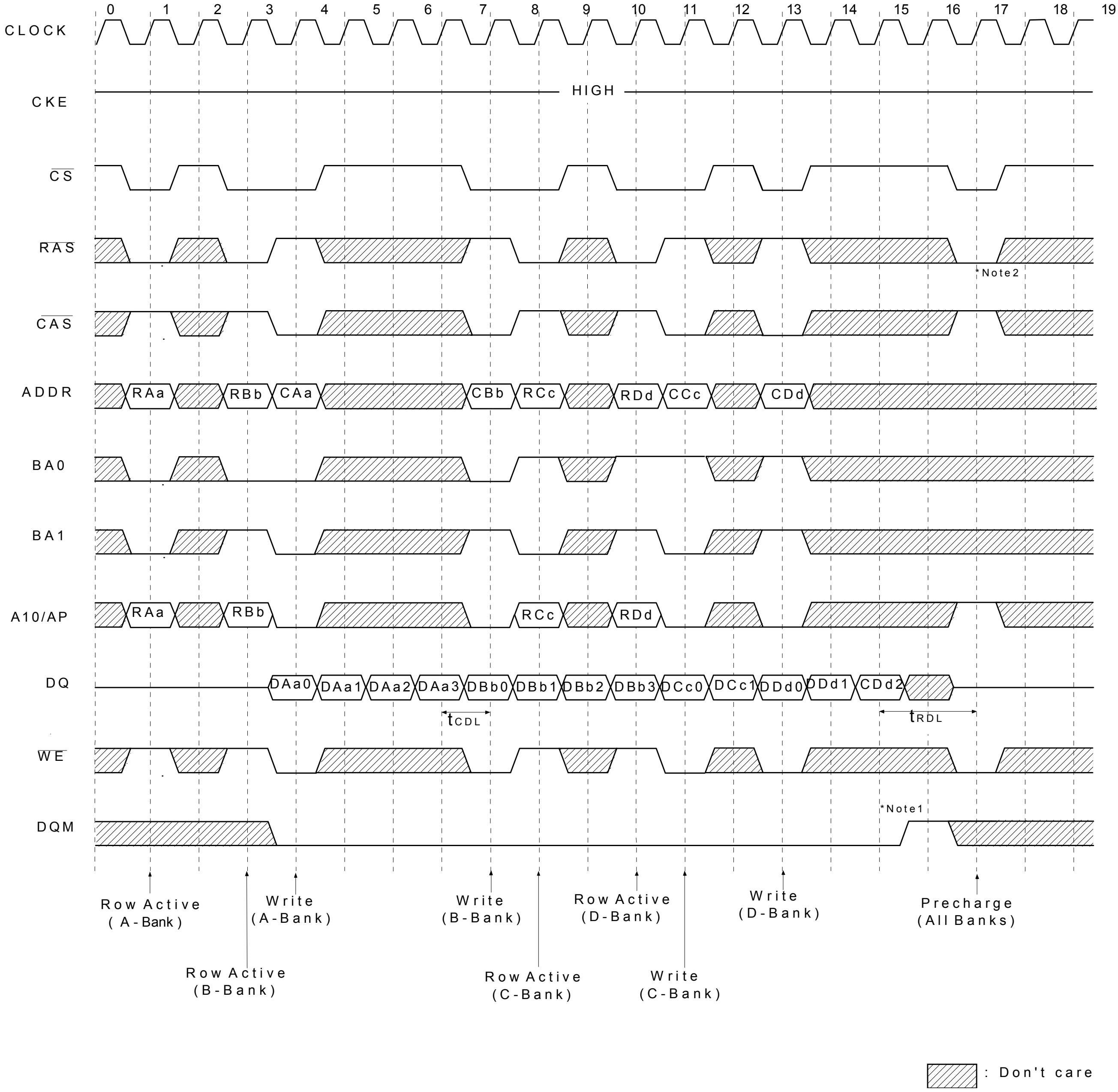
Page Read Cycle at Different Bank @ Burst Length = 4



Note: 1. $\overline{CS}$ can be don't cared when $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ are high at the clock high going edge.

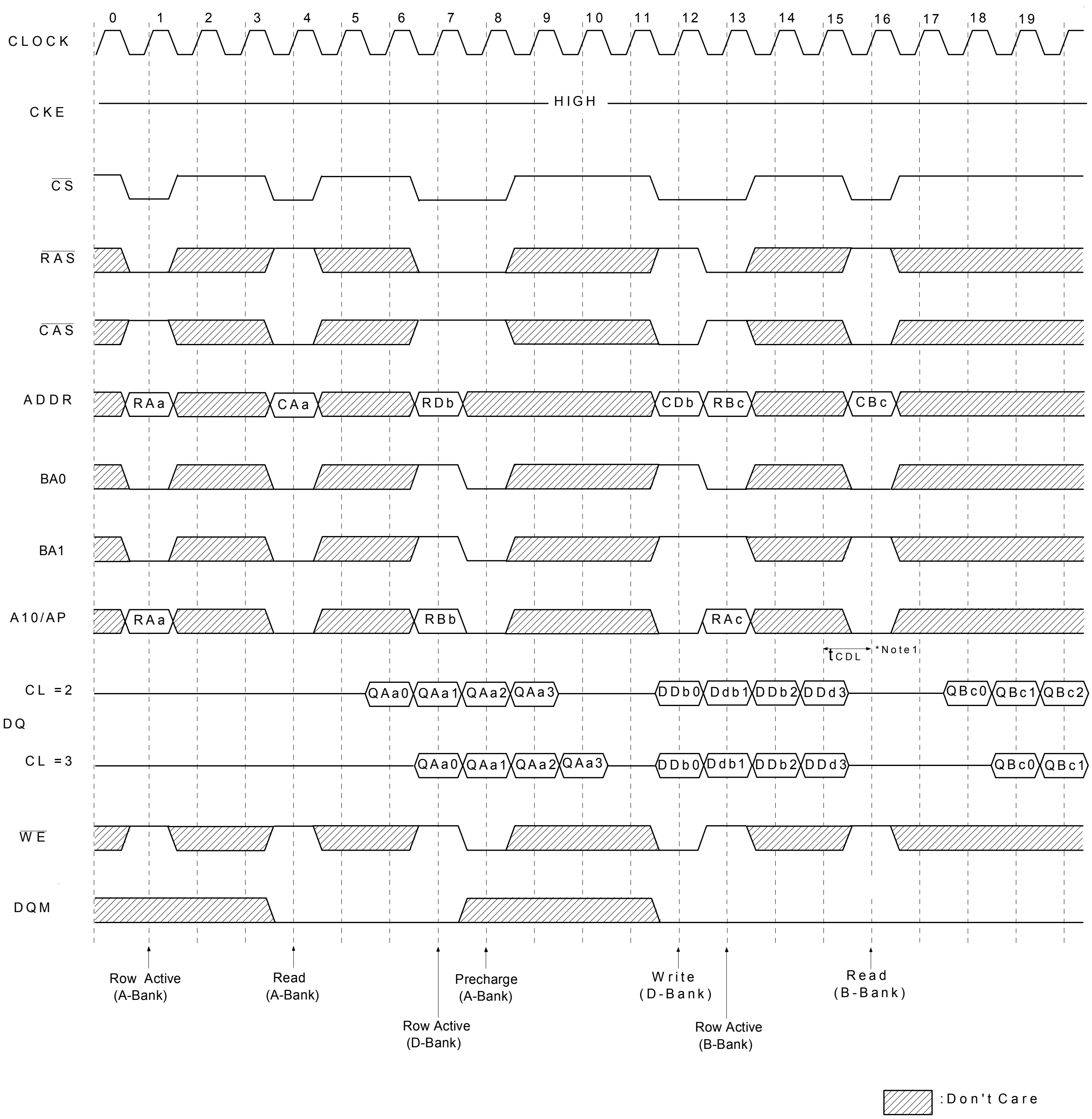
2. To interrupt a burst read by row precharge, both the read and the precharge banks must be the same.

Page Write Cycle at Different Bank @ Burst Length = 4



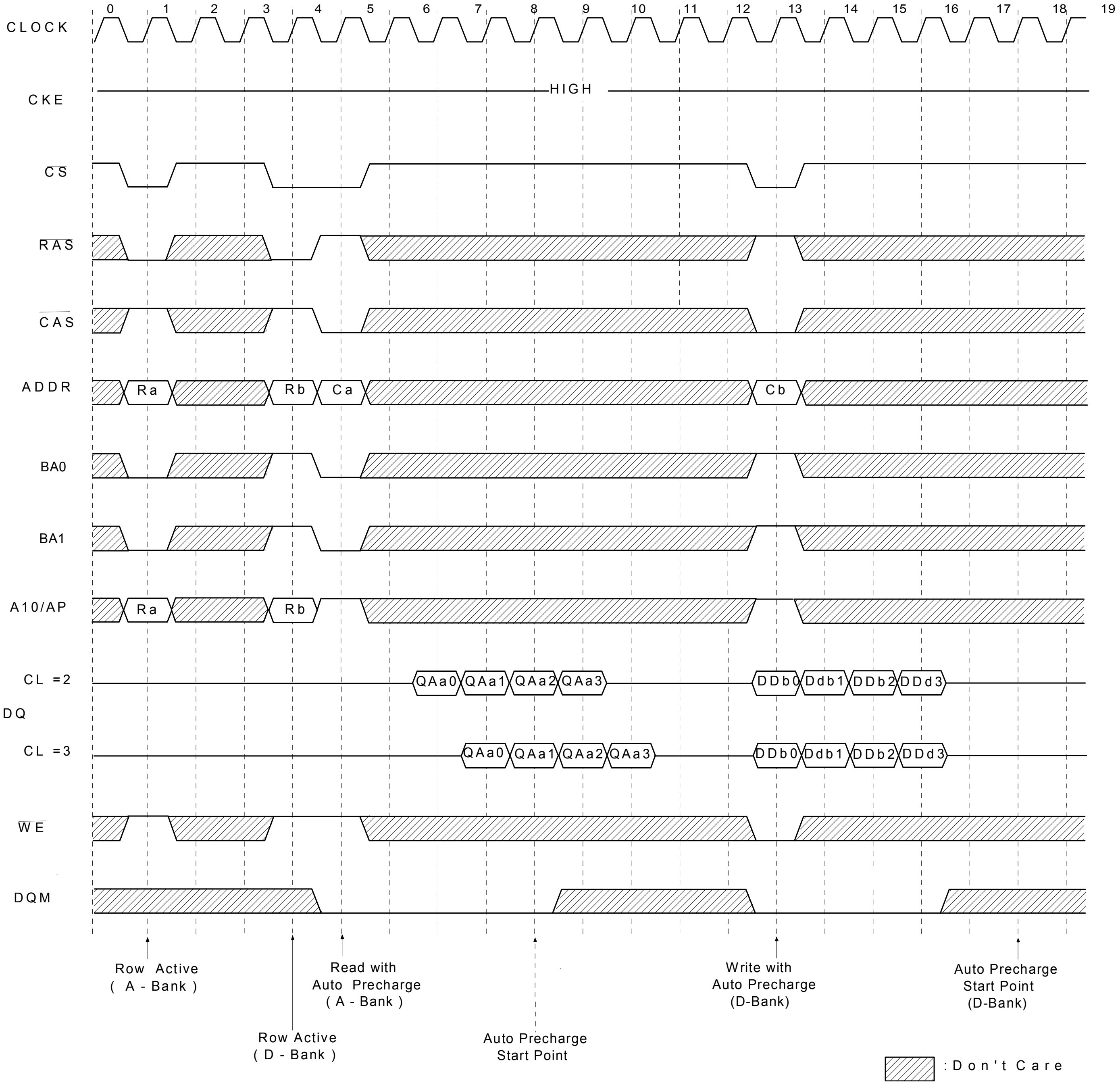
*Note : 1. To interrupt burst write by Row precharge , DQM should be asserted to mask invalid input data.
2. To interrupt burst write by Row precharge , both the write and the precharge banks must be the same.

Read & Write Cycle at Different Bank @ Burst Length = 4



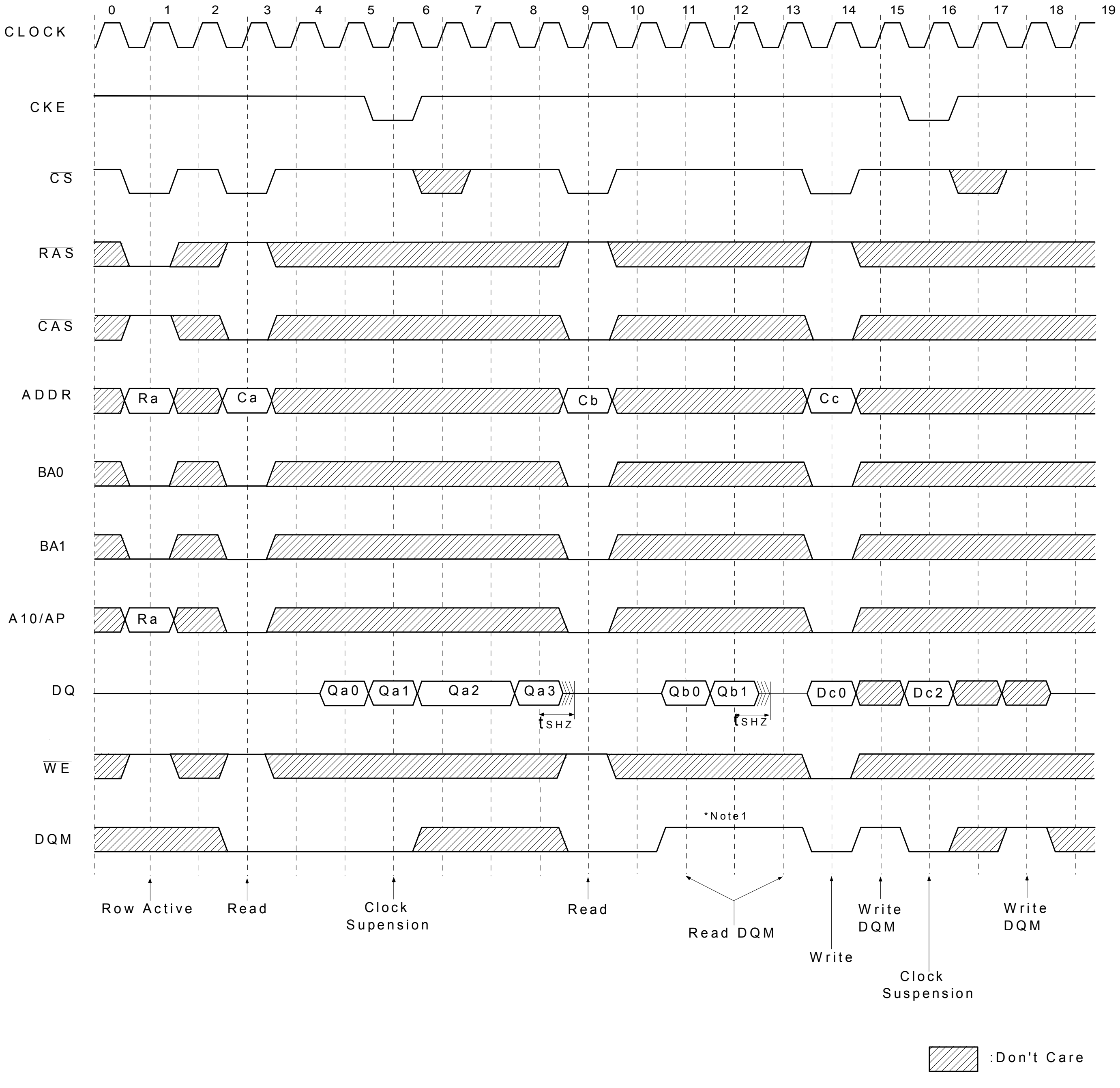
*Note : 1. tCDL should be met to complete write.

Read & Write cycle with Auto Precharge @ Burst Length = 4



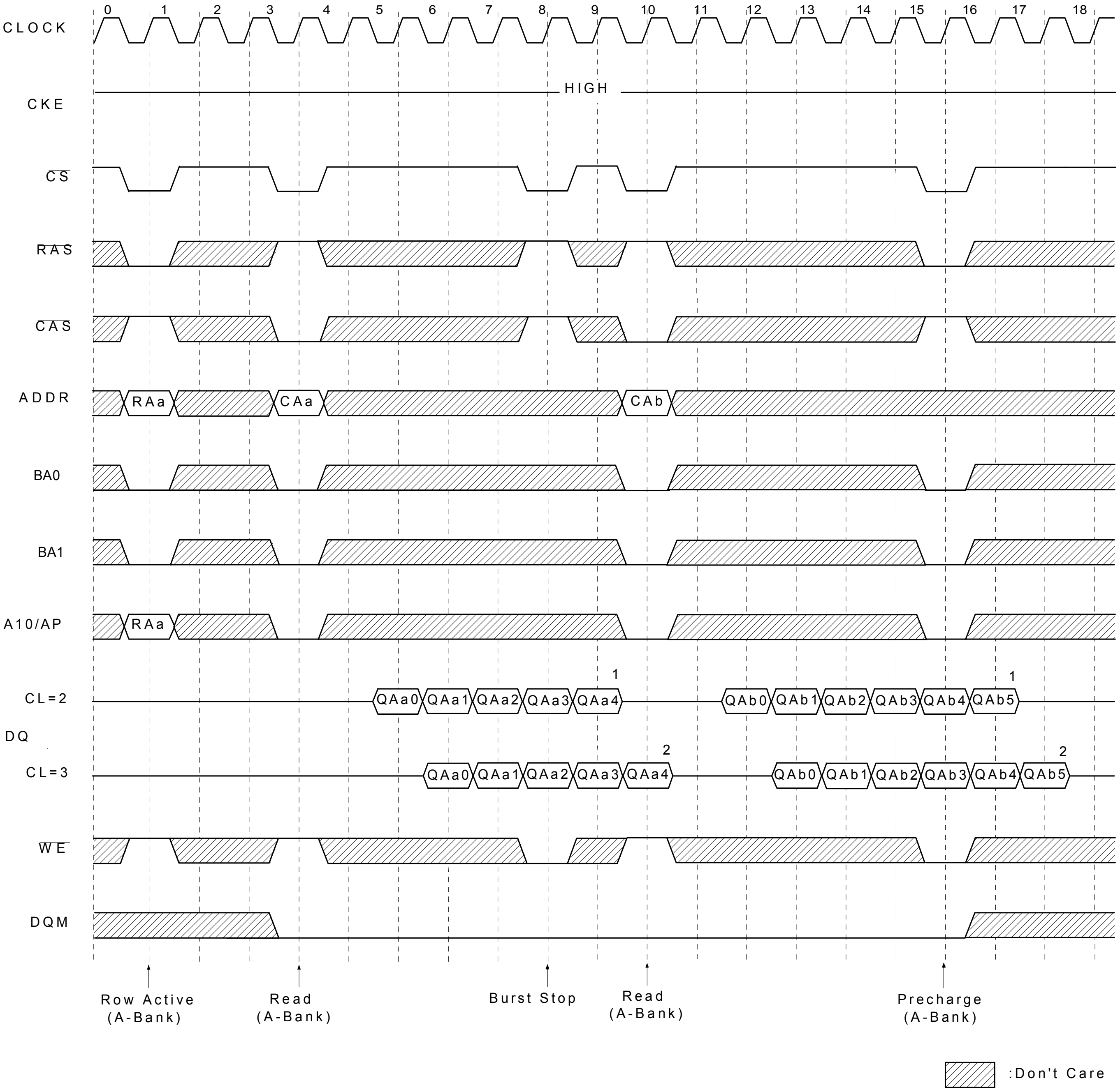
*Note : 1. t_{CDL} should be controlled to meet minimum t_{RAS} before internal precharge start.
(In the case of Burst Length = 1 & 2)

Clock Suspension & DQM Operation Cycle @ CAS Letency = 2 , Burst Length = 4



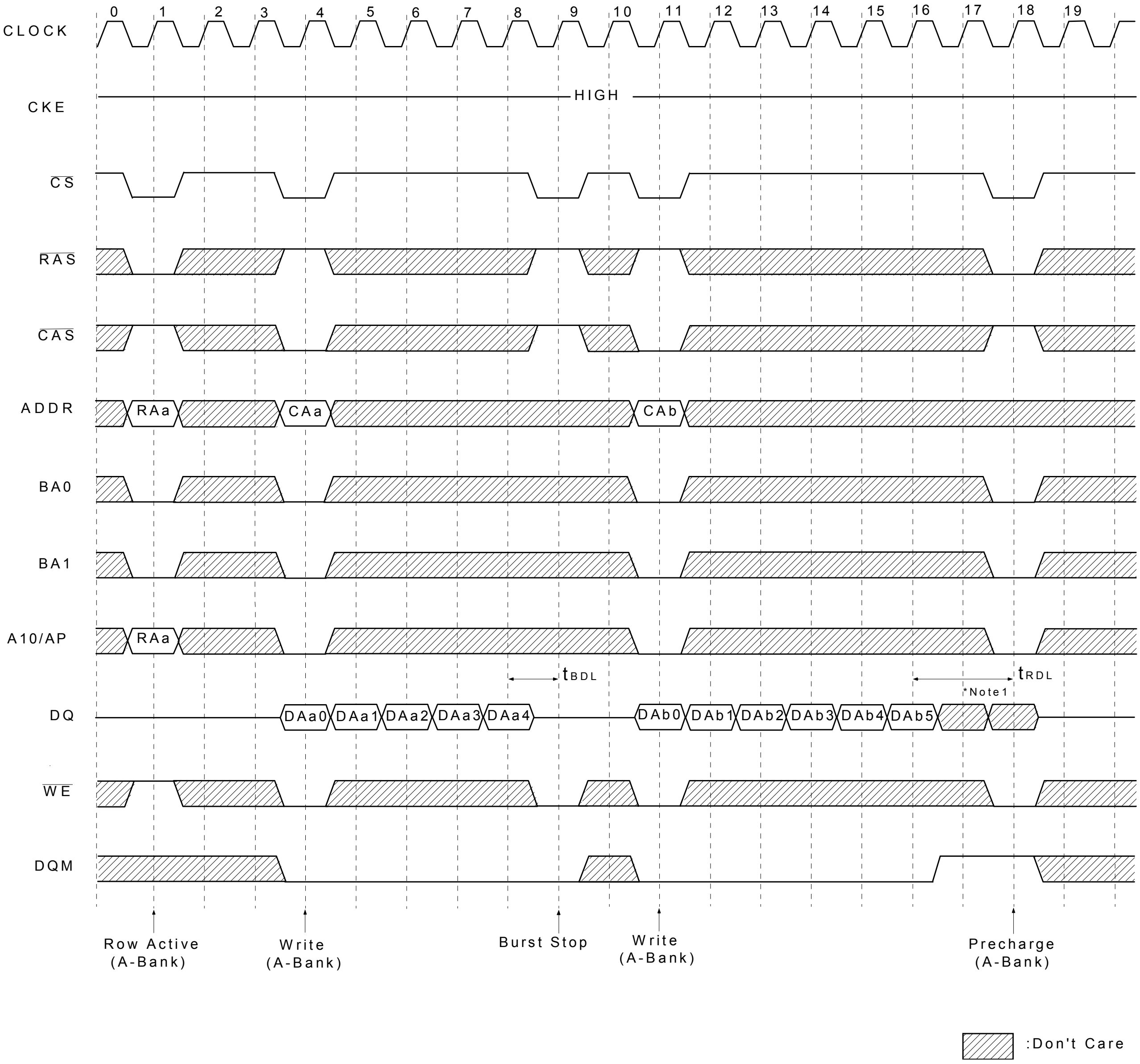
*Note : 1. DQM is needed to prevent bus contention

Read interrupted by Precharge Command & Read Burst Stop Cycle @ Burst Length = Full page



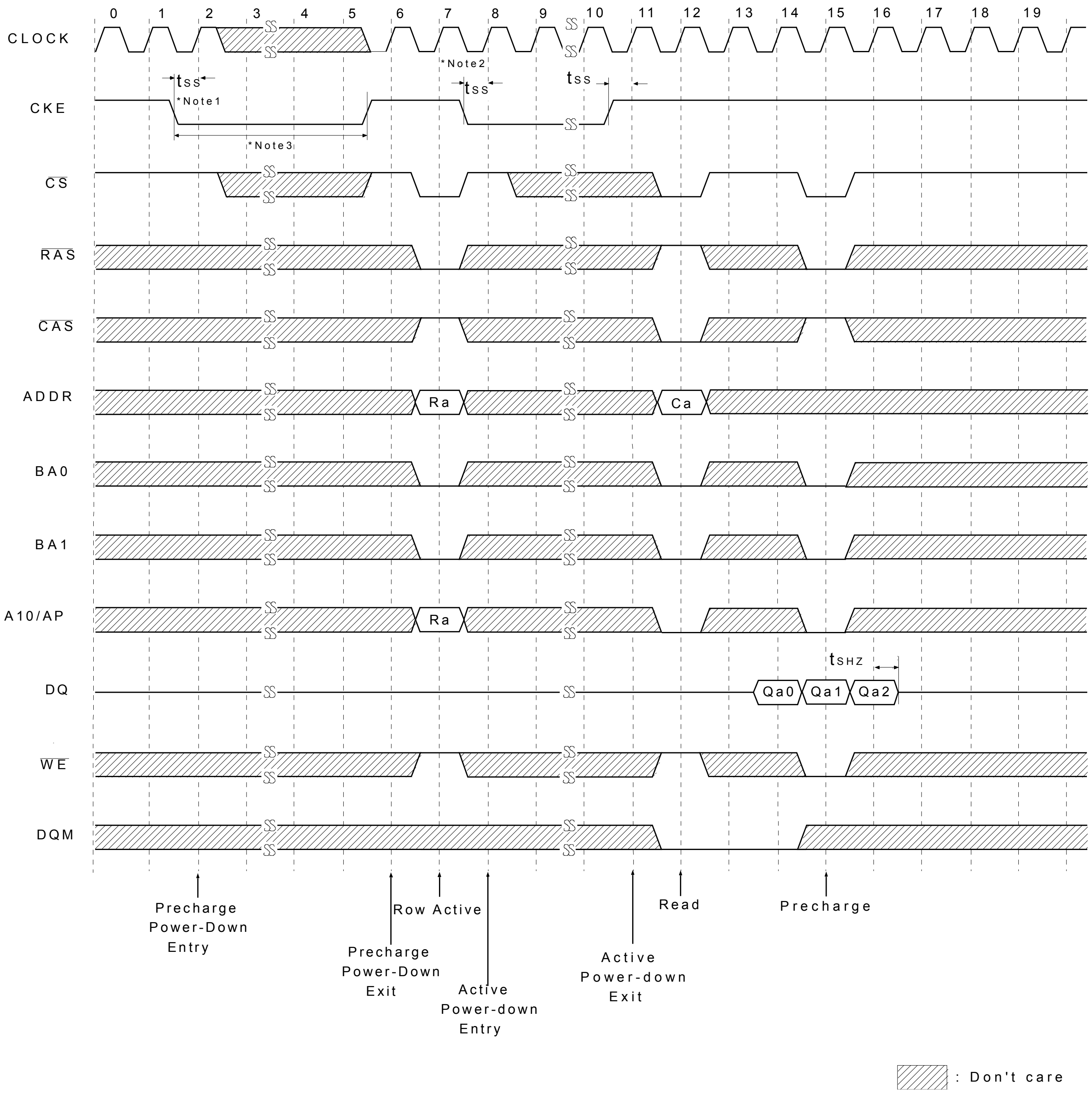
*Note : 1. About the valid DQs after burst stop, it is same as the case of $\overline{\text{RAS}}$ interrupt.
Both cases are illustrated above timing diagram. See the label 1,2 on them.
But at burst write, Burst stop and $\overline{\text{RAS}}$ interrupt should be compared carefully.
Refer the timing diagram of "Full page write burst stop cycles".
2. Burst stop is valid at every burst length.

Write interrupted by Precharge Command & Write Burst Stop Cycle @ Burst Length = Full page



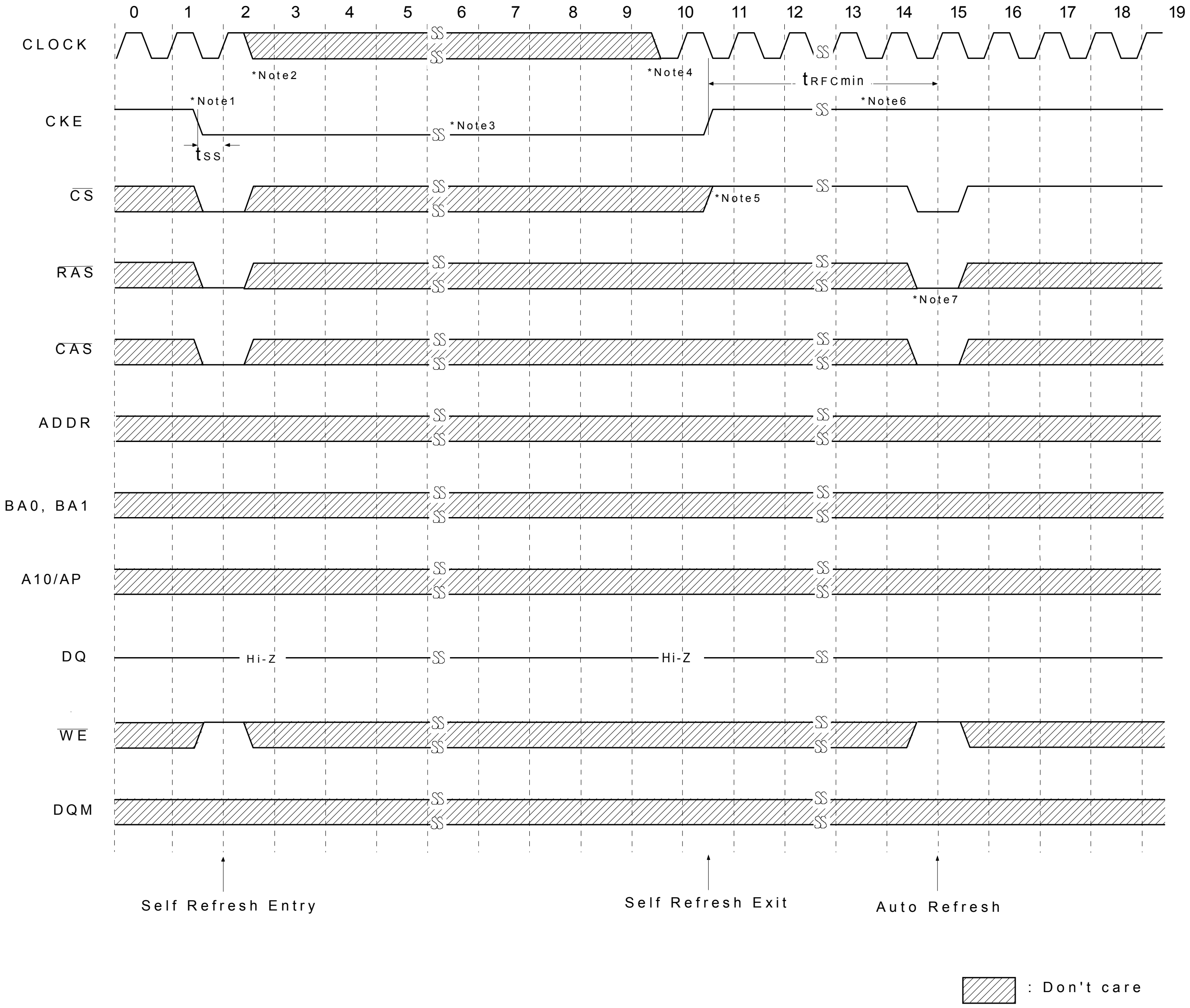
*Note : 1. Data-in at the cycle of interrupted by precharge can not be written into the corresponding memory cell. It is defined by AC parameter of t_{RDL}.
DQM at write interrupted by precharge command is needed to prevent invalid write.
DQM should mask invalid input data on precharge command cycle when asserting precharge before end of burst. Input data after Row precharge cycle will be masked internally.
2. Burst stop is valid at every burst length.

Active/Precharge Power Down Mode @ CAS Latency = 2, Burst Length = 4



*Note:
1. Both banks should be in idle state prior to entering precharge power down mode.
2. CKE should be set high at least 1CLK + t_{SS} prior to Row active command.
3. Can not violate minimum refresh specification. (64ms)

Self Refresh Entry & Exit Cycle



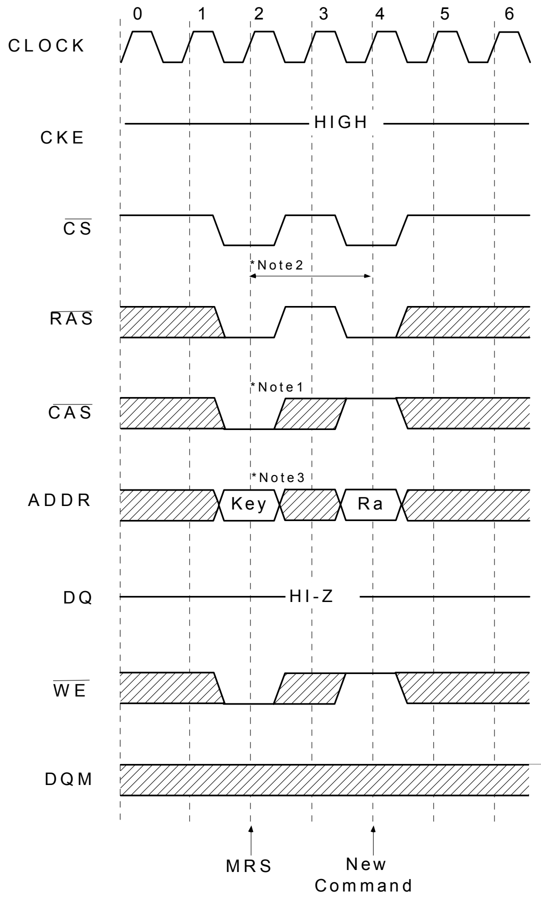
*Note : **TO ENTER SELF REFRESH MODE**

1. $\overline{\text{CS}}$, $\overline{\text{RAS}}$ & $\overline{\text{CAS}}$ with CKE should be low at the same clock cycle.
2. After 1 clock cycle, all the inputs including the system clock can be don’t care except for CKE.
3. The device remains in self refresh mode as long as CKE stays “Low”.
   cf.) Once the device enters self refresh mode, minimum t_{RAS} is required before exit from self refresh.

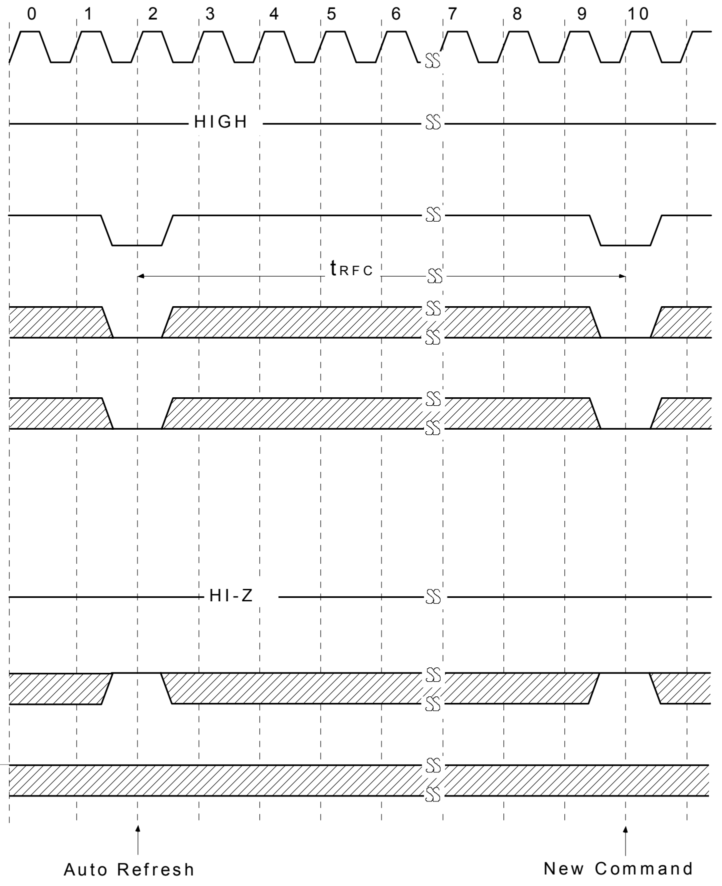
TO EXIT SELF REFRESH MODE

4. System clock restart and be stable before returning CKE high.
5. $\overline{\text{CS}}$ starts from high.
6. Minimum t_{RFC} is required after CKE going high to complete self refresh exit.
7. Burst auto refresh is required before self refresh entry and after self refresh exit if the system uses burst refresh.

Mode Register Set Cycle



Auto Refresh Cycle



▨ :Don't Care

All banks precharge should be completed before Mode Register Set cycle and auto refresh cycle.

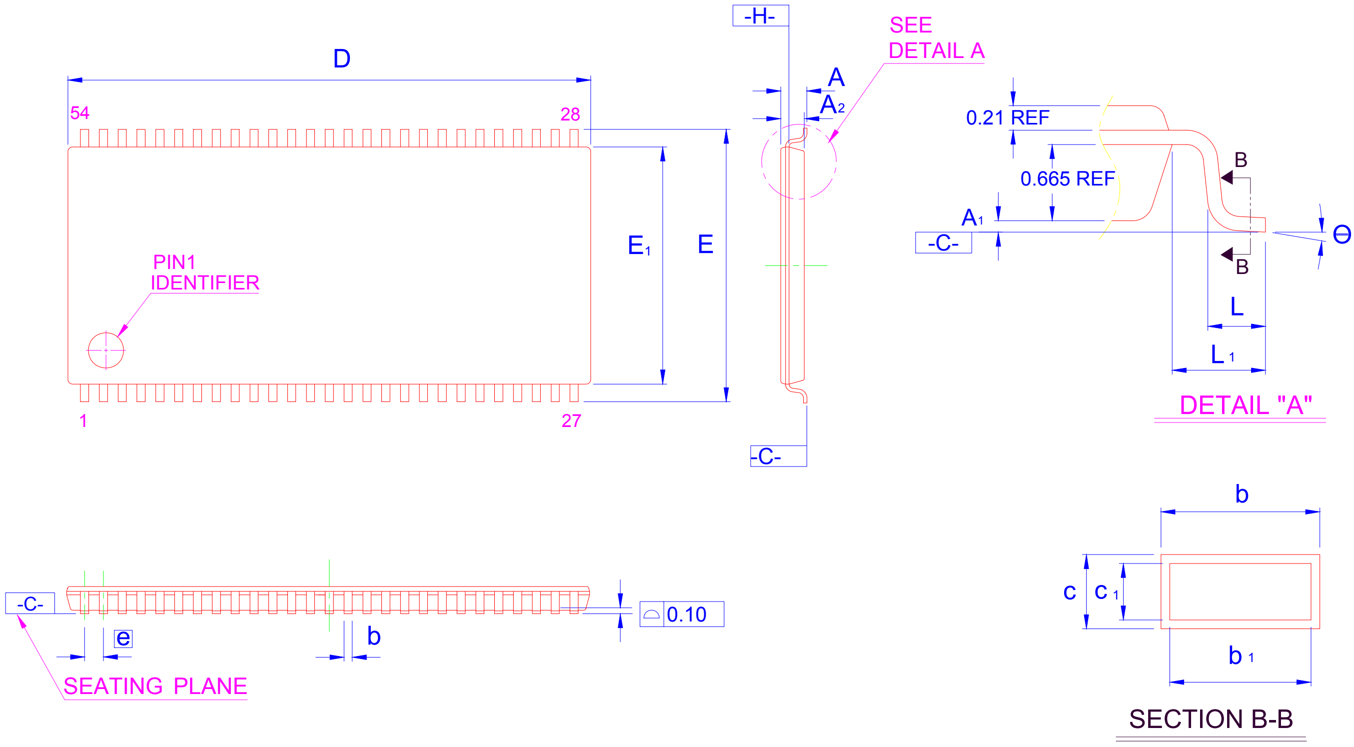
MODE REGISTER SET CYCLE

*Note : 1. $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, & $\overline{WE}$ activation at the same clock cycle with address key will set internal mode register.

2. Minimum 2 clock cycles should be met before new $\overline{RAS}$ activation.

3. Please refer to Mode Register Set table.

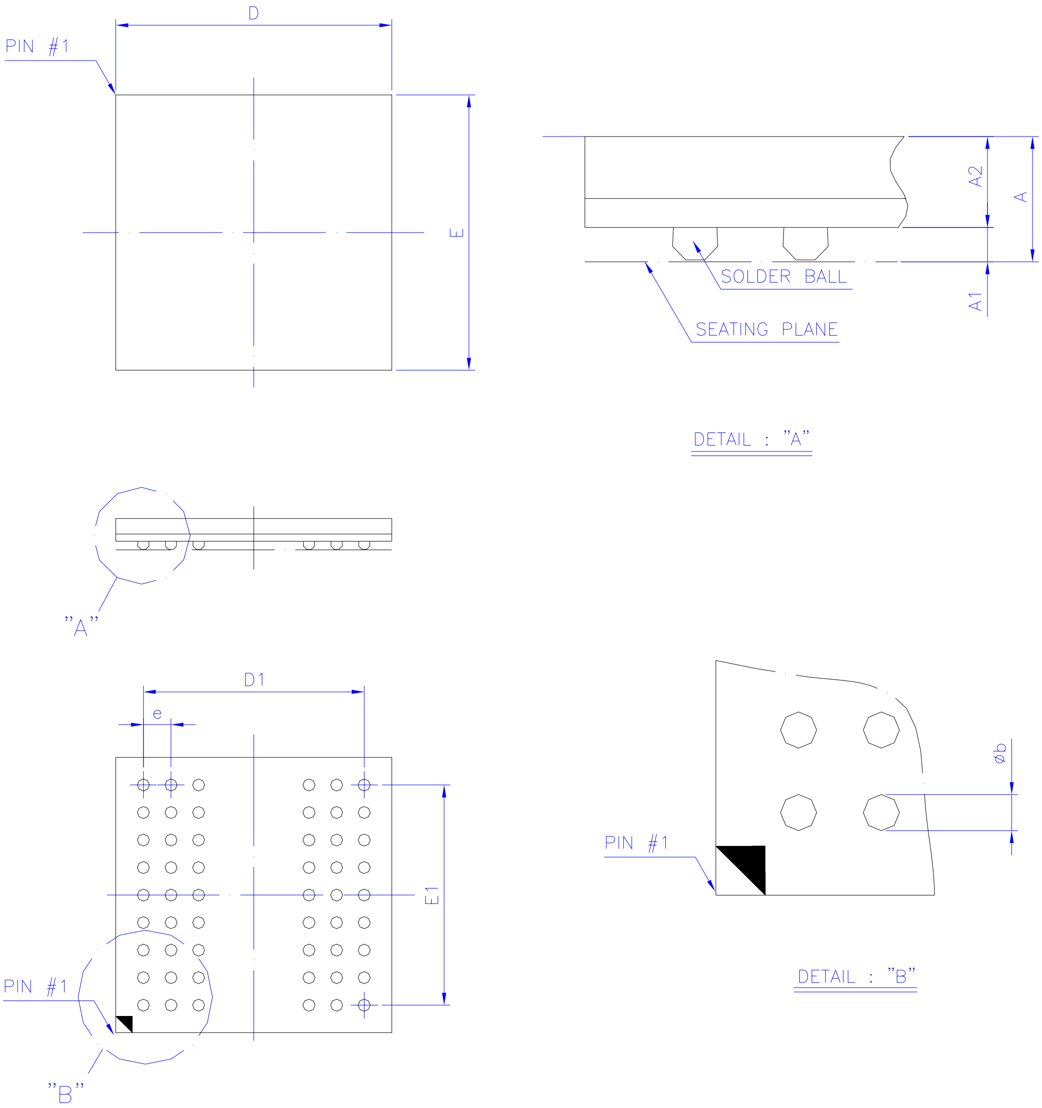
PACKING DIMENSIONS
54-LEAD TSOP(II) SDRAM (400mil) (1:3)



Symbol	Dimension in mm			Dimension in inch		
	Min	Norm	Max	Min	Norm	Max
A	——	——	1.20	——	——	0.047
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.25	——	0.45	0.010	——	0.018
b1	0.25	0.35	0.40	0.010	0.014	0.016
c	0.12	——	0.21	0.005	——	0.008
c1	0.10	0.127	0.16	0.004	0.005	0.006
D	22.22 BSC			0.875 BSC		
E	11.76 BSC			0.463 BSC		
E1	10.16 BSC			0.400 BSC		
L	0.40	0.50	0.60	0.016	0.020	0.024
L1	0.80 REF			0.031 REF		
e	0.80 BSC			0.031 BSC		
Θ	0°	——	10°	0°	——	10°

PACKING DIMENSIONS

54-BALL SDRAM (8x8 mm)



Symbol	Dimension in mm			Dimension in inch		
	Min	Norm	Max	Min	Norm	Max
A	——	——	1.00	——	——	0.039
A_1	0.20	0.25	0.30	0.008	0.010	0.012
A_2	0.61	0.66	0.71	0.024	0.026	0.028
Φ_b	0.30	0.35	0.40	0.012	0.014	0.016
D	7.90	8.00	8.10	0.311	0.315	0.319
E	7.90	8.00	8.10	0.311	0.315	0.319
D_1	——	6.40	——	——	0.252	——
E_1	——	6.40	——	——	0.252	——
e	——	0.80	——	——	0.031	——

Controlling dimension : Millimeter.

Important Notice

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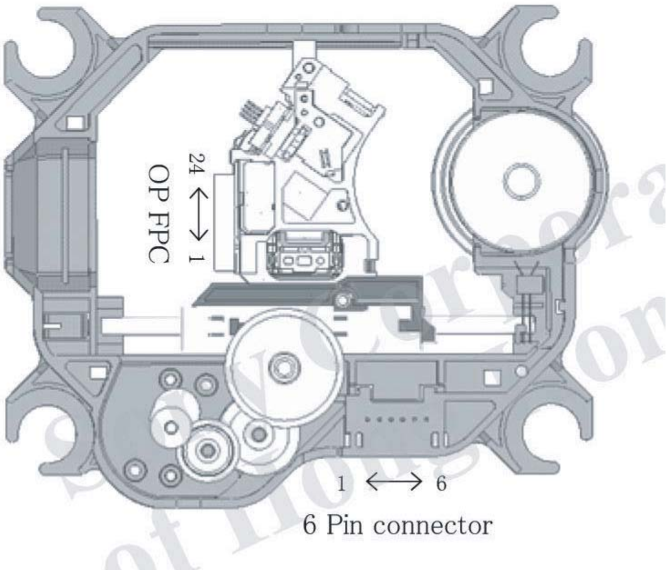
2. Reference Information

2-1 Component Descriptions

2-1-1 DVD SONY HM-313 PUH

Connector Pin Definition



Terminal of FPC connector for OP

Pin No.	Name
1	FCS-
2	FCS+
3	TRK+
4	TRK-
5	C/c
6	D/d
7	MSW
8	RF
9	A/a
10	B/b
11	F
12	GND
13	Vc
14	Vcc
15	E
16	N/C
17	CD VR
18	DVD VR
19	CD LD
20	PD
21	N/C
22	N/C
23	DVD LD
24	LD GND

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Ambient Temperature	TA	0 ~ 70	°C
Storage Temperature	TSTG	-55 ~ 125	°C
Voltage on Any Pin relative to VSS	VIN, VOUT	-1.0 ~ 4.6	V
Voltage on VDD relative to VSS	VDD, VDDQ	-1.0 ~ 4.6	V
Short Circuit Output Current	IOS	50	mA
Power Dissipation	PD	1	W
Soldering Temperature · Time	TSOLDER	260 · 10	°C · Sec

Note : Operation at above absolute maximum rating can adversely affect device reliability

DC OPERATING CONDITION (TA=0 to 70°C)

Parameter	Symbol	Min	Typ.	Max	Unit	Note
Power Supply Voltage	VDD, VDDQ	3.0	3.3	3.6	V	1,2
Input High Voltage	VIH	2.0	3.0	VDDQ + 2.0	V	1,3
Input Low Voltage	VIL	VSSQ - 2.0	0	0.8	V	1,4

Note :
1.All voltages are referenced to VSS = 0V
2.VDD(min) of HY57V641620HG(L)T-5/55/6 is 3.135V
3.VIH (max) is acceptable 5.6V AC pulse width with ≤3ns of duration
4.VIL (min) is acceptable -2.0V AC pulse width with ≤3ns of duration

AC OPERATING CONDITION (TA=0 to 70°C, VDD=3.3 ± 0.3V$^{\text{Note2}}$, VSS=0V)

Parameter	Symbol	Value	Unit	Note
AC Input High / Low Level Voltage	VIH / VIL	2.4/0.4	V	
Input Timing Measurement Reference Level Voltage	Vtrip	1.4	V	
Input Rise / Fall Time	tR / tF	1	ns	
Output Timing Measurement Reference Level	Voutref	1.4	V	
Output Load Capacitance for Access Time Measurement	CL	50	pF	1

Note :
1. Output load to measure access time is equivalent to two TTL gates and one capacitor (50pF)
   For details, refer to AC/DC output circuit
2.VDD(min) of HY57V641620HG(L)T-5/55/6 is 3.135V

3. Product S pecifications

Power supply		AC ~230V/50Hz
Power consumption		105W
Working environment	Temperature	-10~+40℃
	Relative humidity	5%~90%
Disc output	TV System	PAL/NTSC
	Frequency Reponse	±1.5dB(20Hz~20KHz)
	S/N(A weight)	＞80dB(1KHz)
	Dynamic Range	⩾70dB(1KHz)
	THD+NOISE	⩽ - 60dB(1KHz)
Tuner	AM frequency Range	/
	FM band Range	64MHz ~108MHz
Power output (Max)		15WX5+30W
Frequency response		± 1.5dB(20Hz~20KHz)

4. Upgrading System and Changing the Region Code

MTK upgrade:

1. Name upgrade file as "MTK.BIN"(must be in big caps)
2. Record it in a CD-R/W (It can be enclosed a sub-directory which size is about 30M, and the file content can be letter or non used file.)
   disc Format: (advise to use the tool NERO burning ROM)
   Disc volume: MEDIATEK, ISO9660 LEVEL1, MODE1，not JOILET.

3. Put the recorded disc into the DVD player, on the TV will show "upgrade?" after loading. Press PLAY button, the player will automatically upgrade.
4. Do not shut down the player during upgrade, it will restart automatically after upgrade.
5. Upgrade finish!

How to change the region code:

1. Power on the machine, and press OPEN button to push the tray out.
2. Press "1.3.6.9" buttons,the TV display “XXXX”, you can change the region code to 0-6 with 0-6 button, the number 0 means REGION FREE.

5. Operating Instruction

Please refer to the User's Manual for the operating instruction of the system.

Maintenance & Troubleshooting

How to handle discs

To handle, clean and protect discs

- Do not touch the playing side of a disc

- Do not stick any paper or glue strip on a disc.

How to clean discs

- Finger prints and dust on surface can affect the sound and picture quality. Clean discs regularly with a soft cotton cloth from disc center to outside.

- For sticky dust, wipe it with wet cloth and with dry cloth, Any kind of solvent, such as diluting agent, gasoline, liquid detergent, gasoline liquid detergent anti – static aerosol used for vinylon LP, may cause disc damage.

How to protect discs

- Keep away from the direct sunshine or any heat source.
- Do not put discs in damp or dirty places, such as bathroom or near humidifiers. Store discs vertically in disc box and store in a dry place. Piling discs on to top of each other or excess weight load on disc box may cause the disc to warp.

Disc Compatibility

- Some DVD discs may have special requirements for playing, with which this player may not be compatible. Please refer to specifications on individual disc.

DISC TYPE	Content	Size	Total Play time
DVD	AUDIO/ VIDEO	12CM	About 2hrs. (Single side & single layer)
			About 4hrs. (Single side & double layer)
			About 4hrs. (Double side & Single layer)
			About 8hrs. (Double side & double layer)
CD-DA	AUDIO	12CM	About 74 minutes
MP3	AUDIO	12CM	About 300 minutes

Discs types

This DVD player can play the following types of discs: Discs other than listed above cannot be player by this player.
This player uses NTSC/PAL color system. It cannot play discs recorded with other systems, such as SECAM.

Region code

When play the region disc with player unconf -ormity,the screen display "WRONG REGION", you can change the region code,please referr -ence the "How to change the region code".

Copyright

According to the related law, DVD discs without proper authorization are not allowed to be copied broadcast cable broadcast, played publicly or rented. As DVD discs are anti-piracy the copied content is distorted.

TV system

Connect this player to a PAL/NTSC compatible TV.

6.Problems and Solutions

If a fault occurs, first check the points listed below before taking the set for repair.

If you are unable to remedy a problem by following these hints, consult your dealer or service centre.

WARNING: Under no circumstances should you try to repair the set yourself, as this would invalidate the guarantee.

Problems	Cause	Solution
No power indication	**Power plug not connected**	**Plug the power cord into the power supply**
No picture	**TV has not been set to the correct video input**	**Set correct TV video input format for receiving the player's output signals.**
	Video cable not firmly connected.	**Firmly insert the video cable ends to the related terminals.**
No sound	**Audio cable not connected tightly**	**Firmly insert the audio cable ends to the related terminals.**
	Power of audio apparatus is off	**Turn on the power of audio apparatus.**
	Audio output setting is incorrect	**Setup audio output correctly via the setup menu.**
Picture distortion	**Disc is dirty**	**Take out the disc and clean.**
	Fast forward/backward is activated	**The picture may be distorted during fast forward /backward playback.**
Brightness unstable or noisy	**Affected by anti-piracy circuit**	**Connect the player directly to TV.**
The player does not work	**No disc**	**Load a disc.**
	Disc not compatible	**Load a compatible disc (Check the disc format and its colour system).**
	The disc is placed upside down	**Load a compatible disc (Check the disc format and its colour system).**
	The disc not put in the tray correctly	**Check disc is put in correctly.**
	Disc is dirty	**Clean the disc.**
	Player setting are incorrect	**Change the setting via the setup menu.**
	Parental lock is in effect	**Disable this function or reset the rating level.**
No response to key press	**Interference of power wave or other factors such as static interference**	**Turn off the main switch or pull out the power plug, plug it in and turn on the power again.**
Remote control does not work	**The remote control not pointed at the remote sensor on the front panel of the player**	**Point the remote control at the remote sensor.**
	The remote control is out of specified range	**Make sure the remote control range within 7 meters to the remote sensor.**
	Battery power exhausted	**Replace with new batteries.**

Note:

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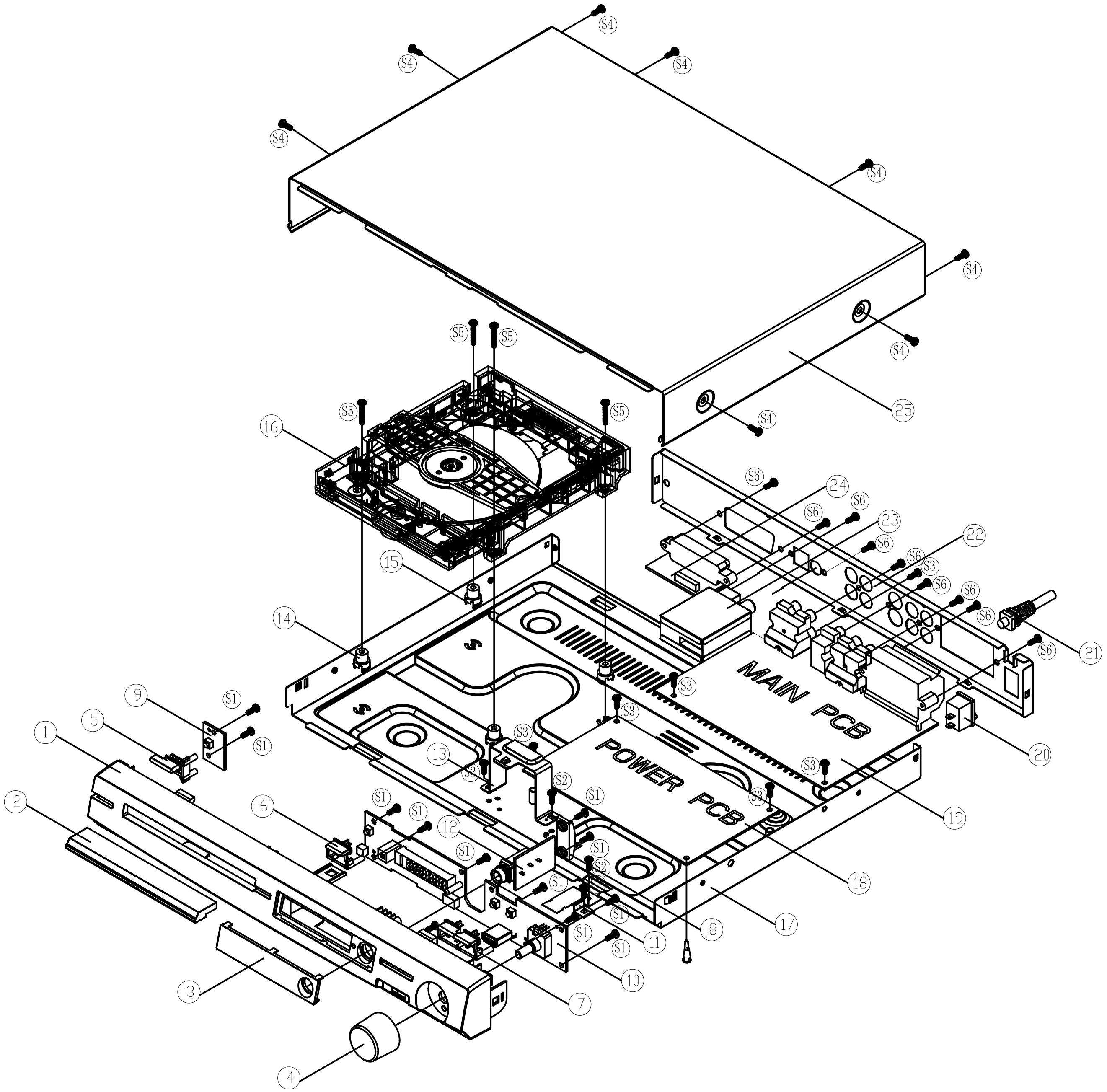


Client	
LOGO	
MODEL	

Item	Description	Qty	Item	Description	Qty
20	Power Switch	1		Bolt	
19	Decode Board	1	S1	PT3× 8PBHNi+	11
18	Power Board	1	S2	3× 4PWMHNi+	4
17	Bottom	1	S3	3× 6PMHNi+	6
16	Mechanism Ass'y	1	S4	3× 6PWMHBNi+	8
15	Plastic pillar H=10	2	S5	3× 17PWMHNi+	4
14	Plastic pillar H=9	2	S6	PT3× 8PBHNi+	9
13	Supporter1	1			
12	Mic Board	1			
11	Earthing Sheet	1			
10	Control Board	1			
9	Standby Board	1			
8	Mic Supporter	1			
7	Key-Press(PLAY/STOP)	1			
6	Key-Press(open/close)	1			
5	Key-Press(standby)	1	25	Cover	1
4	Volume Knob	1	24	SCART Board	1
3	Lens	1	23	Radio Ass'y	1
2	CD Door	1	22	Back Board	1
1	Panel	1	21	Power Line	1

COMMON1389J_HD850_AM5888_STBY

MT1389J DVD Board w/ Sanyo HD6x Series PUHs

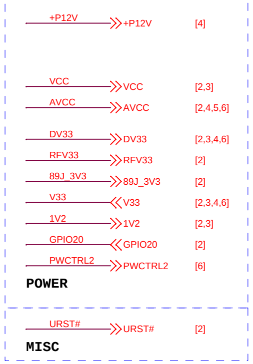
1 INDEX & POWER / RESET
2 MT1389J LQFP128
3 SDRAM & FLASH & MOTOR
4 AUDIO & MIC I/F
5 Video I/F
6 MCR & USB & GXYZ I/F
7 Power Flow

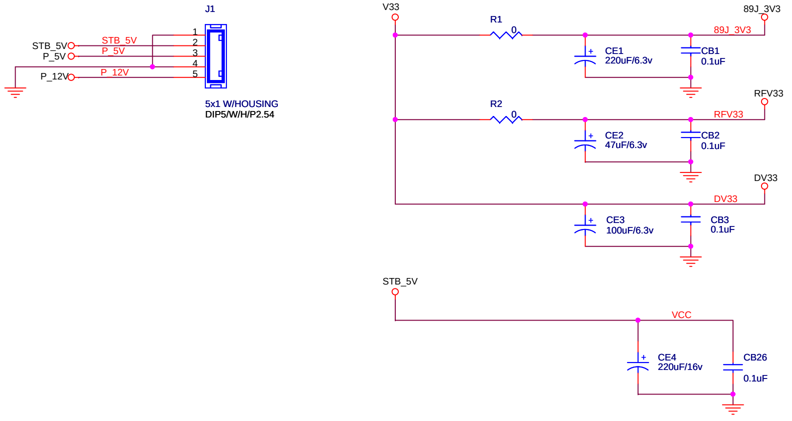
Rev	History	P#	Date
V1	Original release		2009.7.13
V1.1	Modify VR-CD and MDI circuit.		2009.7.30

MT1389J General GPIO List

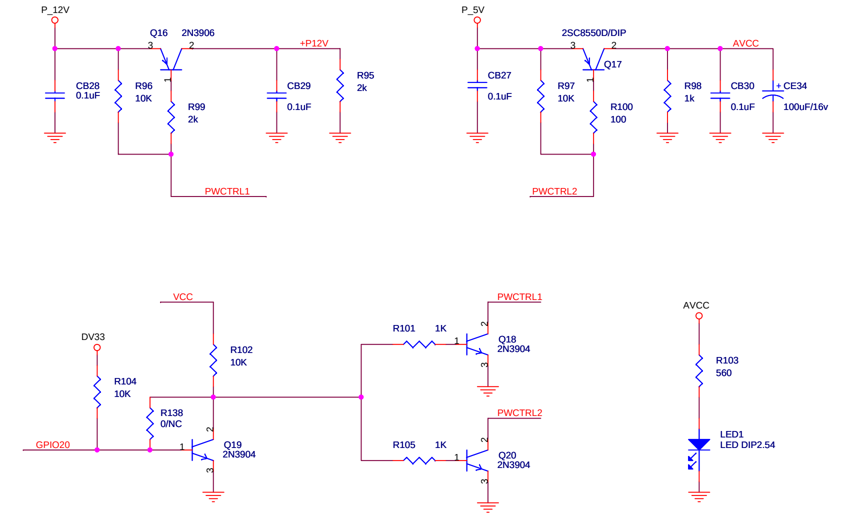
Name	PIN	Features		
GPO5	12	TRCLOSE		
MDI1	13	VR_CD		
GPO_B	20	VR_DVD		
GPIO2	23	TRIN		
UP1_6	34	VSCK		
UP1_7	35	VSDA		
GPIO11	36	Power Key		RXD
GPIO6	37	SD_D0		TXD
GPIO3	40	STBY		
GPIO4	41	TROPEN	IOA	
GPIO13	42	VSTB		
GPIO9	43	MS_D0	SD_CMD	
GPIO8	44	MS_BS	SD_CLK	
GPIO7	45	MS_CLK		
GPIO29	46	Gxyz_LOAD		
GPIO30	47	Gxyz_CLK		
GPIO31	48	Gxyz_DA1		
GPIO32	49	Gxyz_DA2		
GPIO12	93	ASPDIF		
GPIO10	94	SCART1	HSYNC	
GPIO33	95	SCART2	VSYNC	
GPO14	97	AUDIO_MUTE		
GPIO19	106	AKIN2		
GPIO20	107	ADVCM		
GPIO21	108	AKIN1		
GPI36	124	LIMIT	TROUT	

OFF-PAGE CONNECTION

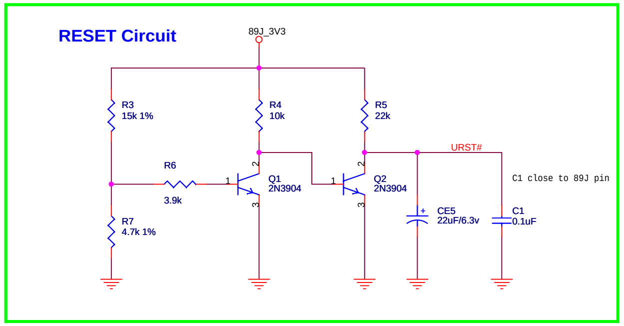


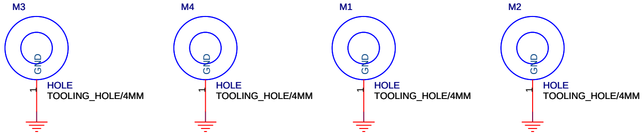


Standby Power Control



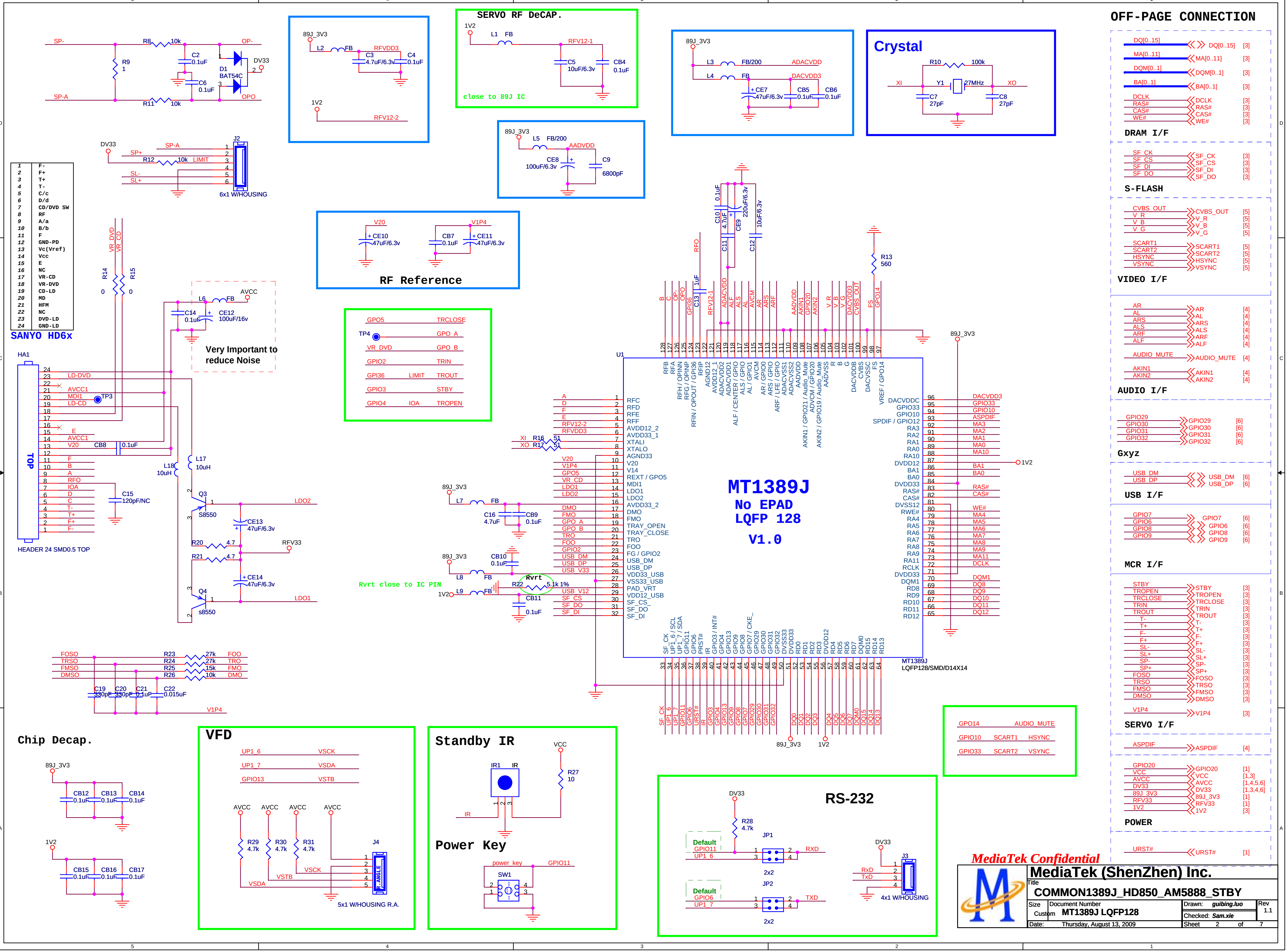
RESET Circuit





MediaTek Confidential

MediaTek (ShenZhen) Inc.
Title
COMMON1389J_HD850_AM5888_STBY
Size Custom
Document Number **INDEX / POWER / RESET**
Drawn: *guibing.luo*
Checked: *Sam.xie*
Rev 1.1
Date: Thursday, August 13, 2009
Sheet 1 of 7

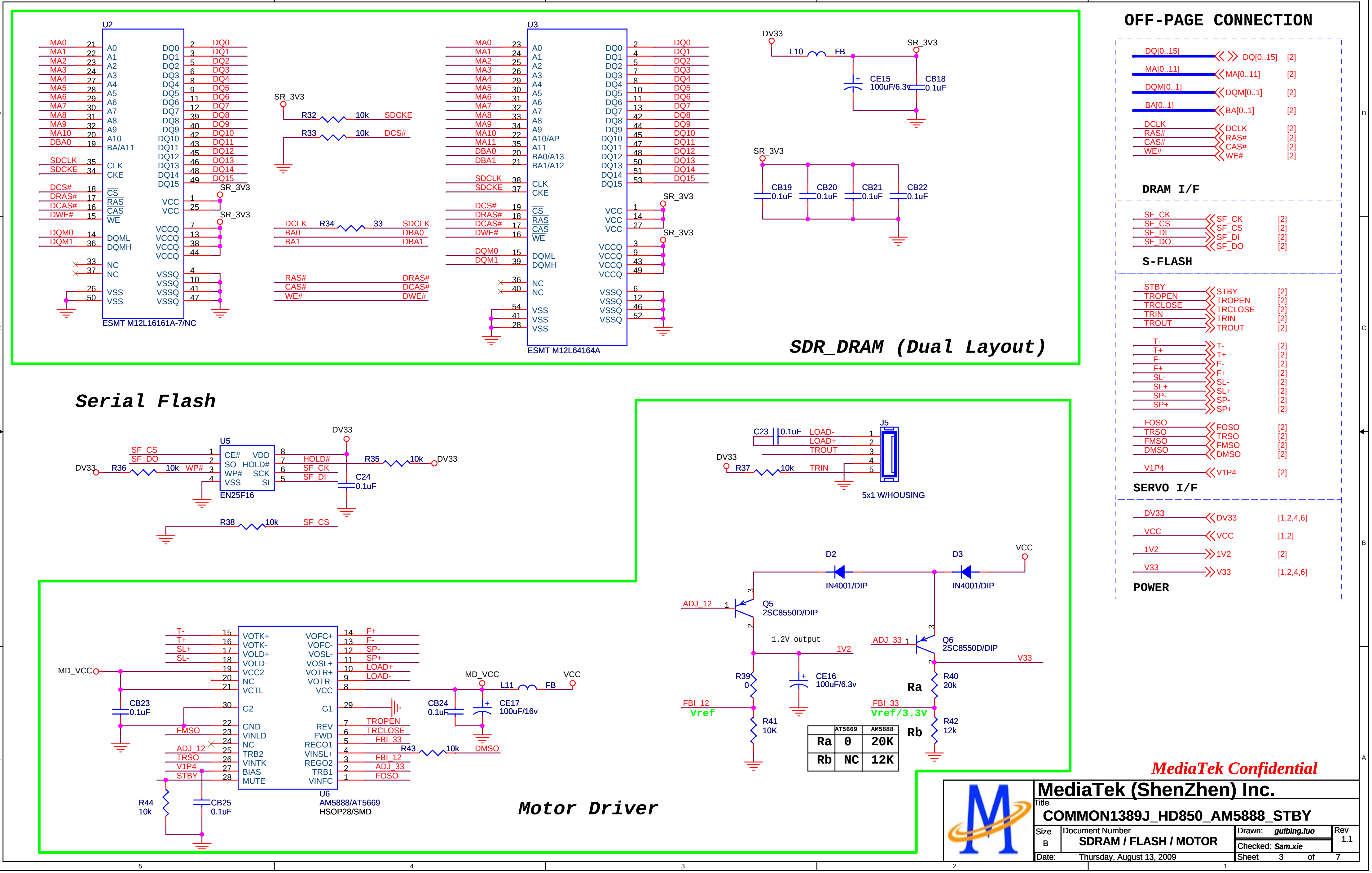


1	F-
2	F+
3	T+
4	T-
5	C/c
6	D/d
7	CD/DVD SW
8	RF
9	A/a
10	B/b
11	F
12	GND-PD
13	Vc(Vref)
14	Vcc
15	E
16	NC
17	VR-CD
18	VR-DVD
19	CD-LD
20	MD
21	HFM
22	NC
23	DVD-LD
24	GND-LD

MediaTek (ShenZhen) Inc.

Title
COMMON1389J_HD850_AM5888_STBY

Size: Custom
Document Number: MT1389J LQFP128
Drawn: guibing.luo
Checked: Sam.xie
Rev: 1.1
Date: Thursday, August 13, 2009
Sheet 2 of 7



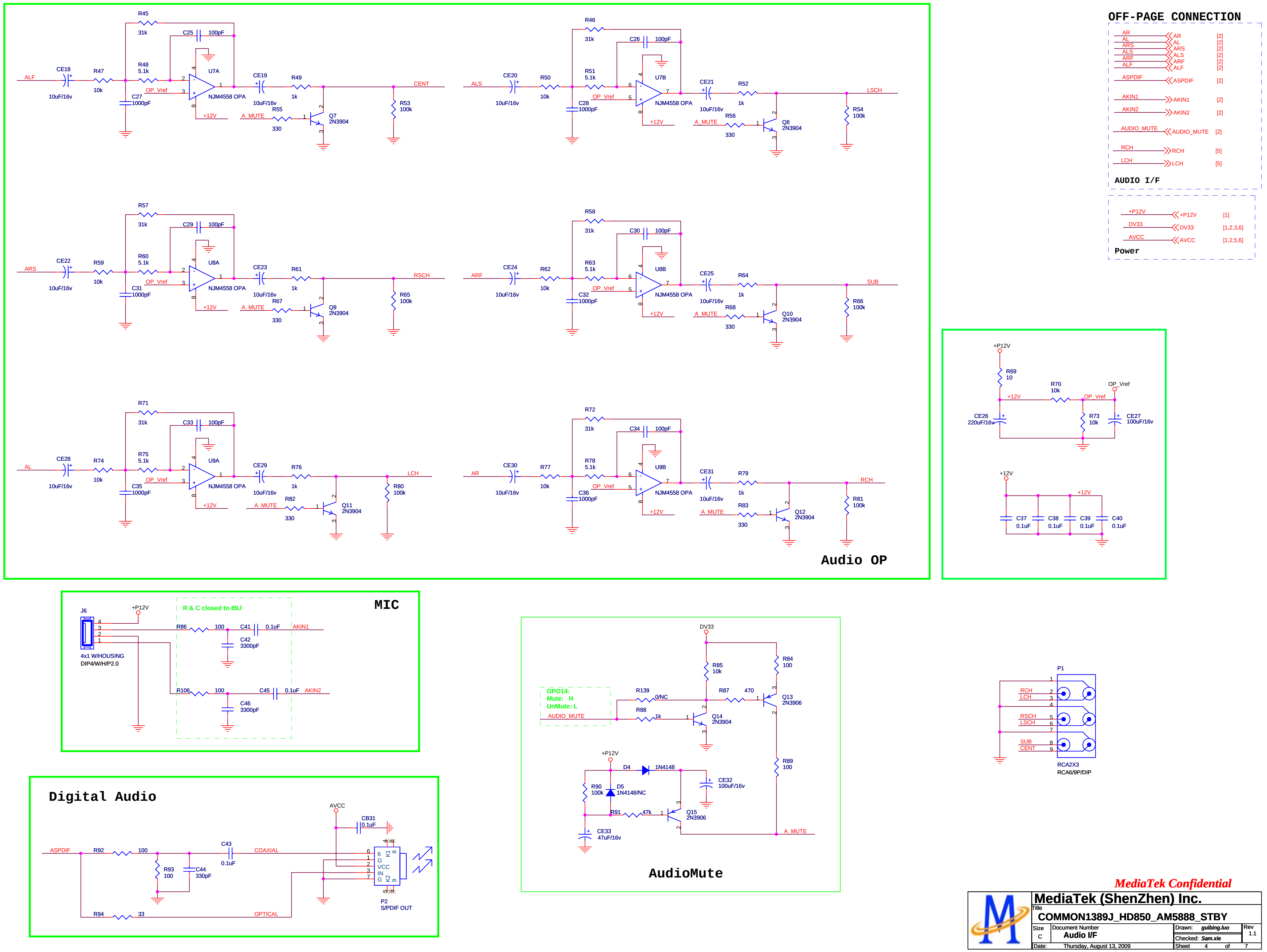
	AT5669	AM5888
Ra	0	20K
Rb	NC	12K

MediaTek Confidential

MediaTek (ShenZhen) Inc.

Title
COMMON1389J_HD850_AM5888_STBY

Size B
Document Number SDRAM / FLASH / MOTOR
Drawn: guibing.luo
Checked: Sam.xie
Rev 1.1
Date: Thursday, August 13, 2009
Sheet 3 of 7



MediaTek Confidential

MediaTek (ShenZhen) Inc.

Title
COMMON1389J_HD850_AM5888_STBY

Size	Document Number		Rev
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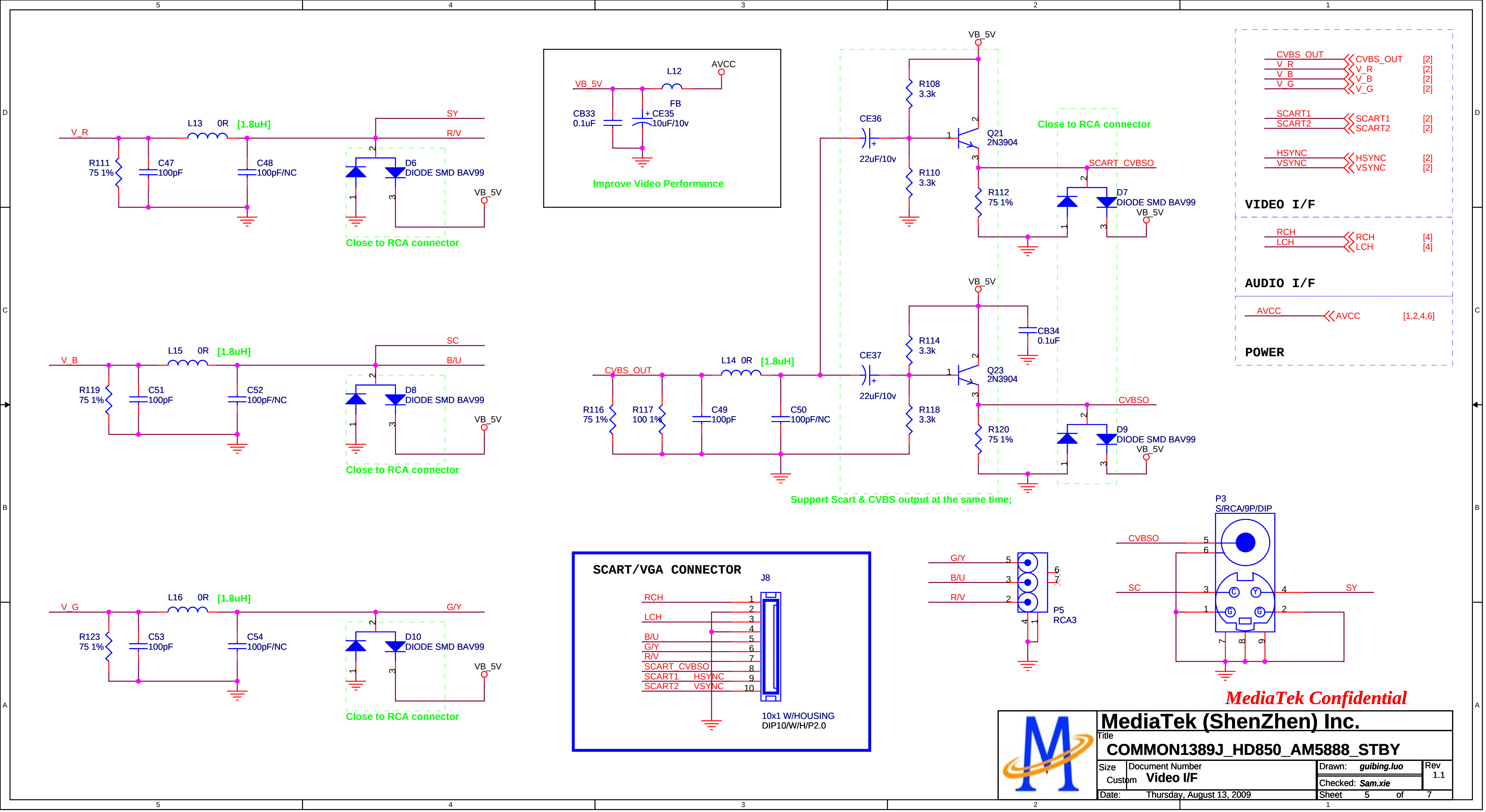
Date:	Thursday, August 13, 2009	Sheet 4 of 7	



MediaTek (ShenZhen) Inc.

Title: COMMON1389J_HD850_AM5888_STBY

Size	Document Number	Drawn: guibing.luo	Rev
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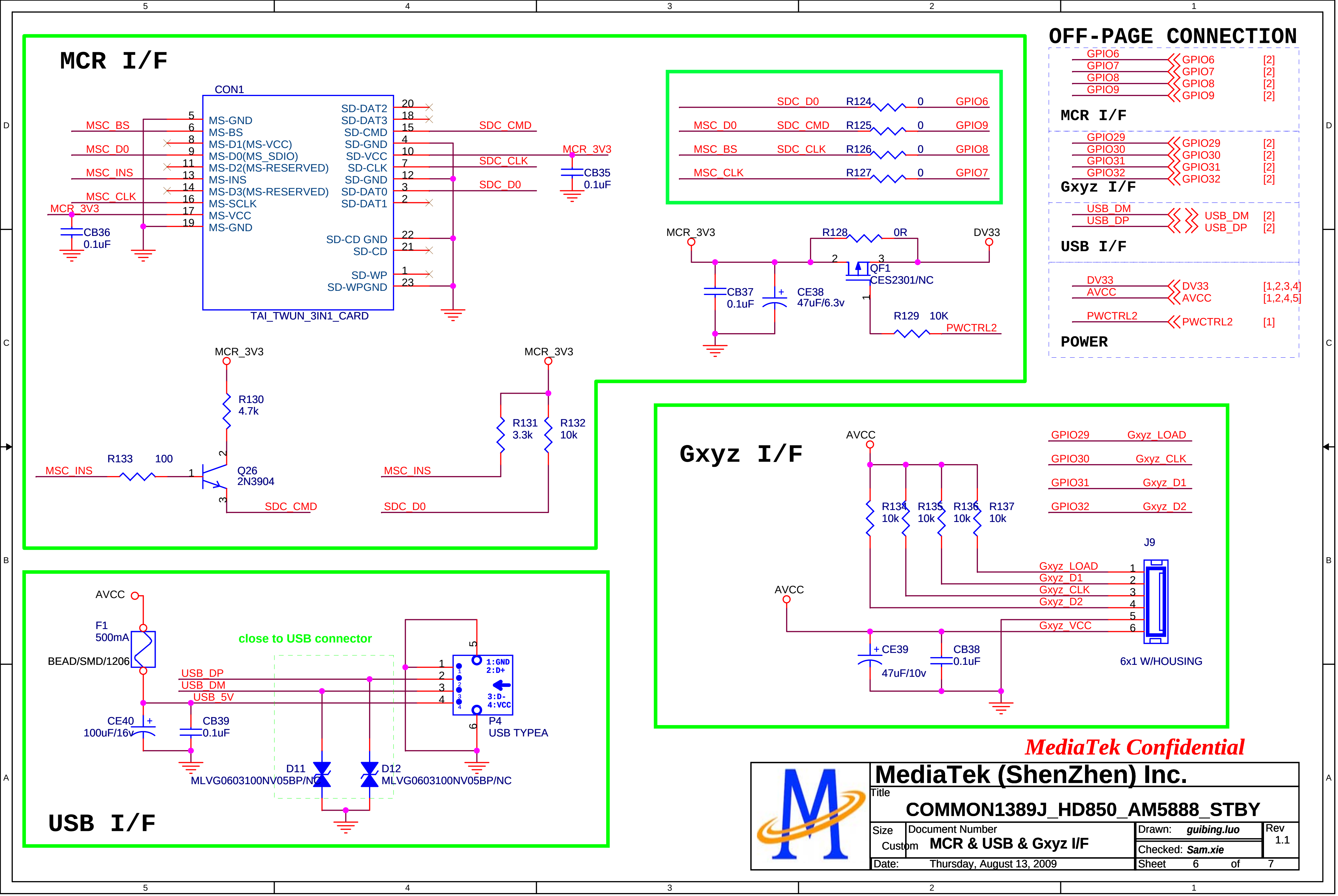
Date: Thursday, August 13, 2009		Sheet 5 of 7	



MediaTek (ShenZhen) Inc.

Title
COMMON1389J_HD850_AM5888_STBY

Size	Document Number	Drawn: guibing.luo	Rev
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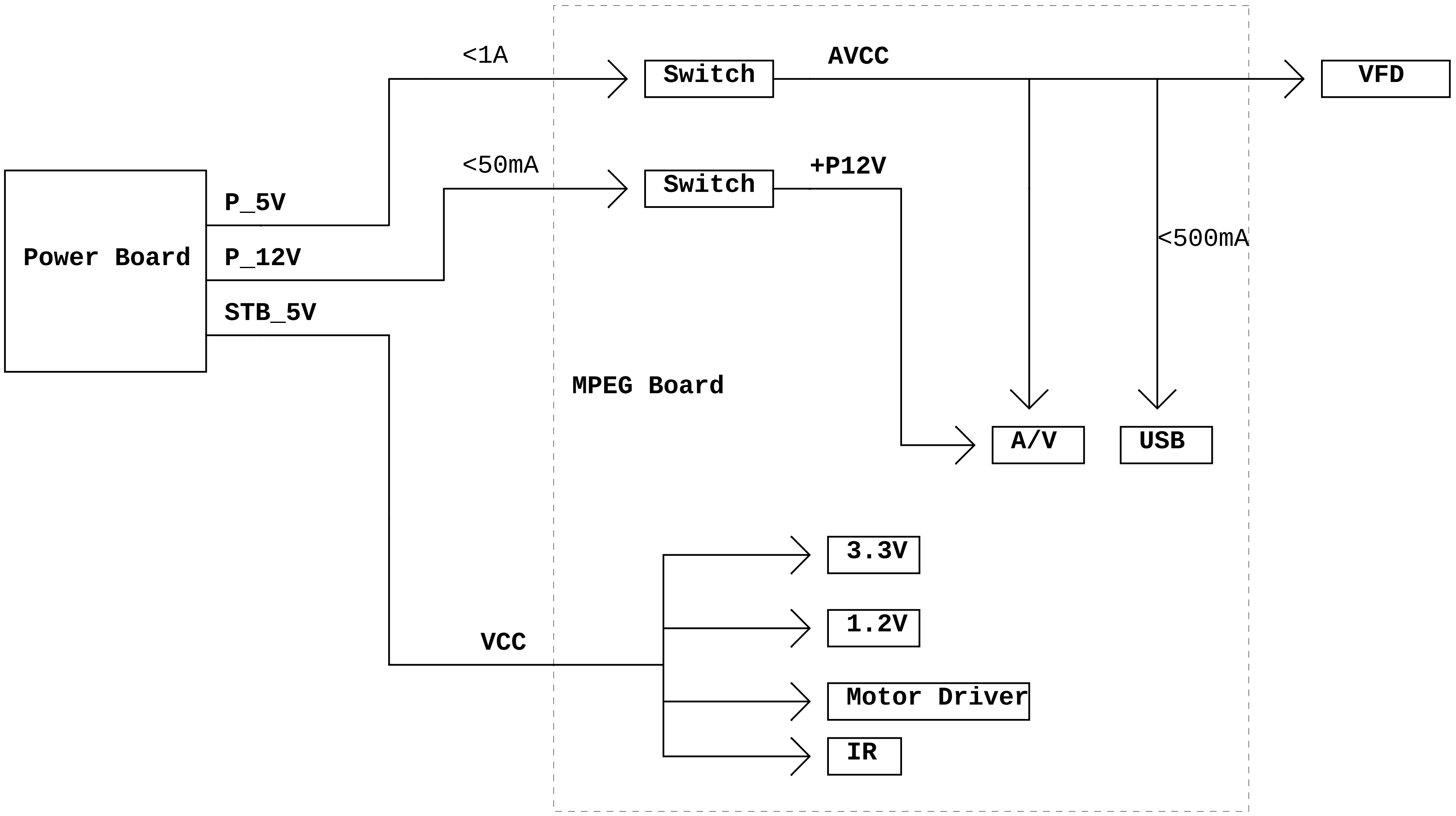
Date:	Thursday, August 13, 2009	Sheet 6 of 7	



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MediaTek (ShenZhen) Inc.

Title
COMMON1389J_HD850_AM5888_STBY

Size A
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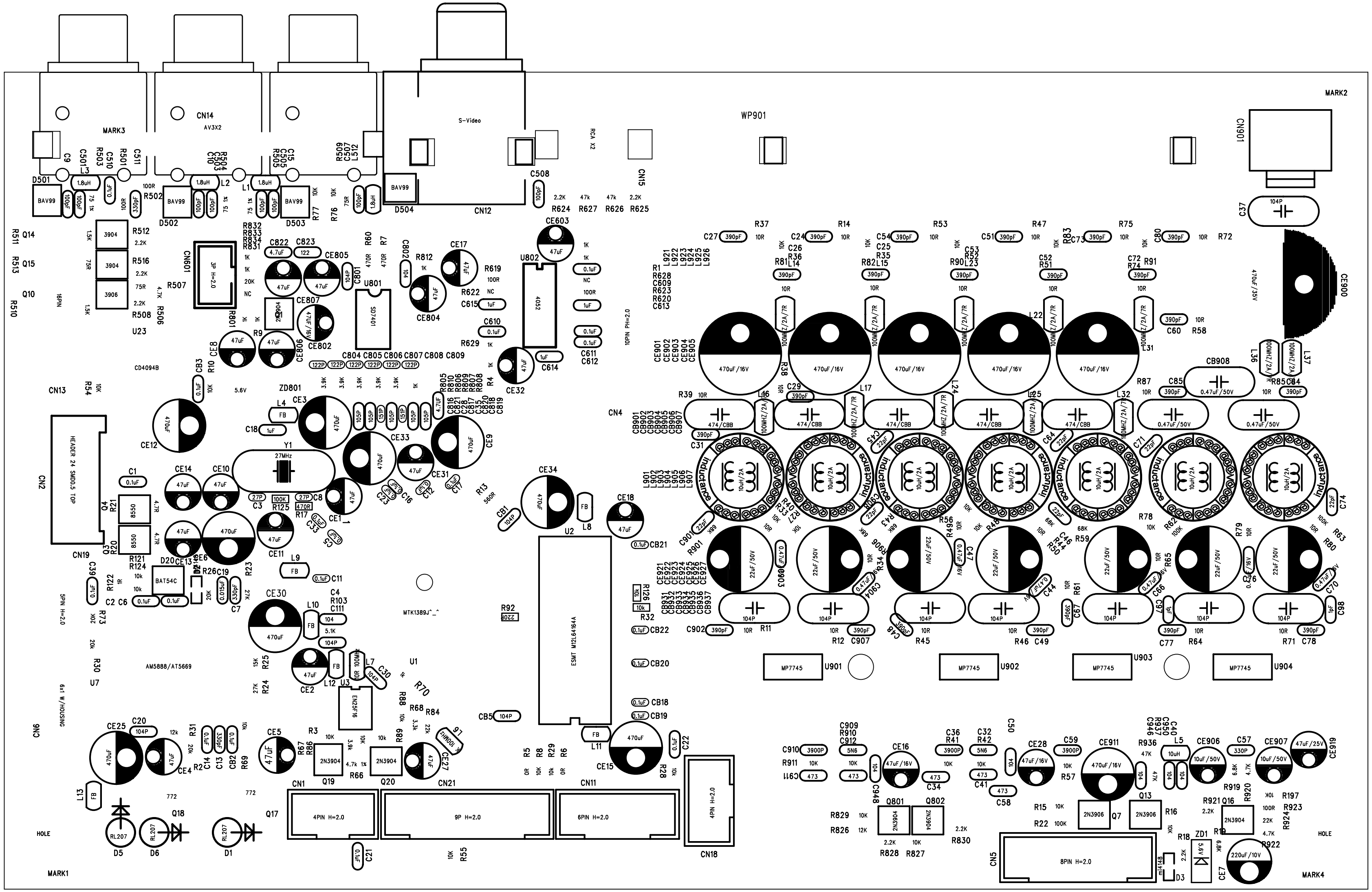
Checked: ***Sam.xie***
Rev 1.1
Date: Thursday, August 13, 2009
Sheet 7 of 7



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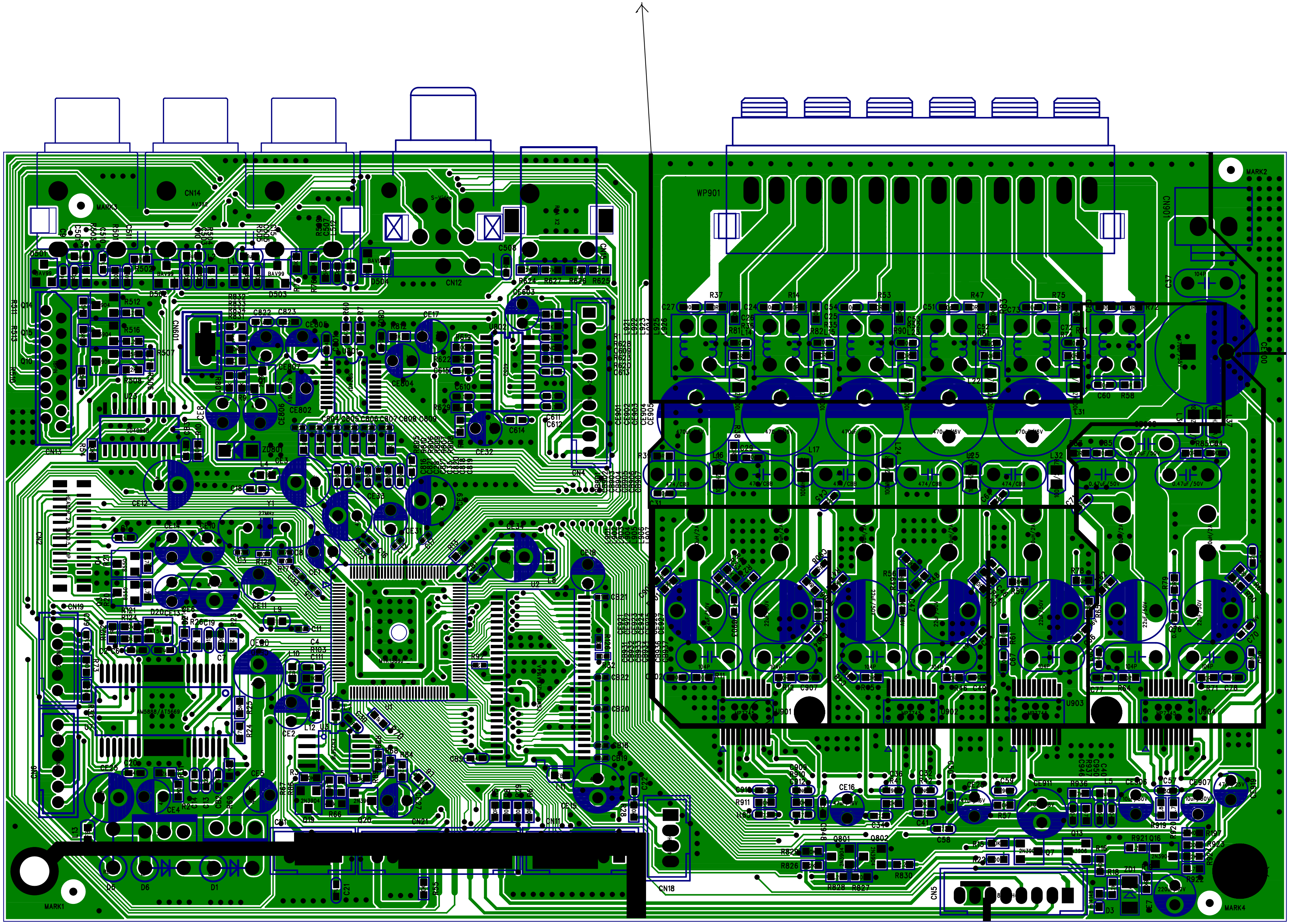

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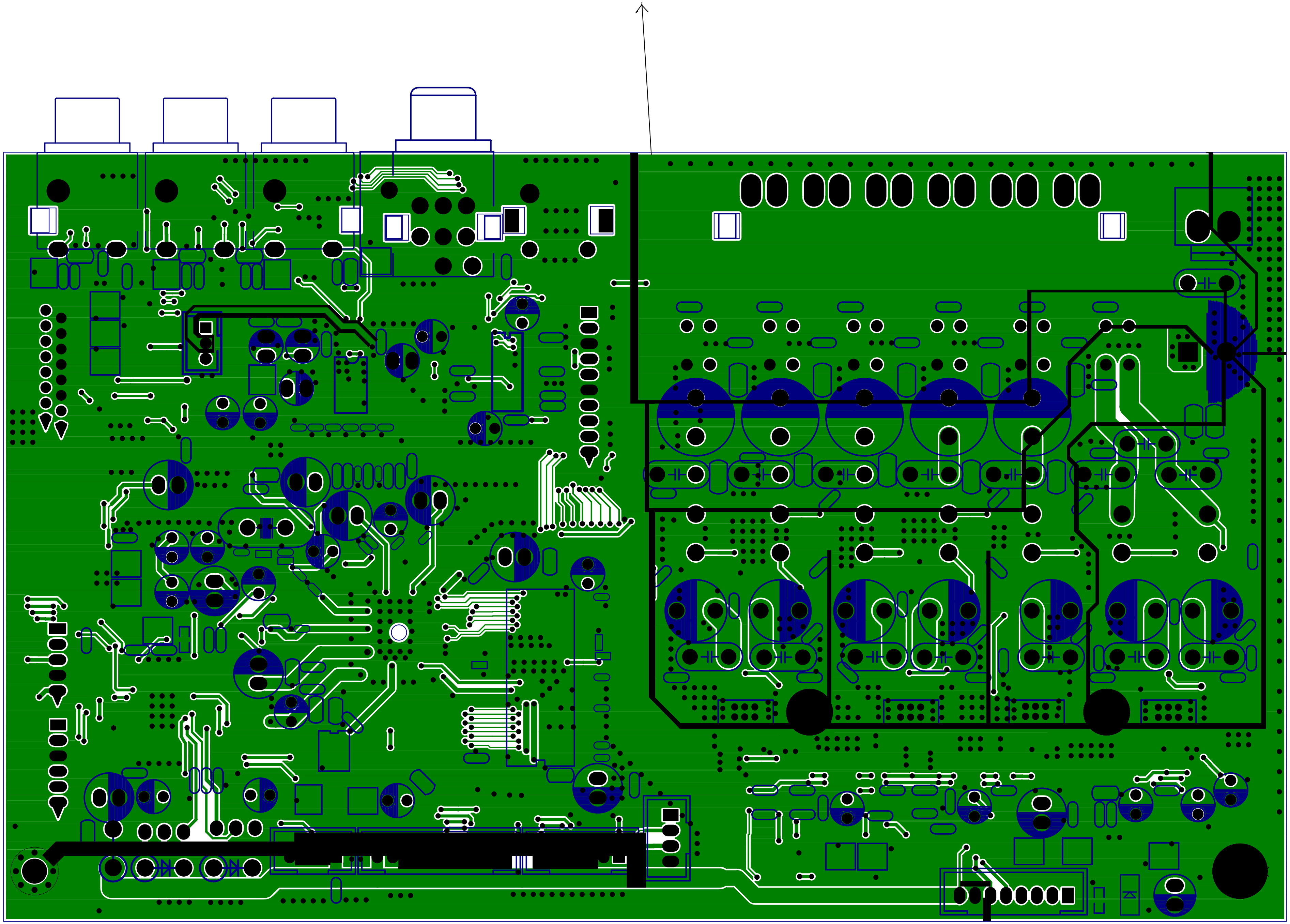

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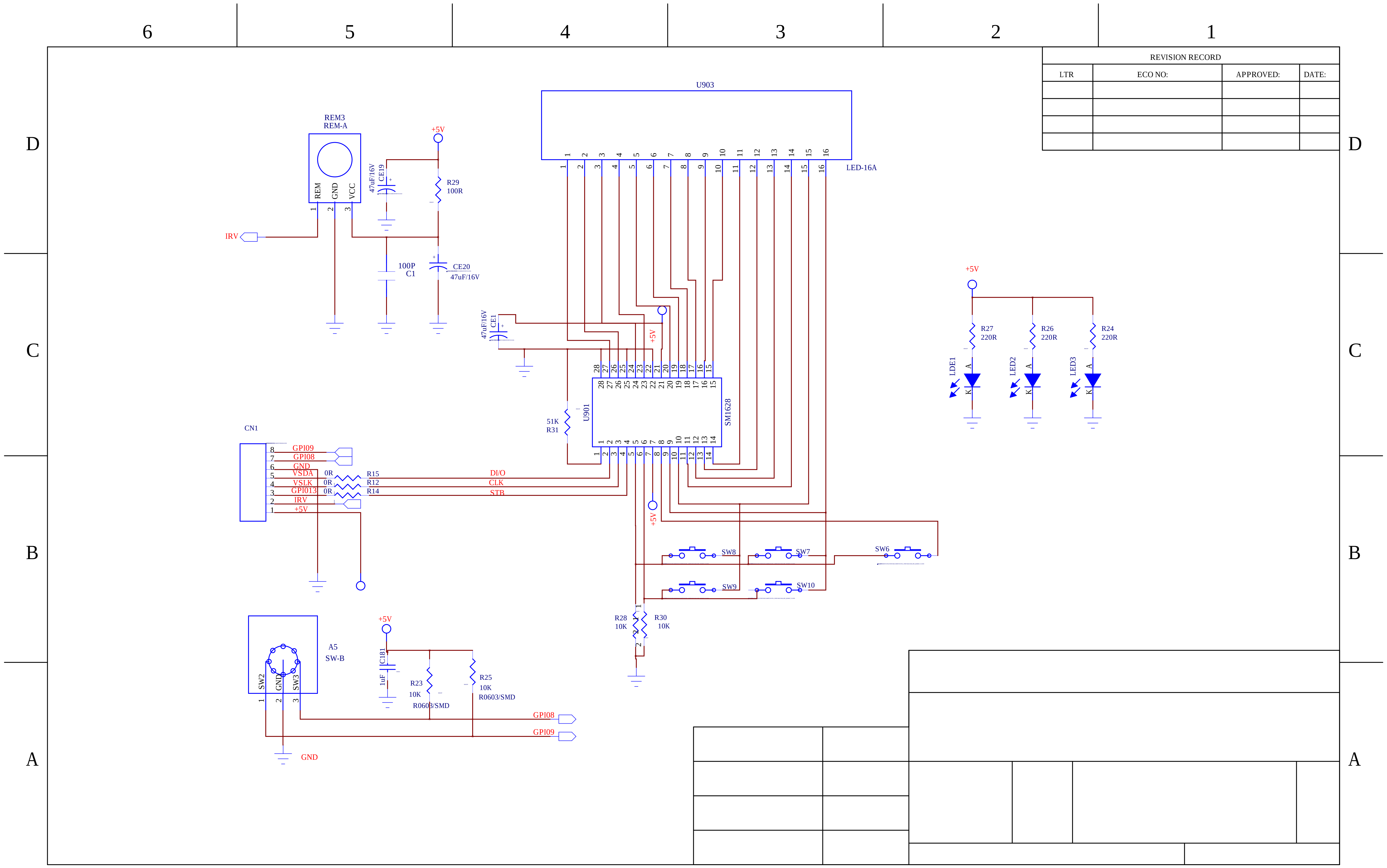
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5
4
3
2
1
D
C
B
A
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LTR
ECO NO:
APPROVED:
DATE:
U903
LED-16A
REM3
REM-A
REM
GND
VCC
IRV
+5V
47uF/16V
CE19
R29
100R
100P
C1
CE20
47uF/16V
CE1
47uF/16V
51K
R31
U901
SM1628
CN1
GPI09
GPI08
GND
VSDA
VSLK
GPI013
IRV
+5V
0R
0R
0R
R15
R12
R14
DI/O
CLK
STB
SW8
SW7
SW6
SW9
SW10
R28
10K
R30
10K
A5
SW-B
SW2
GND
SW3
C181
1uF
R23
10K
R0603/SMD
R25
10K
R0603/SMD
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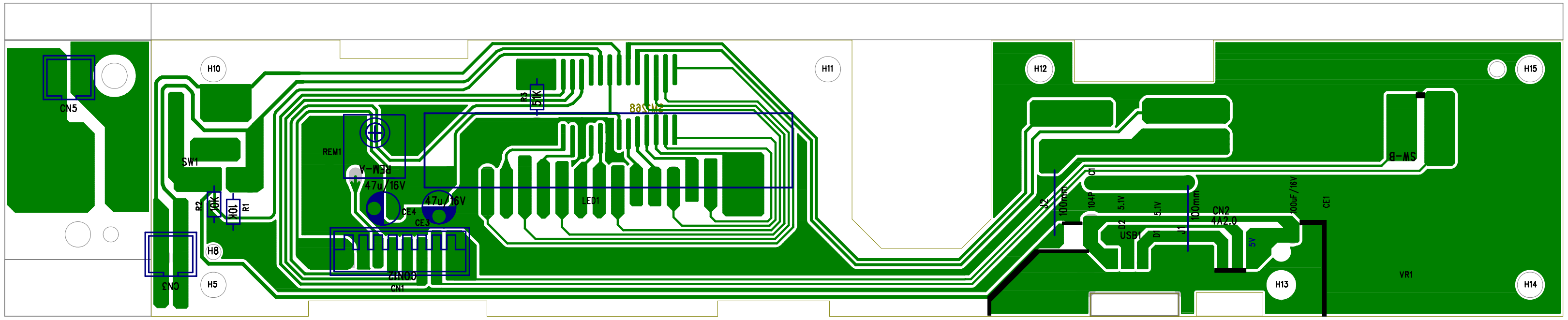
LED2
LED3
A
K



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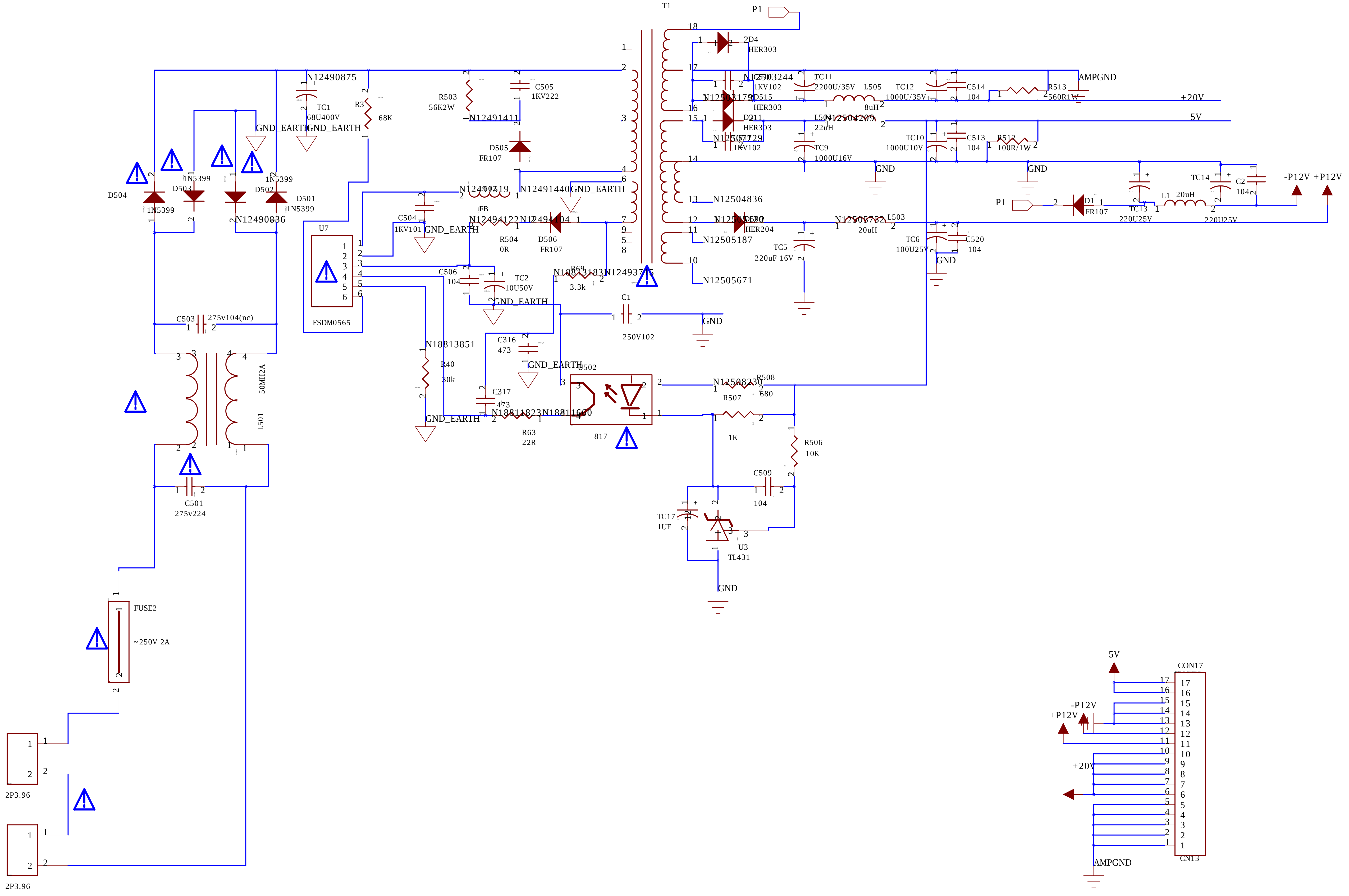
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56K2W
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D505
FR107
GND_EARTH
GND_EARTH
D504
1N5399
D503
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D502
1N5399
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N12491519
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GND_EARTH
C504
1KV101
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U7
FSDM0565
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FR107
C506
104
TC2
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R69
3.3k
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R40
30k
C316
473
GND_EARTH
C317
473
GND_EARTH
N18811823
N18811660
R63
22R
U502
817
C1
250V102
GND
C503
275v104(nc)
50MH2A
L501
C501
275v224
FUSE2
~250V 2A
2P3.96
2P3.96
N12503244
1KV102
N12503179
D515
HER303
D511
HER303
N12507729
1KV102
TC11
2200U/35V
L505
8uH
L504
N12504209
22uH
TC9
1000U16V
TC12
1000U/35V
TC10
1000U10V
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104
C513
104
R513
560R1W
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100R/1W
AMPGND
+20V
5V
GND
GND
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N12505520
HER204
N12505187
N12505671
TC5
220uF 16V
N12505782
L503
20uH
TC6
100U25V
C520
104
GND
P1
D1
FR107
TC13
220U25V
L1
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TC14
220U25V
C2
104
-P12V
+P12V
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680
R507
1K
R506
10K
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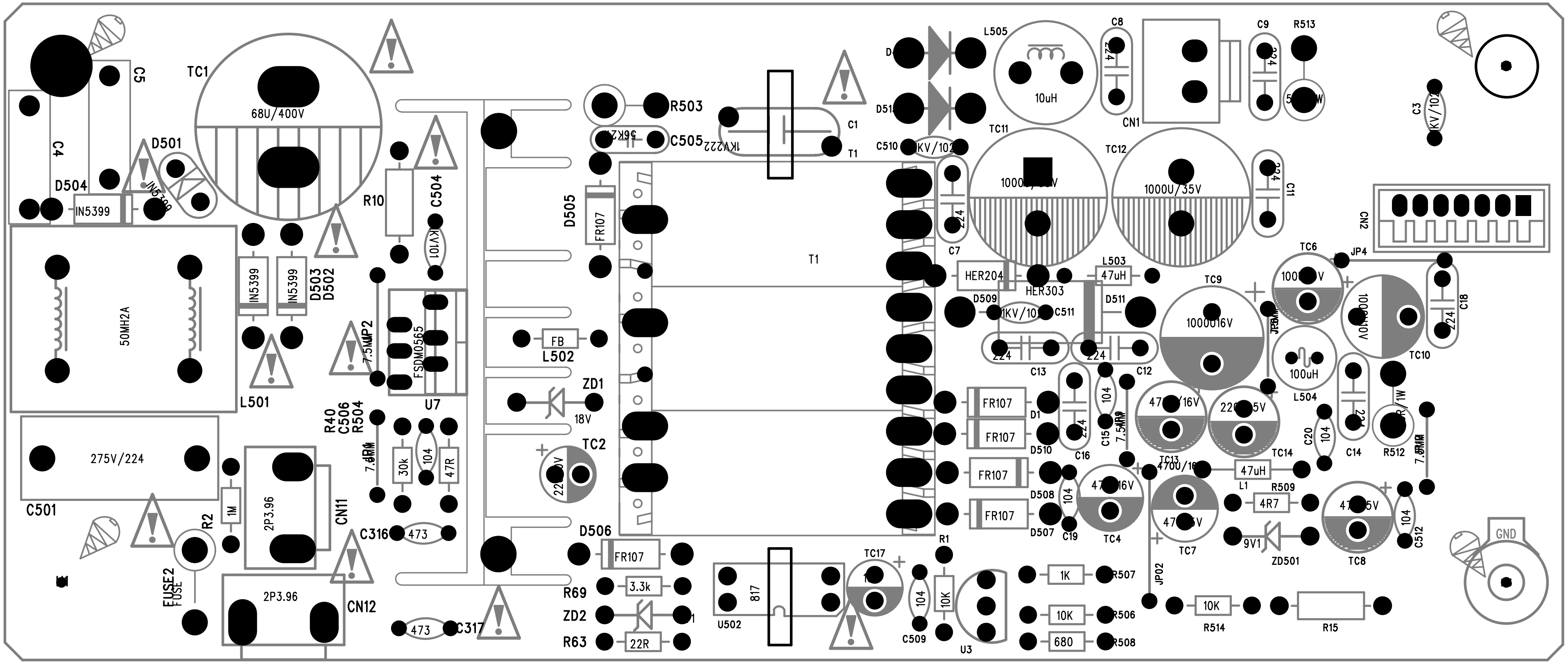

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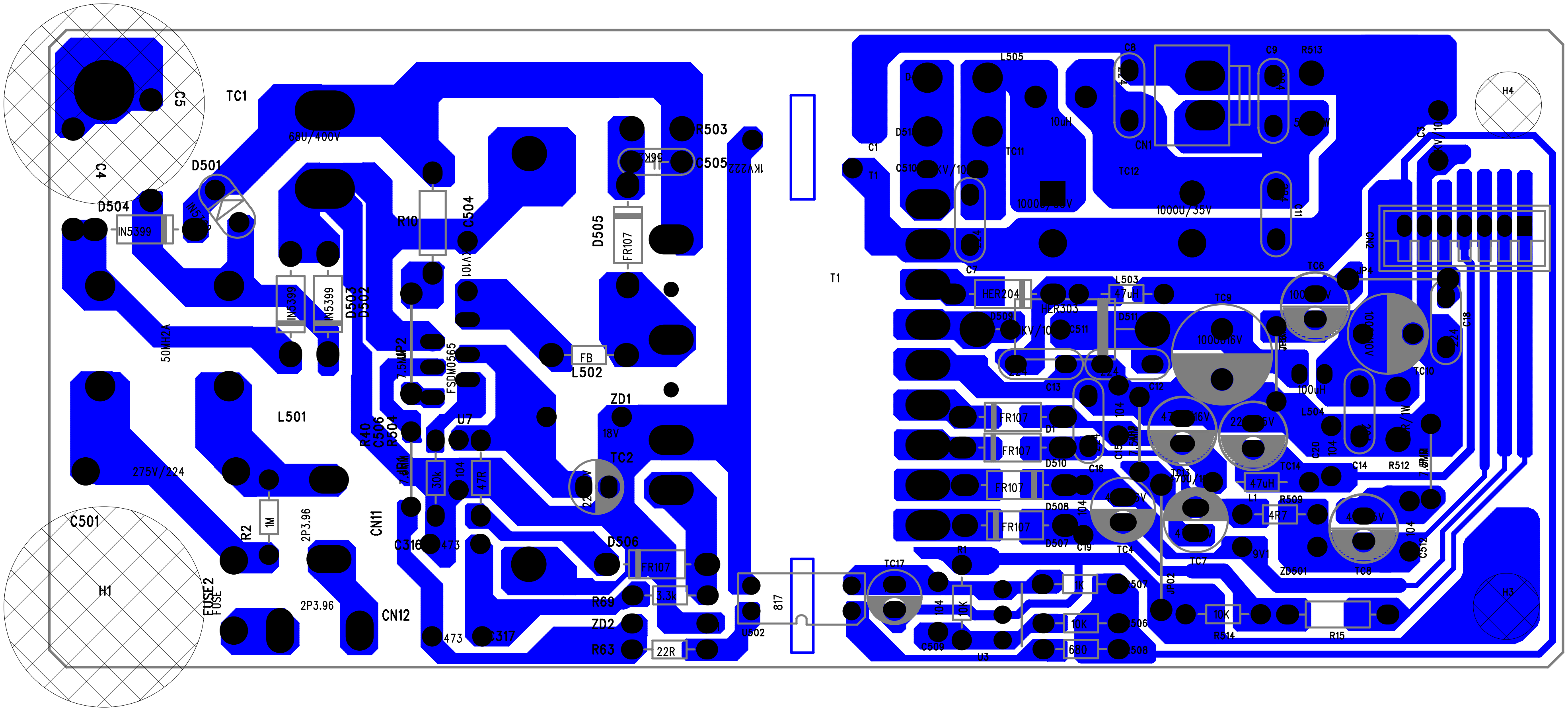

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