November 1991
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FUJITSU

DATA SHEET

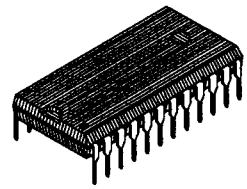
MB88304/MB88305
NMOS INPUT/OUTPUT EXPANDER

NMOS INPUT/OUTPUT EXPANDER

The Fujitsu MB 88304/MB 88305 are peripheral integrated circuits that can be connected to a 4-bit or 8-bit single-chip microcomputer (MCU) to provide additional I/O ports. Besides furnishing simple I/O port expansion, the MB 88304 and MB 88305 can AND or OR port data with data from the MCU, on instruction from the MCU.

The MB 88304/MB 88305 are pseudo-bidirectional ports. They are accessed in 4-bit units, but each individual bit can be used for either input or output, and input and output can be intermixed. The interface to the MCU requires only the connection of a 4-bit interface port and a strobe signal. All output ports of the MB 88304 are open-drain; MB 88305 output ports all have quasi pull-up resistors. The output ports on both chips are reset to the high-impedance state at power-up.

The MB 88304/MB 88305 are fabricated with N-channel silicon-gate E/D MOS process, and packaged in 24-pin plastic DIP. Also, they are powered with a single +5V power supply, and operate over the ambient temperature range of –30°C to +70°C.

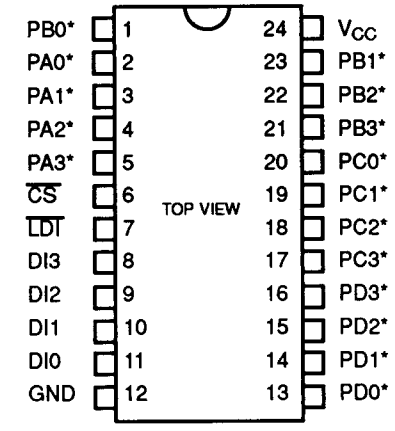


PLASTIC DIP
DIP-24P-M02

FEATURES

- Four 4-bit I/O ports (16 lines)
- Four Functions: parallel input, parallel output, AND output and OR output
- AND and OR functions provide individual output capability
- Single-bit input/output: Input and output can be intermixed on each port.
- High output drive
- Built-in power-on reset circuit
- $\overline{CS}$ pin for simplified input/output expansion
- Two output circuit types:
  - Open-drain output (MB88304)
  - Quasi pulled up output (MB88305)
- Easily connectable to MCUs with 8243 interface
- Single +5V power supply
- –30°C to +70°C operating temperature range
- N-channel silicon-gate E/D MOS process
- 24-pin plastic DIP (Suffix: -P)

PIN ASSIGNMENT



*{ MB 88304: Open-drain outputs
MB 88305: Quasi pulled up outputs

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

LOGIC SYMBOL

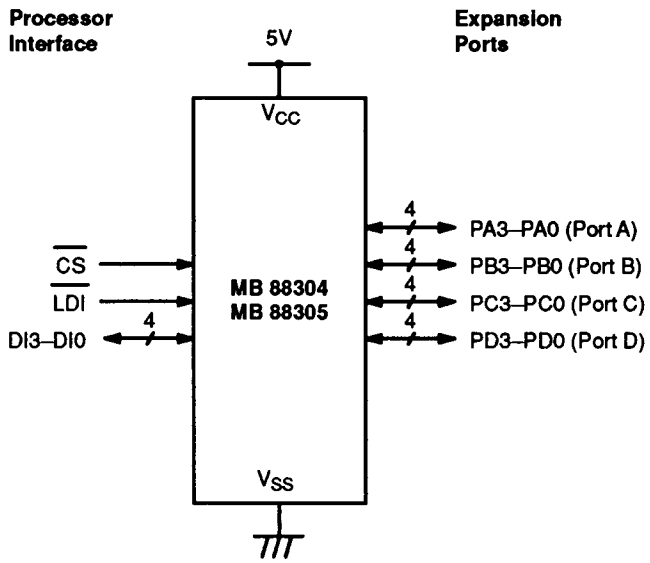
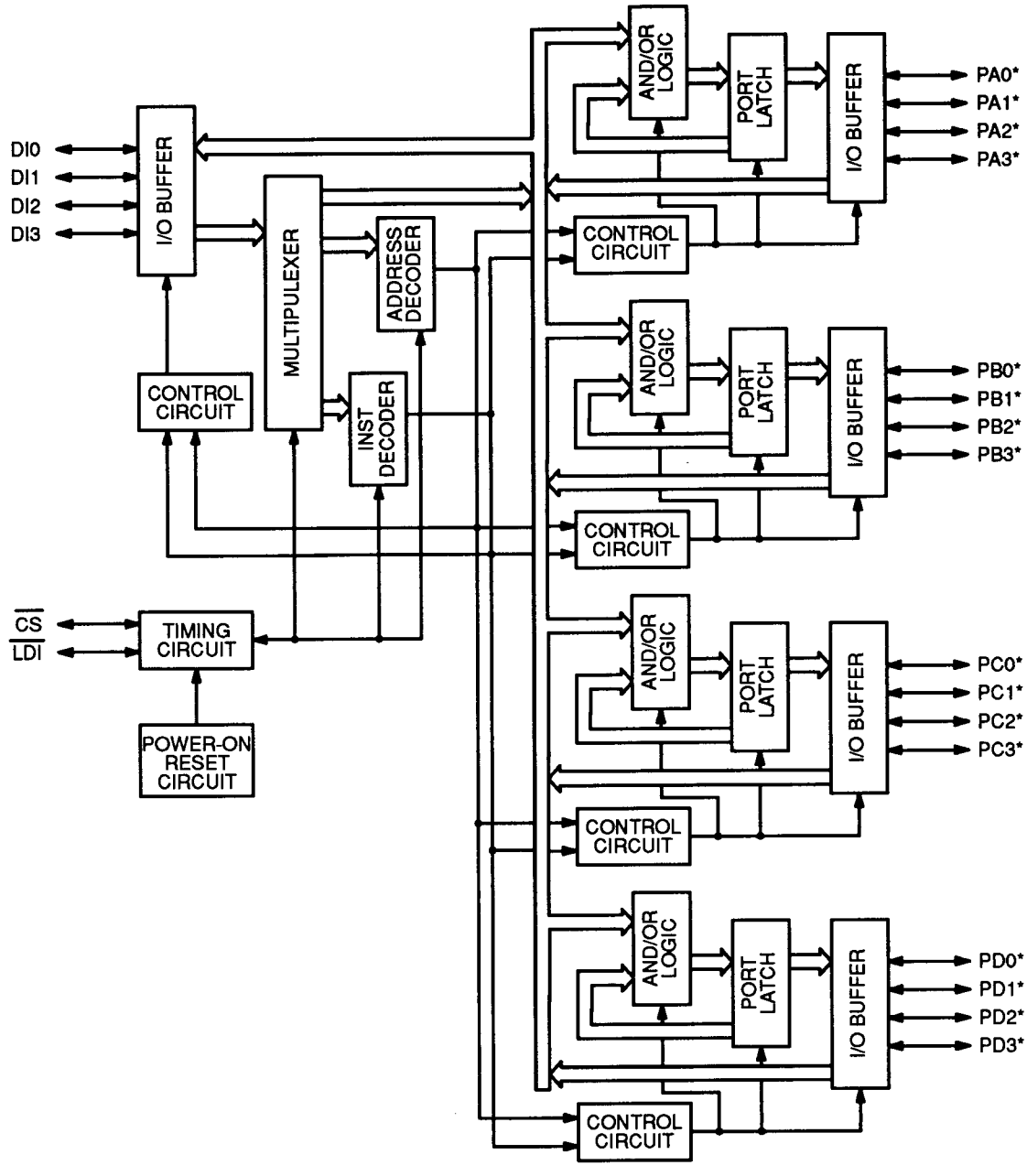


Fig. 1 – BLOCK DIAGRAM



* MB 88304: Open-drain outputs
MB 88305: Quasi pulled up outputs

PIN DESCRIPTION

The MB 88304/88305 have two interfaces: One is the processor interface; $\overline{CS}$, $\overline{LDI}$ and DI3 – DI0, which are used for the processor to communicate with the MB 88304/5 devices. Another is the expansion I/O ports; Ports A, B, C and D, which serve as an expansion of the processor's I/O.

Table 1 PIN DESCRIPTION

Symbol	Pin No.	Type	Name/Function
V_{CC}	24	–	**V_{CC} :** is the +5V power supply pin.
GND	12	–	**GND :** is the ground pin.
$\overline{CS}$	6	I	**Chip Select :** is a low-level-sense high-impedance input. A low level on this input selects the device. This input is TTL-compatible.
$\overline{LDI}$	7	I	**Load Data Input :** is an edge-triggered strobe input. The operation code and address code on DI0 to DI3 are latched at the $\overline{LDI}$ falling edge. The data transferred via DI0 to DI3 becomes valid on the rising edge of the $\overline{LDI}$ input.
DI3 to DI0	8 to 11	I/O	**Data Bus :** is a 4-bit bidirectional port used for interface to the MCU. The operation code and address code provided by the MCU on this port are latched at the falling edge of the $\overline{LDI}$ strobe input, and input/output data is transferred at the rising edge of the $\overline{LDI}$. The DI port remains in the high-impedance state except when the input operation is executed.
PA0 to PA3	2 to 5	I/O	**Ports A, B, C and D** are 4-bit bidirectional ports used as expansion I/O ports. These four ports addressed by address codes provided by the MCU. When an input operation code is given by the MCU, data on the addressed port is transferred to the DI0 to DI3 at the rising edge of the $\overline{LDI}$. When an output operation code is provided, data on the DI0 to DI3 is transferred and latched to the addressed port at the rising edge of the $\overline{LDI}$. Logical operations are also possible, in which data on the addressed port is ANDed or ORed with data on the DI0 to DI3 and the result is latched at the addressed port at the rising edge of the $\overline{LDI}$. After a power-on reset, Ports A to D are all set to the high-impedance state. An individual port is released from the high-impedance state when the OUT, AND or OR function is applied to it. (Since the MB 88304 has open-drain outputs, a line returns to the high-impedance state when an "1" is written on it.)
PB0, PB1 to PB3	1, 21 to 23	I/O	
PC0 to PC3	20 to 17	I/O	
PD0 to PD3	16 to 13	I/O	

FUNCTIONAL DESCRIPTION

The four 4-bit I/O ports of the MB 88304 and MB 88305 are labeled port A, port B, port C and port D (PA, PB, PC and PD). They serve as expansion I/O ports for a one-chip microcomputer (MCU), and can be accessed via an MCU port. Their functions are as follows:

- Data transfer from the MCU to port A, B, C or D
- Data transfer from port A, B, C or D to the MCU
- ANDing of the port A, B, C or D data with MCU data and latching of the result at port A, B, C or D
- ORing of the port A, B, C or D data with MCU data and latching of the result at port A, B, C or D

For interface to the MCU, the MB 88304 and MB 88305 have a 4-bit interface port (DI0 to DI3), a strobe input (~~LDI~~ pin) and a chip select input (~~CS~~ pin). The interface data consists of two 4-bit units. The first 4 bits give the operation code (2-bits) and address code (2-bits). The second 4-bits are the input or output data. Both 4-bit units are transferred through the interface port (DI0 to DI3) on timings determined by the strobe (~~LDI~~) signal. The MB 88304 or MB 88305 reads the operation code and address code from the MCU on the falling edge of the ~~LDI~~ signal, and sends or receives the I/O data on the rising edge of ~~LDI~~.

The ~~GS~~ pin is used to read a chip select signal from the MCU's I/O port when two or more MB 88304 or MB 88305 chips are connected to the MCU.

Ope. Code		Function	Addr. Code		Port Address
DI3	DI2		DI1	DI0	
0	0	IN (Input)	0	0	Port A (PA)
0	1	OUT (Output)	0	1	Port B (PB)
1	0	OR (Logical OR)	1	0	Port C (PC)
1	1	AND (Logical AND)	1	1	Port D (PD)

POWER-ON RESET

The MB 88304 and MB 88305 contain an internal power-on reset circuit that detects the rise of V_{CC} on the power supply line and holds the chip circuits in the reset state. In the reset state, the interface port (pins DI0 to DI3) is set to the input state, and ports A to D (PA to PD) are in the high-impedance state (except that latched output ports are not reset). The V_{CC} line must rise smoothly for the reset circuit to operate. Regardless of the input level (high or low) of the $\overline{\text{LDI}}$ pin at the moment power is applied, the reset state is released at the first falling edge of the $\overline{\text{LDI}}$ input. A power-on reset also occurs if the supply voltage (V_{CC}) drops to 1 V or less, then recovers to the rated voltage.

OUTPUT MODE (Write Mode)

Corresponding to three functions of the MCU, the MB 88304 and MB 88305 have three output modes: data transfer output (OUT), logical OR (OR) and logical AND (AND).

- OUT

The designated port latches and outputs the 4-bit data transferred from the MCU.

- AND

The 4-bit data transferred from the MCU is ANDed with the 4-bit data of the designated port, which then latches the result as output.

- OR

The 4-bit data transferred from the MCU is ORed with the 4-bit data of the designated port, which then latches the result as output.

The operation code and address code sent from the MCU to pins DI0 to DI3 of the MB 88304 or MB 88305 are latched on the falling edge of the strobe signal at the ~~LDI~~ pin. The MCU data is read on the rising edge of the strobe signal and sent to the logic circuit of the designated port, where it is processed. The MCU data is then latched as output data.

INPUT MODE (Read Mode)

The MB 88304 and MB 88305 have only one input mode (IN), corresponding to data input by the MCU.

- IN

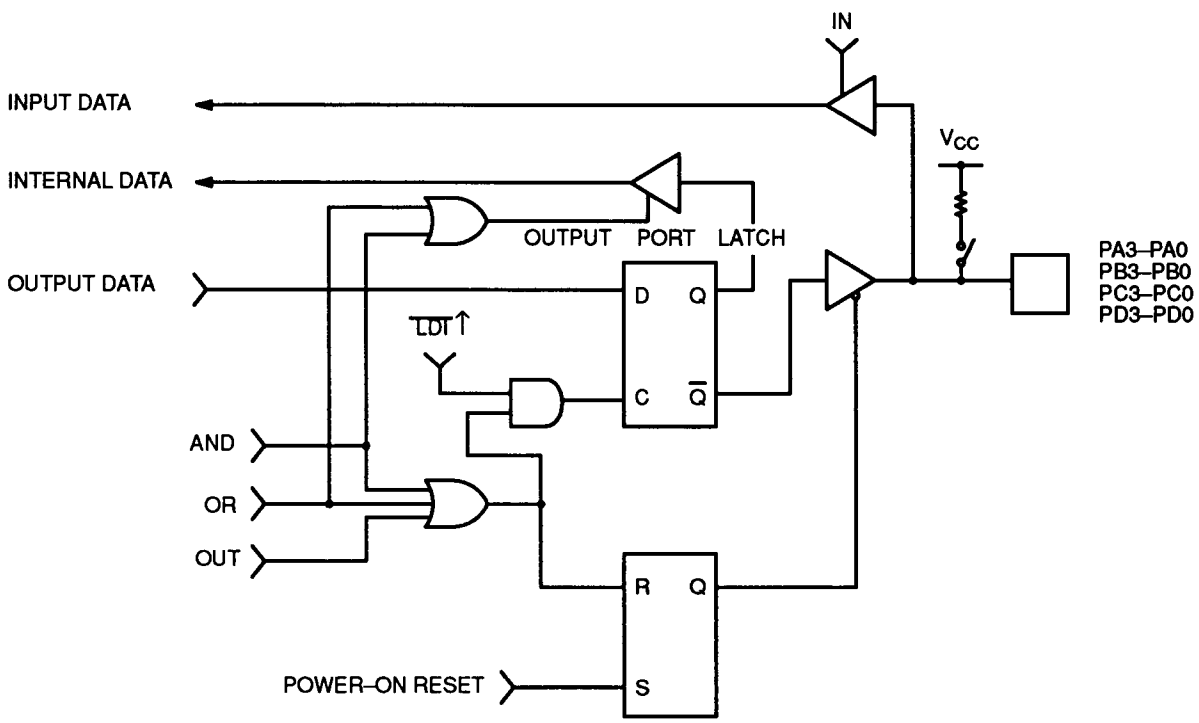
The input data at the port designated by the MCU is read and sent to the MCU via the interface port (DI0 to DI3)

The operation and address code sent from the MCU to pins DI0 to DI3 of the MB 88304 or MB 88305 are latched on the falling edge of the strobe signal at the $\overline{LDI}$ pin. If the operation code specifies input, the MB 88304 or MB 88305 sends data from the port designated by the address code to the MCU via DI0 to DI3.

A power-on reset places the chip in the input mode with ports A to D in the high-impedance state. If only the IN function is used thereafter, the ports remain in the high-impedance state. Release from the high-impedance state takes place when the OUT, AND or OR function is used.

The MB 88304 and MB 88305 are designed for easy external driving. The MB 88304 has open-drain outputs, while the MB 88305 outputs have pull-up resistors. For both chips, the input level of a port to be used for input can be read by writing a 1 and performing the IN function. Input and output can therefore be intermixed within the four bits of each of the four ports (A to D).

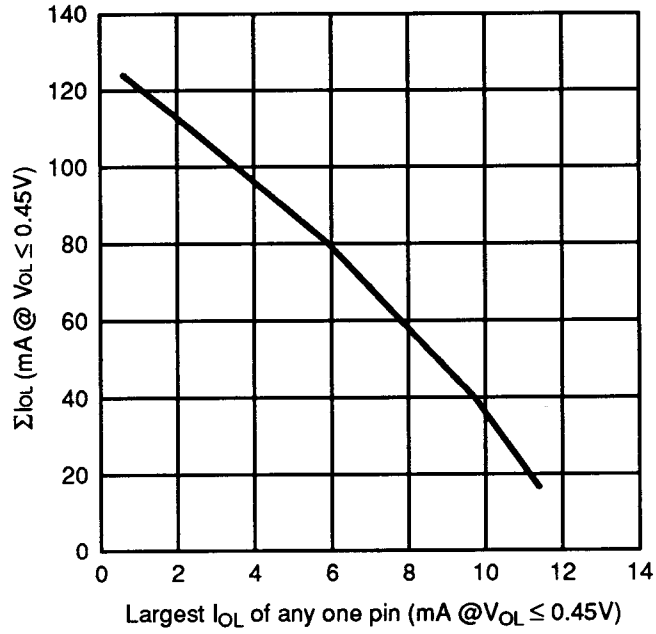
Fig. 2 – PORT CIRCUIT CONFIGURATION



SINK CURRENT FROM PORTS A TO D

When $V_{OL} \leq 0.45V$, the MB 88304 and 88305 can sink 5mA (I_{OL}) on each of their 16 I/O lines simultaneously. When this current sinking capability is not required on all of the I/O lines, or not all of the lines have to sink 5mA, the driving capability (sink current) of the other I/O lines can be increased according to the characteristics shown in the curve below.

Fig. 3 – ΣI_{OL} vs I_{OL} (@ $V_{OL} \leq 0.45V$)



For instance, if one of the I/O lines has to sink 9mA, the total I_{OL} (ΣI_{OL}) of all lines can be up to 45mA.

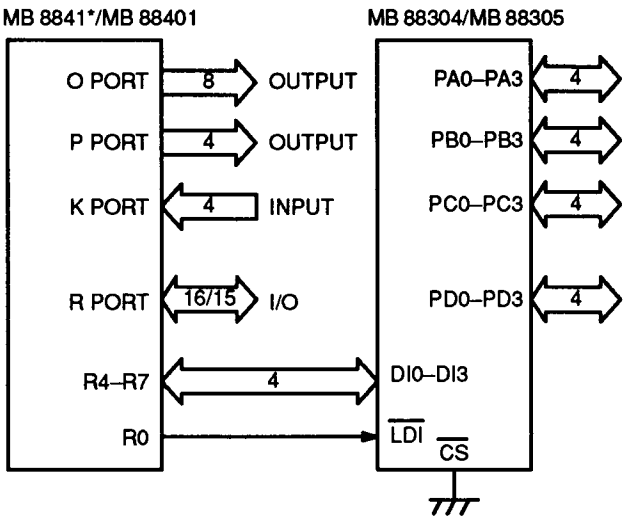
Example-1 : How many I/O lines with 5 TTL loads can be driven?
I_{OL} = 5 x 1.6mA = 8mA
$\Sigma I_{OL} \leq$ 60mA (from the total I_{OL} characteristics curve)
60mA/8mA = 7 I/O lines
The chip can drive 7 lines with 5 TTL loads, making a total of 56mA on these lines. The remaining 4mA can be shared among the other 9 I/O lines.

Example-2 : Suppose that two of the load lines have I_{OL} = 20mA (at $V_{OL} \leq 1V$). Can the MB 88304 or MB 88305 drive the following loads?
2 I/O lines : 20mA (at $V_{OL} \leq 1V$)
8 I/O lines : 4mA (at $V_{OL} \leq 0.45V$)
6 I/O lines : 3.2mA (at $V_{OL} \leq 0.45V$)
Total I_{OL} = (2 x 20mA) + (8 x 4mA) + (6 x 3.2mA)
= 91.2mA
Reading the total I_{OL} characteristics for I_{OL} = 4mA, we see that $\Sigma I_{OL} \leq$ 93mA. Since 91.2mA ≤ 93mA, the chip can drive these loads.

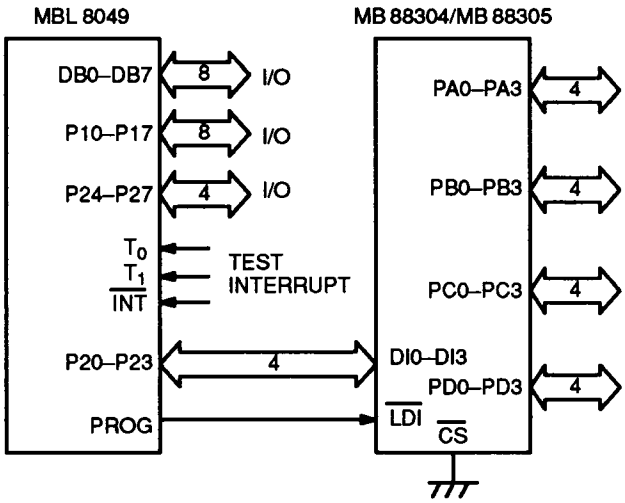
Note : The allowable total I_{OL} (ΣI_{OL}) depends on the maximum sink current of the lines for which V_{OL} must be equal to or less than 0.45V.

Fig. 4 – TYPICAL APPLICATIONS

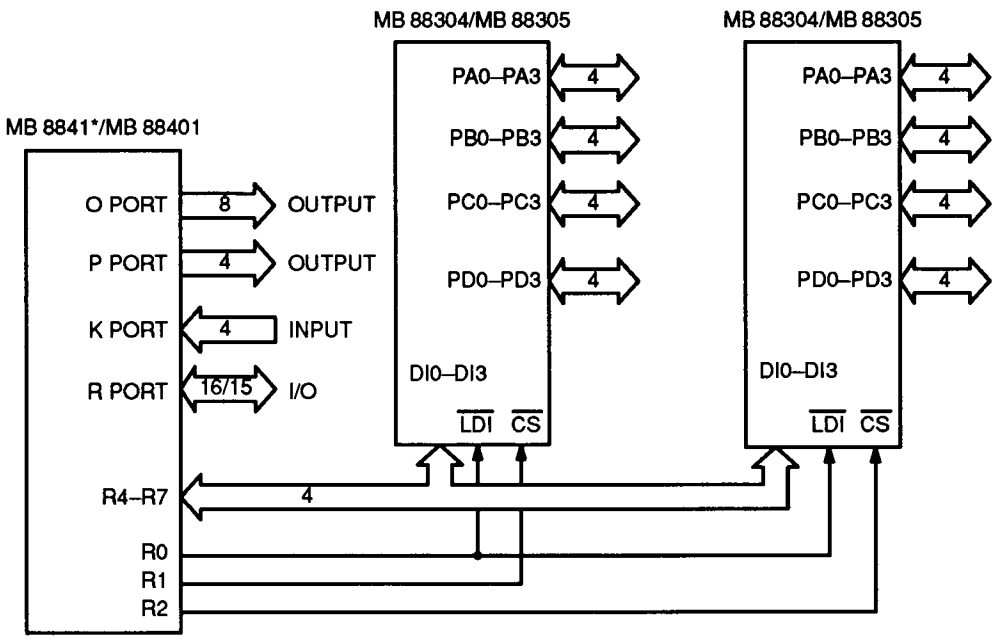
- INTERFACE WITH 4-BIT MICROCOMPUTER



- INTERFACE WITH 8-BIT MICROCOMPUTER



- INTERFACE WITH 4-BIT MICROCOMPUTER



NOTE : * Output port of MB 8841 should be open-drain type.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{CC}	V_{SS} –0.3 to + 7.0	V
Input Voltage	V_{IN}	V_{SS} –0.3 to + 7.0	V
Operating Temperature	T_A	–30 to +70	°C
Storage Temperature	T_{stg}	–55 to +150	°C
Power Dissipation	P_D	1.0	W

NOTE : Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational section of this data sheet. Exposure to ABSOLUTE MAXIMUM RATINGS conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	+5 ± 10%	V
	V_{SS}	0	
Operating Temperature	T_A	–30 to +70	°C

DC CHARACTERISTICS

(T_A = –30°C to +70°C, V_{CC} = +5V ± 10%, V_{SS} = 0V)

Parameter		Symbol	Value			Unit	Conditions
			Min.	Typ.	Max.		
Input Low Voltage		V_{IL}	V_{SS} –0.3		0.8	V	
Input High Voltage		V_{IH}	2.0		V_{CC} +0.3	V	
Output Low Voltage	Port A to D	V_{OL1}	—		0.45	V	I_{OL} = 5mA
		V_{OL2}	—		1.0	V	I_{OL} = 20mA
Output Low Voltage	DI0 to DI3	V_{OL3}	—		0.6	V	I_{OL} = 1.8mA
Output High Voltage	Ports A to D	V_{OH1}	2.4			V	I_{OH} = –50µA (MB 88305)
Output High Voltage	DI0 to DI3	V_{OH2}	2.4			V	I_{OH} = –100µA
Input Leakage Current	Ports A to D	I_{IL1}	–10		20	µA	$V_{SS} \leq V_{IN} \leq V_{CC}$
	DI0 to DI3, $\overline{CS}$, $\overline{LDI}$	I_{IL2}	–10		10	µA	$V_{SS} \leq V_{IN} \leq V_{CC}$
Input Current	Ports A to D	I_I		2.0		mA	V_{IN} = V_{SS} (MB 88305)
Total I_{OL} Output Current from 16 Output		ΣI_{OL}			80	mA	Each output current : 5mA
Supply Current	V_{CC}	I_{CC}		10	24	mA	

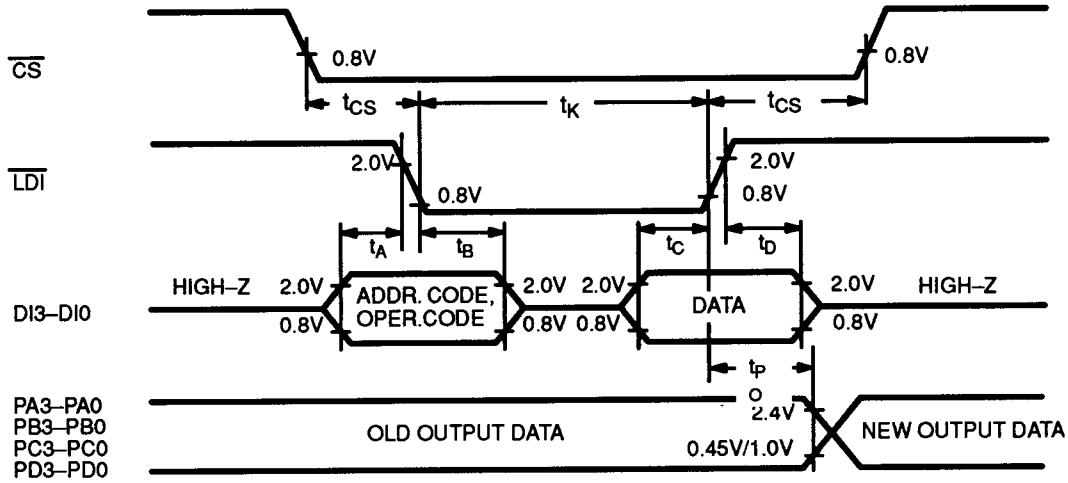
AS CHARACTERISTICS

(T_A = –30°C to +70°C, V_{CC} = +5V ± 10%, V_{SS} = 0V)

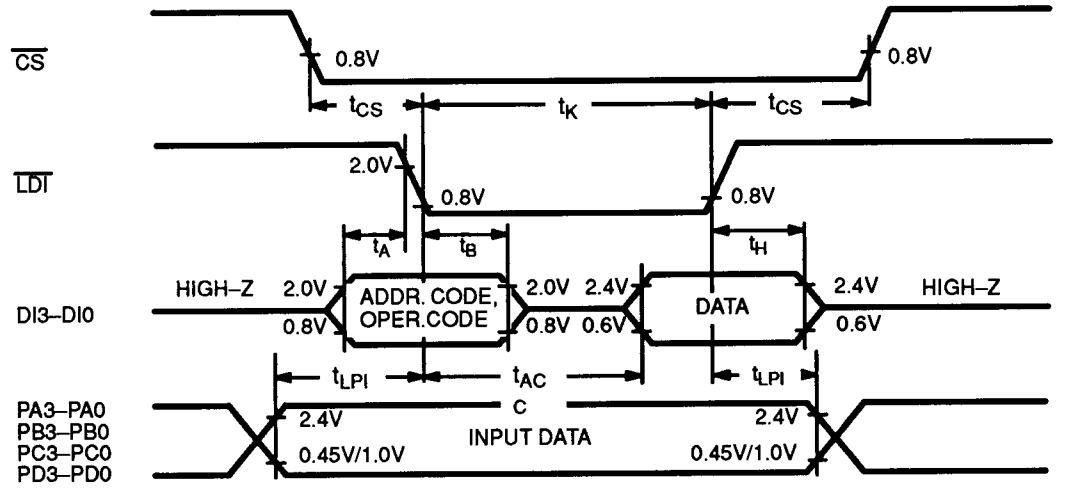
Parameter		Symbol	Value			Unit	Condition
			Min.	Typ.	Max.		
Address/Op Codes Setup Time	DI3 to DI0	t_A	100			ns	C_L = 80pF
Address/Op Codes Hold Time	DI3 to DI0	t_B	60			ns	C_L = 20pF
Data Setup Time	DI3 to DI0 (Output Mode)	t_C	200			ns	C_L = 80pF
Data Hold Time	DI3 to DI0 (Output Mode)	t_D	20			ns	C_L = 20pF
Data Output Delay Time	Ports A to D (Output Mode)	t_{PO}			700	ns	C_L = 100pF
$\overline{\text{LDI}}$ Pulse Width	$\overline{\text{LDI}}$	t_K	700			ns	
$\overline{\text{CS}}$ Setup/Hold Time	$\overline{\text{CS}}$	t_{CS}	50			ns	
Input Data Setup/Hold Time	Ports A to D (Output Mode)	t_{LPI}	100			ns	
Data Output Delay Time	DI3 to DI0 (Input Mode)	t_{ACC}			650	ns	C_L = 80pF
Data Hold Time	DI3 to DI0 (Input Mode)	t_H	0		150	ns	C_L = 20pF

Fig. 5 – TIMING DIAGRAM

OUTPUT MODE (WRITE MODE)



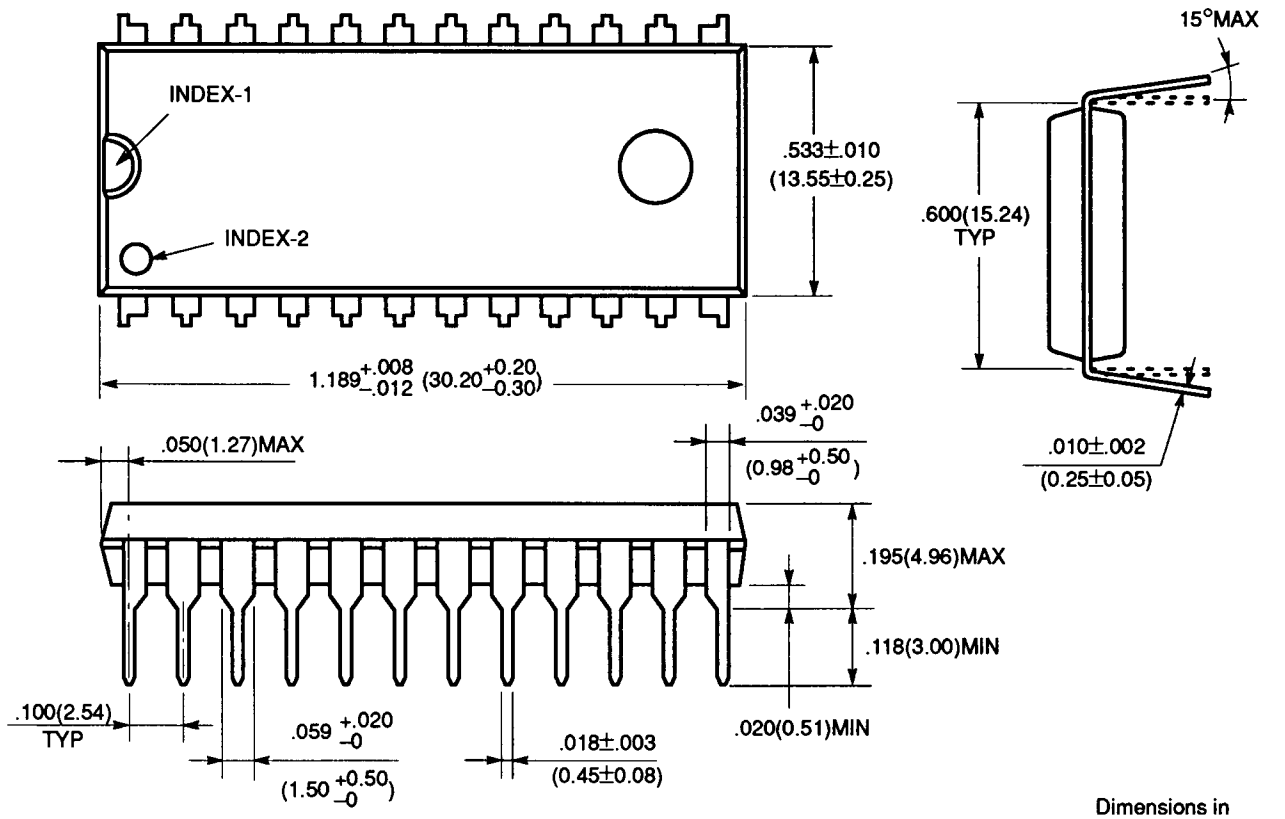
INPUT MODE (READ MODE)



PACKAGE DIMENSIONS

PLASTIC DIP (Suffix: -P)

24-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-24P-M02)



Dimensions in
inches (millimeters)

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