Table of Contents

Chapter I Overview of ABS530T(RU)

I. Description of Functions

ABS530T(RU)**is a mini-type music center integrating with video disc and power amplifier, with the following major features:**

1. The layer adopts “Sanyo deck+MT1389” solution;
2. The power amplifier adopts the analogue power amplification circuit, with the power IC of TDA7265;
3. The audio DAC adopts CS4340 192KHz/24bit sampling, with high integration and high performance and price ratio;
4. It has the function of radio reception, and the tuner adopts Sanzhenxing DTS-44K（CE） module;
5. The power supply adopts the linear power, with stable performance and lower cost;
6. Equipped with SCART（CVBS/RGB） port;
7. “RSD” function;
8. Timed ON/OFF functions.
9. Compact and with beautiful appearance.

II. Block Diagram of ABS530T Complete Player and IC Function Table:

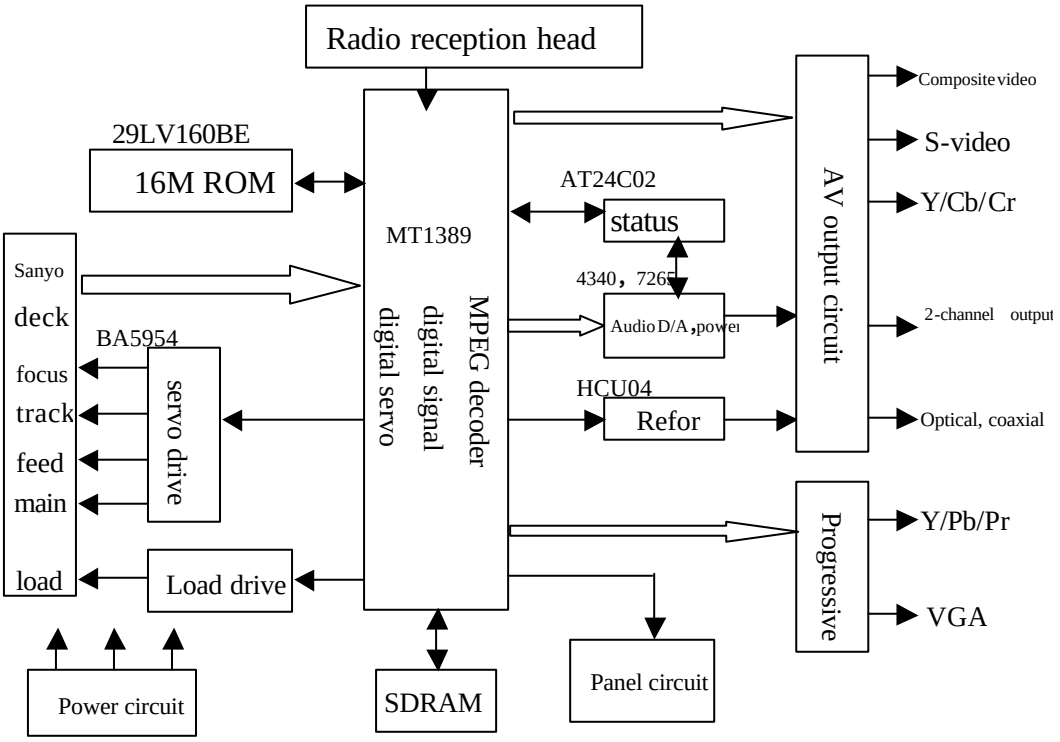


Figure 1

III. Function Table of ICs for ABS530T

Circuit Board	Number	Name	Function
Deck		Sanyo	Pick-up of disc signal
Mother Board	U201	MT1389	RF signal processing, digital signal processing, servo processing, MPEG decoding, line scan, system control
	U202	AT24C02	Series EEPROM, status memory
	U205	HCU04	Hexaphase
	U207	CS4340	AF digital/analog converter circuit
	U209	LM1117MP-1.8	1.8v voltage-regulated power supply
	U211	AE45164016	64Mbit SDRAM
	U214	29LV160BE	16Mbit FLASH ROM
	U219-221	4580	Dual operational amplifier
	U302	D5954	4-channel servo driver circuit
Panel	U401	IC 0791	Panel control, VFD display drive

	U402	HS0038A2	IR sensor
Power Board	N100	LM7812	+12V 3-terminal voltage-regulated power supply
	N102	LM7912	-12V 3-terminal voltage-regulated power supply
	N101	LM1085	5V 3-terminal voltage-regulated power supply
	N104	IC BA033	+3.3V 3-terminal voltage-regulated power supply
	N103	TDA 7265	Power amplification IC

Chapter II Operating Principle of Servo Circuit

I. Processing Procedure of Digital Signal

ABS530T(RU) adopts Sanyo double super error correction mechanism and MTK decoding solution, and its servo circuit mainly consists of preposition signal processing, digital servo processing, digital signal processing IC MT1389 and driver circuit BA5954. MT1389 is also a main part of the decoding circuit.

The A, B, C, D, E, F, SA, SB and RFO signal transmitted from the mechanism are mainly inputted through the 2-13 pins of MT1389, and after amplifying treatment of built-in amplifier of MT 1389, the signals are treated in two parts within MT1389:

After being processed by the internal digital servo signal circuit of MT1389, part of the signal forms into corresponding servo control signal, and output focus (FOSO), tracking (TRSO), main shaft (DMSO) and feed (FMSO) servo control signal from the P42, P41, P37 and P38 of MT1389 and send them to the driver circuit BA5954 to amplify the drive. After drive amplification, the signals will drive the focus coil, tracking coil, main shaft motor and feed motor. The focus and tracking servos will be used to adjust the object lens and enable laser beam to identify signal from compact disc correctly; the feed servo will be used to drive the laser head to move longitudinally, and scan the compact disc; the main shaft servo is used to control the main shaft motor to read the signals in constant linear speed and drive the disc to rotate.

After being processed by the internal VGA voltage-controlled amplifier of MT1389 in amplification and balance frequency compensation; another part of the signals is converted into digital signal by the internal A/D converter. When the mechanism reads the CD/VCD signals, these signals will be EFM demodulated in MT1389, and after accomplishing CIRC error regulation in internal MT1389, output to the next grade to carry out audio and video decoding; when the deck reads the DVD signals, these signals will be ESM demodulated in MT1389, and after accomplishing RSPC error regulation in internal MT1389, output to the next grade to carry out audio and

video decoding.

II. Processing Procedure of Control Signal

1. Automatic control of laser power, with the circuit shown as the Figure II:

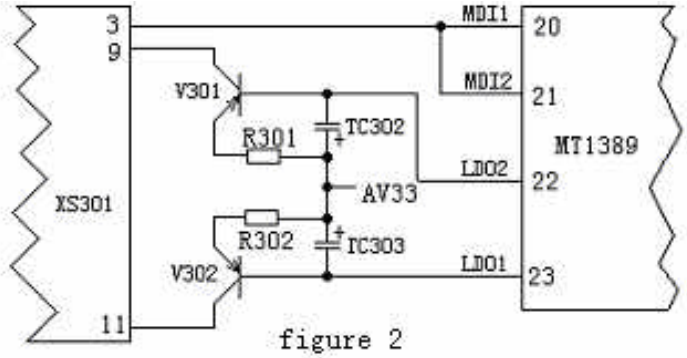


figure 2

MT1389 is integrated with APC (automatic light power control) circuit. Its Pin 20 is the pin for inputting VCD laser power rate detection signal, the Pin 21 is the pin for inputting DVD laser power rate detection signal, and the Pin 23 is the pin for outputting VCD laser power rate drive control. When the Pin 23 finds that the laser output power rate is too strong, the output voltage on Pin 23 will increase after the processing of internal circuit of MT1389, and then the conduction degree of V302 (2SB1132) and the voltage on its integration polar will decrease, which consequently lead to the decrease of voltage supplied to the laser tube, the weakening of laser head lighting, and thus achieve the automatic adjustment on laser output power. The Pin 22 is the pin for outputting DVD laser power drive control, with the specific control procedure similar to that of VCD.

2. The tray open/close control circuit is shown as the Figure III:

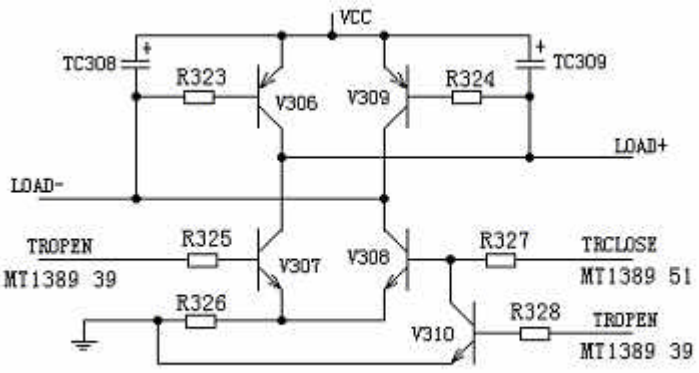


Figure 3

Different from the circuit in former MTK solution, the MT1389 is integrated with preposition signal processing circuit, so the tray open/close control signals are accomplished by MT1389, that is to say, the close control signal is accomplished by the Pin 51 of MT1389, while the open control signal by Pin 39 of MT1389.

When we press the open button, the Pin 51 of MT1389 is in high power level, while the Pin 39 is in low power level, and then the triode V308 will be on-state. Through resistor R323, the base of V306 will be made to be in low power level, and V306 will be on-state, with the current direction as the following figure:

Power voltage VCC ? V306E-C junction ? motor negative terminal LOAD- ? motor positive Load +? V308 C-E junction ? grounding

So the motor will rotate clockwise to accomplish the action of tray closing.

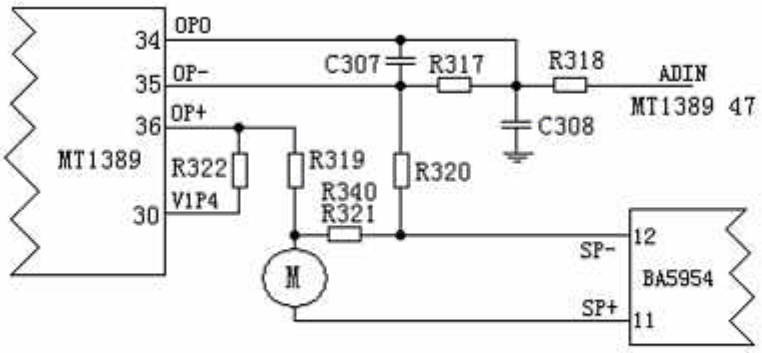
When we press the open button, the Pin 51 of MT1389 is in low power level, while the Pin 39 is in high power level, and then the triode V307 will be conducted. Through resistor R324, the base of V309 will be made to be in low power level, and V309 will be conducted, with the current direction as the following figure:

Power voltage VCC ? V309E-C junction ? motor negative terminal LOAD- ? motor positive Load +? V307 C-E junction? grounding

So the motor will rotate anti-clockwise to accomplish the action of tray opening.

3. The main shaft motor braking circuit is as the Figure IV:

To prolong the lifespan of motor and reduce the influence of start-up impact current, with the installation of disc, our R&D personnel design the main shaft motor to be in the state of constant operation, so that even if the STOP button is pressed, the disc will not be stopped. Therefore, when we press the OPEN button, a braking signal is required to stop the rotation of main shaft motor immediately to accomplish the opening action in a short time.



(figure 4)

During playing, if we press the OPEN button, the main shaft drive signal will disappear, and because of inertia, the main shaft motor is still in operation. As the electromotive force generated in the operation of motor receives the induction voltage on sampling resistors R321 and R340, which, through the resistor R319 and R320, is added to the Pin 36 and Pin 35 of MT1389, and outputted from the Pin 34 after internal processing for amplification in MT1389, and delivered to Pin 47 of MT1389 through R318. After the internal A/D conversion and corresponding processing, an

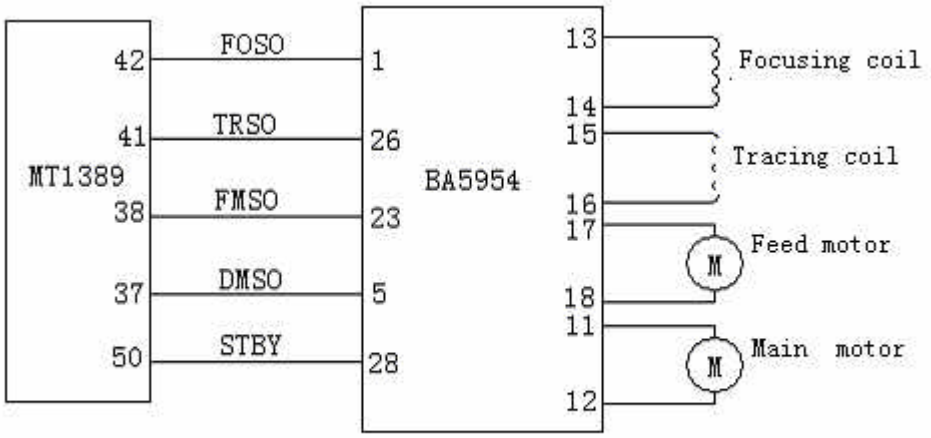
instant motor reversal braking signal will be outputted from the Pin 37 of MT1389 to stop the rotation of main shaft motor immediately, so as to ensure the standstill of the disc when opening the player.

III. Servo drive circuit

The servo drive of the player is accomplished through a piece of 4-channel dedicated drive circuit BA5954, with the circuit as Figure V:

The 4 servo control signals generated in digital servo circuit processing of MT1389, i.e. focusing control FOSO, tracking control TRSO, feed control FMSO and main shaft control DMSO signals, are added to the pins 1, 26, 23 and 5 of BA5954 respectively, and after drive amplification of BA5954, the focusing and tracking drive signals will be outputted from the pins 13 and 14 and pins 15 and 16 of BA5954 respectively, and added to the focusing and tracking coils to drive the light head to accomplish the actions of focusing and tracking.

The feed and main shaft drive signals will be outputted from the pins 17 and 18 and pins 11 and 12 of BA5954 respectively, and added to the feed motor and main shaft motor to drive the light head to move longitudinally and enable the disc to rotate in constant linear speed.



(Figure 5)

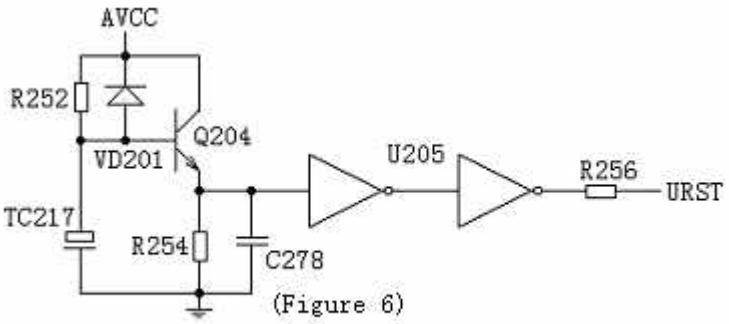
The STBY on Pin 28 of BA5954 is an output-enabling signal, and only when the pin is in high power level, there will be output of drive voltage on the output terminal.

Chapter III Operating Principle of Decoding Circuit

The decoding circuit of the player mainly consists of decoding chips (including MT1389, SDRAM AE45164016 and FLASH ROM 29LV160BE) and audio DAC CS4360.

I. Control Circuit of System

1. Reset circuit is as the Figure VI:



(Figure 6)

The reset circuit of the player consists of triode Q204 9014, reset capacitor TC217 100uF/16V and phase inverter U205 HCU04. In starting up, as the terminal voltage of capacitor cannot be changed suddenly, the basic of Q204 is in low power level. After the cut-off of Q204, its emission polar is in low power level, after secondary phase inversion by U205 and regulation, the low power level reset signal is outputted to the Pin 110 of MT1389 to reset MT 1389.

When the recharging of TC217 is finished, the base of Q204 will be in high power level, Q204 will be conducted, and the emission polar is in high power level. After the secondary phase inversion and regulation by U205, a high power level is outputted and added to the Pin 110 of MT1389 to maintain high power level during its normal operation.

2. Clock circuit

The crystal oscillator of X201 27MHz, C275/27PF, C276/27PF and phase inverter HCU04 form into clock oscillation circuit, and the clock signals generated are added to the pins 229 and 228 of MT1389 through R244 and 4248 to provide operating clock for MT1389.

3. Data communication circuit

The data communication circuit of the player consists of decoding chip MT1389, SDRAM, AE45164016 and FLASH ROM 29LV160BE, as the Figure VII:

MT1389 is a piece of super large integrated circuit, with the operation voltage of +3.3V and +1.8V. Its functions include: RF small signal preposition processing, digital servo, digital signal processing and accomplishing MPEG decoding and video coding. The built-in MCU of MT1389 is also the system control circuit of the whole player.

AE45164016 is a piece of 4M*16bit large capacity SDRAM, with the operation voltage of +3.3 V. In DV971, the 6ns module is adopted, with high speed and the maximum operation frequency up to 166MHz. Its main function is for operation buffer storage of decoding chip MT1389 to store the audio and video data stream in decoding.

29LV160BE is a piece of 16Mbit FLASH ROM, with the operation voltage of +3.3V, mainly for storing the user's information including OSD character information, operational microcode and LOGO in start-up.

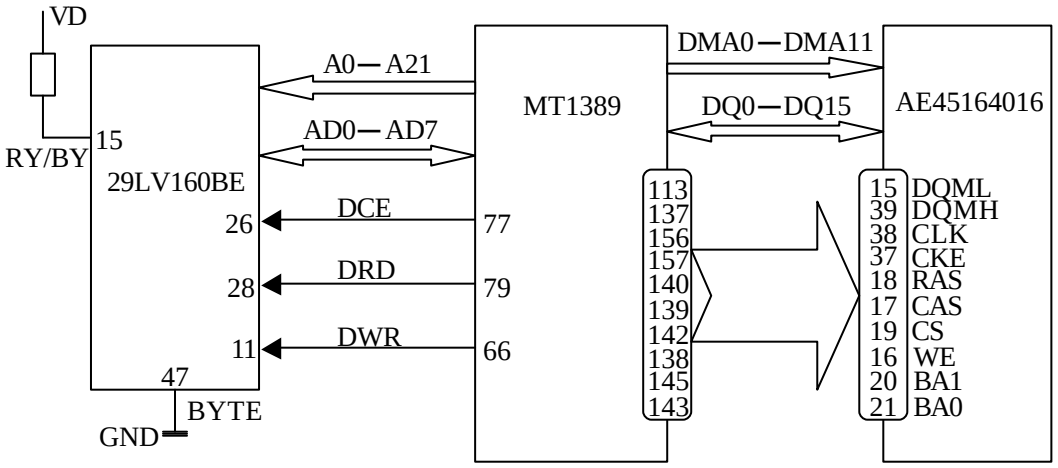


Figure 7

II. Audio and Video Output Circuit

1. Video output circuit

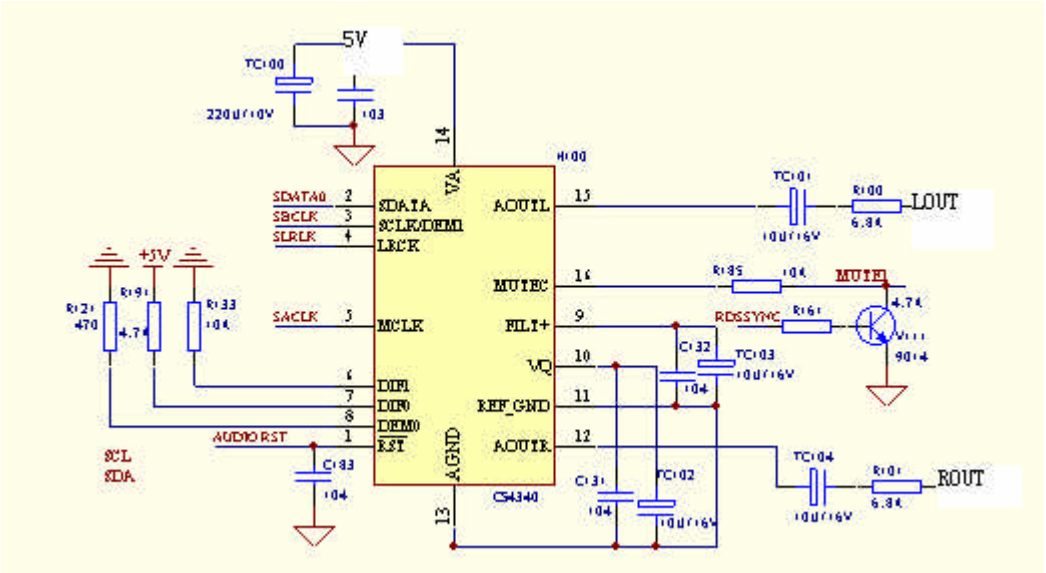
ABS530T(RU) can not only output three types of interlacing video signal (including CVBS composite video, S terminal Y-C signal and Y/Cb/Cr color difference signal), but also output two types of progressive video signal (including Y/Pb/Pr progressive color difference signal and VGA progressive signal).

The decoding chip MT1389 has built-in video encoding circuit for direct output of analogue composite video signal CVBS, S terminal, color difference signal and VGA signal.

The CVBS composite video signal is outputted from the Pin 198 of MT1389, the S terminal signal Y-C is outputted from the pins 194 and 196 of MT1389, the color difference signal and the R-B-G signal of VGA port is outputted from the pins 203, 202 and 200 of MT1389, the row and field synchronization signals of VGA port are outputted from the pins 207 and 205 of MT1389 respectively.

To mention specifically, the interlacing color difference signal, the progressive color difference signal and progressive R-B-G signal are outputted from the same pin, therefore the signal output shall be selected according to the ports of TV, otherwise there will be only sound but without picture display.

2. Audio DAC circuit, as the Figure VIII:



The main function of audio DAC circuit is to convert the digital audio signal decoded from MT1389 into analogue audio signal through D/A converting circuit, and output the audio signal after buffing and amplification to the next amplifying devices to restore it to voice.

The digital audio signals ASDATA0 decoded from MT1389 are outputted from the Pin 217 of MT1389, and delivered to the Pin 2 of audio DAC circuit CS4360. In the mean time, the left and right sound channel clock signal ALRCK, bit clock signal ABCK and the external audio clock signal ACLK required in D/A conversion are outputted from the pins 213, 214 and 215 of MT1389, and added to the pins 5, 3 and 4 of CS4360 respectively.

CS4340 will carry out D/A conversion on the digital audio signals from the channels of SDATA0 under the control of I^2C (SDA, SCL) delivered by MT1389, and output the 2-way analogue audio signals from the pins 12 and 15 of CS4340 for the amplification in the next step. The related functions of various signals are as follows:

ASDATA0----Digital audio signal, including the signals of left and right channels

ALRCK-----Left and right bit clock signals, for separating left and right channels

ABCK-----Bit clock signal, for ensuring the accuracy of signal transmission

ACLK-----External clock signal, as the operation clock of CS4340

3. Audio output amplification circuit

The audio digital signals outputted from the decoding board are delivered to the power amplification part for processing after D/A conversion by IC CS4340.

Power amplification parts:

This model carries 2-channel power amplification, and adopts IC TDA7265 to amplify the sound channels. In rated power and the load resistance of 8 ohms, the output power of each sound channel can reach 6W. With the combination of active

The amplifying circuit adopts solely power IC amplification; therefore it has high

integration degree, simple circuit and easy control. The analogue signal outputted from IC4340 will be amplified by IC 4558, and delivered to N103 IC PT2315 for electronic sound volume regulating processing after the left and right sound channels are gated by N102 IC 4052, and then to IC TDA7265 for power amplification, and output.

IC TDA7265 is a double-channel power amplification IC, with standby and muting mode, without switching impact, but with the function of overcurrent and overload protection to prevent the IC from being damaged in abnormalities effectively. The IC can provide the maximum 30W power output for each channel in normal output mode, and when adopting BTL output, the power can reach 50W. Besides, the IC has strong anti-ripple function, and is featured with low power consumption in standby state.

The functions of the pins of IC TDA9843J are as follows:

Mark	Pin	Function of Pins
-VS	1	Negative supply
OUTPUT1	2	Output of first channel
+VS	3	Positive supply
OUTPUT2	4	Input of second channel
MUTE	5	Mute control line
-VS	6	Negative supply
IN+（2）	7	Channel 2 positive phase input
IN-（2）	8	Channel 2 antiphase input
GND	9	Grounding pin
IN-（1）	10	Channel 1 antiphase input
IN+（1）	11	Channel 1 positive input

Additionally, ABS530T(RU) also has optical and coaxial digital audio output. The digital audio signals after the decompressing of MT1389 are outputted from the Pin 225 of MT1389 in the format of IEC958, and added to the corresponding optical and coaxial terminal output after the regulation by phase inverter HCU04 of U205.

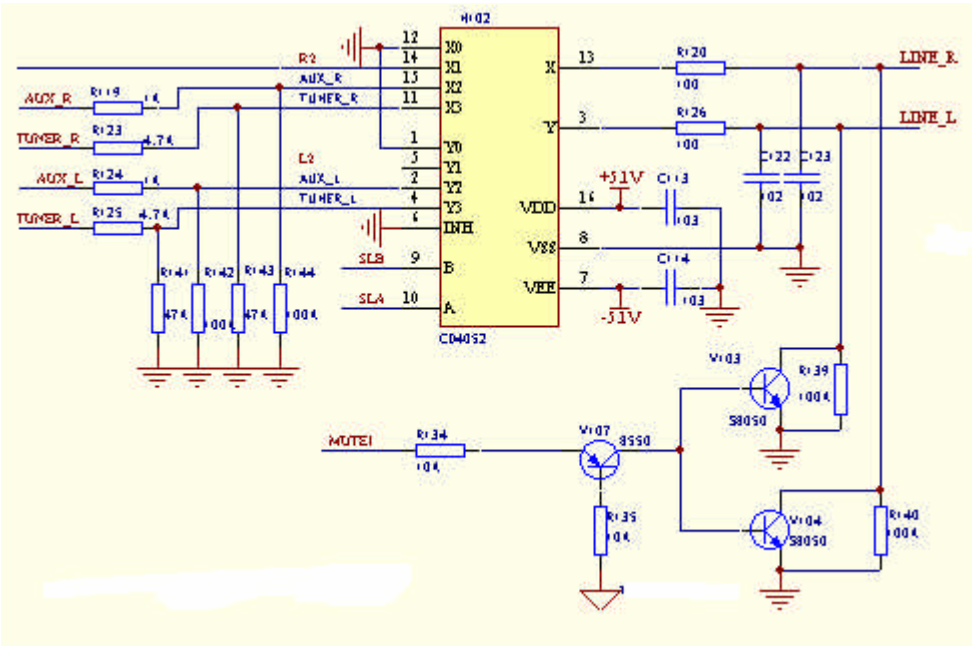
4. Muting and power-off quieting

The muting part of the player is controlled by the SCMUT and LRSWMUT outputted by MT1389. During starting up till reading out the disc, the two controlling lines will output high power level to mute the sound channels. After the disc reads out the signals, MT1389 will alternate the two controlling lines into lower power level to carry out normal signal output. When the remote control muting is pressed, the two controlling lines will be alternated into high power level to realize muting. For this model has just the amplification output of left/right channel, the central mute control line is applied to control the mute of the Karaoke.

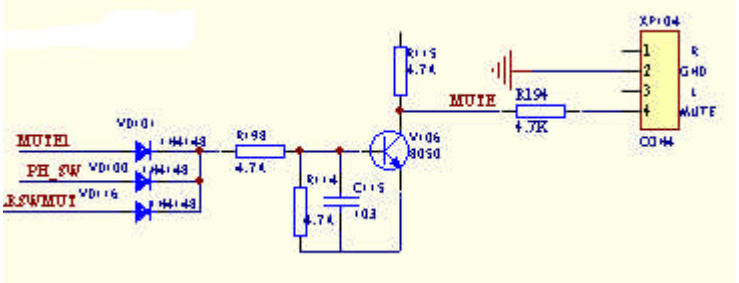
5. Automatic Power-on Function

This model is equipped with the IC M41T81, so that it has the function of a clock; just like a clock, when you power it off, it is supplied with the power from one group of battery inside it; when the external power is cut off, the internal power supply is switched on. Therefore, the clock can still work in case of the power cut.

The most distinctive feature of this player is its automatic turnon function. Whenever you want to turn it on, you just preset the turnon time and then set it to a standby status. As a result, when the clock runs to the preset turnon time, the player will give a high level trigger to the STANBY at P50 of 1389, and the player will be turned on. The preset time is stored in the IC 24C02 while the clock is controlled by the 1389 and IC M41T81.



When the MUTE1 is at the high level, the triode V107 is turned on, so that the triode V103 and V104 are turned on, and the left/right channel signal is connected with the grounding, so that the mute is realized therefore.



This mute circuit includes three diodes in parallel connection; among the three control lines, when there is any one at high level, the MUTE signal outputs at low level, so that the power amplifier tube TDA7265 works normally; only when the three control lines are at low level synchronously, the triode V106 cuts off, so that the MUTE

outputs high level and the zener diode on the power board turns on at the reversed direction while the triode V100 turns on and pulls down the voltage at P5 of TDA7265, and finally the complete muting is realized.

In addition, there is a C128 1U/50V capacitor on the peripheral circuit of IC TDA7265 and the mute control line. The start-up mute is realized, for the voltage at both ends of the capacitor can not change abruptly at the very moment when the player is turned on, so as to make the level at the P5 to be low at the very moment of turning on the player. When the player is turned off, this capacitor discharges quickly via the resistor R114 so as to make the level at P5 to become low rapidly, so that the function of turnoff muting is realized.

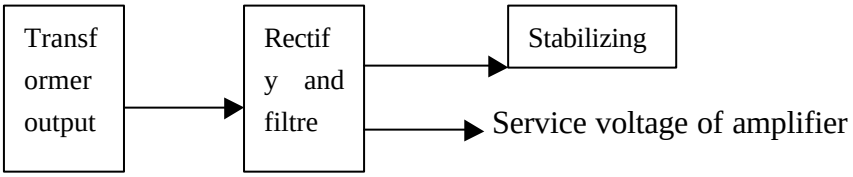
5. Function of Tuning

ABS530T(RU) has the function of tuning, and can receive RDS signal. The signals of radio reception, the auxiliary channel input signal and the left and right sound signal outputted from CS 4360 are gated through N111IC CD4052, and the controlling A and B are controlled by the low and high power level of AUIN SL0 and AUIN SL1 emitted from MT1389.

The radio head control lines CE, DI, CL and DO are controlled by the array lines connected to MT1389 for the direct control by 1389. When any one of the controlling lines is in abnormality, the radio reception will be in malfunction. The RDS signal received by radio head will be delivered to the dedicated IC SAA6588 for processing.

Chapter IV Operating Principle of Power Circuit

I. Block Diagram



II. Analysis of Operating Principle

The player adopts linear power for power supply, and is featured with high power, stable power supply and low cost.

After the input voltage is switched via the insulating transformer, the two groups of AC outputs are rectified via the bridge rectifier composed of the VD100, VD101, VD102, VD103 and filtered via the C100, C101, C112 and C113, and then a group of ±20V DC supplies the power to the amplifier IC—such voltage outputs the stable ± 12V via the IC 7812 and IC 7912. For the current is purified by two groups of filter capacitor, and the stabilizing IC is for the voltage stabilizing output, therefore the output voltage is relatively stable, with low ripple factor. After the rectifying and filtering, the other group of 8.4V AC voltage outputs +5V CD via the stabilization of IC 1805, then after the filtering and the stabilization via the stabilizing IC BA033, it outputs +3.3V to supply the power to the decoding IC. For this model adopts the linear power supply, and the voltage part and signal amplification part are on the same board, it's better to process at the power purifying part in order to keep the effect upon the signals from the power supply surge. In doing so, the player can be ensured to have relatively low fluctuation in its service voltage in case of any change to the public power supply, so that the reliability of the player is ensured. The transformer has another group of voltage output, with an AC connecting directly to the panel so as to supply the filament voltage to the display; another group of voltage outputs a group of +27V DC after the rectifying and filtering, so as to supply the grid voltage to the display.

Additionally, this player has the timed power-on function. To ensure some circuits of this player to work normally without the external voltage so as to realize the purpose of timed start function, this player is added with a group of lithium battery supplying 3V voltage, so that the clock can still work normally when the player is turned off. When the power on the player is turned on, the VCC voltage effects on the diode VD118 and the diode cuts off, so the battery can not supply the power to the entire player. When the power on the player is turned off, the VCC is at zero without the external voltage, and the diode is positively conducted, so that the battery supplies the necessary voltage to the working part of the clock on the player to ensure its normal work.

Chapter 5: Panel control and VFD display circuit

The panel mainly consists of VFD screen, driver IC6311, IR sensor HS0038A2 and button and indicator display circuit, mainly for accomplishing man-player dialogue and display of operation status.

The structural drawing is as follows:

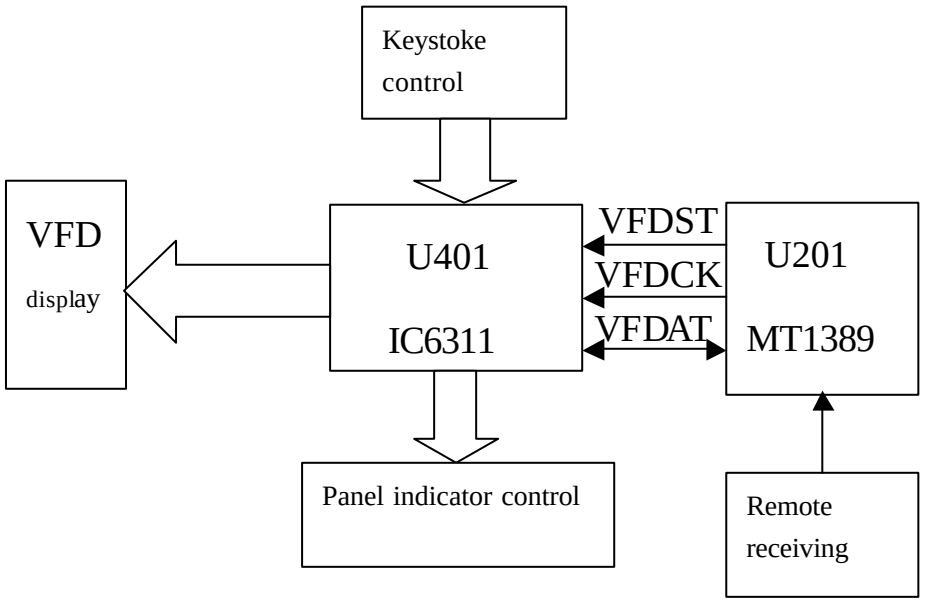


Figure 11

MT1389 will control the U401 IC 6311 to display the operation status of the player through the VFDST status, VFDCK clock and VFDAT data, under the control of CPU built in MT1389, receive the user control commands sent by IC6311, and control the controlled circuit of the player to limit the player to operate in specified status.

When the user operates the panel buttons, the control command is sent to the IC 6311 through keyboard-scanning circuit, and through internal decoding drive, the IC 6311 outputs the control data from the pins 5 and 6 (VFDAT) to the built-in CPU of MT1389, which will realize the control on the controlled circuit, and control the VFD through IC 6311.

VFD401 is a vacuum fluorescence screen, and its biggest feature is its high brightness. Its operation principle is similar to the kinescope of TV. The pins 1, 2, 34 and 35 are for filament power supply; the pins 27-32 are GRID poles, each GRID has 16 different characters of display; the pins 4-19 are SEG poles, and the CPU control the SEG poles through its control on UPD6311, and display the characters of corresponding operation status on the screen.

The remote reception circuit mainly consists of remote receptors HS0038A2, of which

the pin 1 is for grounding, the pin 2 for power supply, the pin 3 for output of reception signal, and they are all connected directly to the CPU in MT1389 to control the corresponding circuit.

Moreover, there are two digital potential device knobs on the panel, one is for track control, and the other is for volume control. Through array lines, they are connected to the pin 168,169,181 and 184 of MT1389 directly.

Troubleshooting

I. Voltage on key points of ABS530T（RU）

Power circuit:

1. PVCC: Around 20V;

Decoding circuit:

Reset:

1. U205 (HCU04): 8 pins, around 3.3V;

2. MT1389: 110 pins, around 3.3V;

3. FLAHS ROM: 12 pins, around 3.3V

Clock:

27MHZ crystal oscillator two ends: Around 0.77V.

I^2C bus SDA: 3.3V

I^2C bus SCL 3.3V

Servo circuit:

LD01： 3.3V；LD02：3.3V

V301 and V302 electron collector LD voltage: 2.3V

BA5954 pin 4 base voltage: 1.4V

BA5954 pins 15 and 16 tracking drive output: Around 2.5V

BA5954 pins 17 and 18 feed drive output: Around 2.5V

BA5954 pins 13 and 14 focus drive signal output: Around 2.5V

BA5954 pins 11 and 12 main shaft drive output: Around 2.5V

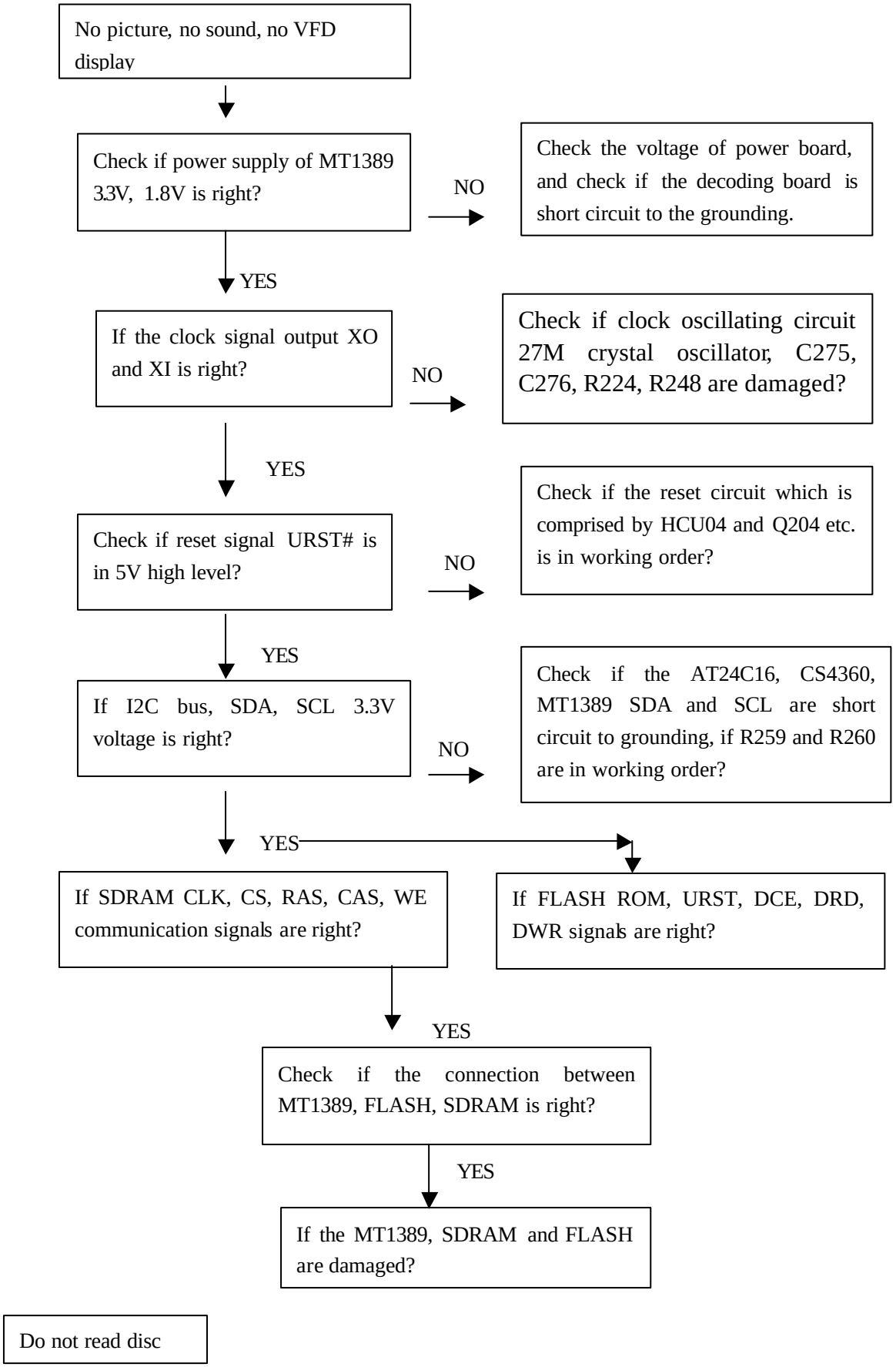
BA5954 pin 1 focus control signal input: 1.4V

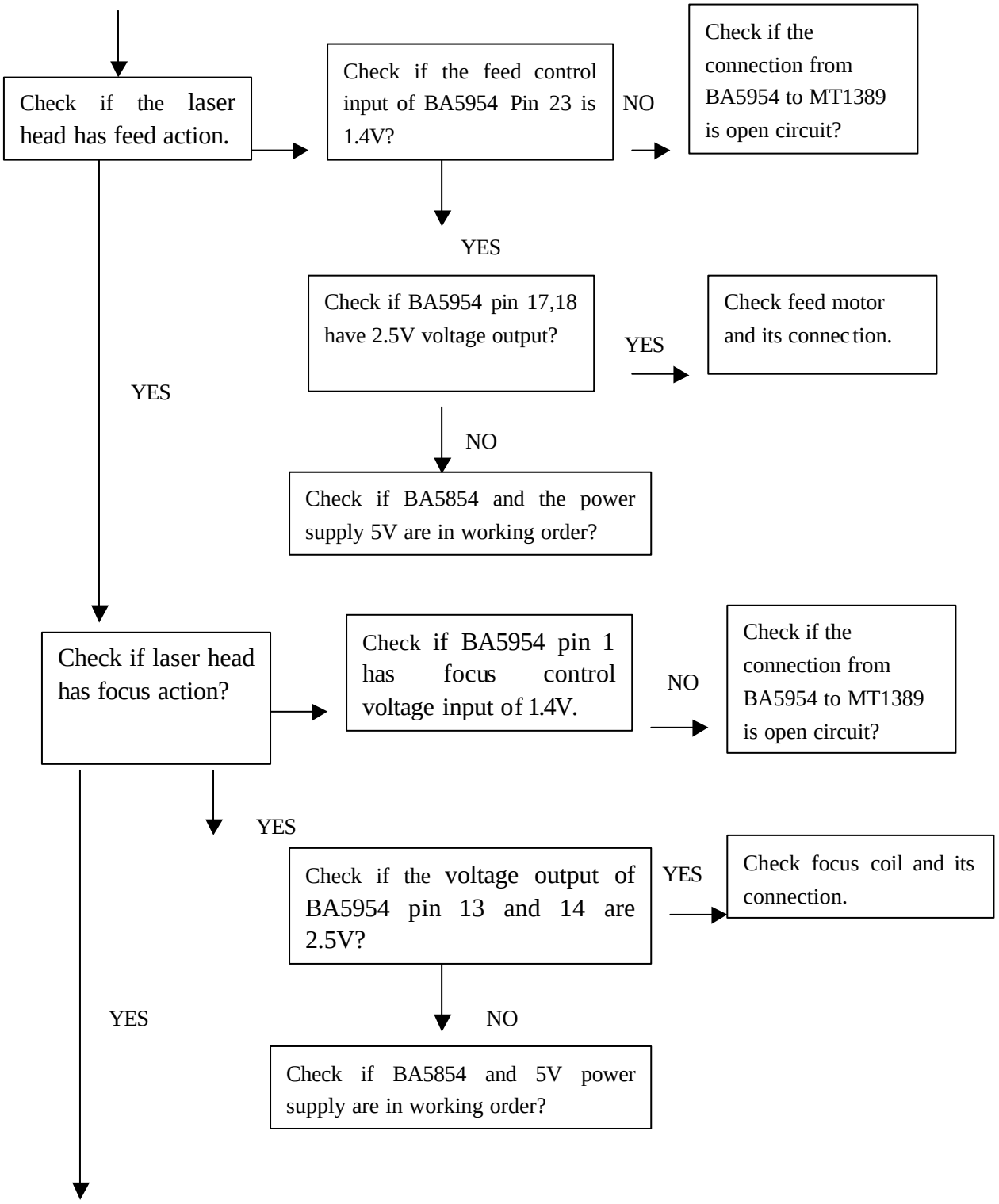
BA5954 pin 5 main shaft control signal input: 1.4V

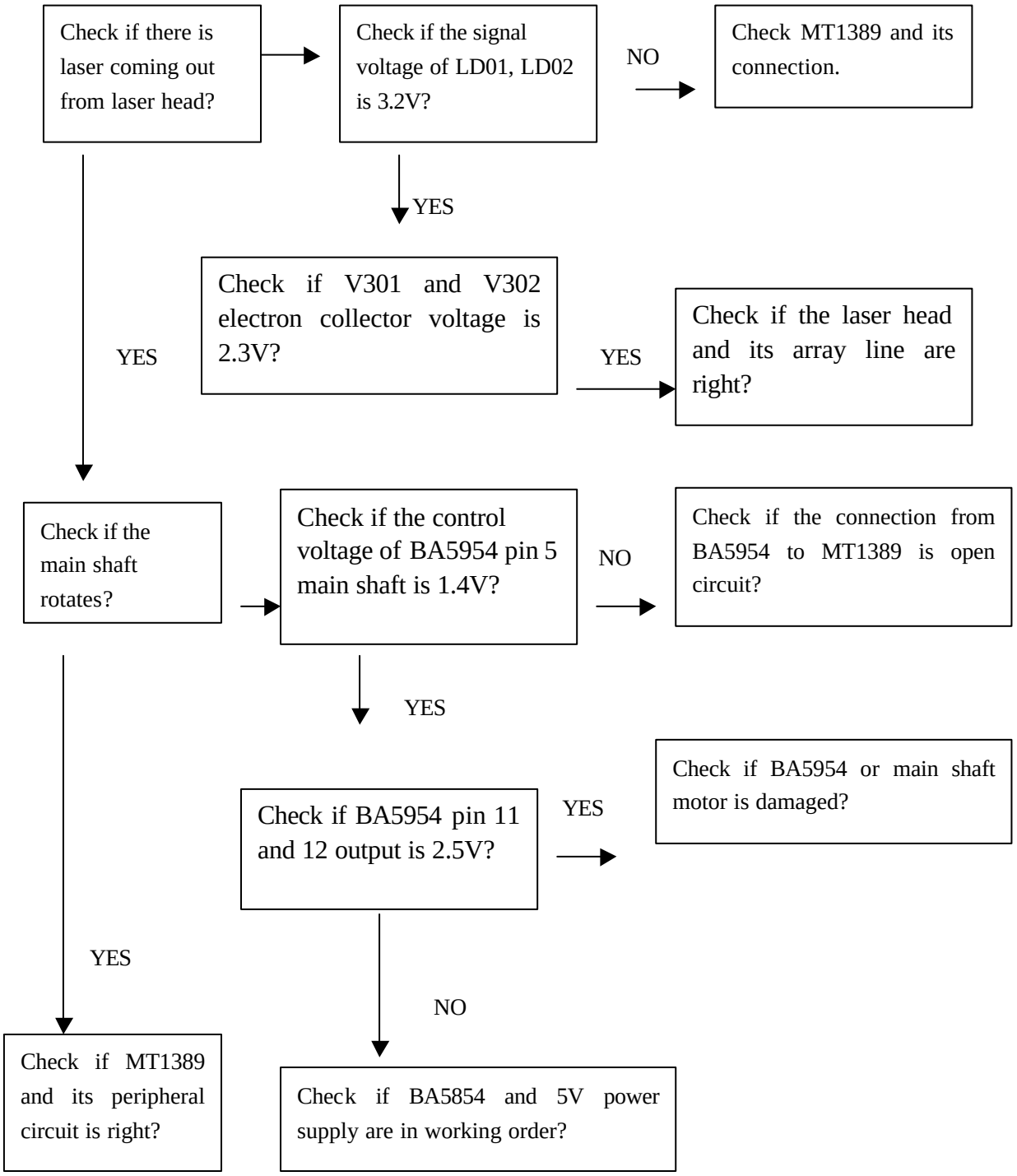
BA5954 pin 26 tracking control signal input: 1.4V

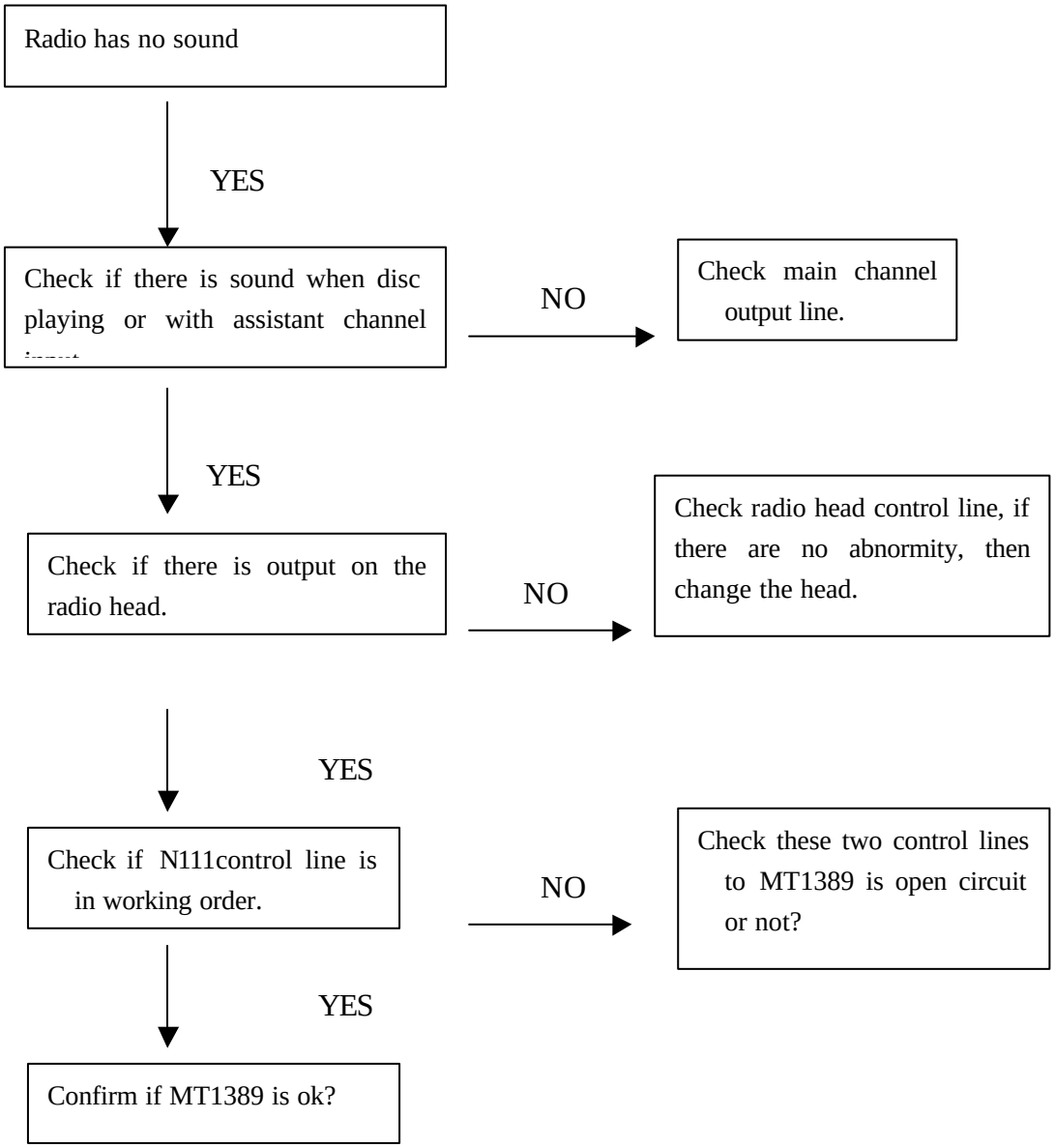
BA5954 pin 23 feed control signal input: 1.4V

II. Troubleshooting of main troubles




Check if the laser head has feed action.
Check if the feed control input of BA5954 Pin 23 is 1.4V?
NO
Check if the connection from BA5954 to MT1389 is open circuit?
YES
Check if BA5954 pin 17,18 have 2.5V voltage output?
YES
Check feed motor and its connection.
YES
NO
Check if BA5854 and the power supply 5V are in working order?
Check if laser head has focus action?
Check if BA5954 pin 1 has focus control voltage input of 1.4V.
NO
Check if the connection from BA5954 to MT1389 is open circuit?
YES
Check if the voltage output of BA5954 pin 13 and 14 are 2.5V?
YES
Check focus coil and its connection.
YES
NO
Check if BA5854 and 5V power supply are in working order?


Check if there is laser coming out from laser head?
Check if the signal voltage of LD01, LD02 is 3.2V?
NO
Check MT1389 and its connection.
YES
Check if V301 and V302 electron collector voltage is 2.3V?
YES
Check if the laser head and its array line are right?
YES
Check if the main shaft rotates?
Check if the control voltage of BA5954 pin 5 main shaft is 1.4V?
NO
Check if the connection from BA5954 to MT1389 is open circuit?
YES
Check if BA5954 pin 11 and 12 output is 2.5V?
YES
Check if BA5954 or main shaft motor is damaged?
YES
NO
Check if MT1389 and its peripheral circuit is right?
Check if BA5854 and 5V power supply are in working order?


Radio has no sound
YES
Check if there is sound when disc playing or with assistant channel input
NO
Check main channel output line.
YES
Check if there is output on the radio head.
NO
Check radio head control line, if there are no abnormity, then change the head.
YES
Check if N111control line is in working order.
NO
Check these two control lines to MT1389 is open circuit or not?
YES
Confirm if MT1389 is ok?

Attachment ：Functions of IC Pins

I. MT1389

MT1389 adopts the LQFP 256 pin packaging and 3.3V/1.8V double voltage operation mode. It is a piece of large-scale CD-ROM and DVD-ROM preposition processing CMOS integrated circuit with excellent performance, and a single chip dedicated to CD/VCD/DVD player. It contains focusing servo error amplification; tracking servo error amplification and RF level output servo control, including the following main functions:

RF small signal preposition processing, mainly for carrying our corresponding processing and amplification on the RF signals transmitted from the light head part, adjusting the laser output power automatically, and identifying the VCD disc and DVD disc.

Digital servo processing can generate focusing, tracking, feed and main shaft servo control signals; digital signal processing, accomplishing the EFM/EFM + demodulating of RF signals.

MPEG-1/MPEG-2/MPEG4/JPEG Video decoding chip, which can not only realize the decoding of VCD and DVD, but also realize MPEG 4 network video decoding, being compatible to “network movie” disc, and decipher JPED pictures to realize the function of digital photo album play.

On audio aspect, it can not only realize AC-3/DTS double decoding, decipher MP3, and is also compatible to DVD-Audio decoding to achieve high-resolution sound restoration in 1000 times higher than CD.

By utilizing the 8032 microprocessor with built-in chip, MT1369E can also realize the system control function of player, which simplifies the circuit design substantially.

The pin functions of MT1389 is as the following table:

Pin	Name	Function
1	AGND	Analogue grounding
2	DVDA	DVD-RF high-frequency AC coupling signal A
3	DVDB	DVD-RF high-frequency AC coupling signal B
4	DVDC	DVD-RF high-frequency AC coupling signal C
5	DVDD	DVD-RF high-frequency AC coupling signal D

6	DVDRFIP	DVD-RF high-frequency AC coupling signal RFIP input
7	DVDRFIN	DVD-RF high-frequency AC coupling signal RFIN input
8	MA	DVD-RAM main light beam RF DC signal input A
9	MB	DVD-RAM main light beam RF DC signal input B
10	MC	DVD-RAM main light beam RF DC signal input C
11	MD	DVD-RAM main light beam RF DC signal input D
12	SA	DVD-RAM auxiliary light beam RF DC signal input A
13	SB	DVD-RAM auxiliary light beam RF DC signal input B
14	SC	DVD-RAM auxiliary light beam RF DC signal input C
15	SD	DVD-RAM auxiliary light beam RF DC signal input D
16	CDFON	CD focusing error phase inversion input
17	CDFOP	CD focusing error phase input
18	TNI	3 light beam auxiliary PD signal phase inversion input
19	TPI	4 light beam auxiliary PD signal phase input
20	MDI1	Laser power monitoring input 1
21	MDI2	Laser power monitoring input 2
22	LDO2	Laser power monitoring output 2
23	LDO1	Laser power monitoring output 1
24	SVDD3	Servo 3.3V power supply
25	CSO/RFOP	Main servo signal output/RF phase output
26	RFLVL/RFON	RF level output/RF phase inversion output

27	SGND	Servo grounding
28	V2REFO	Reference voltage 2.8V
29	V20	Reference voltage 2.0V
30	VREFO	Reference voltage 1.4V
31	FEO	Focusing error signal output
32	TEO	Tracking error signal output
33	TEZISLV	Tracking zero crossover error input
34	OP_OUT	Sensing signal amplification output
35	OP_INN	Sensing signal phase inversion input
36	OP_INP	Sensing signal noninverting input
37	DMO	Main shaft control signal output
38	FMO	Feed control signal output
39	TROPEN PWM	Tray Open signal output
40	PWMOUT1/ADIN9	First-route pulse width demodulating signal output/AD universal input
41	TRO	Tracking control signal output
42	FOO	Focusing control signal output
43	USB_VSS	USB grounding
44	USBP	USB data
45	USBM	USB data
46	USB_VDD3	USB 3.3V power supply
47	FG/ADIN8	Motor sensing signal input/AD universal input
48	TDI/ADIN4	Open position detecting signal input/AD universal input
49	TMS/ADIN5	Close position detecting signal input/AD universal input
50	TCK/ADIN6	BA5954 enabling signal output/AD universal output
51	TDO/ADIN7	Tray close signal output/AD universal input
52、97、122、152、173、221	DVDD18	Digital 1.8V power supply

53-58	IOA2-7	Micro-controller address bit 2-7
59	HIGHA0	Micro-controller address bit 0
60、61	IOA18-19	Micro-controller address 18-19
62、85、94、116、119、134、144、148、161、163、175、216、223	DVSS	Digital grounding
63	APLLCAP	Analogue phase lock loop external capacitor
64	APLLVSS	Analogue phase lock loop grounding
65	APLLVDD3	Analogue phase lock 3.3V power supply
66	IOWR	FLASH read control signal
67-72	HIGHA3-7	Micro-controller address bit 3-7
73、80、108、127、141、155、167、182、204、212	DVDD3	Digital 3.3V power supply
74、75	HIGHA1-2	Micro-controller address bit 1-2
76	IOA20	Micro-controller address bit 20
77	IOCS	FLASH chip selection
78	IOA1	Micro-controller address bit 1
79	IOOE	FLASH output enabling
81-84	AD0-3	Micro-controller address/data bit 0-3
86-88	AD4-6	Micro-controller address/data bit 4-6
89	IOA21/ADIN0	Micro-controller address bit 21/AD universal input
90	ALE	Micro-controller address enabling
91	AD7	Micro-controller address/data bit 7
92	A17	FLASH address bit 17
93	IOA0	Micro-controller address bit 0
95	UWR	Micro-processor reading operation
96	URD	Micro-processor reading operation
98	UP1_2-1_7	Micro-processor port

104	UP3_0	Micro-processor port
105	UP3_1	Micro-processor port
106	UP3_4	Micro-processor port
107	UP3_5	Micro-processor port
109	ICE	Micro-processor correction mode enabling
110	PRST	Reset input
111	IR	Remote control signal input
112	INT0	Micro-processor interruption 0
113	DQM0	DRAM input output shielding signal
114	DQS0	DRAM input output shielding signal
115	RD7	DRAM data
117-118	RD5-6	DRAM data
120-121	RD3-4	DRAM data
123-125	RD0-2	DRAM data
126	RD15	DRAM data
128-133	RD9-14	DRAM data
135	RD8	DRAM data
136	DQS1	DRAM input output shielding signal
137	DQM1	DRAM input output shielding signal
138	RWE	DRAM writing enabling
139	CAS	DRAM column address selection
140	RAS	DRAM row address selection
142	RCS	DRAM chip selection
143	BA0	DRAM section address 0
145	BA1	DRAM section address 1
146	RA10	DRAM address
147	RA0	DRAM address
149	RA1-3	DRAM address
153	RVREF/ADIN3	Reference voltage/AD universal input
154	RCLKB	DRAM clock

156	RCLK	DRAM clock
157	CKE	DRAM clock enabling
158	RA11	DRAM address
159-160	RA8-9	DRAM address
162	RA7	DRAM address
164	RA4-6	DRAM address
168	RD13/ASDATA5	DRAM data/audio series data
169	RD27-30	DRAM data
174	RD26	DRAM data
176-177	RD24-25	DRAM data
178-179	DQM2-3	DRAM I/O shielding signal
180-181	RD22-23	DRAM data
183-188	RD16-21	DRAM data
189	DACVDDC	D/A conversion 3.3V power supply
190	VREF	Reference voltage
191	FS	
192	YUV0/CIN	
193	DACVSSC	D/A conversion grounding
194	YUV1/Y	Video signal YUV1 output/Y signal output
195	DACVDDB	D/A conversion 3.3V power supply
196	YUV2/C	Video signal YUV2 output/C signal output
197	DACVSSB	D/A conversion grounding
198	YUV3/CVBS	Video signal YUV3 output/CVBS signal output
199	DACVDDA	D/A conversion 3.3V power supply
200	YUV4/G	Video signal YUV4 output/G signal output
201	DACVSSA	D/A conversion grounding
202	TUV5/B	Video signal YUV5 output/B signal output

203	YUV6/R	Video signal YUV6 output/R signal output
205	VSYNC/ADIN1	Field synchronization signal output/AD universal input
206	YUV7/ASDATA5	Video signal YUV7 output/audio series data
207	HSYNC/ADIN2	Row synchronization output/AD universal input
208	SPMCLK	
209	SPDATA	
210	SPLRCK	
211	SPBCK/ASDATA5	
213	ALRCK	Audio left and right sound channel clock
214	ABCK	Audio bit clock
215	ACLK	Audio DAC external clock
217-220	ASDATA0-3	Audio series data
222	ASDATA4	Audio series data
224	MC_DATA	Microphone digital audio input
225	SPDIF	Digital audio signal output
226	RFGND18	RF signal grounding
227	RFVDD18	RF signal 1.8V power supply
228	XTALO	Clock output
229	XTALI	Clock input
230	JITFO	RF small signal output
231	JITFN	RF small signal phase inversion and amplification input
232	PLLVSS	Phase lock loop grounding
233	IDACEXLP	
234	PLLVDD3	Phase lock loop 3.3V power supply
235	LPFON	Amplifier loop wave filtration output
236	LPFIP	Amplifier loop wave filtration input
237	LPFIN	Amplifier loop wave filtration input

238	LPFOP	Amplifier loop wave filtration output
239	ADCVDD3	A/D conversion 3.3V power supply
240	S_VCM	
241	ADCVSS	A/D conversion grounding
242	S_VREFP	
243	S_VREFN	
244	RFVDD3	RF 3.3V power supply
245	RFRPDC	DC RF error signal input
246	RFRPAC	AC RF error signal input
247	HRFZC	High-frequency RF signal zero crossover checking
248	CRTPLP	
249	RFGND	RF grounding
250	CEQP	
251	CEQN	
252	OSP	
253	OSN	
254	RFGC	
255	IREF	Reference current
256	AVDD3	Analogue 3.3V power supply

Ⅱ.BA5954

BA5954 is a piece of servo drive single-piece integrated circuit, with built-in 4-channel BTL drive circuit. It can receive directly the PWM control signal outputted by digital servo IC, and with internal wave filter and drive amplifier, it pushes the execution part in the servo mechanism to accomplish the focusing, tracking, feed and main shaft drives. BA5954 adopts the packaging of 28 pins.

Note: The 28 pins of BA5954 are for outputting effective control signal, which is provided by the 50 pins of MT1389. When the signal is in high power level, BA5954 output is in validity, while the signal is in low power level, BA5954 will not be activated, and its output ports are in the state of cutoff.

The functions of pins of BA5954 are as the following table:

Pin	Name	Function
1	VINFC	Focusing control signal input
2	CF1	External feedback loop
3	CF2	External feedback loop
4	VINSL+	Forward control input, connected to the reference voltage
5	VINSL-	Main shaft control signal input
6	VOSL	External feedback resistance
7	VINFFC	Focusing feedback signal input
8	VCC	5V power supply
9	PVCC1	5V power supply
10	PGND	Grounding
11	VOSL-	Main shaft drive inverse voltage output
12	VO2+	Main shaft forward voltage output
13	VOFC-	Focusing drive inverse voltage output
14	VOSC+	Focusing drive forward voltage output
15	VOTK+	Tracking drive forward voltage output
16	VOTK-	Tracking drive inverse voltage output
17	VOLD+	Feed drive forward voltage output
18	VOLD-	Feed drive inverse voltage output
19	PGND	Grounding
20	VINFTK	Tracking feedback signal input
21	PVCC2	5V voltage
22	PREGND	Grounding
23	VINLD	Feed control signal input
24	CTK2	External feedback loop
25	CTK1	External feedback loop
26	VINTK	Tracking control signal input
27	BIAS	1.4 reference voltage input
28	STBY	Enabling control signal

III. 29LV160BE

29LV160BE is a type of 16Mbit FLASH memory manufactured via 0.23um technology, with 16 byte width DQ0-DQ15, memory capacity of 16M bit, operation voltage of 3.3V, and packaging method of 48 pins TSOP. The specific operation mode is as the following table:

Operation status	CE	OE	WE	RESET	A0~A19	DQ0~QD7	DQ8~DQ15	
							BYTE：high level	BYTE: Low level
Read	L	L	H	H	Ain	Dout	Dout	High resistance
Write	L	H	L	H	Ain	Din	Din	High resistance
Waiting	H	×	×	H	×	high resistance	high resistance	high resistance
Output forbidden	L	H	H	H	×	High resistance	High resistance	High resistance
Reset	×	×	×	L	×	High resistance	High resistance	High resistance

The functions of pins of 29LV160BE are as the following table:

Pin	Name	Function
15	RY/BY	Ready/system is busy
1~9、16~25 、48	A0~A19	20-byte address bus
26	CE	Chip enabling
27、46	VSS	Grounding
28	OE	Output enabling
29~36、38~44	DQ0~DQ14	15-byte data bus
37	VCC	5V power supply
45	DQ15/A-1	Character extension mode as the data line; byte expansion mode as the address line
47	BYTE	Adopting 8-byte (in low level) or 16-byte output mode (in high level)
11	WE	Write enabling
12	RESET	Reset, valid in low level
10、13、14	NC	Neutral pin

IV. AE45164016

AE45164016 is a type of 64Mb (4Banks× 1M× 16bit) CMOS synchronization DRAM, featured with large memory and high speed. Its operation power voltage is 3.0V~3.6V, and it is packaged in 54-pin TSOP.

The functions of pins of AE45164016 are as the following table:

Pin	Name	Function
1、14、27	VDD	+3.3V power supply
2、4、5、7、8、10、11、13、42、44、45、47、48、50、51、53	DQ[0~15]	16-byte data bus
3、9、43、49	VDDQ	+3.3V power supply
6、12、46、52	VSSQ	Grounding
28、41、54	VSS	Grounding
15	LDQM	Data I/O shielding signal
16	WE	Write control signal
17	CAS	Column address gate signal
18	RAS	Row address gate signal
19	CS	Chip selection signal
20	SD-BS0	Section address 0 gate signal
21	SD-BS1	Section address 1 gate signal
22~26、29~35	MA[0~11]	12-byte address bus
36、40	NC	Neutral pin
37	CKE	Clock enabling signal
38	CLK	System clock input
39	UDQM	Data I/O shielding signal

V. CS4360

CS4360 is a type of 6- channel audio D/A conversion circuit manufactured by CIRRUS LOGIC Company. It can achieve digital sound volume regulation through software, with 1dB regulation coefficient per level, 119dB attenuating scope and +3.3V or +5V voltage power supply. It adopts 28-pin packaging, and has the following characteristics:

① 24-byte sampling precision

② Maximum 192KHZ sampling frequency

③ Dynamic range: 102dB

④ Signal/noise ratio: -90dB

⑤ Low power consumption (105mW under +3.3V operation voltage)

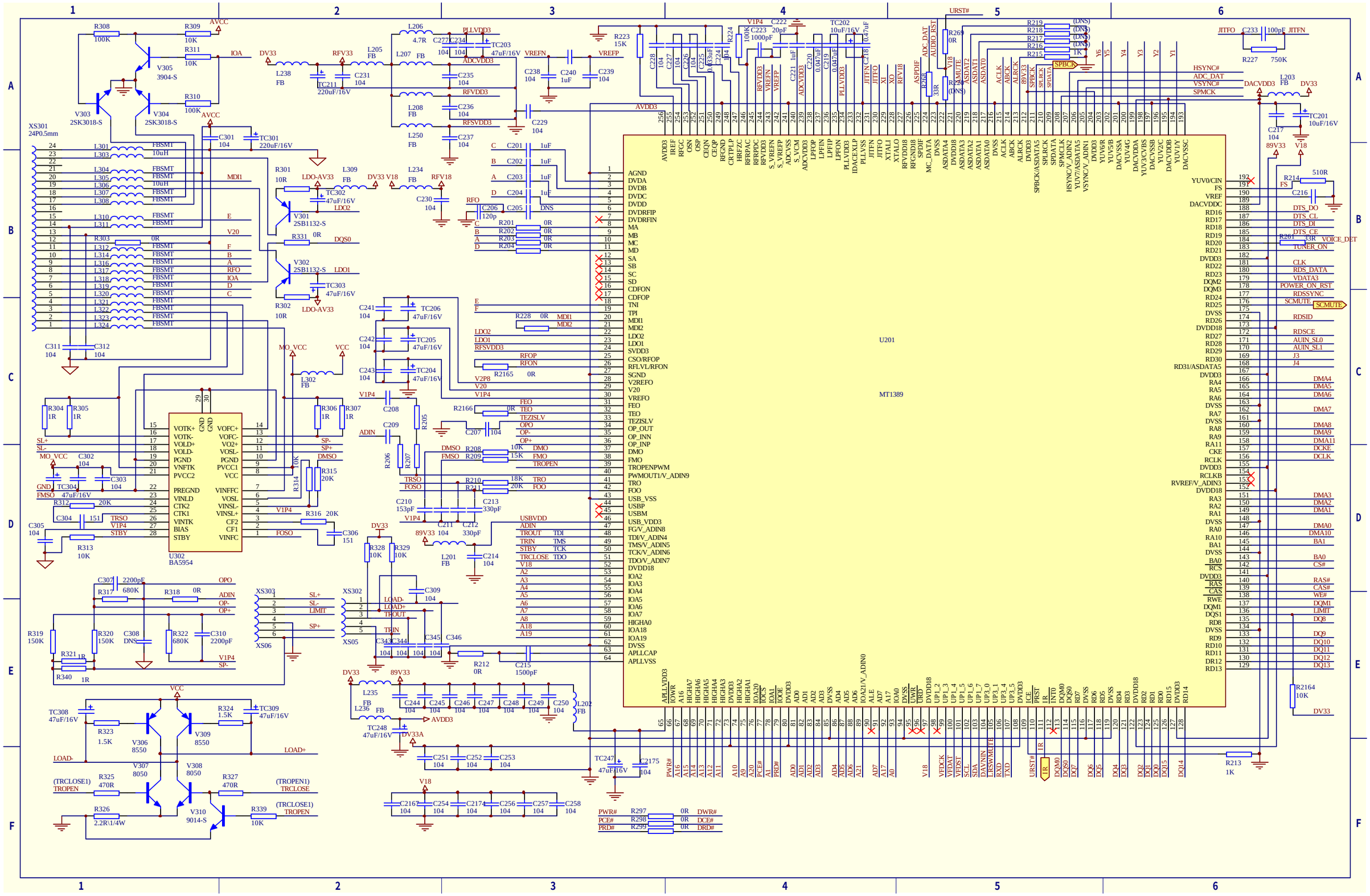
The functions of pins of CS4360 are as the following table:

Pin	Name	Function	Pin	Name	Function
1	VLS	Series audio power supply, +3.3V	15	M2	Mode 2
2	SDIN1	Series audio data 1 input	16	FILT+	In-phase feedback voltage output
3	SDIN2	Series audio data 2 input	17	VQ	Static operation voltage external wave filter
4	SDIN3	Series audio data 3 input	18	MUTEC3	3 muting control output
5	SCLK	Bit clock	19	AOUTB3	Analogue audio 3 output
6	LRCK	Left and right clock	20	AOUTA3	Analogue audio 3 output
7	MCLK	Main clock input	21	GND	Grounding
8	VD	Digital power supply	22	VA	Analogue power supply, +5V
9	GND	Grounding	23	AOUTB2	Analogue audio 2 output
10	RST	Reset input	24	AOUTA2	Analogue audio 2 output
11	SCL	Series control clock	25	MUTEC2	Output 2 muting control
12	SDA	Series control data	26	AOUTB1	Analogue audio 1 output
13	CS/M1	Chip selection/mode 1	27	AOUTA1	Analogue audio 1 output
14	VLC	Control port power supply, +3.3V	28	MUTEC1	Output 1 muting control

ATTACHMENT:

I: CIRCUIT DIAGRAM

1) DECODER BOARD:


U201
MT1389
U302
BA5954
XS301
24P0.5mm
V303
2SK3018-S
V304
2SK3018-S
V305
3904-S
V301
2SB1132-S
V302
2SB1132-S
V306
8550
V307
8050
V308
8050
V309
8550
V310
9014-S
XS303
XS302
XS05
XS06
AVCC
MO_VCC
VCC
DV33
89V33
V18
DV33A
AVDD3
ADCVDD3
RFVDD3
RFSVDD3
PLLVDD3
VREFN
VREFP
VREFO
RFOP
RFON
RFO
RFV33
RFV18
LDO-AV33
LDO1
LDO2
DQS0
MDI1
MDI2
IOA
ADIN
OPO
OP-
OP+
SP-
SP+
SL+
SL-
LIMIT
LOAD-
LOAD+
TROUT
TRIN
TRSO
FOSO
TROPEN
TRCLOSE
DMSO
FMSO
ADJ
E
F
V20
V1P4
V1P8
USBVDD
TDI
TMS
TCK
TDO
HSYNC#
ADC_DAT
VSYNC#
SPMCK
SPBCK
URST#
VOICE_DET
TUNER_ON
DTS_DO
DTS_CL
DTS_DI
DTS_CE
CLK
RDS_DATA
VDATA3
POWER_ON_RST
RDSSYNC
SCMUTE
RDSID
RDSCE
AUIN_SL0
AUIN_SL1
J3
J4
DMA0
DMA1
DMA2
DMA3
DMA4
DMA5
DMA6
DMA7
DMA8
DMA9
DMA10
DMA11
BA0
BA1
CS#
RAS#
CAS#
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DVDA
DVDB
DVDC
DVDD
DVDRFIP
DVDRFIN
MA
MB
MC
MD
SA
SB
SC
SD
CDFON
CDFOP
TNI
TPI
MDI1
MDI2
LDO2
LDO1
SVDD3
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RFLVL/RFON
SGND
V2REFO
V20
VREFO
FEO
TEO
TEZISLV
OP_OUT
OP_INN
OP_INP
DMO
FMO
TROPENPWM
PWMOUT1/V_ADIN9
TRO
FOO
USB_VSS
USBP
USBM
USB_VDD3
FG/V_ADIN8
TDI/V_ADIN4
TMS/V_ADIN5
TCK/V_ADIN6
TDO/V_ADIN7
DVDD18
IOA2
IOA3
IOA4
IOA5
IOA6
IOA7
HIGHA0
IOA18
IOA19
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APLLVSS
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VREF
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RD16
RD17
RD18
RD19
RD20
RD21
DVDD3
RD22
RD23
DQM2
DQM3
RD24
RD25
DVSS
RD26
DVDD18
RD27
RD28
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RD30
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RA3
RA2
RA1
DVSS
RA0
RA10
BA1
DVSS
BA0
RCS
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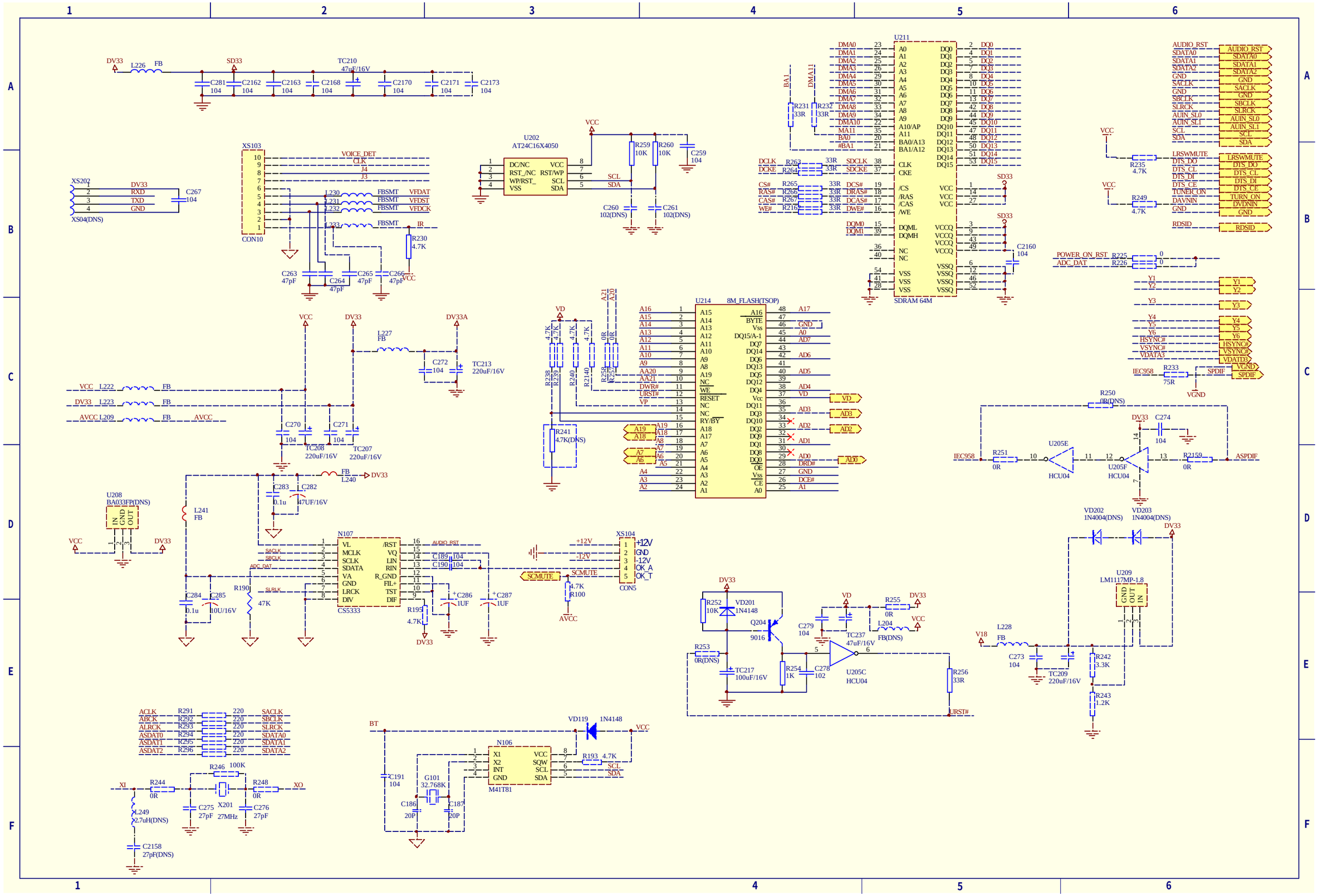
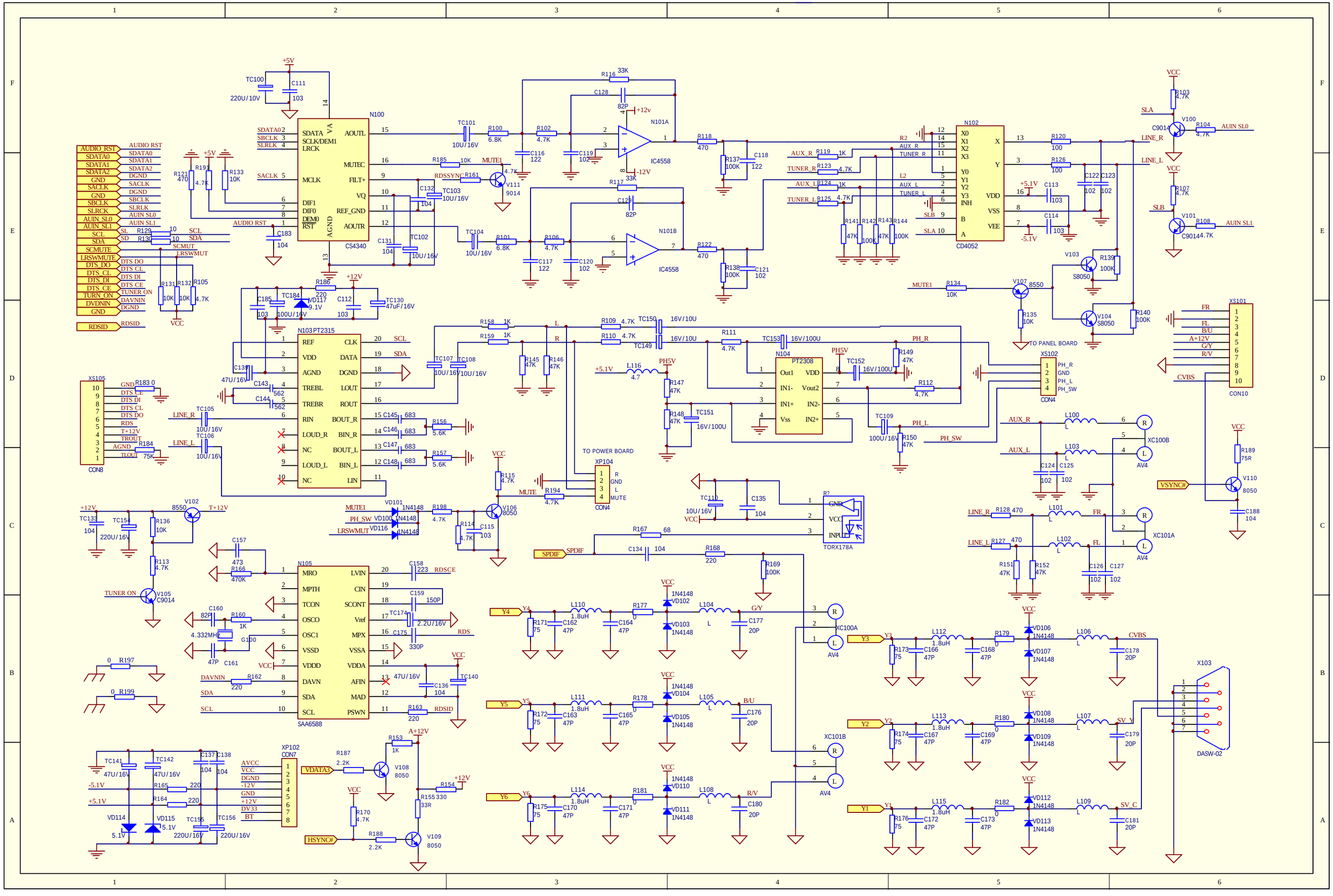
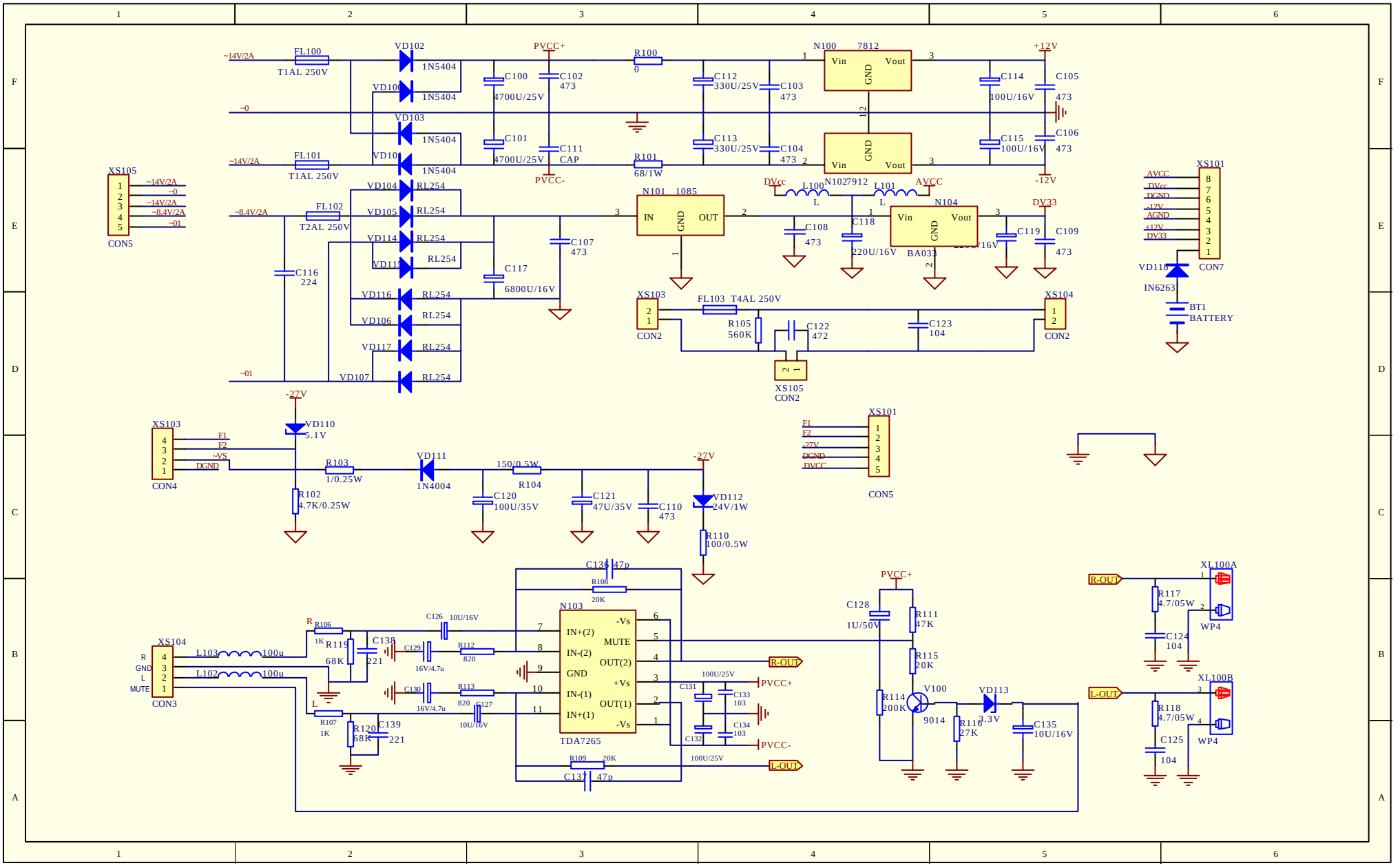
RAS
CAS
RWE
DQM1
DQS1
RD8
DVSS
RD9
RD10
RD11
DR12
RD13

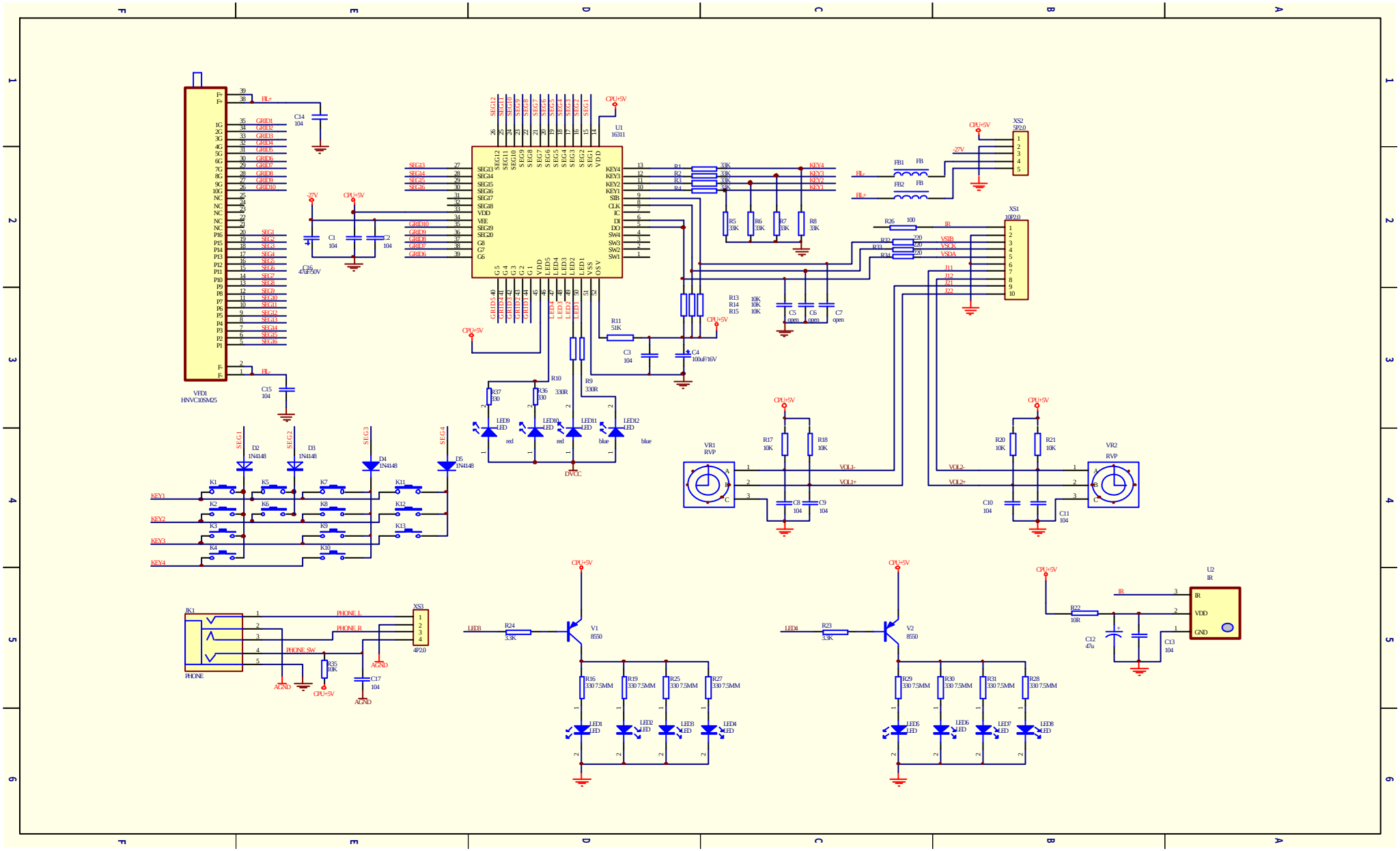

DV33
L226
FB
SD33
TC210
47uF/16V
C281 104
C2162 104
C2163 104
C2168 104
C2170 104
C2171 104
C2173 104
XS103
CON10
VOICE_DET
CLK
J4
J3
L230
L231
L232
L233
FBSMT
VFDAT
VFDST
VFDCK
IR
R230
4.7K
C263 47pF
C264 47pF
C265 47pF
C266 47pF
XS202
XS04(DNS)
C267 104
U202
AT24C16X4050
VCC
R259 10K
R260 10K
C259 104
C260 102(DNS)
C261 102(DNS)
SCL
SDA
U211
SDRAM 64M
BA1
DMA11
R231 33R
R232 33R
DCLK
DCKE
R263 33R
R264 33R
SDCLK
SDCKE
CS#
RAS#
CAS#
WE#
R265 33R
R266 33R
R267 33R
R216 33R
DCS#
DRAS#
DCAS#
DWE#
C2160 104
U214
8M_FLASH(TSOP)
VD
R238 4.7K
R239 4.7K
R240 4.7K
R2140 4.7K
R258 0R
R257 0R
R241 4.7K(DNS)
A21
A20
AUDIO_RST
SDATA0
SDATA1
SDATA2
GND
SACLK
SBCLK
SLRCK
AUIN_SL0
AUIN_SL1
SCL
SDA
LRSWMUTE
DTS_DO
DTS_CL
DTS_DI
DTS_CE
TUNER_ON
DAVNIN
DVDNIN
RDSID
R235 4.7K
R249 4.7K
POWER_ON_RST
ADC_DAT
R225 0
R226 0
Y1
Y2
Y3
Y4
Y5
Y6
HSYNC#
VSYNC#
VDATA3
IEC958
R233 75R
SPDIF
VGND
R250 0R(DNS)
R251 0R
U205E
HCU04
U205F
HCU04
C274 104
R2159 0R
ASPDIF
VCC
DV33
DV33A
L227
FB
C272 104
TC213 220uF/16V
VCC L222 FB
DV33 L223 FB
AVCC L209 FB AVCC
C270 104
C271 104
TC208 220uF/16V
TC207 220uF/16V
FB L240 DV33
C283 0.1u
C282 47UF/16V
U208
BA033FP(DNS)
IN GND OUT
L241
FB
C284 0.1u
C285 10U/16V
R190 47K
SLRLK
N107
CS5333
VL
MCLK
SCLK
SDATA
VA
GND
LRCK
DIV
/RST
VQ
LIN
RIN
R_GND
FIL+
TST
DIF
AUDIO_RST
SACLK
SBCLK
ADC_DAT
C189 104
C190 104
C286 1UF
C287 1UF
R195 4.7K
+12V
-12V
SCMUTE
XS104
CON5
+12V
GND
-12V
OK_A
OK_T
R100 4.7K
AVCC
VD202 1N4004(DNS)
VD203 1N4004(DNS)
U209
LM1117MP-1.8
GND OUT IN
V18
L228
FB
C273 104
TC209 220uF/16V
R242 3.3K
R243 1.2K
VD201 1N4148
R252 10K
Q204 9016
R253 0R(DNS)
TC217 100uF/16V
R254 1K
C278 102
C279 104
TC237 47uF/16V
U205C
HCU04
R255 0R
L204 FB(DNS)
R256 33R
URST#
ACLK
ABCK
ALRCK
ASDAT0
ASDAT1
ASDAT2
R291 220 SACLK
R292 220 SBCLK
R293 220 SLRCK
R294 220 SDATA0
R295 220 SDATA1
R296 220 SDATA2
R246 100K
R244 0R
R248 0R
XI
XO
L249 2.7uH(DNS)
C2158 27pF(DNS)
C275 27pF
X201 27MHz
C276 27pF
BT
VD119 1N4148
N106
M41T81
X1
X2
INT
GND
VCC
SQW
SCL
SDA
R193 4.7K
C191 104
G101 32.768K
C186 20P
C187 20P


N100
CS4340
N101A
N101B
IC4558
N102
CD4052
N103 PT2315
N104
PT2308
N105
SAA6588
CON8
CON4
CON10
CON7
XS101
XS102
XS105
XP102
XP104
TO POWER BOARD
TO PANEL BOARD
TORX178A
DASW-02
XC100A
XC100B
XC101A
XC101B
AV4
AUDIO RST
RDSID
SCL
SDA
SCMUT
LRSWMUT
MUTE1
VSYNC#
HSYNC#
SPDIF
TUNER ON
PH_R
PH_L
PH_SW
CVBS
SV_Y
SV_C
FR
FL
B/U
R/V
G/Y
A+12V
+12V
+5V
-5.1V
+5.1V
VCC

2)POWER BOARD



3)FRONT PANEL BOARD



II PART DATASHEET

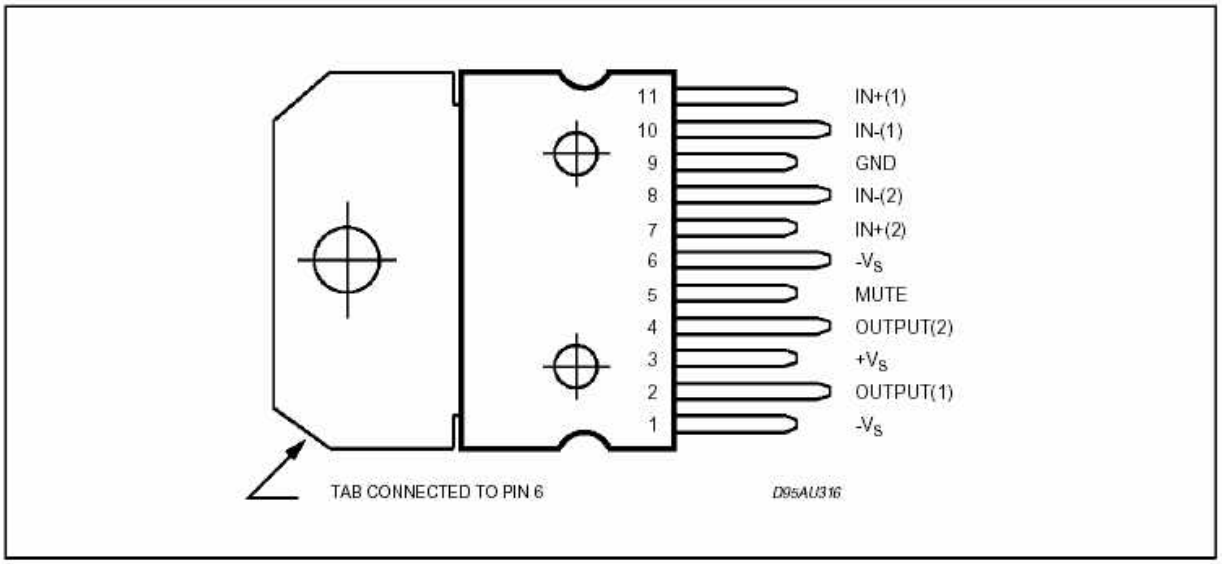
1) POWER AMPLIFIER IC TDA7265

TDA7265

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	DC Supply Voltage	±25	V
I_O	Output Peak Current (internally limited)	4.5	A
P_{tot}	Power Dissipation T_{case} = 70°C	30	W
T_{op}	Operating Temperature	-20 to 85	°C
T_{stg}, T_j	Storage and Junction Temperature	-40 to +150	°C

PIN CONNECTION (Top view)



THERMAL DATA

Symbol	Description		Value	Unit
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max	2	°C/W

ELECTRICAL CHARACTERISTICS (Refer to the test circuit, $V_S = \pm 20V$; $R_L = 8\Omega$; $R_S = 50\Omega$; $G_V = 30dB$; f = 1KHz; $T_{amb} = 25°C$, unless otherwise specified.)

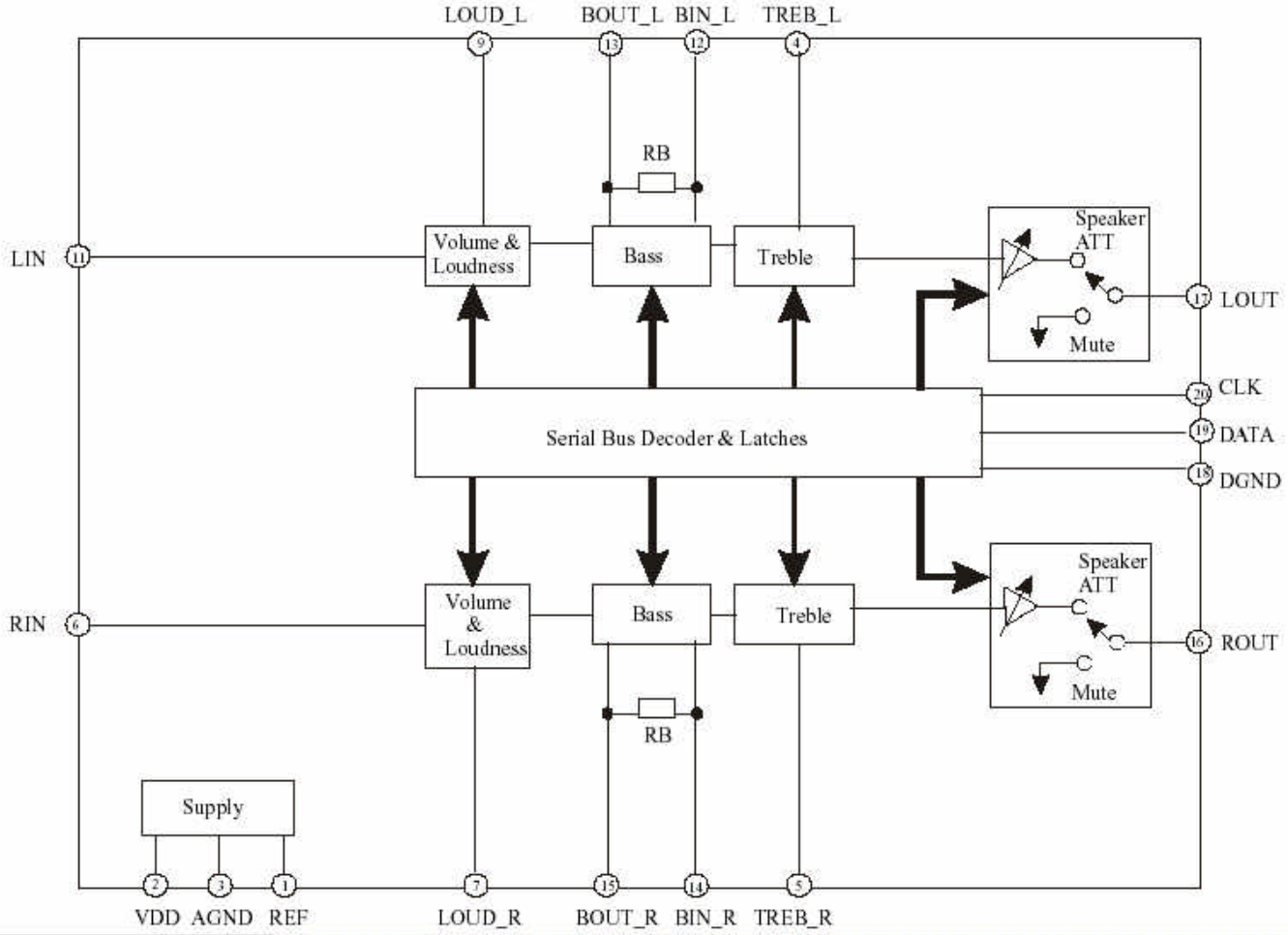
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_S	Supply Range		± 5		± 25	V
I_q	Total Quiescent Current			80	130	mA
V_{OS}	Input Offset Voltage		–20		+20	mV
I_b	Non Inverting Input Bias Current			500		nA
P_O	Music Output Power (*)	THD = 10%; $R_L = 8\Omega$; $V_S = \pm 22.5V$		32		W
P_O	Output Power	THD = 10% $R_L = 8\Omega$; $V_S \pm 16V$; $R_L = 4\Omega$	20	25 25		W W
		THD = 1% $R_L = 8\Omega$; $V_S \pm 16V$; $R_L = 4\Omega$		20 20		W W
THD	Total Harmonic Distortion	$R_L = 8\Omega$; $P_O = 1W$; f = 1KHz		0.01		%
		$R_L = 8\Omega$; $P_O = 0.1$ to 15W; f = 100Hz to 15KHz			0.7	%
		$R_L = 4\Omega$; $P_O = 1W$; f = 1KHz		0.02		%
		$R_L = 4\Omega$; $V_S \pm 16V$; $P_O = 0.1$ to 12W; f = 100Hz to 15KHz			1	%
C_T	Cross Talk	f = 1KHz f = 10KHz		70 60		dB dB
SR	Slew Rate			10		V/µs
G_{OL}	Open Loop Voltage Gain			80		dB
e_N	Total Input Noise	A Curve f = 20Hz to 22KHz		3 4	8	µV µV
R_i	Input Resistance		15	20		KΩ
SVR	Supply Voltage Rejection (each channel)	fr = 100Hz Vr = 0.5V		60		dB
T_j	Thermal Shut-down Junction Temperature			145		°C
MUTE FUNCTION [ref: +Vs]						
VT_{MUTE}	Mute / Play Threshold		-7	-6	-5	V
A_M	Mute Attenuation		60	70		dB
STAND-BY FUNCTION [ref: +Vs]						
VT_{ST-BY}	Stand-by / Mute Threshold		-3.5	-2.5	-1.5	V
A_{ST-BY}	Stand-by Attenuation			110		dB
$I_{q\ ST-BY}$	Quiescent Current @ Stand-by			3		mA

Note :
(*) **FULL POWER up to.** $V_S = \pm 22.5V$ with $R_L = 8\Omega$ and $V_S = \pm 16V$ with $R_L = 4\Omega$
MUSIC POWER is the maximal power which the amplifier is capable of producing across the rated load resistance (regardless of non linearity) 1 sec after the application of a sinusoidal input signal of frequency 1KHz.

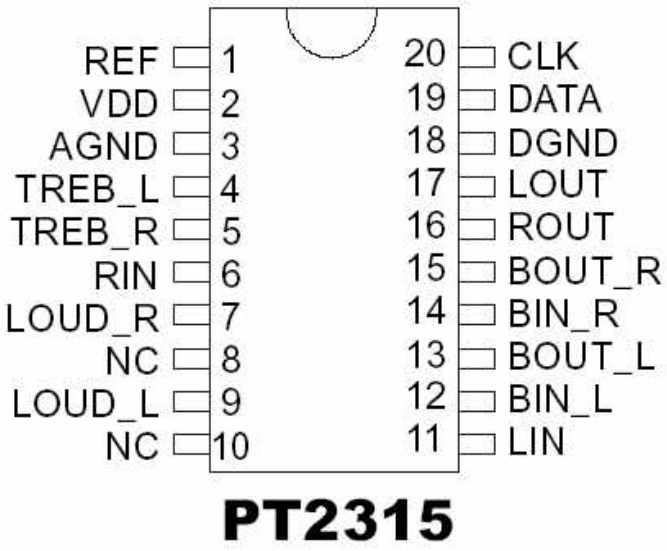
2) DIGITAL VOLUME CONTROL

2-Channel Audio Processor IC PT2315

Block Diagram



Pin Configuration



PT2315

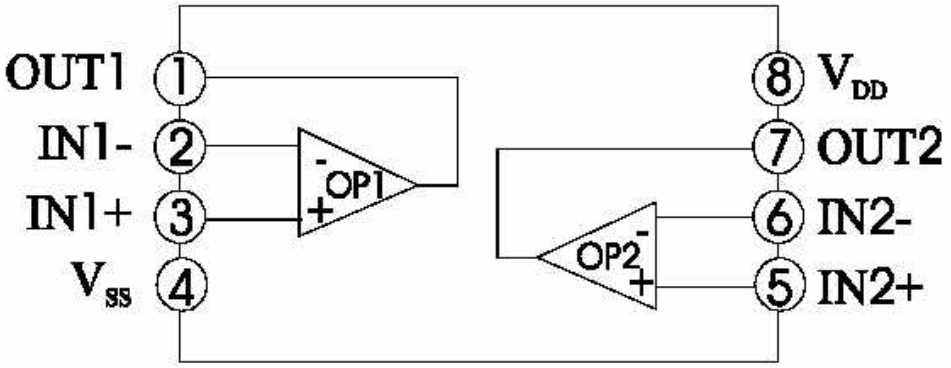
3) HEADPHONE DRIVER

ELECTRICAL PARAMETERS

(Unless otherwise stated, V_{DD}=5V, Vss=0V, Tamb=25°C, fin=1 KHz, R_L=32 Ohms)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
VDD	Single Supply Voltage		3.0	5.0	7.0	V
	Dual Supply Voltage		1.5	2.5	3.5	V
VSS	Negative Power Supply		-1.5	-2.5	-3.5	V
IDD	Supply Current	No Load	-	7.0	-	mA
Ptot	Total Power Dissipation	No Load	-	35	-	mW
Po	Maximum Output Power		-	60	-	mW
THD	Total Harmonic Distortion	Vo(p-p)=3.5V	-	0.03	0.06	%
		Vo(p-p)=3.5V R_L=5 K Ohms	-	0.001	-	
S/N	Signal-to-Noise Ratio		100	110	-	dB
α_{CS}	Channel Separation		-	70	-	dB
		R_L=5 K Ohms	-	105	-	
PSRR	Power Supply Ripple Rejection	fin=100Hz Vripple(p-p)=100mV	-	90	-	dB

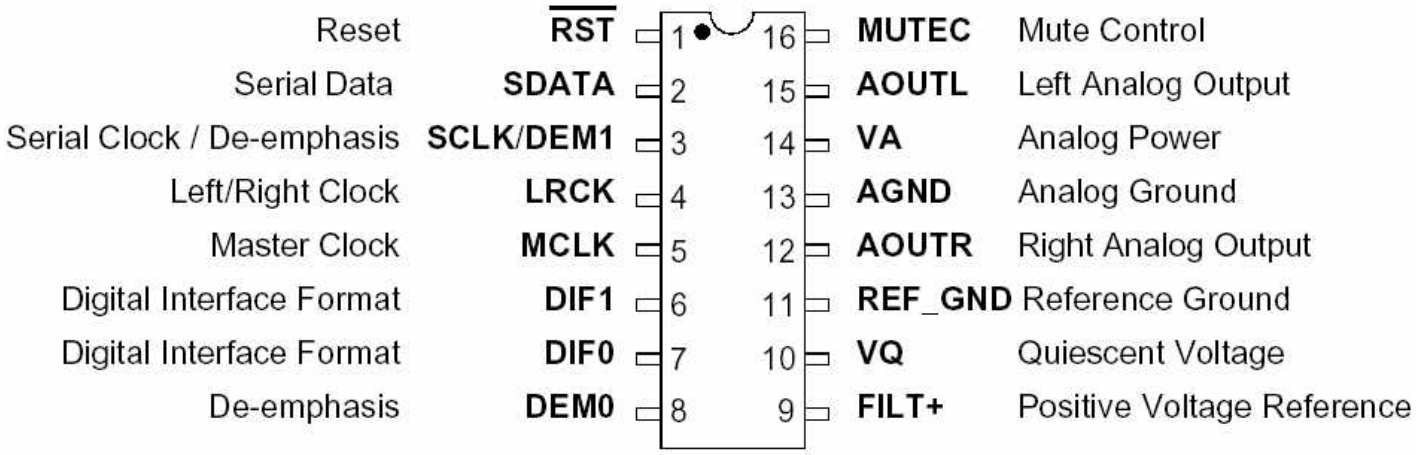
BLOCK DIAGRAM



PT2308

4)DAC –CS4340

PIN DESCRIPTION



POWER AND THERMAL CHARACTERISTICS

Parameters		Symbol	Min	Typ	Max	Units
Power Supplies						
Power Supply Current VA = 5 V	normal operation power-down state	I_A I_A	- -	15 60	17 -	mA µA
Power Dissipation VA = 5 V	(Note 7) normal operation power-down		- -	75 0.3	85 -	mW mW
Power Supply Current VA = 3 V	normal operation power-down state	I_A I_A	- -	10 30	14 -	mA µA
Power Dissipation VA = 3 V	(Note 7) normal operation power-down		- -	30 0.09	42 -	mW mW
Package Thermal Resistance		θ_{JA}	-	110	-	°C/Watt
Power Supply Rejection Ratio (1 kHz)	(Note 8) (60 Hz)	PSRR	- -	60 40	- -	dB dB

Notes: 7. Refer to Figure 15.

8. Valid with the recommended capacitor values on FILT+ and VQ as shown in Figure 1. Increasing the capacitance will also increase the PSRR.

DIGITAL CHARACTERISTICS (T_A = 25°C; VA = 2.7 V - 5.5 V)

Parameters		Symbol	Min	Typ	Max	Units
High-Level Input Voltage	VA = 5 V VA = 3 V	V_{IH}	2.0 2.0	- -	- -	V V
Low-Level Input Voltage	VA = 5 V VA = 3 V	V_{IL}	- -	- -	0.8 0.8	V V
Input Leakage Current		I_{in}	-	-	±10	µA
Input Capacitance			-	8	-	pF
Maximum MUTEC Drive Current			-	3	-	mA

ABSOLUTE MAXIMUM RATINGS (AGND = 0 V; all voltages with respect to ground.)

Parameters	Symbol	Min	Max	Units
DC Power Supply	VA	-0.3	6.0	V
Input Current, Any Pin Except Supplies	I_{in}	-	±10	mA
Digital Input Voltage	V_{IND}	-0.3	VA+0.4	V
Ambient Operating Temperature (power applied)	T_A	-55	125	°C
Storage Temperature	T_{stg}	-65	150	°C

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

5)RDS DECODER –SAA6588

PINNING

SYMBOL	PIN	DESCRIPTION
MRO	1	multi-path rectifier output
MPTH	2	multi-path detector output
TCON	3	test control input pin
OSCO	4	oscillator output
OSCI	5	oscillator input
V_{SSD}	6	digital ground (0 V)
V_{DDD}	7	digital supply voltage (5 V)
DAVN	8	data available output (active LOW)
SDA	9	I^2C-bus serial data I/O
SCL	10	I^2C-bus serial clock input

SYMBOL	PIN	DESCRIPTION
PSWN	11	pause switch output (active LOW)
MAD	12	slave address (LSB) input
AFIN	13	audio signal input
V_{DDA}	14	analog supply voltage (5 V)
V_{SSA}	15	analog ground (0 V)
MPX	16	multiplex input signal
V_{ref}	17	reference voltage output
SCOUT	18	band-pass filter output
CIN	19	comparator input
LVIN	20	level input

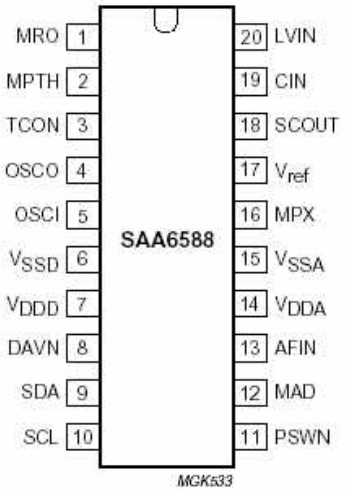


Fig.2 Pin configuration (DIP20).

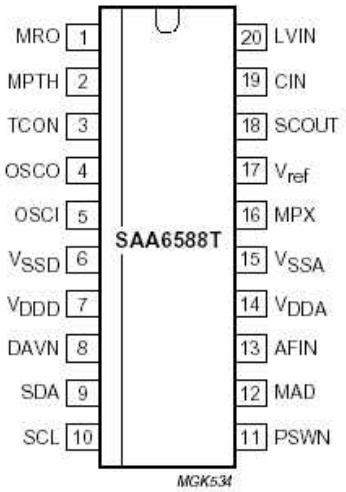
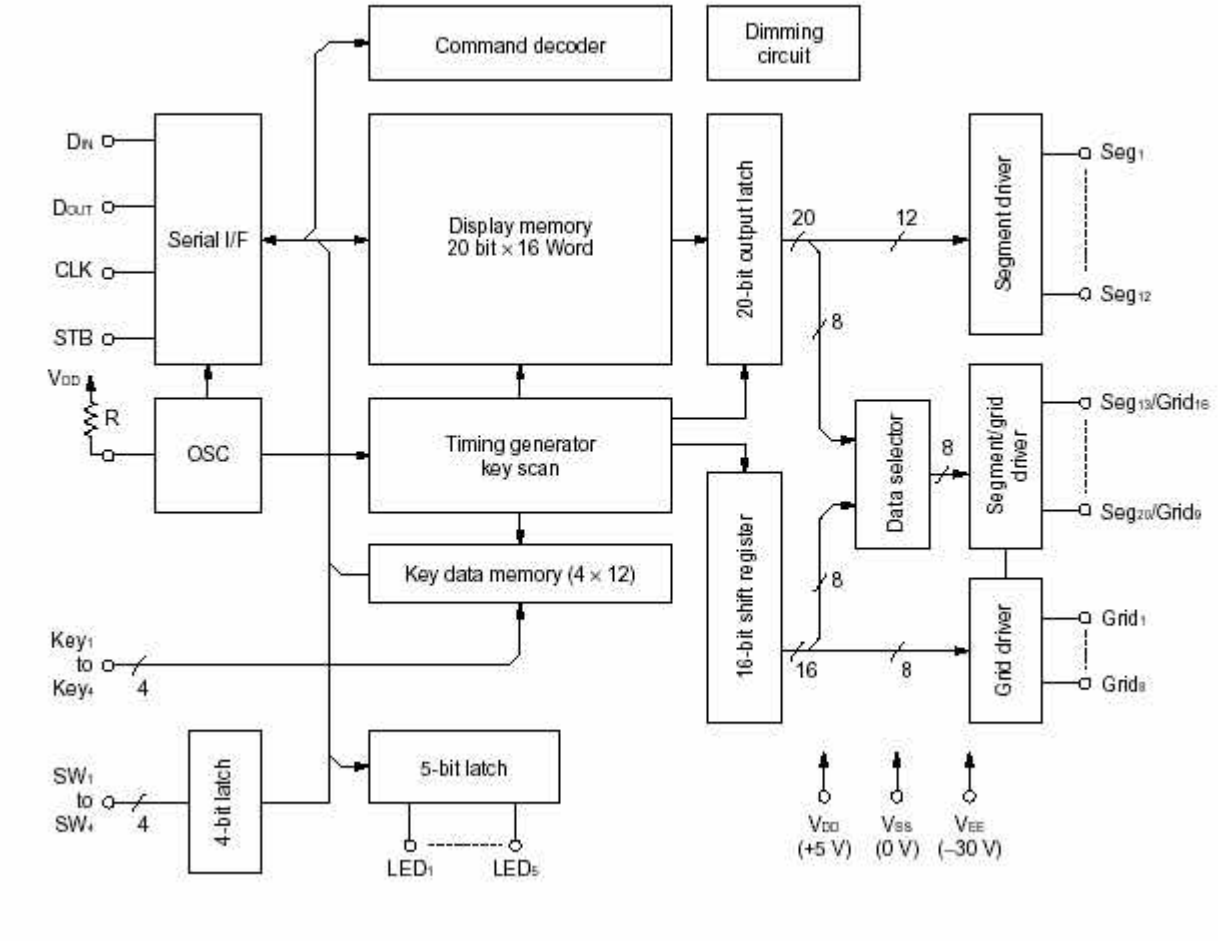


Fig.3 Pin configuration (SO20).

6) VFD DRIVER

BLOCK DIAGRAM



PIN CONFIGURATION (Top View)