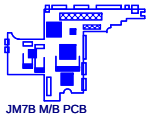

JM7B-DISCRETE

PWA FP384, PWB UW445,
SCHEM KU954. (256MB)
VER : 2A

POWER

- SYSTEM RESET CIRCUIT — PG 44
- BATT SELECTOR — PG 45
- BATT CHARGER — PG 46
- RUN POWER SW — PG 53
  +3.3V_SUS/+5V_SUS
  +5V/+3.3V/+1.8V

AC/BATT CONNECTOR PG 54

Merom
(478 Micro-FCPGA)
PG 3,4
(Symbol Rev.09)

667/800 MHz FSB

POWER

- VGA DC/DC — PG 50
- CPU VR — PG 51
- DC/DC — PG 52
  +3.3V_ALW/+5V_ALW/+15V_ALW
- REGULATOR — PG 47
  +1.8V_SUS/+0.9V_DDR_VTT
- REGULATOR — PG 48
  +1.25V_RUN/+1.05V_VCCP/
  +1.25V_GFX_PCIe
- REGULATOR — PG 49
  +1.5V_RUN

CLOCK
CK410M+LP
PG 17

DDR2-SODIMM1 PG 15,16
533/667 MHZ DDR II

DDR2-SODIMM2 PG 15,16
533/667 MHZ DDR II

Crestline
1299 uFCBGA
PG 5,6,7,8,9,10
(Symbol Rev.09)

PCIEx16

nVIDIA G86/G72M
PCI EXPRESS GFX
PG 18,19,20,21,22

LVDS — **Panel Connector** PG 24
DVI
TVOUT — **MINI DIN 7** PG 23 3
VGA — **CRT CONN.** PG 25

USB2.0 (P0,P1) (EXT SIDE)
USB2.0 (P2,P3) (EXT BACK)
USB2.0 (P8)
POWER USB & USB PG 33

Internal Media Bay
CD-ROM PG 26
IDE

DMI interface

33MHz PCI

Q-SWITCH PG 42

DOCKING CONNECTOR
PG 43

USB1.0

SMART CARD
OZ77CR6LN
PG 28

SATA - HDD PG 26
SATA
USB2.0 (P4)

ICH8-M
676 BGA
PG 11,12,13,14
(Symbol Rev.09)

IHDA

PCIEx1
USB2.0 (P6)
PCIEx2
USB2.0 (P9)
USB2.0 (P7)

CARDBUS/1394
OZ711EZ1TN
PG 27

EXPRESS-CARD
R5538
PG 28

MINI-CARD
WLAN
PG 29

MINI-CARD
WWAN
PG 29

AUDIO/AMP PG 38,39

MDC PG 30

SPI
LPC

USB2.0 (P5)
Biometric PG 35

PCIEx1

Bluetooth PG 35

S/PDIF for Dock PG 43

Audio Jacks PG 39

RJ11 for Dock PG 43

Tip Ring PG 30

S/PDIF for MINI DIN 7 PG 23 3

Keyboard Controllor ECE1077 PG 34
BC

SIO
MEC5025
128KB Flash
TMKBC
128 Pins VTQFP
PG 31

BC

SIO 32
ECE5028
128 Pins VTQFP
PG 32

BCM5755M /BCM5752 PG 40

E-Switch
PI3L500
+3.3V_LAN
PG 41

RJ45/Magnetics PG 41

DOCK LPC

SPI
PS/2

USER INTERFACE PG 36

Keyboard PG 36

FLASH PG 34

Touchpad/ Stick point PG 35

Serial Port PG 33

IrDA PG 35

FAN & THERMAL
EMC4001
PG 37

QUANTA COMPUTER

Title	Schematic Block Diagram	
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INDEX

Power States

Power Rail	Control Signal	S0/M0	S3/M1	S3/M1	S4/M1	S3/ M-off	S4/ M-off	S5/ M-off
+3.3V_ALW								
+5V_ALW								
+3.3V_LAN								
+1.25V_SRC_M								
+1.05V_M								
+1.8V_SUS								
+0.9V_DDR_VTT								
+5V_SUS								
+3.3V_SUS								
+5V_RUN								
+3.3V_RUN								
+1.8V_RUN								
+1.25V_RUN								
+1.5V_RUN								
+1.05V_VCCP								
VCC_VCRE								
+LCDVCC								
+5V_MOD								
+VCC_GFX_CORE								
+1.25V_GFX_PCIe								
+2.5V_RUN								

QUANTA COMPUTER

Title	Index & Power Status	
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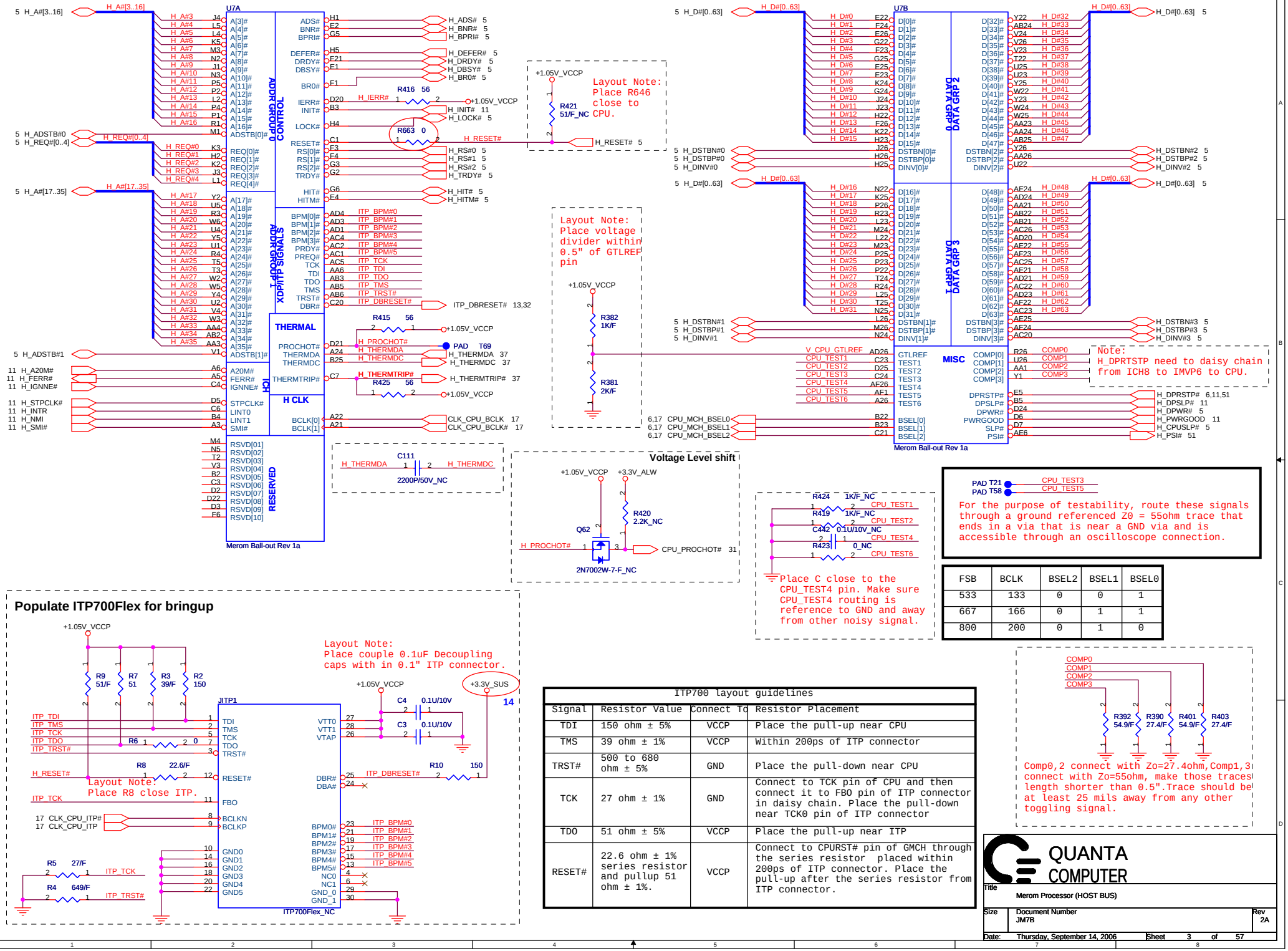

FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0

ITP700 layout guidelines

Signal	Resistor Value	Connect To	Resistor Placement
TDI	150 ohm ± 5%	VCCP	Place the pull-up near CPU
TMS	39 ohm ± 1%	VCCP	Within 200ps of ITP connector
TRST#	500 to 680 ohm ± 5%	GND	Place the pull-down near CPU
TCK	27 ohm ± 1%	GND	Connect to TCK pin of CPU and then connect it to FBO pin of ITP connector in daisy chain. Place the pull-down near TCK0 pin of ITP connector
TDO	51 ohm ± 5%	VCCP	Place the pull-up near ITP
RESET#	22.6 ohm ± 1% series resistor and pullup 51 ohm ± 1%.	VCCP	Connect to CPURST# pin of GMCH through the series resistor placed within 200ps of ITP connector. Place the pull-up after the series resistor from ITP connector.

QUANTA COMPUTER

Title	Merom Processor (HOST BUS)	
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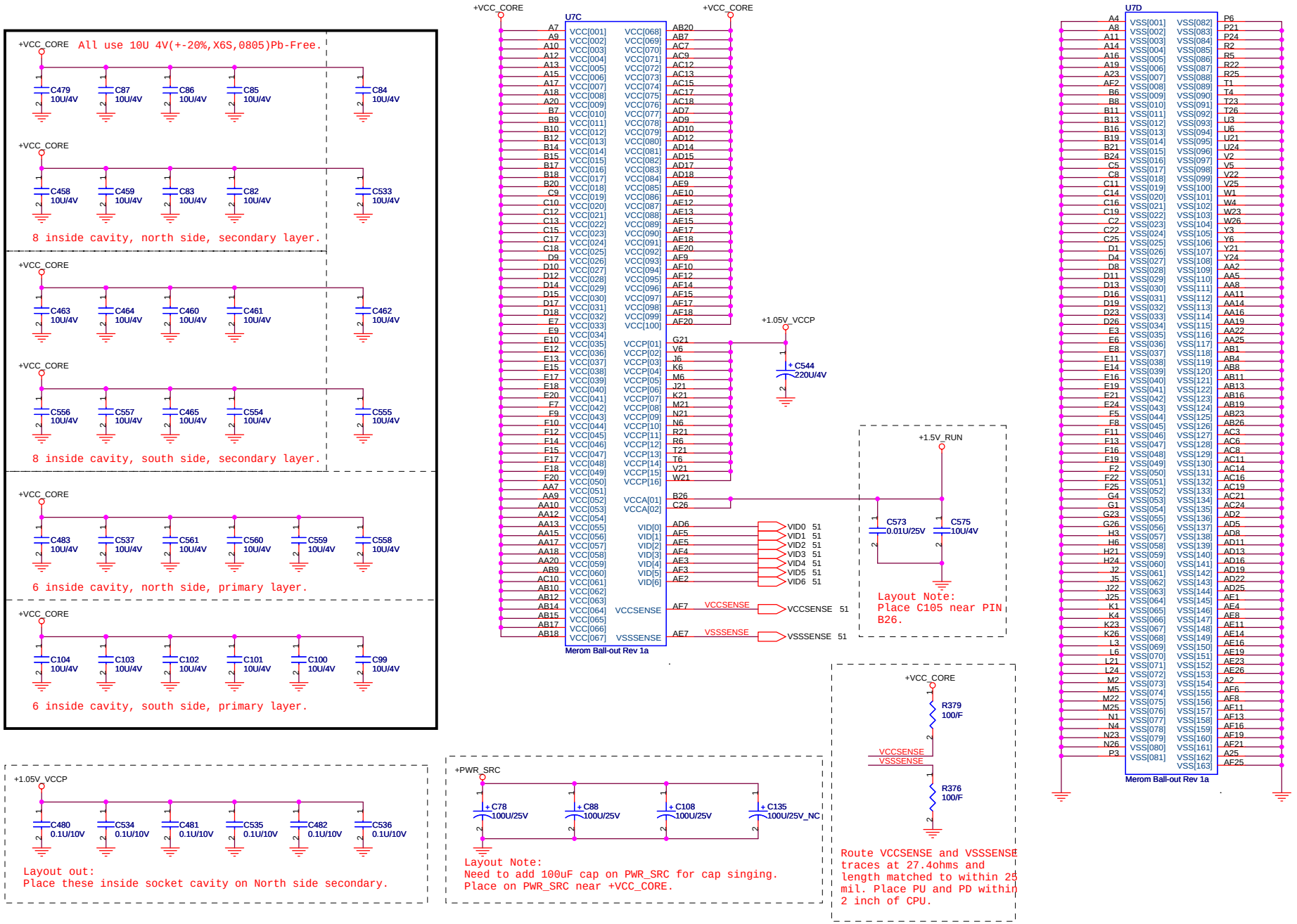

QUANTA COMPUTER

Title	Merom Processor (POWER)	
Size	Document Number JM7B	Rev 2A
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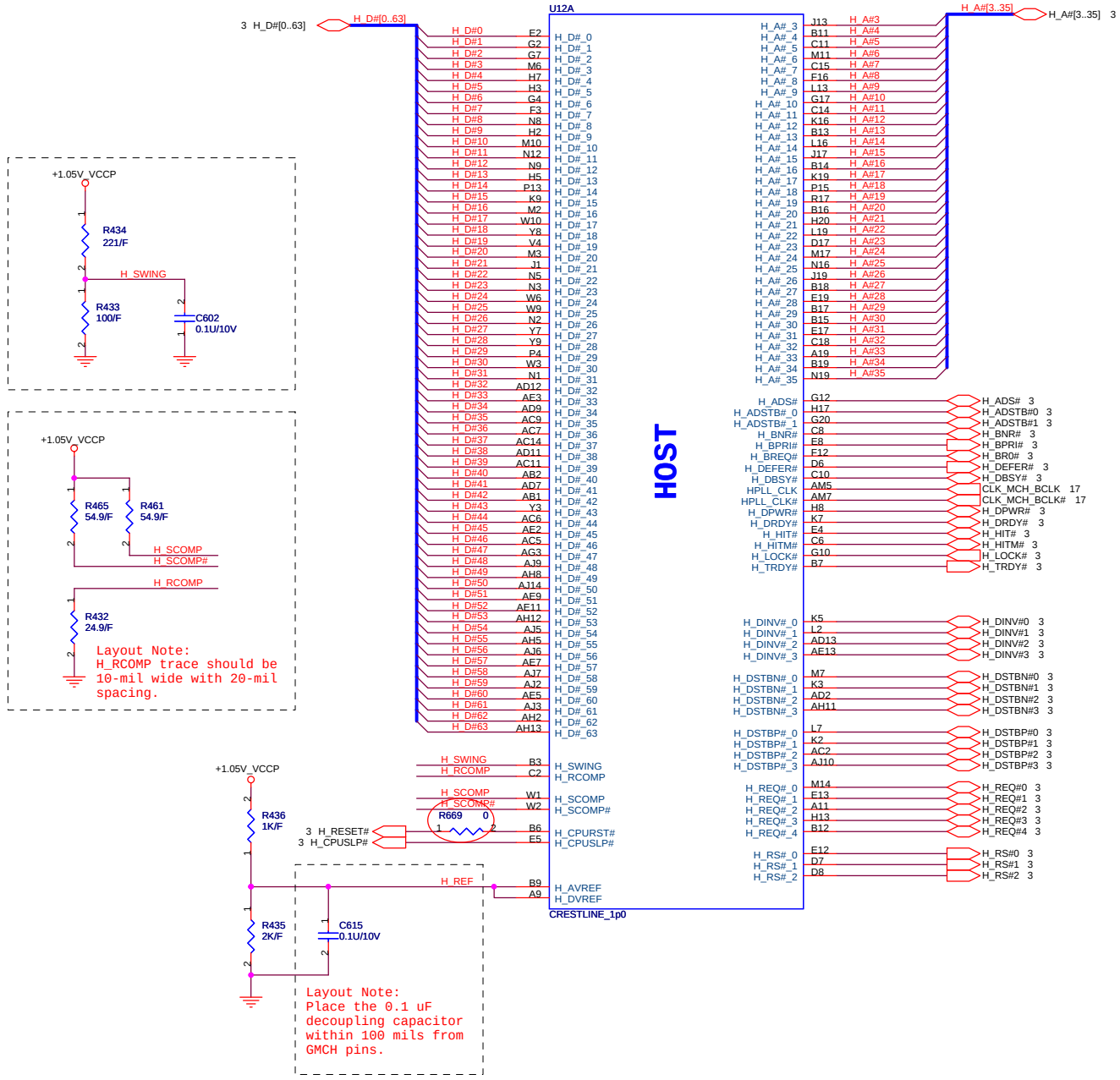

Title	Crestline (HOST)				
Size	Document Number JM7B			Rev 2A	
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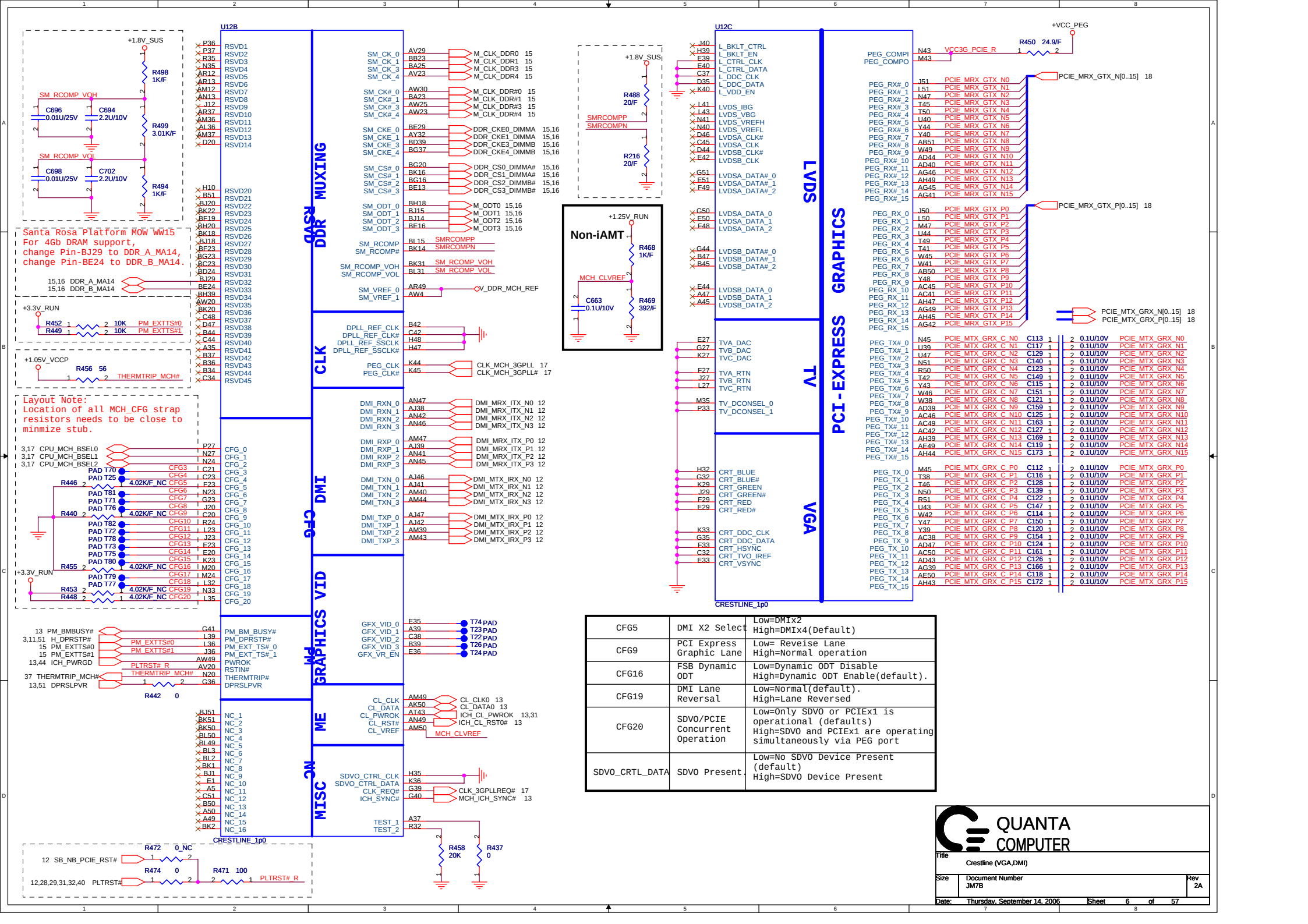

CFG5	DMI X2 Select	Low=DMIx2 High=DMIx4(Default)
CFG9	PCI Express Graphic Lane	Low= Reveise Lane High=Normal operation
CFG16	FSB Dynamic ODT	Low=Dynamic ODT Disable High=Dynamic ODT Enable(default).
CFG19	DMI Lane Reversal	Low=Normal(default). High=Lane Reversed
CFG20	SDVO/PCIE Concurrent Operation	Low=Only SDVO or PCIEx1 is operational (defaults) High=SDVO and PCIEx1 are operating simultaneously via PEG port
SDVO_CRTL_DATA	SDVO Present.	Low=No SDVO Device Present (default) High=SDVO Device Present

QUANTA COMPUTER

Title	Crestline (VGA,DMI)	
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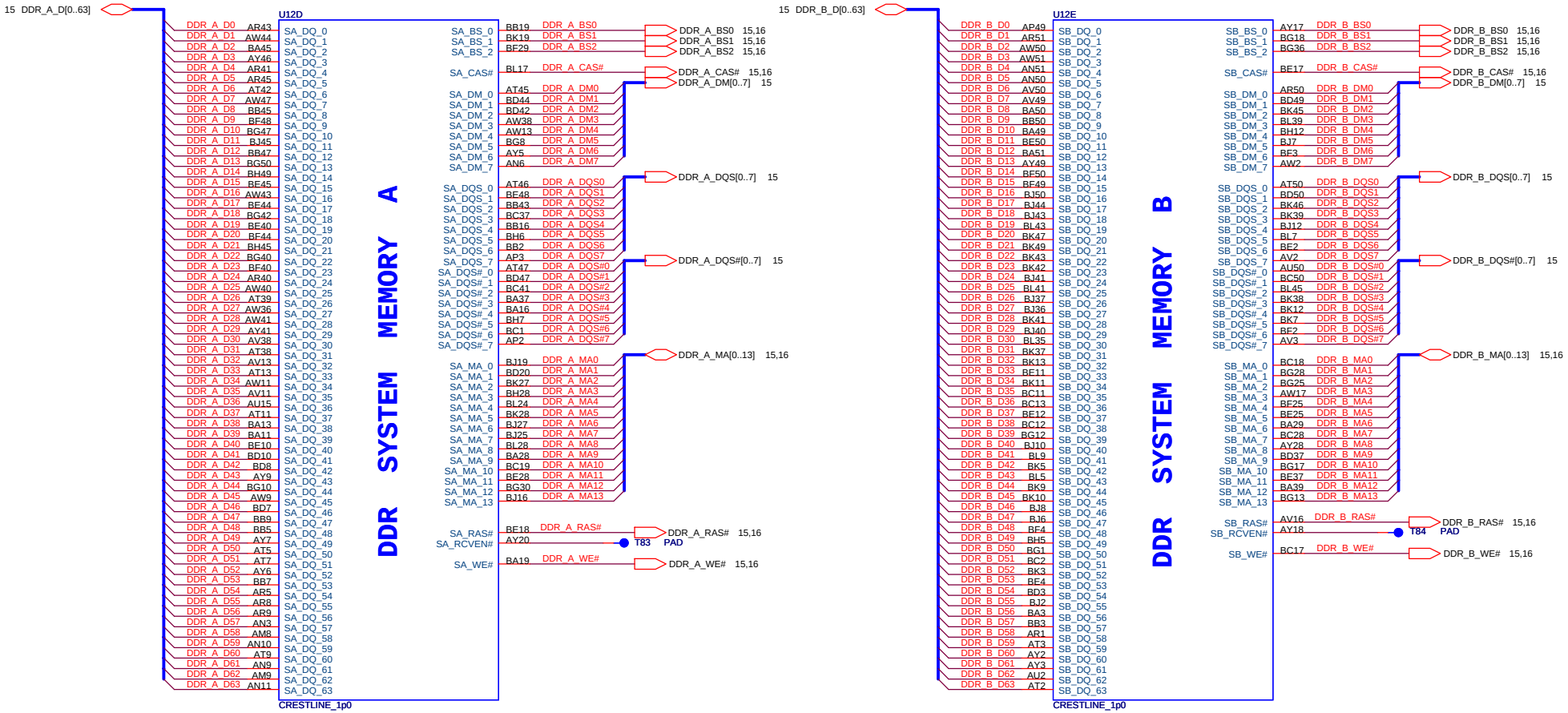

QUANTA COMPUTER

Title	Crestline (DDR2)	
Size	Document Number JM7B	Rev 2A
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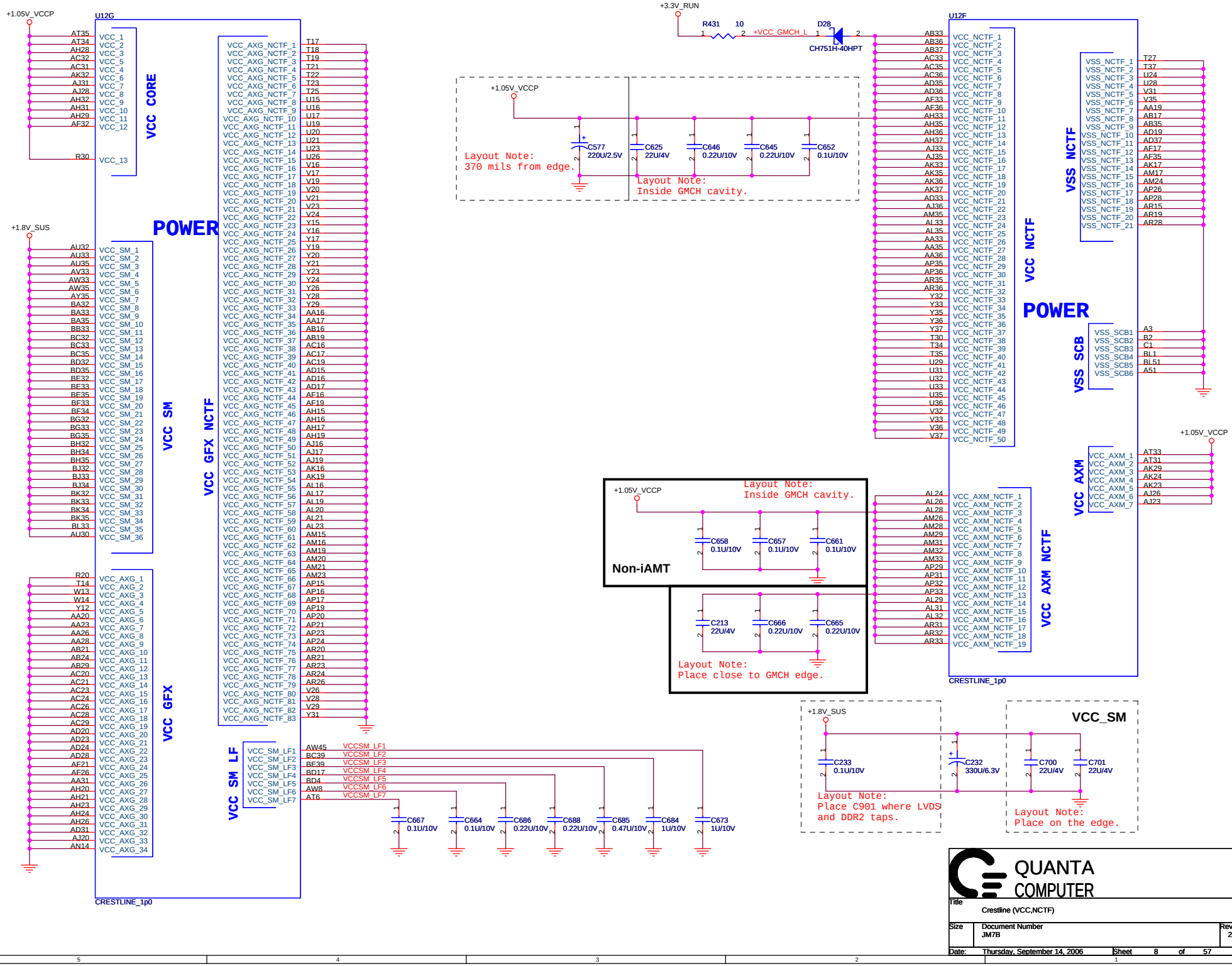

Title	Crestline (VCC,NCTF)	
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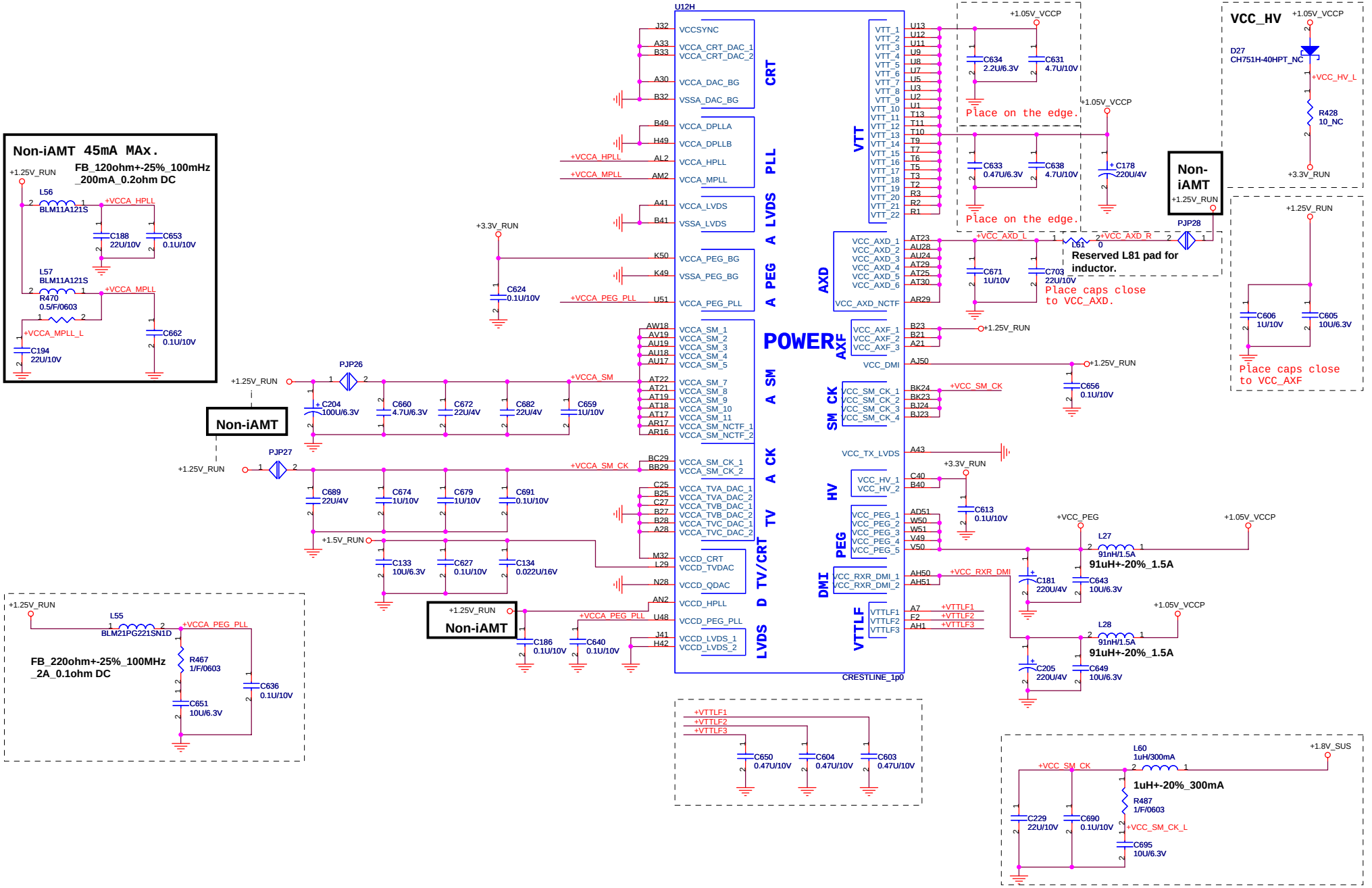

Title	Crestline (POWER)	
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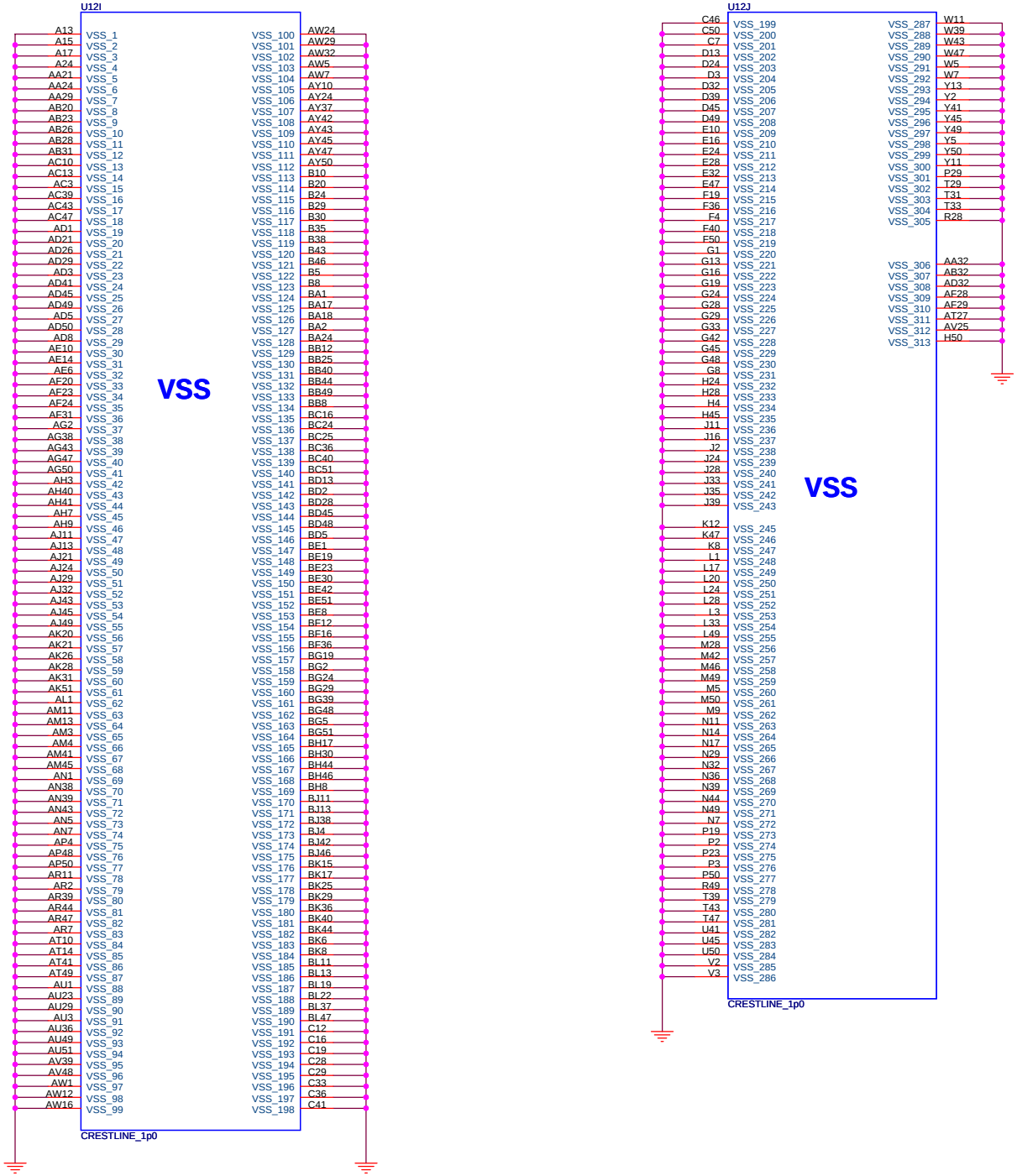
QUANTA COMPUTER



QUANTA COMPUTER		
Title	Crestline (VSS)	
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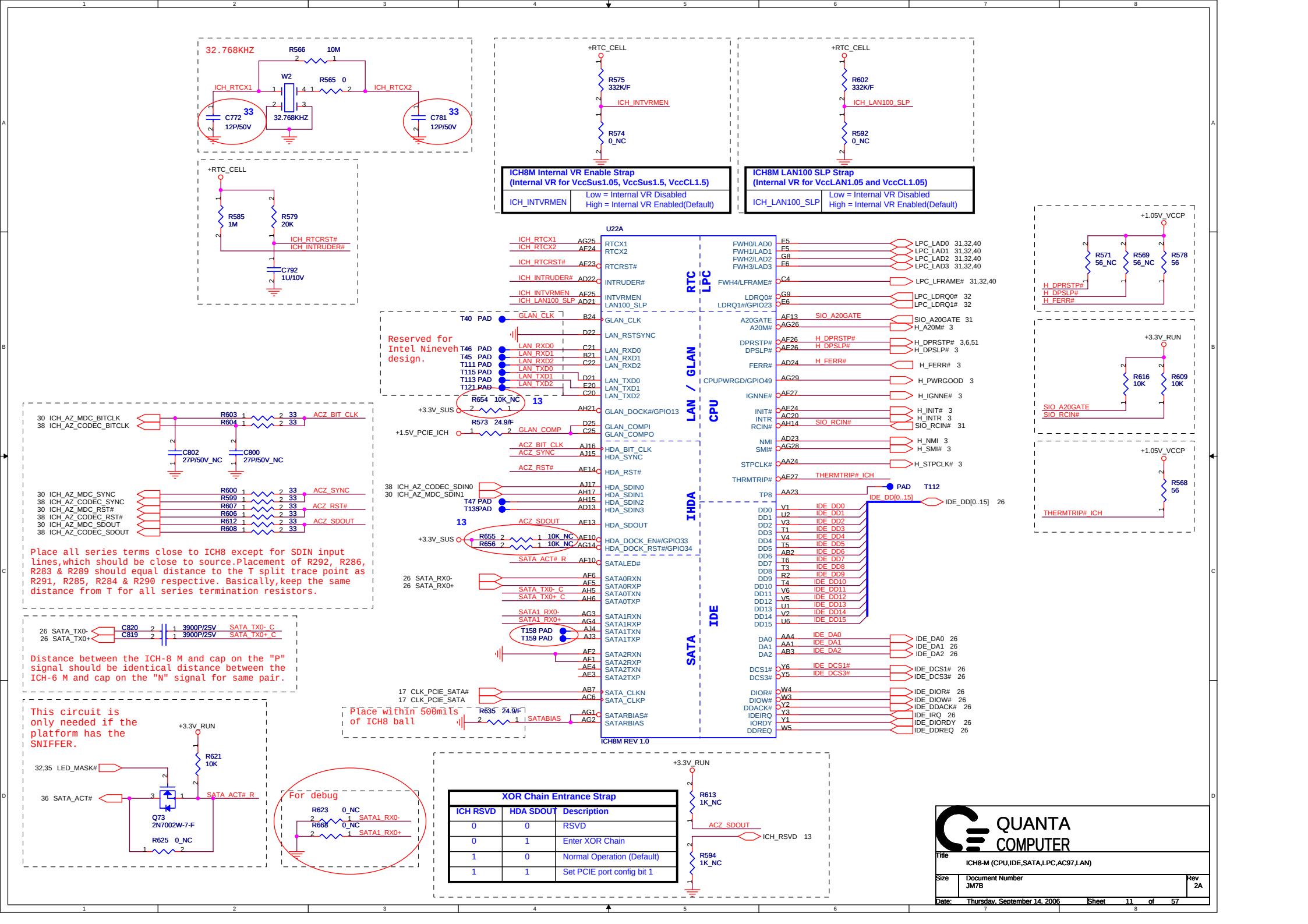
32.768KHZ
R566 10M
W2
R565 0
ICH_RTCX1
ICH_RTCX2
C772 33 12P/50V
32.768KHZ
C781 33 12P/50V
+RTC_CELL
R585 1M
R579 20K
ICH_RTCRST#
ICH_INTRUDER#
C792 1U/10V
+RTC_CELL
R575 332K/F
ICH_INTVRMEN
R574 0_NC
ICH8M Internal VR Enable Strap
(Internal VR for VccSus1.05, VccSus1.5, VccCL1.5)
ICH_INTVRMEN
Low = Internal VR Disabled
High = Internal VR Enabled(Default)
+RTC_CELL
R602 332K/F
ICH_LAN100_SLP
R592 0_NC
ICH8M LAN100 SLP Strap
(Internal VR for VccLAN1.05 and VccCL1.05)
ICH_LAN100_SLP
Low = Internal VR Disabled
High = Internal VR Enabled(Default)
U22A
RTC
LPC
GLAN
CPU
IHDA
IDE
SATA
RTCX1
RTCX2
RTCRST#
INTRUDER#
INTVRMEN
LAN100_SLP
GLAN_CLK
LAN_RSTSYNC
LAN_RXD0
LAN_RXD1
LAN_RXD2
LAN_TXD0
LAN_TXD1
LAN_TXD2
GLAN_DOCK#/GPIO13
GLAN_COMPI
GLAN_COMPO
HDA_BIT_CLK
HDA_SYNC
HDA_RST#
HDA_SDIN0
HDA_SDIN1
HDA_SDIN2
HDA_SDIN3
HDA_SDOUT
HDA_DOCK_EN#/GPIO33
HDA_DOCK_RST#/GPIO34
SATALED#
SATA0RXN
SATA0RXP
SATA0TXN
SATA0TXP
SATA1RXN
SATA1RXP
SATA1TXN
SATA1TXP
SATA2RXN
SATA2RXP
SATA2TXN
SATA2TXP
SATA_CLKN
SATA_CLKP
SATARBIAS#
SATARBIAS
FWH0/LAD0
FWH1/LAD1
FWH2/LAD2
FWH3/LAD3
FWH4/LFRAME#
LDRQ0#
LDRQ1#/GPIO23
A20GATE
A20M#
DPRSTP#
DPSLP#
FERR#
CPUPWRGD/GPIO49
IGNNE#
INIT#
INTR
RCIN#
NMI
SMI#
STPCLK#
THRMTRIP#
TP8
DD0
DD1
DD2
DD3
DD4
DD5
DD6
DD7
DD8
DD9
DD10
DD11
DD12
DD13
DD14
DD15
DA0
DA1
DA2
DCS1#
DCS3#
DIOR#
DIOW#
DDACK#
IDEIRQ
IORDY
DDREQ
ICH8M REV 1.0
Reserved for Intel Nineveh design.
T40 PAD
T46 PAD
T45 PAD
T111 PAD
T115 PAD
T113 PAD
T121 PAD
R654 10K_NC
R573 24.9/F
T47 PAD
T133 PAD
R655 10K_NC
R656 10K_NC
T158 PAD
T159 PAD
R635 24.9/F
Place within 500mils of ICH8 ball
30 ICH_AZ_MDC_BITCLK
38 ICH_AZ_CODEC_BITCLK
R603 33
R604 33
ACZ_BIT_CLK
C802 27P/50V_NC
C800 27P/50V_NC
30 ICH_AZ_MDC_SYNC
38 ICH_AZ_CODEC_SYNC
30 ICH_AZ_MDC_RST#
38 ICH_AZ_CODEC_RST#
30 ICH_AZ_MDC_SDOUT
38 ICH_AZ_CODEC_SDOUT
R600 33
R599 33
R607 33
R606 33
R612 33
R608 33
ACZ_SYNC
ACZ_RST#
ACZ_SDOUT
Place all series terms close to ICH8 except for SDIN input lines,which should be close to source.Placement of R292, R286, R283 & R289 should equal distance to the T split trace point as R291, R285, R284 & R290 respective. Basically,keep the same distance from T for all series termination resistors.
26 SATA_TX0-
26 SATA_TX0+
C820 3900P/25V
C819 3900P/25V
SATA_TX0- C
SATA_TX0+ C
Distance between the ICH-8 M and cap on the "P" signal should be identical distance between the ICH-6 M and cap on the "N" signal for same pair.
This circuit is only needed if the platform has the SNIFFER.
+3.3V_RUN
R621 10K
32,35 LED_MASK#
36 SATA_ACT#
Q73 2N7002W-7-F
SATA_ACT# R
R625 0_NC
For debug
R623 0_NC
R668 0_NC
SATA1_RX0-
SATA1_RX0+
XOR Chain Entrance Strap
ICH RSVD
HDA SDOUT
Description
0 0 RSVD
0 1 Enter XOR Chain
1 0 Normal Operation (Default)
1 1 Set PCIE port config bit 1
+3.3V_RUN
R613 1K_NC
ACZ_SDOUT
ICH_RSVD 13
R594 1K_NC
+1.05V_VCCP
R571 56_NC
R569 56_NC
R578 56
H_DPRSTP#
H_DPSLP#
H_FERR#
+3.3V_RUN
R616 10K
R609 10K
SIO_A20GATE
SIO_RCIN#
+1.05V_VCCP
R568 56
THERMTRIP#_ICH
QUANTA COMPUTER
Title
ICH8-M (CPU,IDE,SATA,LPC,AC97,LAN)
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Place TX DC blocking caps close ICH8.

29 PCIE_TX1-
29 PCIE_TX1+
C777 0.1U/10V PCIE_TXN1_C
C778 0.1U/10V PCIE_TXP1_C

29 PCIE_TX2-
29 PCIE_TX2+
C776 0.1U/10V PCIE_TXN2_C
C775 0.1U/10V PCIE_TXP2_C

28 PCIE_TX4-
28 PCIE_TX4+
C773 0.1U/10V PCIE_TXN4_C
C774 0.1U/10V PCIE_TXP4_C

40 PCIE_TX6-/GLAN_TX-
40 PCIE_TX6+/GLAN_TX+
C779 0.1U/10V GLAN_TXN_C
C780 0.1U/10V GLAN_TXP_C

U22D

29 PCIE_RX1-
29 PCIE_RX1+
MiniWWAN
PCIE_TXN1_C
PCIE_TXP1_C
P27 PERN1
P26 PERP1
N29 PETN1
N28 PETP1

29 PCIE_RX2-
29 PCIE_RX2+
MiniWLAN
PCIE_TXN2_C
PCIE_TXP2_C
M27 PERN2
M26 PERP2
L29 PETN2
L28 PETP2

28 PCIE_RX4-
28 PCIE_RX4+
Express Card
PCIE_TXN4_C
PCIE_TXP4_C
K27 PERN3
K26 PERP3
J29 PETN3
J28 PETP3

H27 PERN4
H26 PERP4
G29 PETN4
G28 PETP4

F27 PERN5
F26 PERP5
F29 PETN5
F28 PETP5

PCI-Express Direct Media Interface

DMI0RXN V27
DMI0RXP V26
DMI0TXN U29
DMI0TXP U28
DMI_MTX_IRX_N0 6
DMI_MTX_IRX_P0 6
DMI_MRX_ITX_N0 6
DMI_MRX_ITX_P0 6

DMI1RXN Y27
DMI1RXP Y26
DMI1TXN W29
DMI1TXP W28
DMI_MTX_IRX_N1 6
DMI_MTX_IRX_P1 6
DMI_MRX_ITX_N1 6
DMI_MRX_ITX_P1 6

DMI2RXN AB26
DMI2RXP AB25
DMI2TXN AA29
DMI2TXP AA28
DMI_MTX_IRX_N2 6
DMI_MTX_IRX_P2 6
DMI_MRX_ITX_N2 6
DMI_MRX_ITX_P2 6

DMI3RXN AD27
DMI3RXP AD26
DMI3TXN AC29
DMI3TXP AC28
DMI_MTX_IRX_N3 6
DMI_MTX_IRX_P3 6
DMI_MRX_ITX_N3 6
DMI_MRX_ITX_P3 6

DMI_CLKN T26
DMI_CLKP T25
CLK_PCIE_ICH# 17
CLK_PCIE_ICH 17

DMI_ZCOMP Y23
DMI_IRCOMP Y24
DMI_COMP
R589 24.9/F
+1.5V_PCIE_ICH
Place within 500mils of ICH8

40 PCIE_RX6-/GLAN_RX-
40 PCIE_RX6+/GLAN_RX+
Giga Bit LOM
GLAN_TXN_C
GLAN_TXP_C
D27 PERN6/GLAN_RXN
D26 PERP6/GLAN_RXP
C29 PETN6/GLAN_TXN
C28 PETP6/GLAN_TXP

Layout Note:
Place R288,R324 and R282
within 500 mils from ICH.

31 ICH_EC_SPI_CLK
R581 15
ICH_EC_SPI_CLK_R
ICH_SPI_CS#
ICH_SPI_CS1#_R
C23 SPI_CLK
B23 SPI_CS0#
E22 SPI_CS1#

31 ICH_EC_SPI_DO
31 ICH_EC_SPI_DIN
R582 15
ICH_EC_SPI_DO_R
D23 SPI_MOSI
F21 SPI_MISO

SPI

USB_OC0_1#
USB_OC2_3#
AJ19 OC0#
AG16 OC1#/GPIO40
AG15 OC2#/GPIO41
AE15 OC3#/GPIO42
AE15 OC4#/GPIO43
AG17 OC5#/GPIO29
AD12 OC6#/GPIO30
AJ18 OC7#/GPIO31
AD14 OC8#
AH18 OC9#

USB

G3 USBP0N
G2 USBP0P
H5 USBP1N
H4 USBP1P
H2 USBP2N
H1 USBP2P
J3 USBP3N
J2 USBP3P
K5 USBP4N
K4 USBP4P
K2 USBP5N
K1 USBP5P
L3 USBP6N
L2 USBP6P
M5 USBP7N
M4 USBP7P
M2 USBP8N
M1 USBP8P
N3 USBP9N
N2 USBP9P

ICH_USBP0- 33
ICH_USBP0+ 33
ICH_USBP1- 33
ICH_USBP1+ 33
PAD T140
PAD T141
ICH_USBP3- 33
ICH_USBP3+ 33
ICH_USBP4- 28
ICH_USBP4+ 28
ICH_USBP5- 35
ICH_USBP5+ 35
ICH_USBP6- 28
ICH_USBP6+ 28
ICH_USBP7- 35
ICH_USBP7+ 35
ICH_USBP8- 43
ICH_USBP8+ 43
ICH_USBP9- 29
ICH_USBP9+ 29

Ext Side Top
Ext Side Bottom
Reserved
Power USB 3
Smart Card
Biometric
Express Card
Blue Tooth
Dock
WWAN

F2 USBRBIAS#
F3 USBRBIAS
USBRBIAS
R631 22.6/F
Short F2 and F3 at the package and keep length to less than 500mils. Trace Impedance should be 60ohms +/- 15%.

ICH8M REV 1.0

+3.3V_ALW
R572 15_NC
U21
R570 15
34 SPI_CS0#
ICH_SPI_CS#
SIO_SPI_CS# 31
R302 0
7SH08_NC

33 USB_OC0_1#
33 USB_OC2_3#
OC4# OC5# OC6# OC7# OC8# OC9#

WWAN Noise - ICH improvements 77
OC6# C871 0.1U/10V
OC4# C872 0.1U/10V
OC5# C873 0.1U/10V
OC7# C878 0.1U/10V
OC8# C874 0.1U/10V
USB_OC2_3# C875 0.1U/10V
USB_OC0_1# C877 0.1U/10V
OC9# C876 0.1U/10V

Non-iAMT
+3.3V_SUS
RP50
OC6# OC4# OC5# OC7#
OC8# USB_OC2_3# USB_OC0_1# OC9#
10P8R-10K

ICH_SPI_CS1#_R
PCI_GNT0#
R628 1K
R580 1K_NC

Boot BIOS Strap

		GNT0#	SPI_CS1#
LPC	11	No stuff	No stuff
PCI	10	No stuff	Stuff
SPI	01	Stuff	No stuff

PCI Pullups
RP45 10P8R-8.2K
PCI_STOP# PCI_FRAME# PCI_REQ1#
RP47 10P8R-8.2K
PCI_DEVSEL# PCI_PIRQD#
PCI_SERR# ICH_GPIO2_PIRQE# PCI_TRDY#
RP48 10P8R-8.2K
ICH_GPIO5_PIRQH# PCI_REQ0# PCI_PLOCK# PCI_PERR#
PCI_PIRQC# PCI_PIRQB# PCI_PIRQA# PCI_IRDY#
+3.3V_RUN

SB_WWAN_PCIE_RST# R595 20K
SB_WLAN_PCIE_RST# R596 20K
SB_LOM_PCIE_RST# R615 20K
SB_NB_PCIE_RST# R667 20K
BIOS should not enable the internal GPIO pull up resistor.

27,42 PCI_AD[0..31]

U22B

PCI_AD0 D20 AD0
PCI_AD1 E19 AD1
PCI_AD2 D19 AD2
PCI_AD3 A20 AD3
PCI_AD4 D17 AD4
PCI_AD5 A21 AD5
PCI_AD6 A19 AD6
PCI_AD7 C19 AD7
PCI_AD8 A18 AD8
PCI_AD9 B16 AD9
PCI_AD10 A12 AD10
PCI_AD11 E16 AD11
PCI_AD12 A14 AD12
PCI_AD13 G16 AD13
PCI_AD14 A15 AD14
PCI_AD15 B6 AD15
PCI_AD16 C11 AD16
PCI_AD17 A9 AD17
PCI_AD18 D11 AD18
PCI_AD19 B12 AD19
PCI_AD20 C12 AD20
PCI_AD21 D10 AD21
PCI_AD22 C7 AD22
PCI_AD23 F13 AD23
PCI_AD24 E11 AD24
PCI_AD25 E13 AD25
PCI_AD26 E12 AD26
PCI_AD27 D8 AD27
PCI_AD28 A6 AD28
PCI_AD29 E8 AD29
PCI_AD30 D6 AD30
PCI_AD31 A3 AD31

PCI

REQ0# A4 PCI_REQ0#
GNT0# D7 PCI_GNT0#
REQ1#/GPIO50 E18 PCI_REQ1#
GNT1#/GPIO51 C18 PCI_GNT1#
REQ2#/GPIO52 B19 SB_WWAN_PCIE_RST#
GNT2#/GPIO53 F18 PCI_GNT2#
REQ3#/GPIO54 A11 SB_LOM_PCIE_RST#
GNT3#/GPIO55 C10 PCI_GNT3#

PCI_REQ0# 43
PCI_GNT0# 42
PCI_REQ1# 27
PCI_GNT1# 27
SB_WWAN_PCIE_RST# 29
PAD T155
SB_LOM_PCIE_RST# 40
PAD T156
39

C/BE0# C17 PCI_C_BE0# 27,42
C/BE1# E15 PCI_C_BE1# 27,42
C/BE2# E16 PCI_C_BE2# 27,42
C/BE3# E17 PCI_C_BE3# 27,42

IRDY# C8 PCI_IRDY# 27,42
PAR D9 PCI_PAR 27,42

PCIRST# G6 PCI_RST# G
DEVSEL# D16 PCI_DEVSEL# 27,42
PERR# A7 PCI_PERR# 27,42
PLOCK# B7 PCI_PLOCK# 42
SERR# F10 PCI_SERR# 27,42
STOP# C16 PCI_STOP# 27,42
TRDY# C9 PCI_TRDY# 27,42
FRAME# A17 PCI_FRAME# 27,42

PLTRST# AG24 PCI_PLTRST#
PCICLK B10 CLK_PCI_ICH
PME# G7
CLK_PCI_ICH 17
ICH_PME# 32

Interrupt I/F

42 PCI_PIRQA#
T131 PAD
T133 PAD
27 PCI_PIRQD#
PCI_PIRQA# F9 PIRQA#
PCI_PIRQB# B5 PIRQB#
PCI_PIRQC# C5 PIRQC#
PCI_PIRQD# A10 PIRQD#

PIRQE#/GPIO2 F8 ICH_GPIO2_PIRQE#
PIRQF#/GPIO3 G11 SB_WLAN_PCIE_RST#
PIRQG#/GPIO4 F12 SB_NB_PCIE_RST#
PIRQH#/GPIO5 B3 ICH_GPIO5_PIRQH#

SB_WLAN_PCIE_RST# 29
SB_NB_PCIE_RST# 6
39

ICH8M REV 1.0

39 PCI_GNT3#
R614 1K_NC

A16 away override strap.

SB_NB_PCIE_RST#	Low = A16 swap override enabled. High = Default.

DOCK	REQ0	GNT0	PIRQA
Cardbus or Cardbus/1394	REQ1	GNT1	PIRQD
1394/MediaCard	REQ2	GNT2	PIRQC PIRQD

CLK_PCI_ICH
R306 10_NC
C337 8.2P/16V_NC
Reserved for EMI.Place resister and cap close to ICH.

Non-iAMT
+3.3V_SUS
C843 0.047U/10V
U48 7SH32
PCI_RST# G
PCI_RST# 27,28,42
C769 0.047U/10V
U45 7SH32
PCI_PLTRST#
PLTRST# 6,28,29,31,32,40
Add Buffers as needed for Loading and fanout concerns.

QUANTA COMPUTER

Title	ICH8-M (USB,DMI,PCIE,PCI)		
Size	Document Number JM7B		Rev 2A
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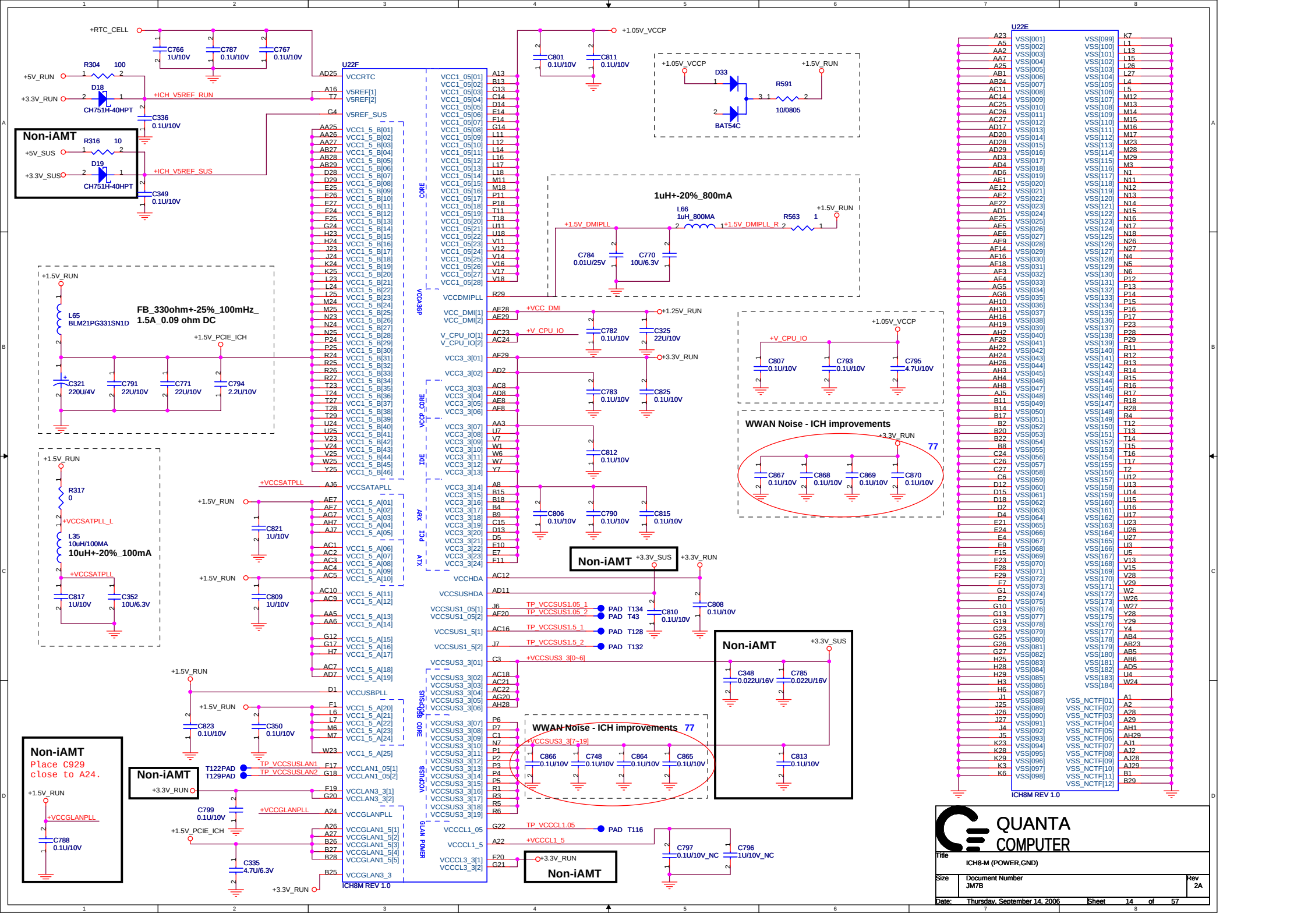
U22F
ICH8M REV 1.0
U22E
ICH8M REV 1.0
Non-iAMT
Non-iAMT
Place C929
close to A24.
Non-iAMT
Non-iAMT
Non-iAMT
Non-iAMT
WWAN Noise - ICH improvements
77
WWAN Noise - ICH improvements
77
1uH+-20%_800mA
FB_330ohm+-25%_100mHz_
1.5A_0.09 ohm DC
10uH+-20%_100mA
QUANTA
COMPUTER
Title
ICH8-M (POWER,GND)
Size
Document Number
JM7B
Rev
2A
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14
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57

A is required to route to Top SoDIMM for AMTto function. Ch.A SODIMM needs to be populated for Intel AMT support.

TOP

JDIM1

PC4800 DDR2 SDRAM SO-DIMM (200P)

TYC_1775804-2

BOT

JDIM2

PC4800 DDR2 SDRAM SO-DIMM (200P)

FOX_AS0A426-M2SN-7F

Non-iAMT

SMbus address A0

CLOCK 0,1
CKE 0,1

SMbus address A4

CLOCK 2,3
CKE 2,3

Place these Caps near So-Dimm1.

Place these Caps near So-Dimm2.

Place these Caps near So-Dimm1.

Place these Caps near So-Dimm2.

QUANTA COMPUTER

Title	DDR2 SO-DIMM (200P) X 2	
Size	Document Number JM7B	Rev 2A
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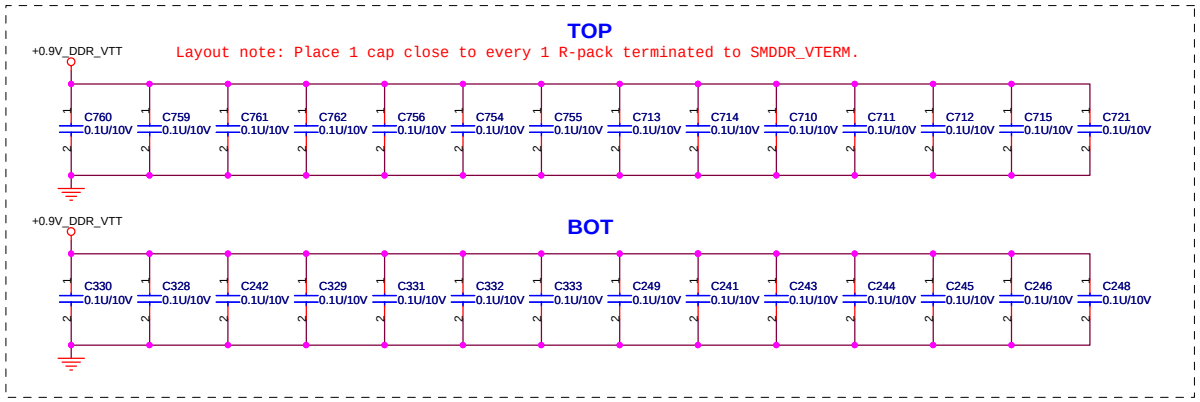

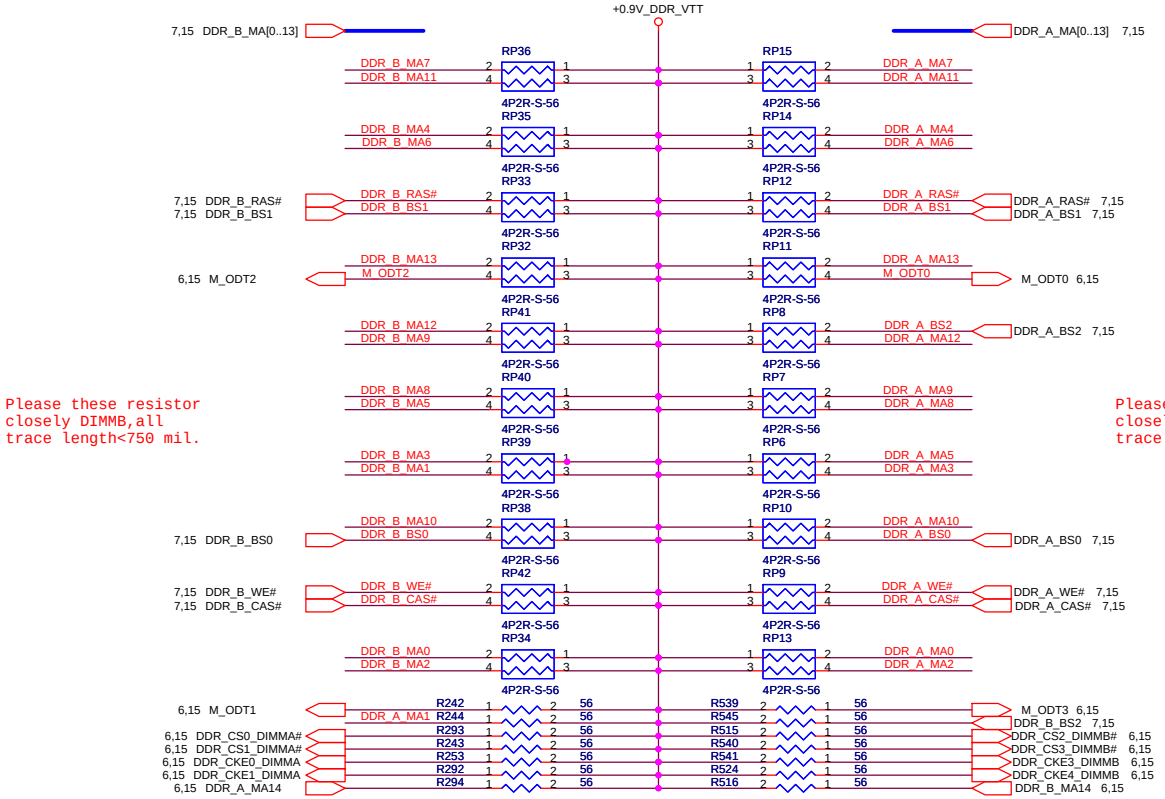

Please these resistor closely DIMMB,all trace length<750 mil.

Please these resistor closely DIMMA,all trace length<750 mil.

QUANTA COMPUTER

Title	DDR2 RES ARRAY	
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Non-iAMT

+3.3V_RUN

R493 10K_NC — FSA

R489 10K_NC

Non-iAMT

+3.3V_RUN

R192 10K — PCI_LOM

R191 10K_NC

0=UMA
1 = Disc. GRFX down

Add capacitor pads for improving WWAN.

C223	27P/50V_NC	CLK_SMCARD_48M
C221	27P/50V_NC	CLK_ICH_48M
C199	27P/50V_NC	CLK_SIO_14M
C197	27P/50V_NC	CLK_ICH_14M
C198	27P/50V_NC	CLK_PCI_5018
C737	27P/50V_NC	CLK_PCI_5025
C211	27P/50V_NC	CLK_PCI_PCCARD
C670	27P/50V_NC	CLK_PCI_DOCK
C212	27P/50V_NC	CLK_PCI_TPM
C215	27P/50V_NC	CLK_PCI_ICH

Y4

CLK_XTAL_IN — 14.318MHZ — CLK_XTAL_OUT

C681 27P/50V

C680 27P/50V

14.318MHz

+3.3V_RUN

CLK_3GPLLREQ#	R183	10K
SATA_CLKREQ#	R189	10K
LOM_CLKREQ#	R231	10K
CARD_CLK_REQ#	R188	10K
MINI1CLK_REQ#	R230	10K
MINI2CLK_REQ#	R233	10K

PGMODE R501 10K_NC

Populate for Napa platforms only.

Non-iAMT

+3.3V_RUN

R479 10K — PCI_PCCARD

Non-iAMT

+3.3V_RUN

Enable ITP

10K R483 — PCI_ICH

Change R764 to 147 ohm TBD and pop R763 84.5 ohm TBD pull down on R764 pin2. CLK_VGA_27M_NSS is max 1.2V.

U41

CK505

CY28547LFXC

1	VDD_SRC_01		
49	VDD_SRC_02		
54	VDD_SRC_03		
65	VDD_SRC_04		
30	VDD_PCI_01	+CK_VDD_MAIN2	
36	VDD_PCI_02		
12	VDD_CPU	+CK_VDD_MAIN	
40	VDD_48	+CK_VDD_48	
18	VDD_REF	+CK_VDD_REF	
20	XIN	CLK_XTAL_IN	
19	XOUT	CLK_XTAL_OUT	
41	48M/FSA	FSA	
45	FSB/TEST_MODE	FSB	
23	REF0/FSC_TEST_SEL	FSC	
22	REF1	CLKREF	
27	PCI1	PCI_SIO	
32	PCI2/TME	PCI_PCCARD	
33	PCI3	PCI_DOCK	
34	PCI4/FCTSEL1	PCI_LOM	
43	DOT96T/27M_NSS	27M_NSS	
44	DOT96C/27M_SS	27M_SS	
37	PCIF0/ITP_SEL	PCI_ICH	
39	VTT_PWRDG#/PD(CKPWRGD/PD#)		
16	SCLK	CLK_SCLK	
17	SDATA	CLK_SDATA	
15	VSS_01		
31	VSS_02		
35	VSS_03		
21	VSS_04		
4	VSS_05		
42	VSS_06		
68	VSS_07		
7	VDDA	+CK_VDD_A	
8	VSSA		
25	PCI_STP#	H_STP_PCI# 13	
24	CPU_STP#	H_STP_CPU# 13	
11	CPUT1_MCH	MCH_BCLK	RP22
10	CPUC1_MCH	MCH_BCLK#	RP22
14	CPUT0	CPU_BCLK	RP20
13	CPUC0	CPU_BCLK#	RP20
6	CPUT2_ITP/SRCT_10	CPU_ITP	RP23
5	CPUC2_ITP/SRCC_10	CPU_ITP#	RP23
9	PGMODE	PGMODE R495 10K_NC	+3.3V_RUN
3	SRCT_9	PCIE_MINI1	RP25
2	SRCC_9	PCIE_MINI1#	RP25
72	CLKREQ9#		MINI1CLK_REQ#
70	SRCT_8	PCIE_MINI2	RP31
69	SRCC_8	PCIE_MINI2#	RP31
71	CLKREQ8#		MINI2CLK_REQ#
66	SRCT_7	PCIE_ICH	RP27
67	SRCC_7	PCIE_ICH#	RP27
38	CLKREQ7#		
63	SRCT_6	PCIE_VGA	RP28
64	SRCC_6	PCIE_VGA#	RP28
62	CLKREQ6#		
60	SRCT_5	PCIE_EXPCARD	RP29
61	SRCC_5	PCIE_EXPCARD#	RP29
29	CLKREQ5#		CARD_CLK_REQ#
58	SRCT_4	PCIE_LOM	RP30
59	SRCC_4	PCIE_LOM#	RP30
57	CLKREQ4#		LOM_CLKREQ#
55	SRCT_3	MCH_3GPLL	RP26
56	SRCC_3	MCH_3GPLL#	RP26
28	CLKREQ3#	R190 475/F	CLK_3GPLLREQ#
52	SRCT_2		
53	SRCC_2		
26	CLKREQ2#		
50	SRCT_1/SATAT	PCIE_SATA	RP24
51	SRCC_1/SATAC	PCIE_SATA#	RP24
46	CLKREQ1#		SATA_CLKREQ#
47	SRCT_0/LCD100MT		
48	SRCC_0/LCD100MC		

28	CLK_SMCARD_48M	CLK_SMCARD_48M	R490 15
13	CLK_ICH_48M	CLK_ICH_48M	R491 15
3,6	CPU_MCH_BSEL0		
3,6	CPU_MCH_BSEL1		R477 8.2K
3,6	CPU_MCH_BSEL2		
32	CLK_SIO_14M	CLK_SIO_14M	R476 15
13	CLK_ICH_14M	CLK_ICH_14M	R186 15
32	CLK_PCI_5018	CLK_PCI_5018	R187 15
31	CLK_PCI_5025	CLK_PCI_5025	R478 15
27	CLK_PCI_PCCARD	CLK_PCI_PCCARD	R480 33
43	CLK_PCI_DOCK	CLK_PCI_DOCK	R481 33
40	CLK_PCI_TPM	CLK_PCI_TPM	R193 33
20	CLK_VGA_27M_NSS	R497 84.5/F	R496 147/F
20	CLK_VGA_27M_SS		R500 33
12	CLK_PCI_ICH	CLK_PCI_ICH	R486 33
13	CLK_PWRGD		

76 L70 BLM18AG601SN1D R492 8.2K

Non-iAMT

Discrete

Broadcom

Discrete without iAMT

+3.3V_RUN

L62 BLM21PG600SN1D 120 ohms@100Mhz

+CK_VDD_MAIN

C707 0.1U/10V — C704 0.1U/10V — C697 0.1U/10V — C705 0.1U/10V — C228 0.1U/10V — C706 10U/6.3V

R211 2.2 — +CK_VDD_A

C699 0.047U/10V — C225 4.7U/6.3V

L58 BLM21PG600SN1D 120 ohms@100Mhz

+CK_VDD_MAIN2

C678 0.1U/10V — C683 0.1U/10V — C677 10U/6.3V

R484 2.2 — +CK_VDD_48

C692 0.047U/10V — C693 4.7U/6.3V

R485 1 — +CK_VDD_REF

C687 0.047U/10V

SMbus address D2

These are for backdrive issue.

Non-iAMT

+3.3V_ALW — +3.3V_RUN

R185 2.2K — RP19 4P2R-2.2K

31 CKG_SMBDAT — Q25 2N7002W-7-F — CLK_SDATA

R184 0_NC

+3.3V_ALW — +3.3V_RUN

R195 2.2K

31 CKG_SMBCLK — Q27 2N7002W-7-F — CLK_SCLK

R204 0_NC

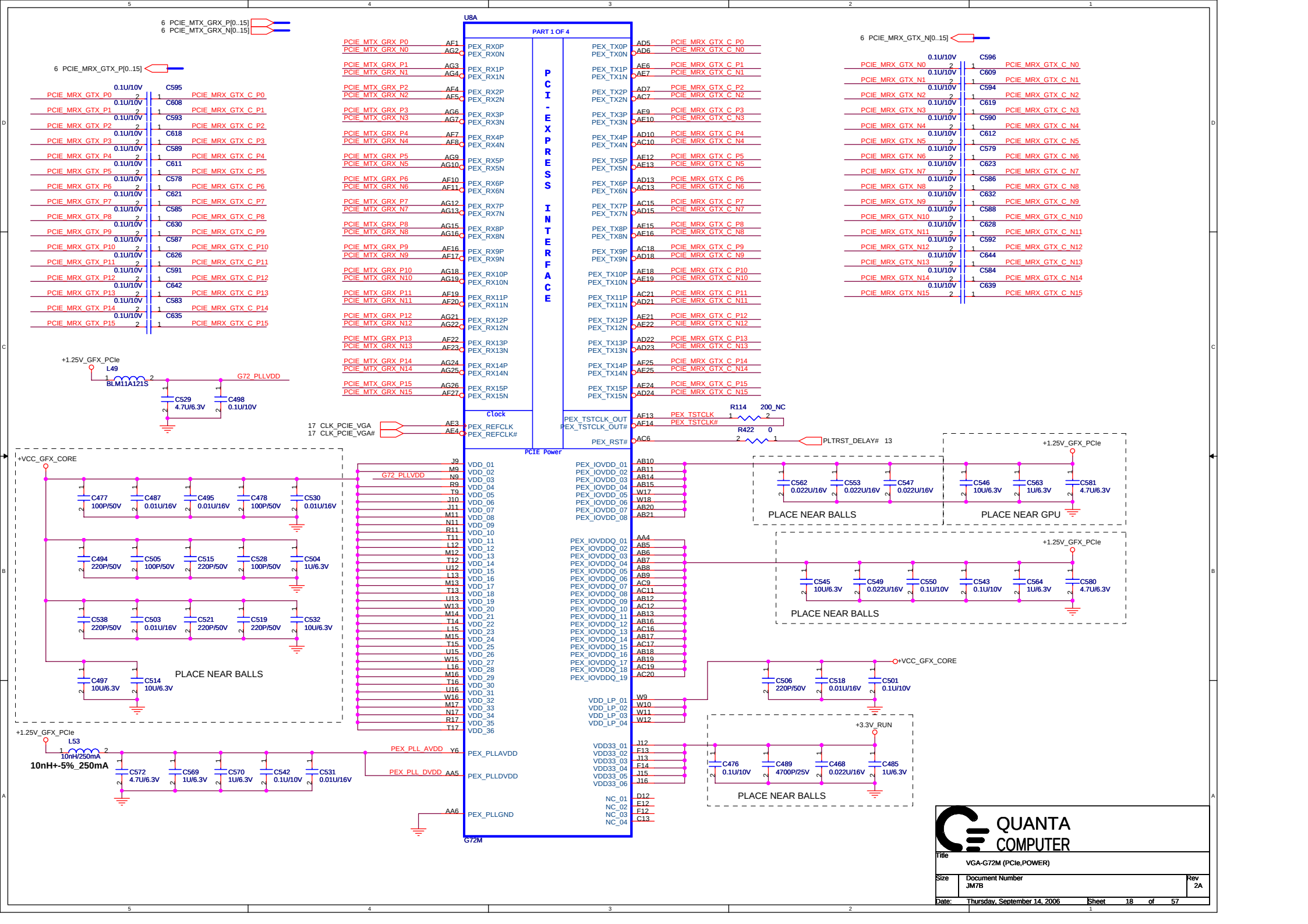
FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

PCI_LOM = FCTSEL1

FCTSEL1 (PIN34)	PIN43	PIN44	PIN47	PIN48
0=UMA	DOT96T	DOT96C	96/ 100M_T	96/ 100M_C
1 = Disc. GRFX down	27Mout	27MSSout	SRCT0	SRCC0

QUANTA COMPUTER

Title	CLOCK GENERATOR	
Size	Document Number JM7B	Rev 2A
Date: Thursday, September 14, 2006	Sheet 17 of 57	


6 PCIE_MTX_GRX_P[0..15]
6 PCIE_MTX_GRX_N[0..15]
6 PCIE_MRX_GTX_P[0..15]
6 PCIE_MRX_GTX_N[0..15]
U8A
PART 1 OF 4
PCI-EXPRESS INTERFACE
PEX_RX0P
PEX_RX0N
PEX_RX1P
PEX_RX1N
PEX_RX2P
PEX_RX2N
PEX_RX3P
PEX_RX3N
PEX_RX4P
PEX_RX4N
PEX_RX5P
PEX_RX5N
PEX_RX6P
PEX_RX6N
PEX_RX7P
PEX_RX7N
PEX_RX8P
PEX_RX8N
PEX_RX9P
PEX_RX9N
PEX_RX10P
PEX_RX10N
PEX_RX11P
PEX_RX11N
PEX_RX12P
PEX_RX12N
PEX_RX13P
PEX_RX13N
PEX_RX14P
PEX_RX14N
PEX_RX15P
PEX_RX15N
PEX_TX0P
PEX_TX0N
PEX_TX1P
PEX_TX1N
PEX_TX2P
PEX_TX2N
PEX_TX3P
PEX_TX3N
PEX_TX4P
PEX_TX4N
PEX_TX5P
PEX_TX5N
PEX_TX6P
PEX_TX6N
PEX_TX7P
PEX_TX7N
PEX_TX8P
PEX_TX8N
PEX_TX9P
PEX_TX9N
PEX_TX10P
PEX_TX10N
PEX_TX11P
PEX_TX11N
PEX_TX12P
PEX_TX12N
PEX_TX13P
PEX_TX13N
PEX_TX14P
PEX_TX14N
PEX_TX15P
PEX_TX15N
Clock
PEX_REFCLK
PEX_REFCLK#
PEX_TSTCLK_OUT
PEX_TSTCLK_OUT#
PEX_RST#
PEX_TSTCLK
PEX_TSTCLK#
PCIE Power
17 CLK_PCIE_VGA
17 CLK_PCIE_VGA#
R114 200_NC
R422 0
PLTRST_DELAY# 13
+1.25V_GFX_PCIe
L49
BLM11A121S
G72_PLLVDD
C529 4.7U/6.3V
C498 0.1U/10V
+VCC_GFX_CORE
C477 100P/50V
C487 0.01U/16V
C495 0.01U/16V
C478 100P/50V
C530 0.01U/16V
C494 220P/50V
C505 100P/50V
C515 220P/50V
C528 100P/50V
C504 1U/6.3V
C538 220P/50V
C503 0.01U/16V
C521 220P/50V
C519 220P/50V
C532 10U/6.3V
C497 10U/6.3V
C514 10U/6.3V
PLACE NEAR BALLS
VDD_01
VDD_02
VDD_03
VDD_04
VDD_05
VDD_06
VDD_07
VDD_08
VDD_09
VDD_10
VDD_11
VDD_12
VDD_13
VDD_14
VDD_15
VDD_16
VDD_17
VDD_18
VDD_19
VDD_20
VDD_21
VDD_22
VDD_23
VDD_24
VDD_25
VDD_26
VDD_27
VDD_28
VDD_29
VDD_30
VDD_31
VDD_32
VDD_33
VDD_34
VDD_35
VDD_36
PEX_IOVDD_01
PEX_IOVDD_02
PEX_IOVDD_03
PEX_IOVDD_04
PEX_IOVDD_05
PEX_IOVDD_06
PEX_IOVDD_07
PEX_IOVDD_08
C562 0.022U/16V
C553 0.022U/16V
C547 0.022U/16V
PLACE NEAR BALLS
C546 10U/6.3V
C563 1U/6.3V
C581 4.7U/6.3V
PLACE NEAR GPU
PEX_IOVDDQ_01
PEX_IOVDDQ_02
PEX_IOVDDQ_03
PEX_IOVDDQ_04
PEX_IOVDDQ_05
PEX_IOVDDQ_06
PEX_IOVDDQ_07
PEX_IOVDDQ_08
PEX_IOVDDQ_09
PEX_IOVDDQ_10
PEX_IOVDDQ_11
PEX_IOVDDQ_12
PEX_IOVDDQ_13
PEX_IOVDDQ_14
PEX_IOVDDQ_15
PEX_IOVDDQ_16
PEX_IOVDDQ_17
PEX_IOVDDQ_18
PEX_IOVDDQ_19
C545 10U/6.3V
C549 0.022U/16V
C550 0.1U/10V
C543 0.1U/10V
C564 1U/6.3V
C580 4.7U/6.3V
PLACE NEAR BALLS
VDD_LP_01
VDD_LP_02
VDD_LP_03
VDD_LP_04
C506 220P/50V
C518 0.01U/16V
C501 0.1U/10V
+3.3V_RUN
C476 0.1U/10V
C489 4700P/25V
C468 0.022U/16V
C485 1U/6.3V
PLACE NEAR BALLS
VDD33_01
VDD33_02
VDD33_03
VDD33_04
VDD33_05
VDD33_06
NC_01
NC_02
NC_03
NC_04
+1.25V_GFX_PCIe
L53
10nH/250mA
10nH+-5%_250mA
PEX_PLL_AVDD
PEX_PLL_DVDD
PEX_PLLAVDD
PEX_PLLDVDD
PEX_PLLGND
C572 4.7U/6.3V
C569 1U/6.3V
C570 1U/6.3V
C542 0.1U/10V
C531 0.01U/16V
G72M
C595
C608
C593
C618
C589
C611
C578
C621
C585
C630
C587
C626
C591
C642
C583
C635
C596
C609
C594
C619
C590
C612
C579
C623
C586
C632
C588
C628
C592
C644
C584
C639
QUANTA COMPUTER
Title
VGA-G72M (PCIe,POWER)
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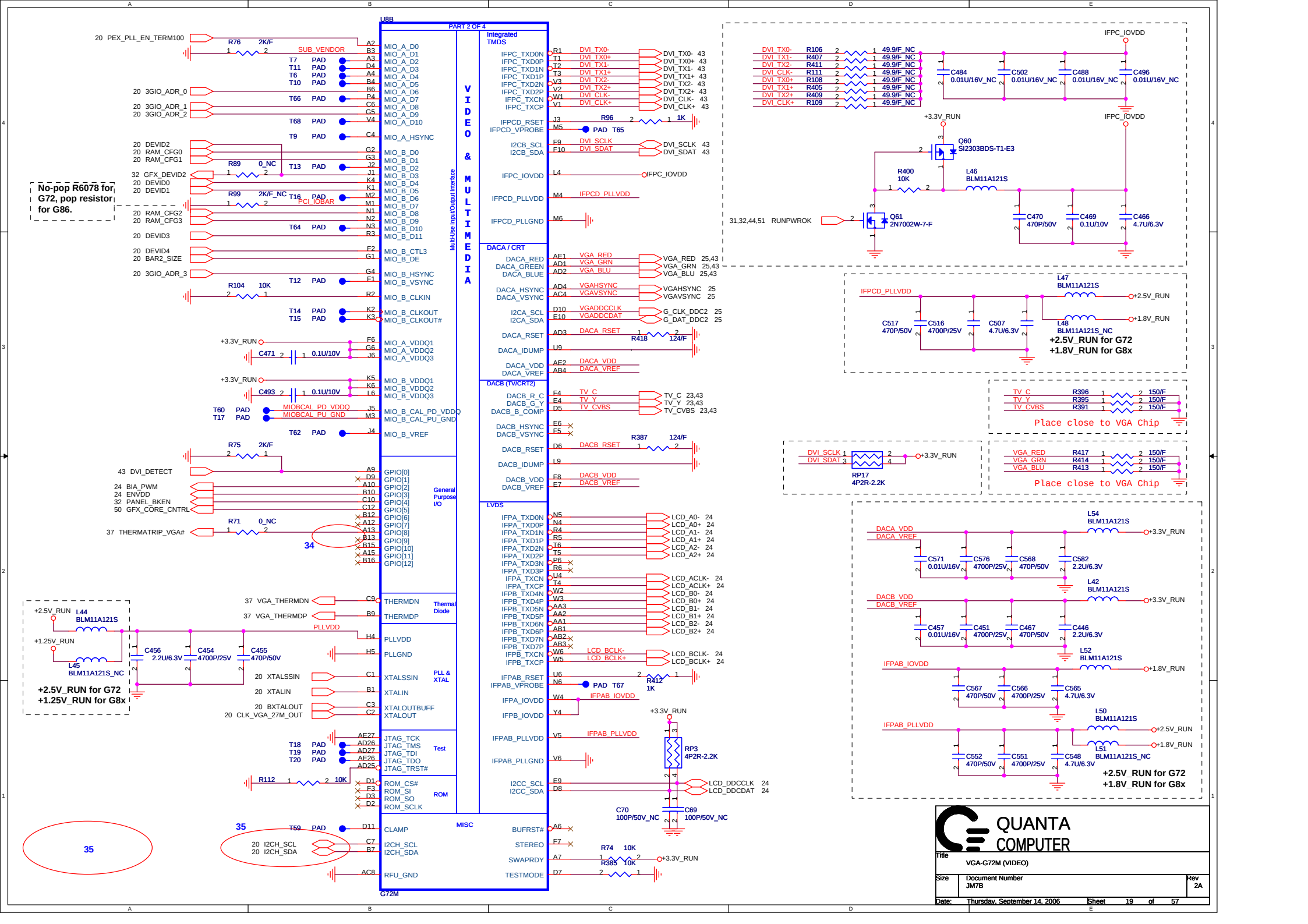
U8B
PART 2 OF 4
VIDEO & MULTIMEDIA
Multi-User Input/Output Interface
Integrated TMDS
DACA / CRT
DACB (TV/CRT2)
LVDS
General Purpose I/O
Thermal Diode
PLL & XTAL
Test
ROM
MISC
G72M
No-pop R6078 for G72, pop resistor for G86.
+2.5V_RUN for G72
+1.25V_RUN for G8x
+2.5V_RUN for G72
+1.8V_RUN for G8x
Place close to VGA Chip
Place close to VGA Chip
+2.5V_RUN for G72
+1.8V_RUN for G8x
QUANTA COMPUTER
VGA-G72M (VIDEO)
JM7B
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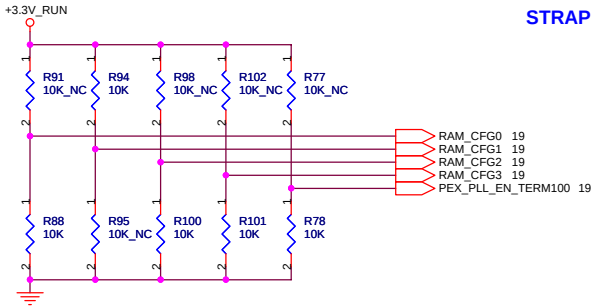
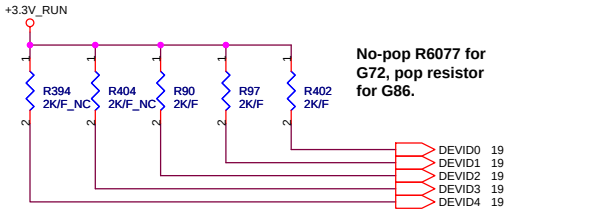
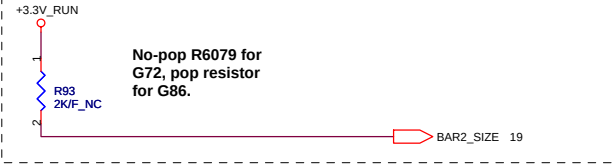
STRAP



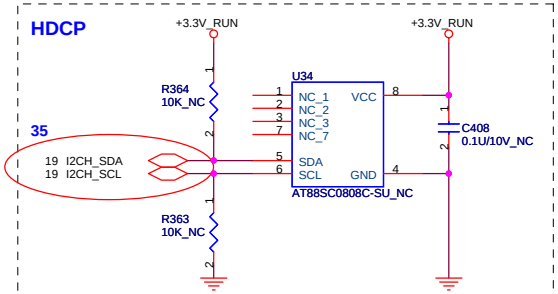


Infineon/Hynix	CFG3	CFG2	CFG1	CFG0
128MB(16M*16)	0	0	1	0
256MB(32M*16)	0	1	1	0
	DEV3	DEV2	DEV1	DEV0
(256MB)G72GLM	1	X	0	0
(128MB)G72MV	0	1	1	1

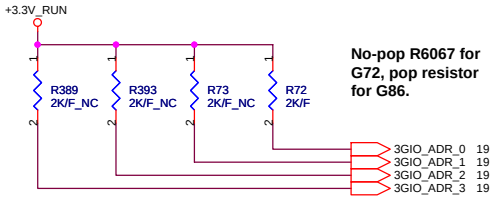
Note: 256MB: Pop R606; depop R6001.
128MB: Pop R6001; depop R606.



HDCP

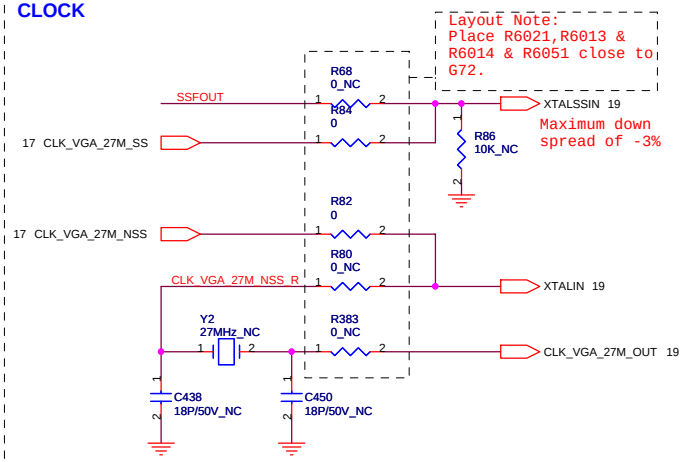


STRAP

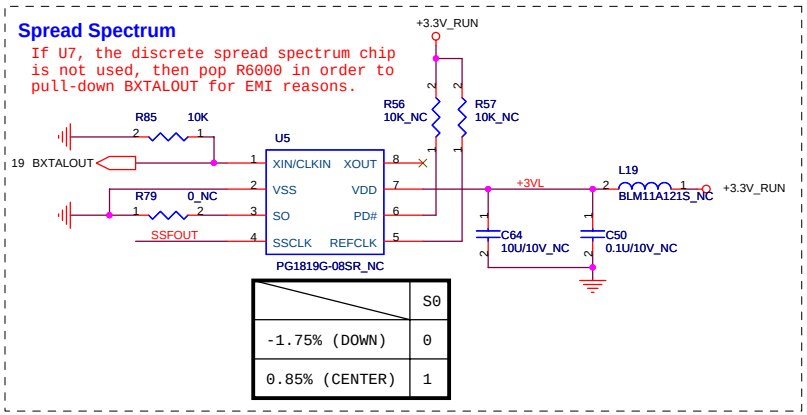


3GIO_ADR_X	ADR3	ADR2	ADR1	ADR0
Desktop	0	0	0	0
Mobile	0	0	0	1

CLOCK



Spread Spectrum



	S0
-1.75% (DOWN)	0
0.85% (CENTER)	1

QUANTA COMPUTER

Title	VGA-G72M (STRAP,CLOCK,HDCP)	
Size	Document Number JM7B	Rev 2A
Date: Thursday, September 14, 2006	Sheet 20 of 57	

FB_CMD[0..26] 22
FBD[0..63] 22
FBDQM[0..7] 22
FBDQS[0..7] 22
FBDQS#[0..7] 22

U8C

Part 3 of 4

MEMORY INTERFACE

FBD0	A26	FB_DQ0	FB_CMD0	G27	FB_CMD0
FBD1	C24	FB_DQ1	FB_CMD1	D25	FB_CMD1
FBD2	B24	FB_DQ2	FB_CMD2	F26	FB_CMD2
FBD3	A24	FB_DQ3	FB_CMD3	E25	FB_CMD3
FBD4	C22	FB_DQ4	FB_CMD4	G25	FB_CMD4
FBD5	A25	FB_DQ5	FB_CMD5	J25	FB_CMD5
FBD6	B25	FB_DQ6	FB_CMD6	J27	FB_CMD6
FBD7	D23	FB_DQ7	FB_CMD7	M26	FB_CMD7
FBD8	G22	FB_DQ8	FB_CMD8	C27	FB_CMD8
FBD9	J23	FB_DQ9	FB_CMD9	C25	FB_CMD9
FBD10	E24	FB_DQ10	FB_CMD10	D24	FB_CMD10
FBD11	F23	FB_DQ11	FB_CMD11	N27	FB_CMD11
FBD12	J24	FB_DQ12	FB_CMD12	G24	FB_CMD12
FBD13	F24	FB_DQ13	FB_CMD13	J26	FB_CMD13
FBD14	G23	FB_DQ14	FB_CMD14	M27	FB_CMD14
FBD15	H24	FB_DQ15	FB_CMD15	C26	FB_CMD15
FBD16	D16	FB_DQ16	FB_CMD16	M25	FB_CMD16
FBD17	E16	FB_DQ17	FB_CMD17	D26	FB_CMD17
FBD18	D17	FB_DQ18	FB_CMD18	D27	FB_CMD18
FBD19	F18	FB_DQ19	FB_CMD19	K26	FB_CMD19
FBD20	E19	FB_DQ20	FB_CMD20	K25	FB_CMD20
FBD21	E18	FB_DQ21	FB_CMD21	K24	FB_CMD21
FBD22	D20	FB_DQ22	FB_CMD22	F27	FB_CMD22
FBD23	D19	FB_DQ23	FB_CMD23	K27	FB_CMD23
FBD24	A18	FB_DQ24	FB_CMD24	G26	FB_CMD24
FBD25	B18	FB_DQ25	FB_CMD25	B27	FB_CMD25
FBD26	A19	FB_DQ26	FB_CMD26	N24	FB_CMD26
FBD27	B19	FB_DQ27			
FBD28	D18	FB_DQ28			
FBD29	C19	FB_DQ29			
FBD30	C16	FB_DQ30	FB_DQM0	D21	FBDQM0
FBD31	C18	FB_DQ31	FB_DQM1	F22	FBDQM1
FBD32	N26	FB_DQ32	FB_DQM2	E20	FBDQM2
FBD33	N25	FB_DQ33	FB_DQM3	A21	FBDQM3
FBD34	R25	FB_DQ34	FB_DQM4	V27	FBDQM4
FBD35	R26	FB_DQ35	FB_DQM5	W22	FBDQM5
FBD36	R27	FB_DQ36	FB_DQM6	V22	FBDQM6
FBD37	T25	FB_DQ37	FB_DQM7	V24	FBDQM7
FBD38	T27	FB_DQ38			
FBD39	T26	FB_DQ39	FB_DQS_RN0	A22	FBDQS#0
FBD40	AB23	FB_DQ40	FB_DQS_RN1	E22	FBDQS#1
FBD41	Y24	FB_DQ41	FB_DQS_RN2	F21	FBDQS#2
FBD42	AB24	FB_DQ42	FB_DQS_RN3	B21	FBDQS#3
FBD43	AB22	FB_DQ43	FB_DQS_RN4	V26	FBDQS#4
FBD44	AC24	FB_DQ44	FB_DQS_RN5	W23	FBDQS#5
FBD45	AC22	FB_DQ45	FB_DQS_RN6	V23	FBDQS#6
FBD46	AA23	FB_DQ46	FB_DQS_RN7	W27	FBDQS#7
FBD47	AA22	FB_DQ47			
FBD48	T24	FB_DQ48	FB_DQS_WP0	B22	FBDQS0
FBD49	T23	FB_DQ49	FB_DQS_WP1	D22	FBDQS1
FBD50	R24	FB_DQ50	FB_DQS_WP2	E21	FBDQS2
FBD51	R23	FB_DQ51	FB_DQS_WP3	C21	FBDQS3
FBD52	R22	FB_DQ52	FB_DQS_WP4	V25	FBDQS4
FBD53	T22	FB_DQ53	FB_DQS_WP5	W24	FBDQS5
FBD54	N23	FB_DQ54	FB_DQS_WP6	U24	FBDQS6
FBD55	P24	FB_DQ55	FB_DQS_WP7	W26	FBDQS7
FBD56	AA24	FB_DQ56			
FBD57	AA27	FB_DQ57			
FBD58	AA26	FB_DQ58			
FBD59	AB25	FB_DQ59			
FBD60	AB26	FB_DQ60			
FBD61	AB27	FB_DQ61			
FBD62	AA25	FB_DQ62			
FBD63	W25	FB_DQ63			

read strobe

write strobe

22 FB_CLK0 → L24 FB_CLK0
22 FB_CLK0# → K23 FB_CLK0#

22 FB_CLK1 → M22 FB_CLK1
22 FB_CLK1# → N22 FB_CLK1#

M23 FB_REFCLK
M24 FB_REFCLK#

T63 PAD — FB_DEBUG K22 FB_DEBUG

FBVREF A16 FB_VREF

FBA_PLLVDD D14 FB_PLLVDD

FB_PLLAVDD D13 FB_PLLAVDD

C15 FB_PLLAGND

FBVTT_01	E15	FBVDDQ_01	E17	FBCAL_PD_VDDQ	D15
FBVTT_02	F15	FBVDDQ_02	E19	FBCAL_PU_GND	E13
FBVTT_03	E16	FBVDDQ_03	J19	FBCAL_TERM_GND	H22
FBVTT_04	J17	FBVDDQ_04	M19		
FBVTT_05	J18	FBVDDQ_05	T19		
FBVTT_06	L19	FBVDDQ_06	J22		
FBVTT_07	N19	FBVDDQ_07	L22		
FBVTT_08	R19	FBVDDQ_08	P22		
FBVTT_09	U19	FBVDDQ_09	U22		
FBVTT_10	W19	FBVDDQ_10	Y22		

FBCAL_PD_VDDQ — R399 40.2/F — +1.8V_RUN

FBCAL_PU_GND

FBCAL_TERM_GND — R398 0_NC — R397 30/F

+1.25V_GFX_PCIe — L41 BLM11A121S — C449 4.7U/6.3V — C452 0.1U/10V — C453 1000P/50V

+1.8V_RUN — R69 1K/F — FBVREF — R70 1K/F — C68 0.1U/10V

FBVREF = FBVDDQ * Rb/(Rt + Rb).
VREF = 0.5 * FBVDDQ.
DDR: 0.9V = 1.8V * 1K/(1K + 1K).

For G8x used

+1.25V_GFX_PCIe — L43 BLM11A121S_NC — FBA_PLLVDD — C444 4.7U/6.3V_NC — C447 0.1U/10V_NC

U8C G72M

U8D

Part 4 of 4

GND

B2	GND_01		GND_48	P14	
E2	GND_02		GND_49	R14	
H2	GND_03		GND_50	U14	
L2	GND_04		GND_51	W14	
P2	GND_05		GND_52	AC14	
U2	GND_06		GND_53	AD14	
Y2	GND_07		GND_54	N15	
AC2	GND_08		GND_55	P15	
AE2	GND_09		GND_56	R15	
AF3	GND_10		GND_57	AF15	
B5	GND_11		GND_58	N16	
E5	GND_12		GND_59	P16	
L5	GND_13		GND_60	R16	
P5	GND_14		GND_61	AD16	
U5	GND_15		GND_62	B17	
Y5	GND_16		GND_63	E17	
AC5	GND_17		GND_64	L17	
H6	GND_18		GND_65	P17	
AF6	GND_19		GND_66	U17	
B8	GND_20		GND_67	AD17	
E8	GND_21		GND_68	AF18	
AD8	GND_22		GND_69	K19	
K9	GND_23		GND_70	P19	
P9	GND_24		GND_71	V19	
V9	GND_25		GND_72	AD19	
AD9	GND_26		GND_73	B20	
AF9	GND_27		GND_74	E20	
B11	GND_28		GND_75	AD20	
E11	GND_29		GND_76	AF21	
F11	GND_30		GND_77	B23	
L11	GND_31		GND_78	E23	
P11	GND_32		GND_79	H23	
U11	GND_33		GND_80	L23	
AD11	GND_34		GND_81	P23	
N12	GND_35		GND_82	U23	
P12	GND_36		GND_83	Y23	
R12	GND_37		GND_84	AC23	
AD12	GND_38		GND_85	AF24	
AF12	GND_39		GND_86	B26	
N13	GND_40		GND_87	E26	
P13	GND_41		GND_88	H26	
R13	GND_42		GND_89	L26	
B14	GND_43		GND_90	P26	
E14	GND_44		GND_91	U26	
J14	GND_45		GND_92	Y26	
L14	GND_46		GND_93	AC26	
N14	GND_47		GND_94	AF26	

U8D G72M

PLACE BELOW GPU

+1.8V_RUN

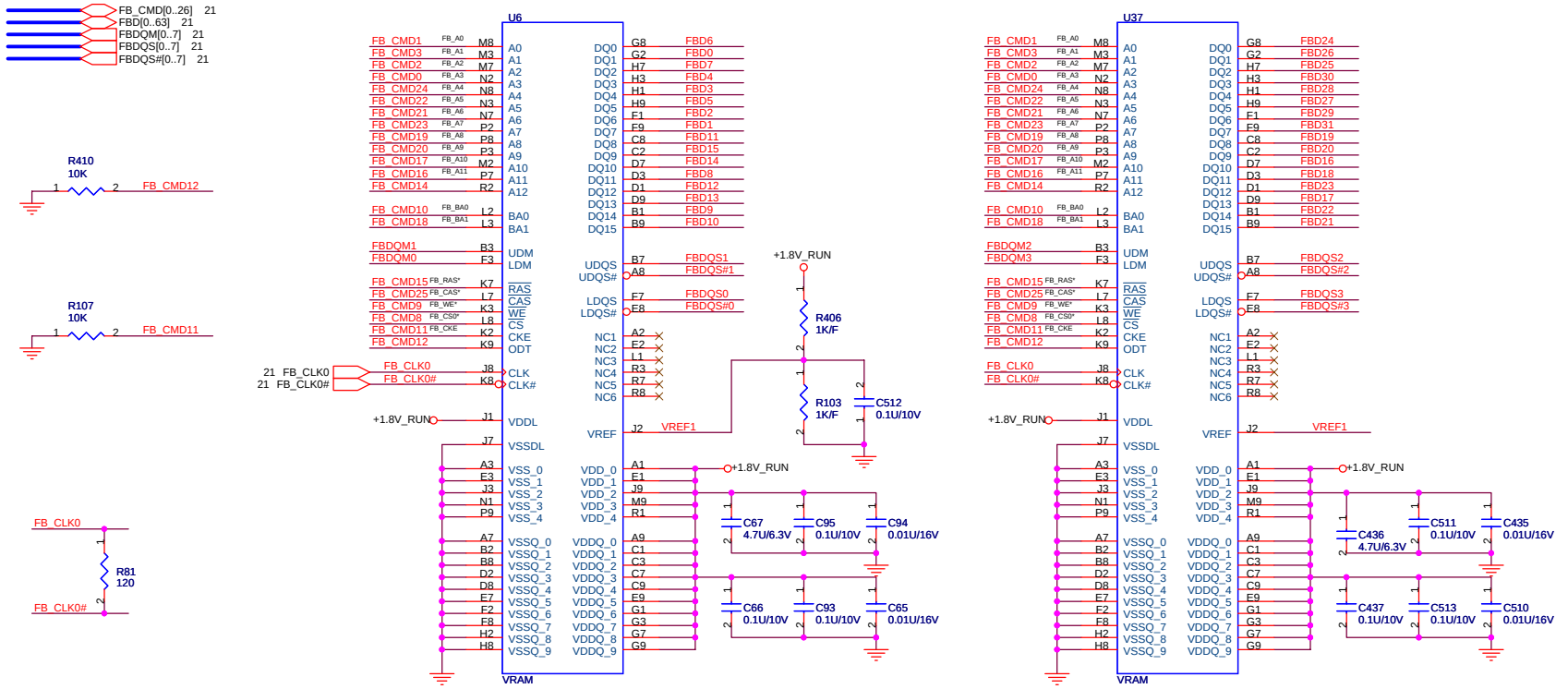
C541 4700P/25V — C540 0.022U/16V — C79 0.1U/10V — C475 4700P/25V — C110 0.1U/10V — C89 4.7U/6.3V — C574 1U/6.3V

C490 4700P/25V — C491 0.022U/16V — C500 0.1U/10V — C499 4700P/25V — C508 0.022U/16V — C509 0.1U/10V — C522 4.7U/6.3V

C486 4700P/25V — C472 0.022U/16V — C473 0.1U/10V — C492 0.022U/16V — C474 0.1U/10V — C539 1U/6.3V

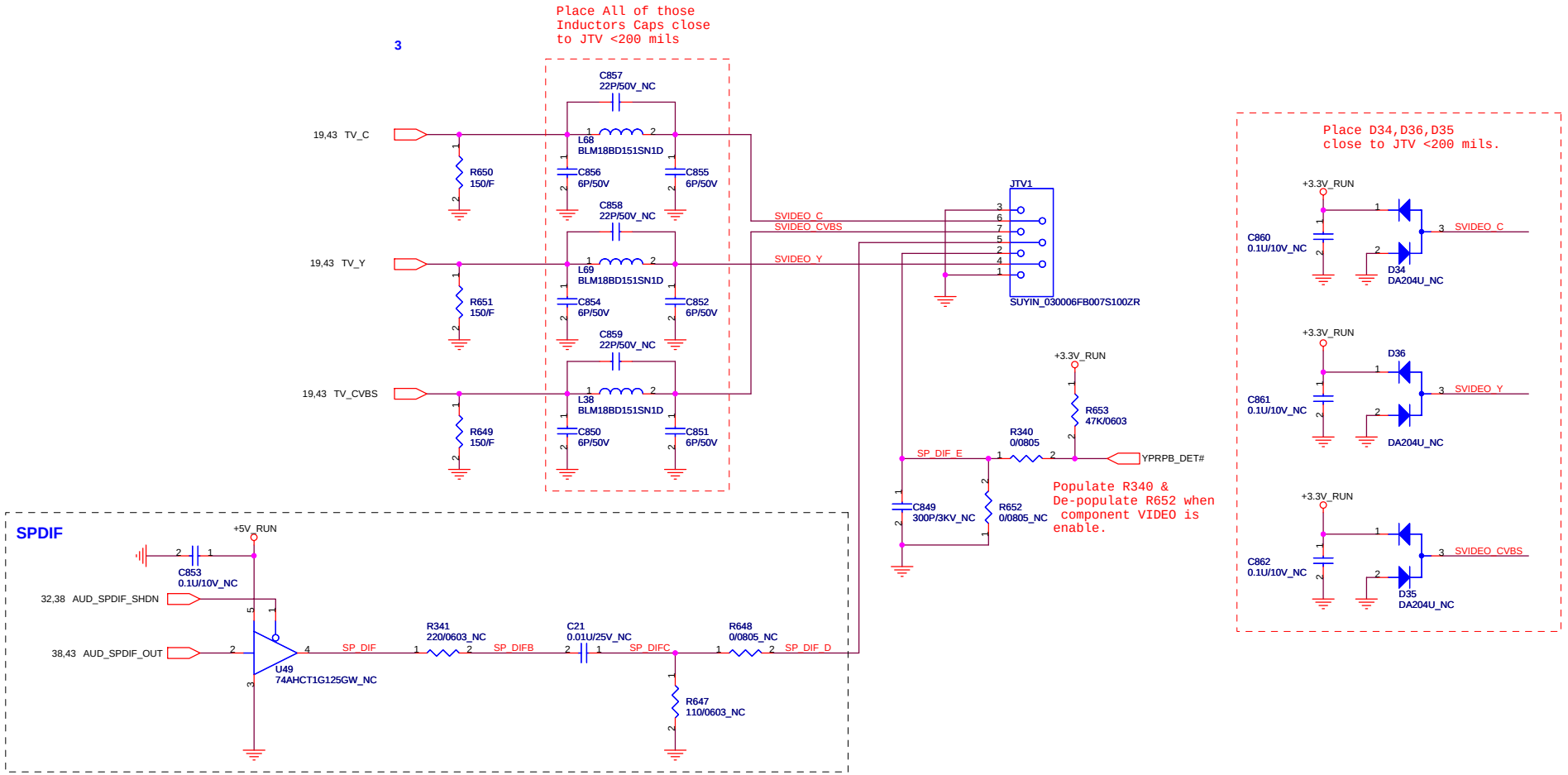
QUANTA COMPUTER

Title	VGA-G72M (MEMORY,GUD)		
Size	Document Number JM7B		Rev 2A
Date:	Thursday, September 14, 2006	Sheet 21 of 57	



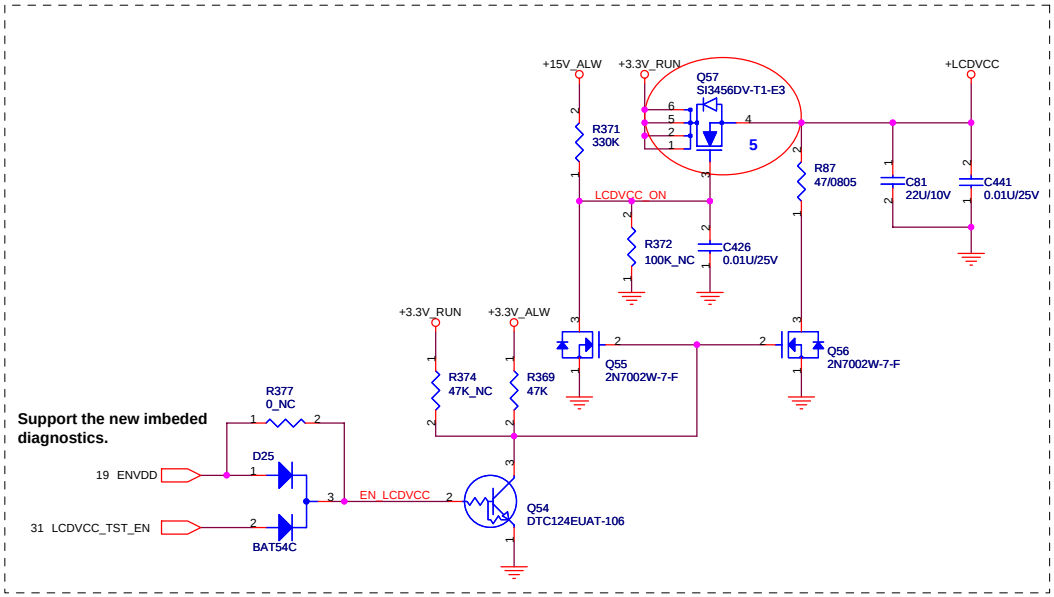
QUANTA COMPUTER

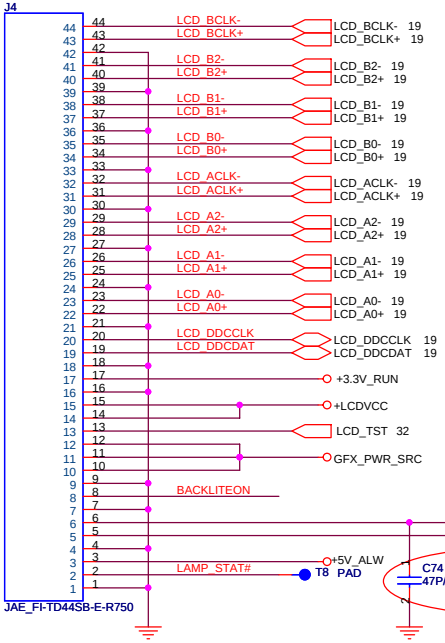
Title	VGA-G72M (VRAM)	
Size	Document Number JM7B	Rev 2A
Date: Thursday, September 14, 2006	Sheet 22 of 57	

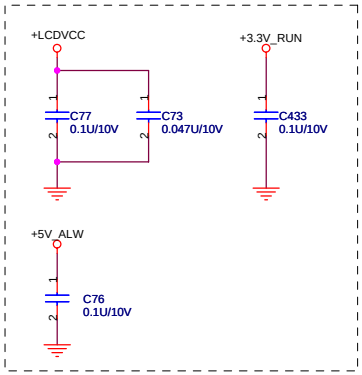


QUANTA COMPUTER

Title	S-Video CONN with SPDIF	
Size	Document Number JM7B	Rev 2A
Date: Thursday, September 14, 2006	Sheet 23 of 57	



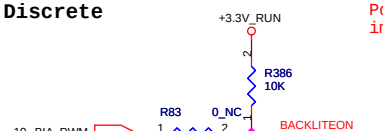




LCD_SMBCLK 31
LCD_SMBDAT 31

Adress : A9H --Contrast
AAH --Backlight

Discrete

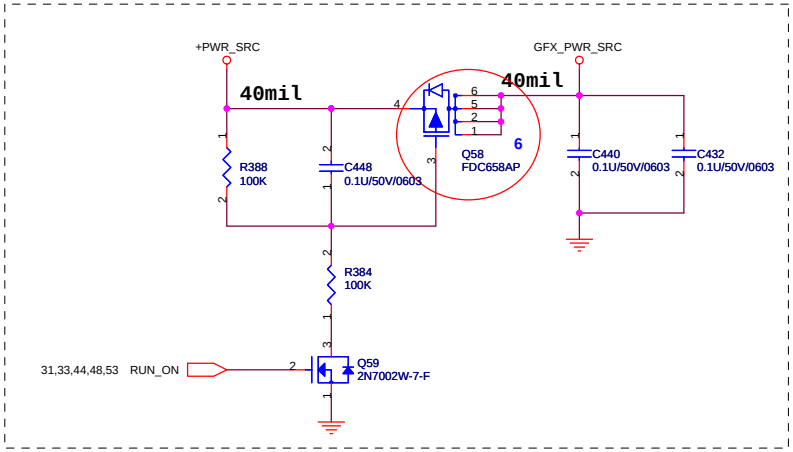


Populate R614 for DPST implementation only.

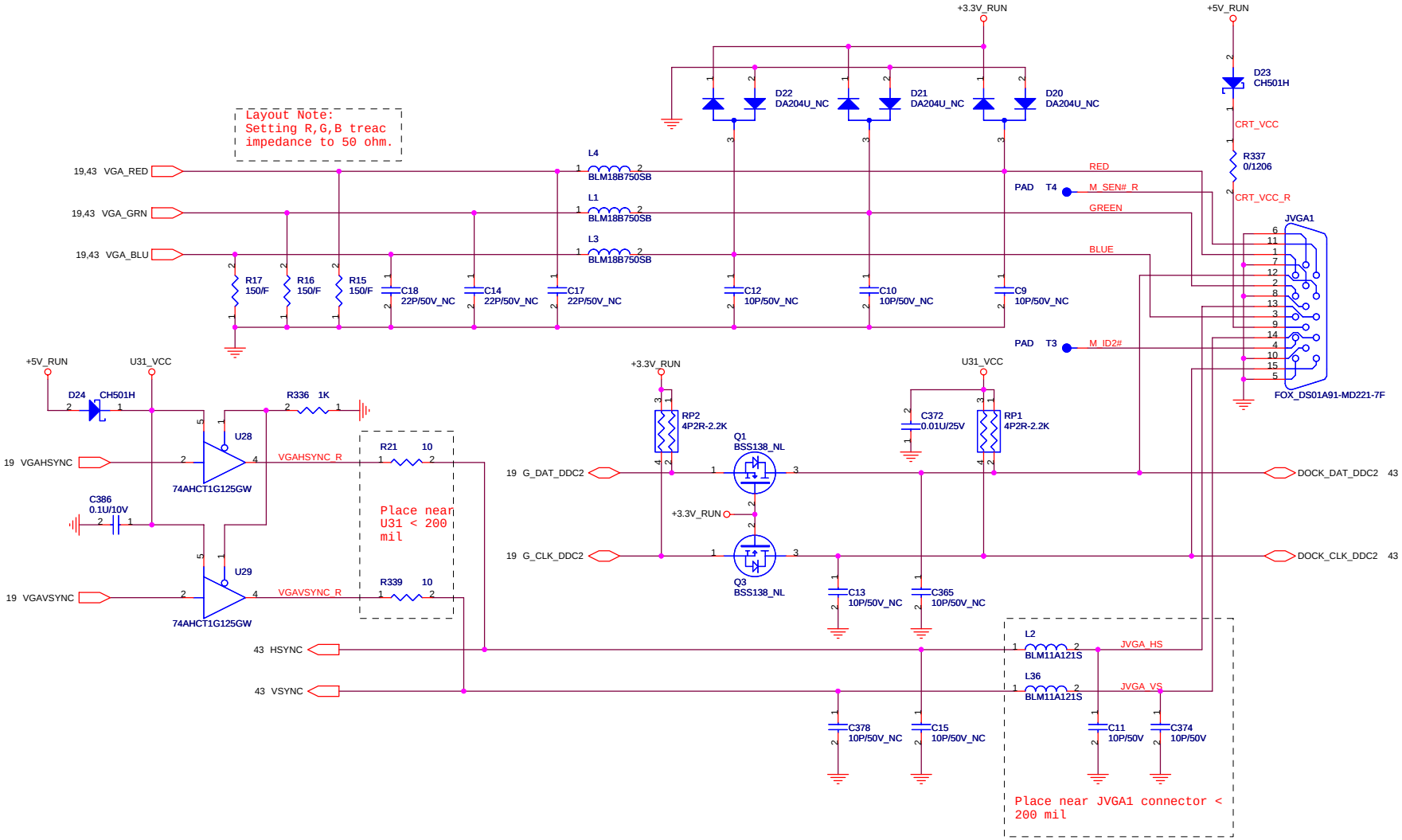
Populate R74 for platform without DPST support. No Stuff for Discrete DSPT support due to back up plan.

Shunt capacitors on LVDS for improving WWAN.

LCD_B0-	C430	2	3.3P/50V_NC	LCD_B0+
LCD_B1-	C434	2	3.3P/50V_NC	LCD_B1+
LCD_B2-	C425	2	3.3P/50V_NC	LCD_B2+
LCD_BCLK-	C63	2	3.3P/50V_NC	LCD_BCLK+
LCD_A0-	C80	2	3.3P/50V_NC	LCD_A0+
LCD_A1-	C71	2	3.3P/50V_NC	LCD_A1+
LCD_A2-	C72	2	3.3P/50V_NC	LCD_A2+
LCD_ACLK-	C57	2	3.3P/50V_NC	LCD_ACLK+



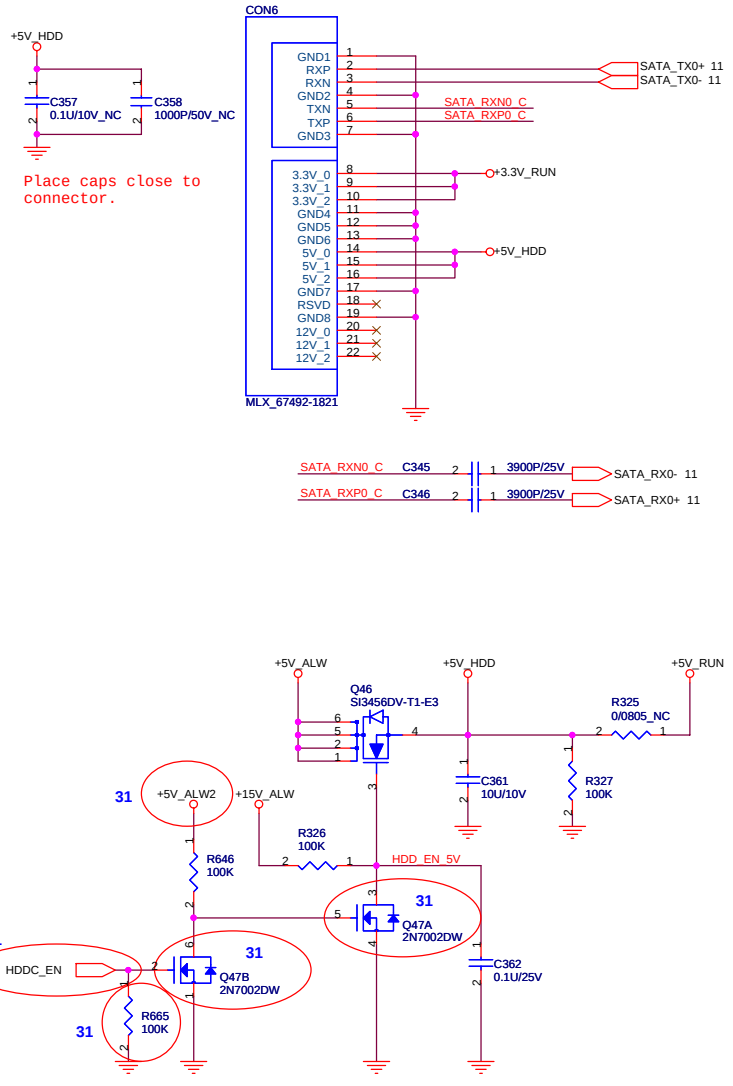
QUANTA COMPUTER		
Title	LCD CONN & CK-SSCD	
Size	Document Number JM7B	Rev 2A
Date: Thursday, September 14, 2006	Sheet 24 of 57	



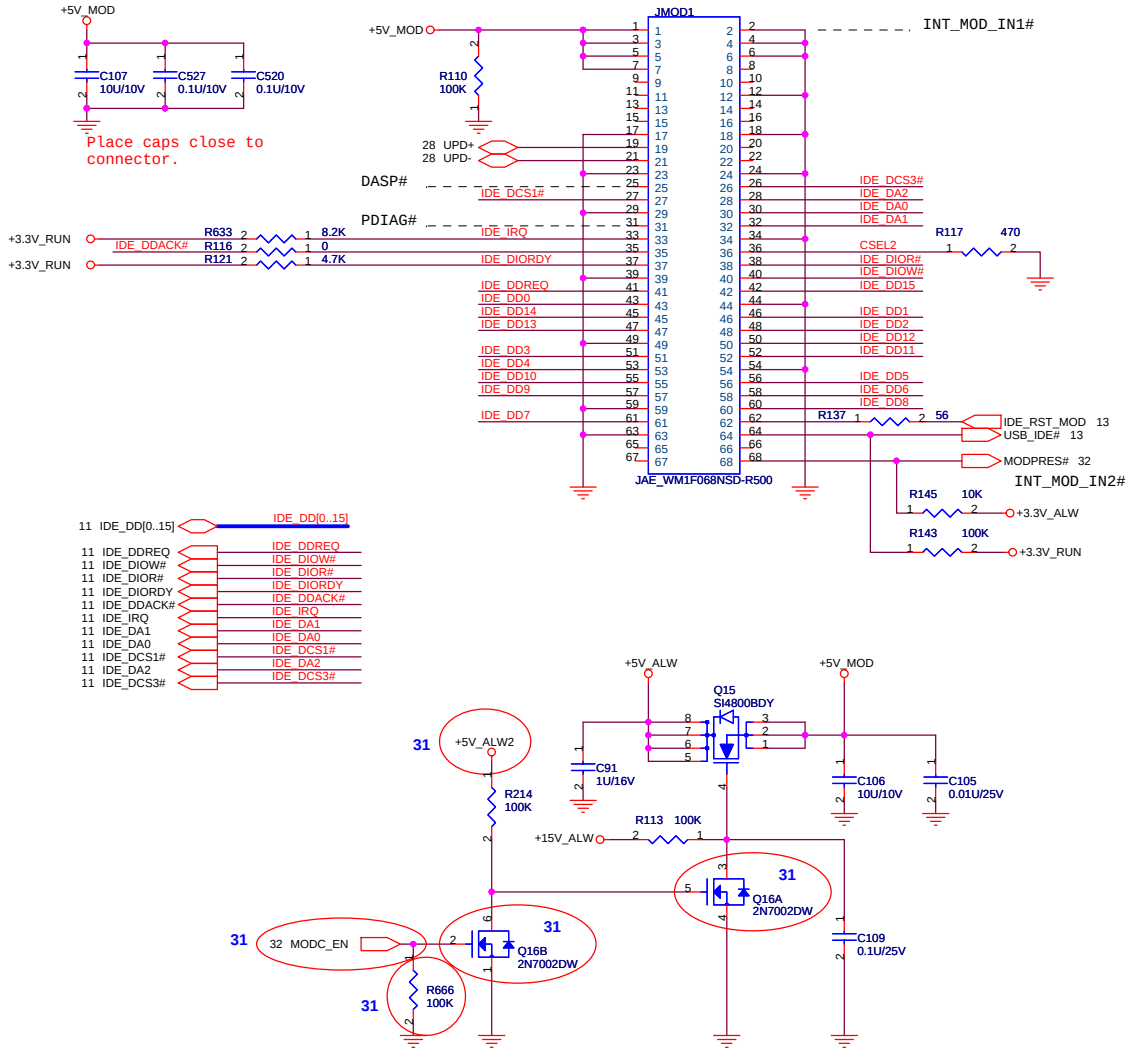
QUANTA COMPUTER

Title	CRT&TV CONN	
Size	Document Number JM7B	Rev 2A
Date: Thursday, September 14, 2006	Sheet 25 of 57	

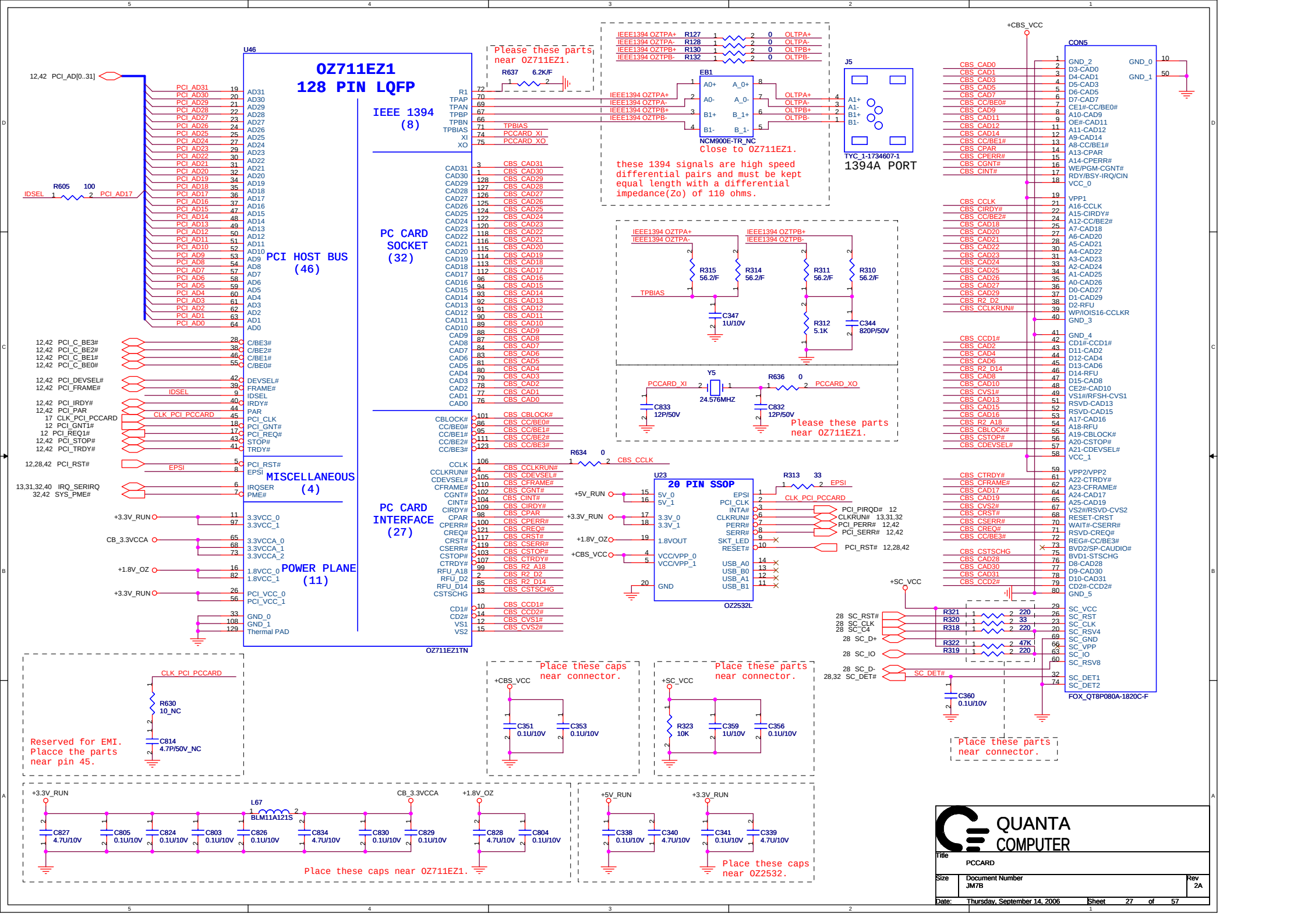
SATA Connector.



ODD Connector.



QUANTA COMPUTER		
Title: SATA (HDD&CD_ROM)		
Size	Document Number: JM7B	Rev: 2A
Date: Thursday, September 14, 2006	Sheet 26 of 57	


OZ711EZ1
128 PIN LQFP
U46
IEEE 1394
(8)
PC CARD
SOCKET
(32)
PCI HOST BUS
(46)
PC CARD
INTERFACE
(27)
MISCELLANEOUS
(4)
POWER PLANE
(11)
OZ711EZ1TN
Please these parts
near OZ711EZ1.
these 1394 signals are high speed
differential pairs and must be kept
equal length with a differential
impedance(Zo) of 110 ohms.
Close to OZ711EZ1.
NCM900E-TR_NC
TYC_1-1734607-1
1394A PORT
Please these parts
near OZ711EZ1.
20 PIN SSOP
OZ2532L
CON5
FOX_QT8P080A-1820C-F
Reserved for EMI.
Place the parts
near pin 45.
Place these caps
near connector.
Place these parts
near connector.
Place these caps near OZ711EZ1.
Place these caps
near OZ2532.
Place these parts
near connector.
QUANTA
COMPUTER
PCCARD
JM7B
2A
Thursday, September 14, 2006
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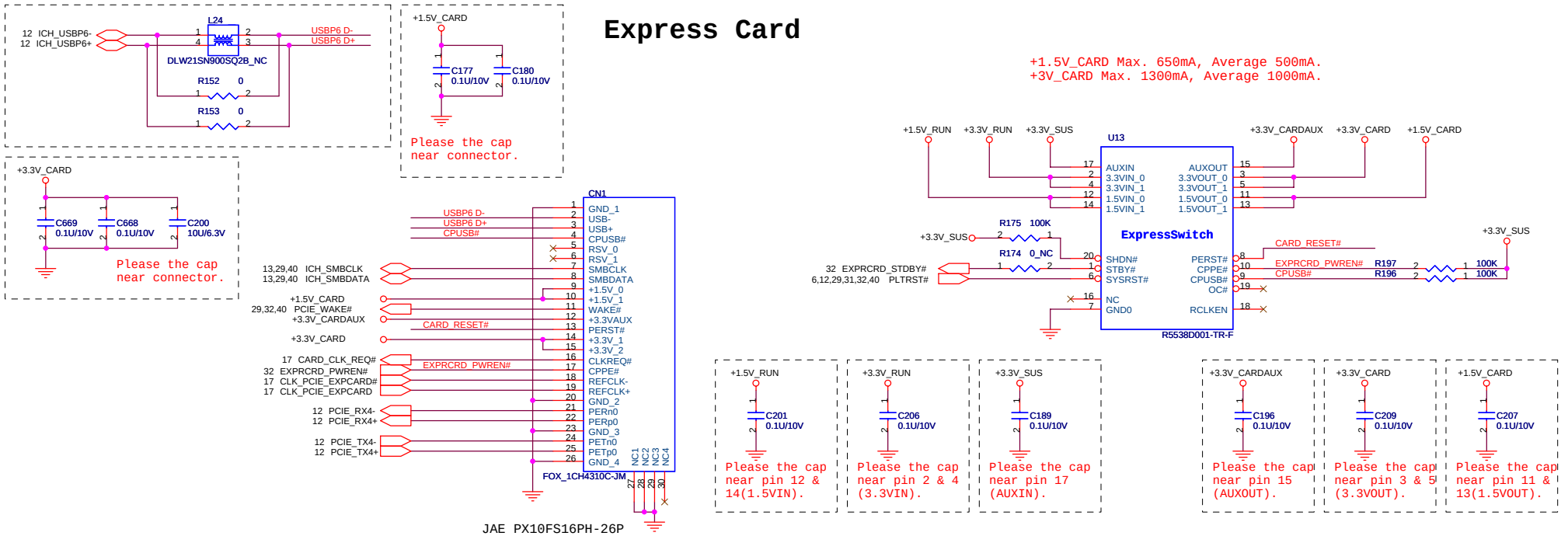
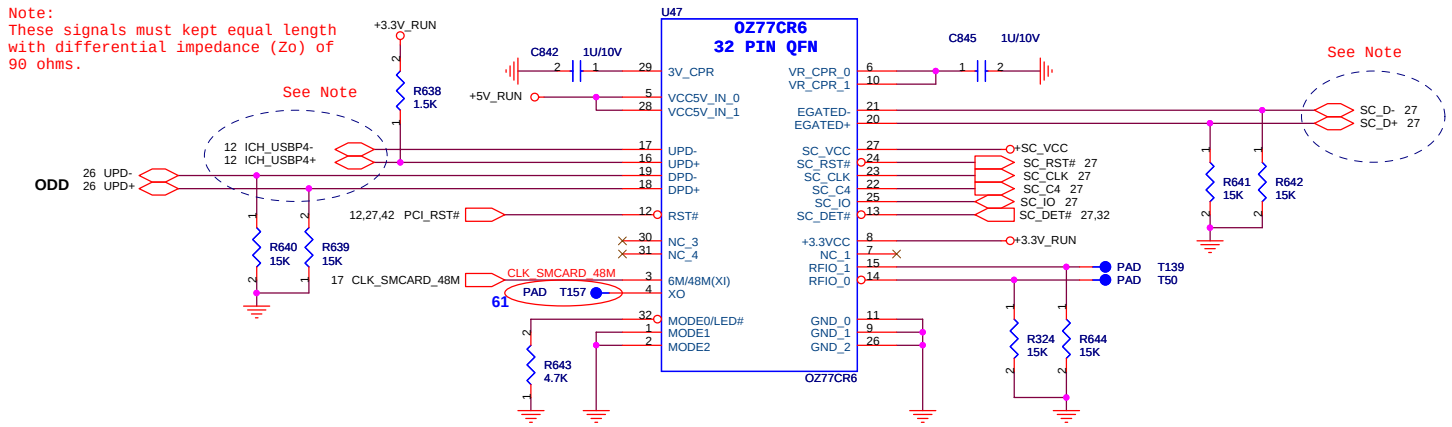
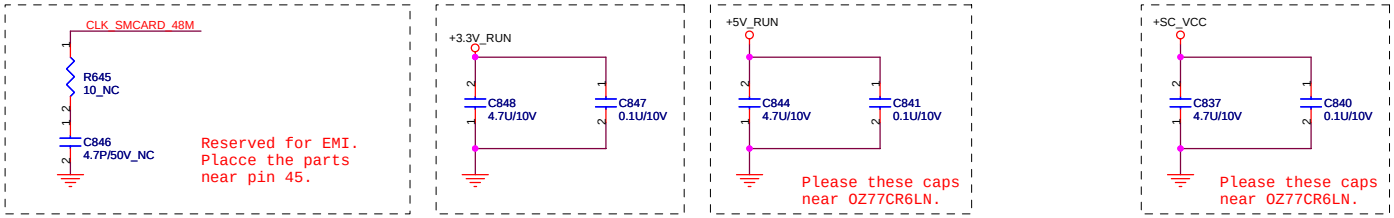
Express Card

+1.5V_CARD Max. 650mA, Average 500mA.
+3V_CARD Max. 1300mA, Average 1000mA.



Smart Card

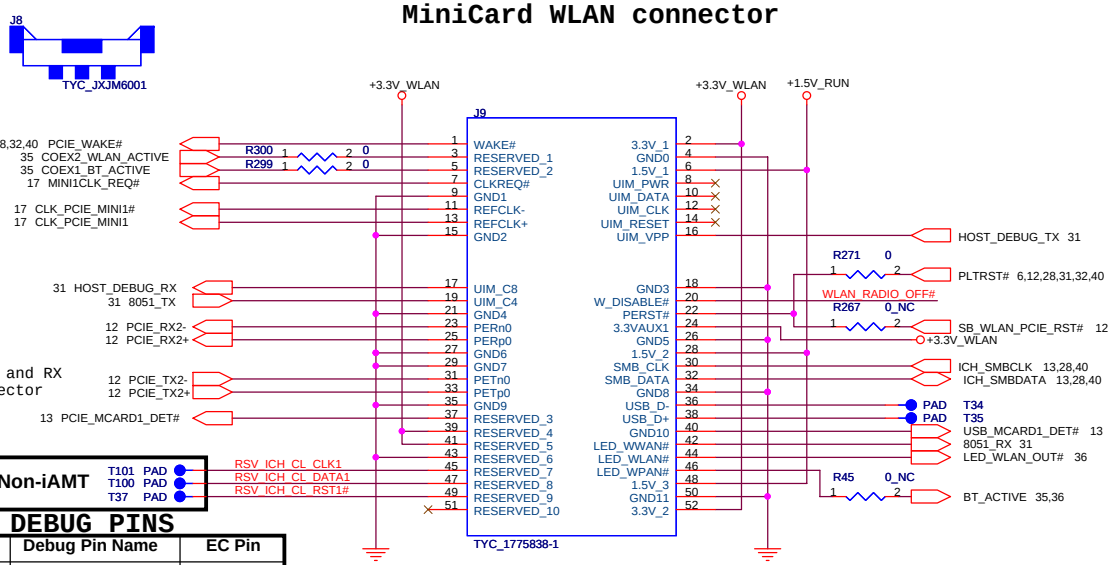




QUANTA COMPUTER

Title	ExpressCard/SmartCard	
Size	Document Number JM7B	Rev 2A
Date: Thursday, September 14, 2006	Sheet 28 of 57	

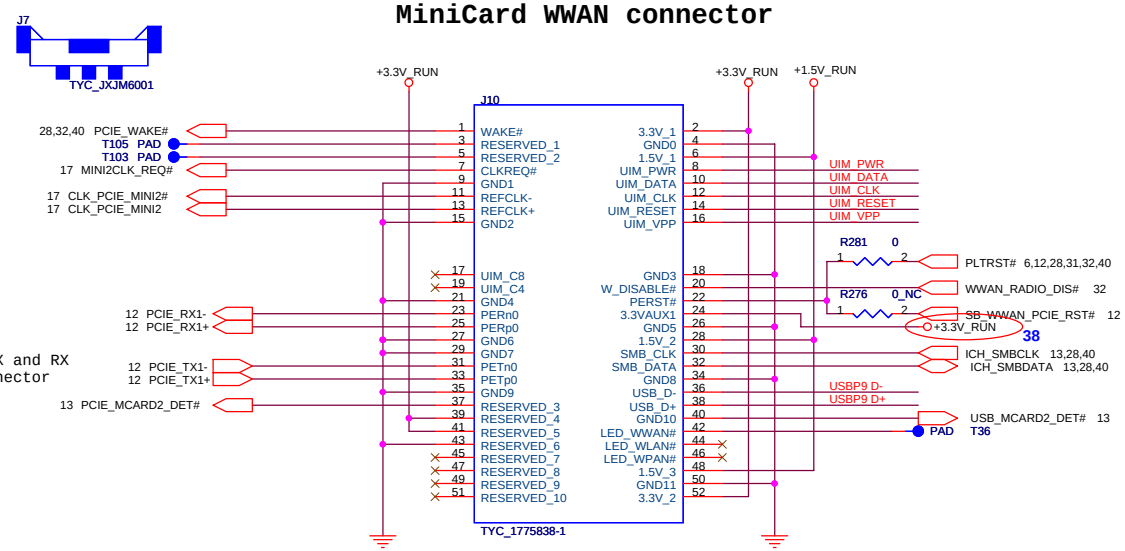
MiniCard WLAN connector

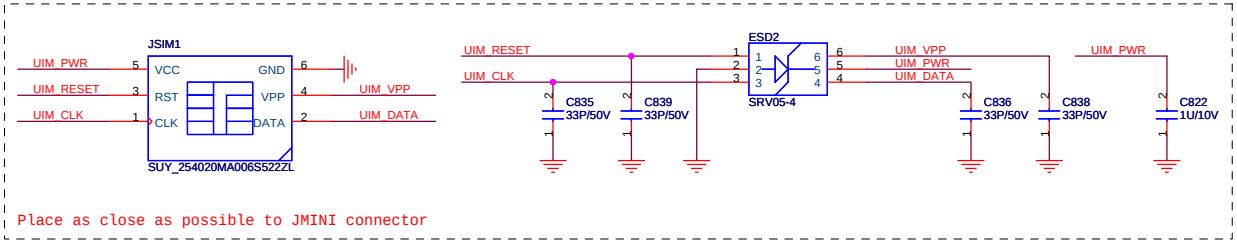


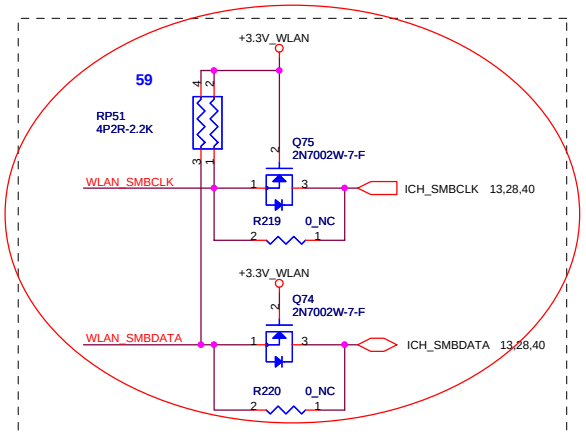
DEBUG PINS

JMINI Pin	Debug Pin Name	EC Pin
16	HOST_DEBUG_TX	70
17	HOST_DEBUG_RX	71
19	8051_TX	82
42	8051_RX	81

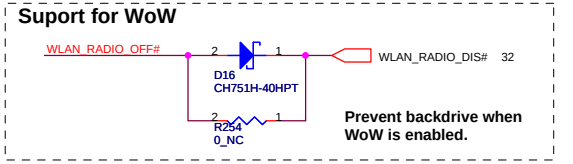
MiniCard WWAN connector

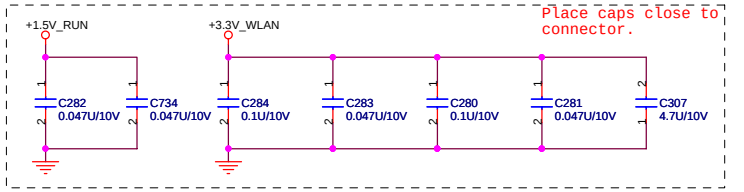




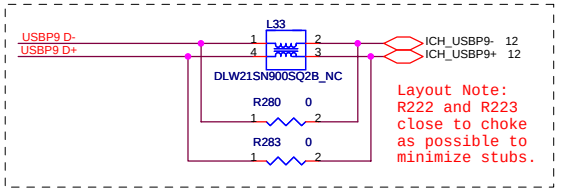


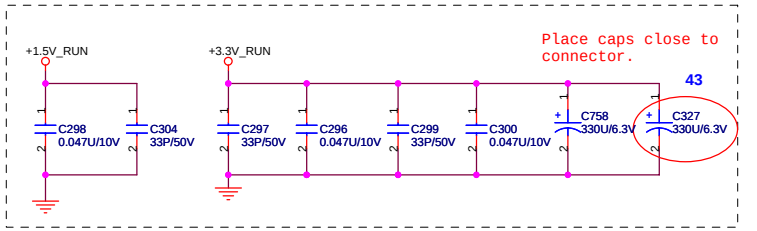
38





38





QUANTA COMPUTER

Title	MINI-PCI	
Size	Document Number JM7B	Rev 2A
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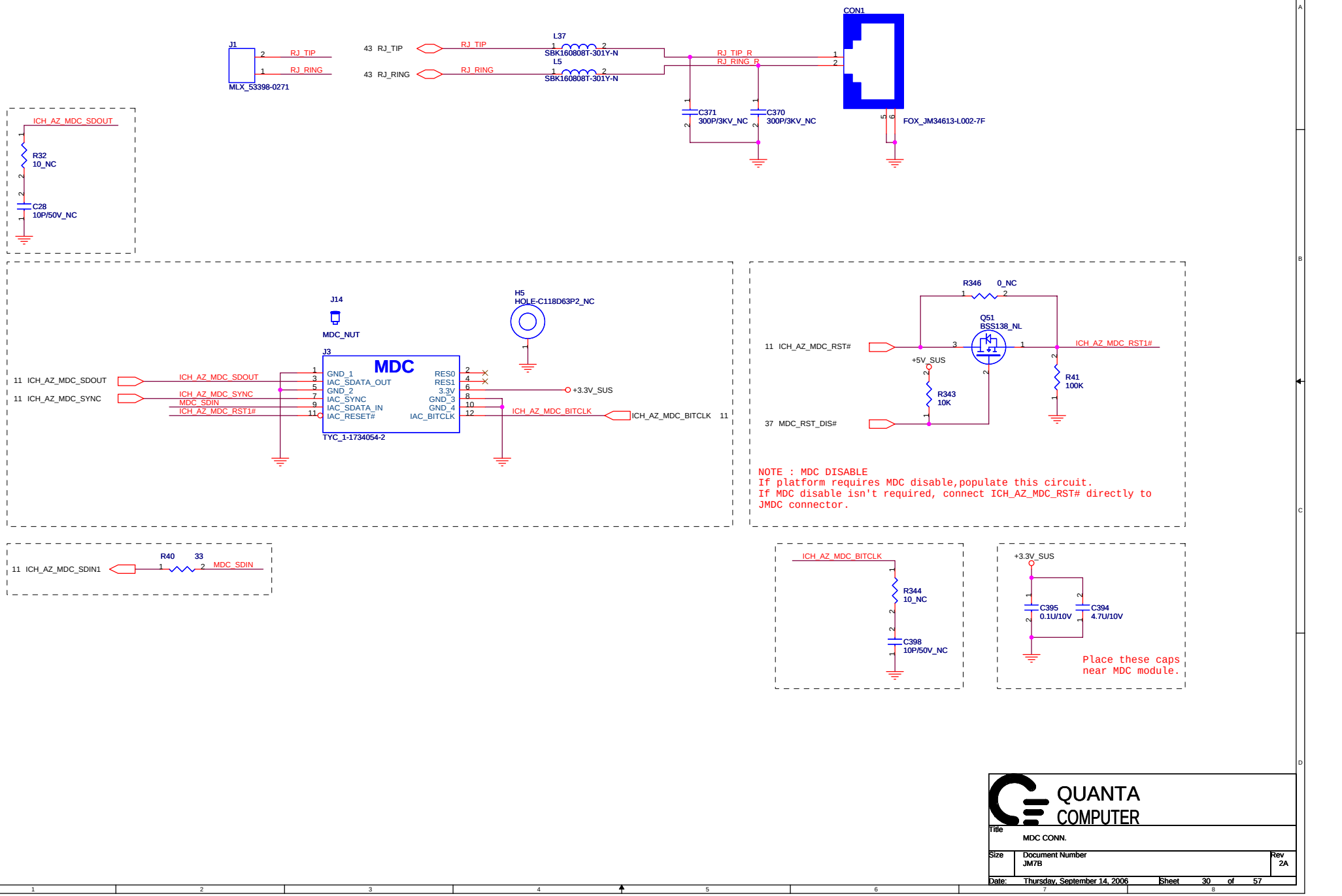

QUANTA COMPUTER		
Title	MDC CONN.	
Size	Document Number JM7B	Rev 2A
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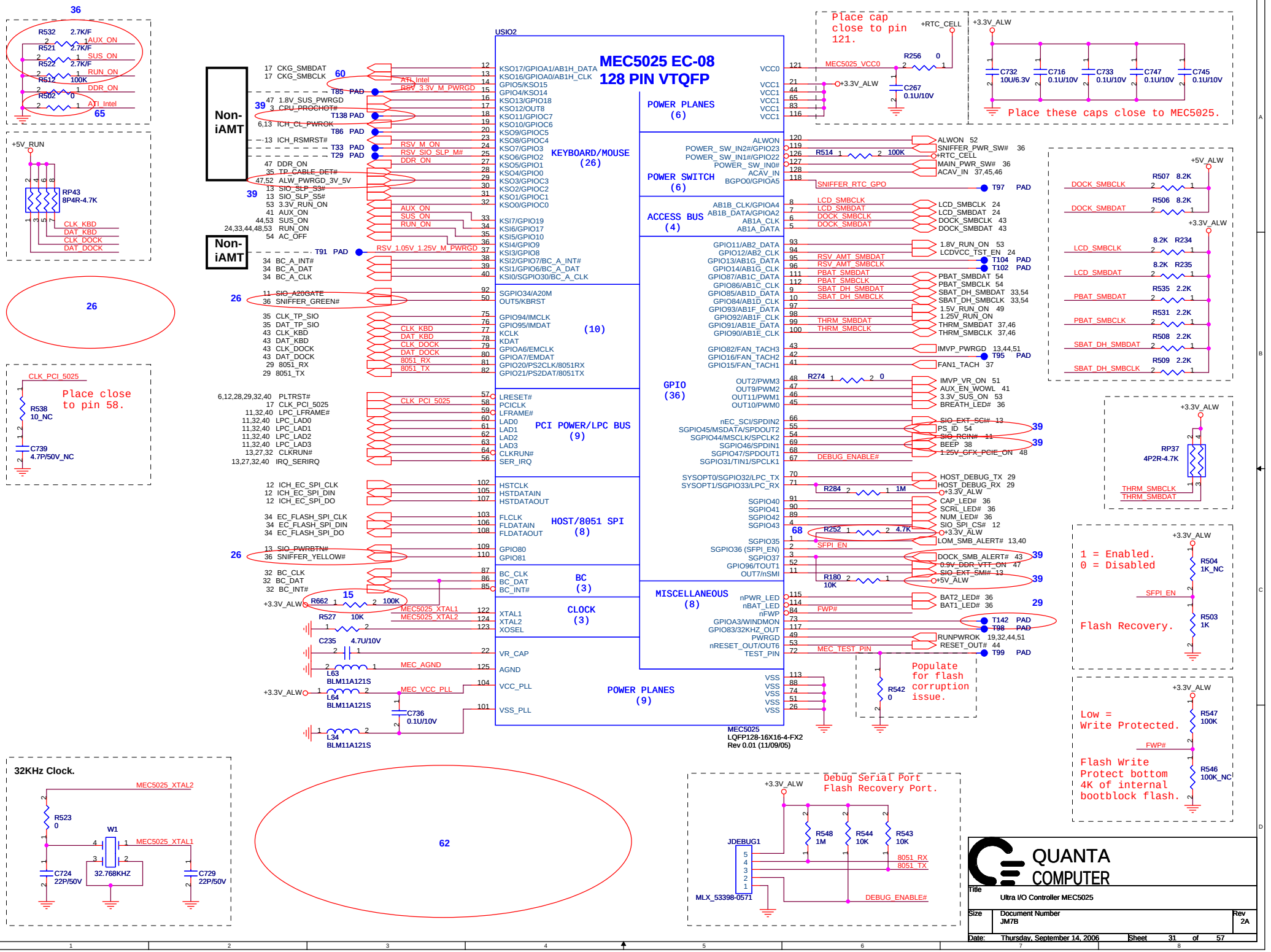
MEC5025 EC-08
128 PIN VTQFP
USIO2
Non-iAMT
Non-iAMT
KEYBOARD/MOUSE (26)
POWER PLANES (6)
POWER SWITCH (6)
ACCESS BUS (4)
GPIO (36)
(10)
PCI POWER/LPC BUS (9)
HOST/8051 SPI (8)
BC (3)
CLOCK (3)
MISCELLANEOUS (8)
POWER PLANES (9)
Place cap close to pin 121.
Place these caps close to MEC5025.
Place close to pin 58.
Place close to pin 58.
1 = Enabled.
0 = Disabled
Flash Recovery.
Low = Write Protected.
Flash Write Protect bottom 4K of internal bootblock flash.
Populate for flash corruption issue.
Debug Serial Port
Flash Recovery Port.
32KHz Clock.
MEC5025 LQFP128-16X16-4-FX2
Rev 0.01 (11/09/05)
QUANTA COMPUTER
Ultra I/O Controller MEC5025
Document Number JM7B
Rev 2A
Thursday, September 14, 2006
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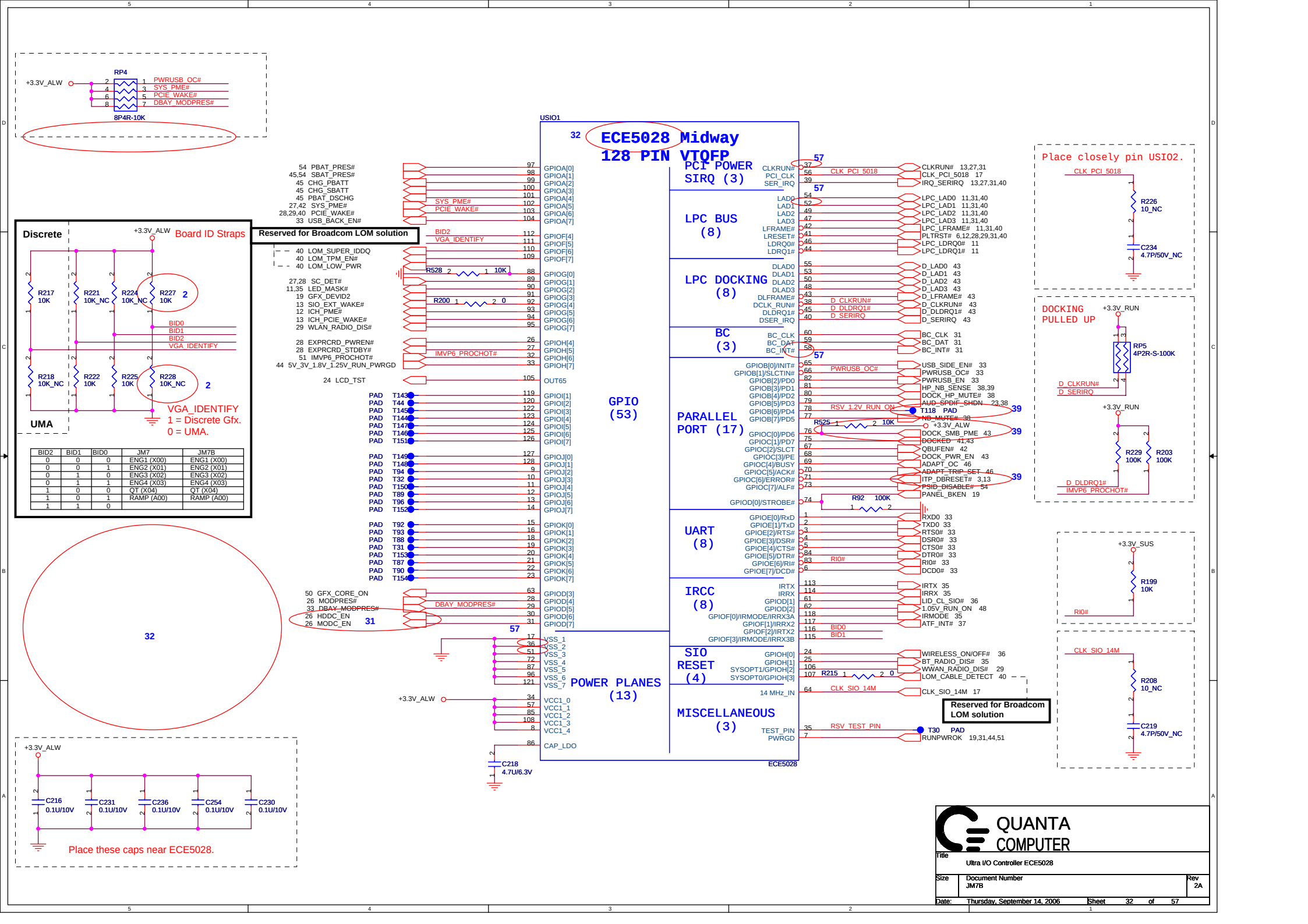
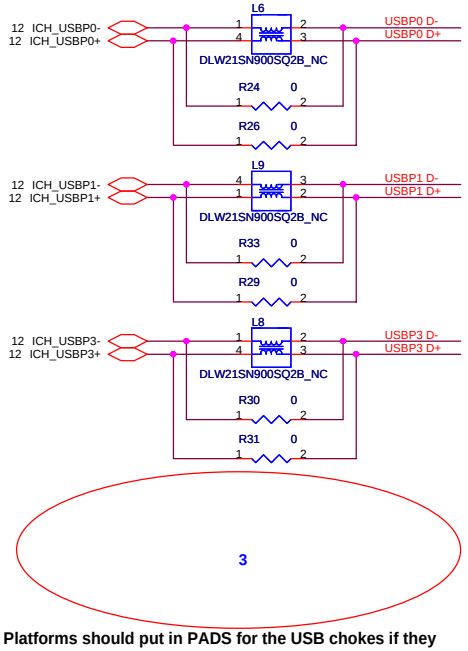
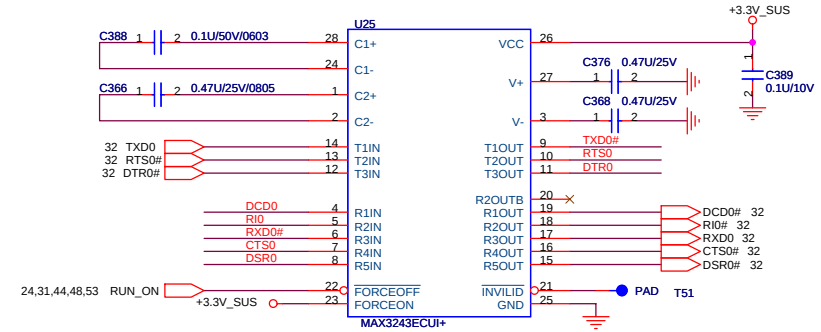


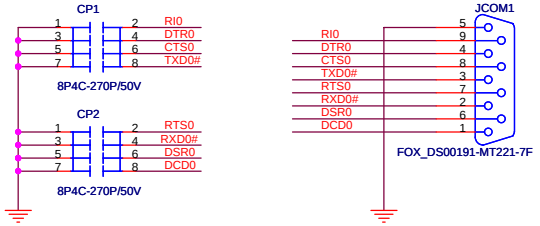
BID2	BID1	BID0	JM7	JM7B
0	0	0	ENG1 (X00)	ENG1 (X00)
0	0	1	ENG2 (X01)	ENG2 (X01)
0	1	0	ENG3 (X02)	ENG3 (X02)
0	1	1	ENG4 (X03)	ENG4 (X03)
1	0	0	QT (X04)	QT (X04)
1	0	1	RAMP (A00)	RAMP (A00)
1	1	0		

External USB PORT hookup reference. Your design may need more or less external ports and may be mapped differently



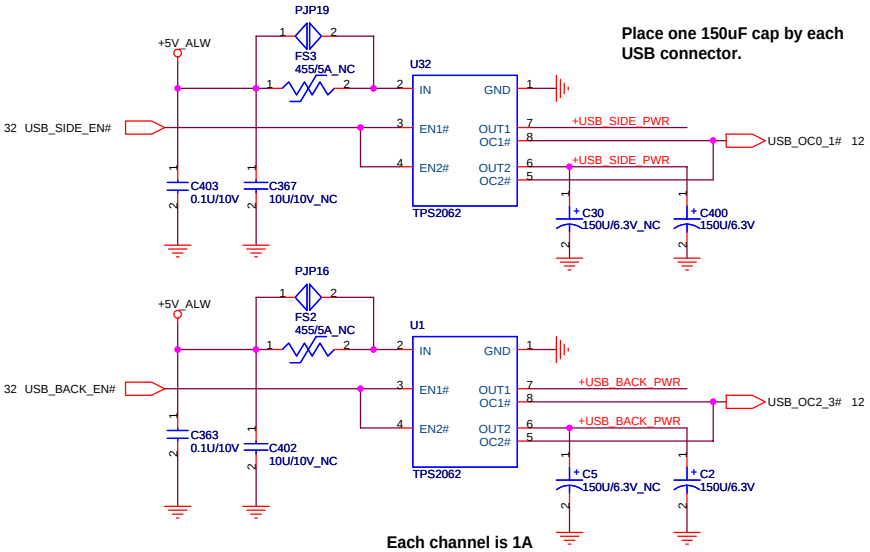
Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.





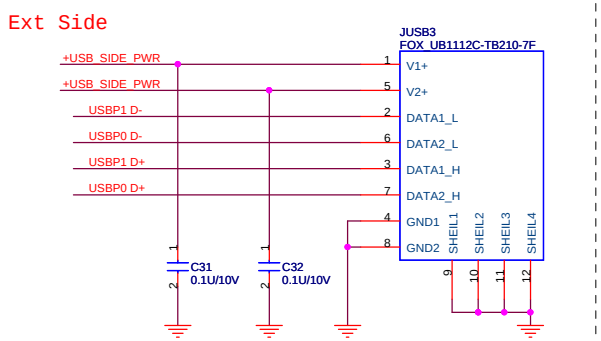
Place these beads close to JCOM1 as soon as possible

If MAX3243 pin 22 tied to RUN_ON,then it can not support Ring Out

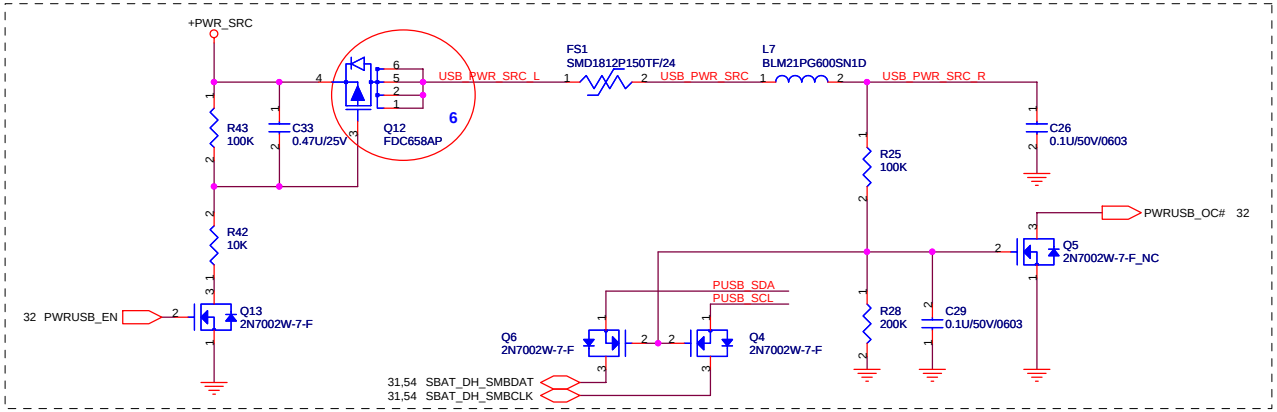


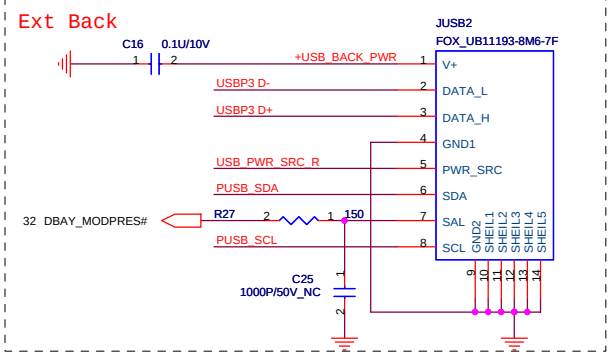
Place one 150uF cap by each USB connector.

Each channel is 1A



3





3

QUANTA COMPUTER

Title	SERIAL PORT & USB	
Size	Document Number JM7B	Rev 2A
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16Mbit (2M Byte), SPI

Non-iAMT +3.3V_SUS

Layout Note:
Place R471 within 500 mils from SPI flash.
Place R498 & R534 within 500 mils of the MEC5025.

12 SPI_CS0#
31 EC_FLASH_SPI_CLK
31 EC_FLASH_SPI_DO
31 EC_FLASH_SPI_DIN

R537 15
R533 15
R529 15

Non-iAMT

R536 10K
R530 10K
16

U43
CE# VDD
SCK
SI
SO HOLD#
WP# VSS
SST_SST25VF016B

C735 0.1U/10V

RTC BATTERY

+RTC_CELL
+3.3V_RTC_LDO
+PWR_SRC

D15
CH751H-40HPT

U17
OUT IN
5/3#
GND SHDN
MAX1615_NC

C289 2.2U/6.3V_NC
C293 1U/25V_NC

D31
CH751H-40HPT
+RTC_1
R463 1K
+RTC

J13
MLX_53261-0271
RTC-BATTERY

C654 1U/25V

Keyboard Scan Extension

+3.3V_ALW

U10

C142 0.1U/10V
C136 0.1U/10V

VCC1
VCC1
NC3
NC1
NC2

ECE1077
40 PIN QFN

+3.3V_ALW
R526 100K_NC
15

31 BC_A_DAT
31 BC_A_CLK
31 BC_A_INT#

BC_DATA
BC_CLK
BC_INT#

R135 0
TEST_PIN
GND_PAD

KSO0 KSO1 KSO2 KSO3 KSO4 KSO5 KSO6 KSO7 KSO8 KSO9 KSO10 KSO11 KSO12 KSO13 KSO14 KSO15
KSO16/GPIO_0
KSO17/GPIO_1
KSO18/GPIO_2
KSO19/GPIO_3
KSO20/GPIO_4
KSO21/GPIO_5
KSO22/GPIO_6

KSO[0..17]
KSO[0..17] 36

KYBD_DET# 36

KSI[0..7]
KSI[0..7] 36

KSI0 KSI1 KSI2 KSI3 KSI4 KSI5 KSI6 KSI7

ECE1077
11/09/2005

QUANTA COMPUTER

Title	FLASH, RTC & KC	
Size	Document Number JM7B	Rev 2A
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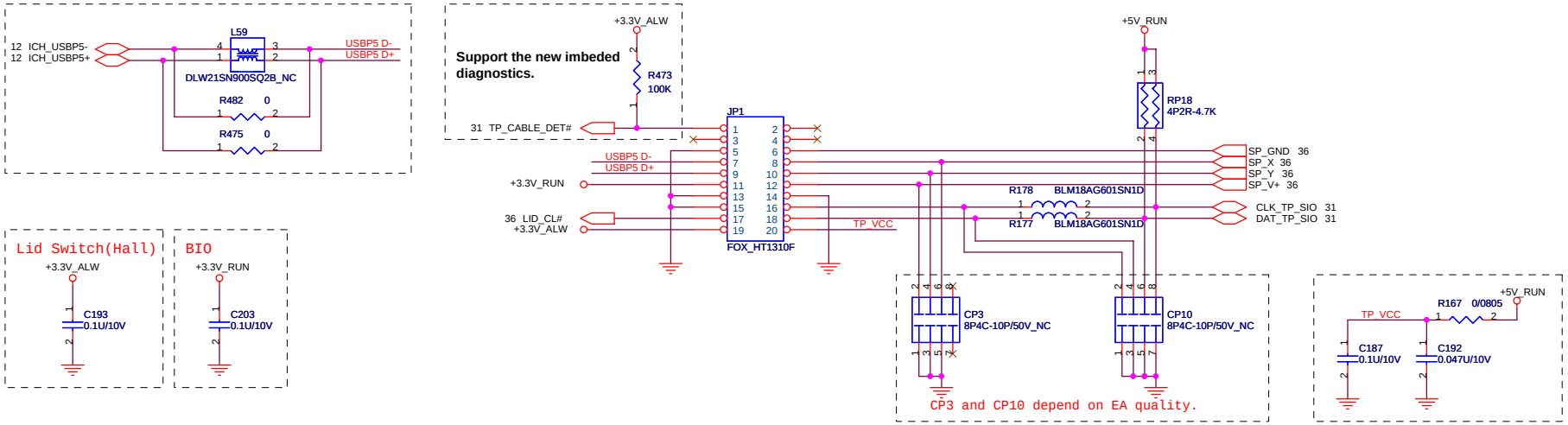
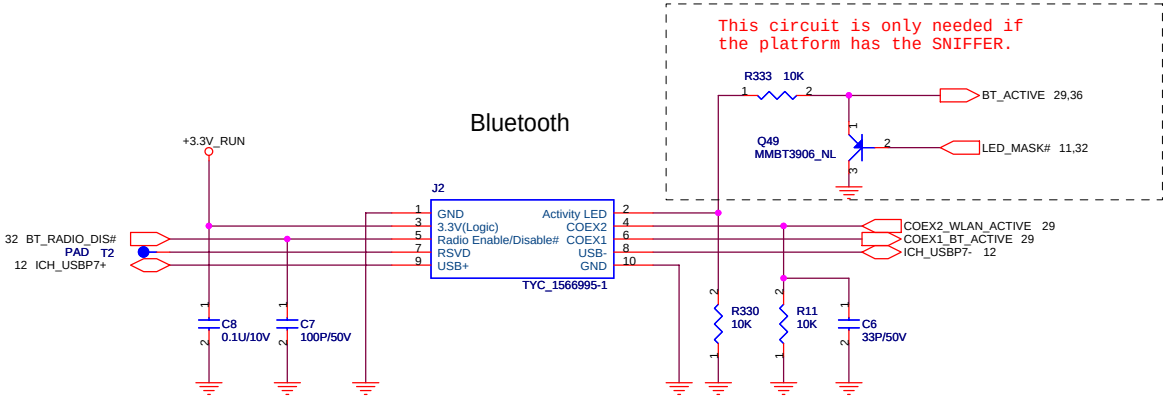
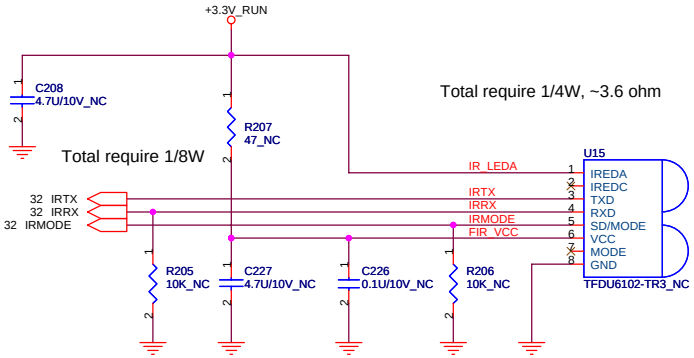
Touch Pad



Bluetooth



FIR



QUANTA COMPUTER

Title	TOUCH PAD, BULE TOOTH & FIR	
Size	Document Number JM7B	Rev 2A
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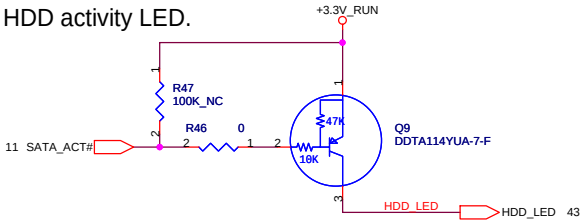
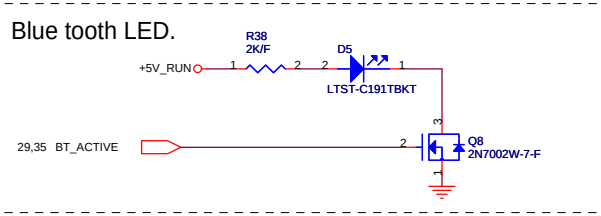
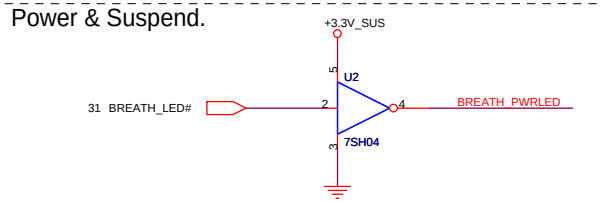
HDD activity LED.



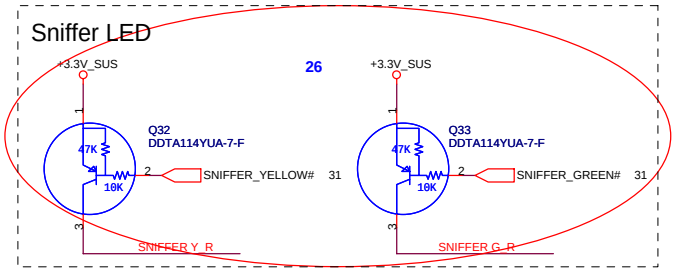
Blue tooth LED.

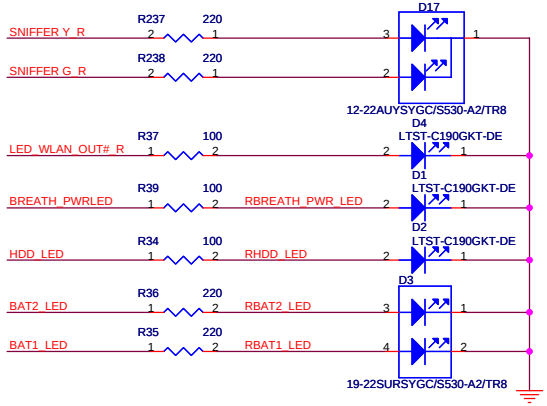


Power & Suspend.

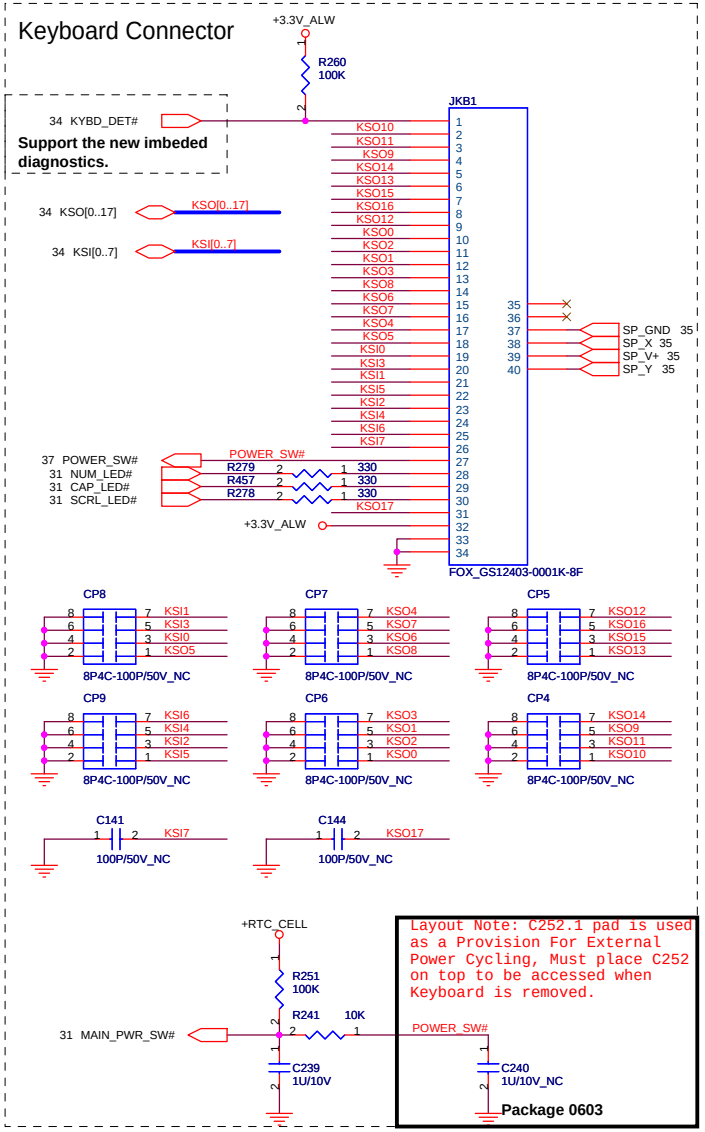


Sniffer LED

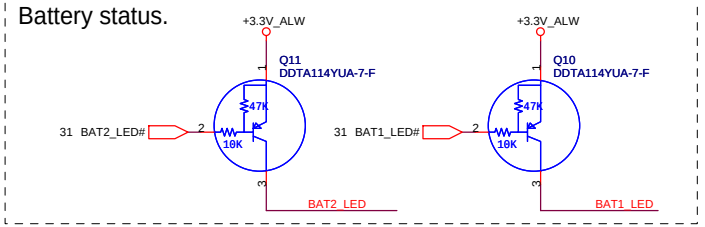




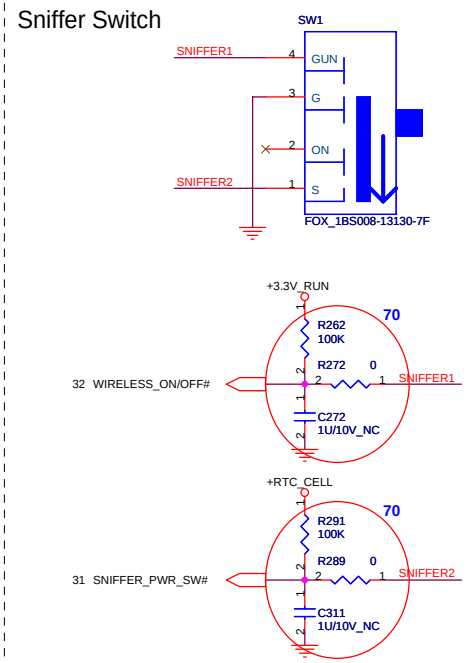
Keyboard Connector



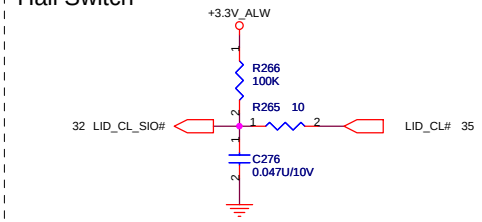
Battery status.



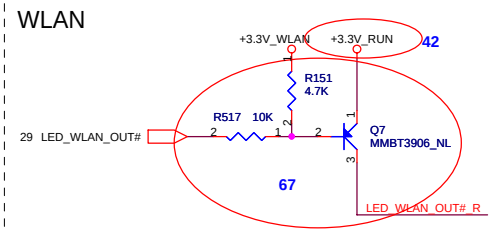
Sniffer Switch



Hall Switch



WLAN



QUANTA COMPUTER		
Title: SWITCH, KEYBOARD & LED		
Size	Document Number: JM7B	Rev: 2A
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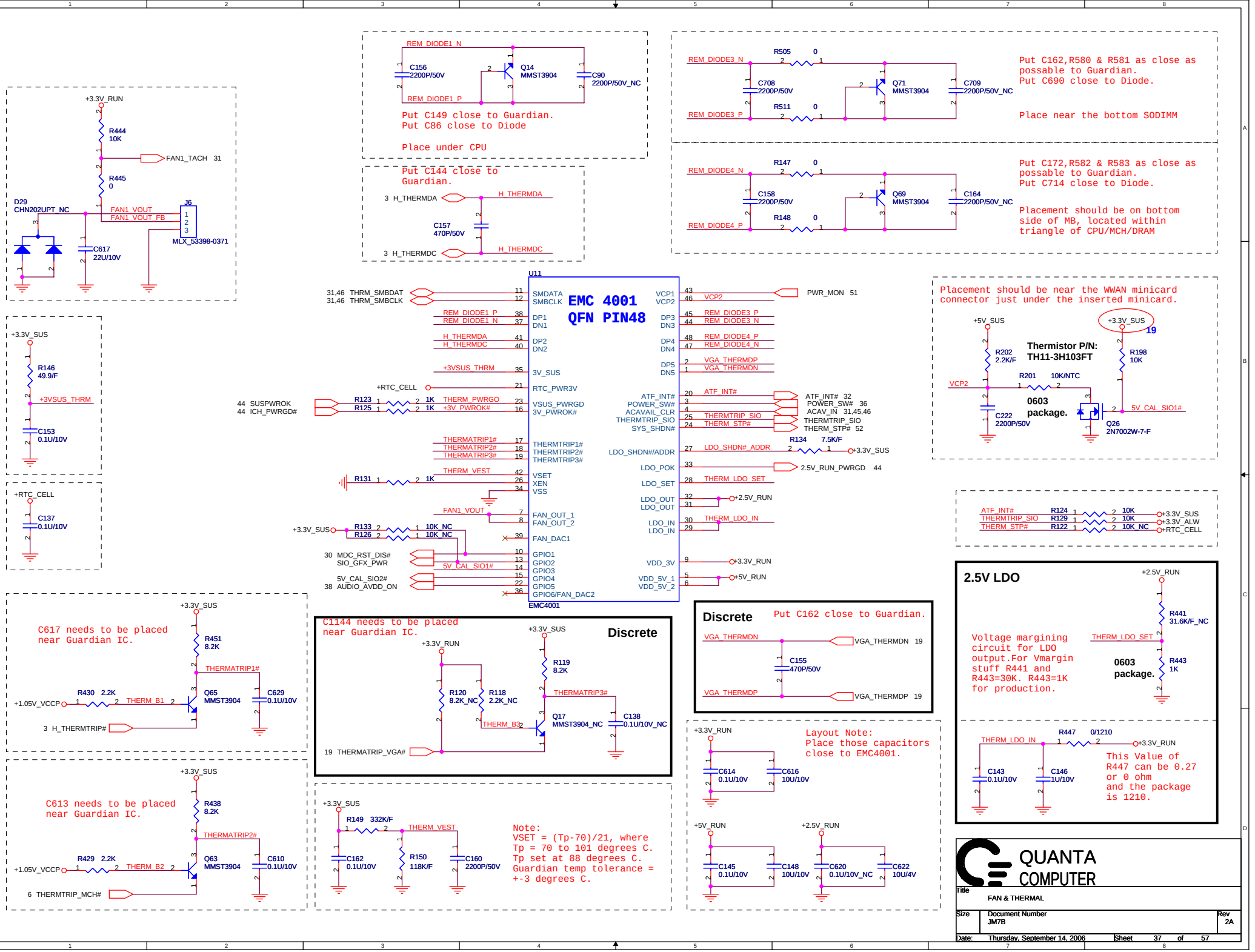
+3.3V_RUN
R444 10K
FAN1_TACH 31
R445 0
D29 CHN202UPT_NC
FAN1_VOUT
FAN1_VOUT_FB
J6
MLX_53398-0371
C617 22U/10V
+3.3V_SUS
R146 49.9/F
+3VSUS_THRM
C153 0.1U/10V
+RTC_CELL
C137 0.1U/10V
REM_DIODE1_N
REM_DIODE1_P
C156 2200P/50V
Q14 MMST3904
C90 2200P/50V_NC
Put C149 close to Guardian.
Put C86 close to Diode
Place under CPU
Put C144 close to Guardian.
3 H_THERMDA
H_THERMDA
C157 470P/50V
3 H_THERMDC
H_THERMDC
REM_DIODE3_N
REM_DIODE3_P
R505 0
R511 0
C708 2200P/50V
Q71 MMST3904
C709 2200P/50V_NC
Put C162,R580 & R581 as close as possable to Guardian.
Put C690 close to Diode.
Place near the bottom SODIMM
REM_DIODE4_N
REM_DIODE4_P
R147 0
R148 0
C158 2200P/50V
Q69 MMST3904
C164 2200P/50V_NC
Put C172,R582 & R583 as close as possable to Guardian.
Put C714 close to Diode.
Placement should be on bottom side of MB, located within triangle of CPU/MCH/DRAM
U11
EMC 4001
QFN PIN48
31,46 THRM_SMBDAT
31,46 THRM_SMBCLK
SMDATA
SMBCLK
REM_DIODE1_P
REM_DIODE1_N
DP1
DN1
H_THERMDA
H_THERMDC
DP2
DN2
+3VSUS_THRM
3V_SUS
+RTC_CELL
RTC_PWR3V
44 SUSPWROK
44 ICH_PWRGD#
R123 1K
R125 1K
THERM_PWRGO
+3V_PWROK#
VSUS_PWRGD
3V_PWROK#
THERMATRIP1#
THERMATRIP2#
THERMATRIP3#
THERMTRIP1#
THERMTRIP2#
THERMTRIP3#
THERM_VEST
R131 1K
VSET
XEN
VSS
FAN1_VOUT
FAN_OUT_1
FAN_OUT_2
+3.3V_SUS
R133 10K_NC
R126 10K_NC
FAN_DAC1
30 MDC_RST_DIS#
SIO_GFX_PWR
5V_CAL_SIO2#
38 AUDIO_AVDD_ON
GPIO1
GPIO2
GPIO3
GPIO4
GPIO5
GPIO6/FAN_DAC2
EMC4001
VCP1
VCP2
DP3
DN3
DP4
DN4
DP5
DN5
PWR_MON 51
REM_DIODE3_P
REM_DIODE3_N
REM_DIODE4_P
REM_DIODE4_N
VGA_THERMDP
VGA_THERMDN
ATF_INT#
POWER_SW#
ACAVAIL_CLR
THERMTRIP_SIO
SYS_SHDN#
ATF_INT# 32
POWER_SW# 36
ACAV_IN 31,45,46
THERMTRIP_SIO
THERM_STP# 52
LDO_SHDN#/ADDR
R134 7.5K/F
LDO_SHDN#_ADDR
+3.3V_SUS
LDO_POK
2.5V_RUN_PWRGD 44
LDO_SET
THERM_LDO_SET
LDO_OUT
LDO_OUT
+2.5V_RUN
LDO_IN
LDO_IN
THERM_LDO_IN
VDD_3V
+3.3V_RUN
VDD_5V_1
VDD_5V_2
+5V_RUN
Placement should be near the WWAN minicard connector just under the inserted minicard.
+5V_SUS
+3.3V_SUS
19
R202 2.2K/F
Thermistor P/N:
TH11-3H103FT
R201 10K/NTC
0603 package.
R198 10K
VCP2
C222 2200P/50V
5V_CAL_SIO1#
Q26 2N7002W-7-F
ATF_INT#
THERMTRIP_SIO
THERM_STP#
R124 10K
R129 10K
R122 10K_NC
+3.3V_SUS
+3.3V_ALW
+RTC_CELL
C617 needs to be placed near Guardian IC.
+3.3V_SUS
R451 8.2K
THERMATRIP1#
R430 2.2K
+1.05V_VCCP
THERM_B1
Q65 MMST3904
C629 0.1U/10V
3 H_THERMTRIP#
C1144 needs to be placed near Guardian IC.
+3.3V_RUN
+3.3V_SUS
Discrete
R120 8.2K_NC
R118 2.2K_NC
R119 8.2K
THERMATRIP3#
THERM_B3
Q17 MMST3904_NC
C138 0.1U/10V_NC
19 THERMATRIP_VGA#
Discrete
Put C162 close to Guardian.
VGA_THERMDN
VGA_THERMDN 19
C155 470P/50V
VGA_THERMDP
VGA_THERMDP 19
2.5V LDO
+2.5V_RUN
R441 31.6K/F_NC
Voltage margining circuit for LDO output.For Vmargin stuff R441 and R443=30K. R443=1K for production.
THERM_LDO_SET
0603 package.
R443 1K
C613 needs to be placed near Guardian IC.
+3.3V_SUS
R438 8.2K
THERMATRIP2#
R429 2.2K
+1.05V_VCCP
THERM_B2
Q63 MMST3904
C610 0.1U/10V
6 THERMTRIP_MCH#
+3.3V_SUS
R149 332K/F
THERM_VEST
C162 0.1U/10V
R150 118K/F
C160 2200P/50V
Note:
VSET = (Tp-70)/21, where
Tp = 70 to 101 degrees C.
Tp set at 88 degrees C.
Guardian temp tolerance = +-3 degrees C.
+3.3V_RUN
Layout Note:
Place those capacitors close to EMC4001.
C614 0.1U/10V
C616 10U/10V
+5V_RUN
+2.5V_RUN
C145 0.1U/10V
C148 10U/10V
C620 0.1U/10V_NC
C622 10U/4V
THERM_LDO_IN
R447 0/1210
+3.3V_RUN
C143 0.1U/10V
C146 1U/10V
This Value of R447 can be 0.27 or 0 ohm and the package is 1210.
QUANTA COMPUTER
Title
FAN & THERMAL
Size
Document Number
JM7B
Rev
2A
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INTERNAL SPEAKER AMP

Package 1206 for THD+N performance and Vista Logo requirements.

X7R

AUD_LINE_OUT_L C334 0.033U/200V
AUD_LINE_OUT_R C291 0.033U/200V
AUD_HP_OUT_L C768 2.2U/25V
AUD_HP_OUT_R C751 2.2U/25V
21
C753 47P/50V_NC
C764 47P/50V_NC
C288 47P/50V_NC
C323 47P/50V_NC
C308 1U/10V
T106 PAD

U20
MAX9789A
TQFN 32PIN
MAX9789A

LIN-
RIN-
HP_OUT_L
HP_OUT_R
AUD_SPK_ENABLE#
AUD_HP_NB_SENSE
AUD_AMP_MUTE#
AUD_AMP_GAIN1
AUD_AMP_GAIN2

SPKR_INL
SPKR_INR
HP_INL
HP_INR
BIAS
SPKR_EN#
HP_EN
MUTE#
GAIN1
GAIN2
HPVDD
CPVDD
C1P
C1N
CPGND
PVSS
CPVSS

OUTL+
OUTL-
OUTR+
OUTR-
HPL
HPR
REGEN
SET
VOUT
VDD
PVDD_8
PVDD_18
GND_28
PGND_5
PGND_21

AUD_SPK_L1
AUD_SPK_L2
AUD_SPK_R1
AUD_SPK_R2
AUD_HP_JACK_L 39
AUD_HP_JACK_R 39
REGEN
SET
+VDDA
VDD
+5V_SPK_AMP
+5V_SPK_AMP

+5V_SPK_AMP
C309 10U/10V_NC
C303 1U/10V
22
C255 1U/16V
C256 1U/16V

JSPK1
MLX_53398-0471
AUD_SPK_R1
AUD_SPK_R2
AUD_SPK_L1
AUD_SPK_L2
C717 100P/50V
C718 100P/50V
C719 100P/50V
C720 100P/50V

L35
FB_600ohm+-25%_100MHz
_200mA_0.6ohm DC
+5V_SPK_AMP
VDD
C319 1U/10V
C292 1U/10V
C294 0.1U/10V
Layout Note: Place close U22.

+VDDA
C277 1U/10V
C274 1U/10V
Layout Note: Place close U22.

For TPA6040A,pop C866,depop R865.
+5V_SPK_AMP
R552 100K
R551 0_NC
AUDIO_AVDD_ON
AUD_AMP_MUTE#

AUDIO_AVDD_ON
AUDIO_AVDD_ON 37
R557 0
REGEN
C763 0.033U/16V_NC
For TPA6040A,pop C1425,depop R409.

+5V_SPK_AMP
+5V_RUN
+5V_SPK_AMP
L31
BLM21PG600SN1D
C320 1U/10V_NC
C326 10U/10V_NC
Layout Note: Place close to pin 8.
FB_60ohm+-25%_100MHz
_3A_0.05ohm DC
C265 1U/10V
C253 10U/10V
Layout Note: Place close to pin 18.

+5V_SPK_AMP
R282 100K
R295 100K
AUD_SPK_ENABLE#
AUD_EAPD
Q41 2N7002W-7-F
NB_MUTE#
Q34 2N7002W-7-F

+5V_SPK_AMP
R550 100K_NC 40
R296 100K 40
AUD_AMP_GAIN1
AUD_AMP_GAIN2
40
R549 100K 40
R297 100K_NC 40

GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

C268 0.1U/10V
+3.3V_RUN
U16
TSH08
AUD_HP_NB_SENSE
HP_NB_SENSE
NB_MUTE#
NB_MUTE# 32

For TPA6040A,pop C331,depop R406.
SET
C322 0.033U/16V_NC
R298 0

AZALIA (HD) CODEC

U19
STAC9205
QFN 48PIN
23
STAC9205X5NBEB1XR

11 ICH_AZ_CODEC_BITCLK
11 ICH_AZ_CODEC_SDIN0
11 ICH_AZ_CODEC_SDOUT
11 ICH_AZ_CODEC_SYNC
11 ICH_AZ_CODEC_RST#
ICH_AZ_CODEC_BITCLK
R277 33 SDIN
ICH_AZ_CODEC_SDOUT

HDA_BITCLK
HDA_SDI_CODEC
HDA_SDO
HDA_SYNC
HDA_RST#
DMIC_CLK
DMIC0/VOL_UP/GPIO1
DMIC1/VOL_DN/GPIO2
SPDIF_IN/EAPD/GPIO0
SPDIF_OUT
NC_43
NC_44
NC_45
DVDD_CORE_1
DVDD_CORE_9
DVDD_CORE_40
DVDD_IO
AVDD_25
AVDD_38
DVSS
AVSS_26
AVSS_42

SENSE_A
SENSE_B
PORT_A_L
PORT_A_R
VREFOUT_A
PORT_B_L
PORT_B_R
VREFOUT_B
PORT_C_L
PORT_C_R
VREFOUT_C
PORT_D_L
PORT_D_R
PORT_E_L
PORT_E_R
GPIO4/VREFOUT_E
PORT_F_L
PORT_F_R
GPIO3/VREFOUT_F
CD_L
CD_GND
CD_R
PC_BEEP
MONO_OUT
VREFFILT
CAP2

+VDDA
R255 100K
AUD_SENSE_A
AUD_SENSE_B
AUD_HP_OUT_L
AUD_HP_OUT_R
AUD_EXT_MIC_L 39
AUD_EXT_MIC_R 39
AUD_VREFOUT_B 39
AUD_INT_MIC_IN 39
AUD_LINE_OUT_L
AUD_LINE_OUT_R
R268 10K
+VDDA
DOCK_HP_MUTE# 32
R263 10K
+VDDA
AUD_SPDIF_SHDN 23,32
AUD_PC_BEEP
AC97VREFI
CAP2
C273 10U/6.3V
C287 10U/6.3V

For tuning.
23,43 AUD_SPDIF_OUT
R257 0
AUD_EAPD
SPDIF_OUT

+3.3V_RUN
C305 10U/10V_NC
C301 0.1U/10V
C302 1U/10V
+3.3V_RUN
C260 0.1U/10V
+VDDA
C258 0.1U/16V
C295 1U/10V
C261 10U/10V_NC

ICH_AZ_CODEC_BITCLK
R275 47_NC
Close to pin 6.
C290 0.1U/10V_NC

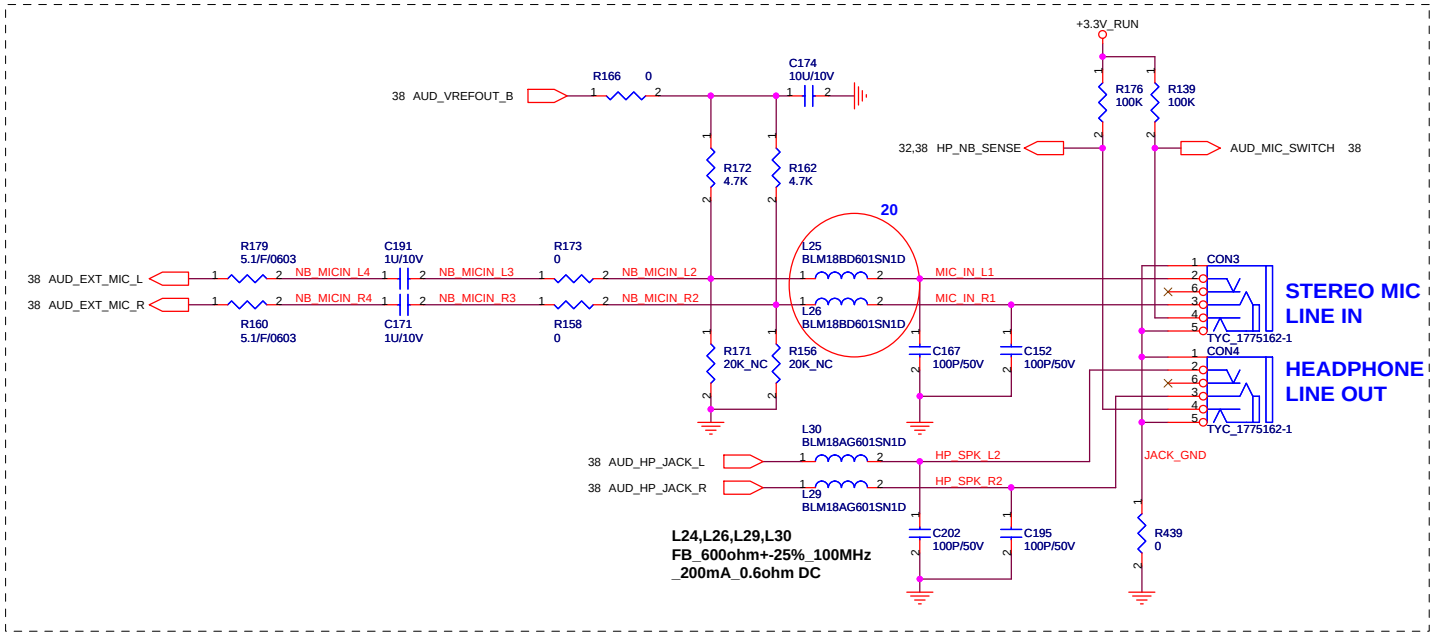
ICH_AZ_CODEC_SDOUT
R273 47_NC
Close to pin 5.
C286 0.1U/10V_NC

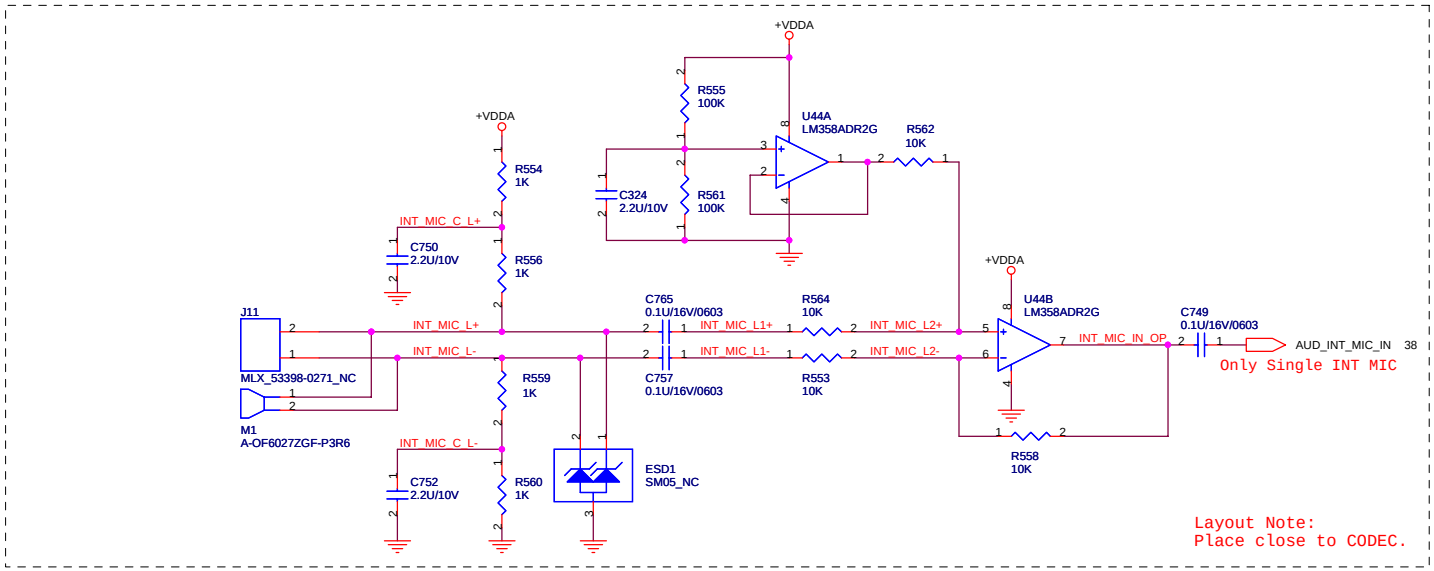
Layout Note: Close to Pin 13.
+VDDA
R285 5.1K/F
AUD_SENSE_A
R286 39.2K/F
R288 20K/F
C315 1000P/50V
32,39 HP_NB_SENSE
HP_NB_SENSE
AUD_MIC_SWITCH 39
Q42 2N7002W-7-F
Q43 2N7002W-7-F

Close to U21.
+VDDA
C278 0.1U/16V
C279 0.1U/10V
R261 20K
AUD_PC_BEEP
BEEP2
BEEP1
R264 10K_NC
BEEP 31
SPKR 13
U18 74LVC1G86GW

QUANTA COMPUTER

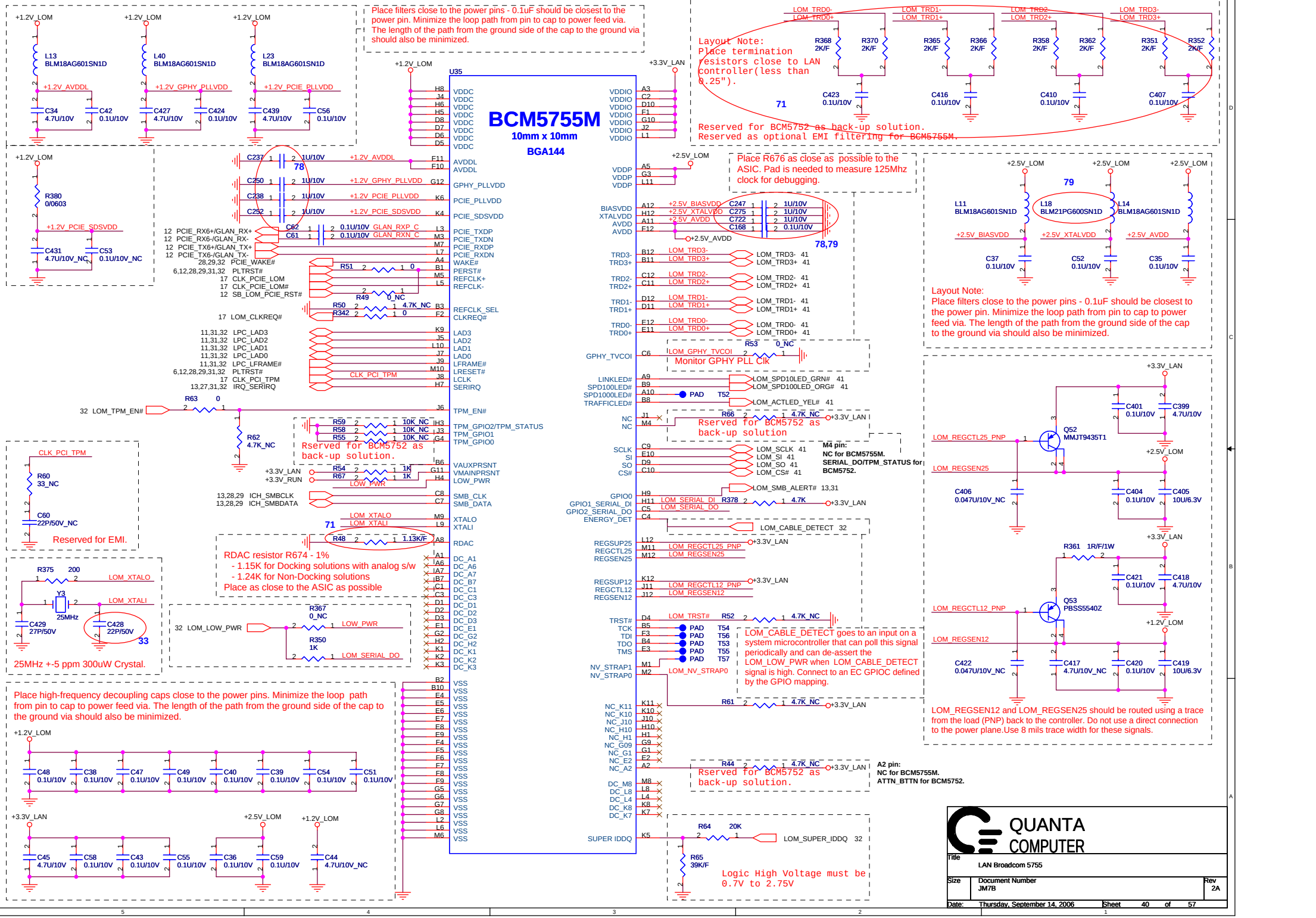
Title	Azalia CODEC	
Size	Document Number JM7B	Rev 2A
Date: Thursday, September 14, 2006	Sheet 38 of 57	





QUANTA COMPUTER

Title	AUDIO CONN	
Size	Document Number JM7B	Rev 2A
Date: Thursday, September 14, 2006	Sheet 39 of 57	


BCM5755M
10mm x 10mm
BGA144
U35
Place filters close to the power pins - 0.1uF should be closest to the power pin. Minimize the loop path from pin to cap to power feed via. The length of the path from the ground side of the cap to the ground via should also be minimized.
Layout Note:
Place termination resistors close to LAN controller(less than 0.25").
Reserved for BCM5752 as back-up solution.
Reserved as optional EMI filtering for BCM5755M.
Place R676 as close as possible to the ASIC. Pad is needed to measure 125Mhz clock for debugging.
Layout Note:
Place filters close to the power pins - 0.1uF should be closest to the power pin. Minimize the loop path from pin to cap to power feed via. The length of the path from the ground side of the cap to the ground via should also be minimized.
Monitor GPHY PLL Clk
Rserved for BCM5752 as back-up solution
Rserved for BCM5752 as back-up solution.
M4 pin:
NC for BCM5755M.
SERIAL_DO/TPM_STATUS for BCM5752.
A2 pin:
NC for BCM5755M.
ATTN_BTTN for BCM5752.
LOM_CABLE_DETECT goes to an input on a system microcontroller that can poll this signal periodically and can de-assert the LOM_LOW_PWR when LOM_CABLE_DETECT signal is high. Connect to an EC GPIOC defined by the GPIO mapping.
RDAC resistor R674 - 1%
- 1.15K for Docking solutions with analog s/w
- 1.24K for Non-Docking solutions
Place as close to the ASIC as possible
25MHz +-5 ppm 300uW Crystal.
Reserved for EMI.
Logic High Voltage must be 0.7V to 2.75V
LOM_REGSEN12 and LOM_REGSEN25 should be routed using a trace from the load (PNP) back to the controller. Do not use a direct connection to the power plane.Use 8 mils trace width for these signals.
Place high-frequency decoupling caps close to the power pins. Minimize the loop path from pin to cap to power feed via. The length of the path from the ground side of the cap to the ground via should also be minimized.
QUANTA COMPUTER
Title: LAN Broadcom 5755
Size: Document Number: JM7B
Rev: 2A
Date: Thursday, September 14, 2006
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TRANSFORM+RJ45

36nH is a suggested value.
Actual value will be systgem dependent.
Must use 0603 package for lower DC resistance.

40 LOM_TRD0-
40 LOM_TRD0+
40 LOM_TRD1-
40 LOM_TRD1+
40 LOM_TRD2-
40 LOM_TRD2+
40 LOM_TRD3-
40 LOM_TRD3+
L22 L21 L20 L17 L16 L15 L12 L10 0603CS-360EJTS
TRD0N_L TRD0P_L TRD1N_L TRD1P_L TRD2N_L TRD2P_L TRD3N_L TRD3P_L

U3
PI3L500-A
PI3L500-A

40 LOM_ACTLED_YEL#
40 LOM_SPD10LED_GRN#
40 LOM_SPD100LED_ORG#
LOM_ACTLED_YEL#
LOM_SPD10LED_GRN#
LOM_SPD100LED_ORG#

32,43 DOCKED
DOCKED
SEL 0: RJ45.
SEL 1: Dock.

+3.3V_LAN
VDD_1 VDD_2 VDD_3 VDD_4 VDD_5 VDD_6 VDD_7
GND_1 GND_2 GND_3 GND_4 GND_5 GND_6 GND_7 GND_8 GND_9 GND_10 GND_11 GND_12 GND_13 GND_14

NB_LOM_TRD0- NB_LOM_TRD0+ NB_LOM_TRD1- NB_LOM_TRD1+ NB_LOM_TRD2- NB_LOM_TRD2+ NB_LOM_TRD3- NB_LOM_TRD3+
NB_LOM_ACTLED_YEL#
NB_LOM_SPD10LED_GRN#
NB_LOM_SPD100LED_ORG#

DOCK_LOM_TRD0- 43
DOCK_LOM_TRD0+ 43
DOCK_LOM_TRD1- 43
DOCK_LOM_TRD1+ 43
DOCK_LOM_TRD2- 43
DOCK_LOM_TRD2+ 43
DOCK_LOM_TRD3- 43
DOCK_LOM_TRD3+ 43
DOCK_LOM_ACTLED_YEL# 43
DOCK_LOM_SPD10LED_GRN# 43
DOCK_LOM_SPD100LED_ORG# 43

Reserve pull up.
+3.3V_LAN
R347 10K_NC
R348 10K_NC
R349 10K_NC
LOM_ACTLED_YEL#
LOM_SPD10LED_GRN#
LOM_SPD100LED_ORG#

+2.5V_LOM
For Broadcom (5755)
R345 0/0603
L39 BLM18AG601SN1D_NC
0603 package.
NB_LOM_TRCT1 NB_LOM_TRCT2 NB_LOM_TRCT3 NB_LOM_TRCT4

Use 2.5V_LOM for center tap on magnetics when using Broadcom; 1.8V_LOM for Intel only

NB_LOM_TRCT1 NB_LOM_TRCT2 NB_LOM_TRCT3 NB_LOM_TRCT4
C396 0.1U/10V
C397 0.1U/10V
C390 0.1U/10V_NC
C391 0.1U/10V_NC
Reserved for EMI.

+3.3V_LAN
CON2
RJ45 Connector
BLS_L830-1J1C-43
NB_LOM_ACTLED_YEL# R1 150 LED_Y_C
NB_LOM_SPD100LED_ORG# R331 150 LED_O_C
NB_LOM_SPD10LED_GRN# R329 150 LED_G_C
LED_Y_C LED_Y_A
NB_LOM_TRD0+ NB_LOM_TRCT1 NB_LOM_TRD0- TRD1+ TRCT1 TRD1-
NB_LOM_TRD1+ NB_LOM_TRCT2 NB_LOM_TRD1- TRD2+ TRCT2 TRD2-
NB_LOM_TRD2+ NB_LOM_TRCT3 NB_LOM_TRD2- TRD3+ TRCT3 TRD3-
NB_LOM_TRD3+ NB_LOM_TRCT4 NB_LOM_TRD3- TRD4+ TRCT4 TRD4-
LED_O_C LED_G_C LED_O/G_A SHIELD1 SHIELD2

+PWR_SRC +3.3V_ALW +3.3V_LAN
PQ47 SI3456DV-T1-E3
PJP20 POWER_JP
PR187 100K
PR181 100K
PC219 1U/10V
PC218 0.1U/10V
PC220 4.7U/6.3V
72
PQ48A 2N7002DW
PQ48B 2N7002DW
31 AUX_ON
PR186 200K
PR178 470K
PC167 4700P/50V/0603_NC

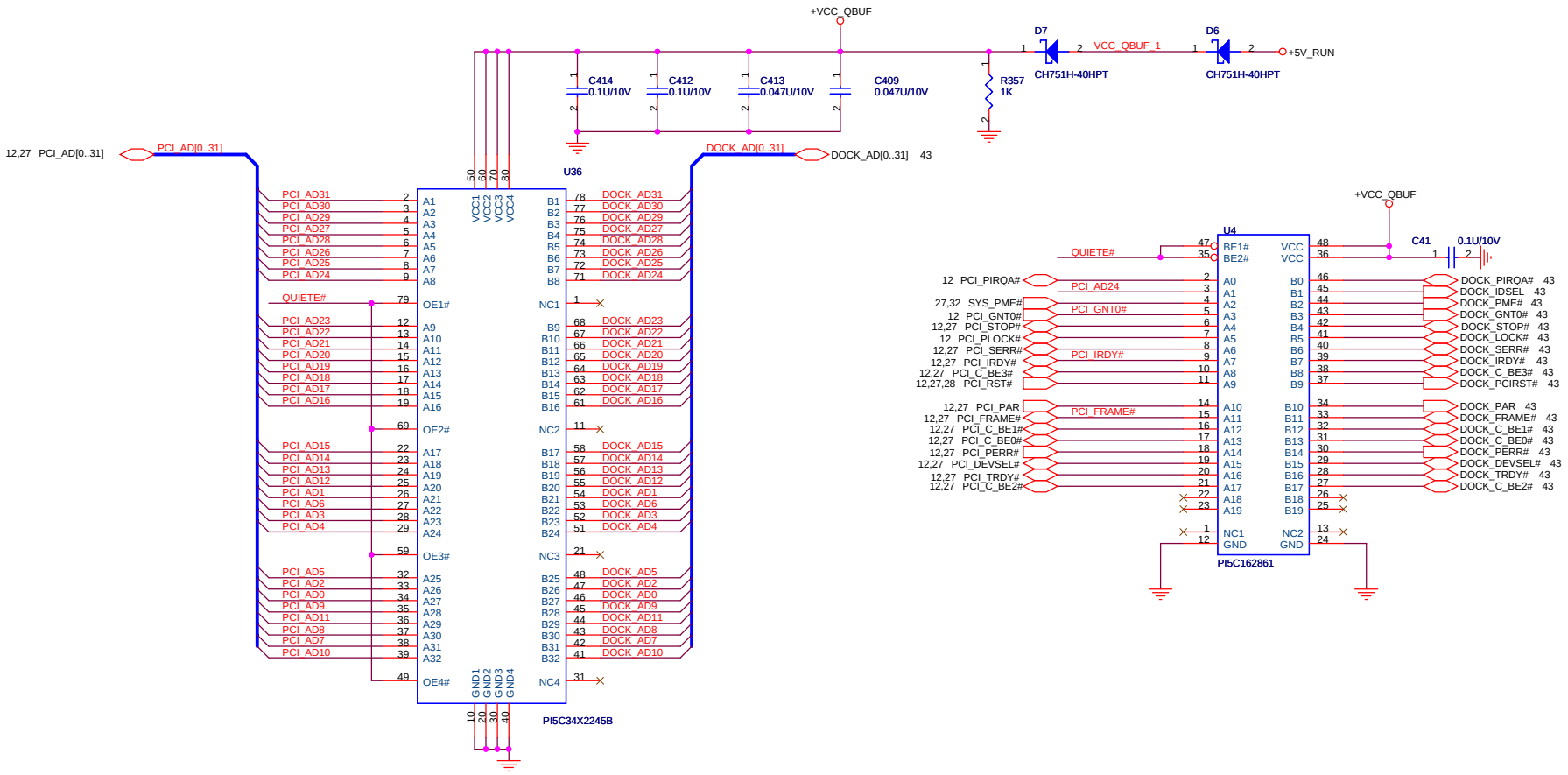
+PWR_SRC +3.3V_ALW +3.3V_WLAN +3.3V_RUN
PQ31 FDC655BN
R270 0/1206_NC
PR78 100K
PR77 100K
PQ28B 2N7002DW
PQ28A 2N7002DW
31 AUX_EN_WOWL
PR79 200K
PR81 470K
PC80 4700P/50V/0603_NC
PR82 100K

	NV_STRAP1	NV_STRAP0	S0	SI	CS#	SCLK
Auto-Sense Mode	0	0	0	0	0	0
ST M45PE20	0	1	1	0	0	1
Atmel AT45BCM021B	0	0	1	0	1	1

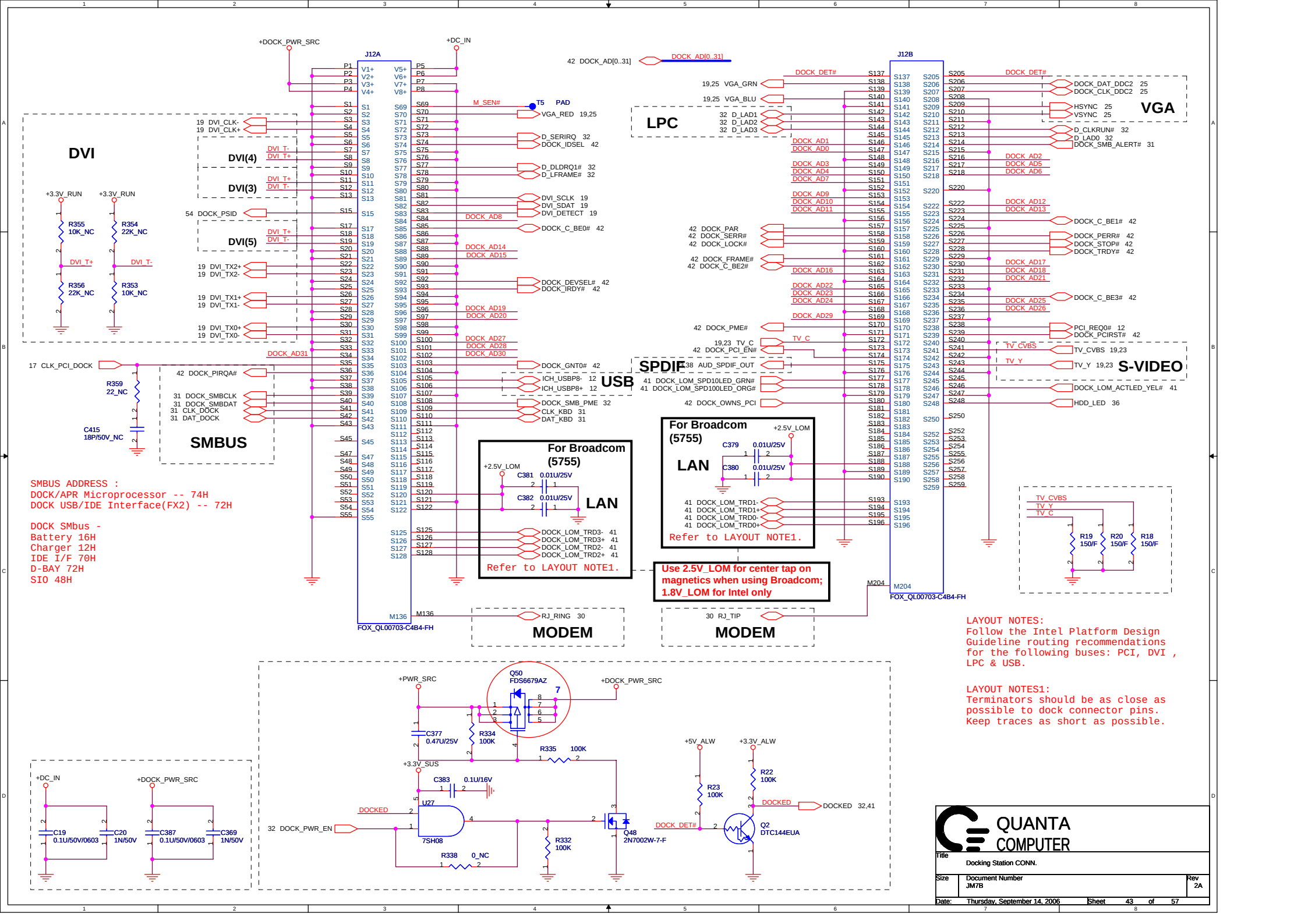
+3.3V_LAN
R13 4.7K_NC
R14 4.7K_NC
R12 4.7K_NC
40 LOM_SCLK
40 LOM_SI
40 LOM_SO
40 LOM_CS#
U24
SCK SO SI CS# VCC WP# RESET# GND
AT45BCM021B
U51
C Q D S# VCC W# RESET# VSS
STM45PE20_NC
37
C1 0.1U/10V

QUANTA COMPUTER

Title	LAN SWITCH	
Size	Document Number JM7B	Rev 2A
Date:	Thursday, September 14, 2006	Sheet 41 of 57



QUANTA COMPUTER		
Title	Docking Q-SWITCH	
Size	Document Number JM7B	Rev 2A
Date: Thursday, September 14, 2006	Sheet 42 of 57	


DVI
DVI(4)
DVI(3)
DVI(5)
SMBUS
USB
LPC
SPDIF
LAN
MODEM
VGA
S-VIDEO
J12A
J12B
FOX_QL00703-C4B4-FH
For Broadcom (5755)
Refer to LAYOUT NOTE1.
Use 2.5V_LOM for center tap on magnetics when using Broadcom; 1.8V_LOM for Intel only
SMBUS ADDRESS :
DOCK/APR Microprocessor -- 74H
DOCK USB/IDE Interface(FX2) -- 72H
DOCK SMbus -
Battery 16H
Charger 12H
IDE I/F 70H
D-BAY 72H
SIO 48H
LAYOUT NOTES:
Follow the Intel Platform Design Guideline routing recommendations for the following buses: PCI, DVI , LPC & USB.
LAYOUT NOTES1:
Terminators should be as close as possible to dock connector pins.
Keep traces as short as possible.
QUANTA COMPUTER
Title
Docking Station CONN.
Size
Document Number
JM7B
Rev
2A
Date:
Thursday, September 14, 2006
Sheet
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of
57

Non-iAMT

Discrete

48 1.25V_RUN_PWRGD — R373 1 2 0

50 GFX_CORE_PWRGD — R159 1 2 0

49 1.5V_RUN_PWRGD — R144 1 2 0
48 1.05V_RUN_PWRGD — R140 1 2 0
37 2.5V_RUN_PWRGD — R138 1 2 0

+5V_RUN
D12 CH751H-40HPT
C176 0.1U/10V
R164 200K
R163 10K
C179 2200P/50V
+5V_ALW
Q20 MMBT3906_NL
R142 4.7K
Q18 MMST3904

+1.8V_RUN
D26 CH751H-40HPT
C601 0.1U/10V
R427 200K
R426 10K
C600 2200P/50V
+1.8V_SUS
Q64 MMBT3906_NL
R141 4.7K
Q19 MMST3904

+3.3V_RUN
D30 CH751H-40HPT
C641 0.1U/10V
R459 200K
R454 10K
C637 2200P/50V
+3.3V_ALW
Q66 MMBT3906_NL
R460 4.7K
Q68 MMST3904

5V_3V_1.8V_1.25V_RUN_PWRGD 32

+1.25V_GFX_PCIe
D10 CH751H-40HPT_NC
C190 0.1U/10V_NC
R155 200K_NC
R154 10K_NC
C165 2200P/50V_NC
+1.25V_RUN
Q23 MMBT3906_NL_NC
R157 4.7K_NC
Q21 MMST3904_NC

Discrete

+3.3V_SUS
D14 CH751H-40HPT
C214 0.1U/10V
R210 200K
R209 10K
C224 2200P/50V
+3.3V_ALW
Q28 MMBT3906_NL
D13 CH751H-40HPT
R194 200K
+3.3V_ALW
C210 0.1U/10V
U14
NC7SZ14P5X_NL

+5V_SUS
D9 CH751H-40HPT
C175 0.1U/10V
R169 200K
R168 10K
C182 2200P/50V
+5V_ALW
Q24 MMBT3906_NL
D11 CH751H-40HPT
R165 200K
R181 200K

39

60

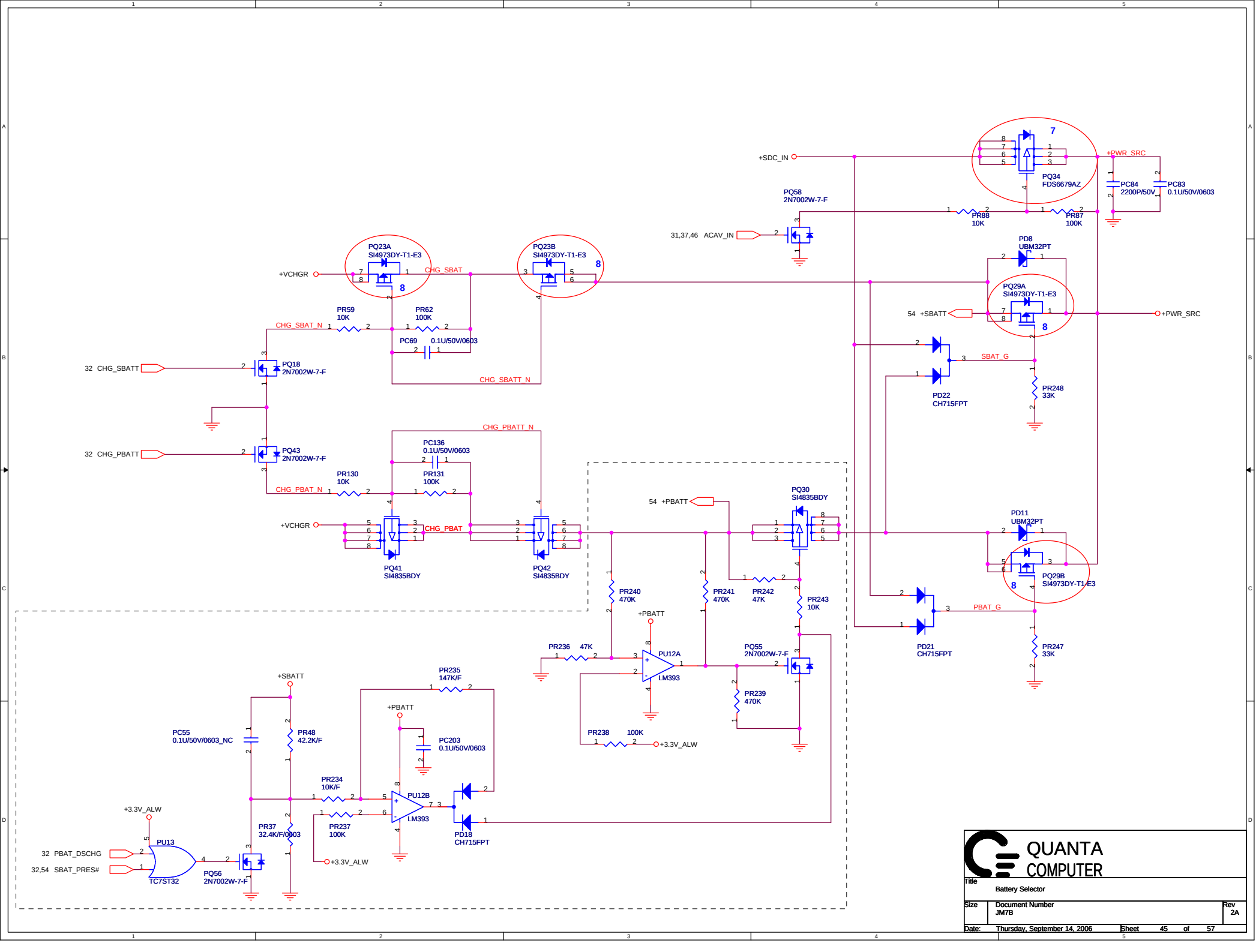
+3.3V_RUN
R182 2.2K_NC
+3.3V_SUS
R462 100K
ICH_PWRGD# 37
Q67 2N7002W-7-F
13,31,51 IMVP_PWRGD
31 RESET_OUT#
U39D
74AHC08PW
ICH_PWRGD 6,13

Keep Away from high speed buses

+3.3V_SUS
R466 20K
C655 0.01U/25V
+3.3V_ALW
C648 0.1U/10V
U40A
NC7WZ14P6X_NL
+3.3V_ALW
U40B
NC7WZ14P6X_NL
+3.3V_ALW
C647 0.1U/10V
U39A
74AHC08PW
R464 0
24,31,33,48,53 RUN_ON
U39B
74AHC08PW
RUNPWROK 19,31,32,51
31,53 SUS_ON
U39C
74AHC08PW
SUSPWROK 37

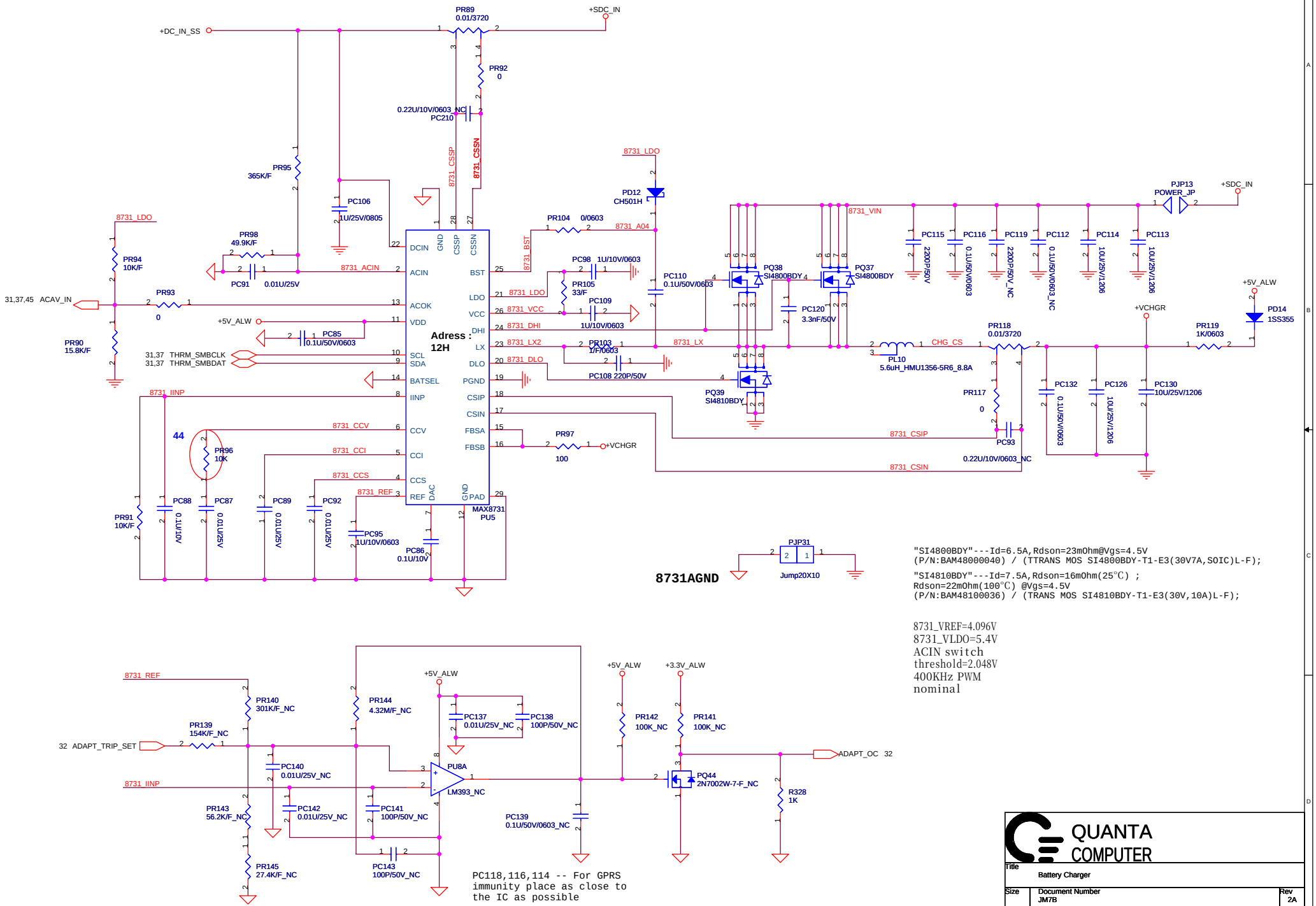
QUANTA COMPUTER

Title	System Reset Circuit	
Size	Document Number JM7B	Rev 2A
Date: Thursday, September 14, 2006	Sheet 44 of 57	



QUANTA COMPUTER

Title	Battery Selector	
Size	Document Number JM7B	Rev 2A
Date: Thursday, September 14, 2006	Sheet 45 of 57	



"SI4800BDY"---Id=6.5A,Rdson=23mOhm@Vgs=4.5V
(P/N:BAM48000040) / (TTRANS MOS SI4800BDY-T1-E3(30V7A,SOIC)L-F);

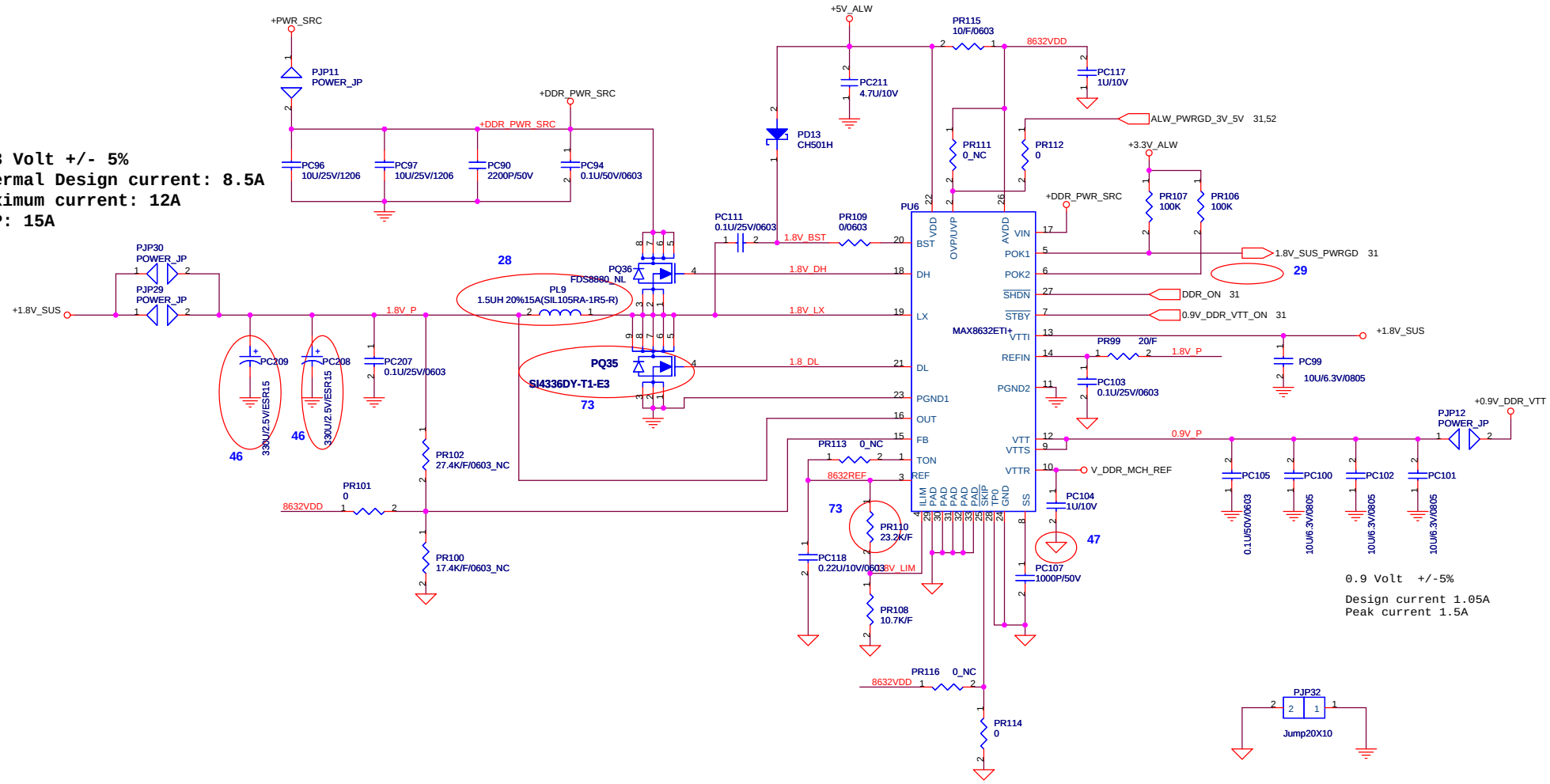
"SI4810BDY"---Id=7.5A,Rdson=16mOhm(25°C) ;
Rdson=22mOhm(100°C) @Vgs=4.5V
(P/N:BAM48100036) / (TRANS MOS SI4810BDY-T1-E3(30V,10A)L-F);

8731_VREF=4.096V
8731_VLDO=5.4V
ACIN switch
threshold=2.048V
400KHz PWM
nominal

PC118,116,114 -- For GPRS immunity place as close to the IC as possible

QUANTA COMPUTER

Title	Battery Charger	
Size	Document Number JM7B	Rev 2A
Date: Thursday, September 14, 2006	Sheet 46 of 57	


1.8 Volt +/- 5%
Thermal Design current: 8.5A
Maximum current: 12A
OCP: 15A
+PWR_SRC
PJP11
POWER_JP
+DDR_PWR_SRC
PC96
10U/25V/1206
PC97
10U/25V/1206
PC90
2200P/50V
PC94
0.1U/50V/0603
+5V_ALW
PC211
4.7U/10V
PD13
CH501H
PR115
10/F/0603
8632VDD
PC117
1U/10V
PR111
0_NC
PR112
0
ALW_PWRGD_3V_5V 31,52
+3.3V_ALW
PR107
100K
PR106
100K
PU6
MAX8632ETI+
VDD
OVP/UVP
AVDD
BST
DH
LX
DL
PGND1
OUT
FB
TON
REF
ILIM
PAD
SKIP
TP0
GND
SS
VIN
POK1
POK2
SHDN
STBY
VTTI
REFIN
PGND2
VTT
VTTS
VTTR
1.8V_SUS_PWRGD 31
DDR_ON 31
0.9V_DDR_VTT_ON 31
+1.8V_SUS
PR99
20/F
PC99
10U/6.3V/0805
PC103
0.1U/25V/0603
+0.9V_DDR_VTT
PJP12
POWER_JP
0.9V_P
V_DDR_MCH_REF
PC104
1U/10V
PC105
0.1U/50V/0603
PC100
10U/6.3V/0805
PC102
10U/6.3V/0805
PC101
10U/6.3V/0805
PC111
0.1U/25V/0603
PR109
0/0603
1.8V_BST
1.8V_DH
1.8V_LX
1.8_DL
PQ36
FDS8880_NL
PQ35
SI4336DY-T1-E3
PL9
1.5UH 20%15A(SIL105RA-1R5-R)
28
73
PJP30
POWER_JP
PJP29
POWER_JP
+1.8V_SUS
1.8V_P
PC209
330U/2.5V/ESR15
PC208
330U/2.5V/ESR15
PC207
0.1U/25V/0603
46
PR102
27.4K/F/0603_NC
PR101
0
PR100
17.4K/F/0603_NC
PR113
0_NC
8632REF
PR110
23.2K/F
PC118
0.22U/10V/0603
8V_LIM
PR108
10.7K/F
PC107
1000P/50V
47
PR116
0_NC
PR114
0
PJP32
Jump20X10
0.9 Volt +/-5%
Design current 1.05A
Peak current 1.5A
QUANTA
COMPUTER
Title
DDR2_1.8VSUS,0.9V
Size
Document Number
JM7B
Rev
2A
Date:
Thursday, September 14, 2006
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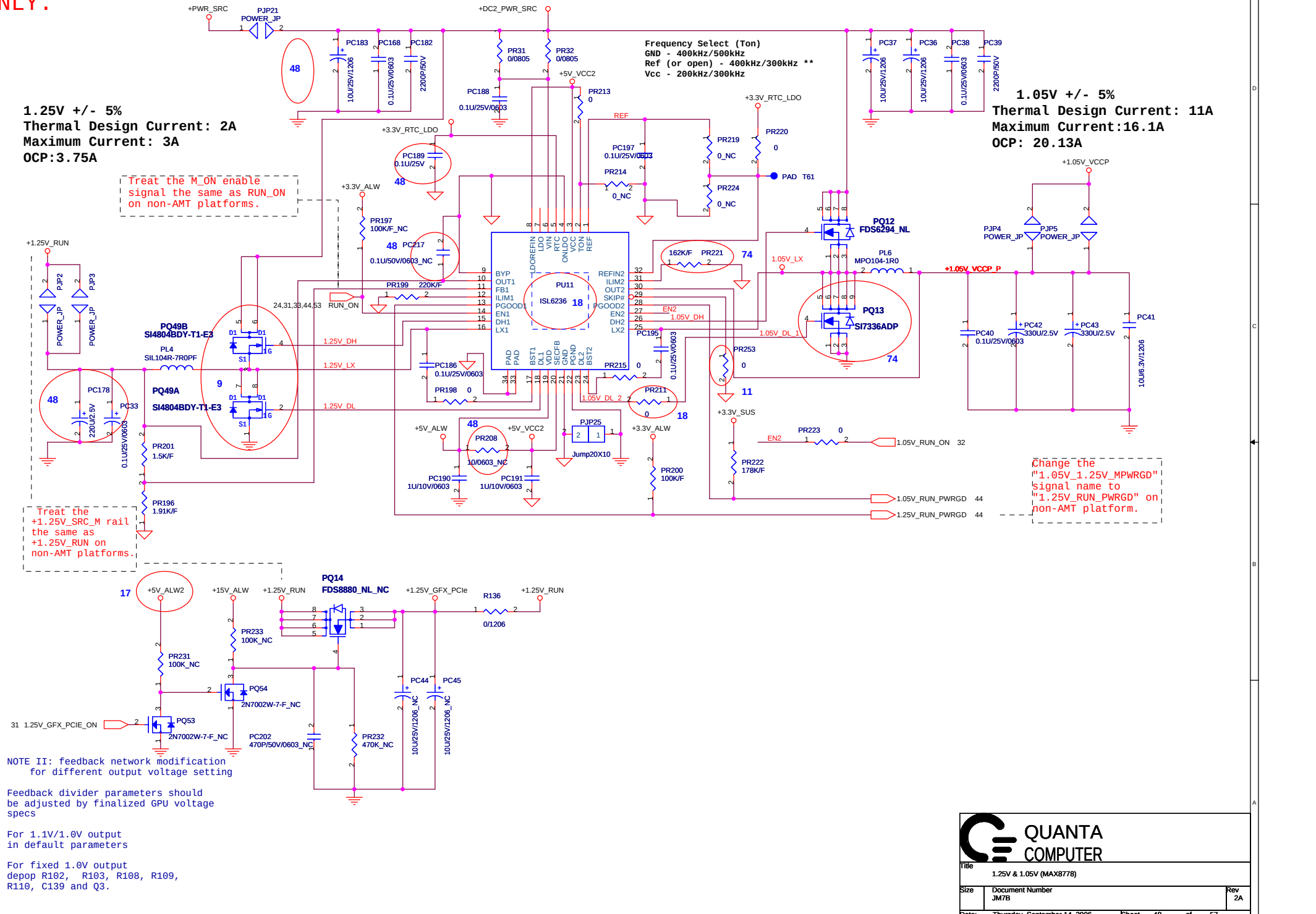
This Reference Schematic to be used for Mainstream Discrete Graphics Down solutions ONLY.



NOTE II: feedback network modification for different output voltage setting

Feedback divider parameters should be adjusted by finalized GPU voltage specs

For 1.1V/1.0V output in default parameters

For fixed 1.0V output depop R102, R103, R108, R109, R110, C139 and Q3.

QUANTA COMPUTER

Title	1.25V & 1.05V (MAX8778)	
Size	Document Number JM7B	Rev 2A
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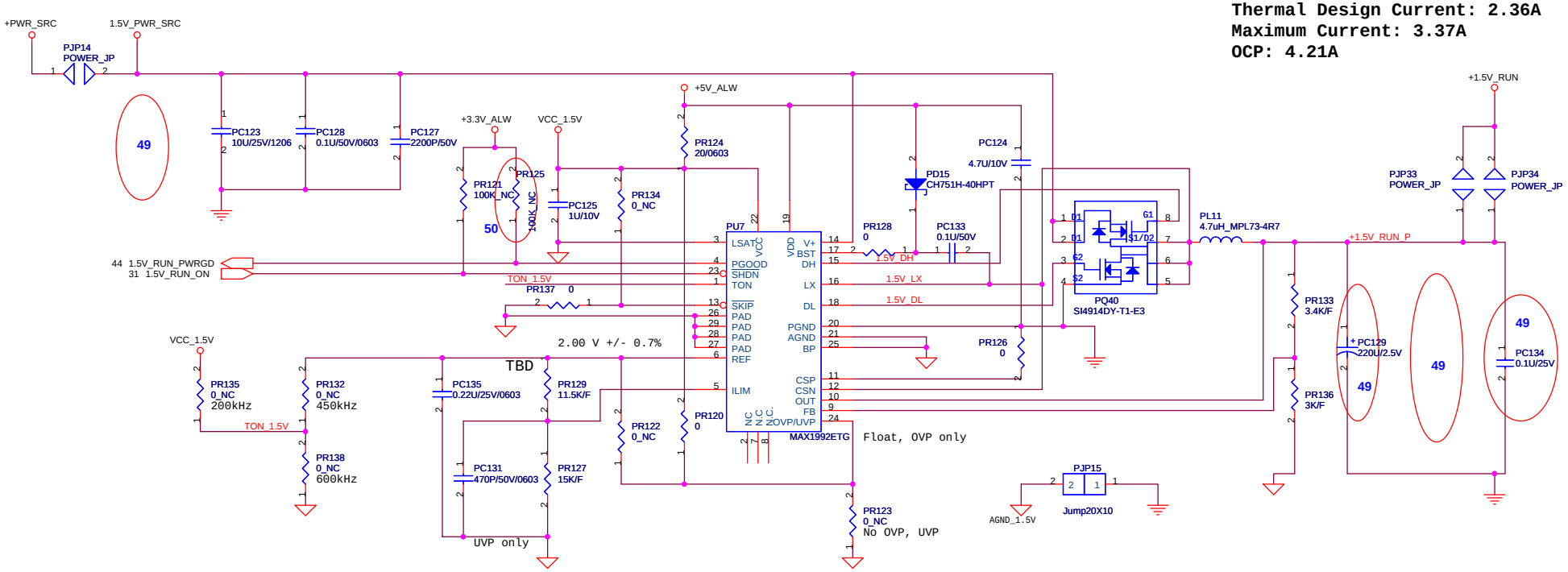
1.5V +/- 5%
Thermal Design Current: 2.36A
Maximum Current: 3.37A
OCP: 4.21A
+PWR_SRC
1.5V_PWR_SRC
PJP14
POWER_JP
49
PC123
10U/25V/1206
PC128
0.1U/50V/0603
PC127
2200P/50V
+3.3V_ALW
VCC_1.5V
+5V_ALW
PR121
100K_NC
PR125
100K_NC
50
PC125
1U/10V
PR134
0_NC
PR124
20/0603
PD15
CH751H-40HPT
PC124
4.7U/10V
PC133
0.1U/50V
PR128
0
1.5V_DH
PU7
LSAT
VCC
PGOOD
SHDN
TON
SKIP
PAD
PAD
PAD
PAD
REF
ILIM
VDD
V+
BST
DH
LX
DL
PGND
AGND
BP
CSP
CSN
OUT
FB
NC
NC
NC
OVP/UVP
MAX1992ETG
1.5V_LX
1.5V_DL
PR126
0
PQ40
SI4914DY-T1-E3
PL11
4.7uH_MPL73-4R7
+1.5V_RUN
PJP33
POWER_JP
PJP34
POWER_JP
+1.5V_RUN_P
44 1.5V_RUN_PWRGD
31 1.5V_RUN_ON
TON_1.5V
PR137
0
2.00 V +/- 0.7%
TBD
PR135
0_NC
200kHz
PR132
0_NC
450kHz
PR138
0_NC
600kHz
PC135
0.22U/25V/0603
PR129
11.5K/F
PC131
470P/50V/0603
PR127
15K/F
UVP only
PR122
0_NC
PR120
0
PR123
0_NC
No OVP, UVP
Float, OVP only
PJP15
Jump20X10
AGND_1.5V
PR133
3.4K/F
PR136
3K/F
PC129
220U/2.5V
PC134
0.1U/25V
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COMPUTER
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1.5V (MAX1992)
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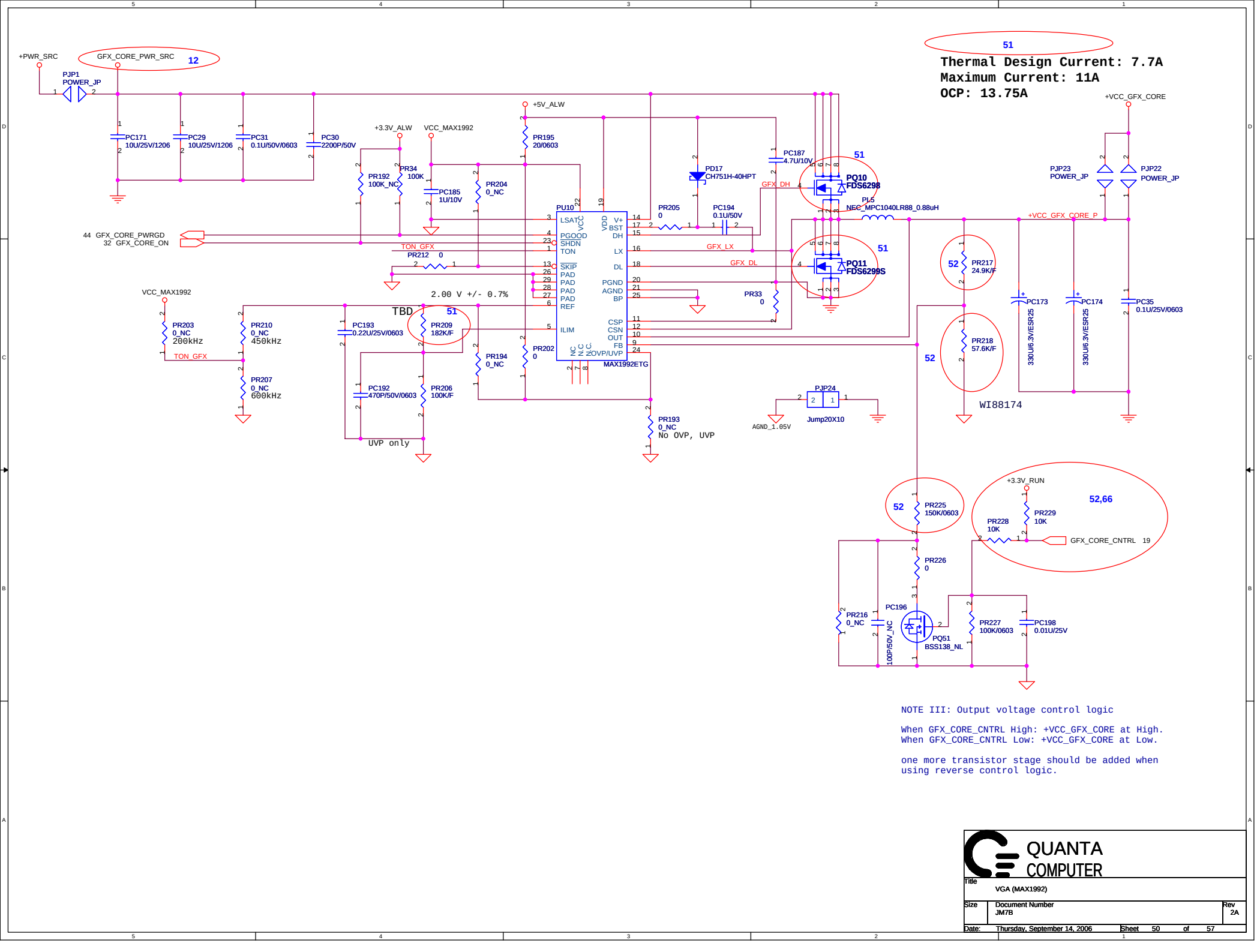
51
Thermal Design Current: 7.7A
Maximum Current: 11A
OCP: 13.75A
+PWR_SRC
GFX_CORE_PWR_SRC
12
PJP1
POWER_JP
PC171
10U/25V/1206
PC29
10U/25V/1206
PC31
0.1U/50V/0603
PC30
2200P/50V
+3.3V_ALW
VCC_MAX1992
+5V_ALW
PR195
20/0603
PR192
100K_NC
PR34
100K
PC185
1U/10V
PR204
0_NC
PD17
CH751H-40HPT
PC187
4.7U/10V
PQ10
FDS6298
GFX_DH
PL5
NEC_MPC1040LR88_0.88uH
+VCC_GFX_CORE
PJP23
POWER_JP
PJP22
POWER_JP
44 GFX_CORE_PWRGD
32 GFX_CORE_ON
PU10
LSATC
PGOOD
SHDN
TON
SKIP
PAD
PAD
PAD
PAD
REF
ILIM
VCC
VDD
V+
BST
DH
LX
DL
PGND
AGND
BP
CSP
CSN
OUT
FB
OVP/UVP
MAX1992ETG
PR205
0
PC194
0.1U/50V
GFX_LX
GFX_DL
PQ11
FDS6299S
PR33
0
TON_GFX
PR212
0
2.00 V +/- 0.7%
TBD
51
PR209
182K/F
PR203
0_NC
200kHz
PR210
0_NC
450kHz
PR207
0_NC
600kHz
PC193
0.22U/25V/0603
PC192
470P/50V/0603
PR206
100K/F
PR194
0_NC
PR202
0
PR193
0_NC
No OVP, UVP
UVP only
PJP24
Jumper20X10
AGND_1.05V
52
PR217
24.9K/F
PR218
57.6K/F
WI88174
PC173
330U/6.3V/ESR25
PC174
330U/6.3V/ESR25
PC35
0.1U/25V/0603
52
PR225
150K/0603
+3.3V_RUN
52,66
PR228
10K
PR229
10K
GFX_CORE_CNTRL 19
PR226
0
PR216
0_NC
PC196
100P/50V_NC
PQ51
BSS138_NL
PR227
100K/0603
PC198
0.01U/25V
NOTE III: Output voltage control logic
When GFX_CORE_CNTRL High: +VCC_GFX_CORE at High.
When GFX_CORE_CNTRL Low: +VCC_GFX_CORE at Low.
one more transistor stage should be added when
using reverse control logic.
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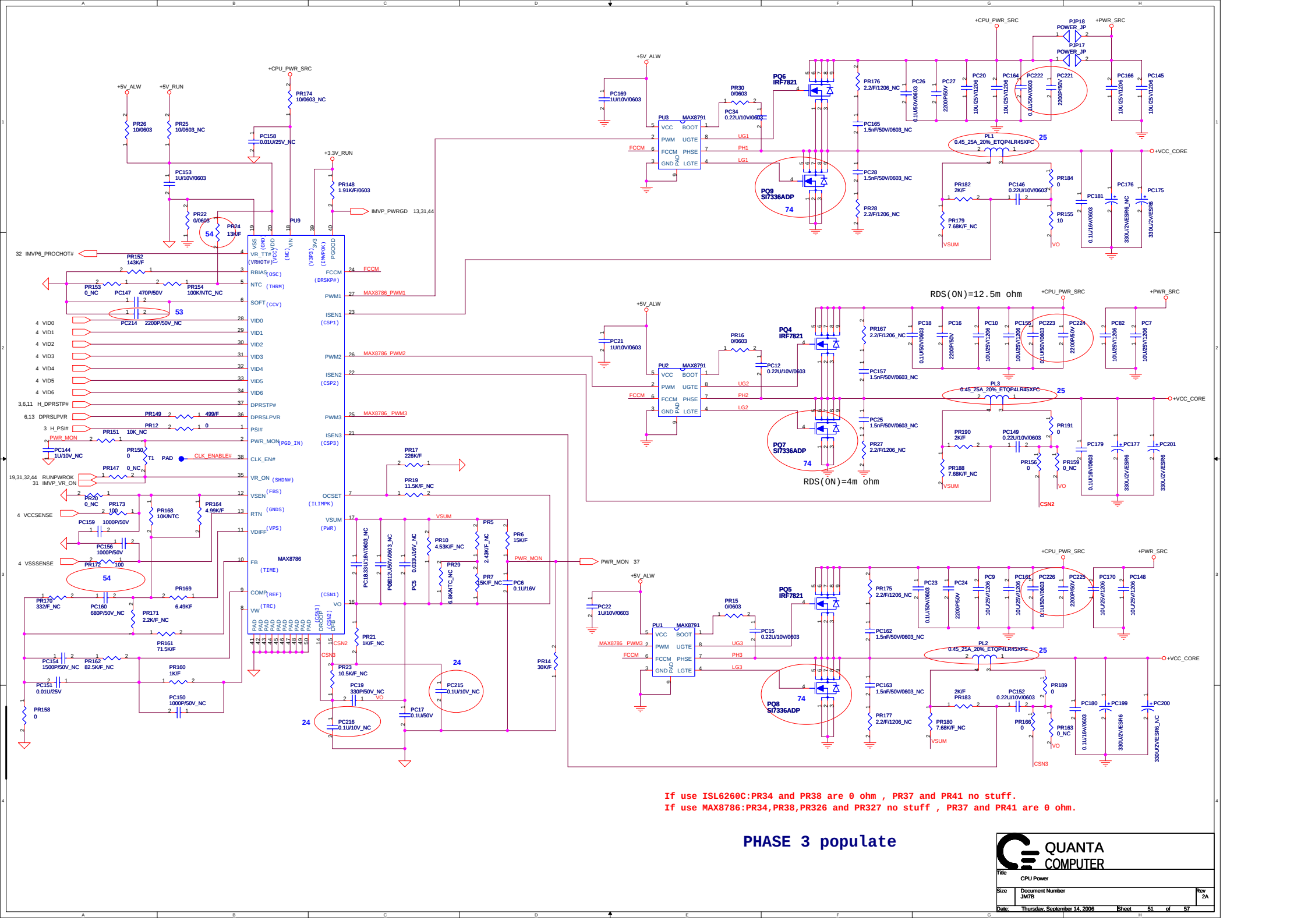
+CPU_PWR_SRC
+5V_ALW
+5V_RUN
+3.3V_RUN
+PWR_SRC
PU9
MAX8786
PU3 MAX8791
PU2 MAX8791
PU1 MAX8791
PQ6 IRF7821
PQ9 SI7336ADP
PQ4 IRF7821
PQ7 SI7336ADP
PQ5 IRF7821
PQ8 SI7336ADP
PJP18 POWER_JP
PJP17 POWER_JP
PL1 0.45_25A_20%_ETQP4LR45XFC
PL3 0.45_25A_20%_ETQP4LR45XFC
PL2 0.45_25A_20%_ETQP4LR45XFC
+VCC_CORE
IMVP_PWRGD 13,31,44
IMVP6_PROCHOT#
VID0
VID1
VID2
VID3
VID4
VID5
VID6
H_DPRSTP#
DPRSLPVR
H_PSI#
PWR_MON
CLK_ENABLE#
RUNPWROK
IMVP_VR_ON
VCCSENSE
VSSSENSE
FCCM
MAX8786_PWM1
MAX8786_PWM2
MAX8786_PWM3
RDS(ON)=12.5m ohm
RDS(ON)=4m ohm
CSN2
CSN3
If use ISL6260C:PR34 and PR38 are 0 ohm , PR37 and PR41 no stuff.
If use MAX8786:PR34,PR38,PR326 and PR327 no stuff , PR37 and PR41 are 0 ohm.
PHASE 3 populate
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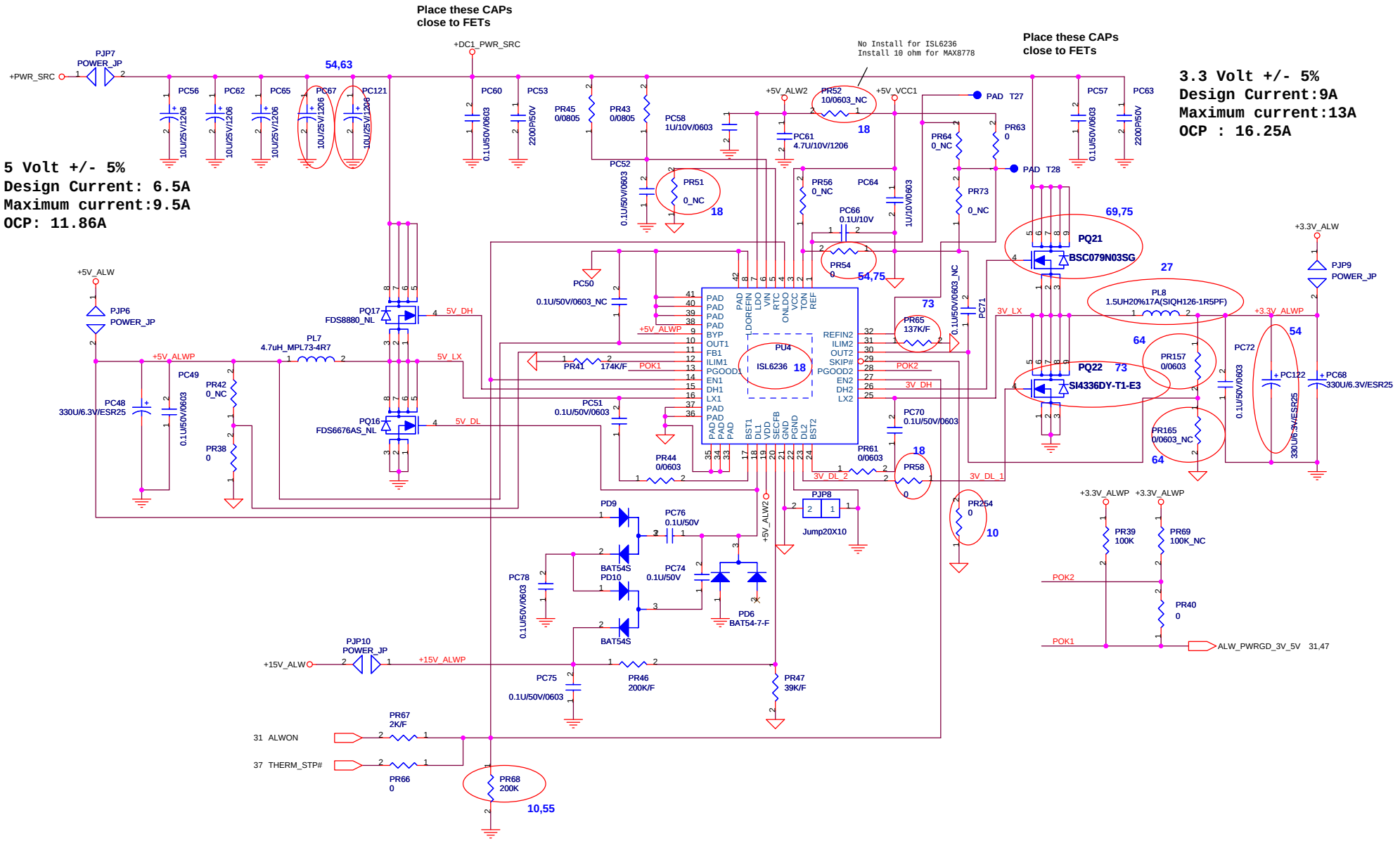
DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+15V_ALW



QUANTA COMPUTER		
Title	3VALW,5V,3V, Power On	
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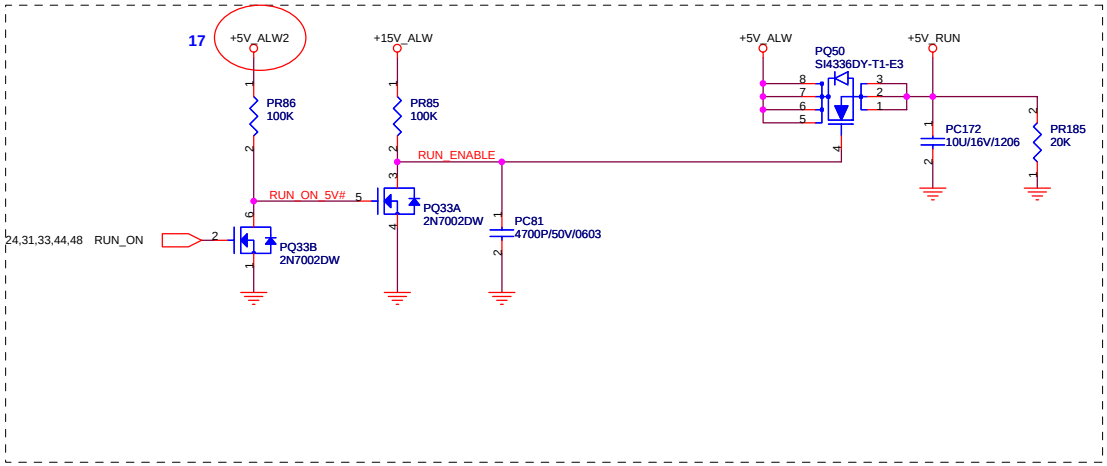

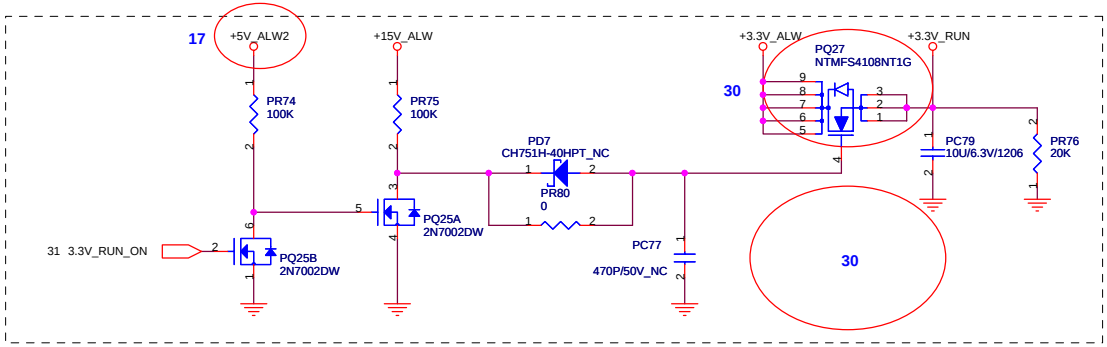

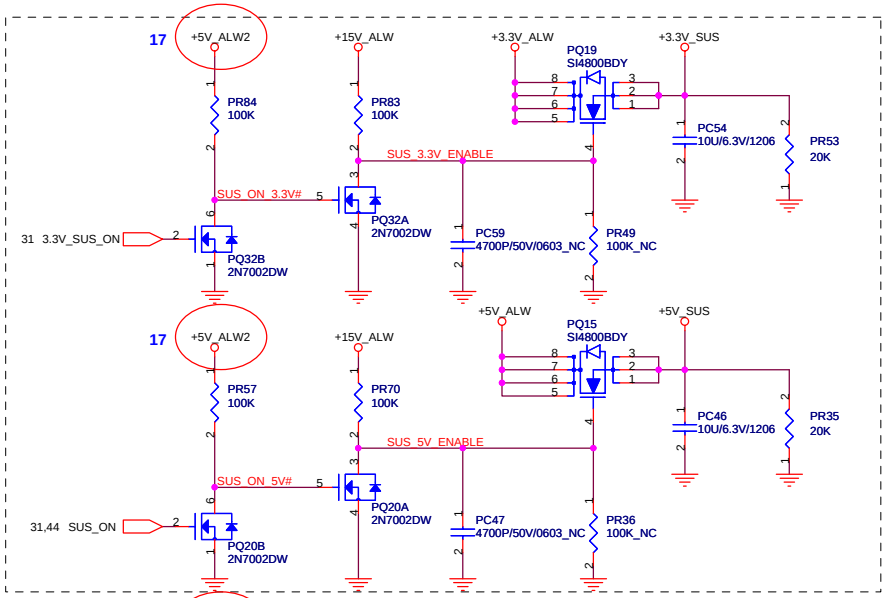

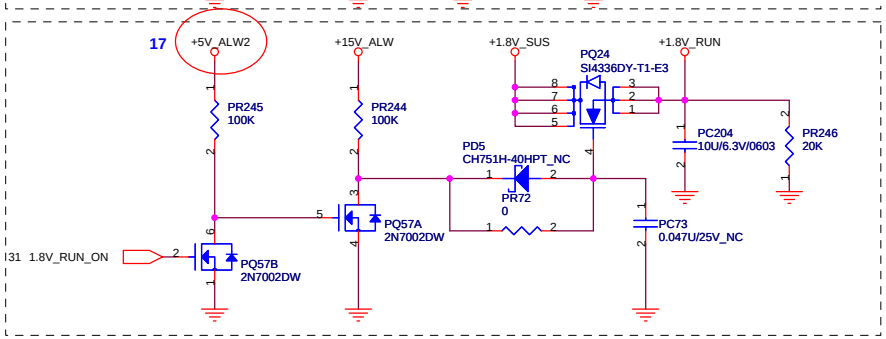

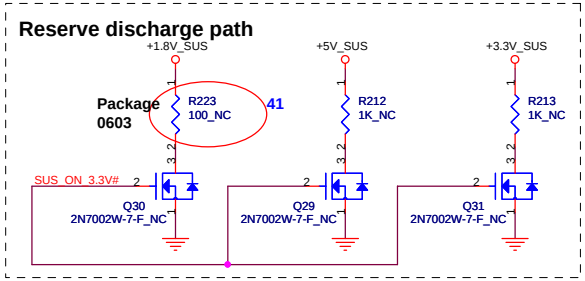

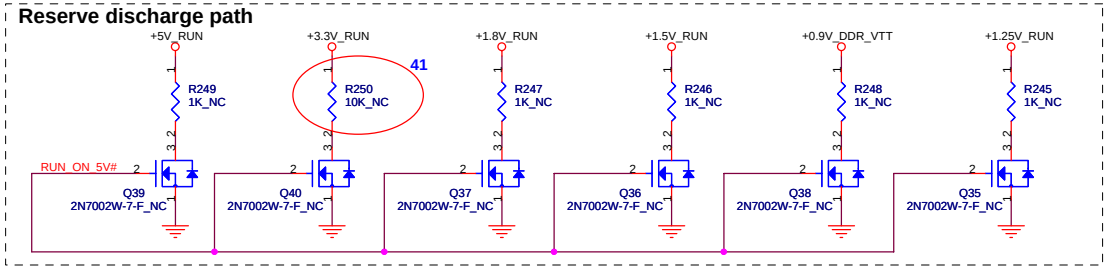

QUANTA COMPUTER

Title	RUN POWER SW	
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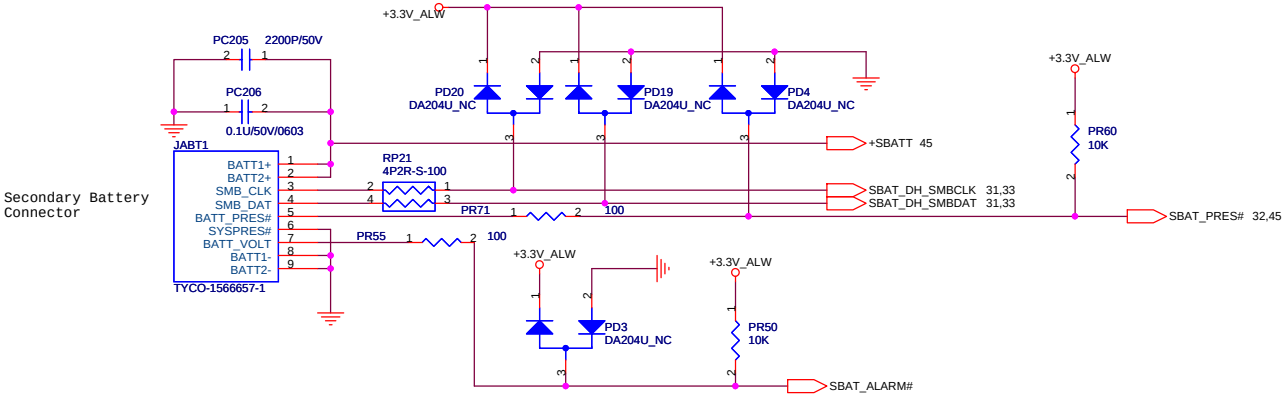
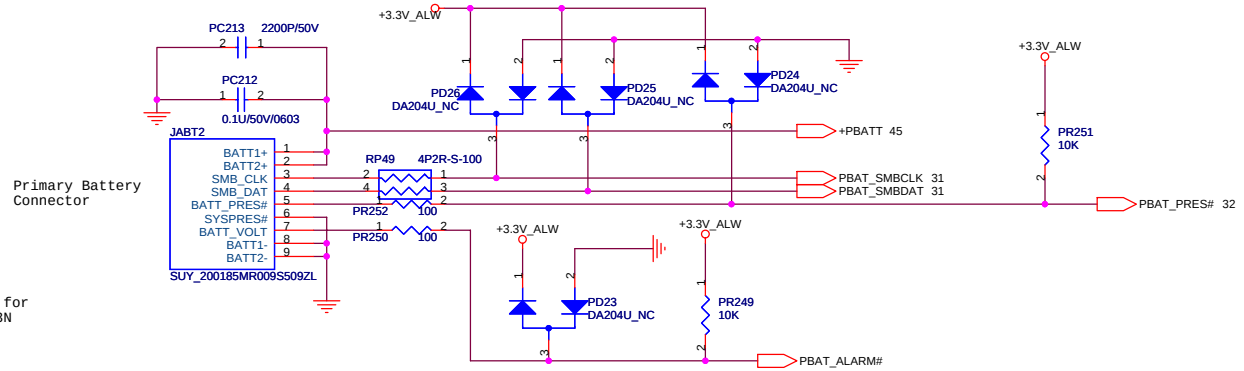


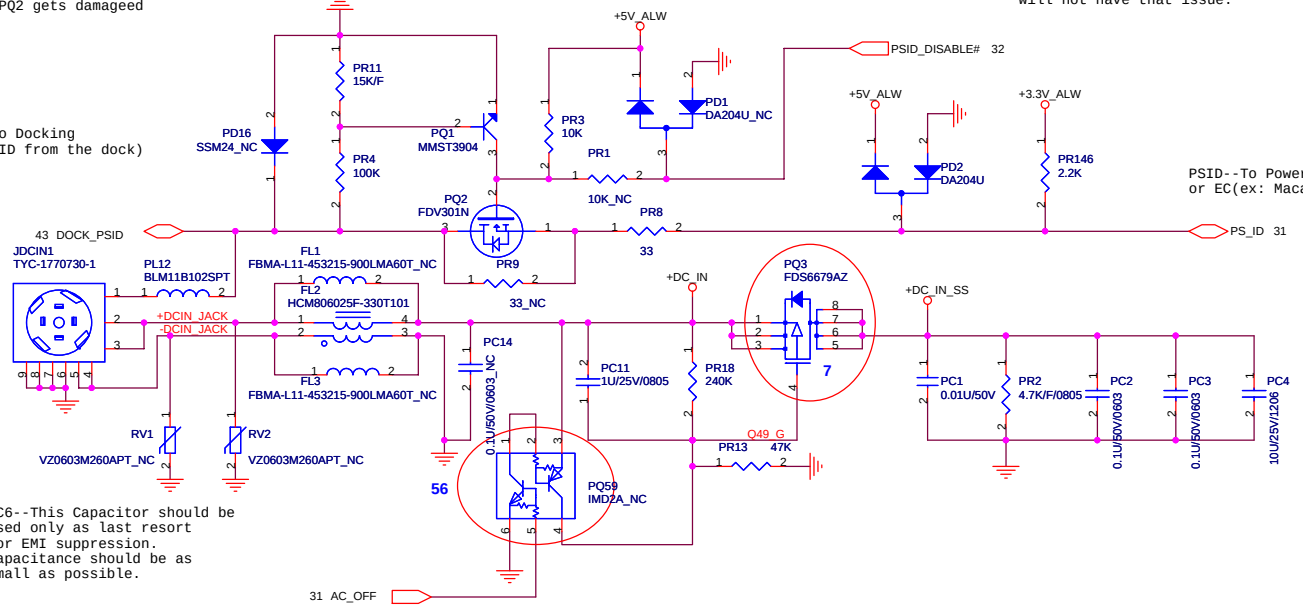


PQ2--Three transistor can be used for PQ2(pin compatible):FDV301N/FDV303N has low Vgs_on w/buit-in ESD protection.MMBT100 BJT works in reverse conduction mode.

D12--This diode is no-stuff populate if PQ2 gets damageed by ESD.

PR1--This resistor must be depopulated if FDV301N/FDV303 are used to avoid a 1.36mA constant current drain from +3VALW. Thus, BIOS will not be to switch Q1 off. MMBT100 will not have that issue.

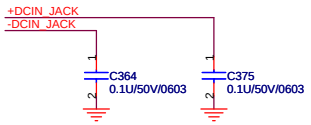
DOCK_PSID--To Docking connector(PSID from the dock)



PSID--To Power Management Controller or EC(ex: Macallan3)

PC6--This Capacitor should be used only as last resort for EMI suppression. Capacitance should be as small as possible.

Reserved for EMI.



QUANTA COMPUTER

Title	DCIN,BATT CONN.	
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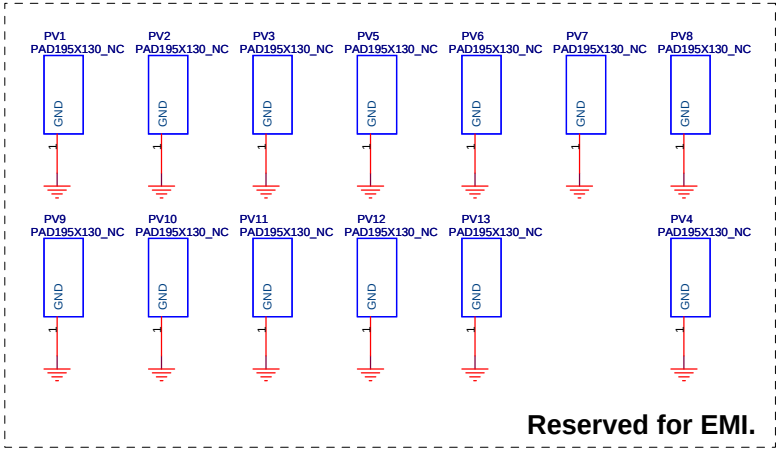

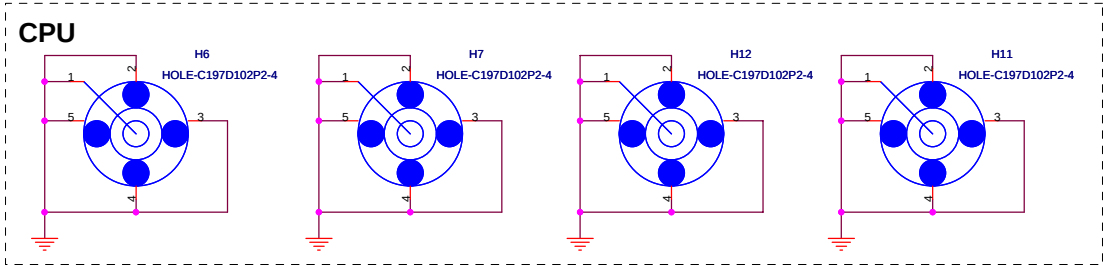

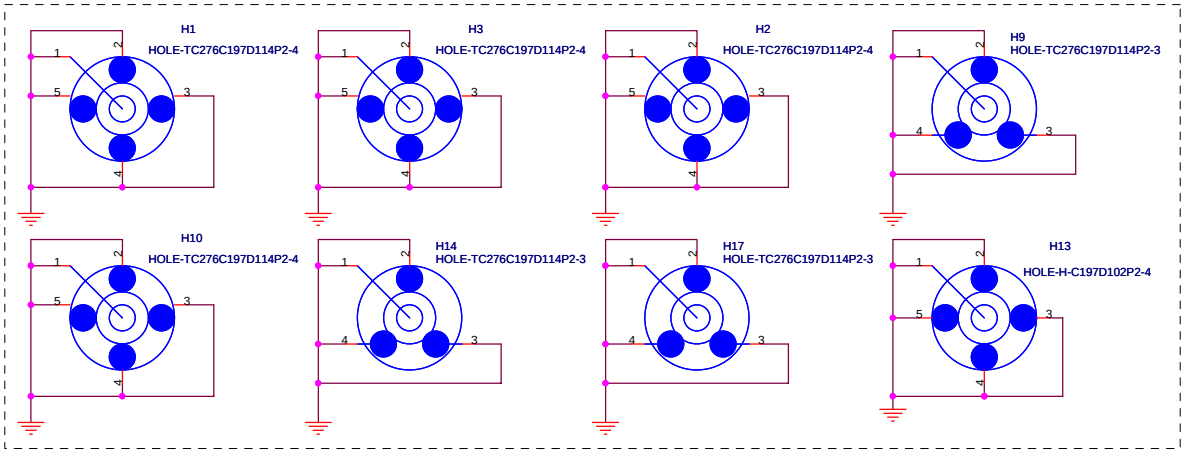

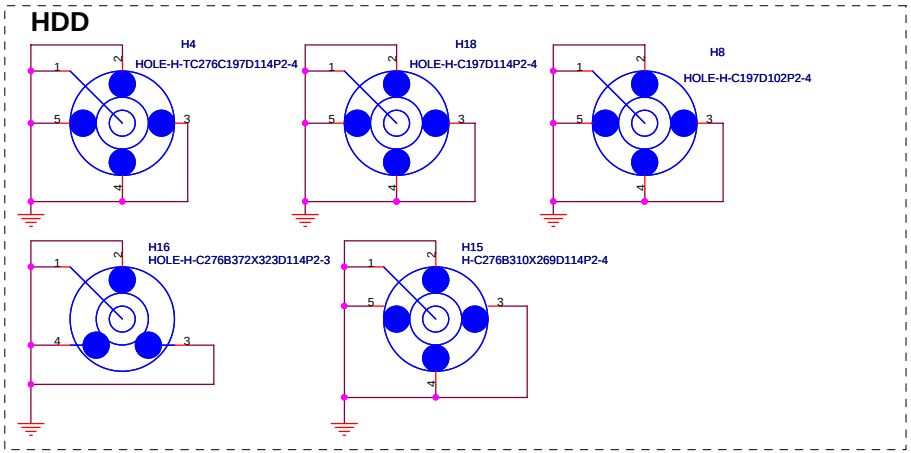

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Title	SCREW PAD	
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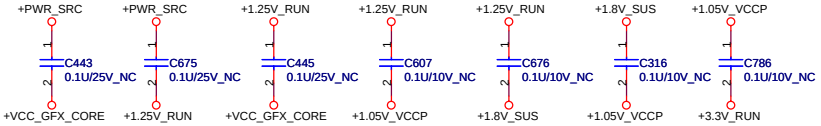
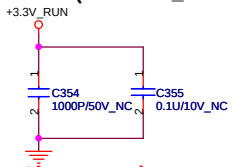
Reserved for EMI.

Stitching caps

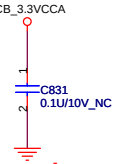


Page 26
SATA (HDD&CD_ROM)



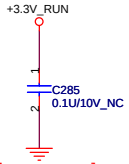
Place caps close
to CON6.

Page 27
PCCARD /CONN



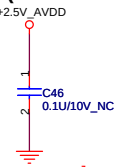
Place cap close
to U47

Page 38
Azelia CODEC



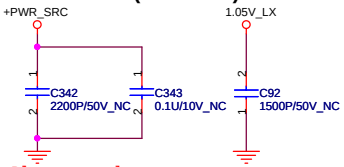
Place cap close
to U21.

Page 40
LAN(BCM5755M)



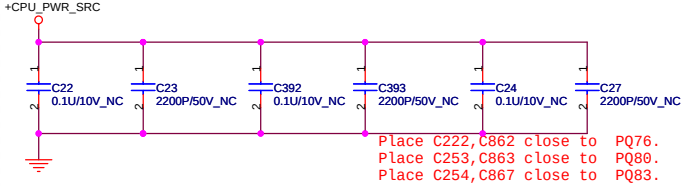
Place cap close
to U58.

Page 48
1.25V & 1.05V(MAX8778)



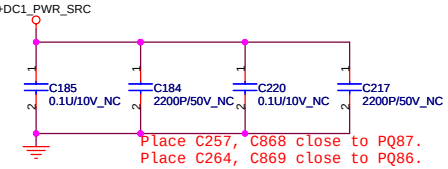
Place cap close
to PQ108.

Page 51
CPU_MAX8786(3phase)



Place C222,C862 close to PQ76.
Place C253,C863 close to PQ80.
Place C254,C867 close to PQ83.

Page 52
D/D Power



Place C257, C868 close to PQ87.
Place C264, C869 close to PQ86.

QUANTA COMPUTER

Title	EMI CAP	
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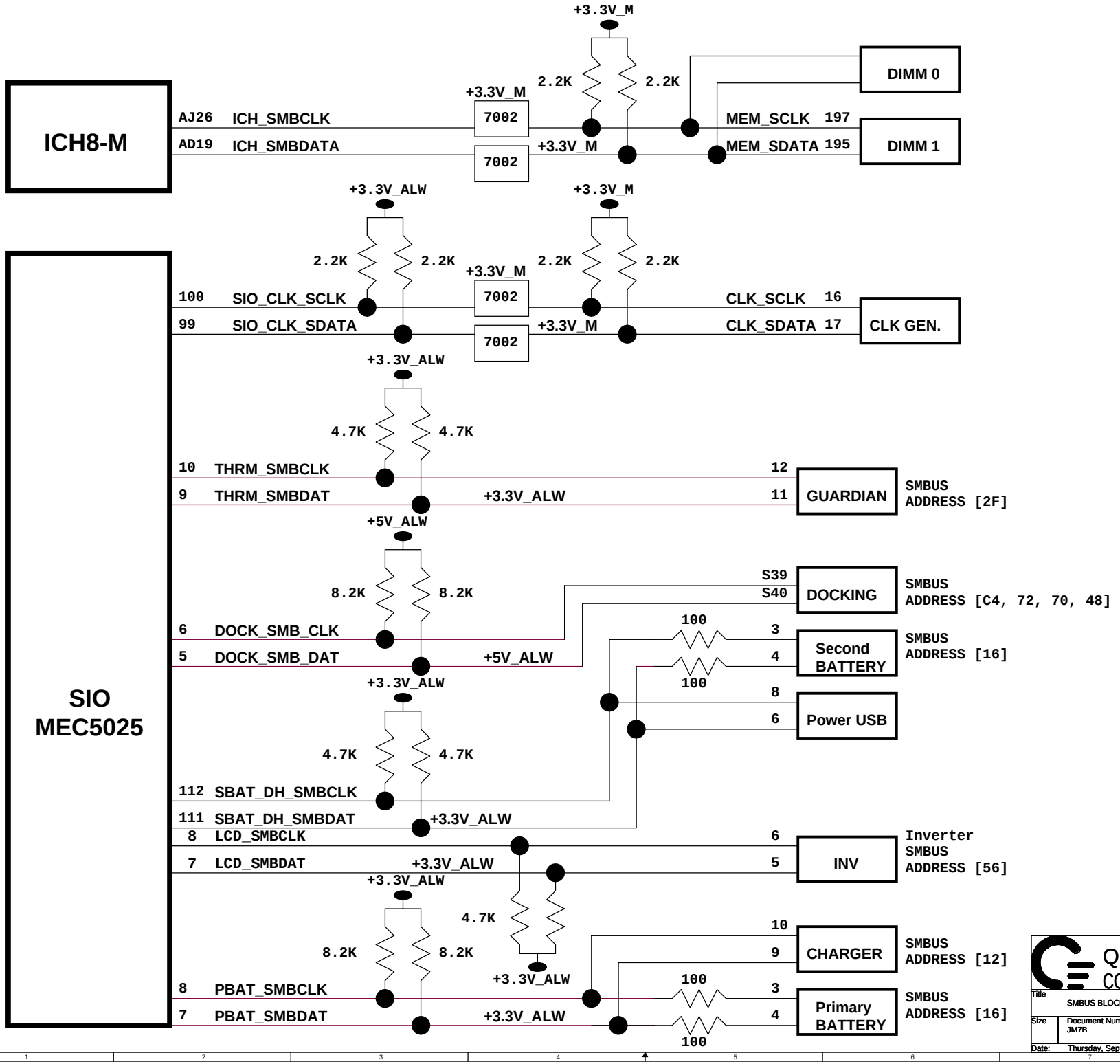

Title	SMBUS BLOCK		
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Model	Item	Page	Date	ECN Number	Item Id	Rev.	Issue Description	Solution Description
JM7B	1	13	7/28/2006		WI82177	2A	SIO_EXT_SMI# Pull-up to Wrong Voltage Rail. SIO_EXT_SMI# pull-up is on 3.3V_ALW. This pull-up should be connected to 3.3V_SUS. This should prevent potential back-drive.	Done.
	2	32	8/1/2006		WI83371	2A	Sch X00 - Change Board ID Straps for X01.	Populate R227 and depopulate R228 for Discrete.
	3	12,23,33	8/3/2006		WI83995	2A	Add S-Video in place of single USB port.	Remove single USB port on page 33 and related USB trace on page 12. Add S-Video schematic on page 23.
		1,23	8/4/2006				Disenable SPDIF function for S-Video. Add S-Video block to page 1.	Done.
	4	24	8/4/2006		WI83867	2A	X00 SM Bus EA issue	LCD_SMBCLK and LCD_SMBDAT rise time over spec. 1us.We need to remove C74, C75 for Discrete to meet SM Bus rise time Spec.
	5	24	7/28/2006		N/A	2A	Change MOSFET Q57 due to EOL.	Because Fairchild will change production material we change Q57 from FDC653N_NL to SI3456DV-T1-E3. SI3456DV-T1-E3 have been used by Brewster for second source.
	6	24,33	7/28/2006		N/A	2A	Change MOSFET Q12,Q58 due to EOL.	Because Fairchild will change production material we change Q12,Q58 from FDC658P_NL to FDC658AP.
	7	43,45,54	7/28/2006		N/A	2A	Change MOSFET PQ3,PQ34,Q50 due to EOL.	Because Fairchild will change production material we change PQ3,PQ34,Q50 from FDS6679 to FDS6679AZ.
	8	45	8/4/2006		N/A	2A	Change MOSFET PQ23,PQ29 due to EOL.	Because Fairchild will change production material we change PQ23,PQ29 from FDS4935 to SI4973DY-T1-E3.SI4973DY-T1-E3 have been used by Brewster for second source.
	9	48	8/8/2006		WI84718	2A	1.25V high side fet and low side fet should be overturn.For FDS6982S, the Q1 of the package is optimized for the high-side, and the Q2 is optimized for the low-side.	Modify PQ49 on Discrete.
	10	52	8/8/2006		WI84734	2A	For the ALWON issue ,PR68 on Dis should be change to 0.47uF cap. PC214 instead of PR68.	Done.
	11	48	8/8/2006		WI84737	2A	Pin 29 of MAX8778 should add a resister to GND since MAX8778 has 5V OVP issue on skip mode.Please refer to attachment from MAXIM.If add a 0 ohm resister on pin29 of MAX8778 ,then we can change to ultrasonic mode.	Add PR253 and PR254 on Dis.
	12	50	8/8/2006		WI84745	2A	Since "GFX_PWR_SRC" net name on page 50 the same as page24. Change "GFX_PWR_SRC" net name to "GFX_CORE_PWR_SRC" on page50.	Done.
	13	11,13	8/9/2006		WI81395	2A	All unused GPIs on the ICH8 need to be terminated by a pull-up. Feedback from Intel advises that all unused GPIs on the ICH8 need to be terminated with a 8.2k - 10k ohm resistor pulled up to their corresponding volatage rails.	Add 10K termination resistors R654,R655,R656 to GPIO13,GPIO33,GPIO34 and pull up to +3.3V_SUS on page 11. Add 10K termination resistors R658 for GPIO12;R657 for GPIO27;R660 for GPIO26 ;R661 for GPIO24;R659 for GPIO10 and pull up to +3.3V_SUS on page 13.
		11,13	8/16/2006				Add 10k termination resistor to GPIO9 pulled up to +3.3V_SUS on page 13 / Depop R654, R655, R656, R657, R660, R661 since default state of these pins are GPO.	Done.
	14	3	8/10/2006		WI82350	2A	Dawson 3VSUS back drive under S4, S5. After check Dawson (UMA and Discrete) 3VSUS back drive under S4, S5. There are two signal (ITP_DBRESET and SIO_EXT_SMI) need change pull up from 3V_ALW to 3VSUS.These changes need implement into UMA and Discrete both.	Change the power rail of ITP_DBRESET# to +3.3V_SUS for back-drive.SIO_EXT_SMI have been corrected with power rail by WI82177.
	15	31,34	8/10/2006		WI82765	2A	Per SMSC, need to have pull-ups for BC Bus Data lines. 1. Add a 100k ohm pullup to +3.3V_ALW on the BC Bus Data line for the high speed BC Bus (pin 86) of the MEC5025. This is needed if the BC Bus is ever operated slower than the 12MHz that we currently operate at. 2. Add a No Stuffed 100k ohm pullup to +3.3V_ALW on the low speed BC Bus Data line for the low speed BC Bus (pin 39) of the MEC5025. There is an internal pullup in the MEC, but since this BC Bus is mulitplexed with the KBC pins, a pad for this resistor is recommended.	Add pullup R662 on BC_DAT to +3.3V_ALW. Change R526 from 10K to 100K and no stuff.
	16	34	8/16/2006		WI85788	2A	SCH X01 - Dawson/Fila PT build needs to use 2MB flash part. Due to increase in number of payloads the BIOS is carrying, we need to move to a 2MB SPI flash part for the PT builds.	Change U43 from SST25LF080A to SST25VF016B.
	17	48,53	8/16/2006		WI85909	2A	Due to the +15V_ALW rail going high before the +5V_ALW rail, the enable circuit for multiple switched fets needs to change, to prevent unwanted glitches from occurring.	Change pullup rail from +5V_ALW to +5V_ALW2 for the following resistors - PR86, PR74, PR84,PR57,PR245 and PR231.
	18	48,52	8/21/2006		WI85916	2A	Change from MAX8778 to ISL6236.	Change PU11 from MAX8778 to ISL6236, PR211 to 0 ohm on sheet 48. Change PU4 from MAX8778 to ISL6236, PR58 to 0 ohm ;depop PR51;depop PR52 on page 52.
	19	37	8/21/2006		WI86681	2A	Change pull-up rail on 5V_CAL_SIO1# to +3.3V_SUS. Feedback from SMSC has indicated that the pull-up rail on 5V_CAL_SIO1# needs to change from +5V_SUS to +3.3V_SUS.This is necessary because the GPIO on the EMC4001 is 3V tolerant, not 5V.	Pullup is at reference designator R198.

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JM7B	20	39 39	8/21/2006 8/25/2006		WI86348	2A	Change L25 and L26 to BLM18BD601SN1D for Vista audio performance.	Done. Change L25,L26 from BLM18BD331SN1D to BLM18BD601SN1D.
	21	38	8/21/2006		WI86347	2A	Recent audio performance tests show that the original 1.0uF has marginal passing results. 2.2uF needed to ensure audio performance requirements are met.	Change C751 and C768 to 2.2uF for Vista performance requirements.
	22	38	8/21/2006		WI86342	2A	Depop C309. This may not be needed in light of C253 and C320.	Done.
	23	38	8/21/2006		WI86335	2A	Change codec package to QFN; U19 needs to change to QFN package. STAC9205X5NBEB1XR.	Done.
	24	51	8/23/2006		WI87472	2A	V_CORE controller should add two caps at "CSN2" and "CSN3" pin.	For MAXIM suggestion and follow MAX8786 spec, add PC215 and PC216.
	25	51	8/23/2006		WI87480	2A	Change v_core choke from "MPC1040LR45" to "ETQP4LR45XFC" since Panasonic(ETQP4LR45XFC) cheaper than NEC-TOKIN(MPC1040LR45).	Change PL1 , PL2 and PL3 to "ETQP4LR45XFC".
	26	31,36	8/25/2006		WI87892	2A	In order to leverage the M07 implementation, the sniffer LED circuit needs to be modified. The MEC5025 pins are being changed from active high to active low.	Change back VC08 design, rename SNIFFER_YELLOW to SNIFFER_YELLOW#, SNIFFER_GREEN to SNIFFER_GREEN# and remove R479 and R480.
	27	52	8/25/2006		WI85389	2A	With a max current of 13A, and calculated ripple of 2.12A, the peak current on PL8 will be 14.06A. The current rating for MPO73-2R2 is marginal at best. Need to choose an inductor with a higher current rating.	Change to 1.5UH20%17A(SIQH126-1R5PF)
	28	47	8/25/2006		WI86712	2A	For a maximum current rating of 12A, the peak inductor current for PL9 will be 13.7A. The MPO104-1R5 part is rated for 20A. Finding an inductor with a lower current rating could possibly lead to a physically smaller and cheaper inductor.	Change to 1.5UH 20%15A(SIL105RA-1R5-R)
	29	31,47	8/25/2006		WI87919	2A	Sch X01: Remove 0.9V_DDR_VTT_PWRGD circuit. The 0.9V_DDR_VTT_PWRGD circuit is not currently being used, and can be removed.	Leave pin 73 of MEC5025 as no connect .
	30	53	8/25/2006		WI88291	2A	Reduce Fets PQ26 and PQ27 into only one Fet. It will be more cheaper. Change PQ27 from "SI4336DY" to "NTMFS4108N". Remove PQ26.	Done.
	31	26,32	8/26/2006		WI88236	2A	Modify HDDC_EN and MODC_EN Circuits to Resolve Glitch Issue. unintentionally for a brief moment.With the current Dawson design, it has been shown that the +15V_ALW rail comes up before the +3V_ALW rail on the original HDDC_EN and MODC_EN circuits. This can cause a momentary glitch at the gate of the power FET, which may cause the FET to turn on unintentionally for a brief moment.	To resolve this issue, please use the HDDC_EN and MODC_EN circuits that are attached below. These new circuits resemble closely our other load switch circuits, but require an additional FET and changes the sense of the HDDC_EN and MODC_EN signals to active high. Please note the use of +5V_ALW2 on these circuits. The +5V_ALW2 voltage comes directly from the LDO output on the 3V/5V switcher in your M08 design.
	32	32	8/26/2006		WI88528 WI88427	2A	SCH X01 - Change ECE5018 to ECE5028. For X01 pilot run, USIO1 needs to change to ECE5028.	Remove R259,R258,C271,C270,C237,C238,C252,R240,R239,Y1,C250,C247, L32,C259,C269,C275. and related stubs for Discrete
	33	11,40	8/28/2006		WI88592	2A	Tune crystal frequency tolerance for 25MHz in LAN and 32.768KHz in ICH.	Change C428 from 27P to 22P for Y2. Change C772,C781 from 15P to 12P for W2.
	34	19	8/28/2006		WI88358	2A	Need to connect thermatrip_vga# to GPIO8 instead of GPIO9.G8x has a new GPIO for our thermal trip output from our internal thermal sensor compared with G7x. So, please connect thermatrip_vga# to GPIO8 instead of GPIO9. It's open collector so it needs a pullup.	Done.
	35	19,20	8/28/2006		WI88367	2A	The HDCP rom needs to be connected to the I2CH_SCL(C7) and I2CH_SDA(B7) and the pullups RP16 need to be removed. Currently these hdcp pins are connected to I2CA.	Connect pin5,6 of U34 from I2CA bus to I2CH bus and remove RP16.
	36	31	8/28/2006		WI88584	2A	Due to the power on defaults of the MEC5025, the pull-downs on the KSI lines of the MEC5025 need to be stronger, to avoid pulses from powering on certain power rails. Please do the following: 1. Change pull-down on SUS_ON to 2.7k 2. Change pull-down on RUN_ON to 2.7k 3. Add 2.7k pull-down to AUX_ON	Change R521,R522 to 2.7K; add pull-up R532 for AUX_ON.
	37	41	8/28/2006		WI88588	2A	U20 (UMA) & U24 (DIS) footprint should be changed to accommodate both wide-body Atmel AT45BCM021B & narrow-body ST-Micro M45PE20.	Add U37 for ST-Micro M45PE20.
	38	29	8/29/2006		WI88810	2A	The 0.1 uF caps can be removed on WLAN (C748) and WWAN (C306). Pin 24 for WWAN should be connected to +3.3V_Run.	Done.

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JM7B	39	12,13 ,31,32, 44	8/29/2006		WI88589	2A	Sch X01: Update GPIOs	1. Swap PS_ID (ECE5018, pin 71) with ITP_DBRESET# (MEC5025, pin 55) 2. Move SB_WLAN_PCIE_RST# from ICH pin F18 to pin G11 3. Move SB_NB_PCIE_RST# from ICH pin C10 to pin F12 4. Move PLTRST_DELAY# MEC5025 pin 69 to ICH pin AF9 5. Move BEEP from ECE5018 pin 78 to MEC5025 pin 69 6. Move SIO_EXT_SCI# from ICH pin AG22 to ICH pin AC19 7. Connect ICH pin AG22 to LOM_SMBALERT#, add a 0-ohm series resistor and depopulate, name the net LOM_ICH_SMBALERT# 8. Disconnect 3.3V_5V_SUS_PWRGD from MEC5025 pin 29 9. Move ALW_PWRGD_3V_5V from MEC5025 pin 18 to pin 29 10. Swap DOCK_SMB_PME# (MEC5025 pin 3) with DOCK_SMB_ALERT# (ECE5018 pin 76)
		31,32	8/30/2006					DOCK_SMB_PME# should be pulled up to +3.3V_ALW DOCK_SMB_ALERT# should be pulled up to +5V_ALW
	40	38	8/29/2006		WI88586	2A	Update GAIN settings / table to reflect MAX9789A production parts.Please update the GAIN settings table on page 38 of the schematics to reflect what is described in the MAX9789A specification. The table that is currently in the schematic is for sample parts, not mass production. In additon, please populate the parts for 15.6dB.	Update GAIN table and populate R296,R549; depopulate R550,R297.
	41	53	8/30/2006		WI88965	2A	Dawson/Fila X00 Gerber board shows that resistor R250 on 3.3V reserved discharge path violates Dell derating guideline (9E154 A03). The resistence has to be increased to approriate value to meet the 70% power derating.	Change R250 from 10 ohm to 10K ohm.
			9/1/2006				R223 should be changed to 100 ohm as you did on UMA version and It has to be 0603.	Change R223 from 33 ohm to 100 ohm package 0603.
	42	36	8/29/2006		WI88815	2A	BJT Q7 should be pulled up to +3.3V_RUN as opposed to +3.3V_WLAN in order to mimic LED behavior on M'07 systems.	Change power rail with Q7 pin1 from +3.3V_WLAN to +3.3V_RUN.
	43	29	8/29/2006		WI88799	2A	Add 2nd 330uF bulk cap for WWAN connected to 3.3V_RUN. This is to help provide enough power for the pulse loads during GPRS operation (max current up to 3A for ~1 ms). Also would help in UMTS modes (more common) where average draw is ~1 A.	Populate 330uF/6.3V to C327.
	44	46	8/29/2006		WI88815	2A	Change PR96 value in charger ckt.Per Maxim's recommendation, change the value of PR108 from 4.7k to 10k.	Change PR96 to 10K ohm.
	45	48	8/29/2006 9/4/2006		WI88444	2A	Cnange value of PC163 on sheet 48.Per Intersil's recommendation, change the value of PC163 from 1uF to 0.1uF.	Change PC163 to 0.1uF/25V.
	46	47	8/29/2006		WI82882	2A	PC209,PC208 to be populated in order to meet output ripple requirements.	Done.
	47	47	8/29/2006		WI86924	2A	PC104 should connect to analog ground.	On sheet 47 of Dawson Discrete, PC104 should connect to analog ground, not power ground.
	48	48	8/29/2006 9/1/2006		WI88468	2A	6 Changes to 1.25V_RUN regulator on sheet 48.	1) Only one 10uF input cap is needed, delete PC184 2) Only one 220uF output cap is needed, delete PC32, and change PC178 from 330uF to 220uF. 3) Change PC33 from 10uF to 0.1uF. 4) Change PC189 from 1uF to 0.1uF. 5) Depop PR208. 6) Add a 0.1uF cap to analog ground from pin 9, BYP.
	49	49	8/29/2006		WI88476	2A	4 Changes to 1.5V_RUN regulator.	1) Only one input cap is needed, delete PC122. 2) PC121 can be deleted 3) PC129 can be changed from 330uF to 220uF 4) Change PC134 from 10uF to 0.1uF.
	50	49	8/29/2006		WI88182	2A	There are two 1.5V_RUN_PWRGD pulled up to 3.3V_ALW on sheet 49 AND to 3.3V_SUS on sheet 44.	Done. PR125 no stuff.
	51	50	8/29/2006 9/8/2006		WI88477	2A	Changes to VCC_GFX_CORE regulator.	1) Delete "1.5V +/- 5%" note at top of page 50. Incorrect. 2) Better FETs will probably need to be chosen. Junction temperatures will reach too high for FDS8880 and FDS6676AS.
	52	50	8/29/2006		WI88174	2A	Proper setting for voltage dividers at +VCC_GFX_CORE.Regulated voltage at +VCC_GFX_CORE should be 1.0 and 1.1V, depending on the state of GFX_CORE_CNTRL. The current values of PR217 (2k), PR218 (3.4k), and PR225 (75k) give calculated output values of 1.11 and 1.13V.	Done. Delete PQ52 ,PR229 and PR230. Chang PR217 to 24.9K , PR218 to 57.6K and PR225 to 150K.
	53	51	8/29/2006 9/1/2006		WI88154	2A	Changes to Vcore circuit.	On sheet 51, Vcore regulator, change PR26 from NC to install (13K). Add a cap, 2.2nF/0402_NC, in parallel with PC127, depopped. Delete PR145.
	54	52	8/29/2006		WI88472	2A	Changes to 3.3V_ALW regulator.	1) Depop PR54 to change switching frequency from 500kHz to 300kHz. 2) 3.3V regulator needs another 10uF input cap to go along with PC65 and PC67. 3) One 330uF output cap will have its ripple rating exceeded, and ESR is too high for 2% output ripple. Add another 330uF in parallel with PC68.

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JM7B	55	52	8/29/2006		WI88163	2A	3V/5V regulator, change enable divider.	On sheet 52, change PC214 back to a 200k resistor. That was the original value. It was changed to a cap to fix a MAX8778 problem, which is no longer used on Dawson/Fila.
	56	54	8/29/2006		WI86725	2A	Change PQ45 and PQ46 in DCIN ckt.	On sheet 54, replace PQ45 and PQ46 with the IMD2A BJT package. The Vgs rating of the Si2301BDS is too low.
	57	32	9/1/2006		WI89654	2A	Update ECE5028 pinout.Per the SMSC ECE5028 v02 spec, the pins 36, 37, 51, and 52 do not change definition from the ECE5018. Please swap pins 36 and 37. In addition, swap pins 51 and 52.	Swap pin36,37 and pin 51,52 and rename pin 58 from BC_INT to BC_INT#.
	58	13 9/2/2006	9/1/2006		WI88948	2A	Intel has advised that the pull-up on LINKALERT# be depopulated and that the pull-up on GPIO14 be 8.2k. Please update.	Change R588 from 10K to 8.2K and no stuff. Depop R593 and Pop R588.
	59	29	9/1/2006		WI88803	2A	Add SMBus isolation circuitry for WLAN.Add isolation circuitry for SMBus on WLAN.	Done.
	60	31,44	9/4/2006 9/5/2006		WI89814	2A	Add ATI_Intel to MEC5025 pin 14 and tie to GND.This connection should be labeled ATI_Intel.	Remove 3.3V_LAN_PWRGD circuit from page 44 Delete 3.3V_LAN_PWRGD from MEC5025 pin 14 Add a connection from the MEC5025 pin 14 and tie to GND.
	61	28	9/4/2006		WI89602	2A	No Connect pin 4 OZ77CR6.Recommendation from O2 Micro is to leave pin 4 of the OZ77CR6 as no connect.	Done.
	62	31	9/4/2006		WI75516	2A	External Work Around Circuit for MEC5025 can be removed.The need for the external work around circuit for the MEC5025 does not exist. Please remove this circuit.	Done.
	63	52	9/4/2006		WI89781	2A	Populate PC67 and PC121 in the 3.3V_ALW regulator. These two caps need to be populated for 3.3V and 5V input ripple requirements.	Done.
	64	52	9/4/2006		WI88782	2A	On sheet 52, add a feedback voltage divider on +3.3V_ALWP.In the current schematic, we are unable to margin test 3.3V. It can only be set to 0-2V and 3.3V.	Add a voltage divider like R26 and R27 in the attached file (connects to +3.3V_ALWP, analog ground, and pin 30). The two resistors should be no-connect.
	65	31	9/6/2006		WI90153	2A	Integrate 0-ohm pull-down resistor on ATI_Intel net. Please integrate a 0-ohm pull-down resistor on ATI_Intel net. This is to have as a place holder to account for any possible issues with the default state of this pin.	Add R502 to GND for ATI_Intel.
	66	50	9/6/2006		WI90252	2A	SCH X01- GFX_CORE_CNTRL requires a pullup. On sheet 50, GFX_CORE_CNTRL requires a 10k pullup to +3V_RUN	Add Pullup PR229 for GFX_CORE_CNTRL.
	67	36	9/7/2006		WI90472	2A	Update WLAN LED implementation.With the current implementation, there is a possibility for backdrive from the WLAN LED control signal to +3.3V_RUN while in S3 / S4 / S5. With the voltage rail being +3.3V_WLAN, there is a high probability that the LED will be illuminated while in S3 / S4 / S5.	Please change the WLAN LED implementation to advice from Dell.
	68	31	9/7/2006		WI90541	2A	Per Broadcom, GPIO0 signal on BCM5755M is an open-drain signal. Hence, needs a stronger pull-up.	Change pull-up on LOM_SMB_ALERT# signal to 4.7K
	69	52	9/8/2006		WI90729	2A	Change switching freq and hi-side FET for +3.3V_ALWP.Change PQ21 to BSC079N03.This FET package will require a layout change.	Change PQ21 to FDS8880_NL.
	70	36	9/9/2006		WI90456	2A	Need to remove RC on WLAN Sniffer circuit.Need to remove R272, R289, C272, and C311 on the sniffer circuit. This RC on those lines is not part of the reference schematic and would just slow those lines down.	Change R272, R289 from 10K to 0 ohm, depopulate C272,C311.
	71	40	9/9/2006		WI90542	2A	Change LOM RDAC & Termination component values to improve IEEE results.some of the test results in the IEEE test suite are marignally passing. Results show variation from system to system (due to component variation, board-to-board impedance variation, etc). Hence, need to make sure of sufficient margins to account for these variations.	Change R48 to 1.13K, 1%. This will allow us to increase amplitude in the 100M & 1G template tests, and to compensate for some of the amplitude loss due to the next change. Change R351, R352, R358, R362, R65, R366, R468, R370 to 2K-ohm, 1% and change C407, C410, C416, C423 to 0.1uF. Populate all for X01. This helps in improving the return loss at the lower frequencies
	72	41	9/11/2006		WI91075	2A	WWAN Noise - LOM Improvement - Additional decoupling on +3.3V_ALW.There's no decoupling on the +3.3V_ALW that sources the +3.3V_LAN and other LOM Voltage rails. The +3.3V_ALW traces across the board (near the edges) and is noisy. Add 4.7uF (0805 pkg), 1uF (0603 pkg) and 0.1uF (0402 pkg) near PQ41 (on UMA) or PQ47 (on DIS) to provide some decoupling on this voltage rail near the LOM.	Add PC218,PC219,PC220 on +3.3V_ALW.
	73	47,52	9/11/2006 9/12/2006		WI91174	2A	FDS7066 will be EOL.Because FDS7066ASN3 will be EOL.	Change PQ35 and PQ22 from FDS7066ASN3 to SI4336DY-T1-E3 and PR110 to 23.2K and PR65 to 137K for setting OCP.
	74	48,51	9/11/2006 9/12/2006		WI91176	2A	FDS7088 will be EOL.Because FDS7088SN3 will be EOL.	Change PQ7,PQ8,PQ9 and PQ13 from FDS7088SN3 to SI7336ADP and change PR221 to 162K for setting OCP.

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JM7B	75	52	9/11/2006 9/12/2006		WI90729	2A	Change switching freq and hi-side FET for +3.3V_ALWP.Intersil has discovered an errata in the controller that produces a problem when using 300kHz at 3.3V. They are still digging into the details, but feel confident they can remove this problem with a silicon change. They have assured us we will not have any problem switching at 500kHz at 3.3V. We will, however, need to provide a better FET package that will perform well at this frequency.	Populate PR54 with zero Ohms to change switching frequency from 300kHz to 500kHz on +3.3V_ALWP. Change PQ21 to BSC079N03. This FET package will require a layout change.
	76	17	9/12/2006		WI90831	2A	LAY X01- WWAN Noise- Clock. Add ferrite bead in series with R492.	Add L64 in series with R441.
	77	12,14	9/12/2006		WI90828	2A	LAY X01- WWAN Noise - ICH improvements. Add one .1 uF cap on each USB OC (over current) trace near the ICH. Add 4 .1uF caps in parallel to C661(UMA)/C813(Disc) close to the ICH pins. Add 4 .1uF caps in parellel to C674(UMA)/C825(Disc) close to the ICH pins.	Add C871~C876 for USB OC. Add C867~C870 in parellel to C813. Add C748,C864~C866 in parellel to C825.
	78	40	9/12/2006		WI90824	2A	WWAN Noise - LOM continued. Try to add one more cap (1 uF) on each analog voltage input to 5755 (1.2V_AVDDL, 1.2V_GPHY_PLLVDD, 1.2V_PCIE_PLLVDD, 1.2V_PCIE_SDSVDD, 2.5V_BIASVDD, 2.5V_XTALVDD, 2.5V_AVDD)	Done.
	79	40	9/12/2006		WI90823	2A	LAY X01- WWAN Noise - LOM improvement. 1) +2.5V_XTALVDD: Change L18 to 0805 package (larger variety of values available in this package size). 2) +2.5V_AVDD: Add one more 0402 capacitor near L14 and U30.F12	1).Change the package of L18 from 0603 to 0805 and use BLM21PG600SN1D instead of BLM18AG601SN1D. 2). Add C168 near L14 and U30.F12

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