SERVICE MANUAL

100 Hz Chassis

28“ CTV

Contents

TECHNICAL DATA

CRT PANEL	
Visible Picture	66 cm
Deflection Angle	110°
Vertical Frequency	100Hz
Horizontal Frequency	31.250Hz

ELECTRONIC

Program Number	100+2AV +SVHS
Teletext	8 pages fast text (Top text optional)
Tuner	PLL
TV System	European CCIR system
Music Power	2x8Watt Rms 10% distortion

CONNECTIONS

Euro AV Socket	Include
SVHS	Include

MAIN STAGE

Mains Voltage	165-260VAC
Mains Frequency	50Hz
Power Consumption	145W
In Stby Mode	2W

RECOMMENDATION FOR SERVICE REPAIRS

1- Use only original spare parts. Only use components with the same specifications for replacement.

2- Original fuse value only should be used.

3- Main leads and connecting leads should be checked for external damage before connection.

Check the insulation.

4- Parts contributing to the safety of the product must not be damaged or obviously unsuitable.

This is valid especially for insulators and insulating parts.

5- Thermally loaded solder pads are to be sucked off and re-soldered.

6- Ensure that the ventilation slots are not obstructed.

7- Potentials as high as 31 KV are present when this receiver is operating. Operation of the receiver outside the cabinet or with back cover removed involve a shock hazard from the receiver.

Servicing should not be attempted by anyone who is not thoroughly familiar with the precautions necessary when working on high voltage equipment.

Perfectly discharge the high potential of the picture tube before handling the tube. The picture tube is highly evacuated and if broken.

Glass fragments will be violently expelled.

Always discharge the picture tube anode to the receiver chassis to keep of the shock hazard before removing the anode cap.

8- Keep wire away from the high voltage or high temperature components.

9- When replacing a wattage resistor in circuit board, keep the resistor 10 mm away from circuit board.

10) Discharging of the picture tube is effected only by the connection point of the aquadaq coating the picture tube.

11) When carrying out repairing process at control unit do not approach too near to the picture tube in order to avoid any charge transfer.

12) Measurements within the primary circuit of the switched mode power supply are allowed to be carried out only when using potential-free measuring equipment. Voltages indicated for this circuit are based on mains voltage reference level.

13) The defined local radiation dosage according to the x-ray radiation regulation is given by the specific type of the picture tube and the maximum permissible EHT voltage. The EHT voltage must not exceed the maximum value of 31kv.

14) When the repair process is carried out 12 V line voltage should not be interrupted because video output stage is endangered by the interruption of 12 V line voltage.

HANDLING OF MOS CHIP COMPONENTS

MOS circuit requires special attention with regard to static charges. Static charges may occur with any highly insulating plastics and can be transferred to persons wearing clothes and shoes made of synthetic materials. Protective circuits on the inputs and outputs of mos circuits give protection to a limited extend only due to time of reaction.

Please observe the following instructions to protect the components against damage from static charges.

1- Keep mos components in conductive package until they are used. Most components must never be stored in styropor materials or plastic magazines.

2- Persons have to rid themselves of electrostatic charges by touching MOS components.

3- Hold the component by the body touching the terminals.

4- Use only grounded instruments for testing and processing purposes.

5- Remove or connect MOS ICs when operating voltage is disconnected.

X-RAY RADIATION PRECAUTION

1- Excessive high voltage can be produce potentially hazardous X-RAY radiation. To avoid such hazard, the high voltage must not be above the specified limit. The value of the high voltage of this receiver is 30KV at zero beam current (minimum brightness) under 220V AC power source. The high voltage must not under any circumstance, exceed 31.5KV. It is recommended the reading of the high voltage be recorded as a part of the service record. It is important to use an accurate and reliable high voltage meter.

2- The primary source of X-RAY radiation in this TV receiver is the picture tube. For continued X-RAY radiation protection, the replacement tube must be exactly the same type tube as specified in the part list.

SOLDERING PROCESS

1) SMD Components (Surface Mounted Device)

Desoldering:

Heat up the component from its terminals for 2 or 3 seconds with a soldering iron and afterwards take out the component carefully by means of the tweezers. Remove superfluous solder at the solder surfaces of the components place at pcb by means of desoldering strand or suction de-solder equipment. Never force the component for removing without heating the terminals sufficiently. Unsoldered components should not be used for once more.

Soldering:

Place the component properly to its position by means of tweezers and solder one side of the component. Then check out the position of the component and be sure if it is soldered to the right place and then solder other side of the component. Terminals of the SMD components must not contact directly to the soldering iron.

2)PLCC Components

Desoldering:

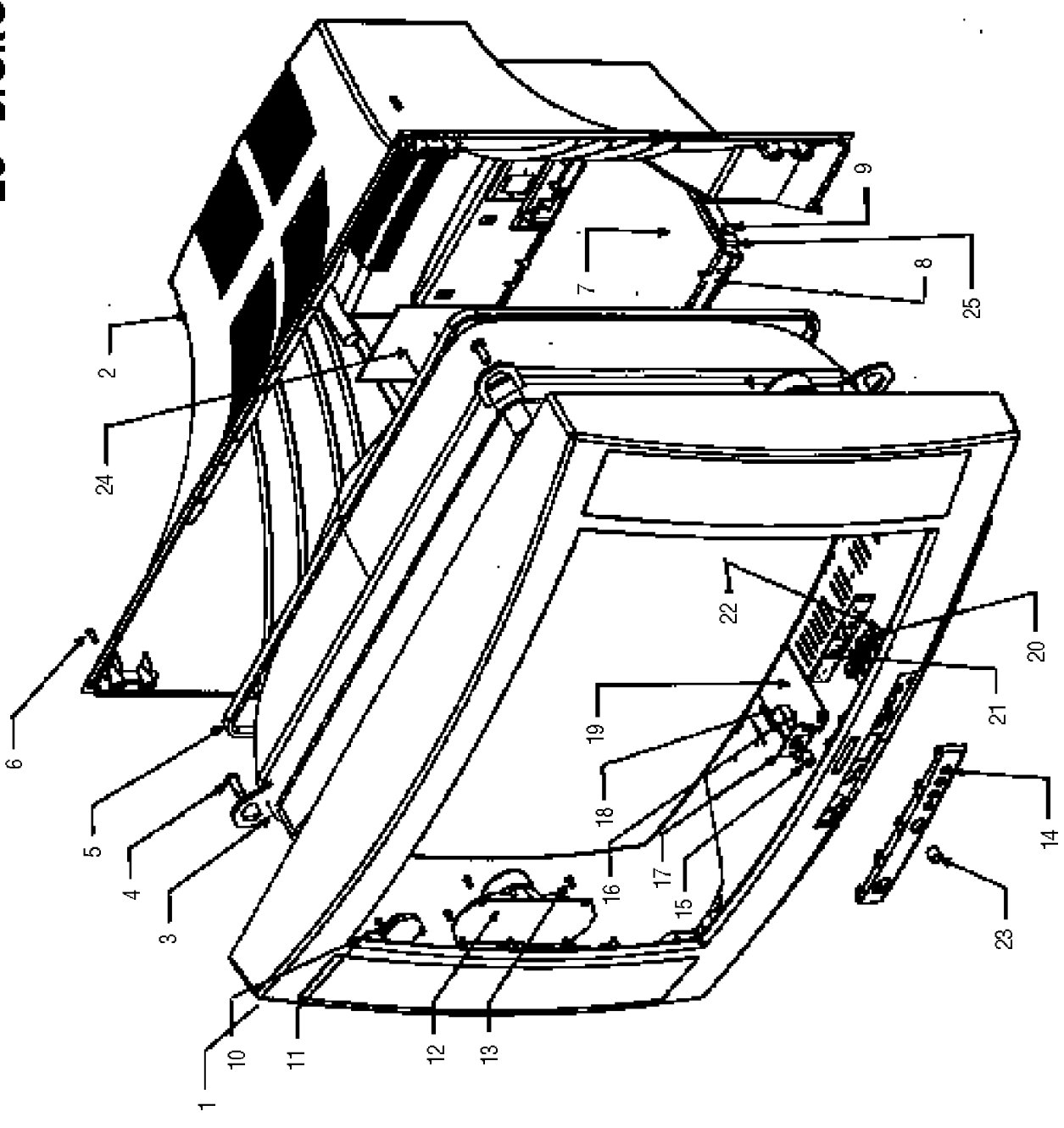
Heat up the terminals of PLCC component for 3 or 5 seconds by means of SMD soldering iron and PLCC desoldering pair (angle 90^{0}C, Leg: 24mm). Take out PLCC component carefully by slightly turning of desoldering tweezers.

Soldering:

Remove superfluous solder at the solder surfaces of the components placed on pcb by means of de-soldering iron or suction de-solder equipment. Apply flux with low grease content. Place PLCC device on the soldering surface and take care for its correct placement. Secure diagonally by means of two soldering joints. Apply soldering paste along PLCC pins. Short circuits which may occure during soldering process have to be removed immediately with a soldering iron.

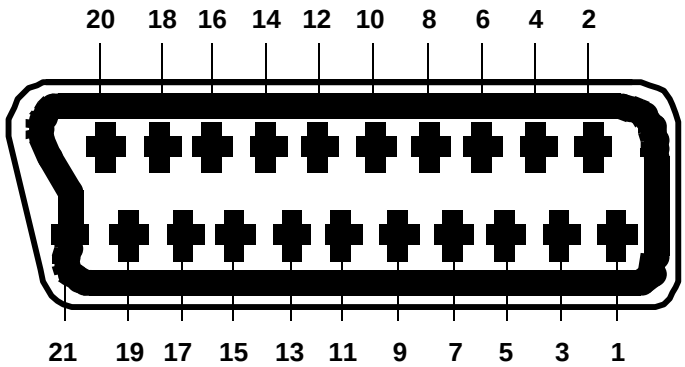
28" BICROMA EXPLODED VIEW

1-9051122800030	28" BICROMA CABINET
2- 9051100280020	IC
9051102800010	SM1 BACKCOVER
3-	28" PICTURE TUBE
4- 015611232070	SCREW CRTØ 7x30
5- 608580004070	DEGAUS COIL
6- 015541819390	SCREW PYSB Ø 3.9x12
7- 614097030211	MAIN CHASSIS
8- 905110002120	STOPER HOLDER LEFT
9051100021110	STOPER HOLDER RIGHT
9- 905110002240	PCB HOLDER LEFT
9051100022250	PCB HOLDER RIGHT
10- 610206610241	TWEETER
11- 015511210290	TWEETER SC.Ø 2.9x9.5
12- 610308128001	SPEAKER
13- 015511210390	SPEAKER SCREW
14- 905113007160	WINDOW
15- 905112000030	ON/OFF BUTTON
16- 001000000231	ON/OFF SWITCH
17- 995113007040	ON/OFF HOLDER
18- 015511210290	SCREW Ø 2.9x9.5
19- 614097040251	ON/OFF & H.PHONE PCB
20- 905118142180	MULTIBUTTON
21- 614097000200	KEYBOARD PCB
22- 015511210290	SCREW Ø 2.9x9.5
23- 005210127020	H.PHONE COVER
24- 614097030260	CRT PCB
25- 015511210290	PCB HOLDER SCREW

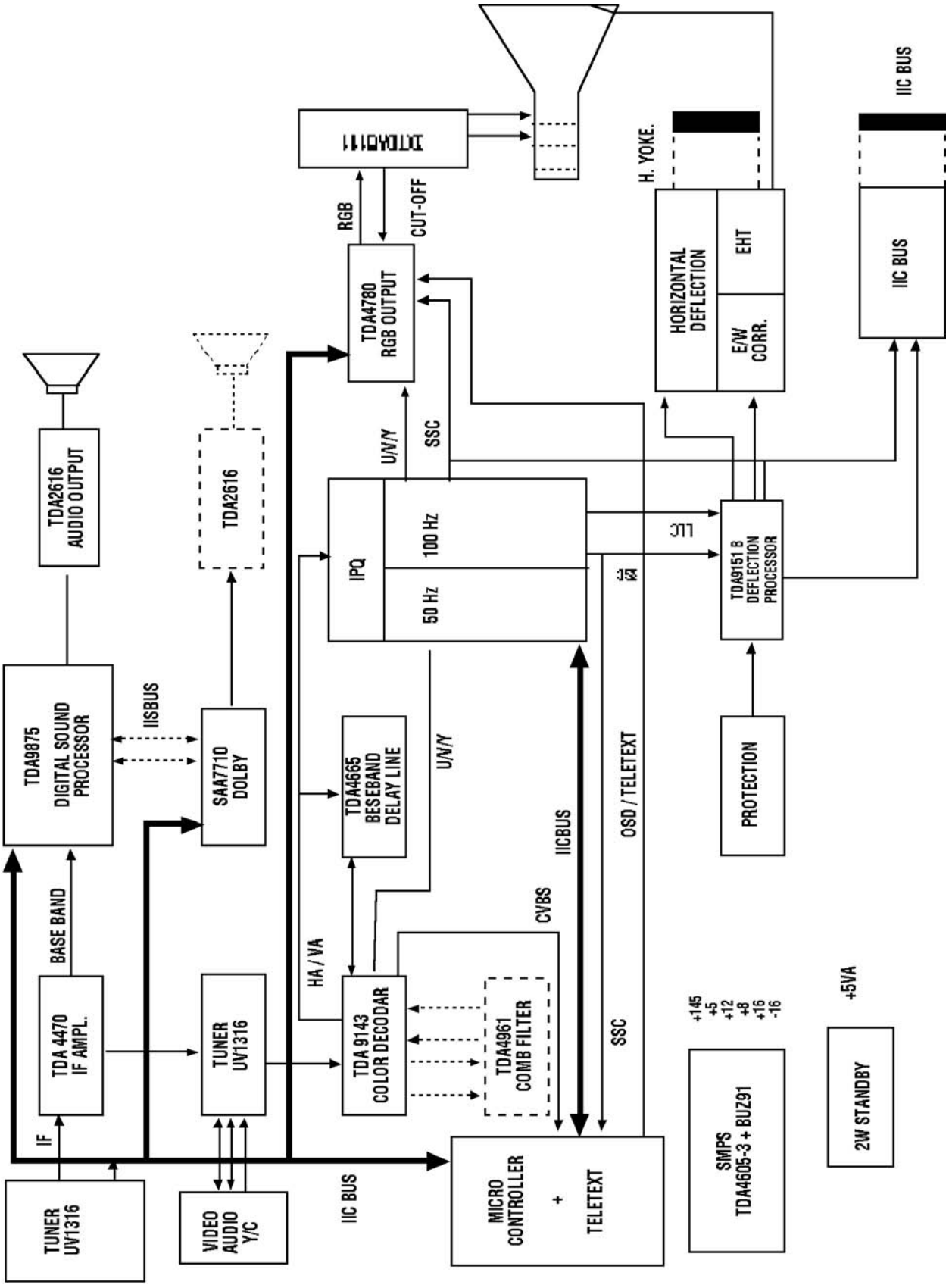


SPECIFICATIONS OF THE CONNECTOR (EURO SCART)

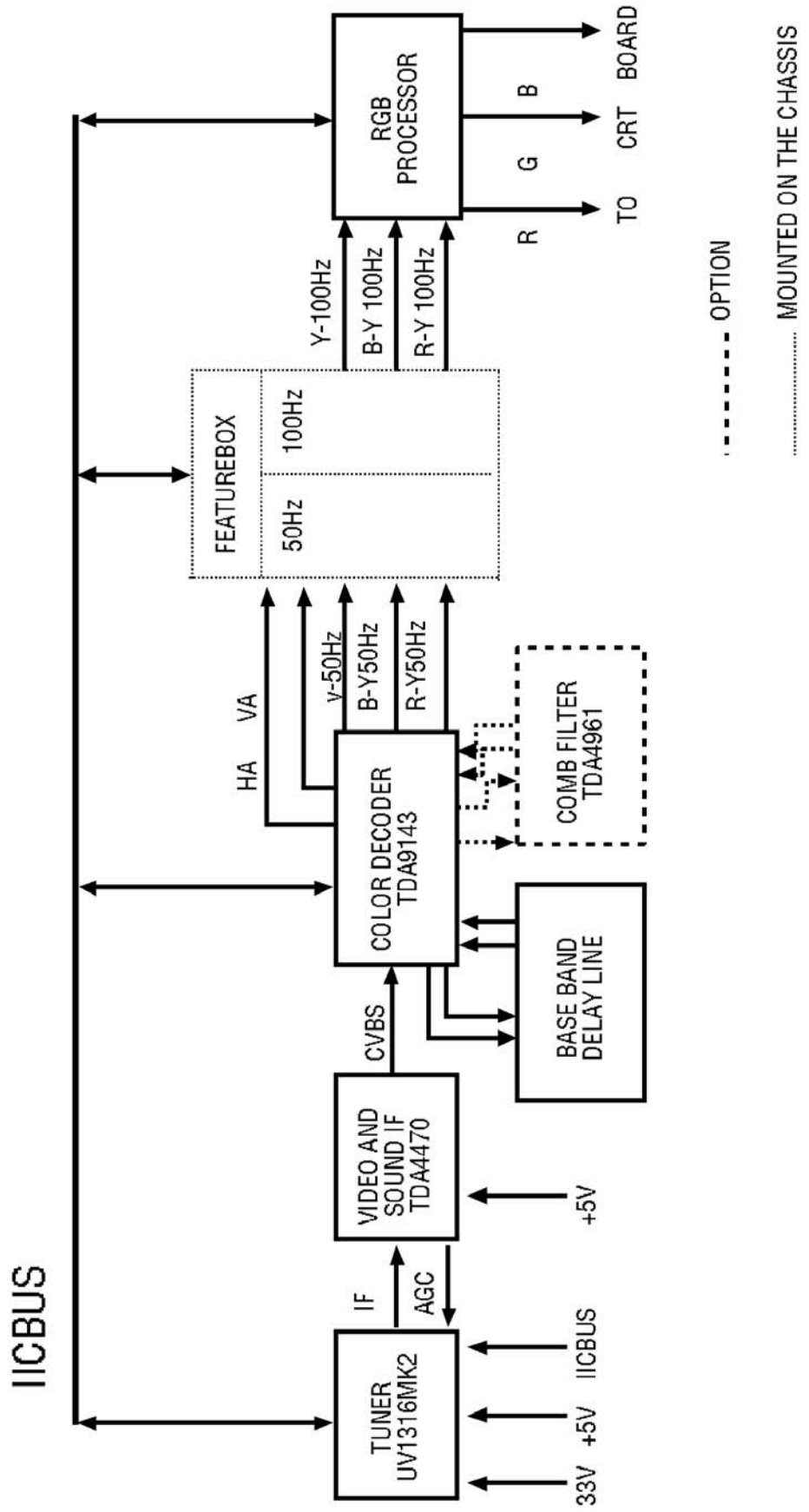
1- Audio output 1. right channel 0.5 VRMS/<1 k 0
2- Audio input 1. right channel 0.5 VRMS (connected to No.6)
3- Audio output 2. left channel 0.5 VRMS (connected to No.1)
4- GND (audio)
5- GND
6- Audio input 2. left channel 0.5 VRMS/>10k 0
7- RGB input, blue (B)
8- Switch signal video (status)
9- GND
10- Reserved for clock signals (not connected)
11- RGB input, green (G)
12- Reserved for remote control (not connected)
13- GND
14- GND switch signal RGB
15- RGB input, red (R)
16- Switch signal RGB
17- GND (video)
18- GND
19- Video output 1 Vpp/75 ohm
20- Video input 1 Vpp/75 ohm
21- Shield



BLOCK DIAGRAM



VIDEO BOARD


IICBUS
TUNER UV1316MK2
33V
+5V
IICBUS
IF
AGC
VIDEO AND SOUND IF TDA4470
+5V
CVBS
COLOR DECODER TDA9143
BASE BAND DELAY LINE
COMB FILTER TDA4961
HA
VA
V-50Hz
B-Y50Hz
R-Y50Hz
FEATUREBOX
50Hz
100Hz
Y-100Hz
B-Y 100Hz
R-Y 100Hz
RGB PROCESSOR
R
G
B
TO CRT BOARD
OPTION
MOUNTED ON THE CHASSIS

CIRCUIT DESCRIPTION

1- MAIN SUPPLY UNIT

A-General Description

In order to obtain 2W power at standby mode, two separate circuits are used. One for standby power supply and another for switched-mode power supply.

The standby supply unit consists of a push-pull converter (Q803 and Q804) producing the required 5V operating voltage by full wave rectification. This voltage is stabilised by means of D807 and D808. This voltage runs the µP (SDA 5250) and IR receiver.

When the standby unit is operating, the under-current relay is pulled up and capacitor C806 which acts as a capacitive series resistor becomes parallel to C807 providing an additional current flow.

To assure the EMC this mains voltage is filtered by multiple choking the feed lines. During standby state the main switched-mode power supply and the degaussing coil are fully disabled by under-current relay. Switching back into the operating state is enabled by the starting-up voltage coming from µp (1701).

The main switched-mode power supply unit including a fly back converter controlled by an opto-electronic coupler consists the driving IC TDA 4605-3 and the switching transistor BUZ91. The following operating voltages are delivered by the transformer of the switched-mode power supply after their rectification.

145Vdc : **+B** Line is a direct output voltage.

33VDC : **+F** Delivered from 145vdc

+16Vdc : **+H** Horizontal driver voltage.

+12Vdc : **+I** Derived from **+H** Supply of the CRT board and the protection circuit.

+8Vdc : **+C** Delivered from **+I**. Supply of the deflection processor, switched matrix, RGB decoder etc.

+5Vdc : **+D** (digital 5v). Supply of the digital part of feature box, µP, DSP (digital sound processor) etc.

+5Vdc : **+A** Supply of the analog part of feature box, µP, DSP (digital sound processor) headphone amplifier etc.

B-Pin Descriptions of the TDA4605-3

PIN 1	Control input signal by comparing the control voltage across control winding 7-9 (SMPS) with an internal reference voltage, the width of the output pulse at pin 5 of the secondary load and the existing mains voltage are matched with each other. The control of the SMPS at pin1 achieved as follows: R102 as a part of control voltage driver (R102, R103 and R104) is variably bypassed by means of the transistor resistance of the opto-coupler which depends on the respective horizontal voltage.
PIN2	Terminal for primary current rise simulation, where an RC network is connected. The voltage rise at pin 2 (sawtooth voltage caused by the charging of C106 through R106 and fast discharging through pin 2) simulates the current rise in the primary winding of the SMPS transformer when the transistor is conducting. When the voltage level reaches the level that is derived from the control voltage at pin 1, the output terminal is set to the ground level terminating the conductivity of Q101. The correct definition of the RC network elements will result a maximum power at the overload.
PIN3 :	Primary voltage detector I101, compares the output voltage at pin3 of the TDA4605-3 which is divided by R106 and R107, with an internal reference voltage and disables the SMPS in case of under voltage (mains approx. 150VAc). If this voltage is greater than the threshold value compensation controlled by pin 2 occurs.
PIN4	**:**GND
PIN5	Switching pulse output, provide control pulses for switching of Q101. This pin provides an output of +/-1A.
PIN6	Supply voltage pin. A stable internal reference voltage as well as the switching threshold for the supply voltage detector are derived from the supply voltage. When the system is switched on the current that is needed is supported through R125 by the transformer winding 7-9.
PIN7	Soft start terminal where C104 is connected. The short pulses because of this capacitor will cause the starting-up to be softly.
PIN8	Zero crossing detector-in the transient state voltage causes a positive output pulse to emerge at pin 5 at every zero transition of the feedback voltage (falling edge).

C-Starting Voltage

After switching on the receiver with the mains button, approximately 320V is present on the charging capacitor C109. Through the resistor R125 the supply voltage of I101 (pin 6) rises to 12 V. Also 5 Vstby supply from the standby power the supply stage is present.

D-Power Supply

The power supply for the receiver employs a free-running switched mode power supply stage with a switching frequency of 35KHz at maximum and I90KHz at minimum load and with a maximum power of 200W. For this reason, a Power Field Effect Transistor is required for the high voltage transistor Q101. The I101 is responsible for driving the MOS power transistor Q101 and also for all control and monitoring functions in the power supply. At Standby mode, the switched mode power supply circuit is switched off. The power consumption is approximately 2W. In this mode, only the µp stage and tuning module is fed with +5Vstby from the "standby" power transformer.

E-Operation

At pin 2 of I101, a saw tooth signal is present and this has a lower reversal point at approx. 1,1V and an upper reversal point at 2,2V. This saw tooth signal is compared by a comparator with the input current at pin1. If the saw tooth signal exceeds the level at pin1, the comparator switches off the high voltage transistor Q101. In order to switch on the transistor again, there must be a zero-cross over signal at pin8. This pin is connected to the transformer winding 2/4 to identify the zero cross-over.

F-The Control

If the transformer is overloaded, all voltages reduce. For controlling the voltage drop, diode D101 is used. Like the voltages when the transformer is loaded, also the voltage on diode D101 decreases resulting a decreased input current of I101-(pin 1). In this case the conduction time of the transistor Q101 increases.

As the operating supply for the line output stage effects the line width, it is necessary for the +B voltage (operating supply for the line output stage) to be stable.

Rising in +B causes the voltage of the optocoupler I102 to decrease. The LED in the optocoupler becomes brighter and the internal transistor between pins 4 and 5 becomes less resistive. This causes the voltage of I101-(pin1) to increase and the conducting time of the high voltage transistor compared with the sawtooth on pin 2 shorter. As a result the +B supply reduces.

G-Overcurrent Protection

The Ics (I101) internal circuit monitors the driving pulses of the switching transistor Q101 by means of the voltage the sawtooth signal at pin 2 of I1O1. The saw tooth voltage on I101 -(pin2), supplies the monitoring of the driving pulses to the switching transistor Q101. If too much current flows through the Power-MOS transistor during an over-load of the power supply, the I101 automatically switches the power supply off.

2- CONTROL UNIT:

A-General Description

The infra-red receiver decodes the infra-red bi-phase signals for µP I701, the master processor. Also the IR-processor can switch the power supply on or off.

The master processor is responsible for the control of the whole system of TV receiver. The set-up data and the settings are stored in the EEPROM I703 and the system control programme is stored in the EPROM I702.

The control and command functions are carried out by the 8bit microcontroller SDA5250 co-operating with the EEPROM I703 and EPROM I702.

Since the microcontroller itself does not include a ROM space, the required operating system will be obtained by using an external EPROM I702. External EPROM contains the specific software program which corresponds to the system of the TV set.

The power supply of the microcontroller is realised by the standby power supply unit (50mA). The low active reset pin 28 is kept as low level for at least 10ms by means of trigger circuit Q701 and Q702 when the mains voltage is applied by switching on the TV set. 18 MHz quartz device X701 acts as a clock generator. Q708, Q709, Q710 and Q711 act as a buffer for supporting all of the IIC BUS ICs. Q704, Q705 , Q706 and Q707 are buffer transistors for OSD.

B- Service and Special Functions Using RC (Remote control)

A) When the EPROM I702 is out of work and should be changed, the service technician should order a new EPROM according to the version number which is written on the IC. EPROM includes the system software (BIOS) for TV.

B) When the EEPROM I703 is out of work and should be changed, the service technician should follow the below steps in order to supply the necessary adjustments. Menu including the deflection and colour data can be loaded via remote controller.

"M" button at RC

Move the cursor to " Service" linc with P+/- button

Press "OK" button

*** Enter code number to the line "for authorized dealer----------"

as "089"

The service menu will appear as follows:

↓ ↓ ↓ ↓

Factory Set Values | Geometry | Video | Tuner Parameters

Factory Set Values:

This function provides the user fast programming without using the menus. This function is especially for the production line at the factory.

Move the cursor to this line

Press ↓ OK

TV will automatically switch to the *** line. If the TV is switched off and switch on again it will automatically switch from the Automatic Search Mode. During the production process at the factory setting this function is the last step before the packing of the set, so the user can have the Automatic Program Search very quickly for the very first time.

(See the related section at the User Manual)

Geometry :

This function provides the service technician to adjust the geometry parameters very quickly in any repair process. These parameters and their step ranges are as follows.

H-Shift	: steps:0-63
H-Amplitude	: steps:0-63
S-Correction	: steps:0-63
V-Amplitude	: steps:0-63
V-Shift	: steps:0-7
E/W Amplitude	: steps:0-63
E/W- Shape	: steps:0-63
E/W- Tilt	: steps:0-7

You should store these set values by moving the cursor to the "memorize" line.

Video:

This function provides the operator at the factory or the service technician to adjust the White Balance parameters.

Red Gain	: Red adjustment at max. Beam current
Green Gain	: Green adjustment at max. Beam current
Blue Gain	: Blue adjustment at max. Beam current
Red Level	: Red adjustment at min. Beam current
Green Level	: Green adjustment at min. Beam current
Blue Level	: Blue adjustment at min. Beam current
Peak White	: It is for the screen adjust ment
Grid 2 Adj	: This adjustment is used at the factory during the production.

You should store these set values by moving the cursor to the "memorize" line.

Tuner Parameters : These values are fixed values and should not be changed.

EHT Compensation: 17

AGC Adjust	:This value should be kept as it is, unless the EEPROM is changed. Otherwise it should be adjusted until not having a snowy picture.

C) Feature Box

Feature Box is completely shielded as it is the most important and sensitive part of 100 Hz Chassis. The YUV signals which are for 50Hz are converted to 100Hz signals by means of sampling and scanning twice of each sampled signal. Inside of the feature box there are Analog-to-Digital converter, Clock Synchronisation Generator, Memory Synchronisation Generator, Digital-to-Analog Converter and Sequential Access Memory. The input signals to the Feature Box are Horizontal Sync, Vertical Sync, CVBS and YUV signals, SDA, SCL and LLC as well as 5V supply and ground. Analog YUV signals are converted to the digital signals at ADC by means of the synchronisation pulses from SDA9257 which uses analog CVBS signal for providing the necessary sync pulses. The ADC conversion are processed at SDA9205. SDA9220 is responsible for driving the SDA9254 (TV- Sequential Access Memory) and generating sync signals. Together with the other devices of the Feature Box it enhances picture quality. SDA9254 is a combination of the TV sequential access memory and an adaptive filter which is used to enhance noisy input signals. SDA9280 is a Display Processor which accepts four different data input formats. These are IIC, Y, B-Y, R-Y. The input data are digital but the output are analog. This IC is the last step at the feature box .

3- DEFLECTION UNIT

The programmable deflection processor TDA9151B provides the driving pulses required for driving the horizontal and vertical output stages operating according to the 100Hz deflection principle. Apart from these, the above mentioned processor is also used for controlling the east-west circuit, carrying out a switch-off function (protection circuit) and providing the super sand castle pulse (SSC100) for the video signal amplifier. This processor is controlled via an I^2C BUS and receives the synchronisation pulses from the IPQ-BOX (as well as LLC-signal (line locked signal)).

PIN 1: Horizontal Flyback Input

Input pin for retrace pulses having an amplitude of 100Vpp by means of capacitive divider C208/C209. The retrace pulse is needed for the phase control of the driving pulse and the SSC pulse.

PIN 2: Display Super Sand Castle Input /Output

From this terminal a double-level SC pulse is provided. The first level i.e. 2.5V is for horizontal and vertical blanking where as the second level i.e. 4,5V is used for video clamping. Further more at pin2 the vertical deflection process is monitored. That means, in case of missing vertical pulses from I202(pin8), pin2 will be locked to 2,5V and the video channel will be controlled to black level.

PIN 6: EAST-WEST GEOMETRY OUTPUT

Output for east-west geometry provides the adjustment of horizontal deflection amplitude, picture width, parabolic east-west correction, east-west pin cushion correction and also parabolic correction of trapezium distortions.

PIN 7: EHT COMPENSATION

EHT compensation pin is an input for keeping the picture size constant although the value of EHT voltage changes (delivered from aquadac coating of the picture tube).

***The EHT voltage transformer provides following voltages:

EHT voltage 30KVDc.
Focusing and G2 voltage.
Filament voltage for picture tube.
+17Vdc
+40Vdc
+220Vdc.

In order to be able to adjust the horizontal amplitude of the picture (picture width) and the raster correction independently from the EHT voltage, the line output stage is connected to a diode modulator. One branch of the bridge consists of C211 and C212, another one consists of deflection coil, linearity coil, C213, and the bridge coil L207. At the diagonal branch C215 is placed where as part of the trace capacitance it simultaneously contributes to the internal pincushion correction. The control circuit of the EAST-WEST correction is connected via L204.

PIN 8:

Pin8 is designed to determine the reference current for the complete vertical deflection current.

PIN 9:

Pin 9 is for flash over protection and is not used at this chassis,

PIN 10:

This pin represents the output terminal for the vertical synchronisation. Pulse is the drive input of the differential amplifier stage belonging to the vertical output.

PIN 11:

At this IC via I^2CBUS, it is possible to adjust the following values:

Amplitude of vertical deflection signal 80%, tangential correction from 0 to 16%, vertical shift centering in 7 steps from - 1,5% to +1,5% and 16/9 change-over.

Pin 12: VA Input

The vertical synchronisation input coming from the Feature Box

PIN 13: HA Input

Horizontal synchronisation input coming from the Feature Box.

PIN 14: LLC Input

This signal is for the line and vertical oscillator. Without LLC signal (27MHz) this IC can not operate.

COMPONENT DESCRIPTIONS

1) TDA4780
2) TDA4665
3) TDA9143
4) SAA4961
5) TDA4470
6) TDA9151
7) TDA8540
8) TDA8351
9) TDA9875-A
10) TDA2616
11) TDA4605-3
12) TDA6111Q
13) M27C2001
14) ST24C16
15) SAA7710
16) TDA7053 A
17) SDA5250

TDA4780

RGB Video Processor with Automatic Cut-off control and Gamma Adjust

GENERAL DESCRIPTION

The TDA4780 is a monolithic integrated circuit with a luminance and a colour difference interface for video processing in TV receivers. Its primary function is to process the luminance and colour difference signals from a colour decoder which is equipped e.g. with the multistandard decoder TDA4655 or TDA9160 plus delayline TDA4661 or TDA4665 and the Picture Signal Improvement (PSI) IC TDA467X or from a feature module.

Two sets of analog RGB colour signals can also inserted, e.g. one from a peritelevision connector (SCART plug) and the other one from an On-Screen Display (OSD) generator. The TDA4780 has I²C-bus control of all parameters and functions with automatic cut-off control of the picture tube cathode currents.

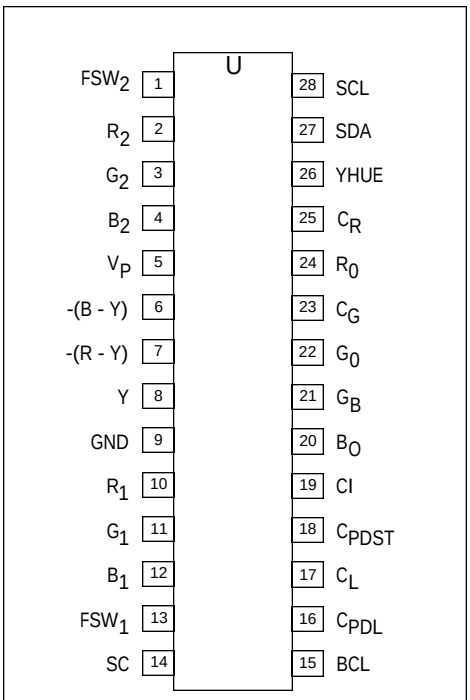
It provides RGB output signals for the video output stages. In clamped output mode it can also be used as an RGB source.

The required input signals are:

- Luminance and negative colour difference signals
- 2 or 3-level sandcastle pulse for internal timing pulse generation
- I²C-bus data and clock signals.

FEATURES

- Gamma adjust
- Dynamic black control (adaptive black)
- All input signals clamped on black-levels
- Automatic cut-off control, alternative: output clamping on fixed levels
- Three adjustable reference voltage levels via I²C-bus for automatic cut-off control
- Luminance/colour difference interface
- Two luminance input levels allowed
- Two RGB interfaces controlled by either fast switches or by I²C-bus
- Two peak drive limiters, selection via I²C-bus
- Blue stretch, selection via I²C-bus
- Luminance output for scan velocity modulation (SCAVEM)
- Extra luminance output; same pin can be used as hue control output e.g. for the TDA4650 and TDA4655
- Non standard operations like 50 Hz/32 kHz are also possible
- Either 2 or 3 level sandcastle pulse applicable
- High bandwidth for 32 kHz application
- White point adjusts via I²C-bus
- Average beam current and improved peak drive limiting
- Two switch-on delays to prevent discoloration during start-up
- All functions and features programmable via I²C-bus
- PAL/SECAM or NTSC matrix selection.



Pin Connections

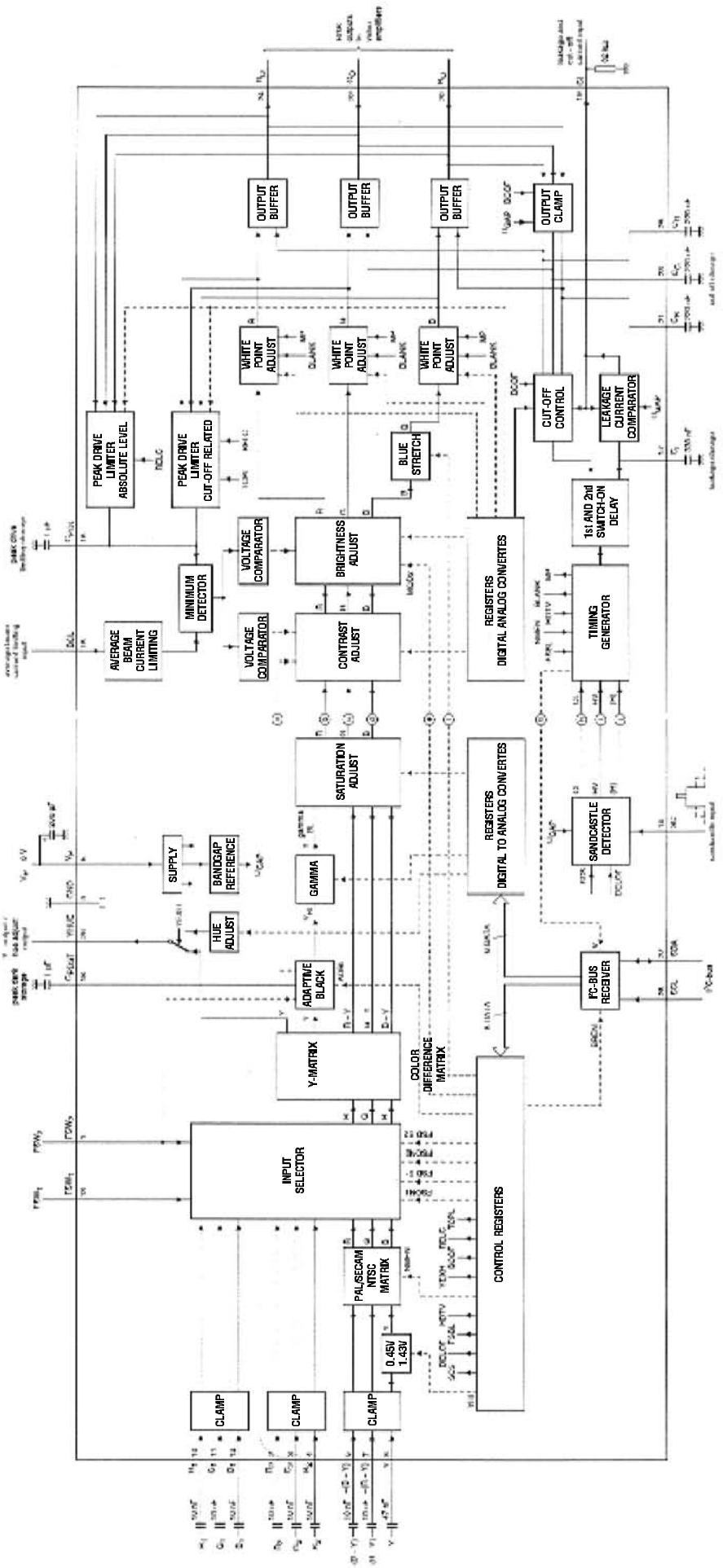
PINNING

SYMBOL	PIN	DESCRIPTION
FSW_2	1	fast switch 2 input
R_2	2	red input 2
G_2	3	green input 2
B_2	4	blue input 2
V_p	5	supply voltage
–(B - Y)	6	colour difference input –(B - Y)
–(R - Y)	7	colour difference input –(R - Y)
Y	8	luminance input
GND	9	ground
R_1	10	red input 1
G_1	11	green input 1
B_1	12	blue input 1
FSW_1	13	fast switch 1 input
SC	14	sandcastle pulse input
BCL	15	average beam current limiting input
C_{PDL}	16	storage capacitor for peak limiting
CL	17	storage capacitor for leakage current compensation
C_{PDST}	18	storage capacitor for peak dark
CI	19	cut-off measurement input
B_0	20	blue output
C_B	21	blue cut-off storage capacitor
G_0	22	green output
C_G	23	green cut-off storage capacitor
R_0	24	red output
C_R	25	red cut-off storage capacitor
YHUE	26	Y-output/hue adjust output
SDA	27	I^2C-bus serial data input/acknowledge output
SCL	28	I^2C-bus serial clock input

QUICK REFERENCE DATA

SYMBOL	PARAMETER	Min.	Typ.	Max.	Unit
V_P	supply voltage (pin5)	7.2	8.0	8.8	V
I_P	supply current (pin5)	8.0	100	120	mA
$V_{8(p-p)}$	luminance input (peak-to-peak value) (C)VBS	-	0.45/1.43	-	V
$V_{6(p-p)}$	–(B - Y) input (peak-to-peak value)	-	1.33	-	V
$V_{7(p-p)}$	–(R - Y) input (peak-to-peak value)	-	1.05	-	V
V_{14}	three-level sandcastle pulse				
	H+V	-	2.5	-	V
	H	-	4.5	-	V
	BK	-	8.0	-	V
	two-level sandcastle pulse				
	H+V	-	2.5	-	V
	BK	-	4.5	-	V
V_i	RGB input signals at pins 2,3,4,10,11 and 12(black-to-white value)	-	0.7	-	V
$V_{o(p-p)}$	RGB output at pins 24, 22 and 20(black-to-white value)	-	2.0	-	V
T_{amb}	operating ambient temperature	-20	-	+70	°C

Block diagram



FUNCTIONAL DESCRIPTION

Signal input stages

The TDA4780 contains 3 sets of input signal stages for:

1. Luminance/colour-difference signals:
   a) Y: 0.45 V (p-p) VBS or 1.43 V (p-p) VBS, selectable via I2C-bus.
   b) -(R - Y): 1.05 V (p-p).
   c) -(B - Y): 1.33 V (p-p).
   The capacitively coupled signals are matrixed to RGB signals by either a PAL/SECAM or NTSC matrix (selected via I^2C-bus).
2. $(RGB)_1$ signals (0.7 V (p-p) VB), capacitively coupled (e.g. from external source).
3. $(RGB)_2$ signals (0.7 V (p-p) VB), capacitively coupled (e.g. videotext, OSD).

All input signals are clamped in order to have the same black levels at the signal switch input. Displayed signals must be synchronous with the sandcastle pulse.

Signal switches

Both fast signal switches can be operated by switching pins (e.g. SCART facilities) or set via the I^2C-bus. With the pin FSW_1 the Y-CD signals or the $(RGB)_1$ signals can be selected, with pin FSW_2 the above selected signals or the $(RGB)_2$ signals are enabled. During the vertical and horizontal blanking time an artificial black level equal to the clamped black level is inserted in order to clip off the sync pulse of the luminance signal and to suppress hum during the cut-off measurement time and eliminate noise during these intervals.

Saturation, contrast and brightness adjust

Saturation, contrast and brightness adjusts are controlled via the I^2C-bus and act on Y, CD as well as on RGB input signals. Gamma acts on the luminance content of the input signals.

Gamma adjust

The gamma adjust stage has a non-linear transmission characteristic according to the formula $y = x^{gamma}$, where x represents the input and y the output signal. If gamma is smaller than unity, the lower parts of the signal are amplified with higher gain.

Automatic cut-off control

During leakage measurement time the leakage current is compensated in order to get a reference voltage at the cut-off measurement info pin. This compensation value is stored in an external capacitor. During cut-off current measurement times for the R, G and B channels, the voltage at this pin is compared with the reference voltage, which is individually adjustable via I^2C-bus for each colour channel. The control voltages that are derived in this way are stored in the external feedback capacitors. Shift stages add these voltages to the corresponding output signals. The automatic cut-off control may be disabled via the I^2C-bus. In this mode the output voltage is clamped to 2.5 V. Clamping periods are the same as the cut-off measurement periods.

Adaptive black (ADBL)

The adaptive black stage detects the lowest voltage of the luminance component of the internal RGB signals during the scanning time and shifts it to the nominal black level. In order to keep the nominal white level the contrast is increased simultaneously.

Blue stretch (BLST)

The blue stretch channel gets additional amplification if the blue signal is greater than 80% of the nominal signal amplitude. In the event the white point is shifted towards higher colour temperature so that white parts of a picture seem to be brighter.

Measurement pulse and blanking stage

During the vertical and horizontal blanking time and the measurement period the signals are blanked to an ultra black level, so the leakage current of the picture tube can be measured and automatically compensated for.

During the cut-off measurement lines (one line period for each R, G or B) the output signal levels are at cut-off measurement level.

The vertical blanking period is timed by the sandcastle pulse. The measurement pulses (leakage, R, G and B) are triggered by the negative going edge of the vertical pulse of the sandcastle pulse and start after the following horizontal pulse.

The IC is prepared for $2f_H$ (32 kHz) application.

Output amplifier and white adjust potentiometer

The RGB signals are amplified to nominal 2 V (p-p), the DC-levels are shifted according to cut-off control.

The nominal signal amplitude can be varied by ±50% by the white point adjustment via the I²C-bus (individually for RGB respect).

Signal limiting

The TDA4780 provides two kinds of signal limiting.

First, an average beam limiting, that reduces signal level if a certain average is exceeded. Second, a peak drive limiting, that is activated if one of the RGB signals even shortly exceeds a via I²C-bus adjusted threshold. The latter can be either referred to the cut-off measurement level of the outputs or to ground.

When signal limiting occurs, contrast is reduced, and at minimum contrast brightness is reduced additionally.

Sandcastle decoder and timer

A 3-level detector separates the sandcastle pulse into combined line and field pulses, line pulses, and clamping pulses. The timer contains a line counter and controls the cut-off control measurement.

Application with a 2-level 5 V sandcastle pulse is possible.

Switch on delay circuit

After switch on all signals are blanked and a warm up test pulse is fed to the outputs during the cut-off measurement lines. If the voltage at the cut-off measurement input exceeds an internal level the cut-off control is enabled but the signal remains still blanked. In the event of output clamping, the cut-off control is disabled and the switch on procedure will be skipped.

Y output and hue adjust

The TDA4780 contains a D/A converter for hue adjust. The analog information can be fed, e.g. to the multistandard decoder TDA4650 or TDA4655. This output pin may be switched to a Y output signal, which can be used for scan velocity modulation (SCAVEM). The Y output is the Y input signal or the matrixed (RGB) input signal according to the switch position of the fast switch.

I²C-bus

The TDA4780 contains an I²C-bus receiver for control function.

ESD protection

The Pins are provided with protection diodes against ground and supply voltage (see Chapter "internal pin configurations"). I²C-bus input pins do not shunt the I²C-bus signals in the event of missing supply voltage.

EMC

The pins are protected against electromagnetic radiation.

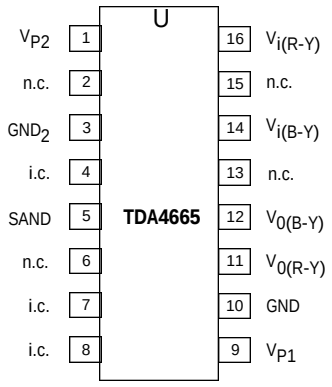
TDA4665
Baseband Delay Line

GENERAL DESCRIPTION
The TDA4665 is an integrated baseband delay line circuit with one line delay.. It is suitable for decoders with colour-difference signal outputs ±(R-Y) and ±(B-Y)

FEATURES
- The comb filters, using the switched-capacitor technique, for one line delay time (64 µs)
- Adjustment-free application
- No crosstalk between SECAM colour carriers (diaphoty)
- Handles negative or positive colour-difference input signals
- Clamping of AC-coupled input signals ±(R-Y) and ±(B-Y))
- VCO without external components
- 3 MHz internal clock signal derived from a 6MHz CCO, line-locked by the sandcastle pulse (64 µs line)
- Sample - and - hold circuits and low-pass filters to suppress the 3 MHz clock signal
- Addition of delayed and non-delayed output signals
- Output buffer amplifiers
- Comb filtering functions for NTSC colour-difference signals to suppress cross-colour)

PINNING

SYMBOL	PIN	DESCRIPTION
V_{P2}	1	+5V supply voltage for digital part
n.c.	2	not connected
GND2	3	ground for digital part (0V)
i.c.	4	internally connected
SAND	5	sandcastle pulse input
n.c.	6	not connected
i.c.	7	internally connected
i.c.	8	internally connected
V_{P1}	9	+5V supply voltage for analog part
GND1	10	ground for analog part (0V)
$V_{0(R-Y)}$	11	±(R–Y) output signal
$V_{0(B-Y)}$	12	±(B–Y) output signal
n.c.	13	not connected
$V_{i(B-Y)}$	14	±(B–Y) input signal
n.c.	15	not connected
$V_{i(R-Y)}$	16	±(R–Y) input signal

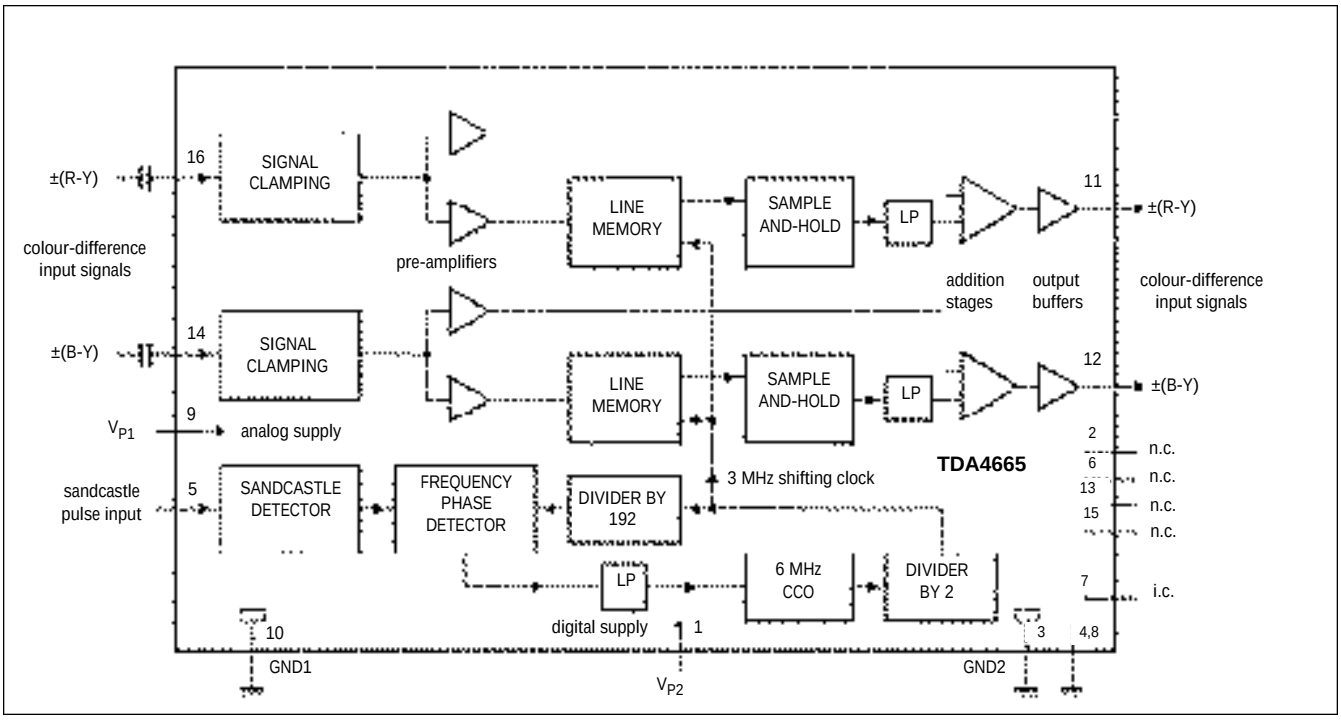


Pin configuration

QUICK REFERENCE DATA

SYMBOL	PARAMETER	Min.	Typ.	Max.	Unit
V_{P1}	analog supply voltage (pin9)	4.5	5	6	V
V_{P2}	digital supply voltage (pin1)	4.5	5	6	V
$I_{P(tot)}$	total supply current	-	5.5	7.0	mA
$V_{i(p-p)}$	±(R - Y) input signal PAL/NTSC(peak-to-peak value; pin 16)	-	525	-	mV
	±(B - Y) input signal PAL/NTSC(peak-to-peak value; pin 14)	-	665	-	mV
	±(R - Y) input signal SECAM (peak-to-peak value; pin 16)	-	1.05	-	V
	±(B - Y) input signal SECAM (peak-to-peak value; pin 14)	-	1.33	-	V
G_V	gain V_0/V_i of colour-difference output signals				
	V_{11} / V_{16} for PAL and NTSC	5.3	5.8	6.3	dB
	V_{12} / V_{14} for PAL and NTSC	5.3	5.8	6.3	dB
	V_{11} / V_{16} for SECAM	-0.6	-0.1	+0.4	dB
	V_{12} / V_{14} for SECAM	-0.6	-0.1	+0.4	dB

Block diagram



LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134). Ground pins 3 and 10 connected together.

SYMBOL	PARAMETER	Min.	Max.	Unit
V_{P1}	analog supply voltage (pin9)	-0.5	+7	V
V_{P2}	digital supply voltage (pin1)	-0.5	+7	V
V_5	voltage on pin 5	-0.5	V_P + 1.0	V
V_n	voltage on pins 11, 12, 14 and 16	-0.5	V_P	V
T_{stg}	storage temperature	-25	+150	°C
T_{amb}	operating ambient temperature	0	70	°C
V_{ESD}	electrostatic handling for all pins;	-	±500	V

CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	Min.	Typ.	Max.	Unit
Supply						
V_{P1}	analog supply voltage (pin9)		4.5	5	6	V
V_{P2}	digital supply voltage (pin1)		4.5	5	6	V
I_{P1}	analog supply current		-	4.8	6.0	mA
I_{P2}	digital supply current		-	0.7	1.0	mA
Colour-difference input signals						
$V_{i(p-p)}$	input signal (peak-to-peak value)					
	±(R - Y) PAL and NTSC (pin 16)		-	525	-	mV
	±(B - Y) PAL and NTSC (pin 14)		-	665	-	mV
	±(R - Y) SECAM (pin 16)		-	1.05	-	V
	±(B - Y) SECAM (pin 14)		-	1.33	-	V
$V_{i(max)(p-p)}$	maximum symmetrical input signal (peak-to-peak value)					
	±(R - Y) or ±(B - Y) for PAL and NTSC	before clipping	1	-	-	V
	±(R - Y) or ±(B - Y) for SECAM	before clipping	2		-	V
$R_{14, 16}$	input resistance during clamping		-	-	40	kΩ
$C_{14, 16}$	input capacitance		-	-	10	pF
$V_{14, 16}$	input clamping voltage	proportional to Vp	1.3	1.5	1.7	V
Colour-difference output signals						
$V_{o(p-p)}$	output signal (peak-to-peak value)					
	±(R - Y) on pin 11	all standards	-	1.05	-	V
	±(B - Y) on pin 12	all standards	-	1.33	-	V
$V_{11,}$ V_{12}	ratio of output amplitudes at equal input signals	$V_{i(14,16)(p-p)}$= 1.33 V	-0.4	0	+0.4	dB
$V_{11, 12}$	DC output voltage	proportional to Vp	2.5	2.9	3.3	V
$R_{11, 12}$	output resistance		-	330	400	Ω
G_v	gain for PAL and NTSC	ratio V_0/V_i	5.3	5.8	6.3	dB
	gain for SECAM	ratio V_0/V_i	-0.6	-0.1	+0.4	dB
V_0/V_{0+1}	ratio of delayed to non-delayed output signals (pins 11 and 12)	$V_{i(14,16)(p-p)}$= 1.33 V; SECAM signals	-0.1	0	+0.1	dB
$V_{n(rms)}$	noise voltage (RMS value pins 11 and 12)	$V_{i(14,16)}$ = 0 V; note 2	-	-	1.2	mV
$V_{(11, 12)(p-p)}$	unwanted signals (line - locked) (peak-to-peak value)	$V_{i(14,16)}$ = 0 V; active video; Rs = 300 Ω				
	meander		-	-	5	mV
	spikes		-	-	10	mV
S/N(W)	weighed signal-to-noise ratio (pins 11 and 12)	$V_{0(p-p)}$ = 1 V	-	54	-	dB
Δt_d	time difference between non-delayed and delayed output signals (pins 11 and 12)		63.94	64	64.06	µs
t_d	delay of non-delayed signals		40	60	80	ns
t_{tr}	transient time of delayed signal on pins 11 respectively 12	300 ns transient of SECAM signal	-	350	-	ns
	transient time of non-delayed signal on pins 11 respectively 12	300 ns transient of SECAM signal	-	320	-	ns
Colour-diff						
f_{BK}	burst-key frequency/sandcastle frequency		14.2	15.625	17.0	kHz
V_{t5}	top pulse voltage		4.0	-	V_p + 1.0	V
V_{slice}	internal slicing level		V_5 - 1.0	-	V_5 - 0.5	V
I_5	input current		-	-	10	µA
C_5	input capacitance		-	-	10	pF

TDA9143

I²C-BUS controlled, alignment-free PAL/NTSC/SECAM Decoder / Sync Processor

GENERAL DESCRIPTION

The TDA9143 is an I²C-bus controlled, alignment-free PAL/NTSC/SECAM decoder/sync processor with blanking facilities for PALplus and EDTV-2 signals. The TDA9143 has been designed for use with baseband chrominance delay lines, and has a combined subcarrier frequency/comb filter enable signal for communication with a PAL/NTSC comb filter.

The IC can process both CVBS input signals and Y/C input signals. The input signal is available on an output pin, in the event of a Y/C signal, it is added into a CVBS signal.

The sync processor provides a two-level sandcastle, a horizontal pulse (CLP or HA pulse, bus selectable) and a vertical (VA) pulse. When the HA pulse is selected, a line-locked clock (LLC) signal is available at the output port pin (6.75 MHz or 6.875 MHz).

A fast switch can select either the internal Y signal with the UV input signals, or YUV signals made of the RGB input signals. The RGB input signals can be clamped with either the internal or an external clamping signal.

Two pins with an input/output port and an output port of the I²C-bus are available.

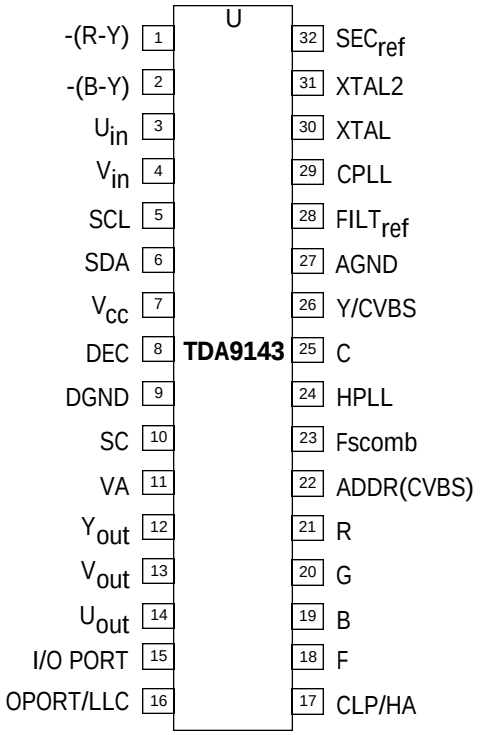
The I²C-bus address of the TDA9143 is hardware programmable.

FEATURES

- Multi-standard colour decoder and sync processor for PAL, NTSC and SECAM
- PALplus helper blanking and EDTV-2 blanking
- I²C-bus controlled
- I²C-bus addresses hardware selectable
- Pin compatible with TDA9141
- Alignment free
- Few external components
- Designed for use with baseband delay lines
- Integrated video filters
- Adjustable luminance delay
- Noise detector with I²C-bus read-out
- Norm/no norm detector with I2C-bus read-out
- CVBS or Y/C input, with automatic detection possibility
- CVBS output, provided I²C-bus address 8A is used
- Vertical divider system
- Two-level sandcastle signal
- VA synchronization pulse (3-state)
- HA synchronization pulse or clamping pulse CLP input/output
- Line-locked clock output (6.75 MHz or 6.875 MHz) or stand-alone I²C-bus output port
- Stand-alone I²C-bus input/output port
- Colour matrix and fast YUV switch
- Comb filter enable input/output with subcarrier frequency
- Internal bypass mode of external delay line for NTSC applications
- Low power standby mode with 3-state YUV outputs
- Fast blanking detector with I²C-bus read-out
- Blanked or unblanked sync on Y_{out} by I²C-bus bit BSY
- Internal MACROVISION gating for the horizontal PLL enabled by bus bit EMG.

PINNING

SYMBOL	PIN	DESCRIPTION
-(R-Y)	1	output signal for -(R–Y)
-(B-Y)	2	output signal for -(B-Y)
U_{in}	3	chrominance U input
V_{in}	4	chrominance V input
SCL	5	serial clock input
SDA	6	serial data input/output
V_{cc}	7	positive supply voltage
DEC	8	digital supply decoupling
DGND	9	digital ground
SC	10	sandcastle output
VA	11	vertical acquisition synchronization pulse
Y_{out}	12	luminance output
V_{out}	13	chrominance V output
U_{out}	14	chrominance U output
I/O PORT	15	input/output port
OPORT/LLC	16	output port/line-locked clock output
CLP/HA	17	clamping pulse/HA synchronization pulse input/output
F	18	fast switch select input
B	19	BLUE input
G	20	GREEN input
R	21	RED input
ADDR(CVBS)	22	I^2C-bus address input (CVBS output)
Fscomb	23	comb filter status input/output
HPLL	24	horizontal PLL filter
C	25	chrominance input
Y/CVBS	26	luminance/CVBS input
AGND	27	analog ground
$FILT_{ref}$	28	filter reference decoupling
CPLL	29	colour PLL filter
XTAL	30	reference crystal input
XTAL2	31	second crystal input
SEC_{ref}	32	SECAM reference decoupling



Pin Configuration

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	Min.	Typ.	Max.	Unit
V_{CC}	positive supply voltage		7.2	8.0	8.8	V
I_{CC}	supply current		50	60	70	mA
$V_{CVBS(p-p)}$	CVBS input voltage (peak-to-peak value)	top sync-white	-	1.0	1.43	V
$V_{Y(p-p)}$	luminance input voltage (peak-to-peak value)	top sync-whit	-	1.0	1.43	V
$V_{C(p-p)}$	chrominance burst input voltage (peak-to-peak value)		-	0.3	0.6	V
$V_{Y(out)}$	luminance black-white output voltage		-	1.0	-	V
$V_{U(out)(p-p)}$	U output voltage (peak-to-peak value)	standard colour bar	-	1.33	-	V
$V_{V(out)(p-p)}$	V output voltage (peak-to-peak value)	standard colour bar	-	1.05	-	V
$V_{SC(bl)}$	sandcastle blanking voltage level		2.2	2.5	2.8	V
$V_{SC(clamp)}$	sandcastle clamping voltage level		4.2	4.5	4.8	V
$V_{VA(bl)}$	VA output voltage		4.0	5.0	5.5	V
$V_{HA(bl)}$	HA output voltage		4.0	5.0	5.5	V
$V_{LLC(p-p)}$	LLC output voltage amplitude (peak-to-peak value)		250	500	-	mV
$V_{R, G, B(p-p)}$	RGB input voltage (peak-to-peak value)	0 to 100% saturation	-	0.7	1.0	V
$V_{clamp(I/O)}$	clamping pulse input(output voltage		-	5.0	-	V
$V_{sub(p-p)}$	subcarrier output voltage amplitude (peak-to-peak value)		150	200	300	mV
V_{OPORT}	port output voltage		4.0	5.0	5.5	V

FUNCTIONAL DESCRIPTION

The TDA9143 is an I²C-bus controlled, alignment-free PAL/NTSC/SECAM colour decoder/sync processor which has been designed for use with baseband chrominance delay lines. For PALplus and EDTV-2 (60 Hz) signals blanking facilities are included.

In the standard operating mode the I²C-bus address is 8A. If the address input is connected to the positive supply rail the address will change to 8E.

Input switch

CAUTION
The voltage on the chrominance pin must never exceed 5.5 V. If it does, the IC enters a testmode.

The TDA9143 has a two pin input for CVBS or Y/C signals which can be selected via the I²C-bus. The input selector also has a position in which it automatically detects whether a CVBS or Y/C signal is on the input. In this input selector position, standard identification first takes place on an added Y/CVBS and C input signal.

After that, both chrominance signal input amplitudes are checked once and the input with the strongest chrominance burst signal is selected. The input switch status is read out by the I²C-bus via output bit YC. The auto input detector indicates YC = 1 for a VBS input signal (no chrominance component).

CVBS output

In the standard operating mode with I²C-bus address 8A, a CVBS output signal is available on the address pin, which represents either the CVBS input signal or the Y/C input signal, added into a CVBS signal.

RGB colour matrix

CAUTION
The voltage on the Ui, pin must never exceed 5.5 V. If it does, the IC enters a test mode.

The TDA9143 has a colour matrix to convert RGB input signals into YUV signals. A fast switch, controlled by the signal on pin F and enabled by I2C-bus via EFS (enable fast switch), can select between these YUV signals and the YUV signals of the decoder. Mode FRGB = 1 (forced RGB) overrules EFS and switches the matrixed RGB inputs to the YUV outputs.

The Y signal is internally connected to the switch. The -(R-Y) and -(B-Y) output signals of the decoder first have to be delayed in external baseband chrominance delay lines. The outputs of the delay lines must be connected to the UV input pins. If the RGB signals are not synchronous with the selected decoder input signal, clamping of the RGB input signals is possible by I²C-bus selection of ECL (external RGB clamp mode) and by feeding an external clamping signal to the CLP pin.

Also in external RGB clamp mode the VA output will

be in a high impedance OFF-state. The YUV outputs can be put in 3-state mode by bus bit LPS (low power standby mode).

Standard identification

The standards which the TDA9143 can decode depend upon the choice of external crystals. If a 4.4 MHz and a 3.6 MHz crystal are used then SECAM, PAL 4.4/3.6 and NTSC 4.4/3.6 can be decoded. If two 3.6 MHz crystals are used then only PAL 3.6 and NTSC 3.6 can be decoded.

Which 3.6 MHz standards can be decoded depends upon the exact frequencies of the 3.6 MHz crystals. In an application where not all standards are required only one crystal is sufficient; in this instance the crystal must be connected to the reference crystal input (pin 30). If a 4.4 MHz crystal is used it must always be connected to the reference crystal input. Both crystals are used to provide a reference for the filters and the horizontal PLL, however, only the reference crystal is used to provide a reference for the SECAM demodulator. To enable the calibrating circuits to be adjusted exactly, two bits from I²C-bus subaddress 00 are used to indicate which crystals are connected to the IC.

The standard identification circuit is a digital circuit without external components.

The decoder (via the I²C-bus) can be forced to decode either SECAM or PAL/NTSC (but not PAL or NTSC). Crystal selection can also be forced. Information concerning standard and which crystal is selected and whether the colour killer is ON or OFF is provided by the read out.

Using the forced-mode does not affect the search loop, it does however prevent the decoder from reaching or staying in an unwanted state. The identification circuit skips impossible standards (e.g. SECAM when no 4.4 MHz crystal is fitted) and illegal standards (e.g. in forced mode). To reduce the risk of wrong identification, PAL has priority over SECAM. Only line identification is used for SECAM. For a vertical frequency of 60 Hz, SECAM can be blocked to prevent wrong identification by means of bus bit SAF.

Integrated filters

All chrominance bandpass and notch filters, including the luminance delay line, are an integral part of the IC. The filters are gyrator-capacitor type filters. The resonant frequency of the filters is controlled by a circuit that uses the active crystal to tune the SECAM Cloche filter during the vertical flyback time. The remaining filters and the luminance delay line are matched to this filter. The filters can be switched to either 4.43 MHz, 4.29 MHz or 3.58 MHz. The switching is controlled by the standard identification circuit. The luminance notch used for SECAM has a lower Q-factor than the notch used for PAL/NTSC. The notches are provided with a little preshoot to obtain a symmetrical step response. In Y/C mode the chrominance notch filters are bypassed, to preserve full signal bandwidth. For a CVBS signal the chrominance notch filters can be bypassed by bus selection of bit TB (trap bypass). The delay of the colour difference signals -(R-Y) and -(B-Y) in the chrominance signal path and the external chrominance delay lines when used, can be fitted to the luminance signal by I²C-bus in 40 ns steps.

The typical luminance delay can be calculated:
delay ≈90 + $\overline{SAK}$. $\overline{SBK}$ {170 + 40($\overline{FRQTB}$)} + 160(YD3) + 160(YD2) + 80(YD1) + 40(YD0) [ns].

Color decoder

The PAL/NTSC demodulator employs an oscillator that can operate with either crystal (3.6 MHz or 4.4 MHz). If the I²C-bus indicates that only one crystal is connected, it will always connect to the crystal on the reference crystal input (pin 30).

The Hue signal which is adjustable by I²C-bus, is gated during the burst for NTSC signals.

The SECAM demodulator is an auto-calibrating pLL demodulator which has two references. The reference crystal, to force the PLL to the desired free-running frequency and the bandgap reference, to obtain the correct absolute value of the output signal. The VCO of the PLL is calibrated during each vertical blanking period, when the IC is in search mode or in SECAM mode.

If the reference crystal is not 4.4 MHz the decoder will not produce the correct SECAM signals. Especially for NTSC applications an internal bypass mode of the external baseband delay line (for instance TDA4665) is added, controlled by bus bit BPS (bypass mode) and with a gain of 2. The bypass mode is not available for SECAM.

Comb filter interfacing

The frequency of the active crystal is fed to the Fscomb output, which can be connected to an external comb filter IC (e.g. SAA4961). When bus bit ECMB is LOW, the subcarrier frequency is suppressed and its DC value is LOW. With ECMB HIGH, the DC value is HIGH with the subcarrier frequency present, and I²C-bus output bit YC and the input switch are always forced in the Y/C mode, unless an external current sink (e.g. from the comb filter) prevents this, as pin Fscomb also acts as input pin. In this event the subcarrier frequency is still present on the same DC HIGH level.

PALplus and EDTV-2 helper blanking

For blanking of PALplus or EDTV-2 helper lines, the helper blanking can extend the vertical blanking of the Y, R-Y and B-Y outputs. Additional helper blanking bits (HOB, HBC) and norm/not norm (NRM) indication determine whether the helper signal has to be blanked or conditionally blanked depending on the signal-to-noise ratio bit SNR. Table 1 is valid in a 50 Hz or 60 Hz mode.

Helper blanking modes

HOB	HBC	SNR BLANKING	HELPER
0	X	X	OFF
1	O	X	ON
1	1	0	OFF
1	1	1	ON

For PALplus (50 Hz, 625 lines) outside the letter box area blanking is possible and takes place on lines 275 to 371 and 587 to 59.

For EDTV-2 (system M, 60 Hz, 525 lines) outside the letter box area blanking is possible and takes place on lines 230 to 312 and 493 to 49

Provided a NORM sync condition is present, with bus bit HBO = 1 and HBC = 0 blanking is activated. Conditional blanking is possible with HBO = 1 and HBC = 1 and SNR = 1.

The black level of the luminance signal is internally clamped with a large time constant to an internal reference black level. This black level is used as fill-in value for the Y signal during blanking.

Fast blanking detector

To detect the presence of a fast blanking signal, a circuit is added which indicates this event if in more than one line per field a blanking pulse is present at the fast blanking input (F). More than one line per field is chosen to prevent switching-off at every spike detected on the fast blanking input. The detector output FBA (fast blanking active) can be read-out by the I²C-bus.

Blanked/unblanked sync

By means of the I2C-bus bit BSY (blanked sync) output signal Yout will be presented with or without its composite sync part. At BSY = 0 the composite sync is present on Yout When activated, helper blanking takes place only during helper lines scan. At BSY = 1 the black level is filled in during the line blanking interval and vertical blanking interval. When activated, the helper blanking extends the

vertical blanking.

Sync processor (ϕ_1 loop)

The main part of the sync circuit is an oscillator running at 440 x f_H (6.875 MHz), provided that I²C-bus address 8A is used or 432 x fH (6.75 MHz) for 8E. Its frequency is divided by 440 or 432 to lock the ϕ_1 loop to the incoming signal.

The time-constant of the loop can be selected by the I²C-bus (fast, auto or slow). In the fast mode the fast time-constant is chosen independent of signal conditions. In the auto mode the medium time-constant is present with a fast time constant during the vertical retrace period ('field boost'). If the noise detector indicates a noisy video signal the time-constant switches to slow with a smaller field boost, which is also the time-constant for the slow mode. In case of a slow time constant sync gating takes place in a 6 µs window around the separated sync pulse. In case of no sync lock, both the auto and the slow mode have a medium time constant, to ensure reliable catching.

The noise content of the video signal is determined by a noise detector circuit. This circuit measures the noise at top sync during a 15 line period every field (65 lines after start VA pulse). When the noise level supersedes the detector threshold in two consecutive fields, noise is indicated and bus bit SNR is set.

The free-running frequency of the oscillator is determined by a digital control circuit that is locked to the active crystal. When a power-on-reset pulse is detected the frequency of the oscillator is switched to a frequency of about 10 MHz (23 kHz horizontal frequency) to protect the horizontal output transistor. The oscillator frequency is calibrated to 6.875 MHz or 6.75 MHz after receiving data on subaddress 01 for the first time after power-on-reset detection.

To ensure that this procedure does not fail it is absolutely necessary to send subaddress 00 before subaddress 01. Subaddress 00 contains the crystal indication bits and when subaddress 01 is received the line oscillator calibration will be initiated (for the start-up procedure after power-on-reset detection, see the I²C-bus protocol). The calibration is terminated when the oscillator frequency reaches 6.875 MHz or 6.75 MHz.

The ϕ_1 loop can be opened using the I²C-bus. This is to facilitate On Screen Display (OSD) information. If there is no input signal or a very noisy input signal, the ϕ_1 loop can be opened to provide a stable line frequency, and thus astable picture.

The sync part also delivers a two-level sandcastle signal, which provides a combined horizontal and vertical blanking signal and a clamping pulse for the display section of the TV.

MACROVISION sync gating

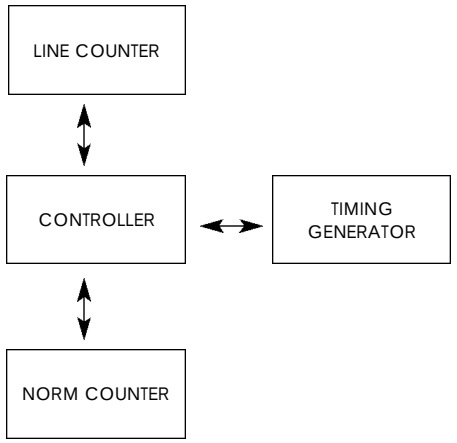
A dedicated gating signal for the separated sync pulses, starting 11 lines after the detection of a vertical sync pulse until picture scan starts, can be used to improve the behaviour of the horizontal PLL with respect to the unwanted disturbances caused by the pseudo-sync pulses in video signals with MACROVISION anti-copy guard signals. This sync gating excludes the pseudo-sync pulses and can only take place in the auto and fast ϕ_1 time constant mode, provided I²C-bus bit SNR = 0 and I²C-bus bit EMG = 1. I²C-bus bit EMG = 1 enables and EMG = 0 disables this sync gating in the horizontal PLL.

Vertical divider system

The vertical divider system has a fully integrated vertical sync separator.

The divider can accommodate both 50 Hz and 60 Hz systems; it can either determine the field frequency automatically or it can be forced to the desired system via the I²C-bus. A block diagram of the vertical divider system is illustrated in the following figure.

The divider system operates at twice the horizontal frequency. The line counter receives enable pulses at this frequency, thereby counting two pulses per line. A state diagram of the controller is shown in Fig.5. Because it is symmetrical only the right-hand part will be described.



Block diagram of the vertical divider system.

Depending on the previously found vertical frequency, the controller will be in one of the COUNT states. When the line counter has counted 488 pulses (i.e. 244 lines of the video input signal), the controller will move to the next state depending on the output of the norm counter. This can be either NORM, NEAR_NORM or NO_NORM, depending on the position of the vertical sync pulse in the previous fields. When the controller is in the NORM state it generates the vertical sync pulse (VSP) automatically and then, when the line counter is at LC = 626, moves to the WAIT state. In this condition it waits for the next pulse of the double line frequency signal, and then moves to the COUNT state of the current field frequency. When the controller returns to the COUNT state, the line counter will be reset half a line after the start of the vertical sync pulse of the video input signal. The NORM window normally looks within one line width and a sudden half line delay of the vertical sync pulse change can therefore be neglected.

When the controller is in the NEAR_NORM state it will move to the COUNT state if it detects the vertical sync pulse within the NEAR-NORM window (i.e. 622 < LC < 628). If no vertical sync pulse is detected the controller will move back to the COUNT state when the line counter reaches LC = 628. The line counter will then be reset.

When the controller is in the NO_NORM state, it will move to the COUNT state when it detects a vertical sync pulse and reset the line counter. If a vertical sync pulse is not detected before LC = 722 (if the ϕ_1 loop is locked in forced mode) it will move to the COUNT state and reset the line counter. If the ϕ_1 loop is not locked the controller will return to the COUNT state when LC = 628.

The forced mode option keeps the controller in either the left-hand side (60 Hz) or the right-hand side (50 Hz) of the state diagram.

Figure 6 illustrates the state diagram of the norm counter which is an up/down counter that increases its counter value by 1 if it finds a vertical sync pulse within the selected window. If not, it decreases the counter value by 1 **(or 2, see Fig.6)**. In the NEAR_NORM and NORM states the first correct vertical sync pulse after one or more incorrect vertical sync pulses is processed as an incorrect pulse. This procedure prevents the system from staying in the NEAR - NORM or NORM state if the vertical sync pulse is correct in the first field and incorrect in the second field.

In case of no sync lock (SLN = 1) the norm counter is reset to NO_NORM (wide search window), for fast vertical catching when switching between video sources. Fast switching between different channels however can still result in a continuous horizontal sync lock situation, when the channel is changed before the norm counter has reached the NORM state. To provide faster vertical catching in this case, measures have been taken to prevent the norm counter to count down to zero before reaching the NO_NORM state. Bus bit FWW (forced wide window) enables the norm counter to stay in the NO_NORM state if desired. The norm/no_norm status is read out by bus bit NRM.

Output port and in/output port

Two stand-alone ports are available for external use. These ports are I2C-bus controlled, the output port by bus bit OPB and the input/output port by bus bit OPA. Bus bit OPA is an open-drain output, to enable input port functionality. The pin status is read out by bus via output bit IP.

Sandcastle

Figure 7 illustrates the timing of the acquisition sandcastle (ASC) and the VA pulse with respect to the input signal. The sandcastle signal is according to the two-level 5 V sandcastle format. An external vertical guard current can overrule the sink current to enable blanking purposes.

SAA4961
Multistandard Comb Filter

The one-chip Multistandard Comb Filter

In TV signal processing a comb filter is used to separate the chrominance and the luminance signals from the CVBS signal without effects such as cross-luminance and cross-colour.

The comb filter SAA 4961/V2 shown in figure 3 uses two 2H delay lines together with an adaptive logical comb filter algorithm for processing the PAL standard. In case of NTSC processing two 1H delay lines are used. Effects like hanging dots or residual cross-colour, seen when using a classical comb filter algorithm, are not produced.

The switched capacitor delay lines produce three output signals 0H, 2H and 4H (NTSC: 0H, 1H, 2H). To prevent alias components resulting from the discrete time signal processing, a low-pass pre-filter is integrated in ront.

Together with the transversal band-pass filters, the logical comb filter eliminates the luminance components (in the chrominance frequency band) from the chrominance signal. To eliminate cross-luminance the comb filtered chrominance is now subtracted from the time compensated CVBS signal and converted by the post filtering to the continuous time domain.

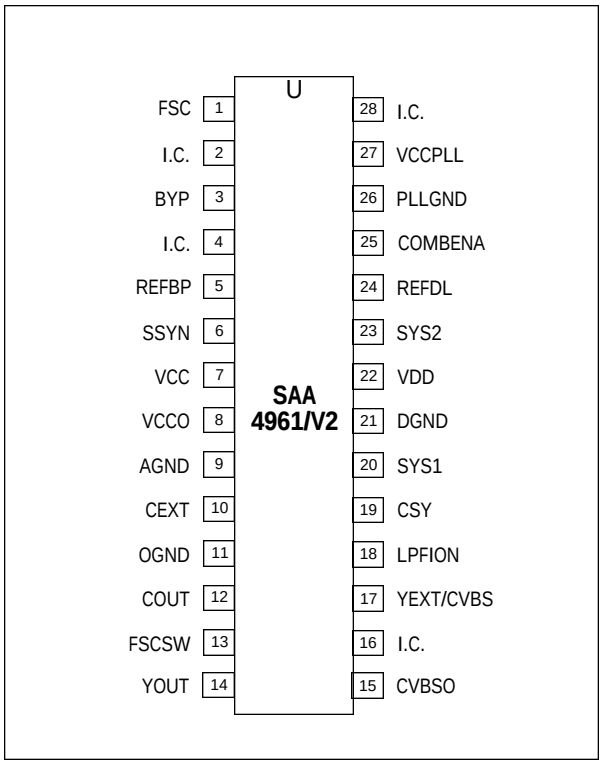
Signal switches for an external SVHS signal or non-delayed CVBS signals are available. They can be controlled externally via BYP (pin 3) and SSYN (pin 6).

Internal clock generation only requires a subcarrier signal (fsc or 2 x fsc). Sync separation (SYNC) is included for the generation of control signals for the delay lines.

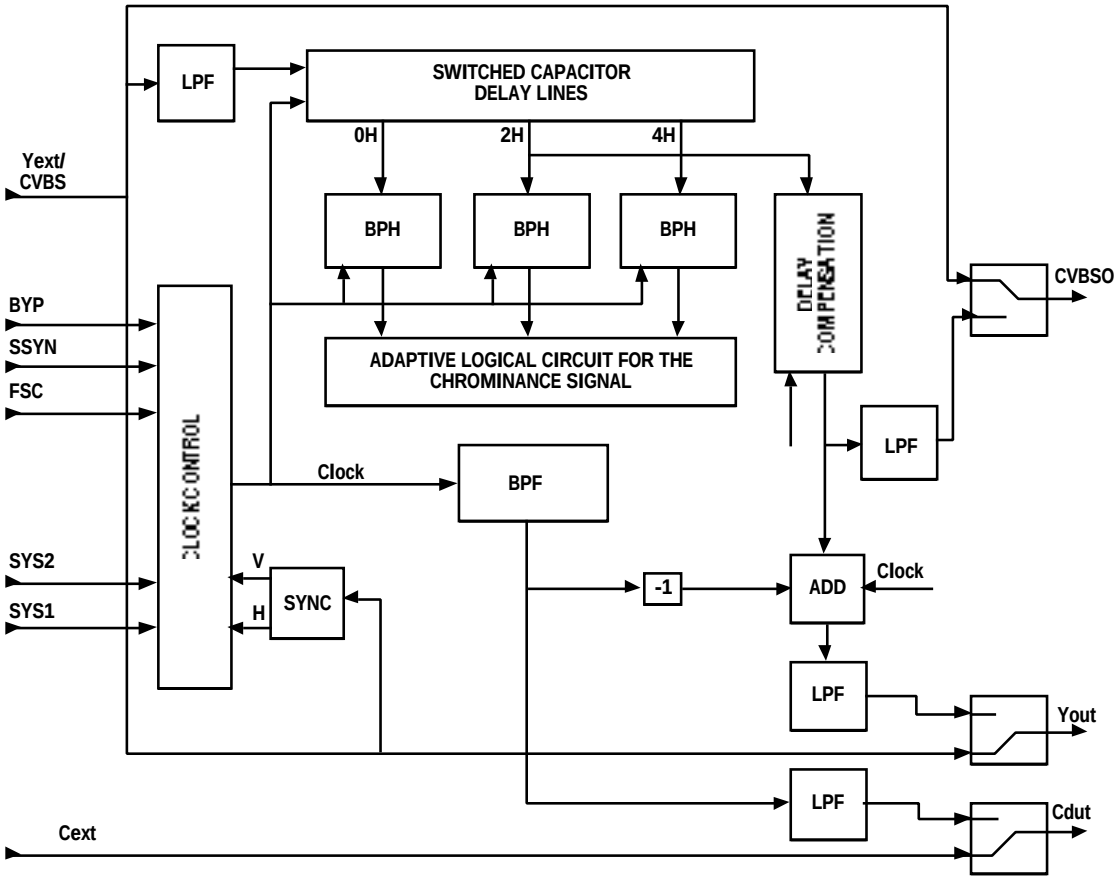
Pin names and shord description

SYMBOL	PIN	DESCRIPTION
FSC	1	subcarrier frequency input
I.C.	2	internal connected
BYP	3	BYPASS mode forcing
I.C.	4	internal connected
REFBP	5	decoupling capacitor for bandpass reference
SSYN	6	BYPASS definition input
V_{cc}	7	analog supply voltage
V_{CCO}	8	analog output supply voltage
AGND	9	analog ground (signal reference)
CEXT	10	external chrominance input
OGND	11	analog output buffer ground
COUT	12	chrominance output signal
FSCSW	13	fsc reference selection
Y_{out}	14	luminance output signal
CVBSO	15	uncombed CVBS output signal
I.C.	16	internal connected
YEXT/CVBS	17	CVBS input signal
LPFION	18	disable alias filter
CSY	19	storage capacitor
GSYS1	20	standard select 1
DGND	21	digital ground
VDD	22	digital supply voltage
SYS2	23	standard select 2
REFDL	24	decoupling capacitor for delay lines
COMBENA	25	COMB mode output signal
PLLGND	26	analog PLL ground
VCCPLL	27	analog PLL supply voltage
I.C.	28	internal connected

Package type:DIP 28



Pinning SAA4961/V2



FUNCTIONAL DESCRIPTION

The Video Processing

The combing path for luminance and chrominance

The CVBS signal is fed by a coupling capacitor to the video input pin 17 (YEXT/CVBS) and is internally clamped. From there it goes to an input anti-aliasing lowpass filter. A selector switch, externally controlled by pin 18 (LPFION) allows to switch the input filter on and off.

From there the video signal is taken to the delay line section of the chip. Here the signal is sampled and sequential stored in a memory of capacitors. The three output signals of this circuit have a delay of 0H, 2H and 4H for PAL signals (NTSC: 0H, 1H and 2H). These three very accurate in time matched signals are bandpass filtered and then fed to a logical comb filter.

Here the comb filter action takes place by adding the 0H and 2H (NTSC: 0H and 1H) signals and by adding at the same way the 2H and 4H (NISC: 1H and 2H) signal, this to free the chrominance signals from unwanted (in band) luminance components. In the same block a decision logic circuit makes the selection which chrominance signal should be taken to the output. This is done to prevent hanging dots, or wrong vertical colour transients.

The output signal of the comb filter block is bandpass filtered and fed to the addition stage. Here the 2H (NTSC: 1H) delayed and time equalized CVBS signal and the comb filtered chrominance signal are added. By this addition the chrominance signal in the luminance channel is cancelled, without influencing the high frequency luminance components.

By post-filtering the luminance and the chrominance output signal paths, the discrete time signals are converted back to the analog time domain and by an output buffer fed to YOUT (pin14) for the luminance and COUT (pin12). for the chrominance signal.

The bypass signal path for non PAL/NTSC signals and Y/C mode (SVHS)

In case the signal is not a PAL or NTSC CVBS signal (for instance SECAM signal) and so not suitable for being combed, the comb filter function is bypassed. In that mode the CVBS input signal is directly switched to the YOUT buffer (pin 14). The chrominance input pin CEXT (pin 10) is then switched to the output buffer of COUT (pin 12).

These paths are also used for SVHS signals, or other Y/C signal sources, where luminance and chrominance signals are already separately available.

Switching from combing to bypass is controlled by the bypass signal BYP (pin 3) and bypass definition signal SSYN (pin 6).

The teletext path (TXT)

It is very important, that the picture on the picture tube is not shifted if the comb filter is switched on or off. There- fore it is recommended to use the Yout path as TV synchronisation source. For TXT signals however the Yout path cannot be used in case of COM B-ON, because the TXT signals are distorted by the comb action. The CVBS signal, available at pin 15 (CVBSO), can be used for TXT concepts which are only using a educed number of lines at the end of the vertical blanking interval.

If the TXT concept is able to use all lines in the vertical interval only the CVBS signal at the input pin 17 can be used.

Clock processing

The delay lines of the SAA4961/V2 are designed for a clock frequency of 3x Fsub. The internal clock frequency is locked to the reference frequency Fsc at pin 1. This reference frequency may be Fsub or 2x Fsub and should be derived from the colour decoder.

Sync processing

A correct function or the comb filter is only possible if the control signals for the delay lines are synchronised with the horizontal and vertical frequency of the processed signal. These H and V signals are derived from the sync signal of the incoming CVBS signal (pin 17) via a sync separation circuit.

This sync separator circuit requires an external capacitor at pin 19.

TDA4470B

Multistandard Video-If and Quasi Parallel Sand Processing

DESCRIPTION

The TDA4470B is an integrated bipolar circuit for multistandard video/sound IF (VIF/SIF) signal processing in TV/VCR and multimed‹a applications. The circuit processes all TV video IF signals with negative modulation (e.g., B/G standard), positive modulation (e.g., L standard) and the AM, FM/NICAM sound IF signals.

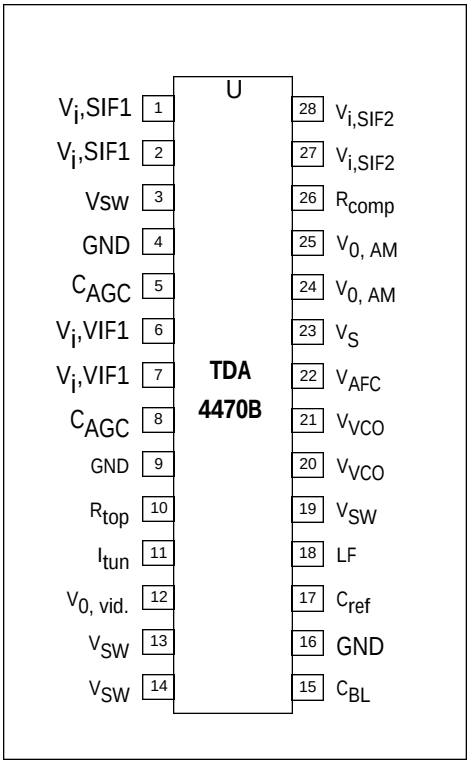
FEATURES

- 5 V supply voltage, low power consumption
- Active carrier generation by FPLL principle (frequency-phase-locked-loop) for true synchronous demodulation
- Very linear video demodulation, good pulse response and excellent intermodulation figures
- VCO circuit is operating on picture carrier frequency, the VCO frequency is switchable for the L` mode
- Alignment free AFC without external reference circuit, polarity of the AFC curve is switchable
- VIF AGC for negative modulated signals (peak sync. detection) and for positive modulation (peak white/black level detector)
- Tuner AGC with adjustable take over point
- Alignment free quasi parallel sound (QPS) mixer for FM/NICAM sound IF signals
- Intercarrier output signals is gain controlled (necessary for digital sound processing)
- Complete alignment-free AM demodulator with gain controlled AF output
- Separate SIF-AGC with average detection
- Two independent SIF inputs
- Parallel operation of the AM demodulator and QPS mixer (for NICAM L stereo sound)
- Package and relevant pinning is compatible with the single standard version TDA4472, which simplifies the design of an universal IF module

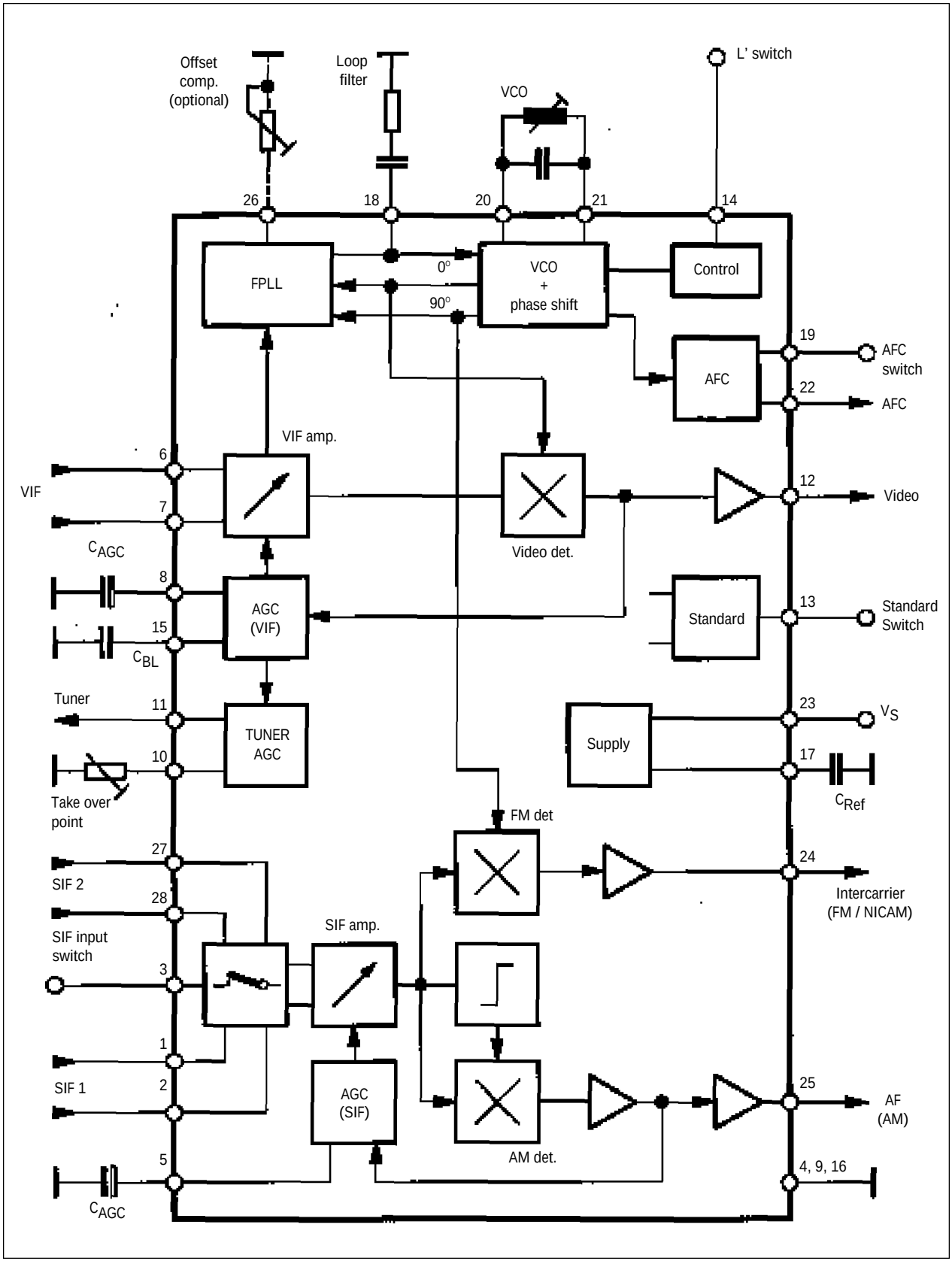
PINNING

Pin	Symbol	Function
1, 2	V_i,SIF1	SIF1 input (symmetrical)
3	Vsw	Input selector switch
4, 9,16	GND	Ground
5	C_{AGC}	SIF-AGC (time constant)
6, 7	V_i,VIF	VIF input (symmetrical)
8	C_{AGC}	VIF-AGC (time constant)
10	R_{top}	Take over point, tuner AGC
11	I_{tun}	Tuner AGC output current
12	V_0,vid	Video output
13	V_{SW}	Standard switch
14	V_{SW}	L' switch
15	C_{bi}	Black level capacitor
17	C_{ref}	Internal reference voltage
18	LF	Loop filter
19	V_{SW}	AFC switch
20.21	V_{VCO}	VCO circuit
22	V_{AFC}	AFC output
23	V_S	Supply voltage
24	$V_{0\text{-}FM}$	Intercarrier output
25	$V_{0\text{-}AM}$	AF output - AM sound
26	R_{comp}	Offset compensation
27, 28	$V_{i,\ SIF2}$	SIF2 input (symmetrical)

Pin Description



Block Diagram for TDA4470-B



CIRCUIT DESCRIPTION

Vision IF Amplifier

The video IF signal (VIF) is fed through a SAW filter to the differential input (Pin 6-7) of the VIF amplifier. This amplifier consists of three AC-coupled amplifier stages. Each differential amplifier is gain controlled by the automatic gain control (VIF-AGC). The output signal of the VIF amplifier is applied to the FPLL carrier generation and the video demodulator.

Tuner-and VIF-AGC

At Pin 8, the VIF-AGC charges/discharges the AGC capacitor to generate a control voltage for setting the gain of the VIF amplifier and tuner in order to keep the video output signal at a constant level. Therefore, in the case of all negative modulated signals (e.g., B/G standard) the sync. level of the demodulated video signal is the criterion for a fast charge/discharge of the AGC capacitor. For positive modulation (e.g., L standard) the peak white level of video signal controls the charge current. In order to reduce reaction time for positive modulation, where a large time constant is needed, an additional black level detector controls the discharge current in the event of decreasing VIF input signal. The control voltage (AGC voltage at Pin 8) is transferred to an internal control signal, and is fed to the tuner AGC to generate the tuner AGC current at Pin 11 (open collector output). The take over point of the tuner AGC can be adjusted at Pin 10 by a potentiometer or an external de voltage (from interface circuit or microprocessor).

FPLL,VCO and AFC

The FPLL circuit (frequency phase locked loop) consists of a frequency and phase detector to generate the control voltage for the VCO tuning. In the locked mode, the VCO is controlled by the phase detector and in unlocked mode, the frequency detector is superimposed. The VCO operates with an external resonance circuit (L and C parallel) and is controlled by internal varicaps. The VCO control voltage is also converted to a current and represents the AFC output signal at Pin 22. At the AFC switch (Pin 19) three operating conditions of the AFC are possible: AFC curve *"rising"* or *"falling"* and AFC "off'.

A practicable VCO alignment of the external coil is the adjustment to zero AFC output current at Pin 22. At center frequency the AFC output current is equal to zero. Furthermore. at Pin 14. the VCO center frequency can be switched for setting to the required L' value (L' standard).

The optional potentiometer at Pin 26 allows an offset compensation of the VCO phase for improved sound quality (fine adjustment). Without a potentiometer (open circuit at Pin 26). this offset compensation is not active.

The oscillator signal passes a phase shifter and supplies the in-phase signal (0°) and the quadrature signal (90°)of the generated picture carrier.

Video Demodulation and Amplifier

The video IF signal, which is applied from the gain controlled IF amplifier, is multiplied with the inphase component of the VCO signal. The video demodulator is designed for low distortion and large bandwidth. The demodulator output signal passes an integrated low pass filter for attenuation of the residual vision carrier and is fed to the video amplifier. The video amplifier is realized by an operational amplifier with internal feedback and 8 MHz bandwidth (-3 dB). A standard dependent de level shift in this stage delivers the same sync. level for positive and negative modulation. An additional noise clipping is provided. The video signal is fed to VIF-AGC and to the video output buffer. This amplifier with a 6 dB gain offers easy adaption of the sound trap. For nominal video

IF modulation the video output signal at Pin 12 is 2 V_{pp}.

Sound IF Amplifier and SIF-AGC

The SIF amplifier is nearly identical with the 3-stage VIF amplifier. Only the first amplifier stage exists twice and is switchable by a control voltage at Pin 3. Therefore with a minimal external expense it is possible to switch between two different SAW filters. Both SIF inputs features excellent cross-talk attenuation and an input impedance which is independent from the switching condition.

The SIF-AGC is related to the average level of AM- or FM-carrier and controls the SIF amplifier to provide a constant SIF signal to the AM demodulator and QPS mixer.

AM Demodulator

The alignment-free AM demodulator is realized by a synchronous detector. The modulated SIF signal from the SIF amplifier output is multiplied in phase with the limited SIF signal (AM is removed). The AF signal of the demodulator output is fed to the output amplifier and to the SIF-AGC. For all TV standards with negative video modulation (eg., B/G standard). the AF output signal (Pin 25) is switched off by the standard switch.

Quasi-Parallel-Sound (QPS) Mixer

The QPS mixer i~ realized by a multiplier. The signal (FM or NICAM carrier) is converted to the intercarrier frequency by the regenerated picture carrier frequency by the regenerated picture carrier (quadrature signal) which is provided from the VCO. The intercarrier signal is fed via an output amplifier to Pin 24.

Standard Switch

To have equal polarity of the video output signal the polarity can be switched in the demodulation stage in accordance with the TV standard. Additional a standard dependent de level shift in the video amplifier delivers the same sync. level. In parallel to this, the correct VIF-AGC is selected for positive or negative modulated VIF signals. In the case of negative modulation (e.g., B/G standard) the AM output signal is switched off. For positive modulation (L standard) the AM demodulator and QPS mixer is active. This condition allows a parallel operation of the AM sound signal and the NICAM-L stereo sound.

L'Switch

With a control voltage at Pin 14 the VCO frequency can be switched for setting to the required L' value (L' standard). Also a fine adjustment of the L'-VCO center frequency is possible via a potentiometer. The L' switch is only active for positive modulated video IF-signals (standard switch in L mode).

AFC Switch

The AFC output signal at Pin 22 can be controlled by a switching voltage at Pin 19. It is possible to select an AFC output signal with a rising-or falling AFC curve and to switch off the AFC.

VCR Mode

For the VCR mode in a TV set (external video source selected), it is recommendable to switch off the IF circuit. With an external switching voltage at Pin 6 or 7, the IF amplifiers are switched off and all signal output levels at Pins 12, 24, and 25 are according to the internal de voltage.

Internal Voltage Stabilizer

The internal bandgap reference ensures constant performance independent of supply voltage and temperature.

TDA9151B
Programmable Deflection Controller

GENERAL DESCRIPTION

The TDA9151B is a programmable deflection controller contained in a 20-pin DIP package and constructed using BIMOS technology.

This high performance synchronization and DC deflection processor has been especially designed for use in both digital and analog based TV receivers and monitors, and serves horizontal and vertical deflection functions for all TV standards.

The TDA9151B uses a line-locked clock at 6.75, 13.5 or 27 MHz, depending on the line frequency and application, and requires only a few external components. The device can be programmed in a self-adaptive mode or in a programmable fixed slope mode. Selection of these modes and a large number of other functions is fully programmable via the I^2C-bus.

FEATURES

General

- 6.75, 13.5 and 27 MHz clock frequency
- Few external components
- Synchronous logic
- I^2C-bus controlled
- Easy interfacing
- Low power
- ESD protection
- Flash detection with restart
- Two-level sandcastle pulse.

Vertical deflection

- 16-bit precision vertical scan
- Self adaptive or programmable fixed slope mode
- DC coupled deflection to prevent picture bounce
- Programmable fixed compression to 75%
- Programmable vertical expansion in the fixed slope mode
- S-correction can be preset
- S-correction setting independent of the field frequency
- Differential output for high DC stability
- Current source outputs for high EMC immunity
- Programmable de-interlace phase.

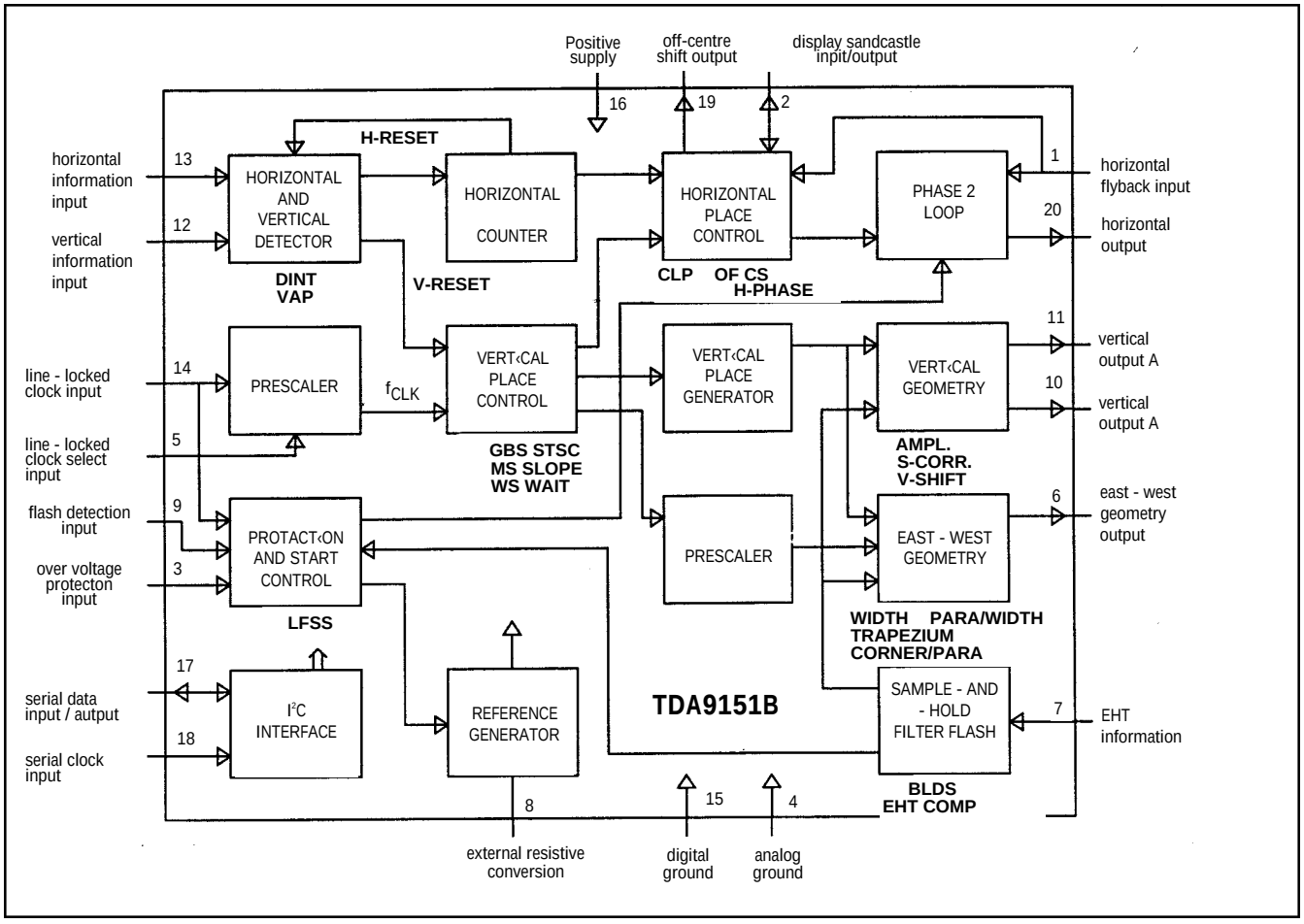
East-West correction

- DC coupled EW correction to prevent picture bounce
- 2nd and 4th order geometry correction can be preset
- Trapezium correction
- Geometry correction settings are independent of field frequency
- Self adaptive Bult generator prevents ringing of the horizontal deflection
- Current source output for high EMC immunity. Horizontal deflection
- Phase 2 loop with low litter
- Internal loop filter
- Dual slicer horizontal flyback input
- Soft start by I^2C-bus
- Over voltage protection/detection with selection and status bit.

EHT correction

- Input selection between aquadag or EHT bleeder
- Internal filter.

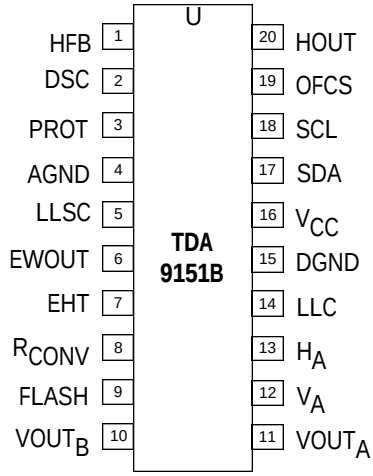
GENERAL DESCRIPTION



PINNING

Pin	Symbol	Function
1	HFB	horizontal flyback input
2	DSC	display sandcastle input/output
3	PROT	over voltage protection input
4	AGND	analog ground
5	LLSC	line-locked clock selection input
6	EWOUT	east-west geometry output
7	EHT	EHT compensation
8	R_{CONV}	external resistive conversion
9	FLASH	flash detection input
10	$VOUT_B$	vertical output B
11	$VOUT_A$	vertical output A
12	V_A	vertical information input
13	H_A	horizontal information input
14	LLC	line-locked clock input
15	DGND	digital ground
16	V_{CC}	supply input (+8V)
17	SDA	serial data input/output
18	SCL	serial clock input
19	OFCS	off-centre shift output
20	HOUT	horizontal output

Pin Description



FUNCTIONAL DESCRIPTION

Input signals (pins 12, 13, 14, 17 and 18)

The TDA9151B requires three signals for minimum operation (apart from the supply). These signals are the line-locked clock (LLC) and the two I²C-bus signals (SDA and SCL). Without the LLC the device will not operate because the internal synchronous logic uses the LLC as the system clock.

I²C-bus transmissions are required to enable the device to perform its required tasks. Once started the IC will use the HA and/or VA inputs for synchronization. If the LLC is not present the outputs will be switched off and all operations discarded (if the LLC is not present the line drive will be inhibited within 2 ms, the EW output current will drop to zero and the vertical output current will drop to 20% of the adjusted value within 100 ms). The SDA and SCL inputs meet the I2C-bus specification, the other three inputs are TTL compatible.

The LLC frequency can be divided-by-two internally by connecting LLCS (pin 5) to ground thereby enabling the prescaler.

The LLC timing is given in the Chapter "Characteristics".

Vertical part (pins 6, 8, 10, 11 and 12)

SYNCHRONIZATION PULSE

The V_A input (Pin 12) is a TTL-compatible CMOS input. Pulses at this input have to fulfil the timing requirements as illustrated in Fig.6. For correct detection the minimum pulse width for both the HIGH and LOW period is 2 internal clock periods. For further requirements on minimum pulse width see also Section "Deinterlace".

VERTICAL PLACE GENERATOR

An overview of the various modes of operation of the vertical place generator is illustrated in Fig.l3.

With control bit CPR a compress to 75% of the adjusted values is possible in all modes of operation. This control bit is used to display 16 : 9 standard pictures on 4 : 3 displays. No new adjustment of other corrections, such as corner and S-correction, is required.

With control bit VPR a reduction of the current during clipping, wait and stop modes to 20% of the nominal volue can be selected, which will reduce the dissipation in the vertical drive circuits.

Vertical place generator in adaptive mode (MS=logic 0).

The vertical start-scan data (subaddress 02) determines the vertical placement in the total range of 64 x 432 clock periods in 63 steps. The maximum number of synchronized lines per scan is 910 with an equivalent field frequency of 17.2 or 34.4 Hz for f_H = 15625 or 31250 Hz respectively.

The minimum number of synchronized lines per scan is 200 with an equivalent field frequency of 78 or 156 Hz for f_H = 15 625 or 31250 Hz respectively.

If the VA pulse is not present, the number of lines per scan will increase to 910.2. If the LLC is not present the vertical blanking will start within 2 µs.

Amplitude control is automatic, with a settling time of 1 to 2 new fields and an accuracy of either 16/12 or 48/12 lines depending on the value of the GBS bit.

Differences in the number of lines per field, as can occur in TXT or in multi-head VTR, will not affect the amplitude setting providing the differences are less than the value selected with GBS. This is called amplitude control guardband. This difference sequence and the difference sequence length are not important.

Vertical place generator in constant slope mode

(MS = logic I)

In this mode the slope can be programmed directly with a two byte value on subaddress 0C (MSB) and 0D (LSB). When the actual number of lines is greater than the programmed number of lines, the circuit will enter the stop state in which the differential vertical output current remains 100% or drops to 20% (programmable with control bit VPR). The programmed value for the slope is the required number of lines multiplied by 72. The programming limits are; minimum 200 x 72 and maximum 910 x 72.

A vertical expansion is obtained with a combination of slope data and a programmable wait status, at subaddress 0E. The wait status is selected with control bit MS and can only be activated in the constant slope mode. The wait state is an 8-bit value, programmable from 0 to 255. The actual wait state is one line longer than the programmed value. If blanking is applied during stop and wait status the differential output current will be the same with VPR selected value (20 or 100%).

DE-INTERLACE

With de-interlace on (DINT = logic 0), the V_A pulse is sampled with LLC at a position supplied by control bit DIP (de-interlace phase).

When DIP = logic 0 sampling takes place 42 clock pulses after the leading edge of H_A ($T = T_{line}$ x 42/432).

When DIP = logic 1 sampling takes place 258 clock pulses after the leading edge of H_A ($T = T_{line}$ x 258/432).

The distance between the two selectable sampling points is (T_{line} x (258 - 42)/432) which is exactly half a line, thus de-interlace is possible in two directions.

The duration of the VA pulse must, therefore, be sufficient to enable the HA pulse to caught, in this event an active time of minimum of half a line.

With de-interlace off, the V_A pulse is sampled with the system clock. The leading edge is detected and used as the vertical reset. Selection of the positive or negative leading edge is achieved by the control bit VAP.

Horizontal part (pins 1,2, 13, 19 and 20

SYNCHRONIZATION PULSE

The HA input (pin 13) is a TTL-compatible CMOS input. Pulses on this input have to fulfil the timing requirements as illustrated in Fig.6. For correct detection the minimum pulse width for both the HIGH and LOW periods is 2 internal clock periods.

FLYBACK INPUT PULSE

The HFB input (pin 1) is a CMOS input. The delay of the centre of the flyback pulse to the leading edge of the HA pulse can be set via the I²C-bus with the horizontal phase byte (subaddress 08) The resolution is 6-bit.

OUTPUT PULSE

The HOUT pulse (pin 20) is an open-drain NMOS output. The duty factor for this output is typically 52/48 (conducting/non-conducting) during normal operation. A soft start causes the duty factor to increase linearly from 5 to 52% over a minimum period of 2000 lines in 2000 steps.

OFF-CENTRE SHIFT

The OFCS output (pin 19) is a push-pull CMOS output which is driven by a pulse-width modulated DAC.

By using a suitable interface, the output signal can be used for off-centre shift correction in the horizontal output stage. This correction is required for HDTV tubes with a 16 x 9 aspect ratio and is useful for high performance flat square tubes to obtain the required horizontal linearity. For applications where off-centre correction is not required, the output can be used as an auxiliary DAC. The OFCS signal is phase-locked with the line frequency. The off-centre shift can be set via the I²C-bus, subaddress 09, with a 6-bit resolution as illustrated in Fig.8.

SANDCASTLE

The DSC input/output (pin 2) acts as a sandcastle generating output and a guard sensing input. As an output it provides 2 levels (apart from the base level), one for the horizontal and vertical blanking and the other for the video clamping. As an input it acts as a current sensor during the vertical blanking interval for guard detection.

CLAMPING PULSE

The clamping pulse width is 21 internal clock periods. The shift, with respect to HA can be varied from 35 to 49 clock periods in 7 steps via the I2C-bus, clamp shift byte subaddress 0A, as illustrated in Fig.9. It is possible to suppress the clamping pulse during wait, stop and protection modes with control bit CSU. This will avoid unwanted reset of the TDA4680/81 (only used in those circuits).

HORIZONTAL BLANKING

The start of the horizontal blanking pulse is minimum 38 and maximum 41 clock periods before the centre of the flyback pulse, depending on the f_{clk}/f_H ratio K in accordance with 41 - (432 - K).

Stop of the horizontal blanking pulse is determined by the trailing edge of the HFB pulse at the horizontal blanking slicing level.

VERTICAL BLANKING

The vertical blanking pulse starts two internal clock pulses after the rising edge of the VA pulse. During this interval a small guard pulse, generated during flyback by the vertical power output stage, must be inserted. Stop vertical blanking is effected at the end of the blanking interval only when the guard pulse is present (see Section "Vertical guard").

The start scan setting determines the end of vertical blanking with a 6-bit resolution in steps of one line via the I^2C-bus subaddress 02.

VERTICAL GUARD

In the vertical blanking interval a small unblanking pulse is inserted. This pulse must be filled-in by a blanking pulse or guard pulse from the vertical power output stage which was generated during the flyback period. In this condition the sandcastle output acts as guard detection input and requires a minimum 800 µA input current. This current is sensed during the unblanking period. Vertical blanking is only stopped at the end of the blanking interval when the inserted pulse is present. In this way the picture tube is protected against damage in the event of missing or malfunctioning vertical deflection

VERTICAL GEOMETRY PROCESSING

The vertical geometry processing is DC-coupled and therefore independent of field frequency. The external resistive conversion (RCONV) at pin 8 sets the reference current for both the vertical and EW geometry processing. A useful range is 100 to 150 µA, the recommended value is 120 µA.

VERTICAL OUTPUTS

The vertical outputs $VOUT_A$ and VOUTB on pins 10 and 11 together form a differential current output. The vertical amplitude can be varied over the range 80 to 120% in 63 steps via the I^2C-bus (subaddress 00). Vertical S-correction is also applied to these outputs and can be set from 0 to 16% by subaddress 01 with a 6-bit resolution.

The vertical off-centre shift (OFCS) shifts the vertical deflection current zero crossing with respect to the EW parabola bottom. The control range is -1.5 to +1.5% (±1/8 x I8) in 7 steps set by the least significant nibble at subaddress 03.

EW GEOMETRY PROCESSING

The EW geometry processing is DC coupled and therefore independent of field frequency. RCONV sets the reference current for both the vertical and EW geometry processing.

The EW output is an ESD-protected single-ended current output.

The EW width/width ratio can be set from 100 to 80% in 63 steps via subaddress 04 and the EW parabola/width ratio from 0 to 20% via subaddress 05. The EW corner/EW parabola ratio has a control range of -40 to 0% in 63 steps via subaddress 06.

The EW trapezium correction can be set from -1.5 to +1.5% in 7 steps via the most significant nibble at subaddress 03.

BULT GENERATOR

The Bult generator makes the EW waveform continuous.

Protection input (pin 3)

The protection input (PROT) is a CMOS input.

The input voltage must be EHT scaled and has the following characteristics:

Two modes of protection are available with the aid of control bit PRD.

- With PRD = logic 1 the protection mode is selected, HOUT will be defeated and the PROT bit in the status word is set if the input voltage is above 3.9 V. Thus the deflection stops and EW output current is zero, while the vertical output current is reduced to 20% of the adjusted value. A new start of the circuit is I^2C-bus controlled with the user software.
- With PRD = logic 0 the detection mode is selected, HOUT will not be defeated and the over voltage information is only written in the PROT status bit and can be read by the I^2C-bus.

All further actions, such as a write of the LFSS bit, are achieved by the I2C-bus. They depend on the configuration used and are defined by user software.

Flash detection/protection input (pin 9)

The FLASH input is a CMOS input with an internal pull-up current of approximately 8 µA.

When a negative-going edge crosses the 0.75 V level a restart will be executed with a soft start of approximately. 2000 lines, such as in the soft-start mode. When the function is not used pin 9 can be connected to ground, VCC or left open-circuit, the internal pull-up current source will prevent any problems. However a hard wired connection to VCC or ground is

recommended when the function is not used.

EHT compensation (pin 7)

The EHT input is a CMOS input.

The EHT compensation input permits scan amplitude modulation should the EHI supply not be perfect. For correct tracking of the vertical and horizontal deflection the gain of the EW output stage, provided by the ratio $R_{CONV-EW}/R_{CONV}$, must be 1/16 V_{scan} X V_{ref}.

The input for EHT compensation can be derived from an EHT bleeder or from the picture tubes aquadag (subaddress 0B, bit BLDS).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	Min.	Typ.	Max.	Unit
V_{CC}	supply voltage		7.2	8.0	8.8	V
I_{CC}	supply current	fclk= 6.75 MHz	-	27	-	mA
P_{tot}	total power dissipation	top sync-white	-	220	-	mW
T_{amb}	operating ambient temperature	top sync-whit	-25	-	+70	C°
Inputs						
V_{14}	line-locked clock (LLC) logic level		-	TTL	-	-
V_{13}	horizontal sync (H_A) logic level		-	TTL	-	-
V_{12}	vertical sync (V_A) logic level		-	TTL	-	-
V_5	line-locked clock select (LLCC) logic level	note 1	-	CMOS 5V	-	-
V_{18}	serial clock (SCL) logic level		-	CMOS 5V	-	-
V_{17}	serial data input (SDA) logic level		-	CMOS 5V	-	-
V_1	horizontal flyback (HFB) phase	FBL = logic 0	-	3.9	-	V
	slicing level	FBL = logic 1	-	1.3	-	V
V_1	horizontal flyback (HFB) blanking slicing level		-	100	-	mV
V_3	over voltage protection (PROT) level		-	3.9	-	V
V_9	EHT flash detection level		-	1.5	-	V
Outputs						
V_{20}	horizontal output (HOUT) voltage (open drain)	I_{20} = 10mA	-	-	0.5	V
I_{11}-$I_{10(M)}$	vertical differential ($VOUT_{A,B}$)	vertical amplitude =100%	440	475	510	µA
	output current (peak value)	I_8 = -120µA				
$V_{10,11}$	vertical output voltage		0	-	3.9	V
$I_{6(M)}$	EW (EWOUT) total output current (peak value)	I_8 = -120µA	-	-	930	µA
V_6	EW (EWOUT) output voltage		1.0	-	5.5	V
SANDCASTLE OUTPUT LEVELS (DSC)						
V_2	base voltage level		-	0.5	-	V
V_2	horizontal and vertical blanking voltage level		-	2.5	-	V
V_2	video blanking voltage leve		-	4.5	-	V
HORIZONTAL OFF-CENTRE SHIFT (OFCS)						
V_{19}	output voltage	I_{19} = 2 mA	0	-	V_{CC}	V

TDA8540
4x4 Video Switch Matrix

GENERAL DESCRIPTION

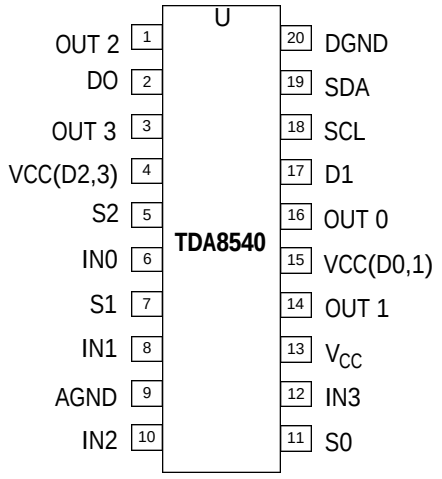
The TDA8540 has been designed for switching between composite video signals, therefore the minimum of four input lines are provided as requested for switching between two S-VHS sources. Each of the four outputs can be set to a high impedance state, to enable parallel connection of several devices.

PINNING

Pin	Symbol	Function
1	OUT2	video output 2
2	DO	control output 0
3	OUT 3	video output 3
4	$V_{CC(D2,3)}$	driver supply voltage; for drivers 2 and 3
5	S2	sub- address input 2
6	INO	video input 0 (CVBS or chrominance signal)
7	S1	sub- address input 1
8	IN1	video input 1 (CVBS or chrominance signal)
9	AGND	analog ground
10	IN2	video input 2 (CVBS or luminance signal)
11	S0	sub- address input 0
12	IN3	video input 3 (CVBS or luminance signal)
13	V_{CC}	general supply voltage
14	OUT1	video output 1
15	$V_{CC(D0,1)}$	driver supply voltage; for drivers 0 and 31
16	OUT0	video output 0
17	D1	control output 1
18	SCL	serial clock input
19	SDA	serial data input/output
20	DGND	digital ground

FEATURES

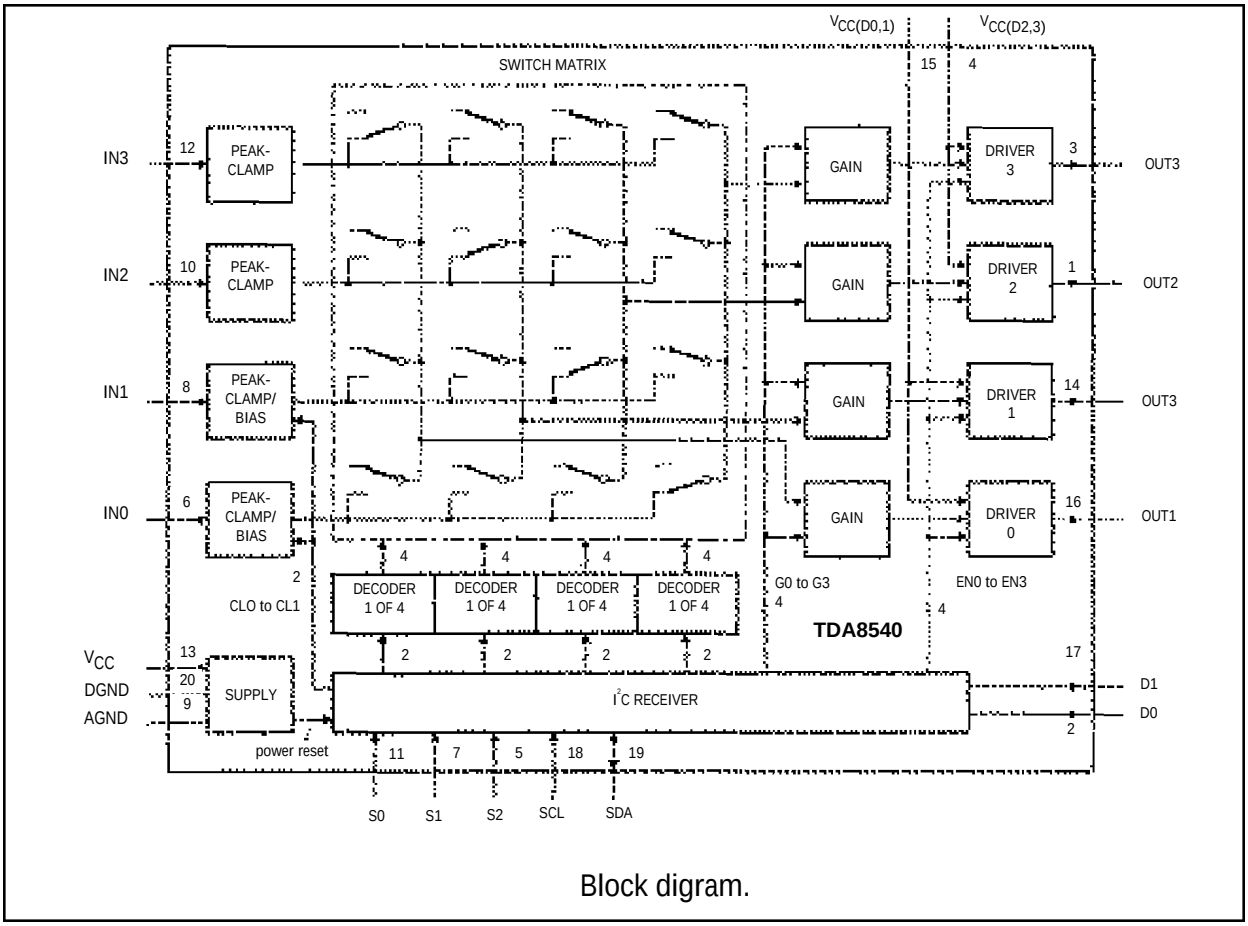
- I^2C-bus or non-I^2C-bus mode (controlled by DC voltages)
- S-VHS or CVBS processing
- 3-state switches for all channels
- Selectable gain for the video channels
- sub-address facility
- Slave receiver in the I^2C mode
- Auxiliary logic outputs for audio switching
- System expansion possible up to 7 devices (28 sources)
- Static short-circuit proof outputs
- ESD protection.



Pin Description

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	Min.	Typ.	Max.	Unit
V_{CC}	supply voltage		7.2	-	8.8	V
I_{CC}	supply current		-	20	30	mA
I_{SO}	isolation 'OFF' state	at f = 5 MHz	60	80	-	dB
B	3dB bandwith		12	-	-	MHz
α_{CT}	crosstalk attenuation between channels		60	70	-	dB



Block digram.

FUNCTIONAL DESCRIPTION

The TDA8540 is controlled via a bidirectional I²C-bus.3 bits of the I²C address can be selected via the address pin, thus providing a facility for parallel connection of 7 devices.

Control options via the I²C-bus:

- The input signals can be clamped at their negative peak (top sync).
- The gain factor of the outputs can be selected between 1x or 2x.
- Each of the four outputs can individually be connected to one of the four inputs.
- Each output can individually be set in a high impedance state.
- Two binary output data lines can be controlled for switching accompanying sound signals.

The SDA and SCL pins (pins 19 and 18)can be connected to the I²C-bus or to DC switching voltage sources. Address inputs S0 to S2 (pins 11, 7 and 5) are used to select sub-addresses or switching to the non-I²C mode. Inputs S0 to S2 can be connected to the supply voltage (HIGH) or the ground (LOW). In this way no peripheral components are required for selection.

I²C-Sus sub-addressing

S2	S1	S0	SUB-ADDRESS		
			A2	A1	AO
L	L	L	0	0	0
L	L	H	0	0	1
L	H	L	0	1	0
L	H	H	0	1	1
H	L	L	1	0	0
H	L	H	1	0	1
H	H	L	1	1	0
H	H	H	non I²C addressable		

I²C-bus control

After power-up the outputs are initialized in the high impedance state, and D0 and D1 are at a LOW level.

Detailed description of the I2C-bus specification, with applications, is given in brochure "The I2C-bus and how to use if': This brochure may be ordered using the code 9398 393 40011.

The TDA8540 is a slave receiver.

TDA8351

DC- Coupled Vertical Deflection Circuit

GENERAL DESCRIPTION

The TDA8351 is a power circuit for use in 90° and 110° colour deflection systems for field frequencies of 50 to120 Hz. The circuit provides a DC driven vertical deflection output circuit, operating as a highly efficient class G system .

FUNCTIONAL DESCRIPTION

The vertical driver circuit is a bridge configuration. The deflection coil is connected between the output amplifiers, which are driven in phase opposition. An external resistor (RM) connected in series with the deflection coil provides internal feedback information. The differential input circuit is voltage driven. The input circuit has been adapted to enable it to be used with the TDA9150A, TDA9151B, TDA9160A, TDA9162, TDA8366 and TDA8376 which deliver symmetrical current signals. An external resistor (RCON) connected between the differential input determines the output current through the deflection coil. The relationship between the differential input current and the output current is defined by: $I_{diff} \times R_{CON} = I_{coil} \times R_M$. The output current is adjustable from 0.5 A (p-p) to 3 A (p-p) by varying R_M. The maximum input differential voltage is 1.8 V. In the application it is recommended that $V_{dif}f$ = 1.5 V (typ), This is recommended because of the spread of input current and the spread in the value of R_{CON}

The flyback voltage is determined by an additional supply voltage V_{FB}. The principle of operating with two supply voltages (class G) makes it possible to fix the supply voltage V_p optimum for the scan voltage and the second supply voltage V_{FB} optimum for the flyback voltage. Using this method, very high efficiency is achieved.

The supply voltage V_{FB} is almost totally available as flyback voltage across the coil, this being possible due to the absence of a decoupling capacitor (not necessary, due to the bridge configuration). The output circuit is fully protected against the following:

- thermal protection
- short-circuit protection of the output pins (pins 4 and 7)
- short-circuit of the output pins to V_p.

A guard circuit VO(guard) is provided. The guard circuit is activated at the following conditions:

- during flyback
- during short-circuit of the coil and during short-circuit of the output pins (pins 4 and 7) to V_p or ground
- during open loop
- when the thermal protection is activated.

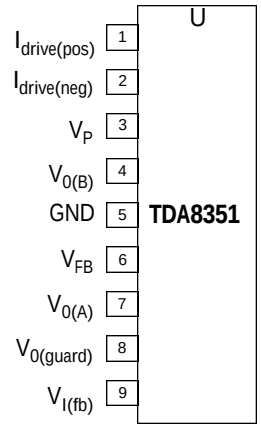
This signal can be used for blanking the picture tube screen.

FEATURES

- Few external components
- Highly efficient fully DC-coupled vertical output bridge circuit
- Vertical flyback switch
- Guard circuit
- Protection against:
  - short-circuit of the output pins (7 and 4)
  - short-circuit of the output pins to V_p
- Temperature (thermal) protection
- High EMC immunity because of common mode inputs
- A guard signal in zoom mode.

PINNING

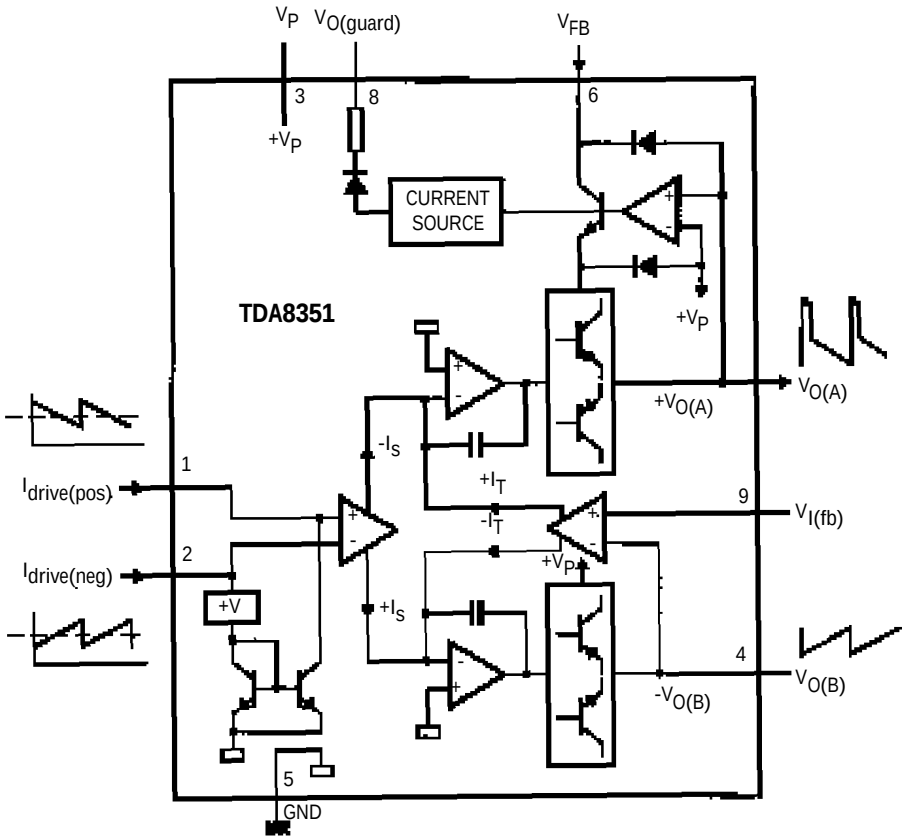
Pin	Symbol	Function
1	$I_{drive(pos)}$	input power-stage (positive); includes $I_{I(sb)}$ signal bias
2	$I_{drive(neg)}$	input power-stage (negative); includes $I_{I(sb)}$ signal bias
3	V_P	operating supply voltage
4	$V_{0(B)}$	output voltage B
5	GND	ground
6	V_{FB}	input flyback supply voltage
7	$V_{0(A)}$	output voltage A
8	$V_{0(guard)}$	guard output voltage
9	$V_{I(fb)}$	input feedback voltage



Pin Configuration

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	Min.	Typ.	Max.	Unit
DC supply						
V_P	supply voltage		9	-	25	V
I_q	quiescent supply current		-	30	-	mA
Vertical circuit						
$I_{O(p-p)}$	output current (peak-to-peak value)		-	-	3	A
$I_{diff(p-p)}$	differential current (peak-to-peak value)		-	600	-	µA
$V_{diff(p-p)}$	differential input voltage (peak-to-peak value)		-	1.5	1.8	V
Flyback switch						
I_M	peak output current		-	-	±1.5	A
V_{FB}	flyback supply voltage		-	-	50	V
		note 1	-	-	60	V
Thermal data (in accordance with IEC 747-1)						
T_{stg}	storage temperature		-55	-	+150	°C
T_{amb}	operating ambient temperature		-25	-	+75	°C
T_{vj}	virtual junction temperature		-	-	150	°C



Block diagram

TDA9875A
Digital TV Sound Processor (DTVSP)

GENERAL DESCRIPTION

The TDA9875A is a single-chip Digital TV Sound Processor (DTVSP) for analog and digital multi-channel sound systems in TV sets and satellite receivers.

Supported standards

The multistandard/multi-stereo capability of the TDA9875A is mainly of interest in Europe, but also in Hong Kong/Peoples Republic of China and South East Asia. This includes B/G, D/K, I, M and L standard. In other application areas there exists only subsets of those standard combinations otherwise only single standards are transmitted.

M standard is transmitted in Europe by the American Forces Network (AFN) with European channel spacing (7 MHz VHF, 8 MHz UHF) and monaural sound.

The AM sound of L/L' standard is normally demodulated in the 1 st sound IF. The resulting AF signal has to be entered into the mono audio input of the TDA9875A. A second possibility is to use the internal AM demodulator stage, however this gives limited performance.

Korea has a stereo sound system similar to Europe and is supported by the TDA9875A. Differences include deviation, modulation contents and identification. It is based on M standard.

An overview of the supported standards and sound systems and their key parameters is given in Table B

The analog multi-channel sound systems (A2, A2+ and A2*) are sometimes also named 2CS (2 carrier systems).

FEATURES

Demodulator and decoder section

- Sound IF (SIF) input switch e.g. to select between terrestrial TV SIF and SAT SIF sources
- SIF AGC with 24 dB control range
- SIF 8-bit Analog-to-Digital Converter (ADC)
- DQPSK demodulation for different standards, simultaneously with i-channel FM demodulation
- NICAM decoding (B/G, I and L standard)
- Two-carrier multistandard FM demodulation (B/G, D/K and M standard)
- Decoding for three analog multi-channel systems (A2, A2+ and A2*) and satellite sound
- Optional AM demodulation for system L, simultaneously with NICAM
- Programmable identification (B/G, D/K and M standard) and different identification times.

DSP section

- Digital crossbar switch for all digital signal sources and destinations
- Control of volume, balance, contour, bass, treble, pseudo stereo, spatial, bass boost and soft-mute
- Plop-free volume control
- Automatic Volume Level (AVL) control
- Adaptive de-emphasis for satellite
- Programmable beeper
- Monitor selection for FM/AM DC values and signals, with peak detection option
- I^2S-bus interface for a feature extension (e.g. Dolby surround) with matrix, level adjust and mute.

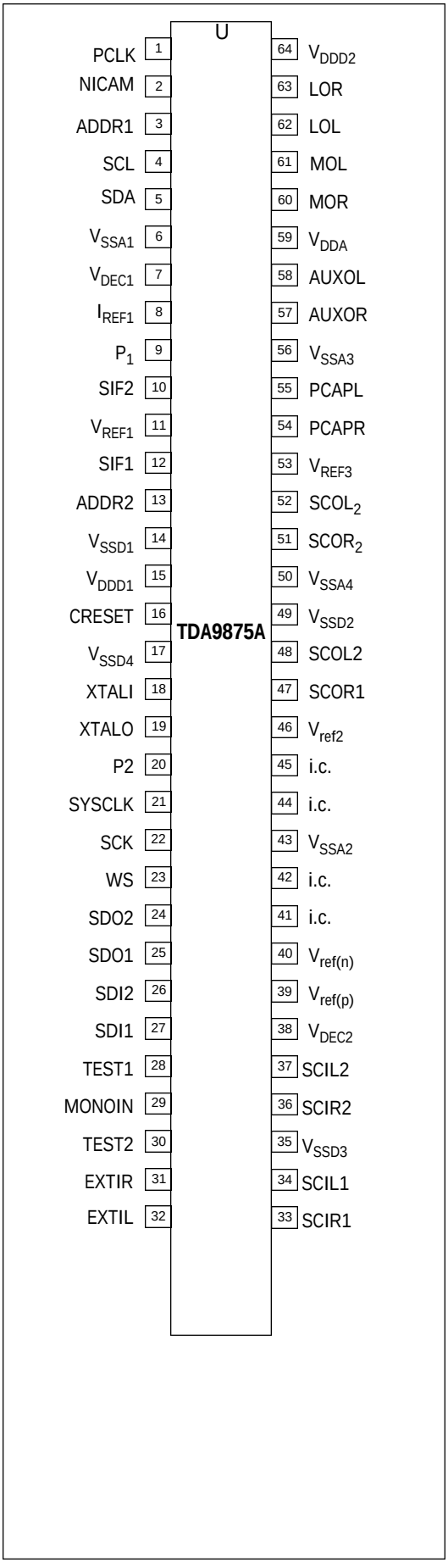
Analog audio section

- Analog crossbar switch with inputs for mono and stereo (also applicable as SCART 3 input), SCART 1 input/output, SCART 2 input/output and line output
- User defined full-level/-3 dB scaling for SCART outputs
- Output selection of mono, stereo, dual A/B, dual A or dual B
- 20 kHz bandwidth for SCART-to-SCART copies
- Standby mode with functionality for SCART copies
- Dual audio digital-to-analog converter from DSP to analog crossbar switch, bandwidth 15 kHz
- Dual audio ADC from analog inputs to DSP
- Two dual audio Digital-to-Analog Converters (DACs) for loudspeaker (Main) and headphone (Auxiliary) outputs; also applicable for L, R, C and S in the Dolby Pro Logic mode with feature extension.

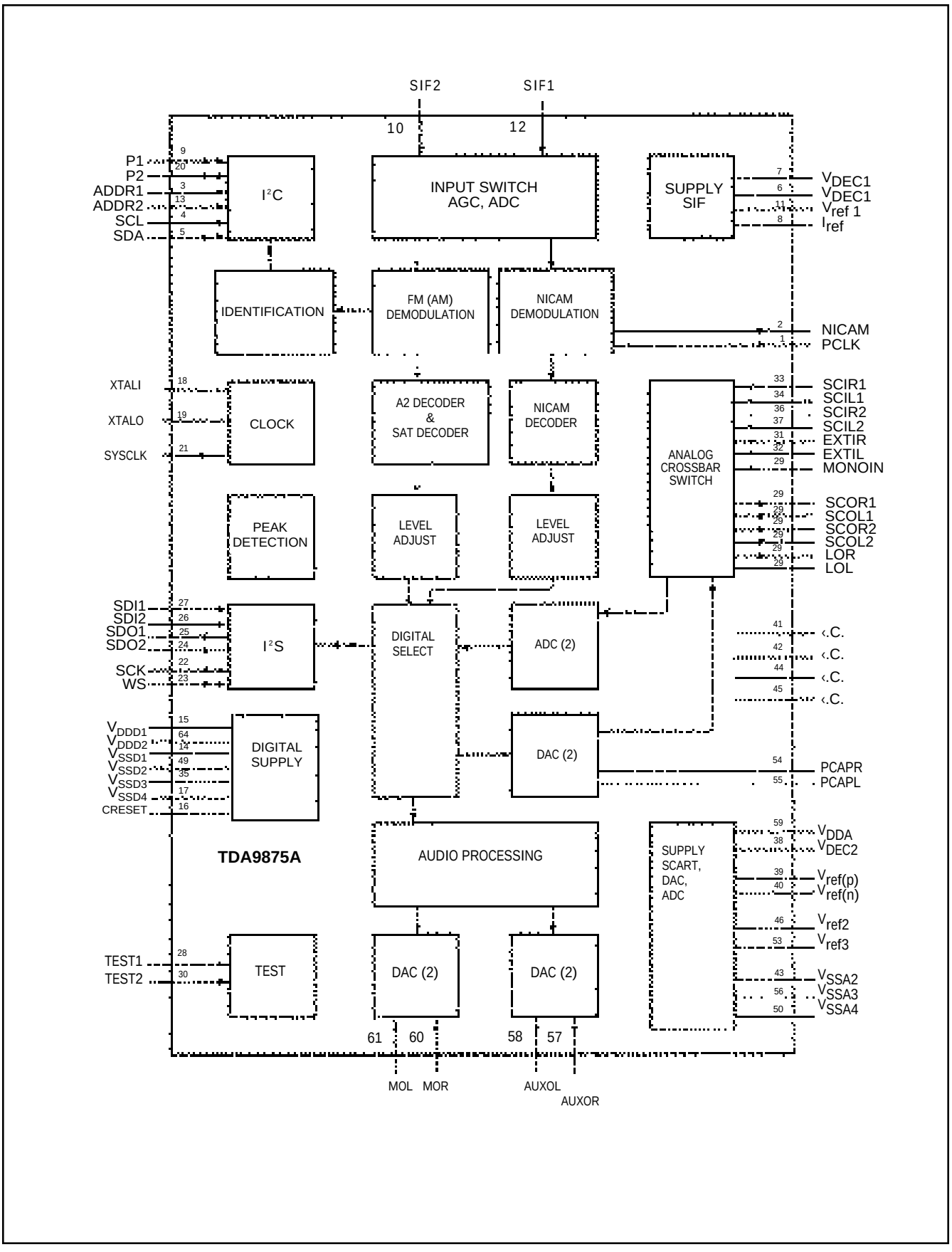
PINNING

SYMBOL	PIN	I/O	DESCRIPTION
PCLK	1	O	NICAM clock output at 728 kHz
NICAM	2	O	serial NICAM data output at 728 kHz
ADDR1	3	I	first I^2C-bus slave address modifier
SCL	4	I	I^2C-bus clock
SDA	5	I/O	I^2C-bus data
V_{SSA1}	6	supply	supply ground 1; analog front-end circuitry
V_{DEC1}	7	-	positive power supply voltage 1 decoupling; analog front-end circuitry
I_{REF1}	8	-	resistor for reference current generator; analog front-end circuitry
P_1	9	I/O	first general purpose I/O pin
SIF2	10	I	sound IF input 2
V_{REF1}	11	-	reference voltage; analog front-end circuitry
SIF1	12	I	sound IF input 1
ADDR2	13	I	second I^2C-bus slave address modifier
V_{SSD1}	14	supply	supply ground 1; digital circuitry
V_{DDD1}	15	supply	digital supply voltage 1; digital circuitry
CRESET	16	-	capacitor for power-on reset
V_{SSD4}	17	supply	supply ground 4; digital circuitry
XTALI	18	I	crystal oscillator input
XTALO	19	O	crystal oscillator output
P2	20	I/O	second general purpose I/O pin
SYSCLK	21	O	system clock output
SCK	22	I/O	I^2C-bus clock
WS	23	I/O	I^2C-bus word select
SDO2	24	O	I^2C-bus data output 2
SDO1	25	O	I^2C-bus data output 1
SDI2	26	I	I^2C-bus data input 2
SDI1	27	I	I^2C-bus data input 1
TEST1	28	I	first test pin; connected to V_{SSD1} for normal operation
MONOIN	29	I	audio mono input
TEST2	30	I	second test pin; connected to V_{SSD1} for normal operation
EXTIR	31	I	external audio input right channel
EXTIL	32	I	external audio input left channel
SCIR1	33	I	SCART 1 input right channel
SCIL1	34	I	SCART 1 input left channel
V_{SSD3}	35	supply	supply ground 3; digital circuitry
SCIR2	36	I	SCART 2 input right channel
SCIL2	37	I	SCART 2 input left channel
V_{DEC2}	38	-	positive power supply voltage 2 decoupling; audio analog-to-digital converter circuitry
$V_{ref(p)}$	39	-	positive reference voltage; audio analog-to-digital converter circuitry
$V_{ref(n)}$	40	-	reference voltage ground; audio analog-to-digital converter circuitry
i.c.	41	-	internal connected; note 1
i.c.	42	-	internal connected; note 2
V_{SSA2}	43	supply	supply ground 2, audio analog-to-digital converter circuitry
i.c.	44	-	internal connected; note 2
i.c.	45	-	internal connected; note 1
V_{ref2}	46	-	reference voltage; audio analog-to-digital converter circuitry
SCOR1	47	O	SCART 1 output right channel

SYMBOL	PIN	I/O	DESCRIPTION
SCOL2	48	O	SCART 1 output left channel
V_{SSD2}	49	supply	supply ground 2; digital circuitry
V_{SSA4}	50	supply	supply ground 4; audio operational
			amplifier circuitry
$SCOR_2$	51	O	SCART 2 output right channel
$SCOL_2$	52	O	SCART 2 output left channel
V_{REF3}	53	-	reference voltage; audio digital-to-analog converter and operational amplifier circuitry
PCAPR	54	-	post-filter capacitor pin right channel, audio digital-to-analog converter
PCAPL	55	-	post-filter capacitor pin left channel, audio digital-to-analog converter
V_{SSA3}	56	supply	supply ground 3; audio digital-to-analog converter circuitry
AUXOR	57	O	headphone (Auxiliary) output right channel
AUXOL	58	O	headphone (Auxiliary) output left channel
V_{DDA}	59	supply	positive analog power supply voltage;
			analog circuitry
MOR	60	O	loudspeaker (Main) output right channel
MOL	61	O	loudspeaker (Main) output left channel
LOL	62	O	line output left channel
LOR	63	O	line output right channel
V_{DDD2}	64	supply	digital supply voltage 2; digital circuitry



BLOCK DIAGRAM



ANALOG 2- CARRIER SYSTEMS

Table B- Frequency modulation

STANDARD	SOUND SYSTEM	CARRIER FREQUENCY (MHZ)	FM DEVIATION (kHz) NOM./MAX./OVER	MODULATION		BANDWIDTH/ DE-EMPHASIS (kHz/µs)
				SC1	SC2	
M	mono	4.5	15/25/50	mono	-	15/75
M	A2+	4.5/4.724	15/25/50	1/2(L + R)	1/2(L - R)	15/75 (Korea)
B/G	A2	5.5/5.742	27/50/80	1/2(L + R)	R	15/50
I	mono	6.0	27/50/80	mono	-	15/50
D/K	A2	6.5/6.742	27/50/80	1/2(L + R)	R	15/50
D/K	A2*	6.5/6.258	27/50/80	1/2(L + R)	R	15/50

Table C- identification for A2 systems

PARAMETER	A2/A2*	A2+ (KOREA)
Pilot frequency	54.6875 kHz = 3.5 x line frequency	55.0699 kHz = 3.5 x line frequency
Stereo identification frequency	117.5 Hz = $\frac{\text{line frequency}}{133}$	149.9 Hz = $\frac{\text{line frequency}}{105}$
Dual identification frequency	274.1 Hz = $\frac{\text{line frequency}}{57}$	276.0 Hz = $\frac{\text{line frequency}}{57}$
AM modulation depth	50%	50%

2- CARRIER SYSTEMS WITH NICAM

Table D- NICAM

STANDARD	MODULATION				SC2 (MHz) NICAM	DE-EMPHASIS	ROLL-OFF (%)	NICAM CODING
	FREQUENCY (MHZ)	TYPE	MODULATION					
			INDEX (%) NOM./MAX	DEVIATION (kHz) NOM./MAX				
B/G	5.5	FM	-	27/50	5.85	J17	40	note 1
I	6.0	FM	-	27/50	6.552	J17	100	note 1
DK	6.5	FM	-	27/50	5.85	J17	40	note 2
L	6.5	AM	54/100	-	5.85	J17	40	note 1

SATELLITE SYSTEMS

An important specification for satellite TV reception is the "Astra specification". The TDA9875A is suited for the reception of Astra and other satellite signals.

Table E- FM satellite sound

CARRIER TYPE	CARRIER FREQUENCY (MHZ)	MODULATION INDEX	MAXIMUM FM DEVIATION (kHz)	MODULATION	BANDWIDTH/ DE-EMPHASIS (kHz/µs)
Main	6.50[1]	0.26	85	mono	15/50[1]
Sub	7.02/7.20	0.15	50	m/st/d[2]	15/adaptive[3]
Sub	7.38/7.56	0.15	50	m/st/d[2]	15/adaptive[3]
Sub	7.74/7.92	0.15	50	m/st/d[2]	15/adaptive[3]
Sub	8.10/8.28	0.15	50	m/st/d[2]	15/adaptive[3]

FUNCTIONAL DESCRIPTION

Description of the demodulator and decoder section

1- SIF INPUT

Two input pins are provided, SIF1 e.g. for terrestrial TV and SIF2 e.g. for a satellite tuner. For higher SIF signal levels the SIF input can be attenuated with an internal switchable -10 dB resistor divider. As no specific filters are integrated, both inputs have the same specification giving flexibility in application. The selected signal is passed through an AGC circuit and then digitized by an 8-bit ADC operating at 24.576 MHz.

2- AGC

The gain of the AGC amplifier is controlled from the ADC output by means of a digital control loop employing hysteresis. The AGC has a fast attack behaviour to prevent ADC overloads and a slow decay behaviour to prevent AGC oscillations. For AM demodulation the AGC must be switched off. When switched off, the control loop is reset and fixed gain settings can be chosen from Table 15 (subaddress 0).

The AGC can be controlled via the I²C-bus. Details can be found in the I²C-bus register definitions .(see Chapter 10).

3- MIXER

The digitized input signal is fed to the mixers, which mix one or both input sound carriers down to zero IF. A 24-bit control word for each carrier sets the required frequency. Access to the mixer control word registers is via the I²C-bus. When receiving NICAM programs, a feedback signal is added to the control word of the second carrier mixer to establish a carrier-frequency loop.

4- FM AND AM DEMODULATION

An FM or AM input signal is fed via a band-limiting filter to a demodulator that can be used for either FM or AM demodulation. Apart from the standard (fixed) de-emphasis characteristic, an adaptive de-emphasis is available for encoded satellite programs. A stereo decoder recovers the left and right signal channels from the demodulated sound carriers. Both the European and Korean stereo systems are supported.

5- FM IDENTIFICATION

The identification of the FM sound mode is performed by AM synchronous demodulation of the pilot signal and narrow-band detection of the identification frequencies. The result is available via the I²C-bus interface. A selection can be made via the I²C-bus for B/G, D/K and M standard and for three different modes that represent different trade-offs between speed and reliability of identification.

6- NICAM DEMODULATION

The NICAM signal is transmitted in a DQPSK code at a bit rate of 728 kbit/s. The NICAM demodulator performs DQPSK demodulation and feeds the resulting bitstream and clock signal onto the NICAM decoder and, for evaluation purposes, to PCLK (pin 1)and NICAM (pin 2).

A timing loop controls the frequency of the crystal oscillator to lock the sampling rate to the symbol timing of the NICAM data.

7- NICAM DECODER

The device performs all decoding functions in accordance with the *"EBU NICAM 728 specification"*. After locking to the frame alignment word, the data is descrambled by applying the defined pseudo-random binary sequence; the device will then synchronize to the periodic frame flag bit C0.

The status of the NICAM decoder can be read out from the NICAM status register by the user (see the I²C-bus register description in Section 10.4.2). The OSB bit indicates that the decoder has locked to the NICAM data. The VDSP bit indicates that the decoder has locked to the NICAM data and that the data is valid sound data. The C4 bit indicates that the sound conveyed by the FM mono channel is identical to the sound conveyed by the NICAM channel. The error byte contains the number of sound sample errors, resulting from parity checking, that occurred in the past 128 ms period. The Bit Error Rate (BER) can be calculated using the following equation; bit error

$$BER = \frac{\text{bit errors}}{\text{total bits}} = \text{error byte} \times 1.74 \times 10^{-5}$$

8- NICAM AUTO-MUTE

This function is enabled by setting bit AMUTE LOW subaddress 14 (see Section 10.3.11). Upper and lower error limits may be defined by writing appropriate values to two registers in the I²C-bus section (subaddresses 16 and 17; see Sections 10.3.13 and 10.3.14). When the number of errors in a 128 ms period exceeds the upper error limit the auto-mute function will switch the output sound from NICAM to whatever sound is on the first sound carrier (FM

or AM). When the error count is smaller than the lower error limit the NICAM sound is restored.

The auto-mute function can be disabled by setting bit AMUTE HIGH. In this condition clicks become audible when the error count increases; the user will hear a signal of degrading quality.

A decision to enable/disable the auto-muting is taken by the microcontroller based on an interpretation of the application control bits C1, C2, C3 and C4 and, possibly, any additional strategy implemented by the set maker in the microcontroller software.

For NICAM L applications, it is recommended to demodulate AM sound in the first sound IF and connect the audio signal to the mono input of the TDA9875A. By setting the AMSEL bit subaddress 14 (see Section 10.3.11), the auto-mute function will switch to the audio ADC instead of switching to the first sound carrier.

The ADC source selector subaddress 23 (see Section 10.3.20) should be set to mono input, where the AM sound signal should be connected.

9- CRYSTAL OSCILLATOR

The digital-controlled crystal oscillator (DCXO) is illustrated in Fig.8 (see Chapter 12). The circuitry of the DCXO is fully integrated, only the external 24.576 MHz crystal is needed.

10- TEST PINS

Both test pins are active HIGH, in normal operation of the device they are wired to V_{SSD1}. Test functions are for manufacturing tests only and are not available to customers. Without external circuitry these pads are pulled down to LOW level with internal resistors.

11- POWER-ON RESET FLIP-FLOP

The power-on reset flip-flop monitors the internal power supply for the digital part of the device. If the supply has temporary been lower than the specified lower limit, the power-on reset bit POR, transmitter register subaddress 0 (see Section 10.4.1), will be set to HIGH. The CLRPOR bit, slave register subaddress 1 (see Section 10.3.2), resets the power-on reset flip-flop to LOW. If this is detected, an initialization of the TDA9875A has to be carried out to ensure reliable operation.

TDA2616

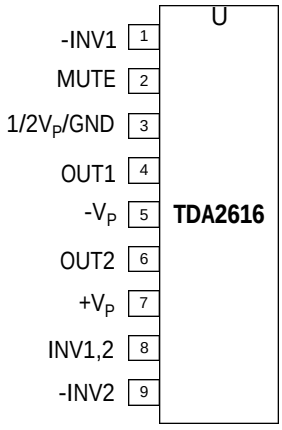
2x12W Hi-Fi Audio Power Amplifiers with Mute

GENERAL DESCRIPTION

The TDA2616 is a dual power amplifiers. It has been especially designed for mains fed applications such as stereo radio and stereo TV.

FEATURES

- Requires very few external components
- No switch-on/switch-off clicks
- Input mute during switch-on and switch-off
- Low offset voltage between output and ground
- Excellent gain balance of both amplifiers
- Hi-Fi accordance with IEC 268 and DIN 45500
- Short-circuit proof and thermal protected
- Mute possibility.



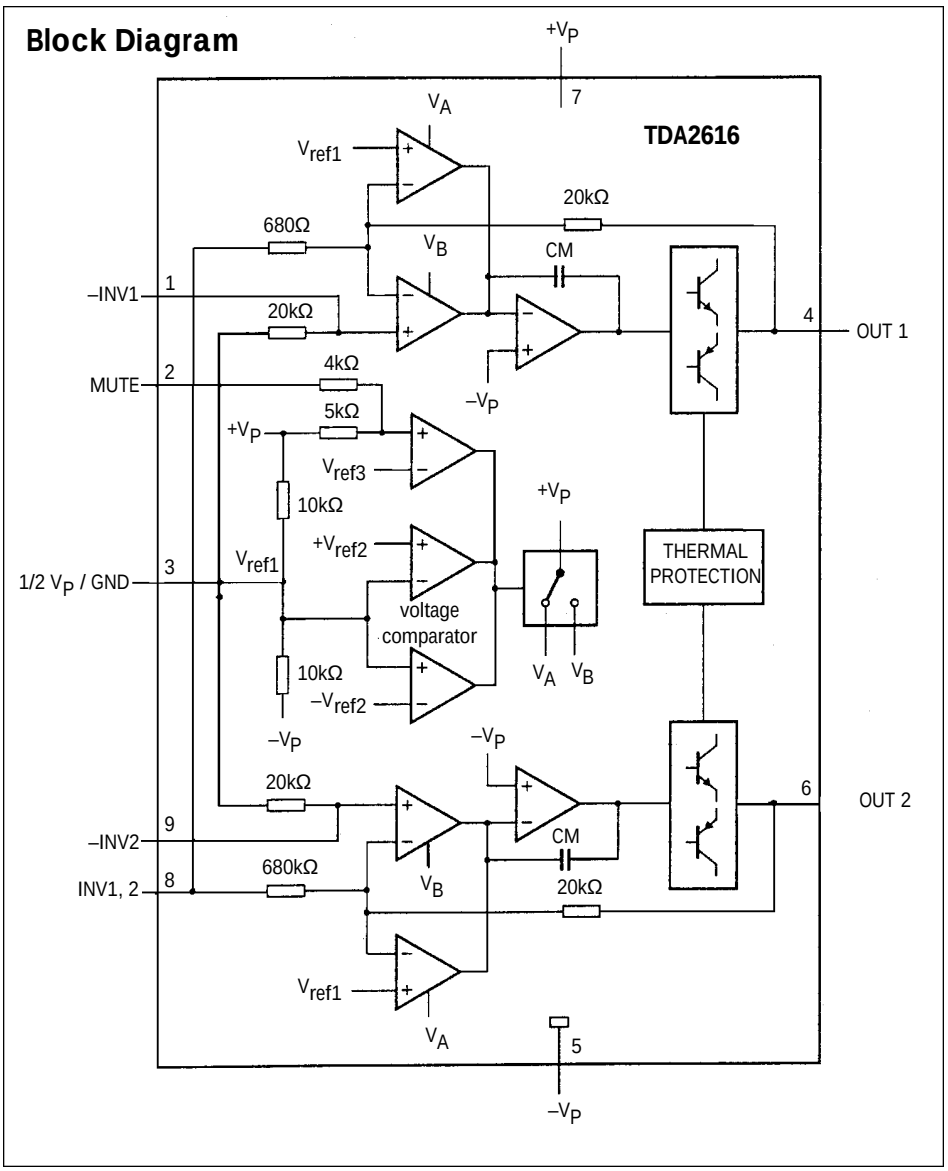
Pin Configuration

PINNING

Pin	Symbol	Function
1	-INV1	non-inverting input 1
2	MUTE	mute input
3	$1/2V_P$/GND	1/2 supply voltage or ground
4	OUT1	output 1
5	$-V_P$	supply voltage (negative)
6	OUT2	output 2
7	$+V_P$	supply voltage (positive)
8	INV1,2	inverting inputs 1,2
9	-INV2	non-inverting input 2

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	Min.	Typ.	Max.	Unit
$\pm V_P$	supply voltage range		7.5	-	21	V
P_O	output power	V_P = ±16V; THD = 0.5%	-	12	-	W
G_V	internal voltage gain		-	30	-	dB
$\lvert G_V \rvert$	channel unbalance		-	0.2	-	dB
α	channel separation		-	70	-	dB
SVRR	supply voltage ripple rejection		-	60	-	dB
V_{no}	noise output voltage		-	70	-	µV



FUNCTIONAL DESCRIPTION

The TDA2616 is a hi-fi stereo amplifier designed for mains fed applications, such as stereo radio and TV. The circuit is optimally designed for symmetrical power supplies, but is also well-suited to asymmetrical power supply systems.

An output power of 2 x 12 W (THD = 0.5%) can be delivered into an 8 Ω load with asymmetrical power supply of ±16 V. The gain is internally fixed at 30 dB, thus offering a low gain spread and a very good gain balance between the two amplifiers (0.2 dB).

A special feature is the input mute circuit. This circuit disconnects the non-inverting inputs when the supply voltage drops below ±6 V, while the amplifier still retains its DC operating adjustment. The circuit features suppression of unwanted signals at the inputs, during switch-on and switch-off.

The mute circuit can also be activated via pin 2. When a current of 300 µA is present at pin 2, the circuit is in the mute condition.

The device is provided with two thermal protection circuits. One circuit measures the average temperature of the crystal and the other measures the momentary temperature of the power transistors. These control circuits attack at temperatures in excess of +150 °C, so a crystal operating temperature of max. +150 °C can be used without extra distortion. With the derating value of 2.5 K/W, the heatsink can be calculated as follows:

at R_L = 8 Ω and V_p = ±16 V. the measured maximum dissipation is 14.6 W.

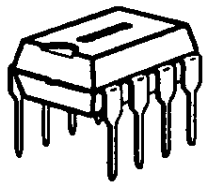
With a maximum ambient temperature of +65 °C, the thermal resistance of the heatsink is:

$$R_{th} = \frac{150 - 65}{14.6} - 2.5 = 3.3 \text{ K/W}.$$

The internal metal block has the same potential as Pin 5.

TDA4605-3
Control IC for SMPS

FEATURES
- Fold-back characteristics provides overload protection for external components
- Burst operation under secondary short-circuit condition implemented
- Protection against open or a short of the control loop
- Switch-off if line voltage is too low (undervoltage switch-off)
- Line voltage depending compensation of fold-back point
- Soft-start for quiet start-up without noise generated by the transformer
- Chip-over temperature protection implemented (thermal shutdown)
- On-chip ringing suppression circuit against parasitic oscillations of the transformer
- AGC-voltage reduction at low load



P-DIP-8-1

The IC TDA 4605-3 controls the MOS-power transistor and performs all necessary control and protection functions in free running flyback converters. Because of the fact that a wide load range is achieved, this IC is applicable for consumer as well as industrial power supplies.

The serial circuit and primary winding of the flyback transformer are connected in series to the input voltage. During the switch-on period of the transistor, energy is stored in the transformer. During the switch-off period the energy is fed to the load via the secondary winding. By varying switch-on time of the power transistor, the IC controls each portion of energy transferred to the secondary side such that the output voltage remains nearly independent of load variations. The required control information is taken from the input voltage during the switch-on period and from a regulation winding during the switch-off period. A new cycle will start if the transformer has transferred the stored energy completely into the load.

In the different load ranges the switched-mode power supply (SMPS) behaves as follows:

No load operation
The power supply is operating in the burst mode at typical 20 to 40 kHz. The output voltage can be

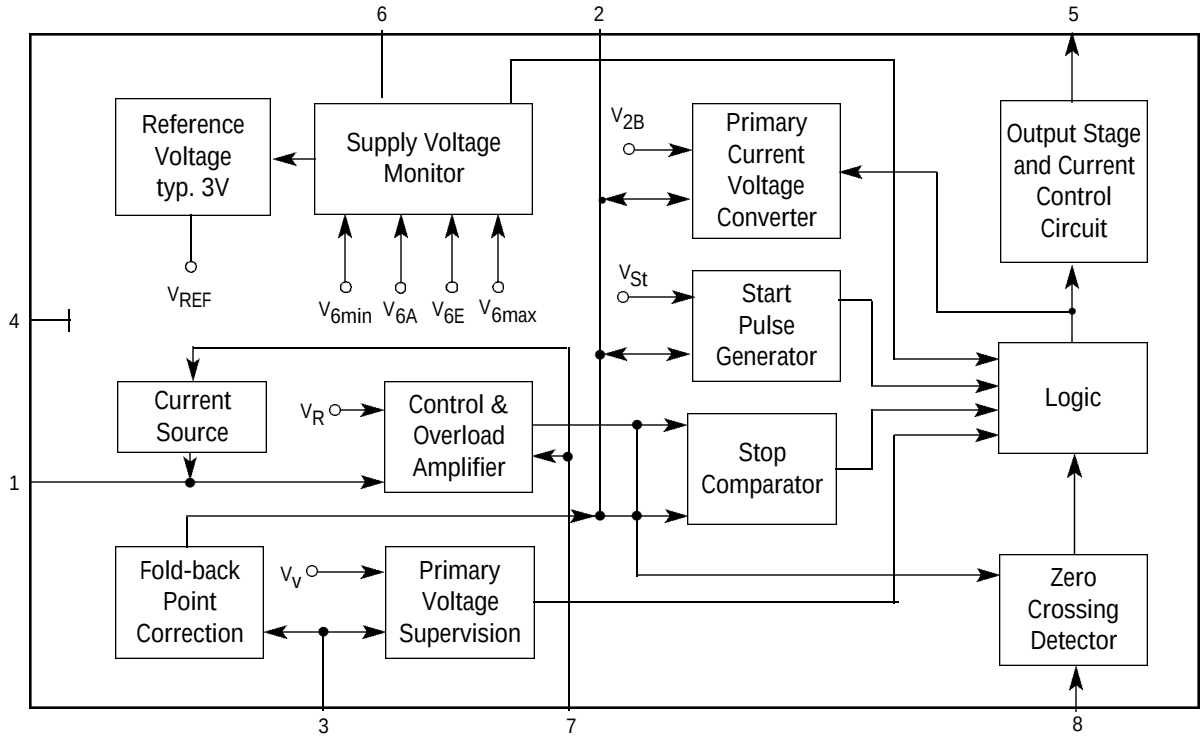
a little bit higher or lower than the nominal value depending of the design of the transformer and the resistors of the control voltage divider.

Nominal operation
The switching frequency is reduced with increasing load and decreasing AC-voltage.

The output voltage is only dependent on the load.

Overload point
Maximal output power is available at this point of the output characteristic.

Overload
The energy transferred per operation cycle is limited at the top. Therefore the output voltages declines by secondary overloading.



Pin Definitions and Functions

Pin No.	Function
1	**Information Input Concerning Secondary Voltage** By comparing the regulating voltage - obtained trom the regulating winding of the transformer - with the internal reference voltage, the output impulse width on pin 5 is adjusted to the load of the secondary side (normal, overload, short-circuit, no load).
2	**Information Input Regarding the Primary Current** The primary current rise in the primary winding is simulated at pin 2 as a voltage rise by means of external RC-element. When a voltage level is reached thats derived from the regulating voltage at pin 1, the output impulse at pin 5 is terminated. The RC-element serves to set the maximum power at the overload point set.
3	**Input for Primary Voltage Monitoring** In the normal operation $V3$ is moving between the thresholds V_{3H} and V_{3L} ($V_{3H} > V_3 > V_{3L}$). $V_3 < V_{3L}$: SMPS is switched OFF (line voltage too low). $V_3 > V_{3H}$: Compensation of the overload point regulation (controlled by pin 2) starts at $V_{3H} : V_{3L} = 1.7$.
4	**Ground**
5	**Output** Push-pull output provides ±1 A for rapid charge and discharge of the gate capacitance of the power MOS-transistor.
6	**Supply Voltage Input** A stable internal reference voltage V_{REF} is derived from the supply voltage also the switching thresholds V_{6A}, V_{6E}, V_6 max and V_6 min for the supply voltage detector. If $V_6 > V_{6E}$ then V_{REF} is switched on and switched off when $V_6 < V_{6A}$ - In addition the logic is only enable for V_6 min < V_6 < $V_{6\ max}$.
7	**Input for Soft-Start** Start-up will begin with short pulses by connecting a capacitor from pin 7 to ground.
8	**Input for the Oscillation Feedback** After starting oscillation, every zero transition of the feedback voltage (falling edge) through zero (failing edge) triggers an output pulse at pin 5. The trigger threshold is at + 50 mV typical.

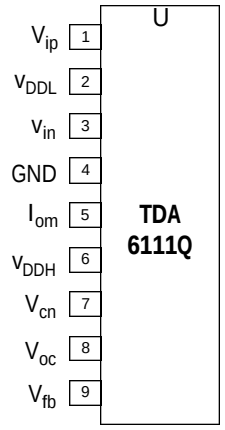
TDA6111Q
Video Output Amplifier

FEATURES
- High bandwidth and high slew rate
- Black-current measurement output for Automatic Black-current Stabilization (ABS)
- Two cathode outputs; one for DC currents, and one for transient currents
- A feedback output separated from the cathode outputs
- Internal protection against positive appearing Cathode-Ray Tube (CRT) flashover discharges
- ESD protection
- Simple application with a variety of colour decoders
- Differential input with a designed maximum common mode input capacitance of 3 pF, a maximum differential mode input capacitance of 0.5 pF and a differential input voltage temperature drift of 50 µV/K
- Defined switch-off behaviour.

GENERAL DESCRIPTION
The TDA6111Q is a video output amplifier with 16 MHz bandwidth. The device is contained in a single in-line 9-pin medium power (DBSSMPF) package, using high-voltage DMOS technology, intended to drive the cathode of a colour CRT.

PINNING

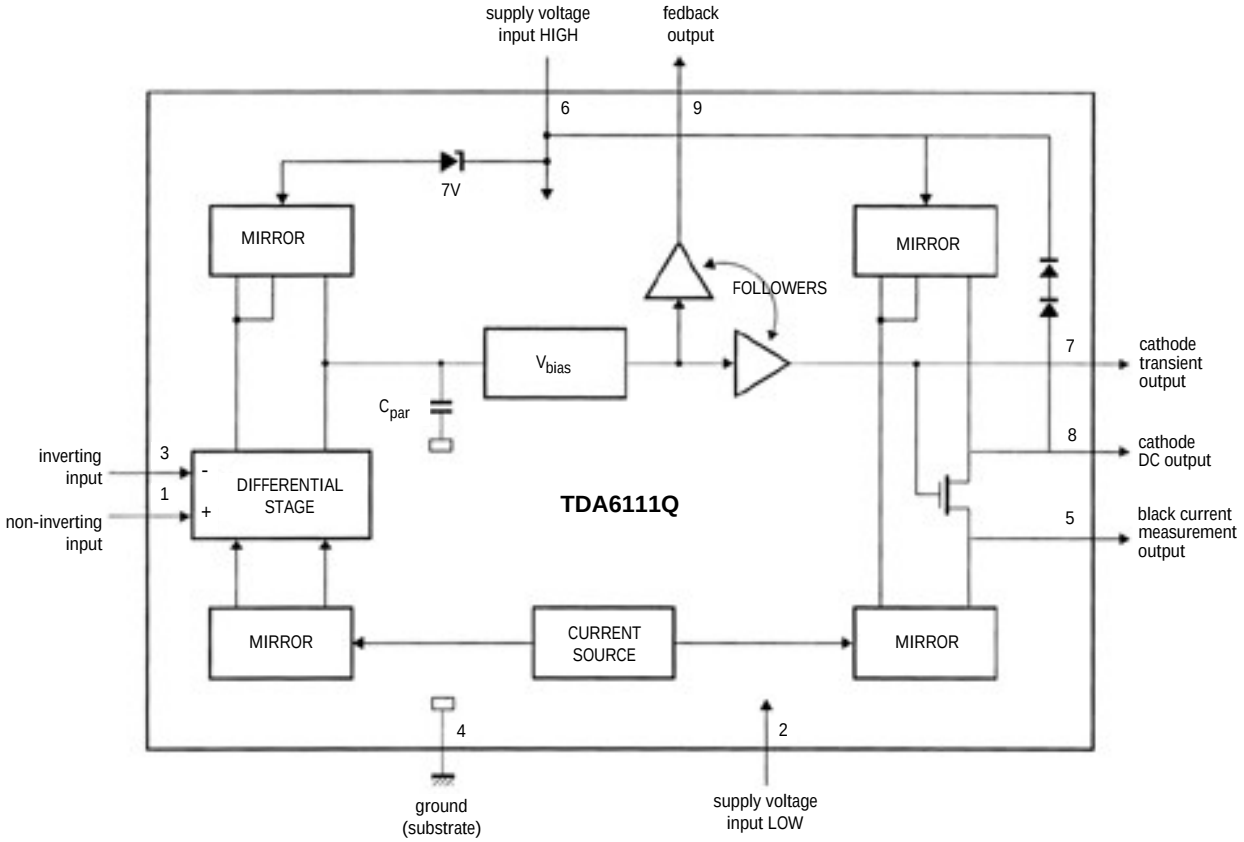
Pin	Symbol	Function
1	V_{ip}	non - inverting voltage input
2	v_{DDL}	supply voltage LOW
3	v_{in}	inverting voltage input
4	GND	ground, substrate
5	I_{om}	black current measurement output
6	v_{DDH}	supply voltage HIGH
7	V_{cn}	cathode transient voltage output
8	V_{oc}	cathode DC voltage output
9	V_{fb}	feedback voltage output



Pin Configuration

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	Min.	Typ.	Max.	Unit
v_{DDH}	high level supply voltage		0	-	250	V
v_{DDL}	low levelsupply voltage		0	-	14	W
I_{DDH}	quiescent high voltage supply current	$V_{oc} = 0.5V_{DDH}$	7.0	9.0	11.0	mA
I_{DDL}	quiescent low voltage supply current	$V_{oc} = 0.5V_{DDH}$	5.0	6.8	8.0	mA
V_i	input voltage		0	-	V_{DDL}	V
V_{oc}, V_{fb}	output voltage		V_{DDL}	-	V_{DDH}	V
T_{stg}	storage temperature		-55	-	+150	°C
T_{amb}	operating ambient temperature		-20	-	+65	°C



A-Block diagram

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134). Voltages measured with respect to GND (pin 4); currents as specified in A; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	Min.	Max.	Unit
v_{DDH}	high level supply voltage		0	250	V
v_{DDL}	low levelsupply voltage		0	14	W
V_i	input voltage		0	V_{DDL}	V
V_{IDM}	differential mode input voltage		-6	+6	V
V_{om}	measurement output voltage		0	V_{DDL}	
V_{oc}	cathode output voltage		V_{DDL}	V_{DDH}	V
V_{fb}	feedback output voltage		V_{DDL}	V_{DDH}	V
I_{in}, I_{ip}	input current		0	1	mA
I_{cosmL}	low-non repetitive peak cathode output current	flashover discharge = 100µC	0	5	A
I_{cosmH}	high-non repetitive peak cathode output current	flashover discharge = 100nC	0	10	A
P_{tot}	total power dissipation		0	4	W
T_{stg}	storage temperature		-55	+150	°C
T_j	junction temperature		-20	+150	°C
V_{es}	electrostatic handling human body model (HBM) machine model (MM)		 - -	 >1500 >400	 V V

Cathode output

The cathode output is protected against peak currents (caused by positive voltage peaks during high-resistance flash) of 5 A maximum with a charge content of 100 µC.

The cathode is also protected against peak currents (caused by positive voltage peaks during low-resistance flash) of 10 A maximum with a charge content of 100 nC.

Flashover protection

The TDA6111Q incorporates protection diodes against CRT flashover discharges that clamp the cathode output pin to the V_{DDH} pin. The DC supply voltage at the V_{DDH} Pin has to be within the operating range of 180 to 210 V to ensure that the Absolute Maximum Rating for V_{DDH} of 250 V will not be exceeded during flashover. To limit the diode current, an external 680 R carbon high-voltage resistor in series with the cathode output and a 2 kV spark gap are needed (for this resistor-value, the CRT has to be connected to the main PCB). This addition produces an increase in the rise and fall times of approximately 5 ns and a decrease in the overshoot of approximately 4%.

V_{DDH} to GND must be decoupled:

1. With a capacitor >20 nF with good HF behaviour (e.g. foil). This capacitance must be placed as close as possible to pins 6 and 4, but definitely within 5 mm.
2. With a capacitor >10 CIF on the picture tube base print (common for three output stages).

V_{DDL} to GND must be decoupled:

1. With a capacitor >20 nF with good HF behaviour (e.g. ceramic). This capacitance must be placed as close as possible to pins 2 and 4, but definitely within 10 mm.

Switch-off behaviour

The switch-off behaviour of the TDA6111Q is defined: when the bias current becomes zero, at V_{DDL} (pin 2) lower than approximately 5 V, all the output pins (pins 7, 8 and 9) will be high.

M27C2001

2 Megabit (256 kx8) UV EPROM

FEATURES

- Fast access time: 55ns
- Low Power "CMOS" Consumption:
  - Active Current: 30 mA
  - Standby Current 100 µA
- Programming voltage: 12.75V
- Electronic signature for Automated programming
- Programming times of around 24 sec. (Presto II algorithm)

FDIP32W (F)

DESCRIPTIONS

The M27C2001 is a high speed 2 Megabit UV erasable and electrically programmable EPROM ideally suited for microprocessor systems requiring large programs. It is organised as 262, 144 by 8 bits.

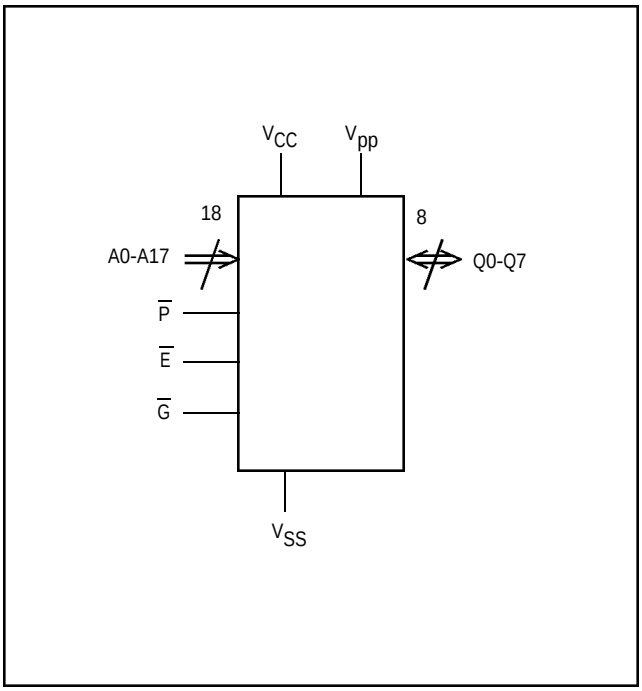
The Window Ceramic Frit-Seal Dual-in-Line and Leadless Chip Carrier packages have transparent lids which allow the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

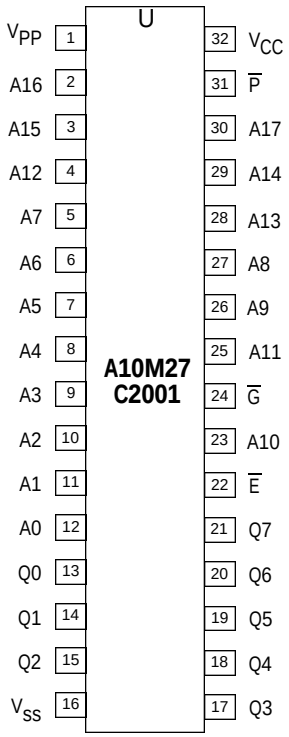
For applications where the content is programmed only one time and erasure is not required, the M27C2001 is offered in both Plastic Leaded Chip Carrier and Plastic Thin Small Outline packages.

SIGNAL NAMES

A0 - A17	address ›nputs
Q0 - Q7	data outputs
$\overline{E}$	chip enable
$\overline{G}$	output enable
$\overline{P}$	program
Vpp	program supply
Vcc	supply voltage
Vss	ground

Figure 1. Logic Diagram





Pin Connections

DEVICE OPERATION

The modes of operations of the M27C2001 are listed in the Operating Modes table. A single power supply is required in the read mode. All inputs are TTL levels except for V_{pp} and 12V on A9 for Electronic Signature.

Read Mode

The M27C2001 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable (E) is the power control and should be used for device selection. Output Enable (%) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, the address access time (t_{AVQV}) is equal to the delay from E to output (t_{ELQV}). Data is available at the ou~put after a delay of t_{GLQV} from the falling edge of G, assuming that E has been low and the addresses have been stable for at least t_{AVQV}-t_{GLQV}.

Standby Mode

The M27C2001 has a standby mode which reduces the active current from 30mA to 100µA. The M27C2001 is placed in the standby mode by applying a CMOS high signal to the E input. When in the standby mode, the outputs are in a high impedance state, independent of the G input.

Two Line Output Control

Because EPROMs are usually used in larger memory arrays, this product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows:

a- the lowest possible memory power dissipation,

b- complete assurance that output bus contention will not occur.

For the most efficient use of these two control lines, E should be decoded and used as the primary device selecting function, while G should be made a common connection to all devices in the array and connected to the READ line from the system control bus. This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is required from a particular memory device.

System Consideration

The power switching characteristics of Advanced CMOS EPROMs require careful decoupling of the devices. The supply current, Icc, has three segments that are of interest to the system designer : the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of E. The magnitude of the transient current peaks is dependent on the capacitive and inductive loading of the device at the output.

The associated transient voltage peaks can be suppressed by complying with the two line output

control and by properly selected decoupling capacitors. It is recommended that a 0.1µF ceramic capacitor be used on every device between Vee and Vss. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7µF bulk electrolytic capacitor should be used between Vee and Vss for every eight devices. The bulk capacitor should be located near the power supply connection point.The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	VALUE	Unit
T_A	ambient operating temperature	40 to 125	°C
T_{BIAS}	temperature under bias	50 to 125	°C
T_{stg}	storage temperature	65 to 150	°C
V_{IO}(2)	input or output voltage (except A9)	2 to 7	V
v_{CC}	supply voltage	2 to 7	V
v_{A9}(2)	A9 voltage	2 to 13.5	V
V_{PP}	program supply voltage	2 to 14	V

1 Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings'" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the SGS-THOMSON SURE Program and other relevant quality documents.

2. Minimum DC voltage on Input or Output is 0.5V with possible undershoot to 2.0V for a period less than 20ns. Maximum DC voltage on Output is V_{CC}+0.5V with possible overshoot to V_{CC} + 2V for a period less than 20ns.

AC MEASUREMENT CONDITIONS

	HIGH SPEED	STANDARD
Input Rise and Fall Times	≤10ns	≤20ns
Iput Pulse Voltage	0 to 3 V	0.4 V to 2.4 V
Input and Output Timing Ref. Voltages	1.5 V	0.8 V and 2 V

OPERATING MODES

Mode	$\overline{E}$	$\overline{G}$	$\overline{P}$	A9	V_{PP}	Q0-Q7
Read	V_{IL}	V_{IL}	x	x	V_{CC} or V_{SS}	Data Out
Output disable	V_{IL}	V_{IL}	x	x	V_{CC} or V_{SS}	Hi-Z
Program	V_{IL}	V_{IL}	V_{IL} Pulse	x	V_{PP}	Data In
Verify	V_{IL}	V_{IL}	V_{IH}	x	V_{PP}	Data Out
Program Inhibit	V_{IH}	x	x	x	V_{PP}	Hi-Z
Standby	V_{IH}	x	x	x	V_{CC} or V_{SS}	Hi-Z
Electronic Signature	V_{IL}	V_{IL}	V_{IH}	V_{ID}	V_{CC}	Codes

Note: x = V_{IH} or V_{IL}, V_{ID}= 12V ±0.5V

ST24C16
Serial 16K (2Kx8) EEPROM

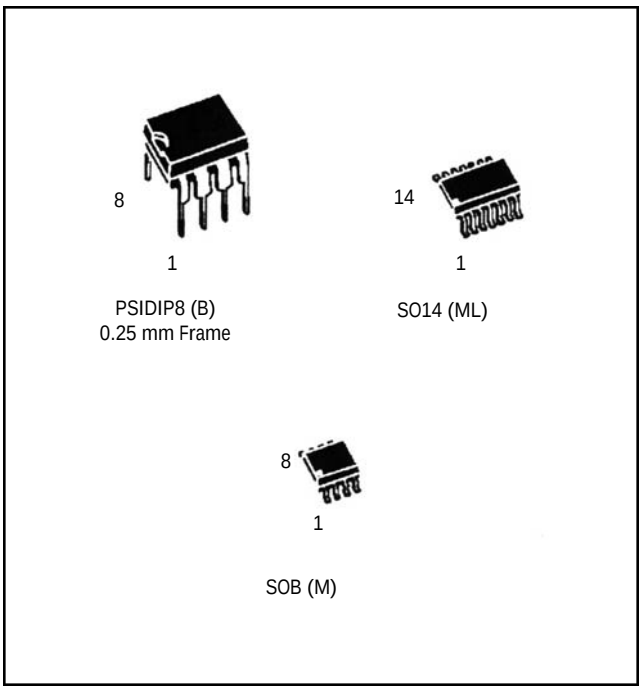
FEATURES
- 1million erase / write cycles, with 10 years data retention
- Single supply voltage:
  - -4.5V to 5.5V for ST24x16 versions
  - - 2.5V to 5.5V for ST25x16 versions
- Hardware write control versions: ST24W16 and ST25W16
- Two wire serial interface, fully I²Cbus compatible
- Byte and multibyte write (up to 8 bytes) for the ST24C16
- Page write (up to 16 bytes)
- Byte, random and sequential read modes
- Self timed programming cycle
- Automatic address incrementing
- Enhanced ESD/Latch up performances

DESCRIPTION

This specification covers a range of 16K bits I²C bus EEPROM products, the ST24/25C16 and the ST24/25W16. In the text, products are referred to as ST24/25x16 where "X" is: "C" for Standard version and "W" for hardware Write Control version.

The ST24/25x16 are 16K bit electrically erasable programmable memories (EEPROM), organized as 8 blocks of 256x8 bits. These are manufactured in SGS-THOMSON's Hi-Endurance Advanced CMOS technology which guarantees an endurance of one million erase/write cycles with a data retention of 10 years. The ST25x16 operates with a power supply value as low as 2.5V. Both Plastic Dual-in-Line and Plastic Small Outline packages are available.

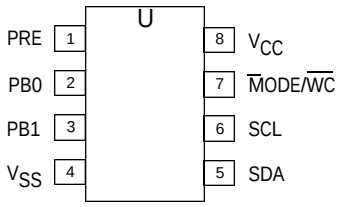
The memories are compatible with the I²C standard, two wire serial interface which uses a bi-directional data bus serial clock. The memories carry a built-in 4 bit, unique device identification. The memories behave as slave devices in the I²C protocol with all memory operations synchronized by the serial clock. Read and write operations are initiated by a START condition generated by the bus master. The START condition is followed by a stream of 4 bits (identification code 1010), 3 block select bits, plus one read/write bit and terminated by an acknowledge



SIGNAL NAMES

PRE	write protect enable
PB0, PB1	protect block select
$\overline{S}$DA	serial data address input/output
$\overline{S}$CL	serial clock
$\overline{M}$ODE	Multybyte/page write mode (C version)
WC	write control (W version)
V_{cc}	supply voltage
V_{ss}	ground

ST24x16
ST25x16



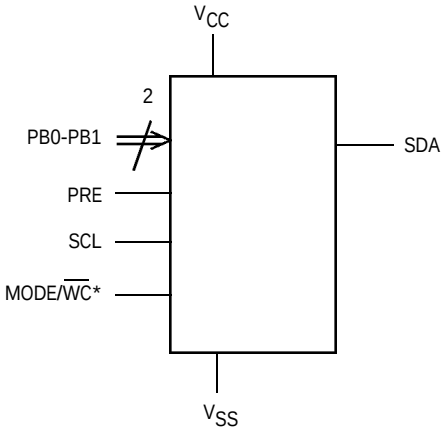
DIP Pin Connections

bit.When writing data to the memory it responds to the 8 bits received by asserting an acknowledge bit during the 9th bit time. When data is read by the bus master, it acknowledges the receipt of the data bytes in the same way. Data transfers are terminated with a STOP condition .

Data in the 4 upper blocks of the memory may be write protected. The protected area is programma-ble to start on any 16 byte boundary. The block in which the protection starts is selected by the input pins PB0, PBI. Protection is enabled by setting a Protect Flag bit when the PRE input pin is driven High.

Power On Reset: Vcc lock out write protect. In order to prevent data corruption and inadvertent write operations during power up, a Power On Reset (POR) circuit is implemented. Until the V_{CC} voltage has reached the POR threshold value, the internal reset is active: all operations are disabled and the device will not respond to any command. In the same way, when V_{CC} drops down from the operating voltage to below the POR threshold value, all operations are disabled and the device will not respond to any command. A stable V_{CC} must be applied before applying any logic signal.

Logic Diagram



Note: WC signal is only available for ST24/25W16 products.

SAA7710T

Dolby Pro Logic Surround; Dolby 3 stereo; Incredible Sound

GENERAL DESCRIPTION

This specification describes the 104 ROM-code version of the SAA7710T chip. The SAA7710T chip is a high quality audio-performance digital add-on processor for digital sound systems. It provides all the necessary features for complete Dolby Pro Logic surround sound on chip.

In addition to the Dolby Pro Logic surround function, this device also incorporates a 3-band parametric equalizer, a 5-band parametric equalizer, a tone control section and a volume control. Instead of Dolby Pro Logic surround, the Hall/matrix surround and Incredible sound functions can be used together with the equalizer or tone control.

FEATURES

- Two stereo I²S-bus digital input channels
- Three stereo I²S-bus digital output channels
- I²C-bus mode control
- Up to 45 ms on-chip delay-line (f_S = 44.1 kHz)
- Optional clock divider for crystal oscillator
- Package: SO32L
- Operating supply voltage range: 4.5 to 5.5 V.

Functions

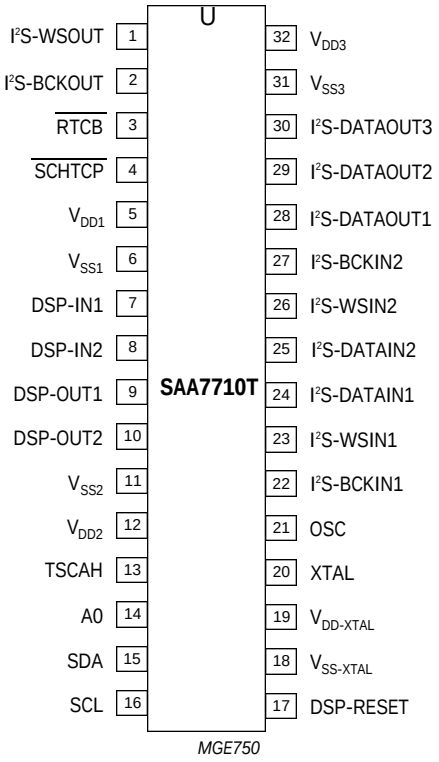
- 4-channel active surround, 20 Hz to 20 kHz (maximum i/$_2f_S$)
- Adaptive matrix
- 7 kHz low-pass filters
- Adjustable delay for surround channel
- Modified Dolby B noise reduction
- Noise sequencer
- Variable output matrix
- Sub woofer
- Centre mode control: on/off, normal, phantom, wide
- Output volume control
- Automatic balance and master level control with DC-offset filter
- Hallimatrix surround sound functions
- Incredible sound functions
- 8-band parametric equalizer on main channels left, centre, right (f_S = 44.1 kHz)
- 5-band parametric equalizer on main channels left, centre, right (f_S = 32 kHz)
- Tone control (bass/treble) on all four output channels (f_S = 44.1 kHz).

QUICK REFERENCE DATA

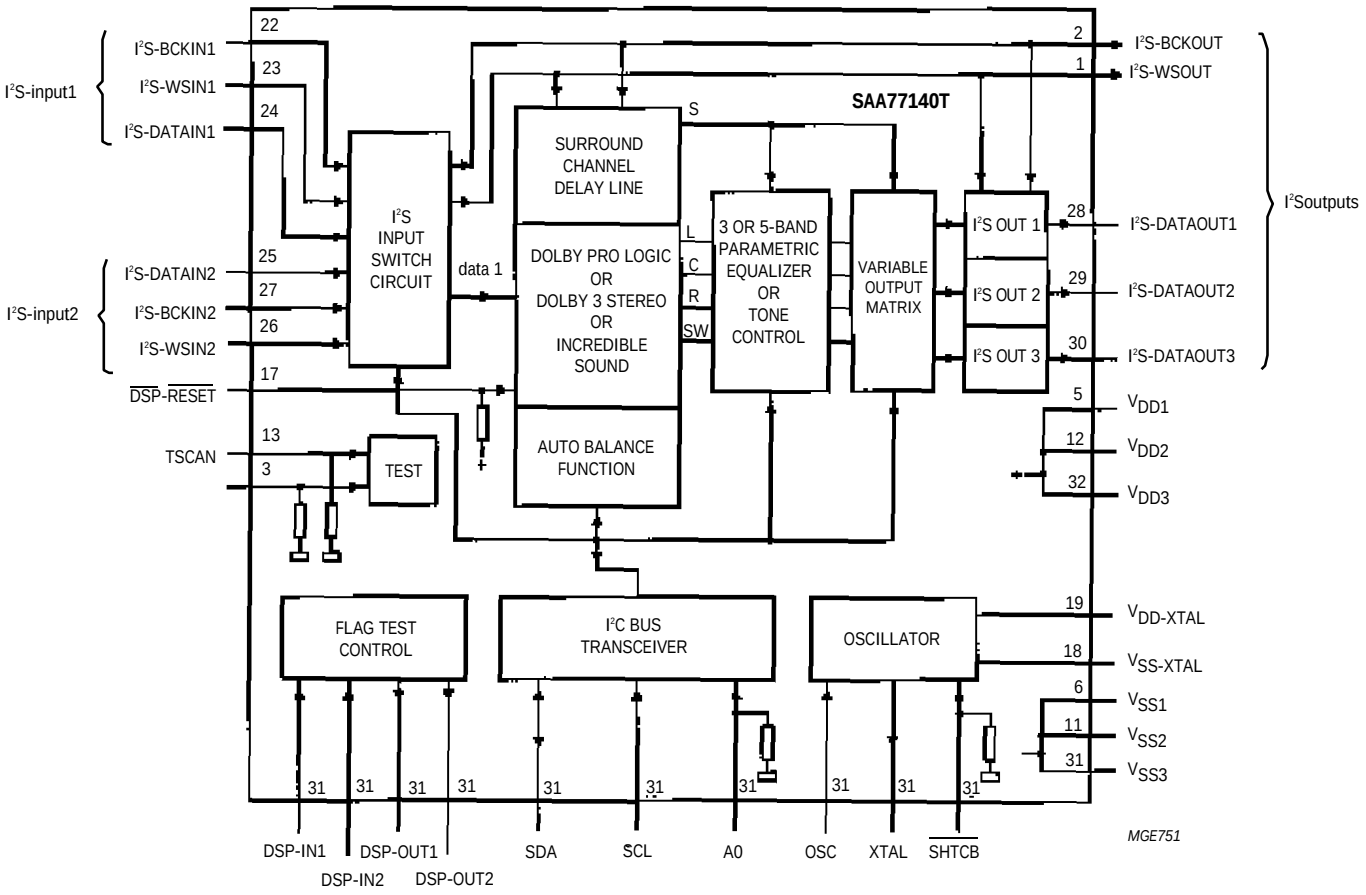
SYMBOL	PARAMETER	Min.	Max.	Unit
v_{DD}	DC supply voltage	-0.5	+6.5	V
Δv_{DD}	voltage difference between two V_{DDx} pins	-	550	mV
v_i	Maximum input voltage	-0.5	V_{DD}+0.5	V
I_{DD}	DC supply current	-	50	mA
I_{ss}	DC supply current	-	50	mA
T_{amb}	ambient operating temperature	-40	+85	°C
T_{stg}	storage temperature range	-65	+150	°C

PINNING

Symbol	Pin	Function
I^2S-WSOUT	1	I^2S-bus slave word-select output
I^2S-BCKOUT	2	I^2S-bus slave bit-clück output
$\overline{RTCB}$	3	asynchronous reset test control block input (active LOW)
$\overline{SHTCB}$	4	clock divider switch eneble input (LOW = divide)
V_{DD1}	5	positive power supply
V_{SS1}	6	ground power supply
DSP-IN1	7	flag input 1
DSP-IN2	8	flag input 2
DSP-OUT1	9	flag output 1
DSP-OUT2	10	flag output 2
V_{SS2}	11	ground power supply
V_{DD2}	12	positive power supply
TSCAN	13	scan control input
AO	14	I^2S-bus slave adress selection input
SDA	15	I^2S bus serial data input/output
SCL	16	I^2S-bus serial clock input
$\overline{DSP\text{-}RESET}$	17	chip reset input (active LOW)
$V_{SS\text{-}XTAL}$	18	ground power supply crystal oscillator
$V_{DD\text{-}XTAL}$	19	positive power supply crystal oscillator
XTAL	20	crystal oscillator output
OSC	21	crystal oscillator input
I^2S-BCKIN1	22	I^2S-bus master bit-clock input 1
I^2S-WSIN1	23	I^2S-bus master word-select input 2
I^2S-DATAIN1	24	I^2S-bus master data input 1
I^2S-DATAIN2	25	I^2S-bus master data input 2
I^2S-WSIN2	26	I^2S-bus master word-select input 2
I^2S-BCKIN2	27	I^2S-bus master bit-clock input 2
I^2S-DATAOUT1	28	I^2S-bus slave data output
I^2S-DATAOUT2	29	I^2S-bus slave data output
I^2S-DATAOUT3	30	I^2S-bus slave data output
V_{SS3}	31	ground power supply
V_{SS3}	32	positive power supply



Pin Configuration



FUNCTIONAL DESCRIPTION

Figure 1 shows the block diagram of the SAA7710T. The SAA7710T consists of a Dolby Pro Logic decoder together with equalizer or tone control. The Dolby Pro Logic part of the IC may be used to decode audio soundtracks (Dolby surround movies or Dolby surround video productions) from for example, a video recorder (VCR) or a CD laser disc into four channels Left, Centre, Right and Surround (L, C, R and S).

If desired, post-processing with either an equalizer or a tone control section is possible. In addition to this, a Sub Woofer (SW) channel, digital volume control and a user-programmable variable output matrix are implemented.

Hall/matrix surround sound functions are implemented for material not encoded using Dolby Surround. These features can be used as an alternative to Dolby Pro Logic and can also be combined with the equalizer or tone control sections.

Incredible sound is a Philips patented technology which substantially improves the stereo effect of a television or audio system. Using advanced signal processing, speakers that are positioned close together can imitate the sound produced by speakers that are far apart.

Functional modes

The device thus supports three main modes, Dolby Pro Logic/Dolby 3 stereo or hall/matrix surround or Incredible sound mode. All modes can be combined with equalizing (3-band or 5-band) or tone control depending on f_S and available cycle budget.

THE DOLBY PRO LOGIC MODE

In Dolby Pro Logic mode, several blocks must be initialized and controlled during operation:

- Noise generator and noise sequencer
- Centre channel mode(1) (normal, phantom, wide, off)
- Combining network coefficients
- 7 kHz low-pass filter in surround channel(1)
- Surround channel delay time(1)
- Modified Dolby B noise reduction must be on.

Possible post-processing modes for Dolby Pro Logic are:

- Volume control only
- Equalizer (3- or 5-band on L, C and R) or tone control (L, C, R and S); fixed output matrix(1); volume control
- Equalizer (5-band on L, C and R); variable output matrix(1); volume control
- Extra sub woofer(1).

THE DOLBY 3 STEREO MODE

in Dolby 3 stereo mode, several blocks must be initialized and controlled during operation:

- Nojise generator and noise sequencer
- Centre channel model(1) (normal, phantom, wide and off)
- Combining network coefficients.

THE HALL/MATRIX SURROUND MODE

In hall/matrix surround mode, the blocks listed below must be initialized and controlled during operation:

- Input balance control
- Hall or matrix surround Mode setting
- All-pass and filter transfer characteristic(1)
- 7 kHz low-pass filter in surround channel(1)
- Surround channel delay(1)

Possible post-processing modes for hall/matrix surround are as above:

- Volume control only
- Equalizer (3- or 5-band on L, C and R) or tone control (L, C, R and S); fixed output matrix(1); volume control
- Equalizer (5-band on L,C,R): variable output matrix(1) volume control
- Extra sub woofer(1)

THE INCREDIBLE SOUND MODE

In the Incredible sound mode the blocks listed below must be initialized and controlled during operation:

- Incredible sound coefficients
- Combining network coefficients.

Possible post-processing modes for incredible sound are as follows:

- Volume control only
- Equalizer (5-band on L and R) or tone control (L and R); variable output matrix(1), volume control
- Extra sub-woofer(1).

ADDITIONAL INFORMATION

The possible modes of operation are discussed in more detail in the *"SAA 7710T Dolby Pro Logic Programming Guide, Application Note AN95063"*: This also includes which features are available for a given system clock frequency and sample frequency and the possible input configurations.

Clock circuit and oscillator

The chip has an on board crystal clock oscillator. The block schematic of this Pierce oscillator is shown in Figs 3 and 4. The active element needed to compensate for the loss resistance of the crystal is the amplifier Gm.

This amplifier is placed between the XTAL (output) pin and the OSC (sense) pin. The gain of the oscillator is internally controlled by the automatic gain control. This prevents too much power loss in the crystal. The higher harmonics are then as low as possible. The signals on the OSC and XTAL pin are differentially amplified.

The oscillator has these two modes of operation:

The crystal oscillator mode: in this mode a quartz crystal oscillator is used to generate a clock signal which is subsequently divided by 2 to ensure that the final clock signal has a 50% duty cycle.

The oscillator circuit components R_{bias} and C1, C2 depend on the crystal. In the case of an overtone oscillator, the ground harmonic is filtered out by L1 and C3. Pin SHTCB is held low so that the divided signal is selected. Only a quartz crystal should be used in this mode.

The slave oscillator mode: in this mode the oscillator circuit acts as a slave driven by a master system clock. The clock divider can be switched on or off using pin SHTCB. When the divider is not used, the duty cycle of the clock will depend on the master system clock duty cycle and the rising and falling edge times. This places a tolerance of 5% on the 50% duty cycle of the master system clock (see Chapter "AC characteristics").

In order to be able to control the phase of the clock signal during testing the divider is skipped and the signal is directly fed to the circuit via the multiplexer in the TEST position.

SUPPLY OF THE CRYSTAL OSCILLATOR

The power supply connections to the oscillator are separated from the other supply lines to minimise feedback from on-chip ground bounce to the oscillator circuit. Noise on the power supply affects the AGC operation so the power supply should be decoupled. The $V_{SS-XTAL}$ pin is used as ground supply and the

$V_{DD-XTAL}$ as positive supply.

TDA7053A

Stereo BTL Audio Output Amplifier with DC Volume Control

FEATURES

- DC volume control
- Few external components
- Mute mode
- Thermal protection
- Short-circuit proof
- No switch-on and switch-off clicks
- Good overall stability
- Low power consumption
- Low HF radiation
- ESD protected on all pins.

GENERAL DESCRIPTION

The TDA7053A (2x1 W) and TDA7053AT (2 x 0.5 W) are stereo BTL output amplifiers with DC volume control. The devices are designed for use in TV and monitors, but are also suitable for battery-fed portable recorders and radios.

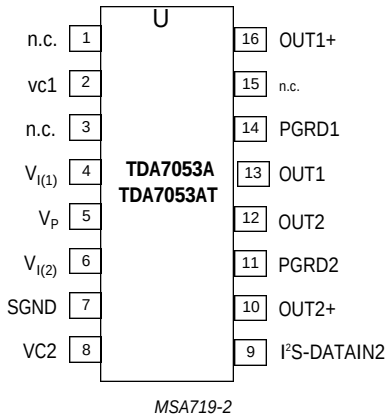
Missing Current Limiter (MCL)

A MCL protection circuit is built-in. The MCL circuit is activated when the difference in current between the output terminal of each amplifier exceeds 100 mA (typical 300 mA). This level of 100 mA allows for headphone applications (single-ended).

QUICK REFERENCE DATA

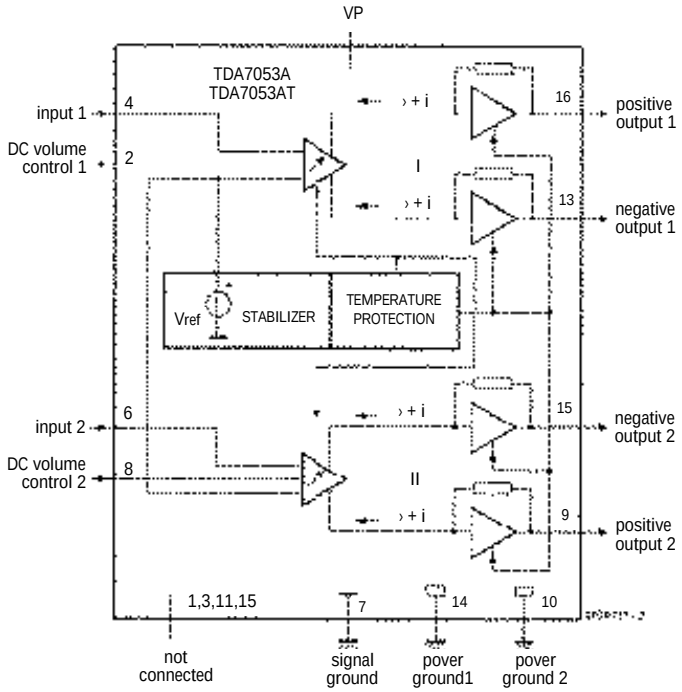
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage		4.5	-	18	V
P_{out}	output power	V_p = 6 V				
	TDA7053A	R_L = 8 Ω	0.85	1.0	-	W
	TDA7053AT	R_L = 16 Ω	0.5	0.55	-	W
G_V	voltage gain		39.5	40.5	41.5	dB
G_C	gain control		68.0	73.5	-	dB
$I_{q(to}$	total quiescent curren	Vp = 6 V; Rl = ∞	-	22	25	mA
THD	total harmonic current					
	TDA7053A	P_{out} = 0.5 W	-	0.3	1	%
	TDA7053AT	P_{out} = 0.25 W	-	0.3	1	%

SYMBOL	PIN	DESCRIPTION
n.c.	1	not connected
VC1	2	DC volume contol 1
n.c.	3	not connected
$V_{I (1)}$	4	voltage input 1
V_P	5	positive supply voltage
$V_{I (2)}$	6	voltage input 2
SGND	7	signal ground
VC2	8	DC volume contol 2
OUT2+	9	positeve output 2
PGND2	10	power ground 2
n.c.	11	not connected
OUT2-	12	negative output 2
OUT1-	13	negative output 1
PGND1	14	powwer ground 1
n.c.	15	not connected
OUT1+	16	positive output 1



MSA719-2

Pin Configuration



LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX	UNIT
V_P	supply voltage		-	18	V
I_{ORM}	repetetitive peak output current		-	1.25	A
I_{OSM}	non-repetitive peak output current		-	1.5	A
P_{tot}	total power dissipation	$T_{amb} \leq 25\ ^oC$			
	TDA7053A		-	2.5	W
	TDA7053AT		-	1.32	W
t_{sc}	short-circuit time		-	1	hr
V_n	input voltage pins 2,4,6 and 8		-	5	V
T_{amb}	operating ambient temperaure		-40	+85	°C
T_{stg}	storage temperature		-55	+150	°C
T_{vj}	virtual junction temperature		-	+150	°C

FUNCTIONAL DESCRIPTION

The TDA7053A and TDA7053AT are stereo output amplifiers with two DC volume control stages, designed for TV and monitors, but also suitable for battery-fed portable recorders and radios.

In conventional DC volume control circuits the control or input stage is AC coupled to the output stage via external capacitors to keep the offset voltage low.

The two DC volume control stages are integrated into the input stages so that no coupling capacitors are required and a low offset voltage is still maintained. The minimum supply voltage also remains low.

The BTL principle offers the following advantages:

- Lower peak value of the supply current
- The frequency of the ripple on the supply voltage is twice the signal frequency.

Consequently, a reduced power supply with smaller capacitors can be used which results in cost reductions For portable applications there is a trend to decrease the supply voltage, resulting in a reduction of output power at conventional output stages. Using the BTL principle increases the output power.

The maximum gain of the amplifier is fixed at 40.5 dB. The DC volume control stages have a logarithmic control characteristic. Therefore, the total gain can be controlled from +40.5 to -33 dB.

If the DC volume control voltage falls below 0.4 V, the device will switch to the mute mode.

The amplifier is short-circuit protected to ground, V_p and across the load. A thermal protection circuit is also implemented. If the crystal temperature rises above 150 °C the gain will be reduced, thereby reducing the output power.

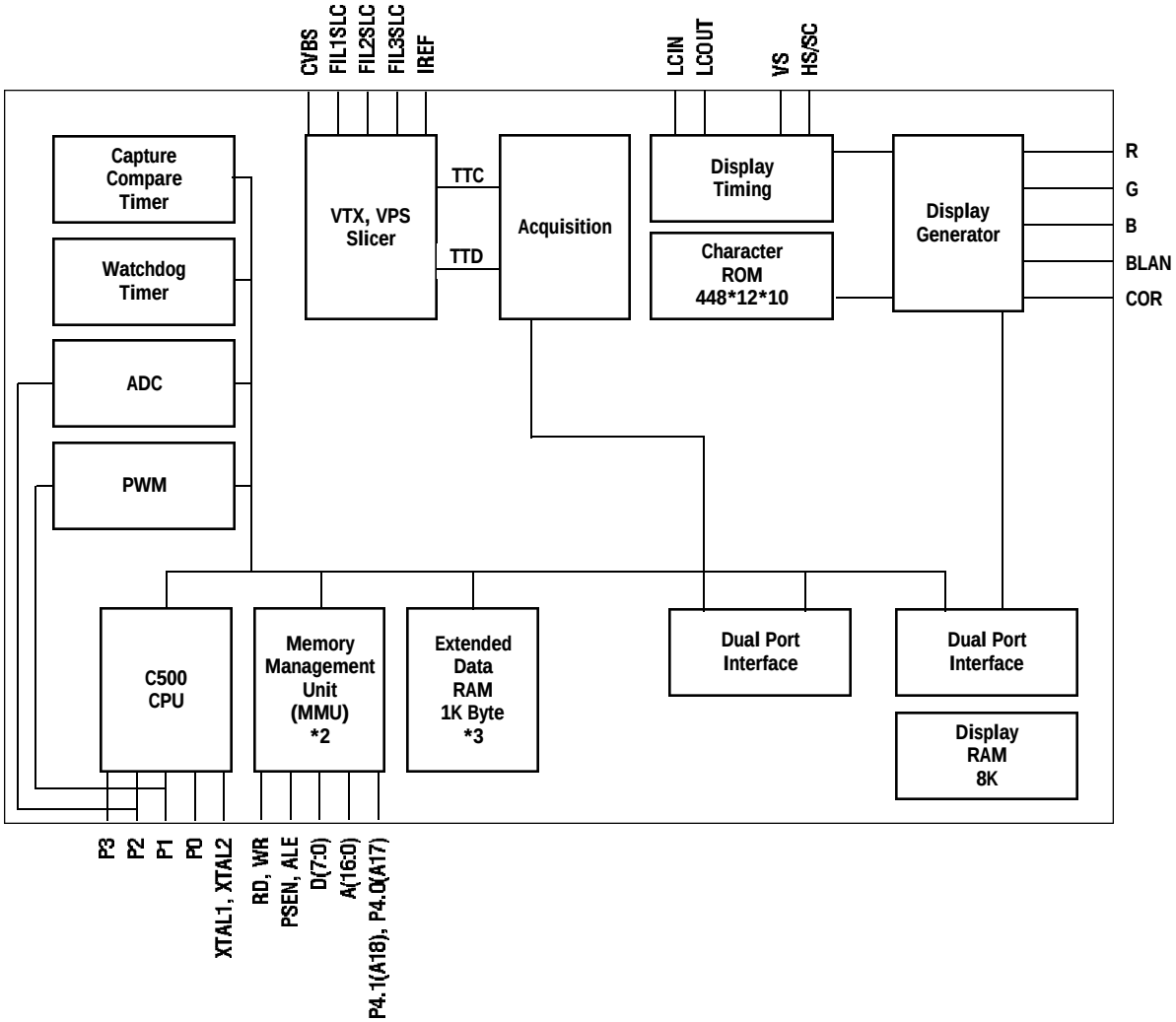
Special attention is given to switch-on and switch-off clicks, low HF radiation and a good overall stability.

SDA5250
Microcontroller Unit

General Description

The SDA 5250 contains a slicer for VPS and TTX, an accelerating acquisition hardware module, a display generator for "level 1.5" TTX data and a 8 bit micro controller running at 333 nsec cycle time. The controller with dedicated hardware quarantees flexibility, does most of the internal processing of TTX acquisition, transfers data to/from the external memory interface and receives/transmits data via I^2C and UART user interfaces. The block diagram shows the internal organization of the SDA5250. The slicer combined with dedicated hardware stores TTX data in a VBI buffer of 1 Kbyte.

The micro controller firmware does the total acquisition task (hamming-and parity- checks, page search and evaluation of header control bits) once per field.



Microcontroller Unit

Symbol	Pin number	Function	Pin voltage
SCL	48	I²C-Bus clock line (SCL)	5V/Vpp
SDA	49	I²C-Bus data line (SDA)	5V/Vpp
EXT2	50	EXT2	-
RSTMSP	51	Reset Msp	5V
KYB4	52	Keyboard scan line input / output	-
KYB3	53	Keyboard scan line input / output	-
KYB2	54	Keyboard scan line input / output	-
KYB1	55	Keyboard scan line input / output	-
VOL	84	Volume control output	0-5V
COLOR	83	Color control output	0-5V
BRI	82	Brightness control output	0-5V
CON	81	Contrast control output	0-5V
HUE	80	Hue control output	0-5V
STD	79	Standard select input	5V
L/L'	78	L / l' output	-
VTUNE	77	Tuning voltage	0-5V
AFC	61	Analogue AFC sense input	-
STATUS-AV	60	Status AV input (1or 2 AV)	-
AGC	59	Automatic Gain Control Output	-
AVOUT	76	AV select output	0-5V
BND2	75	Band switch 2-output	0-5V
BND0	74	Band switch 1-output	0-5V
IRIN	73	Remote control output	0-5V
BND1	72	Band switch 0-output	0-5V
MUTE	71	Mute output for sound	-
OFF / ON	70	Stand-by / On control input / output	-
NEG / POS	69		
A0, A1,...A18	29,27,26 24,22,20 18,16,17 19,25,21 14,15,13 12,10,9,11	Address bus for external memory	5Vpp
D0, D1,...D7	31,33,35 36,34,32 30,28	Data bus for external memory	5Vpp
PSEN	23	Program store enable	-
ALE	8	Address latch enable	-
XTAL1	4	Input to the inverting oscillator amp.	5V
XTAL2	3	Output of the inverting oscillator amp.	5V

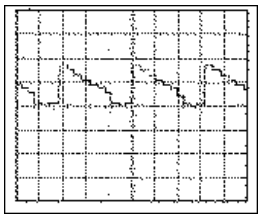
Symbol	Pin number	Function	Pin voltage
RST	5	Power on reset	5V
Vdd	2,43	Power supply voltage	5V
Vss	1,42	Ground	0V
RD	7	Read access from external memory	-
WR 6	6	Write access to external memory	-
R	37	OSD Red color signal output	4.5Vpp
G	38	OSD Green color signal output	4.5Vpp
B	39	OSD Blue color signal output	4.5Vpp
BLAN	40	OSD fast blanking output	4.5Vpp
COR	41	Contrast reduction output	
HS/SC	46	Horizontal sync input	5Vpp,HF
VS	47	Vertical sync input	5Vpp,HF
CVBS	68	CVBS input	5Vpp
IREF	67	Reference current for slicer PLLs	-
VDDA	66	Analog supply voltage for slicer	5V
VSSA	62	Analog ground for slicer	0V
FIL1SLC	65	PLL loop filter I/O for vps slicing	-
FIL2SLC	64	PLL loop filter I/O for teletext slicing	0V
FIL3SLC	63	PLL loop filter I/O for phase shifting of VPS teletext data	-
LCIN	44	LCIN and LCOUT are used to connect the external display dot clock frequency	-
LCOUT	45	reference	-
NC	56,57	Not connected	-

27C010 (27C1001) EPROM

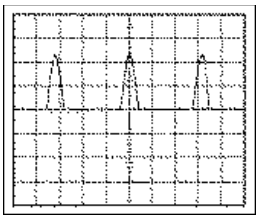
VCC	32	Supply voltage	5V
VDD	16	Ground	0V
A0-A16	12,11,10 9,8,7,6,5 4,3,2,23 25,26,27 28,29	Address Bus	0-5
D0-D7	13,14,15 17,18,19 20,21	Data Bus	0-5V
E	22	Enable	0-5V
G	24	Output Enable	-
VPP	1	Programming Voltage	-
PGM	31	Programming Pulse	-
NC	30	Not Connected	-

OSCILLOSCOPE SIGNALS

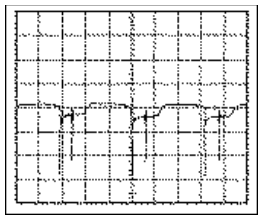
1)K201 pin 7 Luminance Y
100Hz Div: 1V; T:1ms



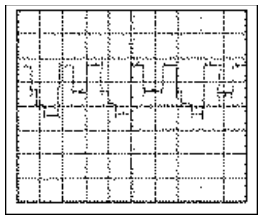
2) Q203 Collector Pulse
Div: 500V; T: 10ms



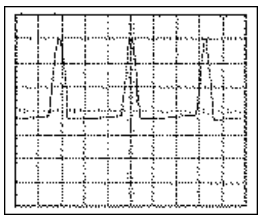
3) Q203 Base Hor. Drive
Pulse D:5V; T:10ms



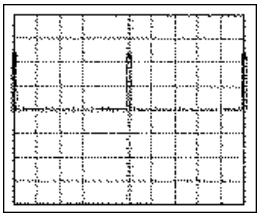
4)K311 pin 9 Red
Div: 1V; T: 10ms



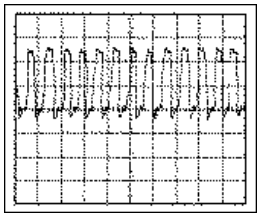
5)Horizontal Flyback I201
pin 1 Div: 2V; T:10ms



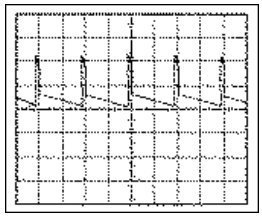
6)I201 pin 12 Vertical
Pulse Div: 2V; T:2ms



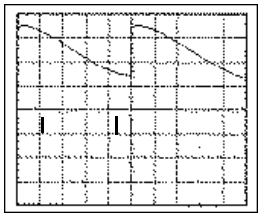
7)K202 pin 3 Line-locked
Clock 27MHz Div: 2V; T:50ms



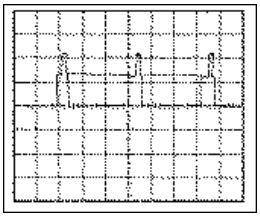
8) I202 pin 7 Vertical Def.
Output Div: 20V; T:5ms



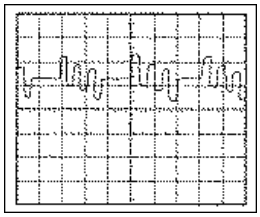
9)I201 pin 10 Ver. Dri.
Pulse Div: 1V; T:2ms



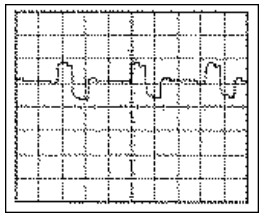
10) I202 pin 2 Sandcastle
Div: 2V; T: 10ms



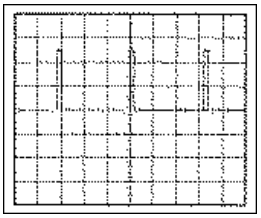
11) K201 pin 9 B-Y
Div: 1V; T: 10ms



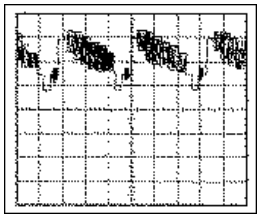
12) K201 pin 8 R-Y
Div: 1V; T: 10ms



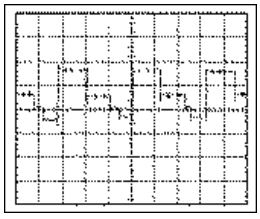
13) K311 pin 1 HA
Div: 2V; T: 20ms



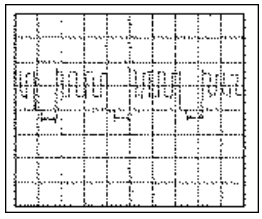
14) K311 pin 16 CVBS
Div: 1V; T: 20ms



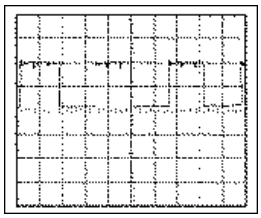
15) K311 pin 8 Green
Div: 1V; T: 10ms



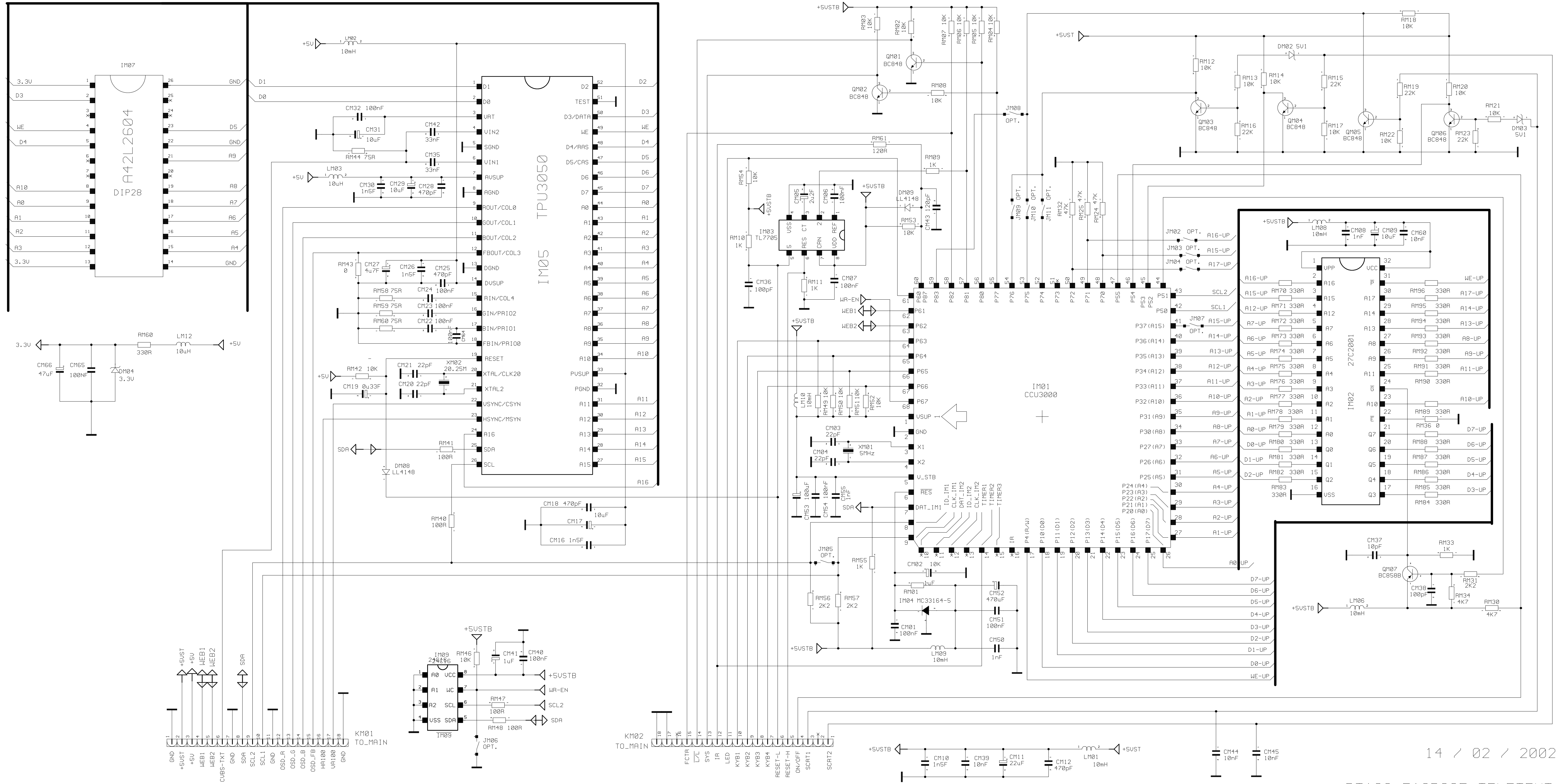
16) K311 pin 7 Blue
Div: 1V; T: 10ms



17) Q202 Collector Hor. Drive
Pulse Div: 2V; T: 10ms

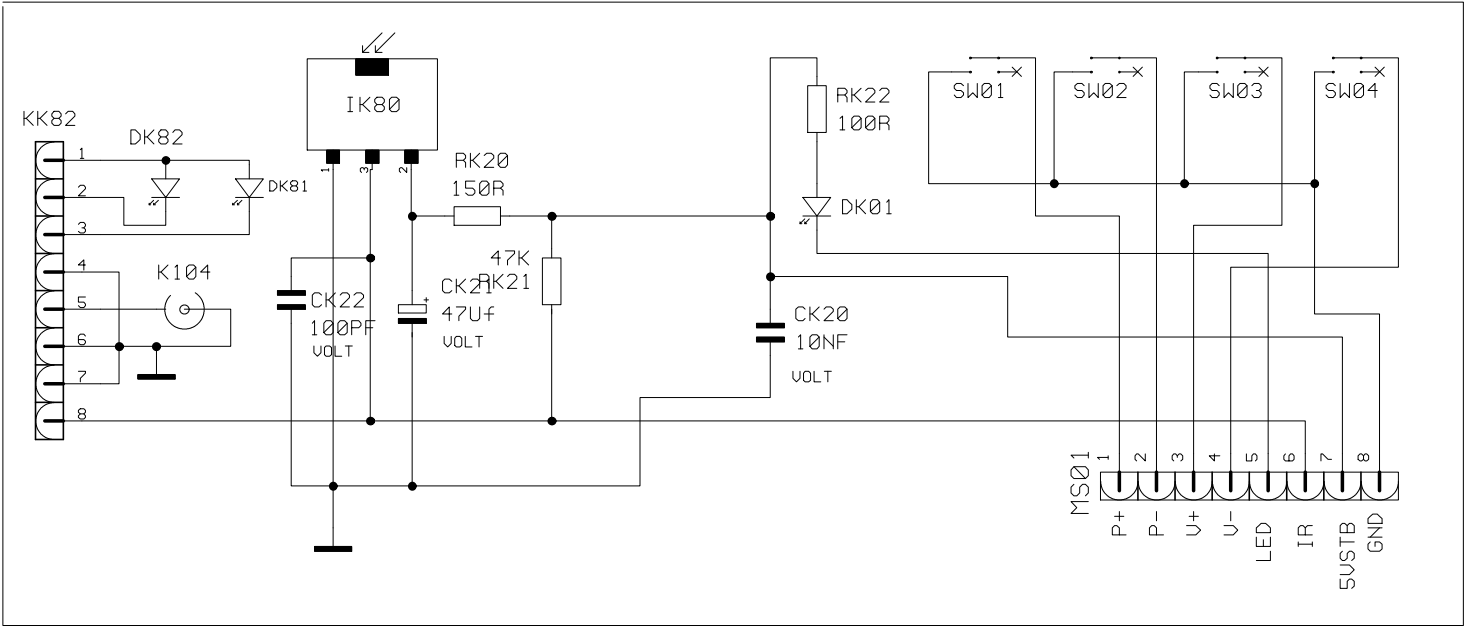



SS03 SCRT3
SS01 SCRT1
SS02 SCRT2
IT01 TDA4470
TT01 CTT5520E
IS01 MSP3411G
IS02 TDA6920
74HCT86 ID02
IS05 TDA7264
IS04 TDA7264
IP01 TDA16846
IP02 TCDT1101G
TP01 SMPS
IP06 7812
IP05 7808
IP07 L4940V
IP04 L4931CV33
ID01 STV9379AF
TD01 DST
K005 TO_FTR.BOX.
K001 TO_uP
K004 TO_FTR.BOX.
K006 TO_POWER
K002 NAME
K003 TO_KYB_IRLED
KD01 TO-CRT
KD02 H-YOKE
KD03 V-YOKE
KP01 AC220-IN
KP02 TO_DVD_POWER
SW01 TO_WEB
SW03 TO_WEB
SW04 TO_WEB
SD01 TO_DVD
SD02 TO_DVD
SD04 TO_DVD
SS04 HSP-242V
SS05 DSW-02
SS06 SVHS_IN
KS06
KS07 TO_SPK
KS01 TO_SPK
KS02 TO_SPK
00TA055-6
PT100 MAIN SCH
11/04/2002
ALL RIGHT RESERVED



14 / 02 / 2002

PT100 512PAGE TELETEXT


KK82
DK82
DK81
K104
IK80
RK20
150R
CK22
100PF
VOLT
CK21
47Uf
VOLT
47K
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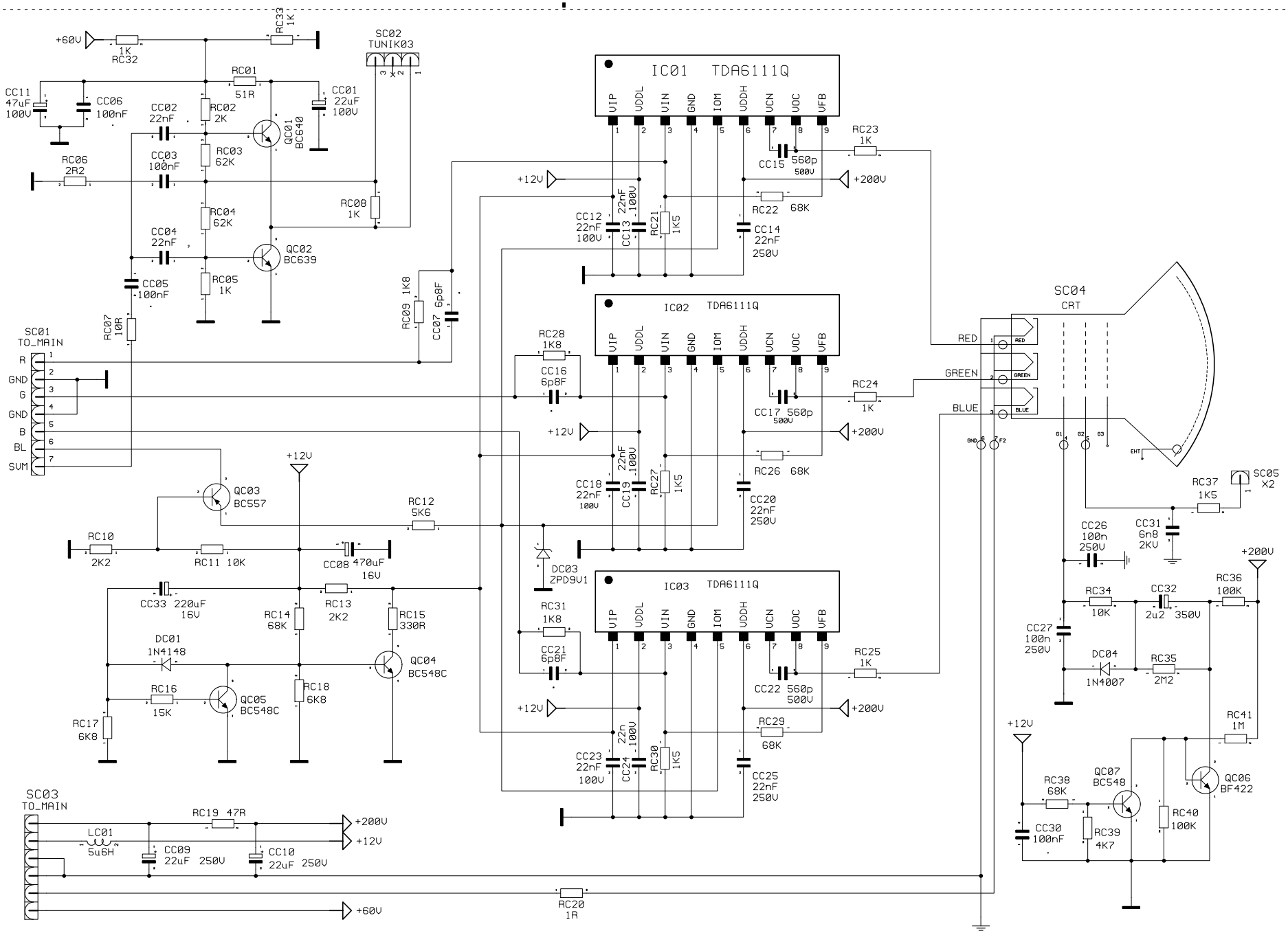
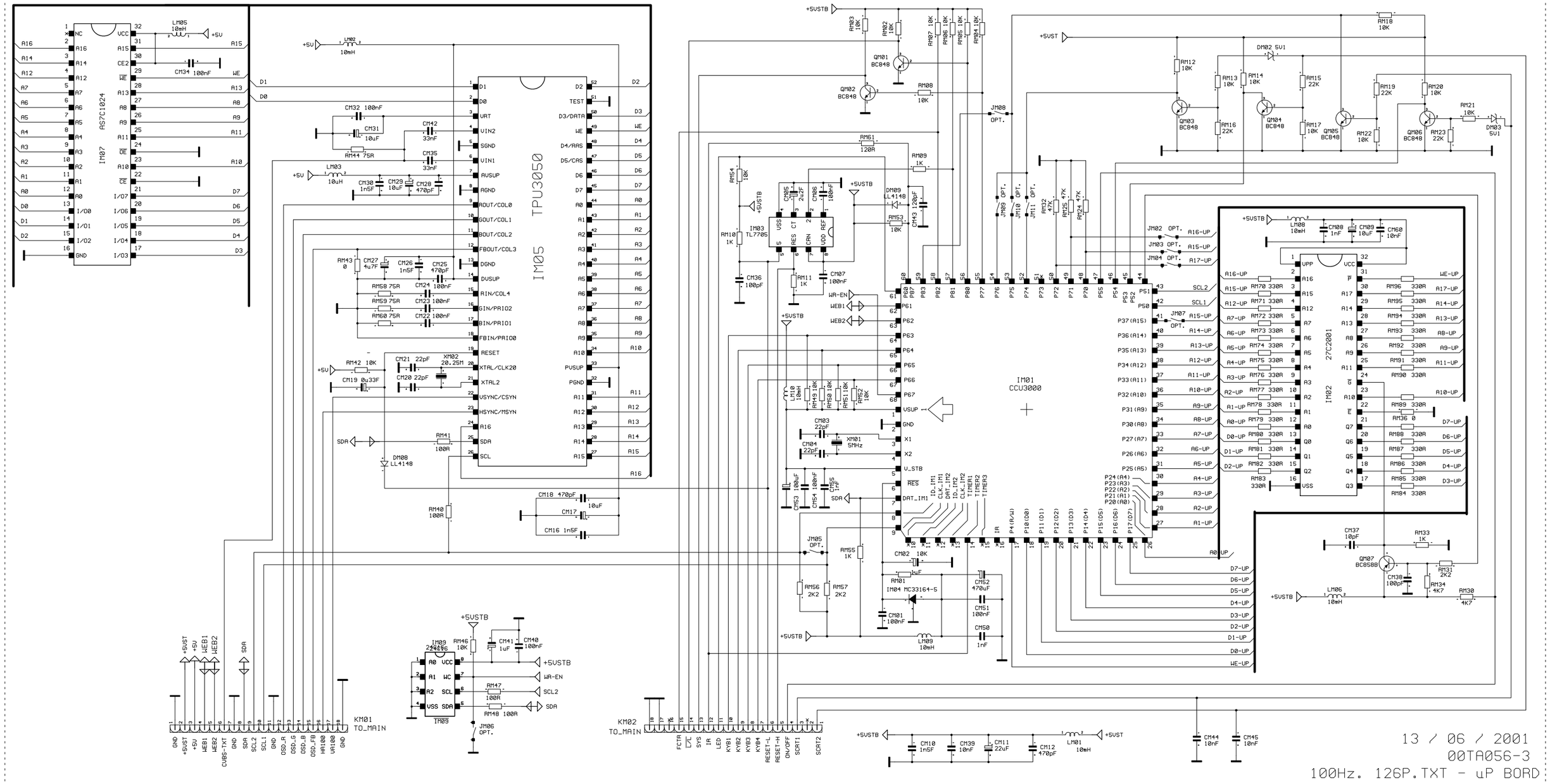
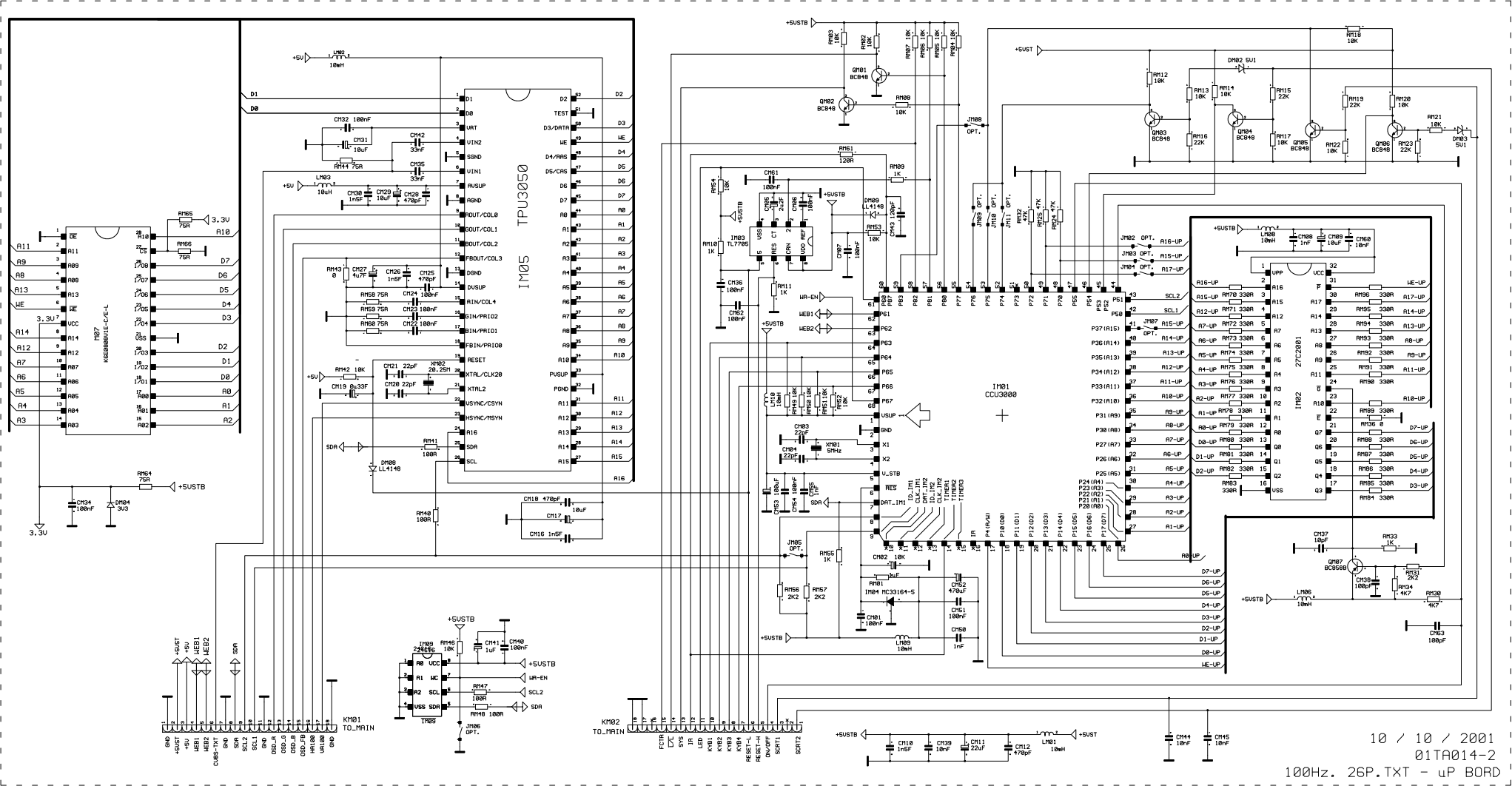
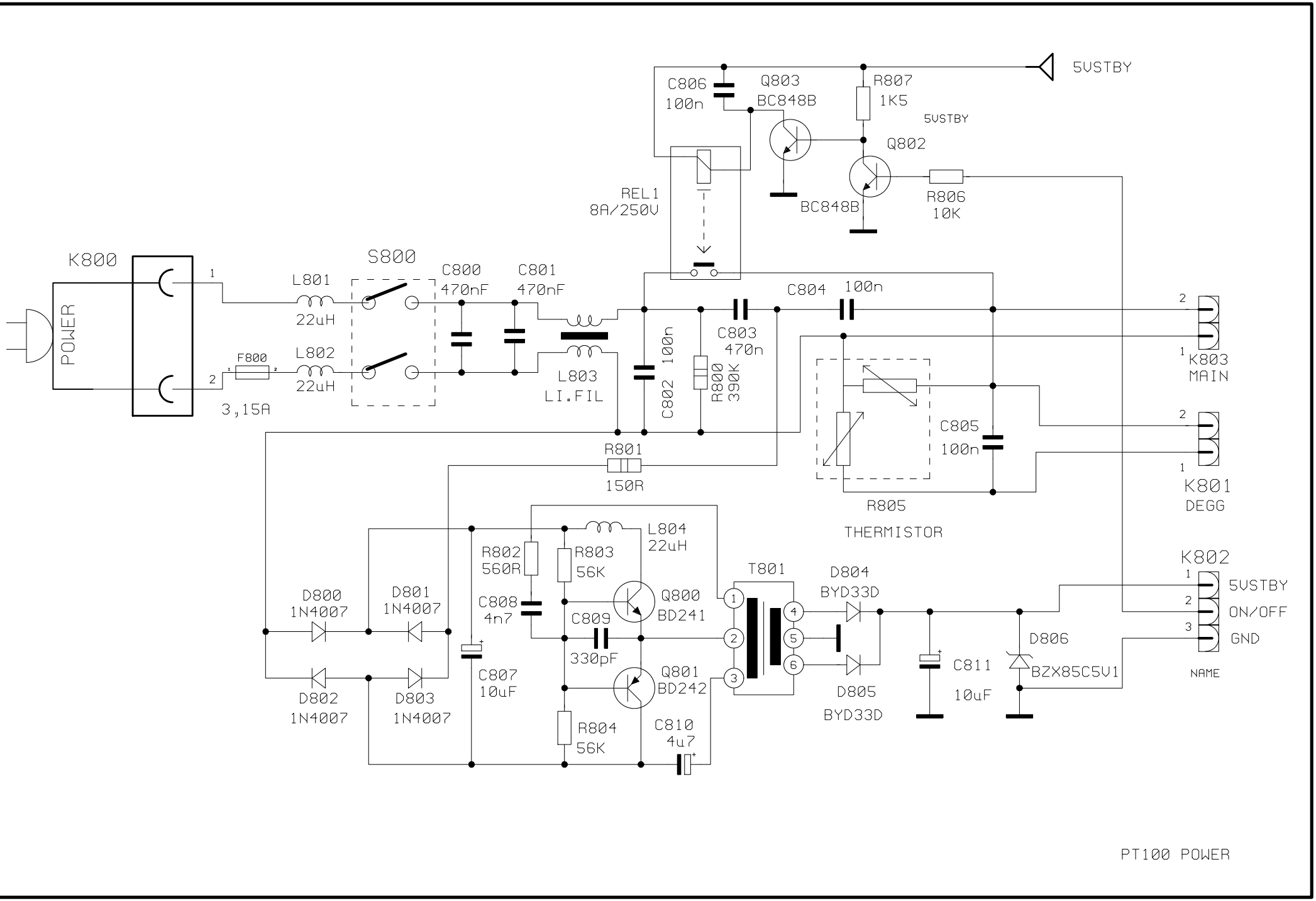
RK22
100R
DK01
CK20
10NF
VOLT
SW01
SW02
SW03
SW04
MS01
P+
P-
V+
V-
LED
IR
5VSTB
GND

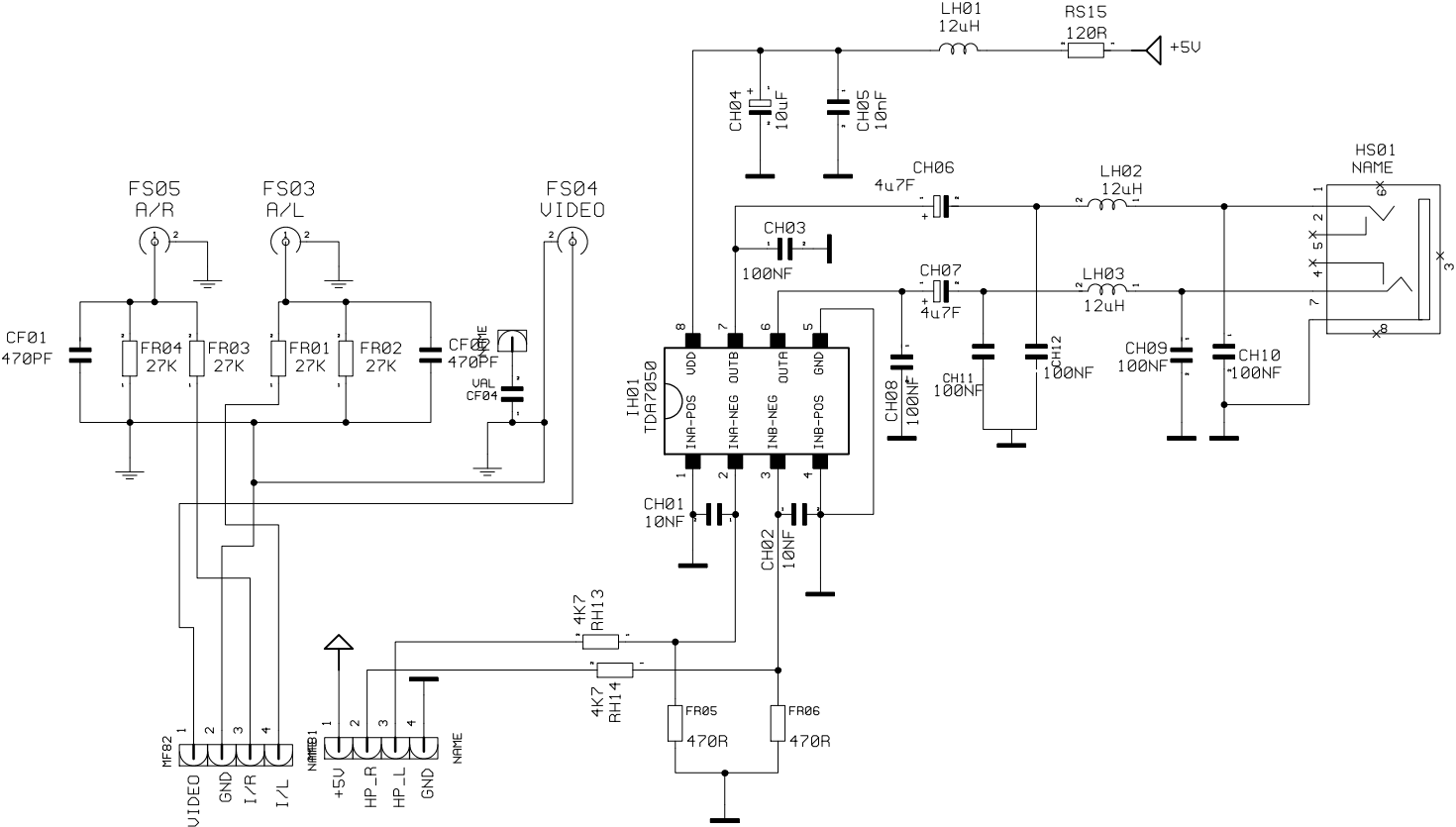


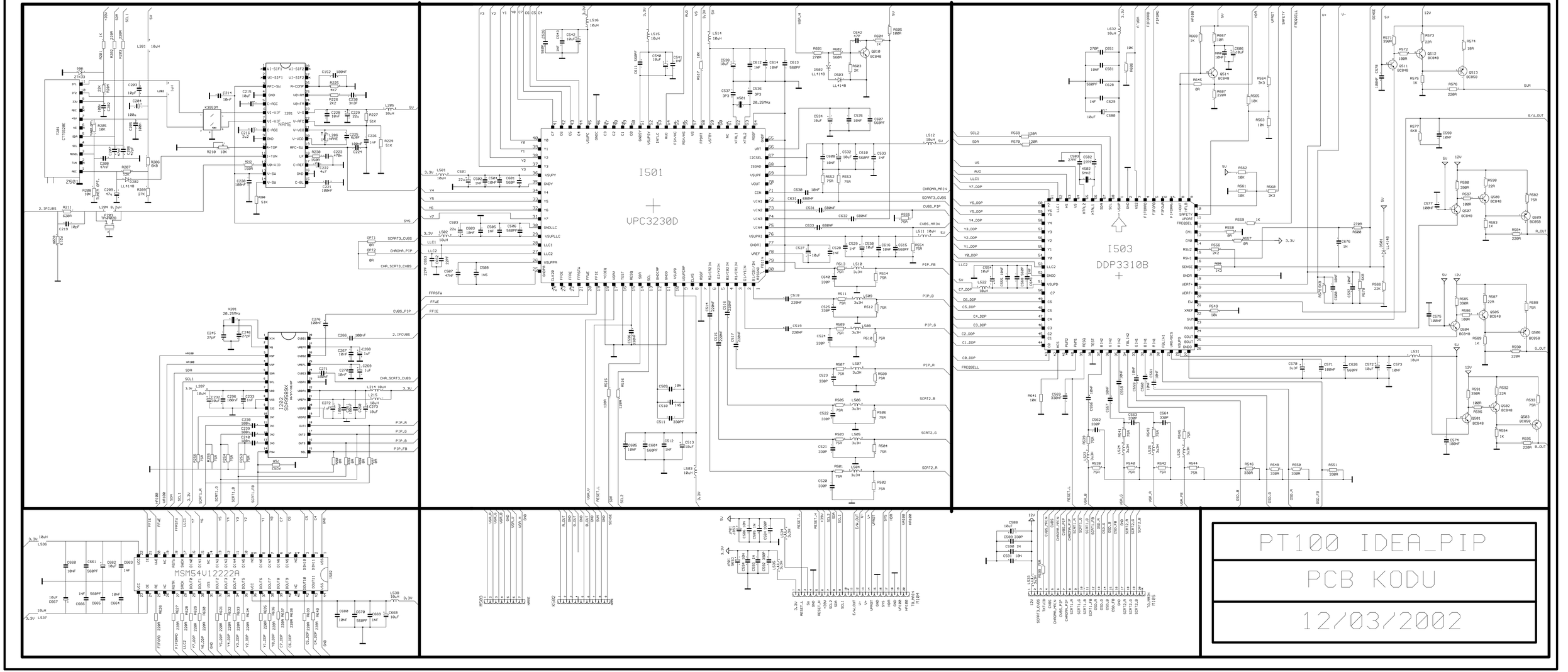
12 / 03 / 2001
100 Hz. CRT PCB


IM07 AS7C1024
IM05 TPU3050
IM01 CCU3000
IM02 27C2001
IM03 TL7705
IM04 MC33164-5
IM09 24LC16
QM01 BC848
QM02 BC848
QM03 BC848
QM04 BC848
QM05 BC848
QM06 BC848
QM07 BC858B
DM01 LL4148
DM02 5V1
DM03 5V1
DM08 LL4148
XM01 5MHz
XM02 20.25M
KM01 TO_MAIN
KM02 TO_MAIN
+5VSTB
+5VST
+5V
WEB1
WEB2
SDA
WR-EN
SCL1
SCL2
13 / 06 / 2001
00TA056-3
100Hz. 126P.TXT - uP BORD


IM05 TPU3050
IM01 CCU3000
IM02 27C2001
M07 K9S08B40YIE-C/E-L
KM01 TO_MAIN
KM02 TO_MAIN
10 / 10 / 2001
01TA014-2
100Hz. 26P.TXT - uP BORD


5VSTBY
C806
100n
Q803
BC848B
R807
1K5
5VSTBY
Q802
BC848B
R806
10K
REL1
8A/250V
K800
POWER
S800
L801
22uH
L802
22uH
F800
3,15A
C800
470nF
C801
470nF
L803
LI.FIL
C802 100n
R800
390K
C803
470n
C804
100n
K803
MAIN
C805
100n
K801
DEGG
R805
THERMISTOR
R801
150R
L804
22uH
R802
560R
R803
56K
Q800
BD241
C808
4n7
C809
330pF
Q801
BD242
R804
56K
C810
4u7
C807
10uF
D800
1N4007
D801
1N4007
D802
1N4007
D803
1N4007
T801
D804
BYD33D
D805
BYD33D
C811
10uF
D806
BZX85C5V1
K802
5VSTBY
ON/OFF
GND
NAME
PT100 POWER


LH01
12uH
RS15
120R
+5V
CH04
10uF
CH05
10nF
HS01
NAME
CH06
4u7F
LH02
12uH
CH03
100NF
CH07
4u7F
LH03
12uH
FS05
A/R
FS03
A/L
FS04
VIDEO
CF01
470PF
FR04
27K
FR03
27K
FR01
27K
FR02
27K
CF02
470PF
VAL
CF04
IH01
TDA7050
VDD
OUTB
OUTA
GND
INA-POS
INA-NEG
INB-NEG
INB-POS
CH08
100NF
CH11
100NF
CH12
100NF
CH09
100NF
CH10
100NF
CH01
10NF
CH02
10NF
4K7
RH13
4K7
RH14
FR05
470R
FR06
470R
MF02
VIDEO
GND
I/R
I/L
NAME01
+5V
HP_R
HP_L
GND
NAME


I501
VPC3230D
I503
DDP3310B
PT100 IDEA_PIP
PCB KODU
12/03/2002