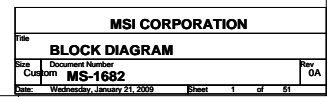


- 01 BLOCK DIAGRAM
- 02 PLATFORM
- 03 PENRYN-1 (HOST BUS)
- 04 PENRYN-2 (POWER/GND)
- 05 M672DX-1 (HOST BUS & PCIE)
- 06 M672DX-2 (MutliO)
- 07 M672DX-3 (DDR2)
- 08 M672DX-4 (POWER)
- 09 M672DX-5 (VSS)
- 10 DDR2 SODIMM 0
- 11 DDR2 SODIMM 1
- 12 DDR2 TERMINATION
- 13 M92M-host-lvds
- 14 M92M-IO
- 15 M92M-power
- 16 M92M-power-straps
- 17 M92M_MEM_Interface
- 18 M92M_DDR2_A0
- 19 M92M_DDR2_A1
- 20 CRT & LVDS CONN
- 21 CLOCK GEN & Dimm BUF
- 22 SIS968-1 (PCI/IDE/SPI/MutIO)
- 23 SIS968-2 (CPU/SATA)
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- 26 USBX2&Camera&MDC&BT CONN
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- 28 RTS158E_CARD READER
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- 30 MINI_PCIECARD & LED & SW
- 31 AUDIO(ALC662) / AMP(APA2031)
- 32 SPK & HP & MIC
- 33 KBC/EC/FAN (ENE3925)
- 34 PWRGD & UP & C3/C4
- 35 Battery select
- 36 Battery Charger
- 37 M_System power
- 38 M_1.8V & SMDDR_VTERM & 1.5V
- 39 M_1.2V & VTT power
- 40 VGA power
- 41 CPU power
- 42 Screw
- 43 EMI
- 44 Power Sequence-1
- 45 Power Sequence-2
- 46 Power Sequence_3
- 47 Launch Board
- 48 TP Board
- 49 USBx2 & RJ45 & RJ11 Board



Voltage Rails

Voltage	Description	Control Signal
PWR_SRC	AC ADAPTER OR BATTERY IN	
V_CORE	Core Voltage for Processor	VR_ON
+VTT	1.05 rail for Processor & SIS968 GTL IO	+1_5VM_PG
+1_5VRUN	1.5V switched power rail(off in S3-S5)	+5VRUN
+1_2VRUN	1.2V power rail SISM672FX Analog (off in S3-S5)	RUND (RUN_ON)
+3VRUN	3.3V switched power rail(off in S3-S5)	RUND (RUN_ON)
+5VRUN	5.0V switched power rail(off in S3-S5)	RUND (RUN_ON)
SMDDR_VTERM	0.9V DDR Termination voltage (off in S4-S5)	RUN_ON
+1_8VDIMM	1.8V power rail DDRII (off in S4-S5)	DIMM_ON
+1_8VRUN	1.8V power for SIS968 MuTIOL IO and core logic (off in S3-S5)	RUND (RUN_ON)
+1_8VSUS	1.8V power rail for SB core logic (off in S4-S5)	SUS_ON
+3VSUS	3.3V power rail (off in S4-S5)	SUS_ON
+5VSUS	5.0V power rail (off in S4-S5)	SUS_ON
+3VALW	3.3V always on power rail	PWR_SRC
+5VALW	5.0V always on power rail	PWR_SRC
+V5_AUDIO	5.0V Power rail Audio codec(off in S3-S5)	RUND
+1_2VSUS	1.2V power rail SISM672FX Digital (off in S4-S5)	SUS_ON

POWER STATES

STATE \ SIGNAL	SLP_S3#	SLP_S5#	+V*ALWAYS	+V*SUS	+V*RUN	Clocks	+1_8VDIMM
Full ON	HIGH	HIGH	ON	ON	ON	ON	ON
S1(Power On Suspend)	HIGH	HIGH	ON	ON	ON	LOW	ON
S3(Suspend to RAM)	LOW	HIGH	ON	ON	OFF	OFF	ON
S4(Suspend to Disk)	LOW	LOW	ON	OFF	OFF	OFF	OFF
S5 / Soft OFF	LOW	LOW	ON	OFF	OFF	OFF	OFF

Note : WHEN AC MODE , System turn on then +V*SUS will always keep high

MSI CORPORATION

Title

PLATFORM

Size

Custom

Document Number

MS-1682

Rev

0A

Date

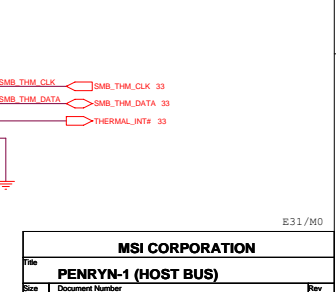
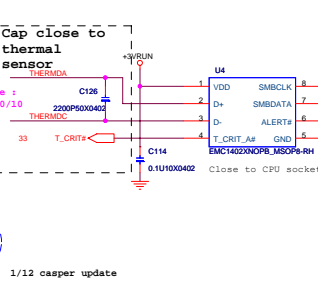
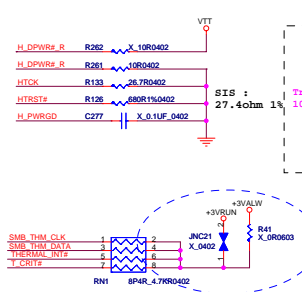
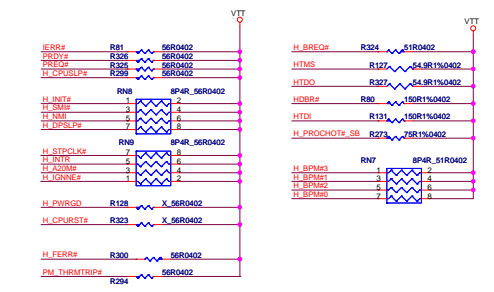
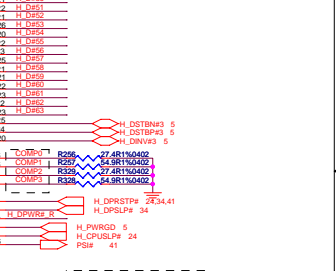
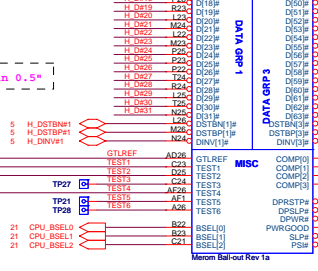
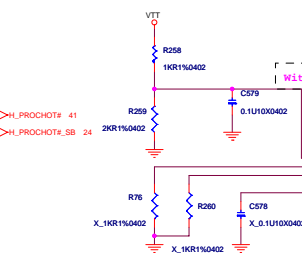
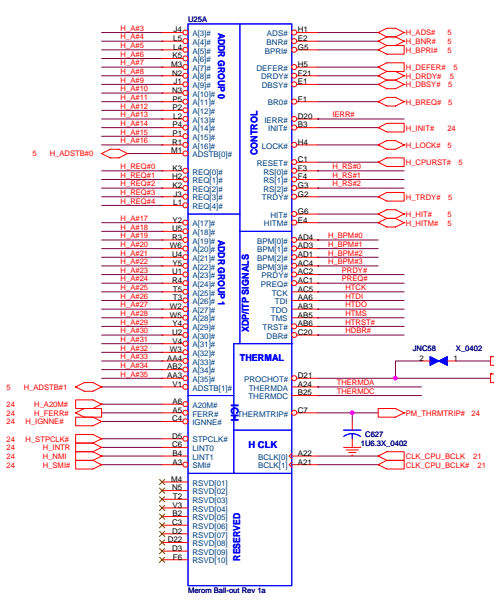
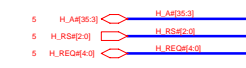
Wednesday, January 21, 2009

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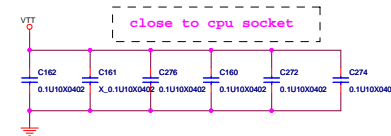
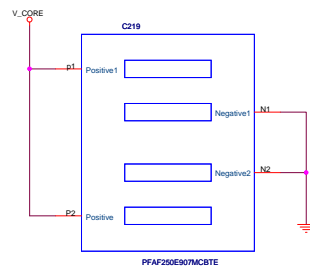
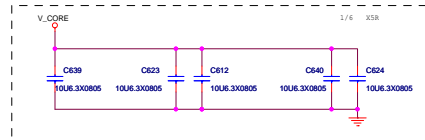
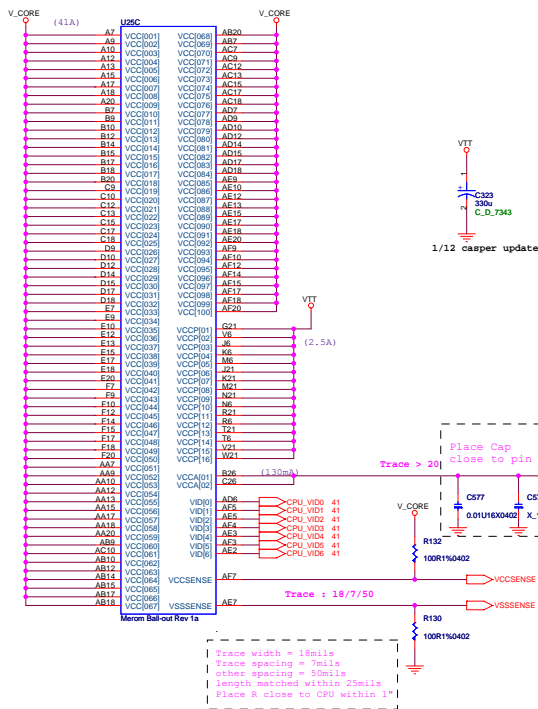
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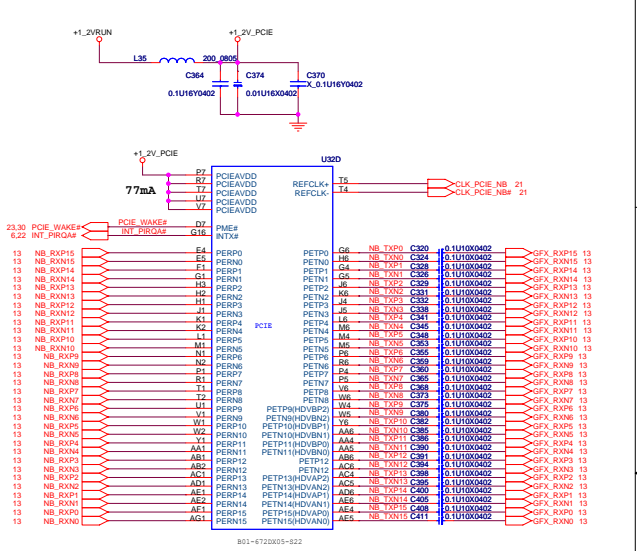
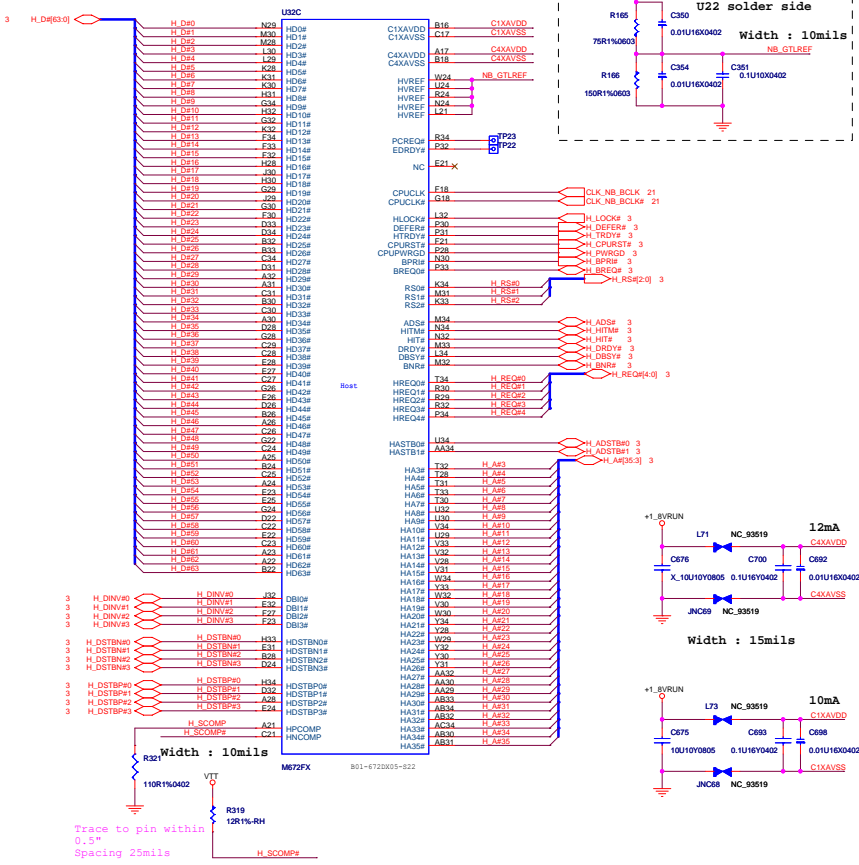
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PENRYN-1 (HOST BUS)			
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AB	VSS002	VSS003
AC	VSS003	VSS004
AD	VSS004	VSS005
AE	VSS005	VSS006
AF	VSS006	VSS007
AG	VSS007	VSS008
AH	VSS008	VSS009
AI	VSS009	VSS010
AL	VSS010	VSS011
AM	VSS011	VSS012
AN	VSS012	VSS013
AO	VSS013	VSS014
AP	VSS014	VSS015
AQ	VSS015	VSS016
AR	VSS016	VSS017
AS	VSS017	VSS018
AT	VSS018	VSS019
AV	VSS019	VSS020
AW	VSS020	VSS021
AX	VSS021	VSS022
AY	VSS022	VSS023
AZ	VSS023	VSS024
BA	VSS024	VSS025
BB	VSS025	VSS026
BC	VSS026	VSS027
BD	VSS027	VSS028
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BG	VSS030	VSS031
BH	VSS031	VSS032
BI	VSS032	VSS033
BJ	VSS033	VSS034
BK	VSS034	VSS035
BL	VSS035	VSS036
BM	VSS036	VSS037
BN	VSS037	VSS038
BO	VSS038	VSS039
BP	VSS039	VSS040
BQ	VSS040	VSS041
BR	VSS041	VSS042
BS	VSS042	VSS043
BT	VSS043	VSS044
BU	VSS044	VSS045
BV	VSS045	VSS046
BW	VSS046	VSS047
BX	VSS047	VSS048
BY	VSS048	VSS049
BZ	VSS049	VSS050
CA	VSS050	VSS051
CB	VSS051	VSS052
CC	VSS052	VSS053
CD	VSS053	VSS054
CE	VSS054	VSS055
CF	VSS055	VSS056
CG	VSS056	VSS057
CH	VSS057	VSS058
CI	VSS058	VSS059
CJ	VSS059	VSS060
CK	VSS060	VSS061
CL	VSS061	VSS062
CM	VSS062	VSS063
CN	VSS063	VSS064
CO	VSS064	VSS065
CP	VSS065	VSS066
CQ	VSS066	VSS067
CR	VSS067	VSS068
CS	VSS068	VSS069
CT	VSS069	VSS070
CU	VSS070	VSS071
CV	VSS071	VSS072
CW	VSS072	VSS073
CX	VSS073	VSS074
CY	VSS074	VSS075
CZ	VSS075	VSS076
DA	VSS076	VSS077
DB	VSS077	VSS078
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DD	VSS079	VSS080
DE	VSS080	VSS081
DF	VSS081	VSS082
DF	VSS082	VSS083



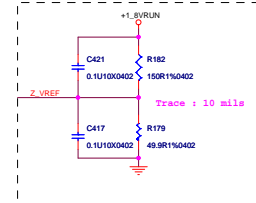
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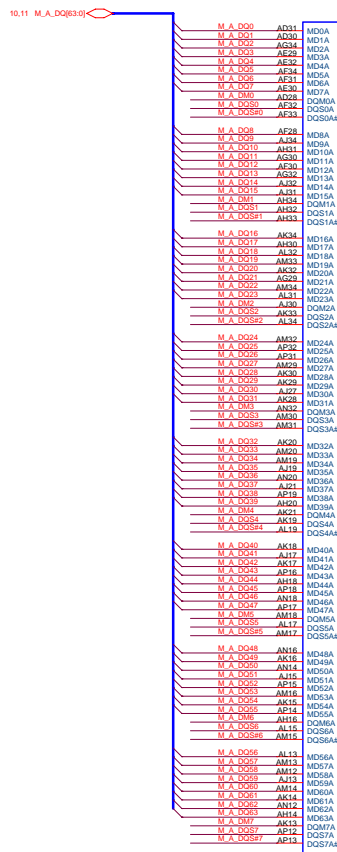
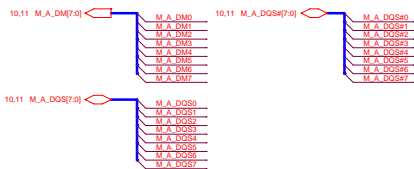
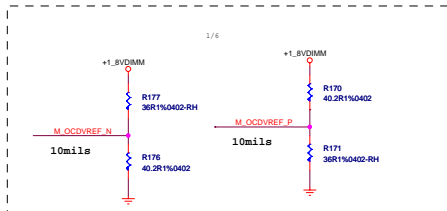
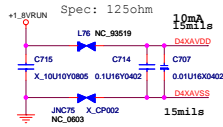
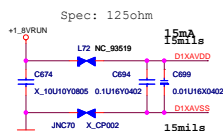
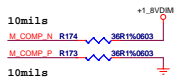
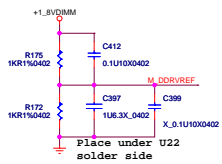
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Size: Custom	Document Number: MS-1682	Rev: 0A	
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E49 / M0

MSI CORPORATION			
672DX-1 (HOST BUS & PCIE)			
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Size	Custom	MS-1682	
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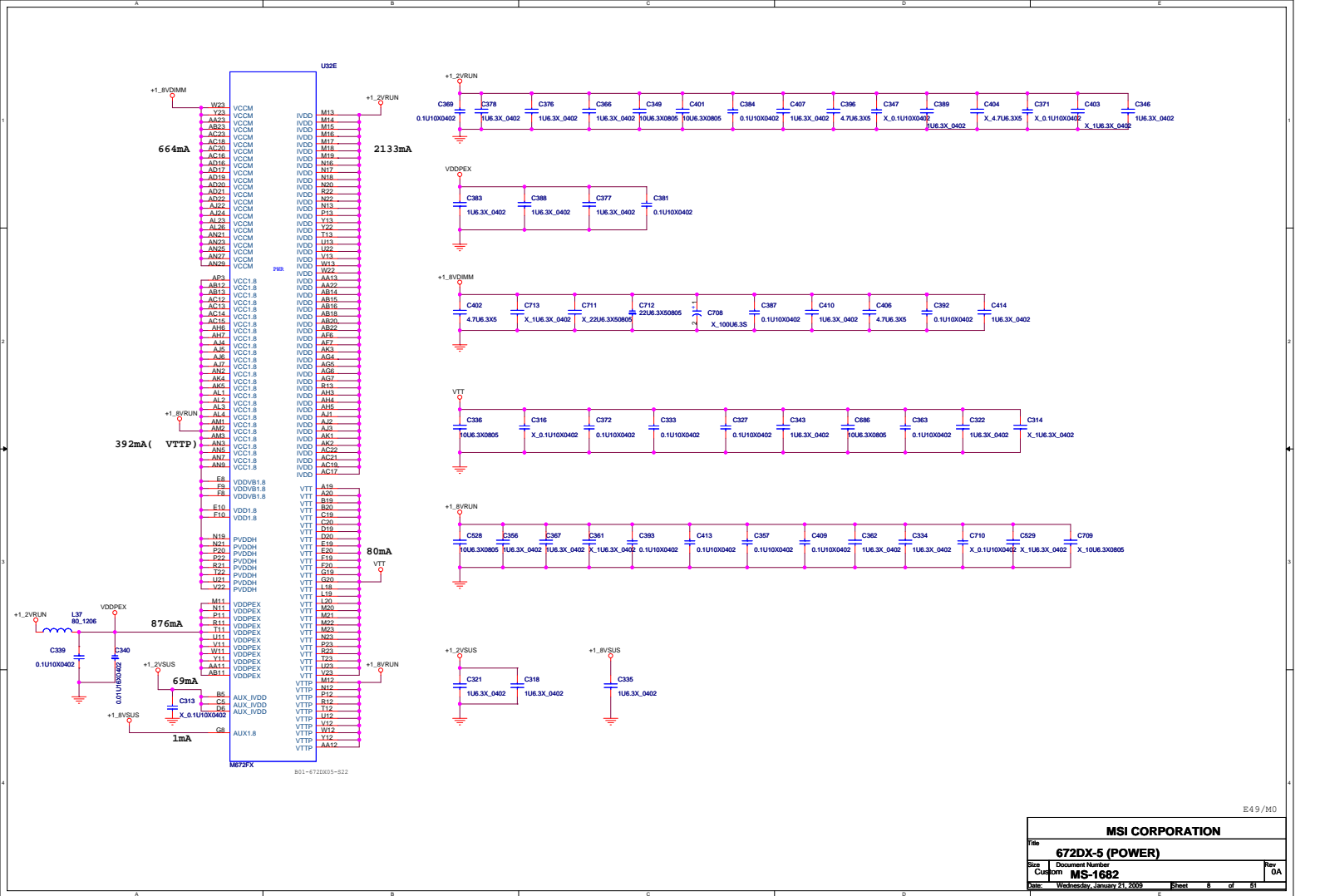




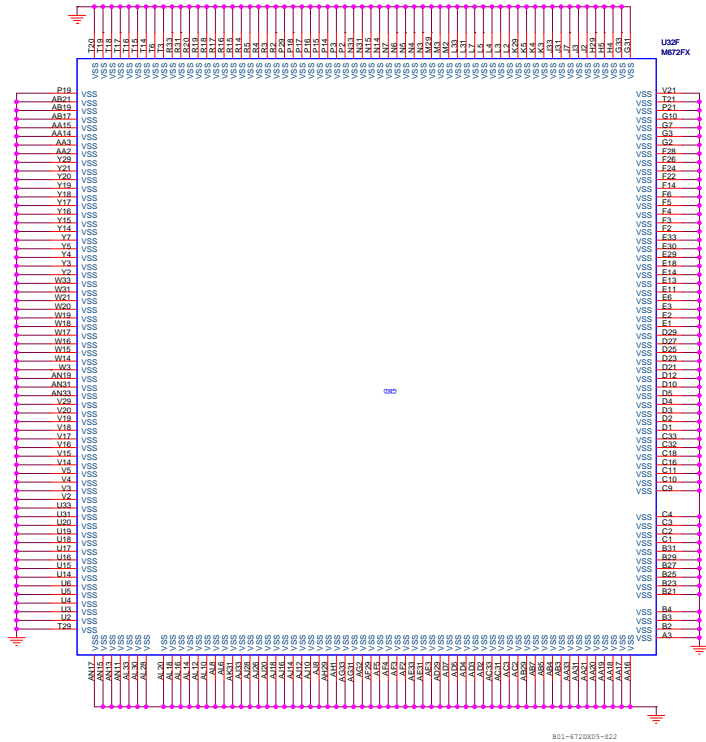
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E17/M0

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Size	Document Number	Rev	
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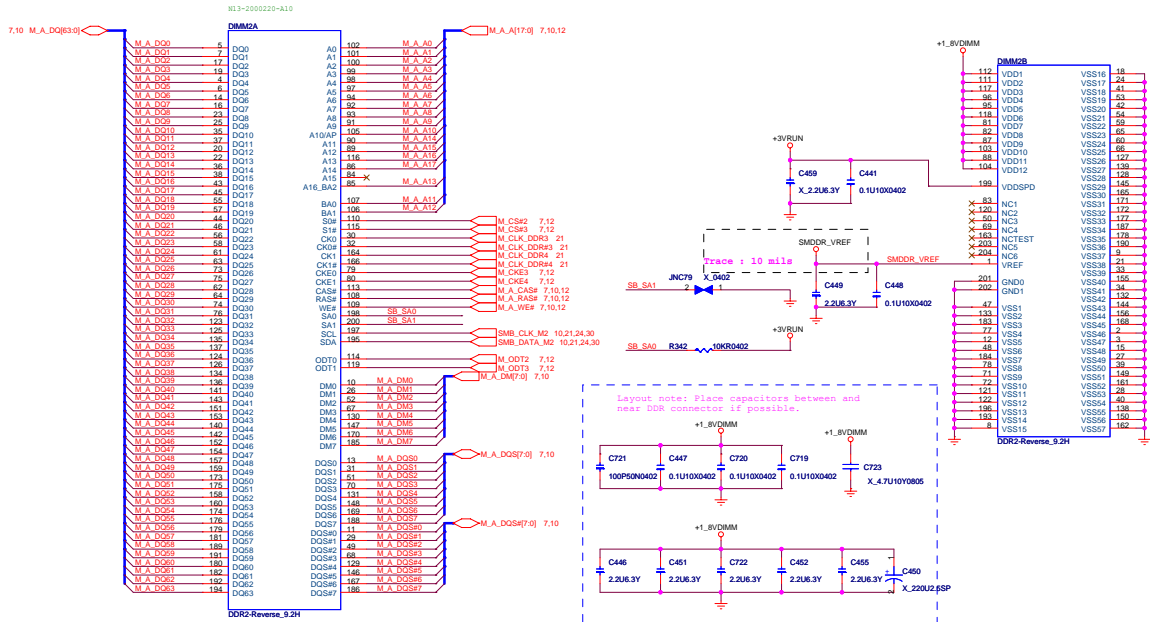
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Size: Custom	Document Number: MS-1682	Rev: 0A	
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B01-672DX5-822

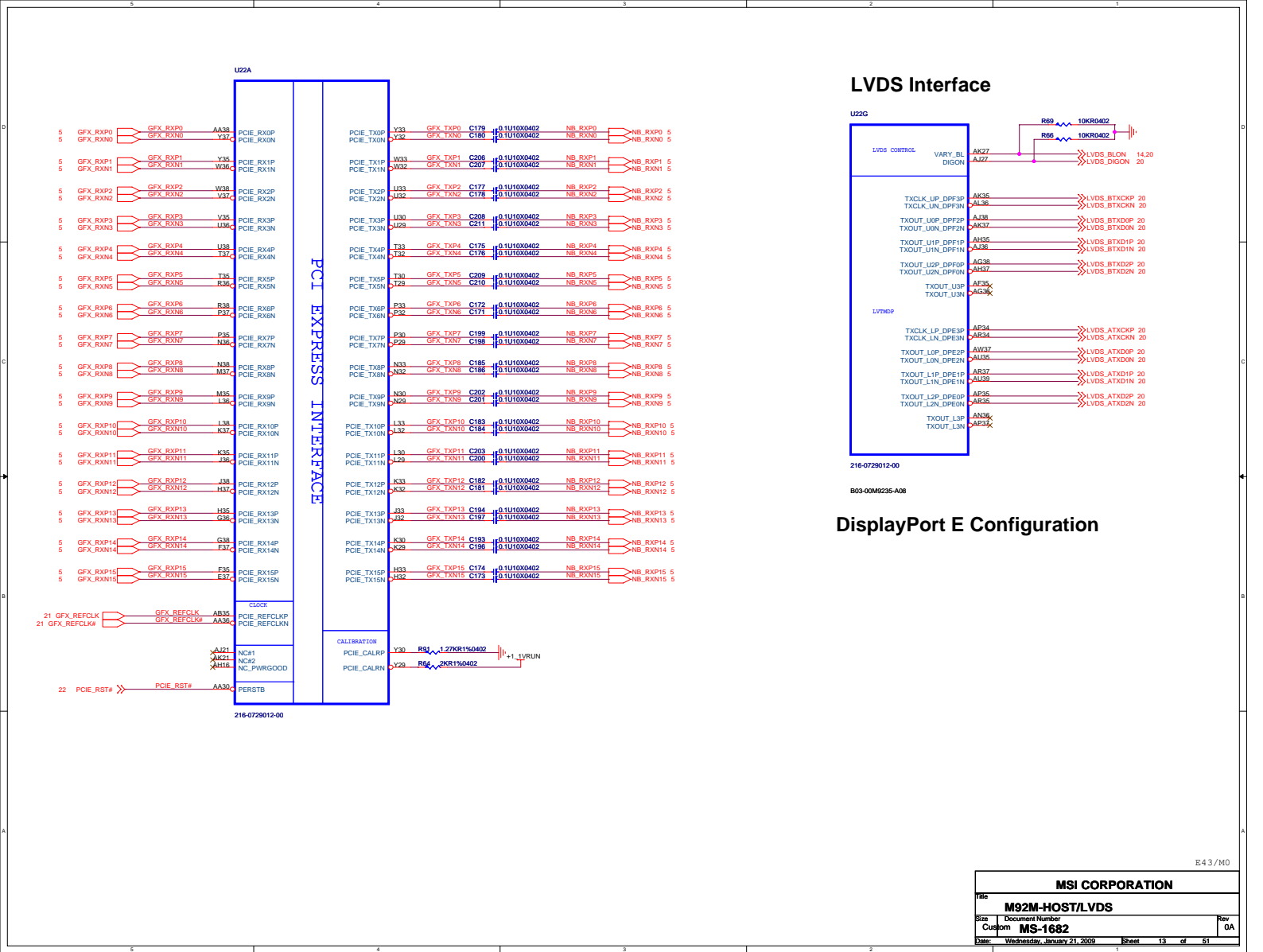
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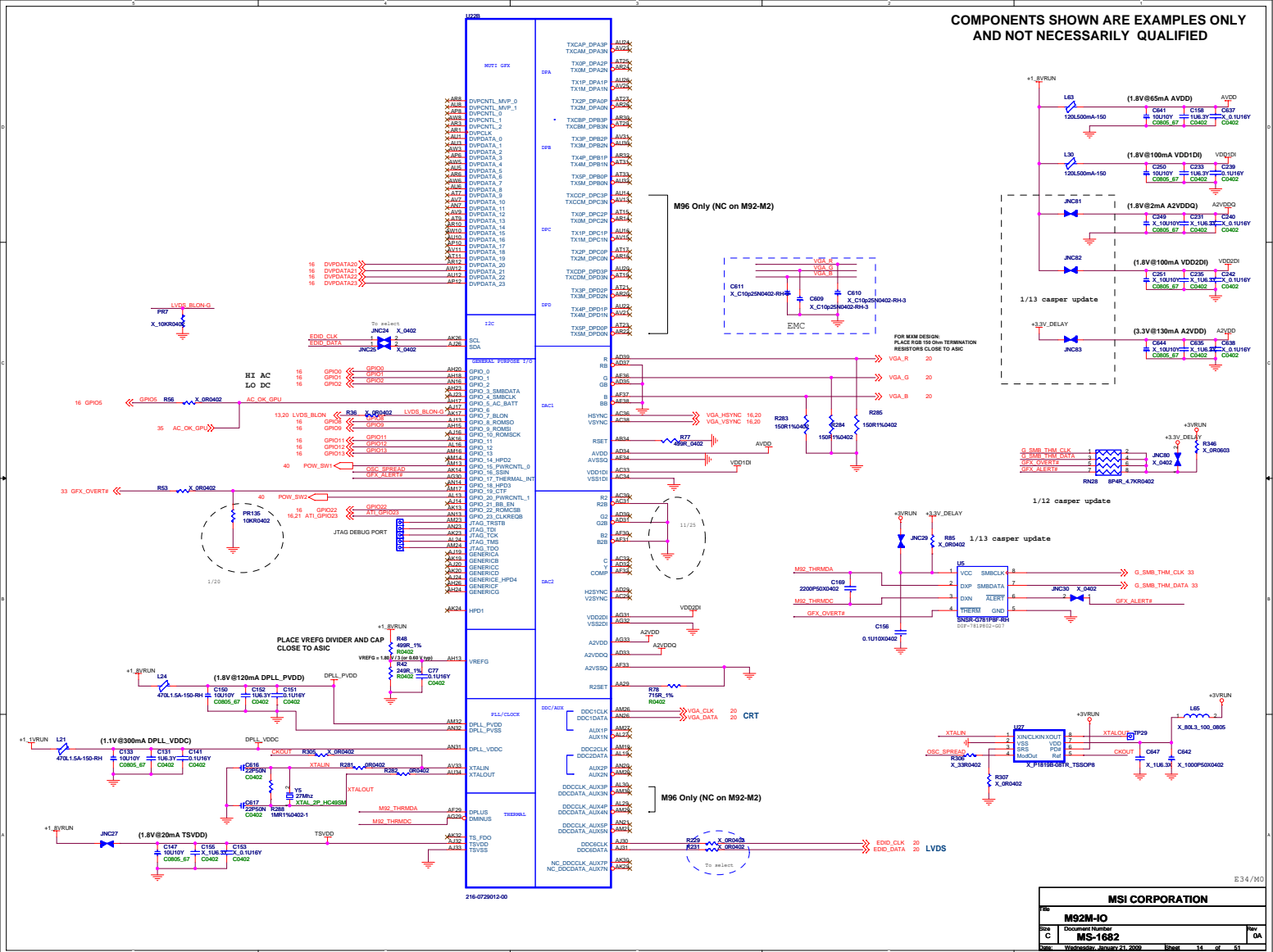


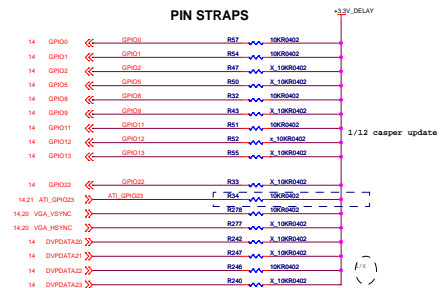
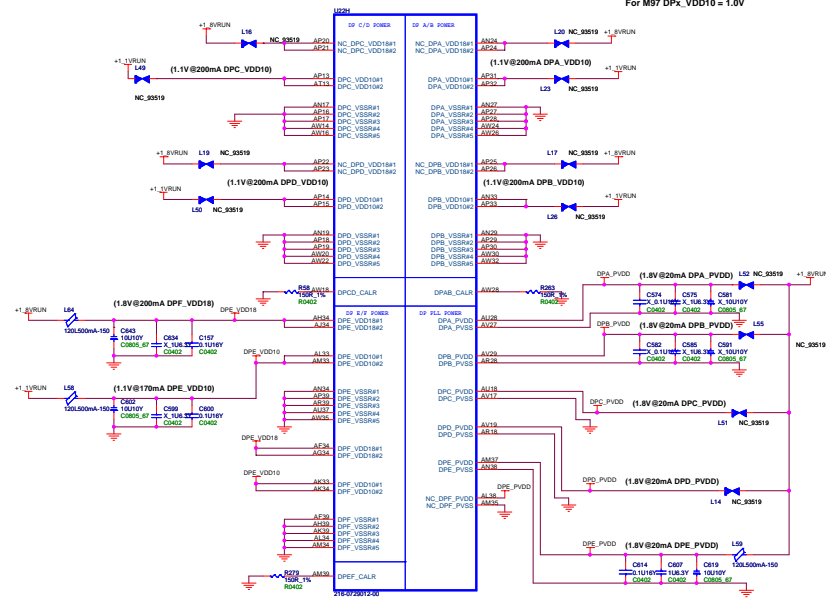
E12/M0

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File	DDR2 SODIMM 1		
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COMPONENTS SHOWN ARE EXAMPLES ONLY
AND NOT NECESSARILY QUALIFIED

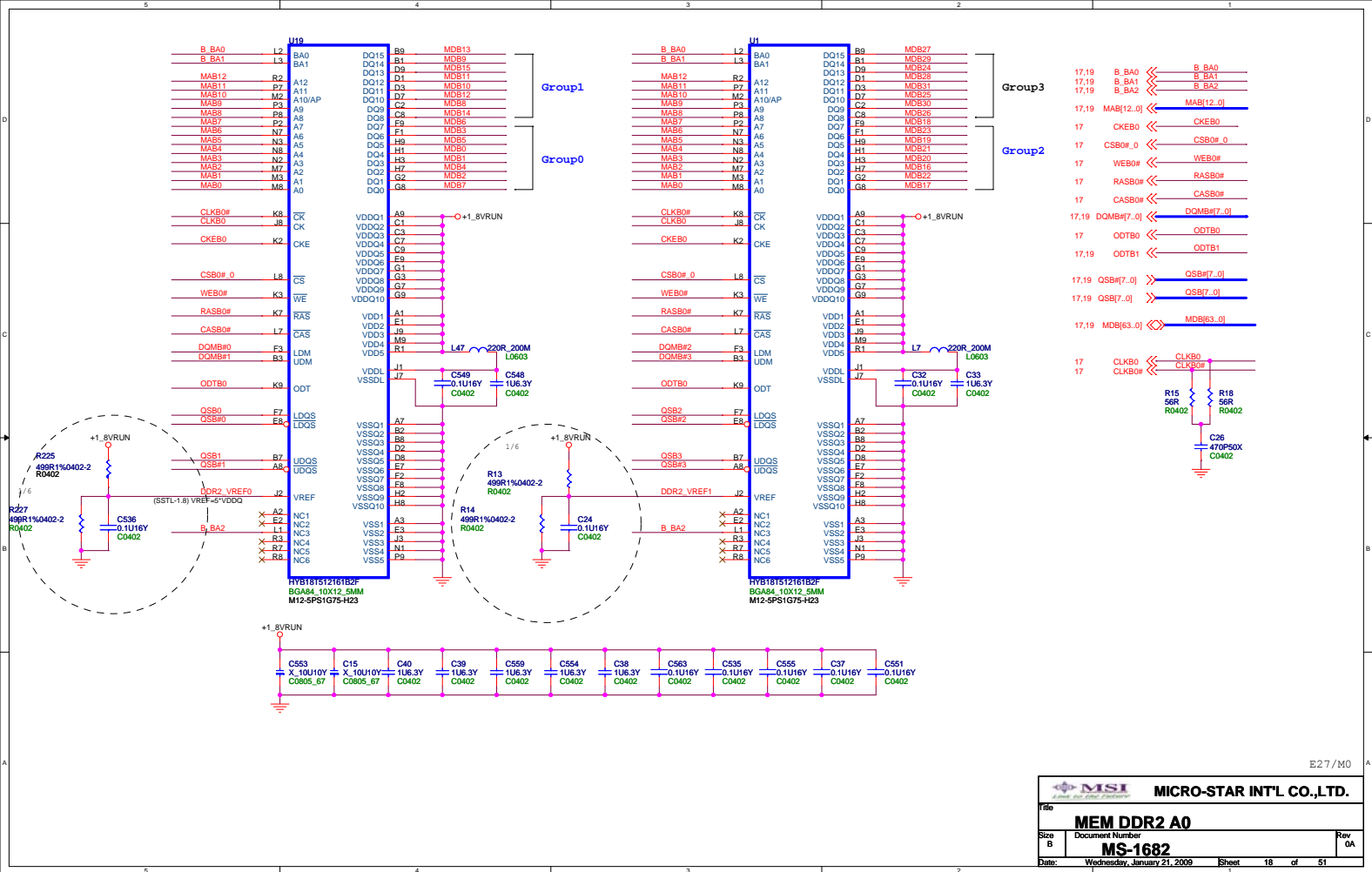


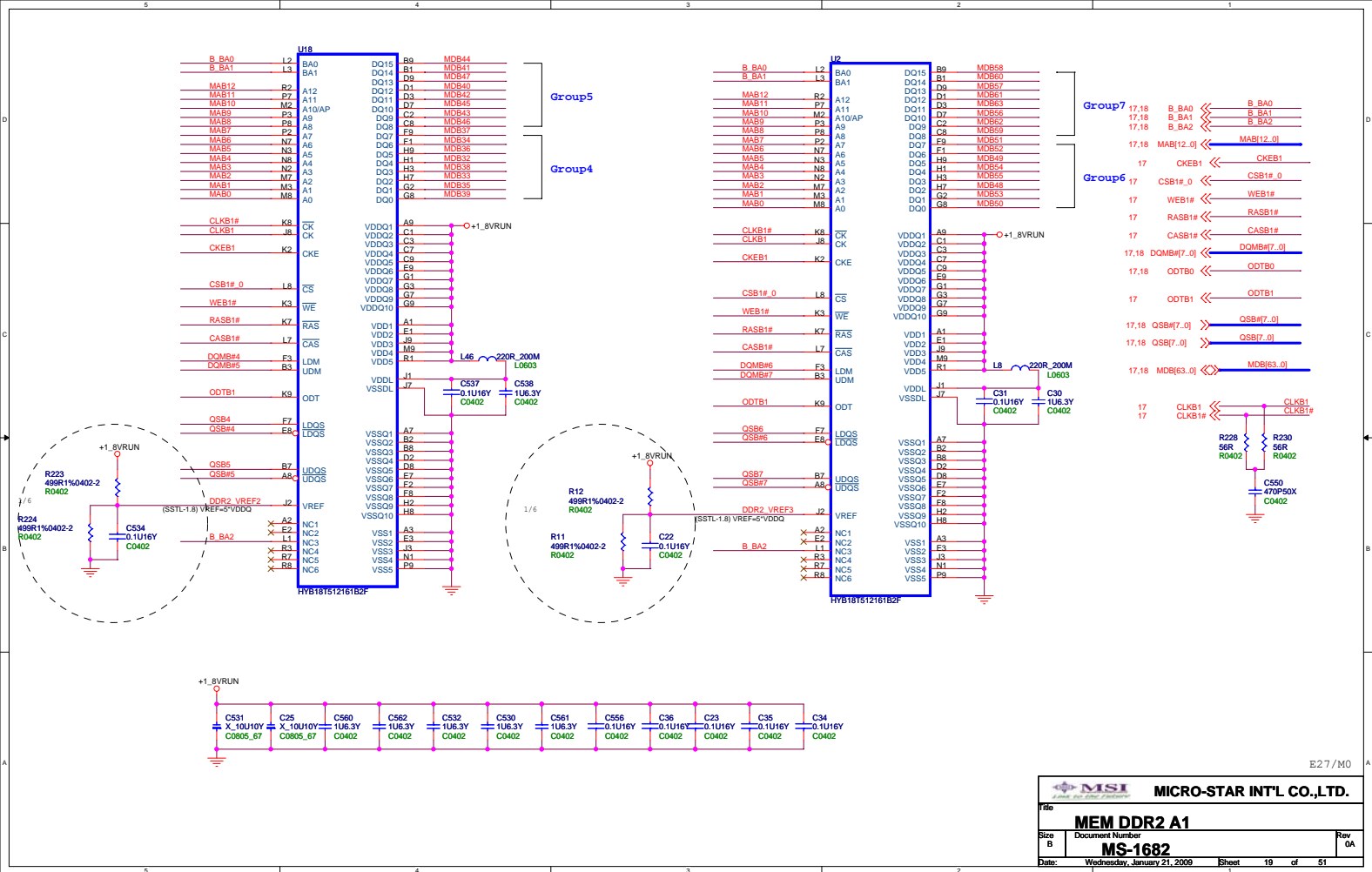


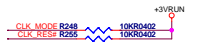
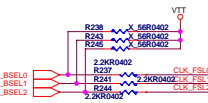
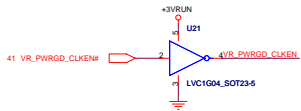
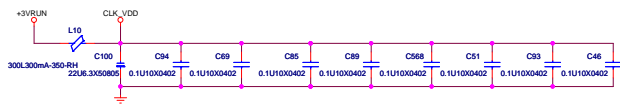
CONFIGURATION STRAPS	
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET	RECOMMENDED SETTINGS 0 = DO NOT INSTALL RESISTOR 1 = INSTALL 10K RESISTOR X = DESIGN DEPENDANT NA = NOT APPLICABLE

STRAPS		PN	DESCRIPTION OF DEFAULT SETTINGS	
	TX_PWR_ENB	GP00	Transmitter Power Savings Enable 0-20% Tx output swing for mobile mode 1-Set Tx output swing (initial setting for desktop)	1
	TX_DEMPH_EN	GP01	PCI Express Transmitter De-emphasis Enable 0-Tx de-emphasis disabled for mobile mode 1-Tx de-emphasis (initial setting for desktop)	1
	BF_GEN2_EN	GP02	0 - Automates the PCIe device as 2.0 OTs reports at power-on 1 - Automates the PCIe device as 2.0 OTs reports at power-on 2.0 OTs Capability will be verified by	0
	STRAP_BF_CLK_PM_EN	GP08	Enable CLAREGE Power Management 0-CLAREGE Power Management capability is disable 1-CLAREGE Power Management capability is enable	
	BF_VGA_DIS	GP09	VGA ENABLED	0
	BF_RX_P1_CALIB_BP	GP021	BF_RX_P1_CALIB_BP	
	BIOS_ROM_EN	GPIO_22_ROMCSB	Enable external BIOS ROM device 0-disable external BIOS ROM device 1-enable external BIOS ROM device	0
config2: 1, 0		GPIO13: 12, 0	GPIO 0 is 1,12 (CONFIG3 3.2.1.0) 0 if BIOS_ROM_EN = 1 then Config3[12] defines the rom type 0 if BIOS_ROM = 0 then Config3[12] defines the Romtype size	0 0 1 256MB
Mem type		DVDA[Q21.21.22]	0 If VPP_DEVICE_STRAP_EN = 1 then this pin is used to sense whether a VPP slave device is connected to the VPP device 0 If VPP_DEVICE_STRAP_EN = 0 then this pin is not used as a strap at all (i.e. its value during reset is unimportant), and it can be used as a regular GPIO	0 0 0 vendor
VPP_DEVICE_STRAP_ENA	V2YN2N			
REVIO	GENERIC	HS02NC		0
REVIO	GENERIC	HS02NC		0
AUX[0]	VSYN			1

DV DATA	23	22	21	20	
SAMSUNG	0	0	0	0	32*16
Hynix	0	0	0	1	32*16
SAMSUNG	0	0	1	0	64*16
Hynix	0	1	0	0	64*16





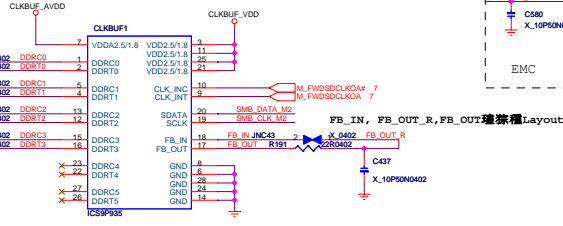
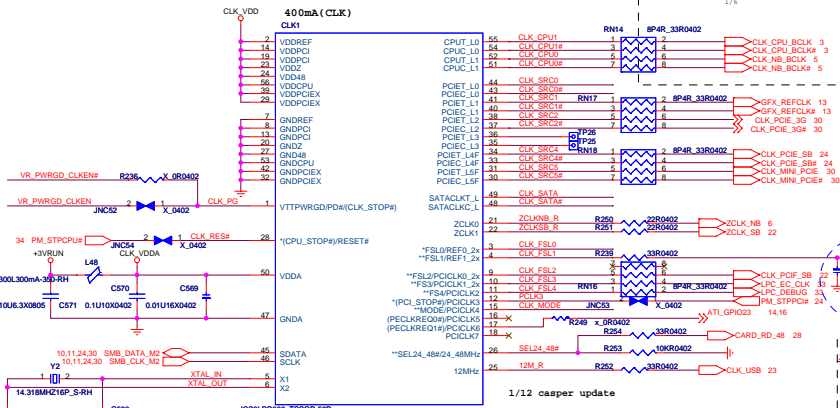


Strapping Configuration(IC5)

PIN#	High	Low(Default)
15	Pin 16/17 : PECLKREQ	Pin 16/17 : PCICLK

CPU Table			FSB Freq (MHz)
BSEL[2]	BSEL[1]	BSEL[0]	
L	H	H	667 MHz
L	H	L	800 MHz
L	L	L	1066 MHz

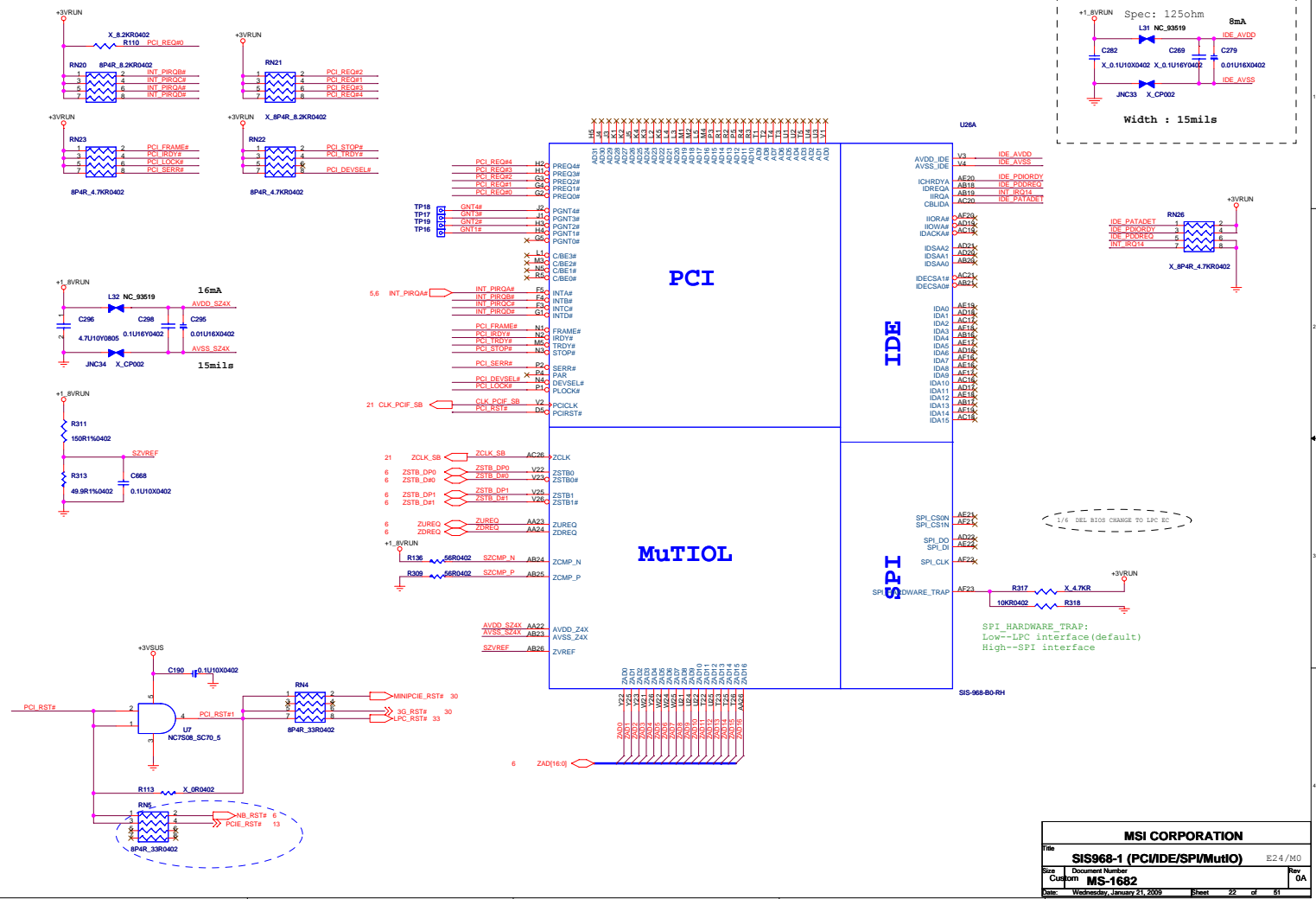
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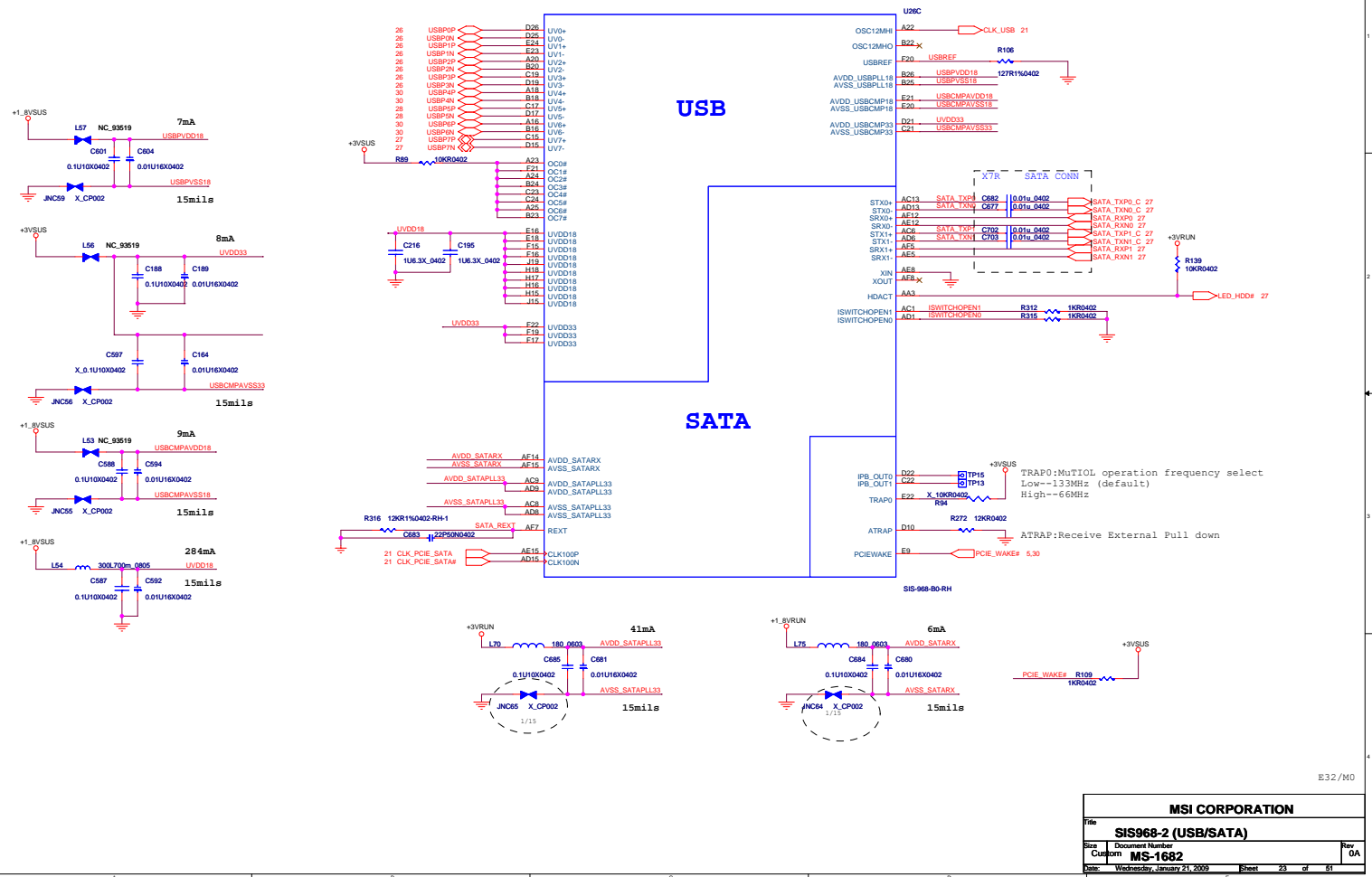


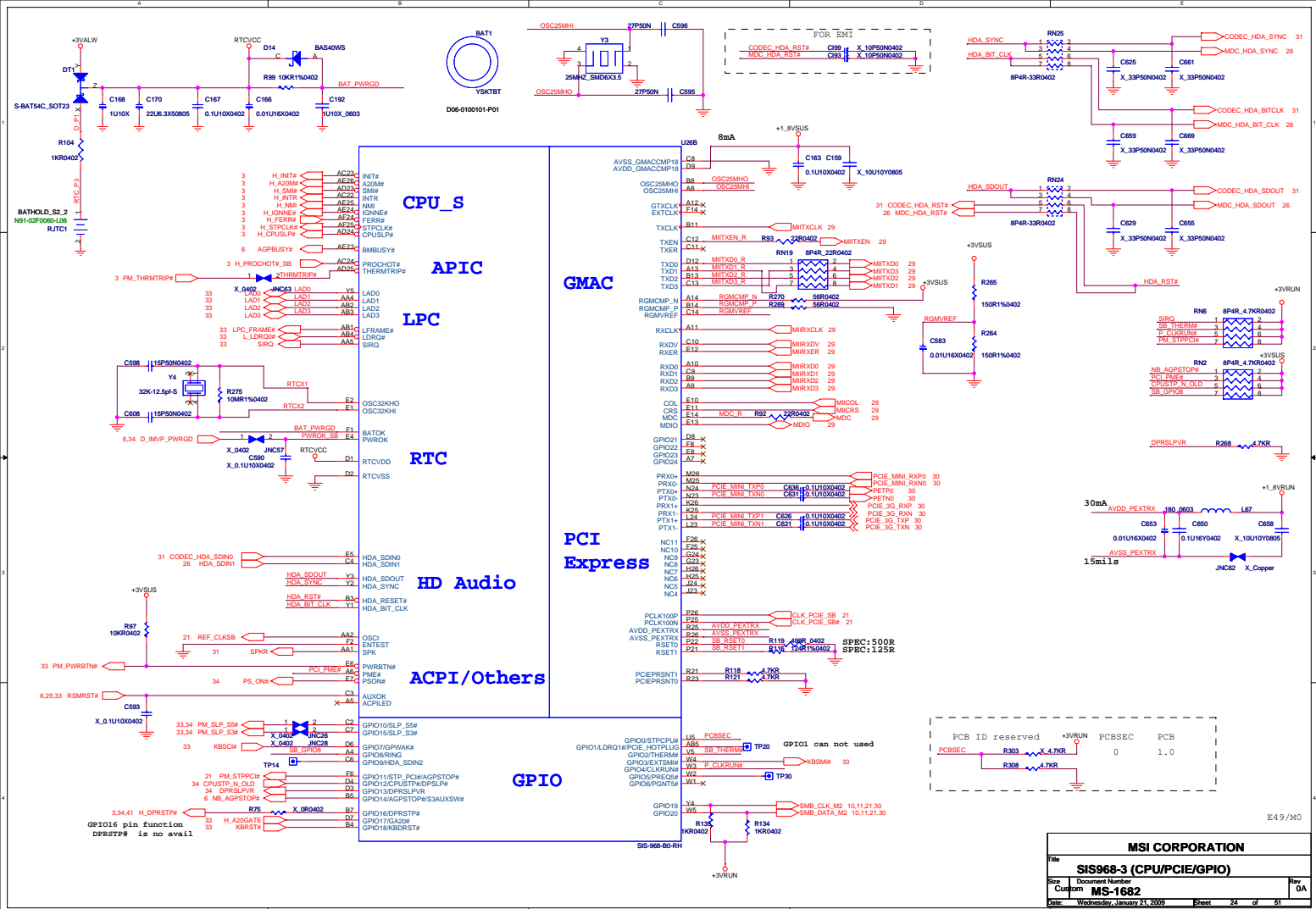
1/16 JNC39,40,41,42 +1.5" AND JNC43 +2"FOR 3D MARK 06 BUG ,

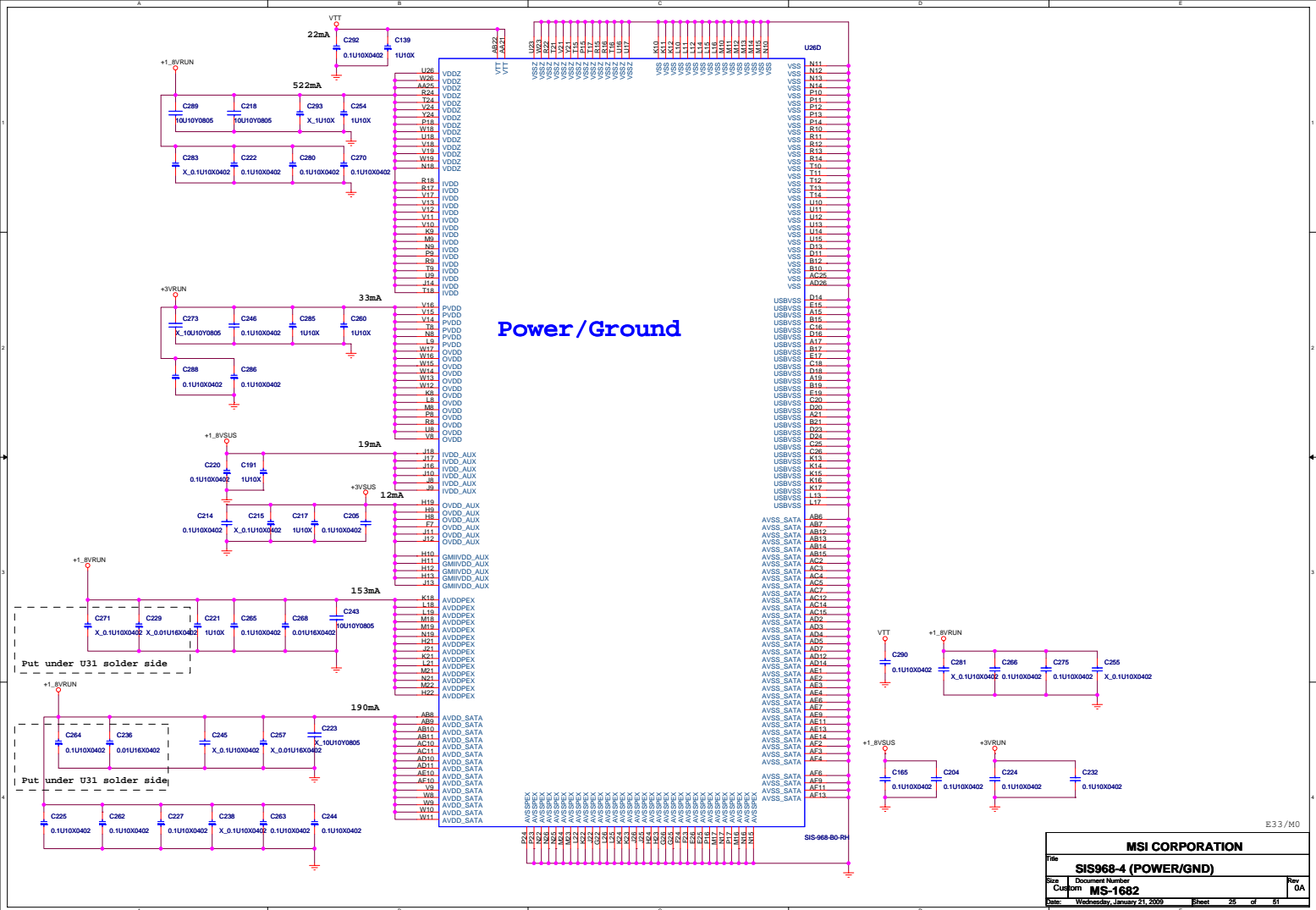
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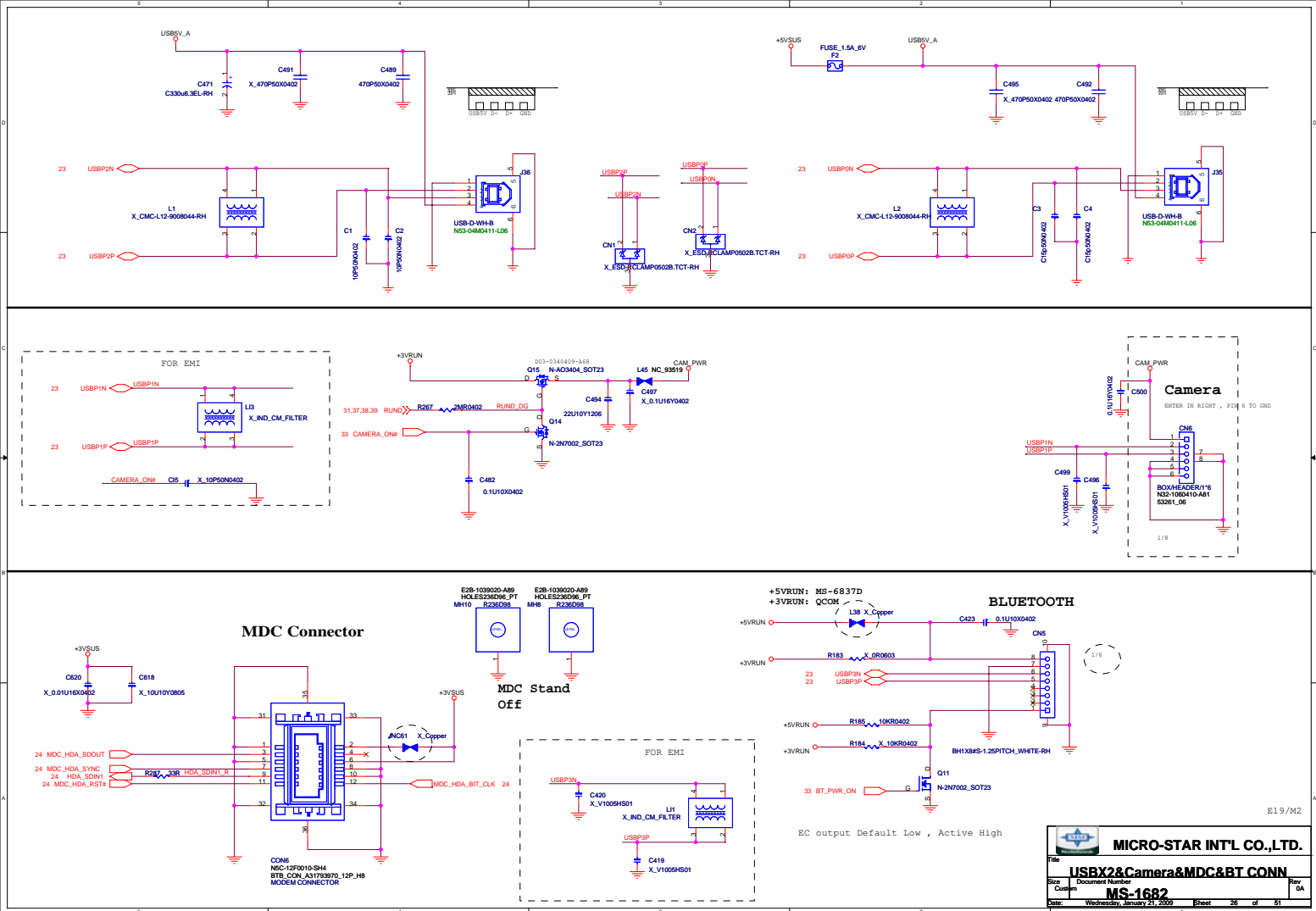
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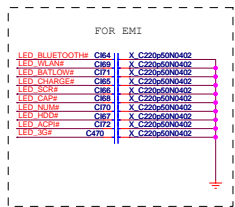
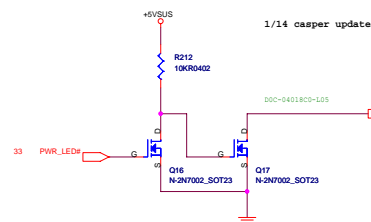
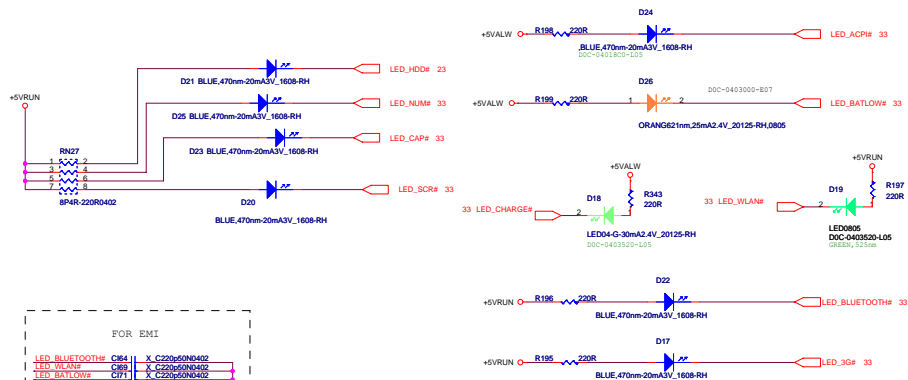
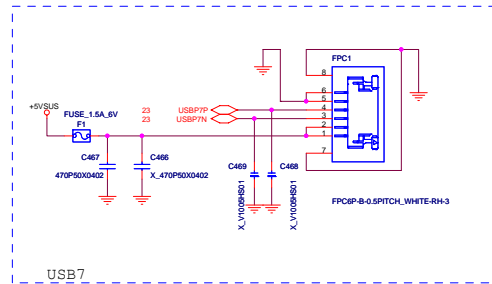
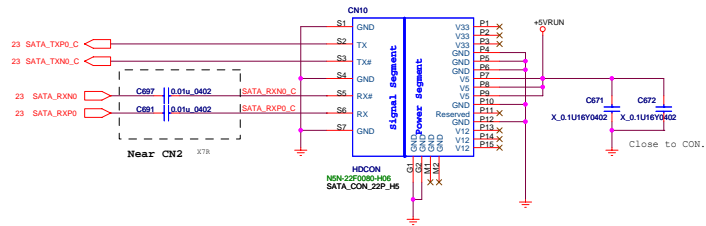
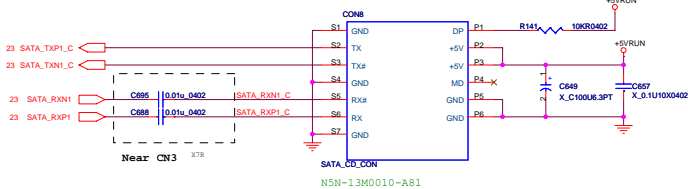
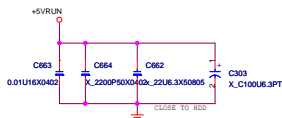






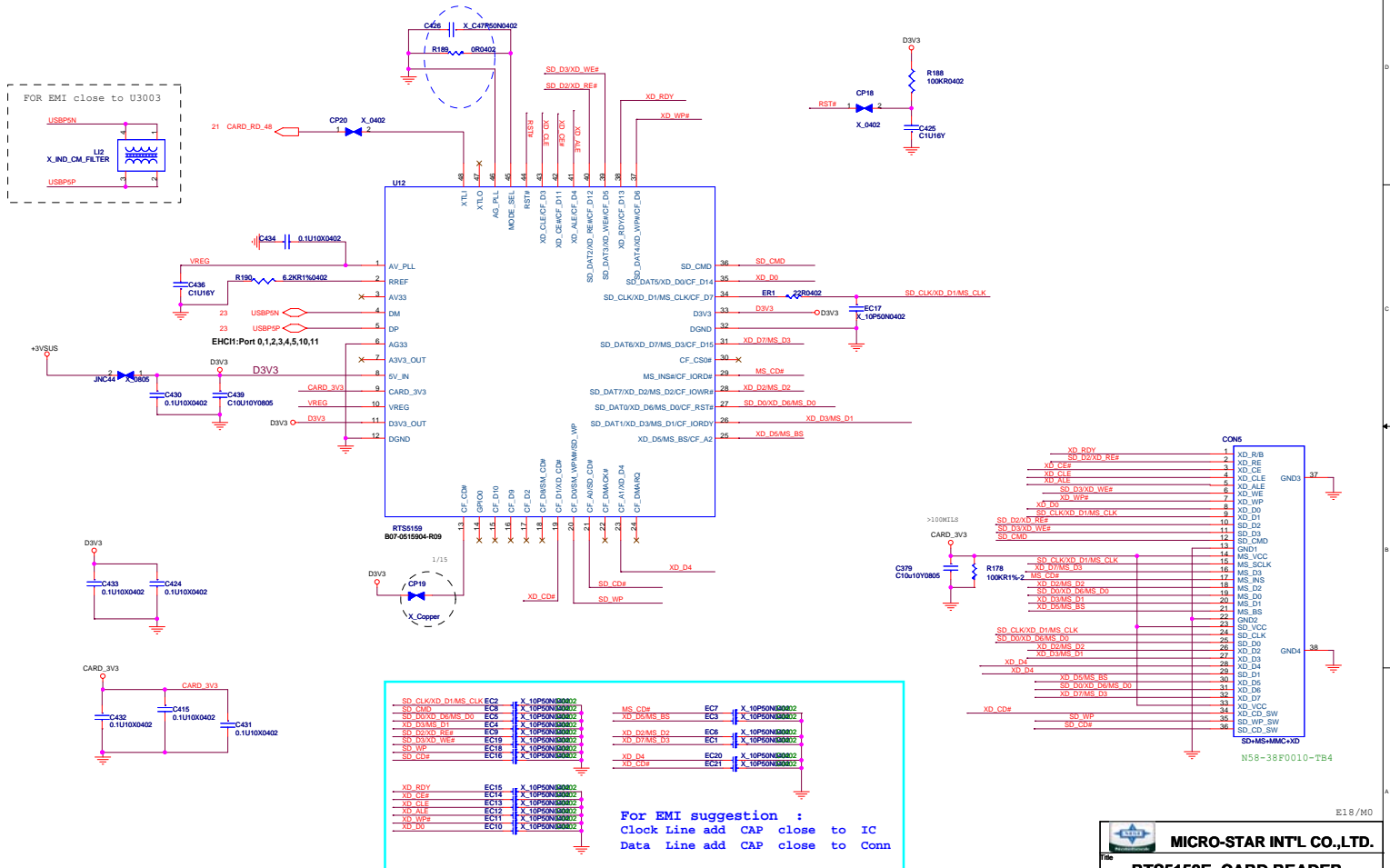


MICRO-STAR INT'L CO.,LTD.			
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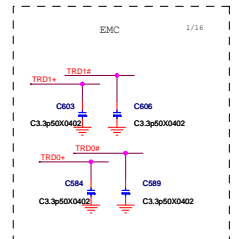
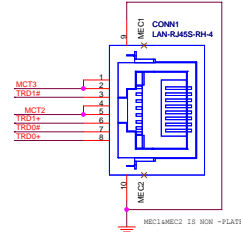
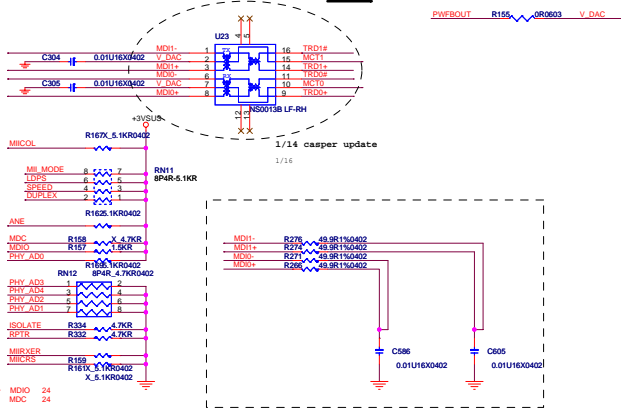
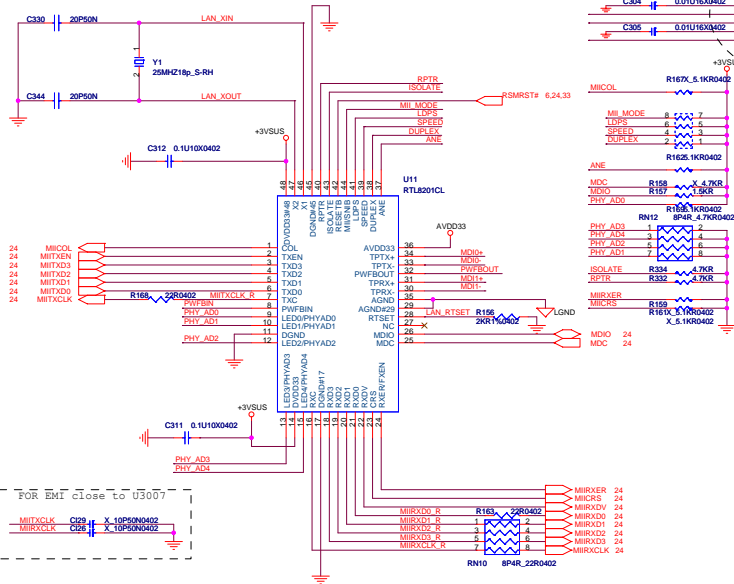
MICRO-STAR INT'L CO.,LTD.			
Title: HDD & ODD CONN & USB7 & LED			
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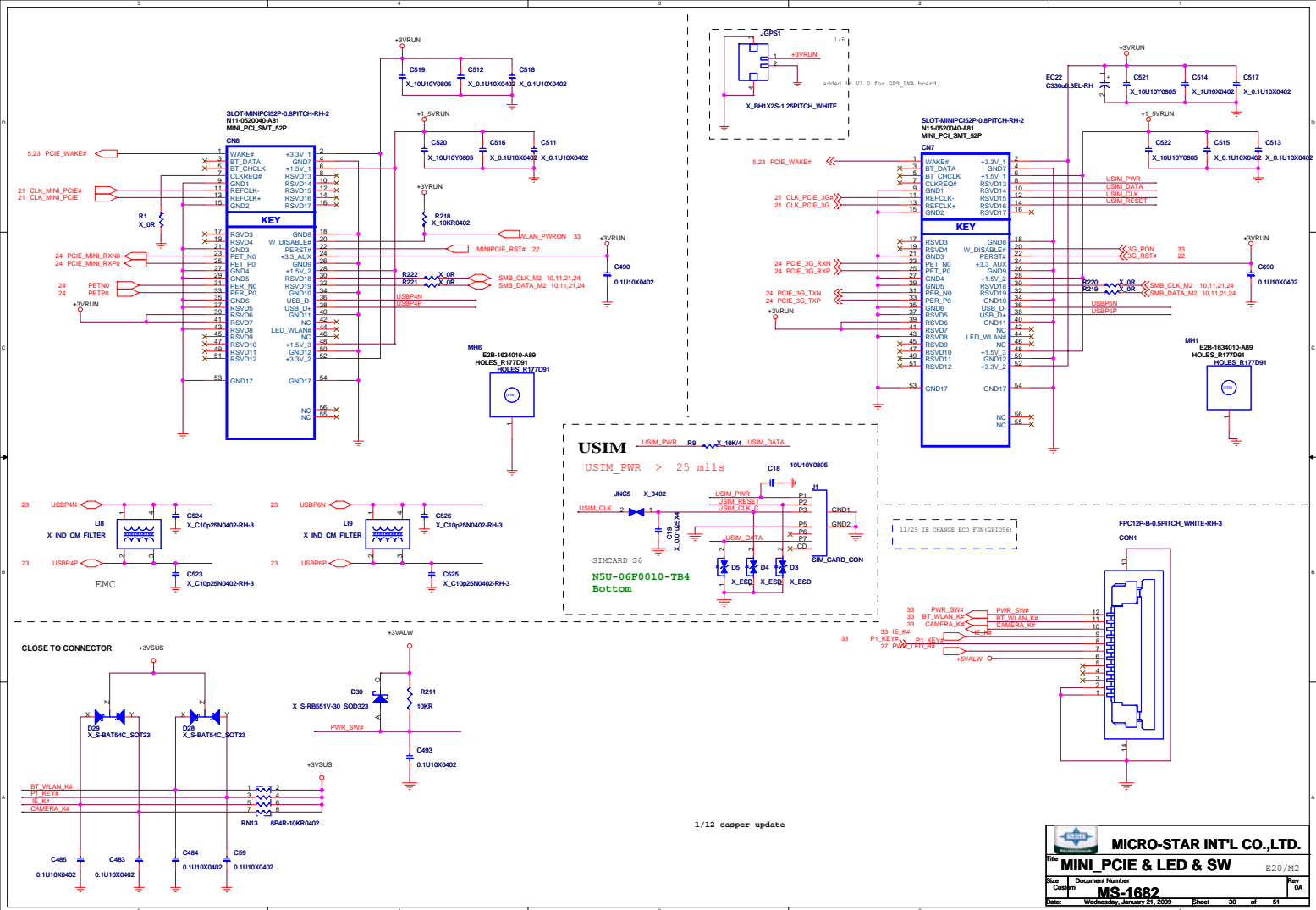


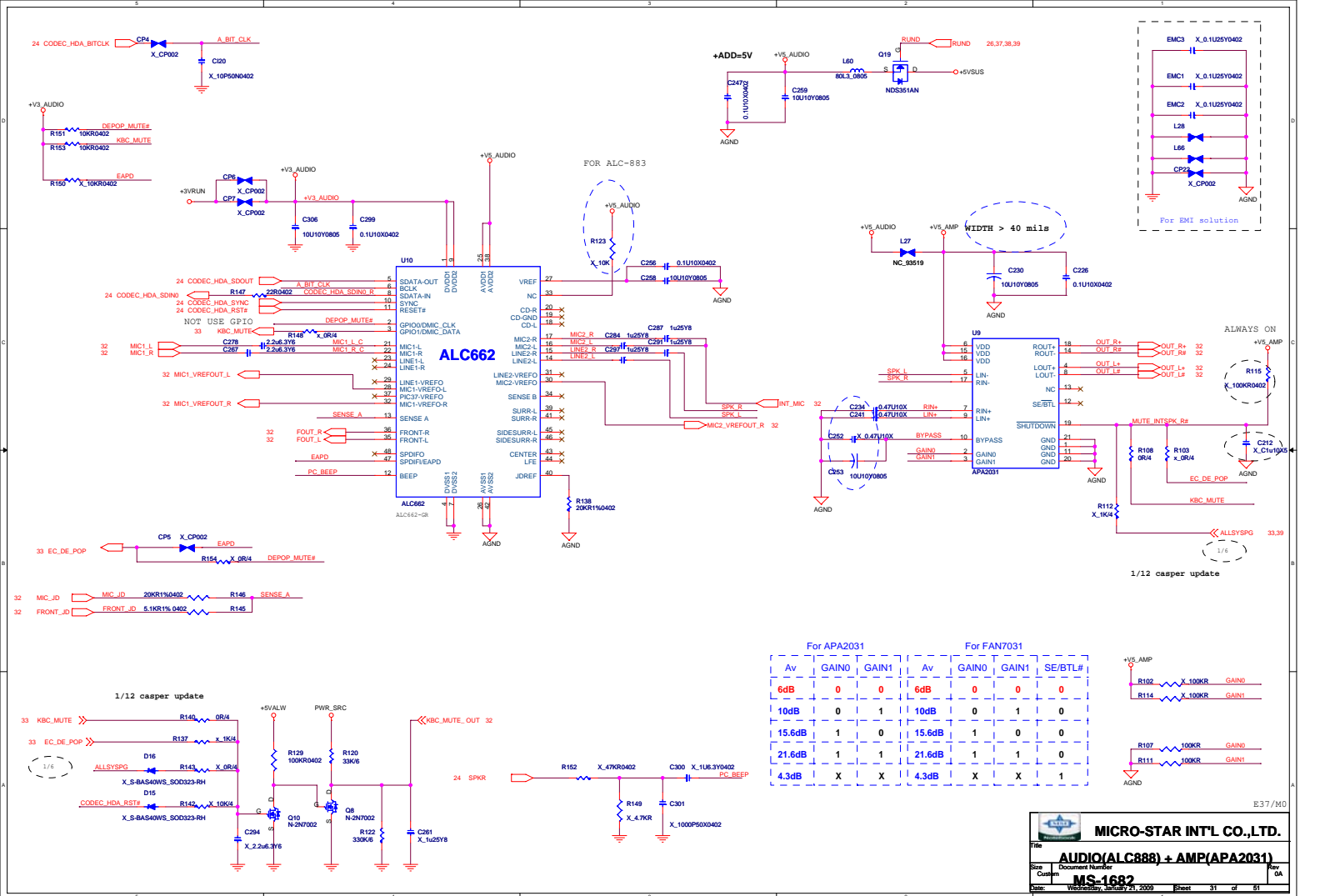
LAN MAGNETICS

1/12 casper update

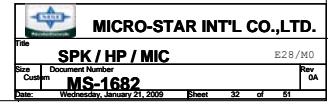


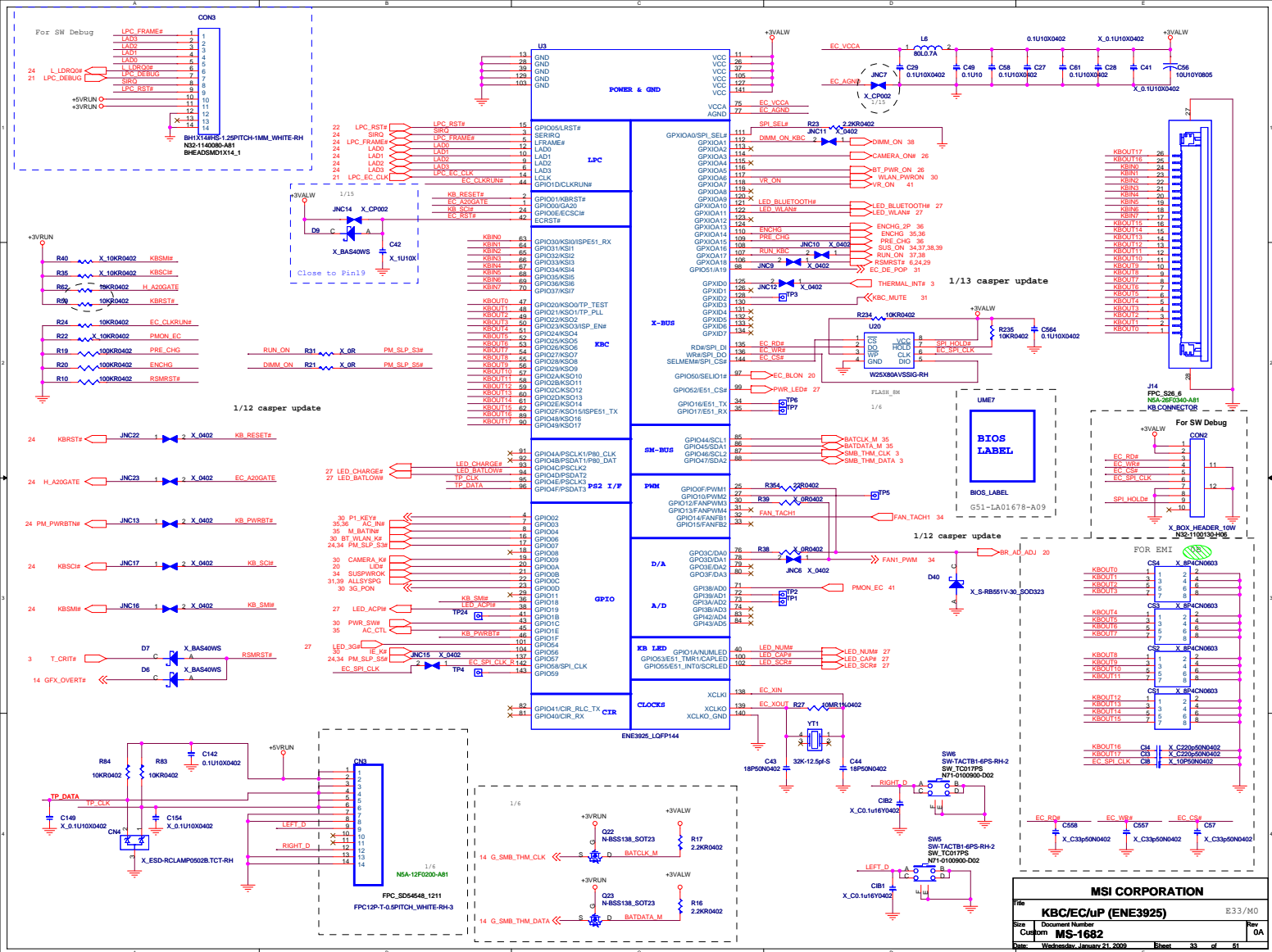
MICRO-STAR INT'L CO.,LTD.			
PHY LAN (RTL8201CL)			
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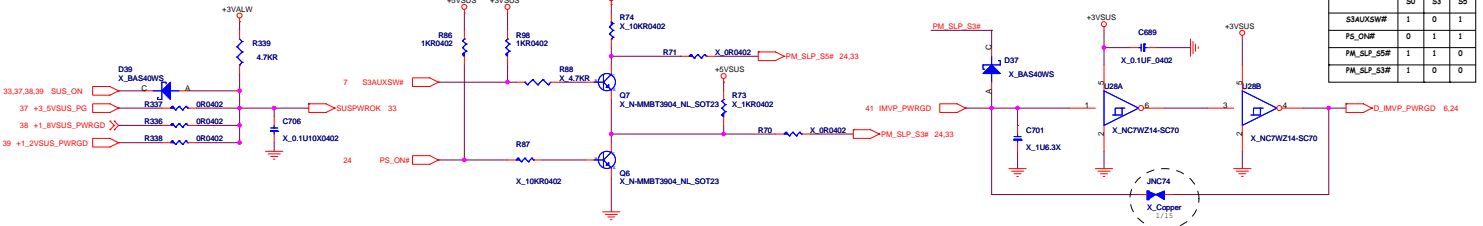
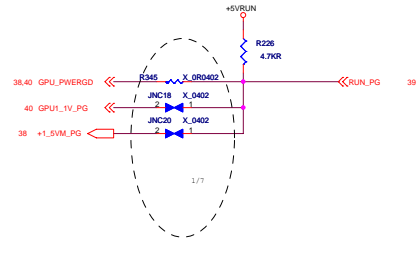
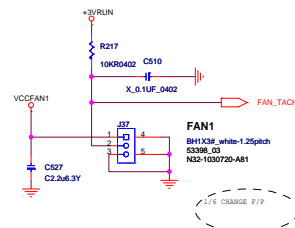
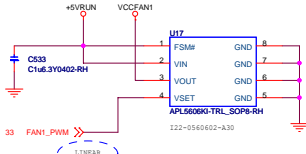


HP IN IS LOW

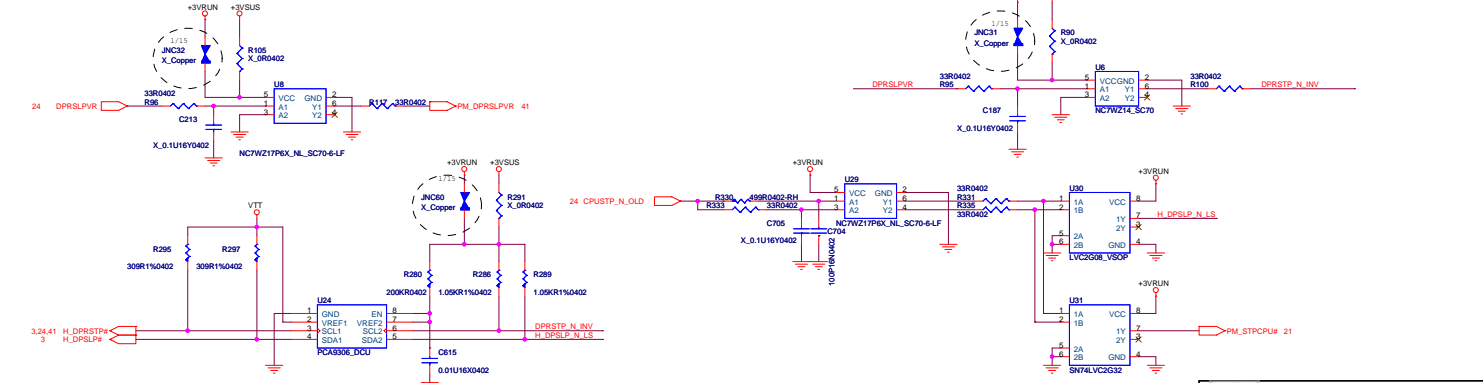




VCCFAN1=1.6+FAN1_PWM



	S0	S3	S5
S3AUXSW#	1	0	1
PS_ON#	0	1	1
PM_SLP_S#	1	1	0
PM_SLP_S#	1	0	0



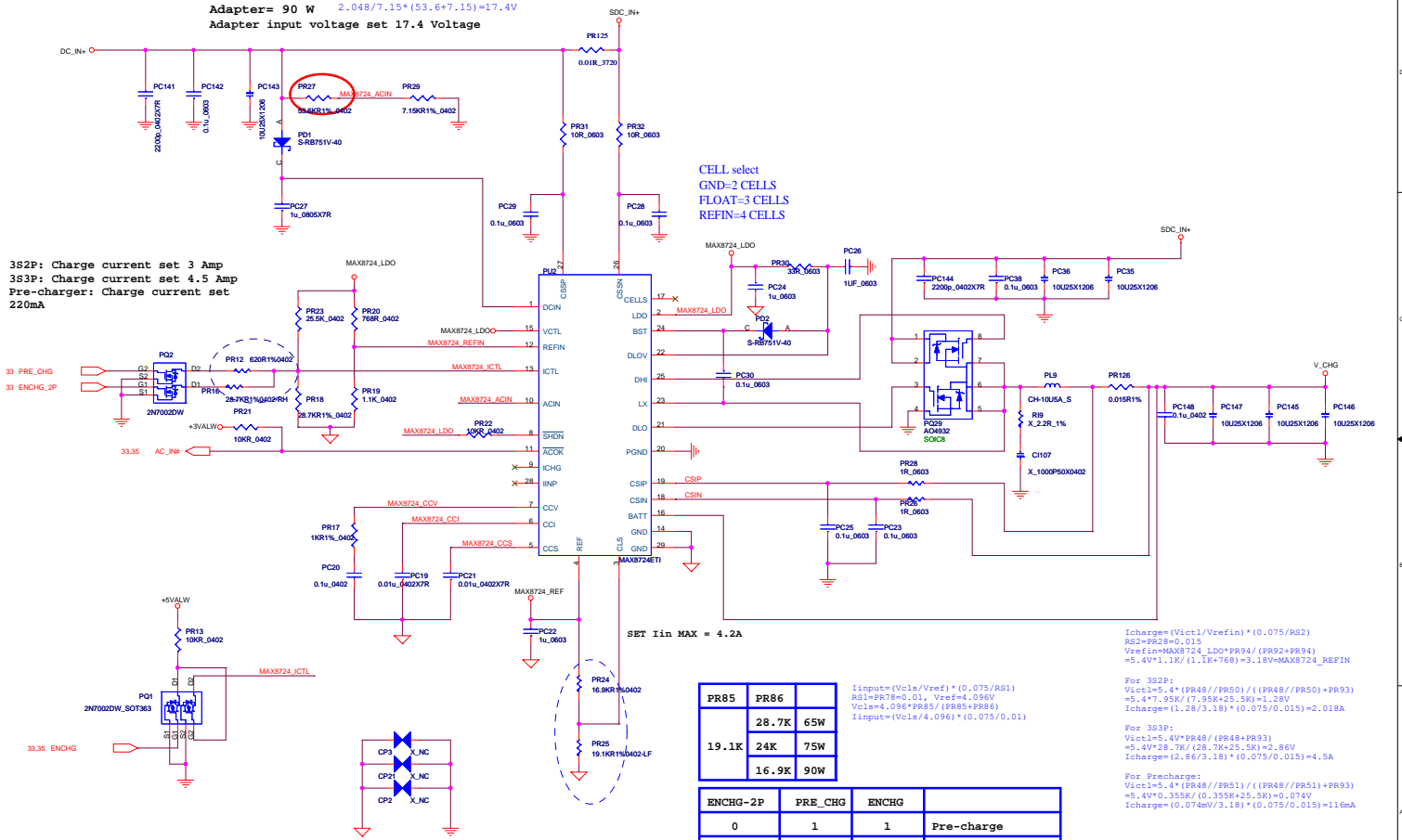
MICRO-STAR INT'L CO.,LTD.

File: **PWRGD & FAN & C3/C4** E33/M0

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Adapter= 90 W $2.048/7.15 \times (53.6+7.15)=17.4V$
 Adapter input voltage set 17.4 Voltage



CELL select
 GND=2 CELLS
 FLOAT=3 CELLS
 REFIN=4 CELLS

SET Iin MAX = 4.2A

PR85	PR86	
19.1K	28.7K	65W
	24K	75W
	16.9K	90W

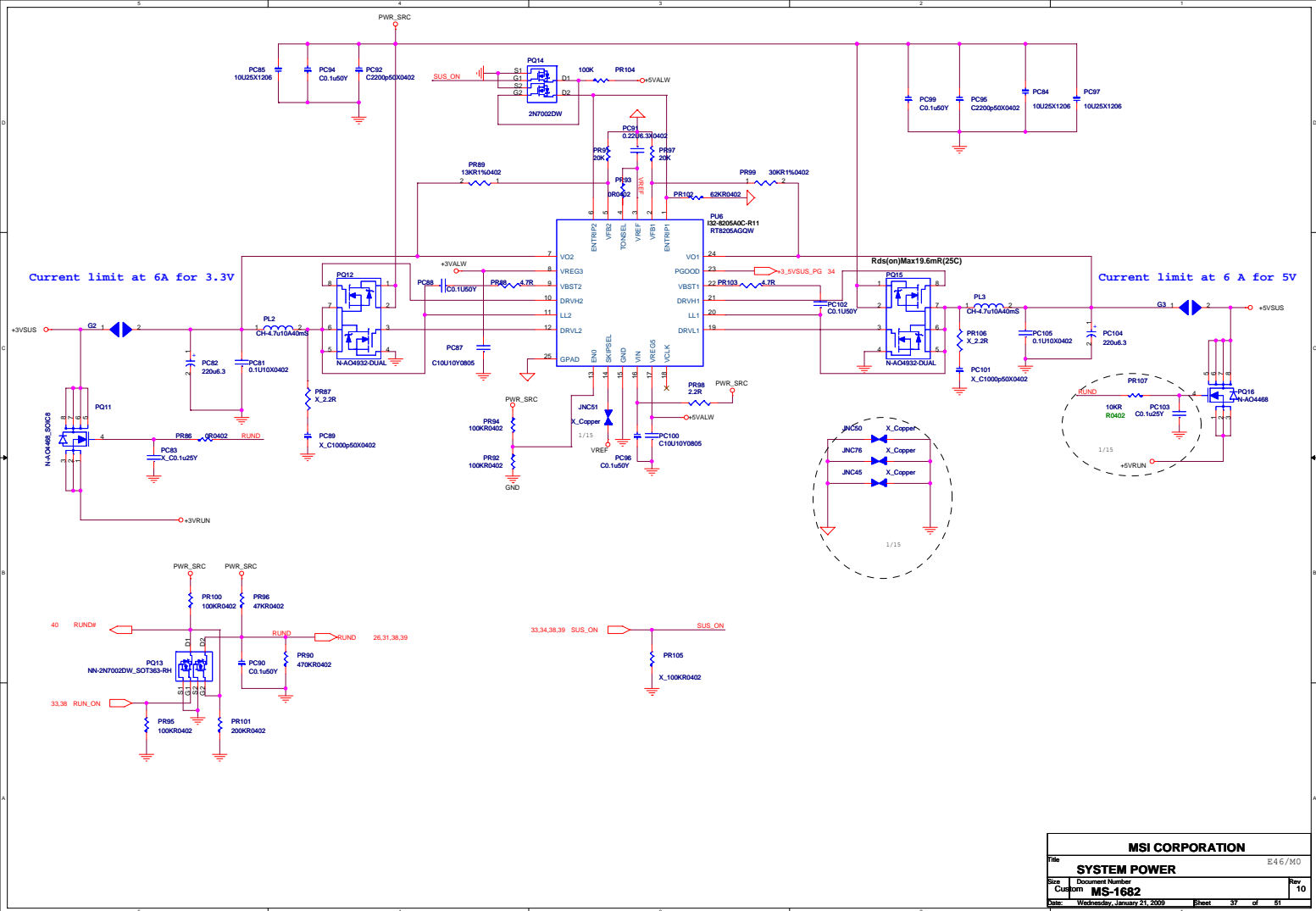
ENCHG-2P	PRE_CHG	ENCHG	
0	1	1	Pre-charge
1	0	1	3S2P-Fast charge
0	0	1	3S3P-Fast charge
0	0	0	STOP CHARGE

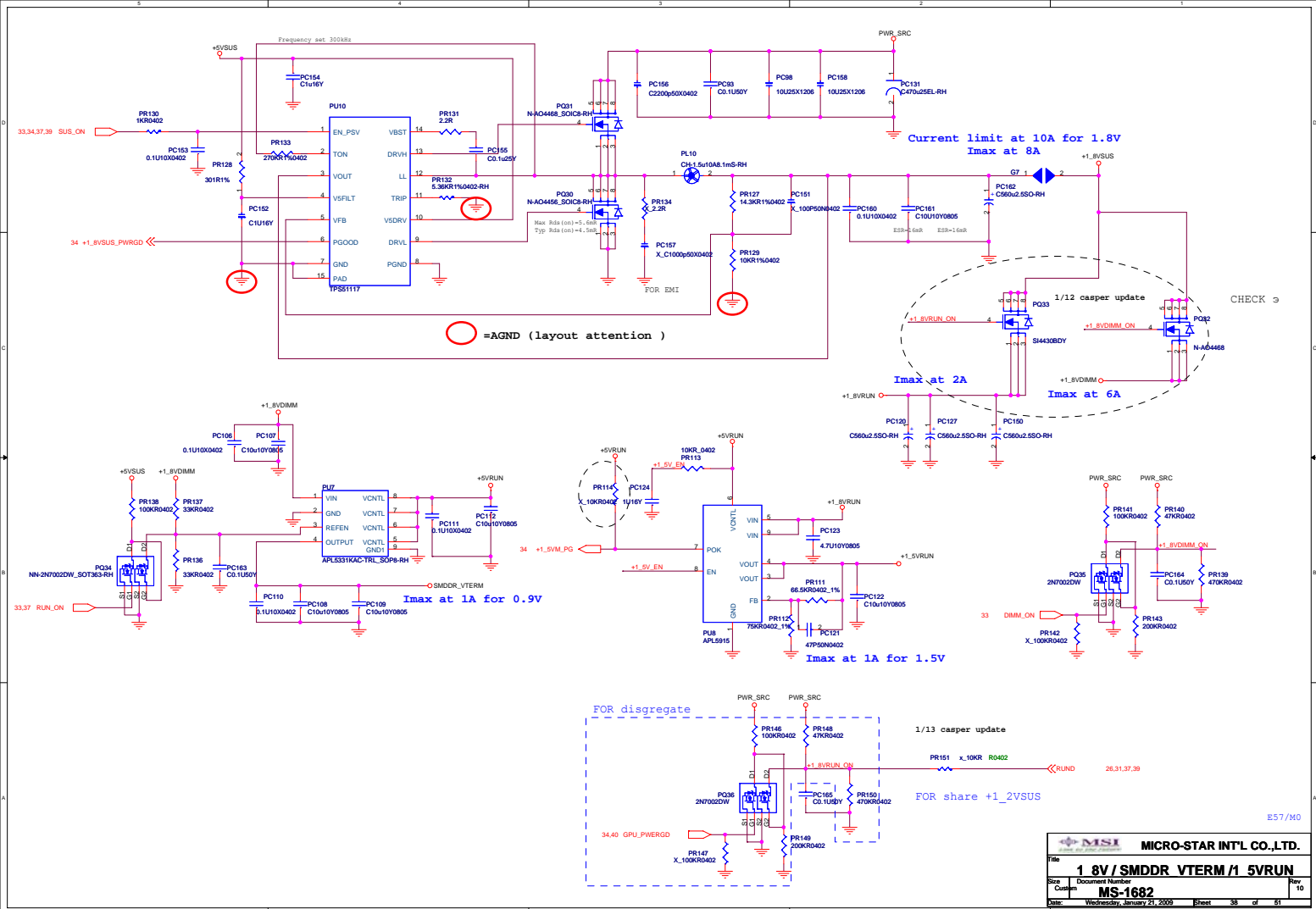
$I_{charge} = (V_{ict1}/V_{ref}) \times (0.075/RS2)$
 $RS2 = PR28 = 0.015$
 $V_{ref} = MAX8724_LDO \times PR94 / (PR92 + PR94)$
 $= 5.4V \times 1.1K / (1.1K + 768) = 3.18V = MAX8724_REFIN$
 For 3S2P:
 $V_{ict1} = 5.4V \times (PR48 / PR50) / ((PR48 / PR50) + PR93)$
 $= 5.4V \times 7.95K / (7.95K + 25.5K) = 1.28V$
 $I_{charge} = (1.28V / 3.18V) \times (0.075 / 0.015) = 2.018A$
 For 3S3P:
 $V_{ict1} = 5.4V \times PR48 / (PR48 + PR93)$
 $= 5.4V \times 28.7K / (28.7K + 25.5K) = 2.86V$
 $I_{charge} = (2.86V / 3.18V) \times (0.075 / 0.015) = 4.5A$
 For Precharge:
 $V_{ict1} = 5.4V \times (PR48 / PR51) / ((PR48 / PR51) + PR93)$
 $= 5.4V \times 0.355K / (0.355K + 25.5K) = 0.074V$
 $I_{charge} = (0.074V / 3.18V) \times (0.075 / 0.015) = 116mA$

MICRO-STAR INT'L CO.,LTD.

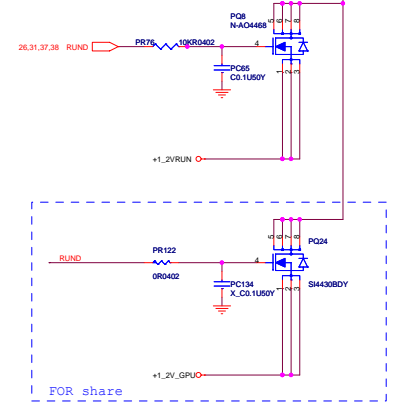
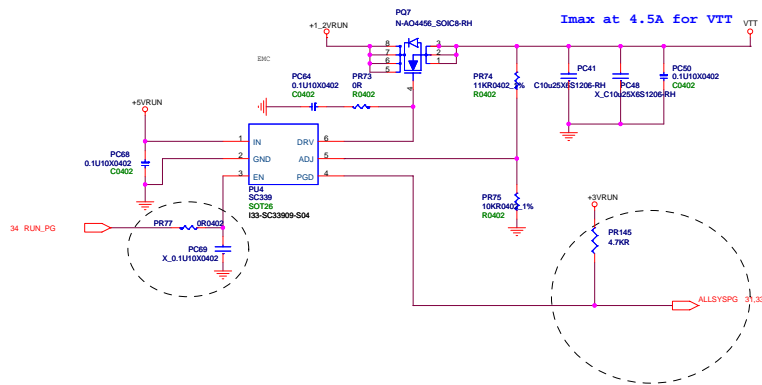
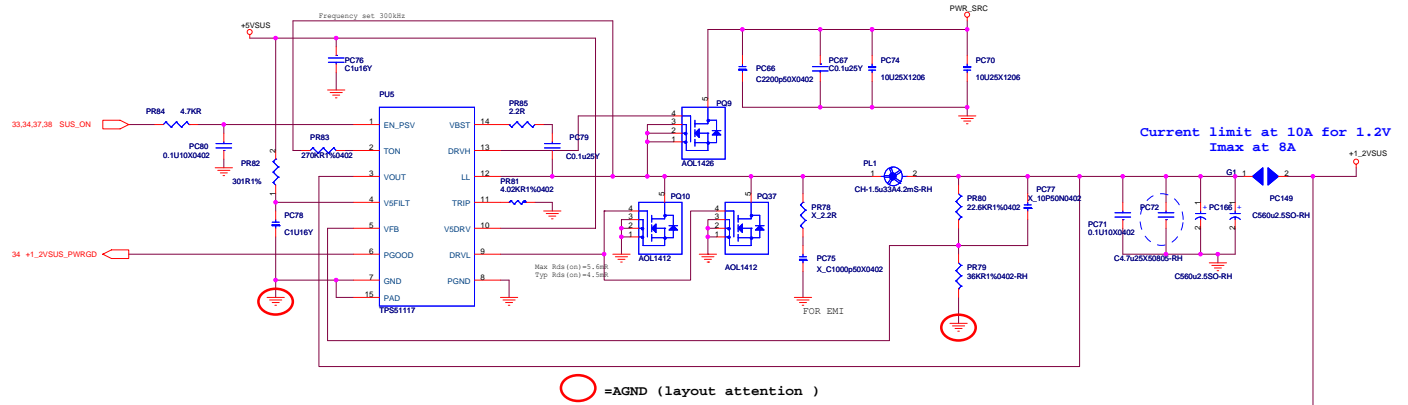
Battery Charger

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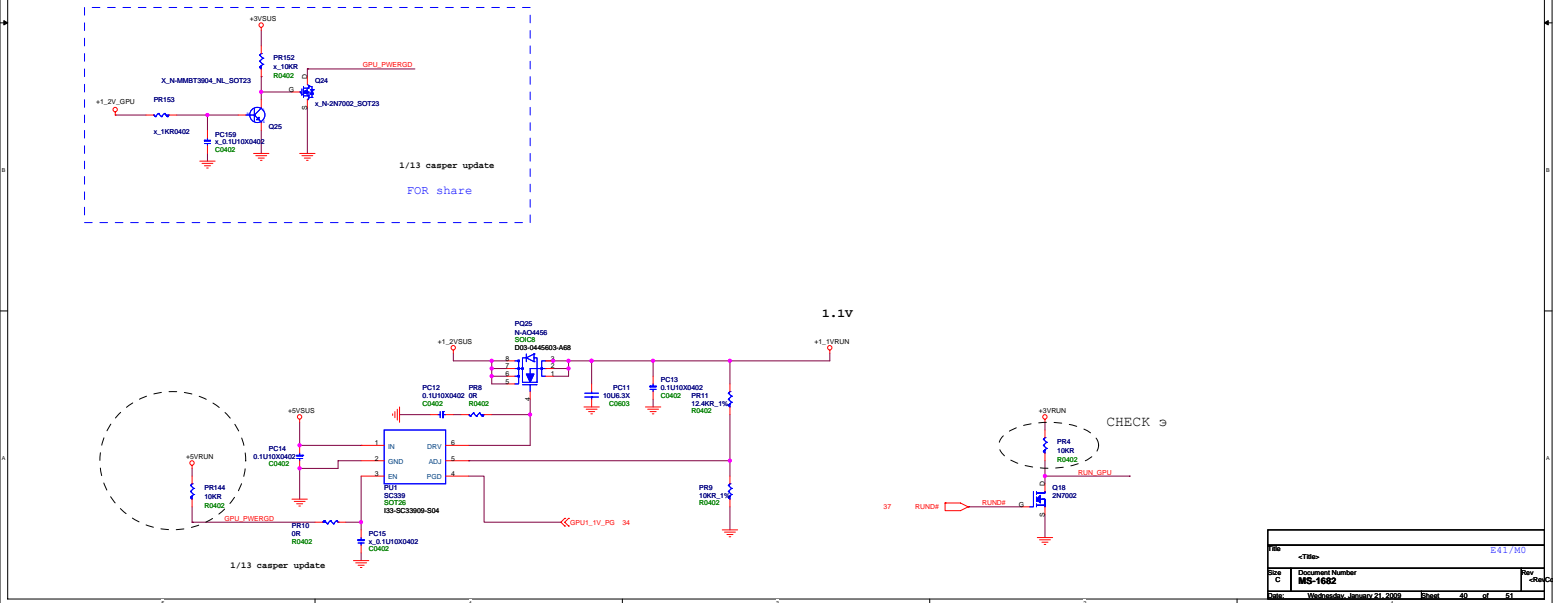


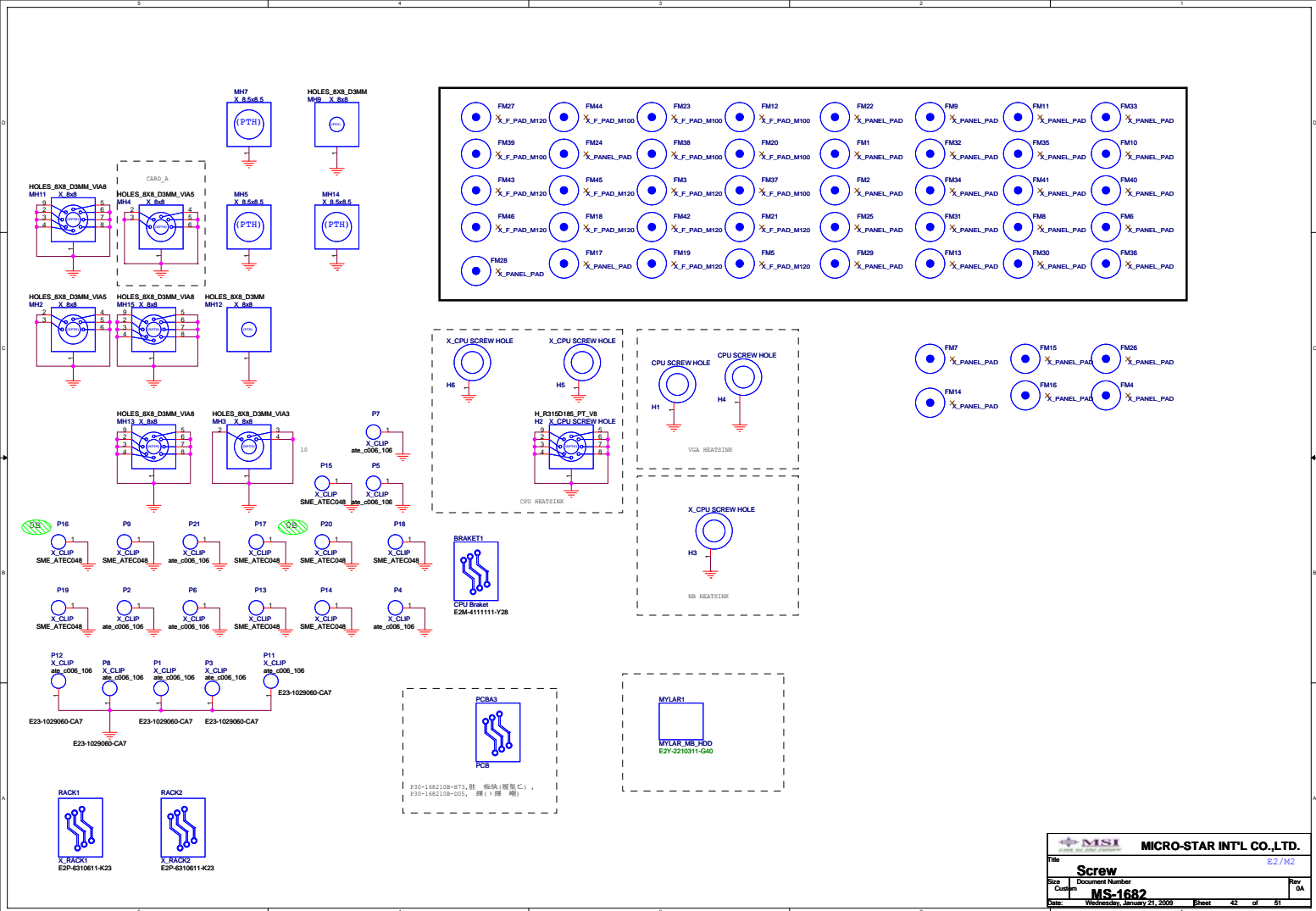


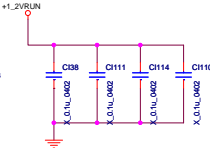
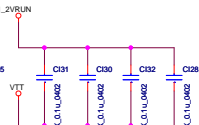
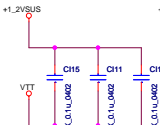
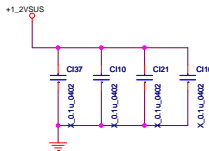
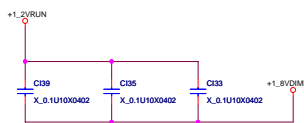
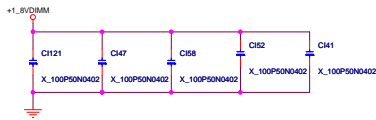
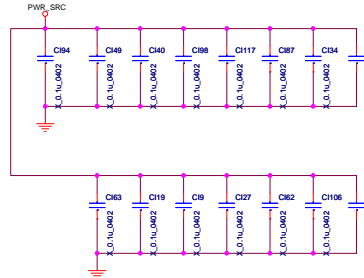
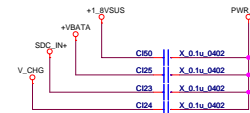
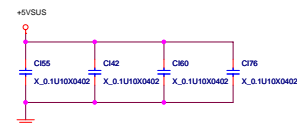
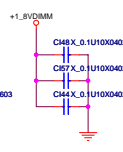
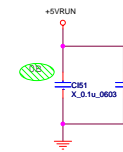
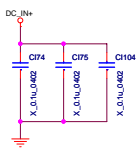
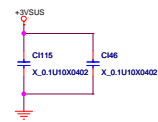
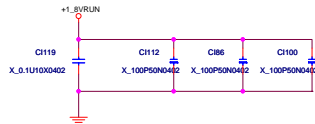
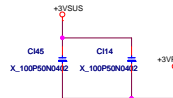
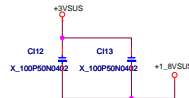
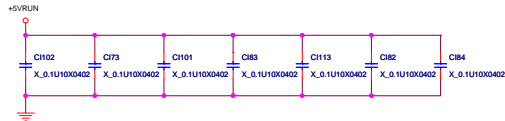
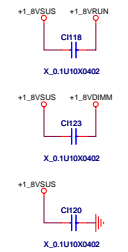
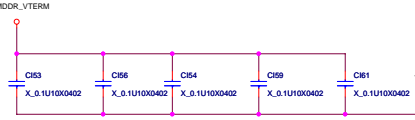
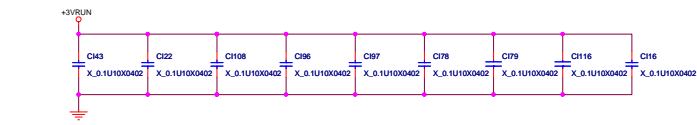
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Title: 1.8V / SMDDR VTERM / 1.5VRUN			
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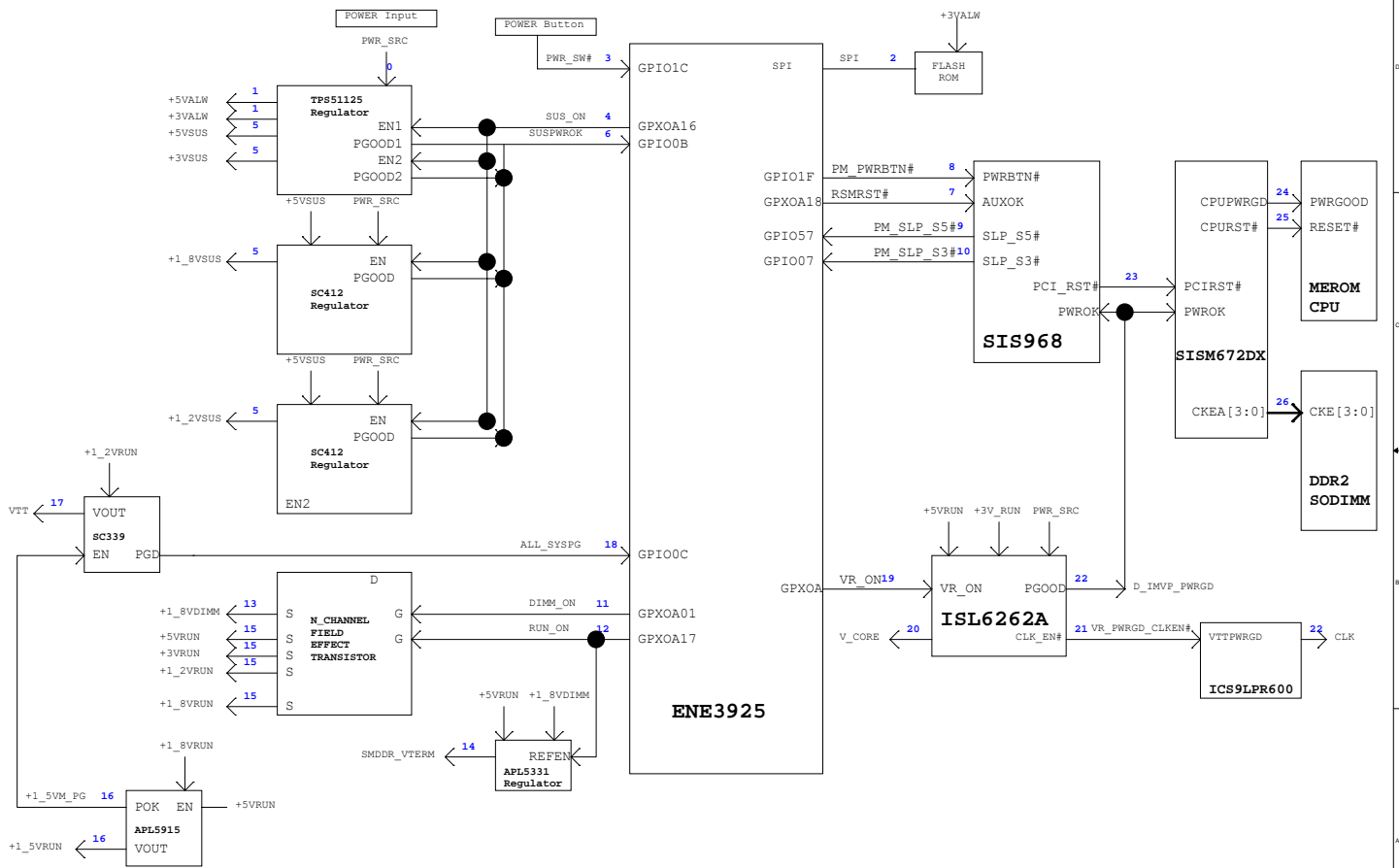


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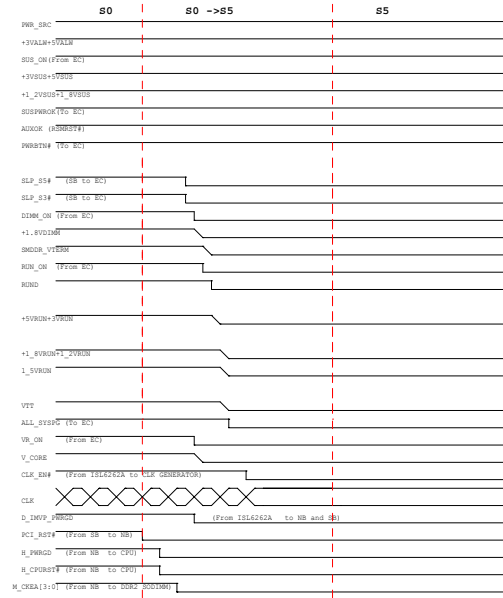




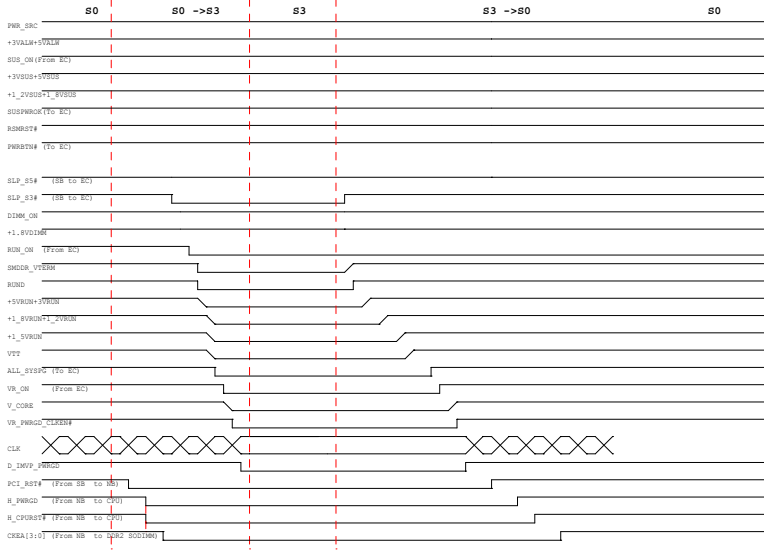


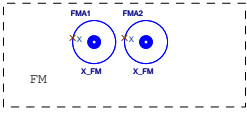
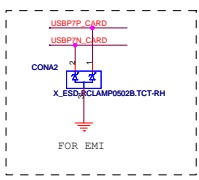
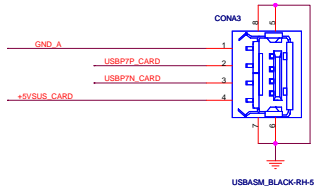
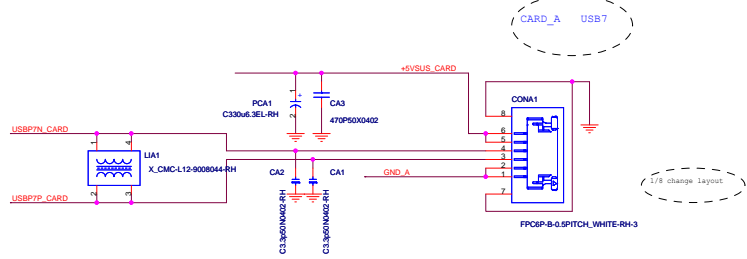
EC programming timing
SiSM672FX + 968 timing SPEC

EC programming timing
SiSM672FX + 968 timing SPEC

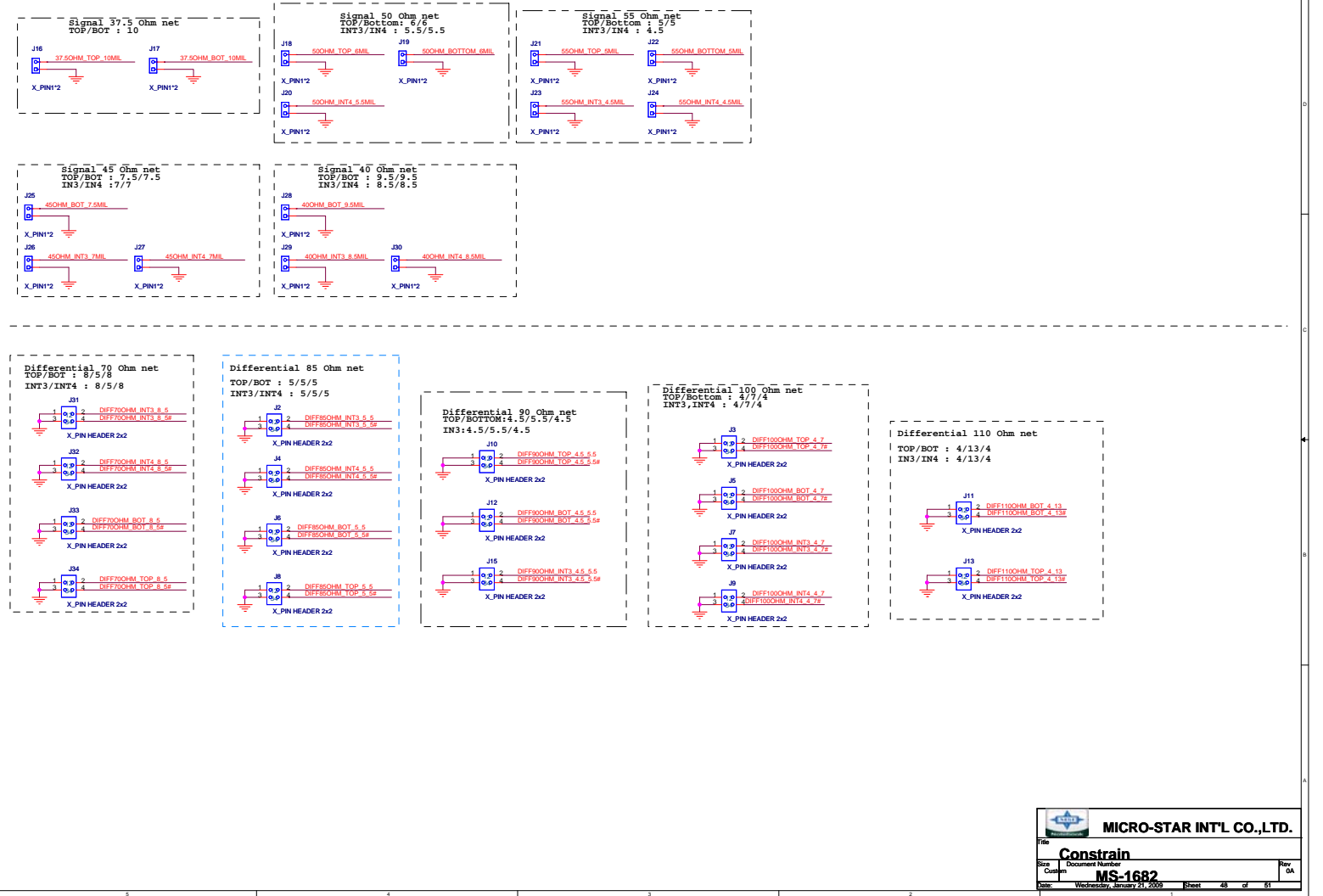


AC S0-S3-S0
EC programming timing
Si8M672FX + 968 timing SPEC





P30-1682A0B-H73, 胜 痴缺 (履集亡)
P30-1682A0B-D05, 緯 () 緯 喇),



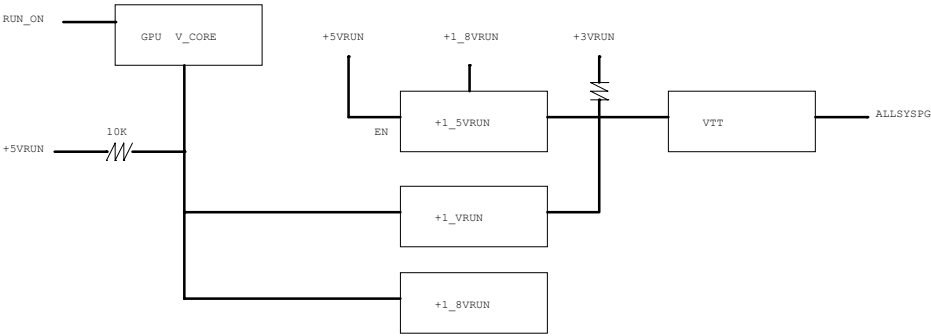
0A -- 0B Note

MS-1682

P03, C579 INSTALL by SA BUG ,R41 CHANGE F/P TO R0603
P04, C639,C623,C612,C640,C624 INSTALL X5R
P06, R322 INSTALL
P07, R177,R171 CHANGE 36R , R170,R176 CHANGE 40.2R ,JNC70,JNC75 CHANGE F/P TO NC_0603
P14, R124,R125,R301 CHANG JNC81,JNC82,JNC83 AND INSTALL , R67,R68 DEL ,ADD PR135,RN28,JNC80,R346 ,R346 CHANGE F/P TO R0603, U5 PIN 8 ,7 CHANGE NET NAME ,JNC29 &R85 CHANGE
P15, C50 INSTALL
P16, R52,R246 INSTALL ,R51,R242 DON'T INSTALL
P18, R225,R227,R13,R14 CHANGE 499R
P19, R223,R224,R12,R11 CHANGE 499R
P20, CHANGE U15 FOOTPRINT TO " SOT23_5_NPC30X " , VGA_DATA AND VGA_CLK AND "J38 : PIN 30 "CHANGE TO +3.3V_DELAY , R232,R233 ,C486,C487,C488 INSTALL
P21, RN14 PIN 2,4 SWAP PIN 6,8
P22, DEL SPI SKET1,JNC66,JNC67,JNC71,JNC72,CON4 , R318 INSTALL, R317 DON'T INSTALL ,JNC34 ,JNC33 CHANGE F/P TO NC_0603
P23, JNC65,JNC64,JNC59,JNC56,JNC55 INSTALL by SA BUG ,R41 CHANGE F/P TO R0603
P26, CN5 CHANGE CAD, CN6 CHANGE LAYOUT AND PIN 6 TO GND
P27, DEL D1,D2, R212 CHANGE TO +5VSUS
P28, R189 CHANGE 0 Ohm AND INSTALL , CHANGE CON5 PIN 29,20,27 NET NAME, DEL R187,R186 , U12 CHANGE 5159 "B07-0515904-R09 "
P29, Y1 CHANGE F/P, U23 NET CHANGE
P30, JGF81 DON'T INSTALL, USIM_PWR > 25 mils, DEL SW1,SW2,SW3,SW4,JNC1,2,3,4
P31, R112,D16 TO ALLSYSFG, R115,C212 NOT INSTALL, R108 INSTALL
P32, R290 CHANG TO 33K ,C622 CHANGE TO 4.7U,CON7 SWAP PIN 1 &PIN 2
P33, U20 CHANGE FOOTPRINT SIC8_SST_S2A , CN3 CHANGE NEW PN , DEL R346 TO RUN_PG, U3 PIN 113 CHANGE TO PIN 23 , U3 PIN 98 & PIN 130 SWAP,JNC8 OGANGE R38 , ADD R354 220HM , SW5,SW6 SWAP LAYOUT, YT1 MOVE
P34, JNC19 CHANGE R345 DON'T INSTALL ,J37 CHANGE FOOT PRINT
P36, PR12 360 CHANGE 620 (R11-0621T12-R01) (spre-charge current), PR16 9.31K CHANGE 28.7K(R11-2872T12-W08) (36-CELL charge current)
P37, PR107 CHANGE 10K ,INSTALL PC103
P38, ADD PQ36 TO DELAY +1 8VRUN, DEL PR135,PC159 , DON'T INSTALL PR114
P39, PU4 PIN4 TO ALLSYSFG ,PR77 CHANGE 0 Ohm, PC69 DON'T INSTALL ,PC72 10uF CHANGE 4.7uF(C11-4753014-W08) (3jitter)
P40, PR4 CHANGE TO 10K Ohm ,PR63 147 CHANGE 147K(R11-1473T12-Y01) ,ADD GPU_PWERGD NET WAY
P41, PR63 CHANGE TO 147K Ohm , ADD R353 DON'T INSTALL ,C613 INSTALL
P42 , H1:P30 , MH1:CHANGE TO 5020
P47 , CONA1 CHANGE LAYOUT

JNC21, JNC80 修改
ADD PR144 TO +5VRUN 3check
ADD PR145 TO +3VRUN 3check

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