Figure 10. Pinout Diagram (Top View—Left Side)

	26	25	24	23	22	21	20	19	18	17	16	15	14	
AF	SKTOCC#	Reserved	Reserved	BCLK1	BCLK0	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VSS	**AF**
AE	OPTIMIZED/COMPAT#	DBR#	VSS	VCCA	VSS	Reserved	VCC	VSS	VCC	VSS	VCC	VSS	VCC	**AE**
AD	ITP_CLK1	TESTHI12	TESTHI0	VSS	VSSA	VSS	VCCIOPLL	VCC	VSS	VCC	VSS	VCC	VSS	**AD**
AC	ITP_CLK0	VSS	TESTHI4	TESTHI5	VSS	TESTHI2	TESTHI3	VSS	VCC	VSS	VCC	VSS	VCC	**AC**
AB	SLP#	RESET#	VSS	PWR GOOD	TESTHI7	VSS	VSS	VCC	VSS	VCC	VSS	VCC	VSS	**AB**
AA	VSS	D61#	D63#	VSS	D62#	GTLREF	TESTHI6	VSS	VCC	VSS	VCC	VSS	VCC	**AA**
Y	D56#	VSS	D59#	D58#	VSS	D60#								**Y**
W	D55#	D57#	VSS	DSTBP3#	DSTBN3#	VSS								**W**
V	VSS	D51#	D54#	VSS	D53#	DBI3#								**V**
U	D48#	VSS	D49#	D50#	VSS	D52#								**U**
T	D44#	D45#	VSS	D47#	D46#	VSS								**T**
R	VSS	D42#	D43#	VSS	DSTBN2#	D40#								**R**
P	DBI2#	VSS	D41#	DSTBP2#	VSS	D34#								**P**
N	D38#	D39#	VSS	D36#	D33#	VSS								**N**
M	D37#	VSS	D35#	D32#	VSS	D27#								**M**
L	VSS	DP3#	COMP0	VSS	D28#	D24#								**L**
K	DP2#	DP1#	VSS	D30#	DSTBN1#	VSS								**K**
J	DP0#	VSS	D29#	DSTBP1#	VSS	D14#								**J**
H	VSS	D31#	D26#	VSS	D16#	D11#								**H**
G	D25#	DBI1#	VSS	D18#	D10#	VSS								**G**
F	D22#	VSS	D20#	D19#	VSS	DSTBP0#	GTLREF	VCC	VSS	VCC	VSS	VCC	VSS	**F**
E	VSS	D21#	D17#	VSS	DSTBN0#	DBI0#	VCC	VSS	VCC	VSS	VCC	VSS	VCC	**E**
D	D23#	D15#	VSS	D13#	D5#	VSS	VSS	VCC	VSS	VCC	VSS	VCC	VSS	**D**
C	D12#	VSS	D8#	D7#	VSS	D4#	VCC	VSS	VCC	VSS	VCC	VSS	VCC	**C**
B	VSS	D9#	D6#	VSS	D1#	D0#	VSS	VCC	VSS	VCC	VSS	VCC	VSS	**B**
A	VSS	D3#	VSS	D2#	Reserved	VSS	VCC	VSS	VCC	VSS	VCC	VSS	VCC	**A**
	26	25	24	23	22	21	20	19	18	17	16	15	14	

Figure 11. Pinout Diagram (Top View—Right Side)

	13	12	11	10	9	8	7	6	5	4	3	2	1	
AF	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VCCVID	VCCVIDLB	VCC	VSS	AF
AE	VSS	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VID0	VID1	VID2	VID3	VID4	AE
AD	VCC	VSS	VCC	VSS	VCC	VSS	VCC	BSEL0	BSEL1	VSS	VID5	VIDPWRGD	BOOT SELECT	AD
AC	VSS	VCC	VSS	VCC	VSS	VCC	VSS	BPM0#	VSS	BPM2#	IERR#	VSS	AP0#	AC
AB	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VSS	BPM1#	BPM5#	VSS	RSP#	A35#	AB
AA	VSS	VCC	VSS	VCC	VSS	VCC	VSS	GTLREF	BPM4#	VSS	BINIT#	TESTHI1	VSS	AA
Y								BPM3#	VSS	STPCLK#	TESTHI10	VSS	A34#	Y
W								VSS	INIT#	TESTHI9	VSS	A33#	A29#	W
V								MCERR#	AP1#	VSS	A32#	A27#	VSS	V
U								TESTHI8	VSS	A31#	A25#	VSS	A23#	U
T								VSS	A30#	A26#	VSS	A22#	A17#	T
R								A28#	ADSTB1#	VSS	A21#	A18#	VSS	R
P								A24#	VSS	A20#	A19#	VSS	COMP1	P
N								VSS	A16#	A15#	VSS	A14#	A12#	N
M								A8#	VSS	A11#	A10#	VSS	A13#	M
L								A5#	ADSTB0#	VSS	A7#	A9#	VSS	L
K								VSS	REQ1#	A4#	VSS	A3#	A6#	K
J								TRDY#	VSS	REQ2#	REQ3#	VSS	REQ0#	J
H								BR0#	DBSY#	VSS	REQ4#	DRDY#	VSS	H
G								VSS	RS1#	LOCK#	VSS	BNR#	ADS#	G
F	VCC	VSS	VCC	VSS	VCC	VSS	TMS	GTLREF	VSS	RS2#	HIT#	VSS	RS0#	F
E	VSS	VCC	VSS	VCC	VSS	VCC	VSS	TRST#	LINT1	VSS	HITM#	DEFER#	VSS	E
D	VCC	VSS	VCC	VSS	VCC	VSS	VCC	VSS	TDO	TCK	VSS	BPRI#	LINT0	D
C	VSS	VCC	VSS	VCC	VSS	VCC	VSS	A20M#	VSS	THERMDC	PROCHOT#	VSS	TDI	C
B	VCC	VSS	VCC	VSS	VCC	VSS	VCC	FERR#/PBE#	SMI#	VSS	THERMDA	IGNNE#		B
A	VSS	VCC	VSS	VCC	VSS	VCC	Reserved	TESTHI11	VCC_SENSE	VSS_SENSE	VSS	THERMTRIP#		A
	13	12	11	10	9	8	7	6	5	4	3	2	1	

Table 23. Alphabetical Pin Assignment

Pin Name	Pin #	Signal Buffer Type	Direction
A3#	K2	Source Synch	Input/Output
A4#	K4	Source Synch	Input/Output
A5#	L6	Source Synch	Input/Output
A6#	K1	Source Synch	Input/Output
A7#	L3	Source Synch	Input/Output
A8#	M6	Source Synch	Input/Output
A9#	L2	Source Synch	Input/Output
A10#	M3	Source Synch	Input/Output
A11#	M4	Source Synch	Input/Output
A12#	N1	Source Synch	Input/Output
A13#	M1	Source Synch	Input/Output
A14#	N2	Source Synch	Input/Output
A15#	N4	Source Synch	Input/Output
A16#	N5	Source Synch	Input/Output
A17#	T1	Source Synch	Input/Output
A18#	R2	Source Synch	Input/Output
A19#	P3	Source Synch	Input/Output
A20#	P4	Source Synch	Input/Output
A21#	R3	Source Synch	Input/Output
A22#	T2	Source Synch	Input/Output
A23#	U1	Source Synch	Input/Output
A24#	P6	Source Synch	Input/Output
A25#	U3	Source Synch	Input/Output
A26#	T4	Source Synch	Input/Output
A27#	V2	Source Synch	Input/Output
A28#	R6	Source Synch	Input/Output
A29#	W1	Source Synch	Input/Output
A30#	T5	Source Synch	Input/Output
A31#	U4	Source Synch	Input/Output
A32#	V3	Source Synch	Input/Output
A33#	W2	Source Synch	Input/Output
A34#	Y1	Source Synch	Input/Output
A35#	AB1	Source Synch	Input/Output
A20M#	C6	Asynch GTL+	Input
ADS#	G1	Common Clock	Input/Output
ADSTB0#	L5	Source Synch	Input/Output
ADSTB1#	R5	Source Synch	Input/Output
AP0#	AC1	Common Clock	Input/Output
AP1#	V5	Common Clock	Input/Output
BCLK0	AF22	Bus Clock	Input
BCLK1	AF23	Bus Clock	Input

Table 23. Alphabetical Pin Assignment

Pin Name	Pin #	Signal Buffer Type	Direction
BINIT#	AA3	Common Clock	Input/Output
BNR#	G2	Common Clock	Input/Output
BOOTSELECT	AD1	Power/Other	Input
BPM0#	AC6	Common Clock	Input/Output
BPM1#	AB5	Common Clock	Input/Output
BPM2#	AC4	Common Clock	Input/Output
BPM3#	Y6	Common Clock	Input/Output
BPM4#	AA5	Common Clock	Input/Output
BPM5#	AB4	Common Clock	Input/Output
BPRI#	D2	Common Clock	Input
BR0#	H6	Common Clock	Input/Output
BSEL0	AD6	Power/Other	Output
BSEL1	AD5	Power/Other	Output
COMP0	L24	Power/Other	Input
COMP1	P1	Power/Other	Input
D0#	B21	Source Synch	Input/Output
D1#	B22	Source Synch	Input/Output
D2#	A23	Source Synch	Input/Output
D3#	A25	Source Synch	Input/Output
D4#	C21	Source Synch	Input/Output
D5#	D22	Source Synch	Input/Output
D6#	B24	Source Synch	Input/Output
D7#	C23	Source Synch	Input/Output
D8#	C24	Source Synch	Input/Output
D9#	B25	Source Synch	Input/Output
D10#	G22	Source Synch	Input/Output
D11#	H21	Source Synch	Input/Output
D12#	C26	Source Synch	Input/Output
D13#	D23	Source Synch	Input/Output
D14#	J21	Source Synch	Input/Output
D15#	D25	Source Synch	Input/Output
D16#	H22	Source Synch	Input/Output
D17#	E24	Source Synch	Input/Output
D18#	G23	Source Synch	Input/Output
D19#	F23	Source Synch	Input/Output
D20#	F24	Source Synch	Input/Output
D21#	E25	Source Synch	Input/Output
D22#	F26	Source Synch	Input/Output
D23#	D26	Source Synch	Input/Output
D24#	L21	Source Synch	Input/Output
D25#	G26	Source Synch	Input/Output

Table 23. Alphabetical Pin Assignment

Pin Name	Pin #	Signal Buffer Type	Direction
D26#	H24	Source Synch	Input/Output
D27#	M21	Source Synch	Input/Output
D28#	L22	Source Synch	Input/Output
D29#	J24	Source Synch	Input/Output
D30#	K23	Source Synch	Input/Output
D31#	H25	Source Synch	Input/Output
D32#	M23	Source Synch	Input/Output
D33#	N22	Source Synch	Input/Output
D34#	P21	Source Synch	Input/Output
D35#	M24	Source Synch	Input/Output
D36#	N23	Source Synch	Input/Output
D37#	M26	Source Synch	Input/Output
D38#	N26	Source Synch	Input/Output
D39#	N25	Source Synch	Input/Output
D40#	R21	Source Synch	Input/Output
D41#	P24	Source Synch	Input/Output
D42#	R25	Source Synch	Input/Output
D43#	R24	Source Synch	Input/Output
D44#	T26	Source Synch	Input/Output
D45#	T25	Source Synch	Input/Output
D46#	T22	Source Synch	Input/Output
D47#	T23	Source Synch	Input/Output
D48#	U26	Source Synch	Input/Output
D49#	U24	Source Synch	Input/Output
D50#	U23	Source Synch	Input/Output
D51#	V25	Source Synch	Input/Output
D52#	U21	Source Synch	Input/Output
D53#	V22	Source Synch	Input/Output
D54#	V24	Source Synch	Input/Output
D55#	W26	Source Synch	Input/Output
D56#	Y26	Source Synch	Input/Output
D57#	W25	Source Synch	Input/Output
D58#	Y23	Source Synch	Input/Output
D59#	Y24	Source Synch	Input/Output
D60#	Y21	Source Synch	Input/Output
D61#	AA25	Source Synch	Input/Output
D62#	AA22	Source Synch	Input/Output
D63#	AA24	Source Synch	Input/Output
DBI0#	E21	Source Synch	Input/Output
DBI1#	G25	Source Synch	Input/Output
DBI2#	P26	Source Synch	Input/Output

Pin Name	Pin #	Signal Buffer Type	Direction
DBI3#	V21	Source Synch	Input/Output
DBR#	AE25	Power/Other	Output
DBSY#	H5	Common Clock	Input/Output
DEFER#	E2	Common Clock	Input
DP0#	J26	Common Clock	Input/Output
DP1#	K25	Common Clock	Input/Output
DP2#	K26	Common Clock	Input/Output
DP3#	L25	Common Clock	Input/Output
DRDY#	H2	Common Clock	Input/Output
DSTBN0#	E22	Source Synch	Input/Output
DSTBN1#	K22	Source Synch	Input/Output
DSTBN2#	R22	Source Synch	Input/Output
DSTBN3#	W22	Source Synch	Input/Output
DSTBP0#	F21	Source Synch	Input/Output
DSTBP1#	J23	Source Synch	Input/Output
DSTBP2#	P23	Source Synch	Input/Output
DSTBP3#	W23	Source Synch	Input/Output
FERR#/PBE#	B6	Asynch AGL+	Output
GTLREF	AA21	Power/Other	Input
GTLREF	AA6	Power/Other	Input
GTLREF	F20	Power/Other	Input
GTLREF	F6	Power/Other	Input
HIT#	F3	Common Clock	Input/Output
HITM#	E3	Common Clock	Input/Output
IERR#	AC3	Asynch GTL+	Output
IGNNE#	B2	Asynch GTL+	Input
INIT#	W5	Asynch GTL+	Input
ITP_CLK0	AC26	TAP	Input
ITP_CLK1	AD26	TAP	Input
LINT0	D1	Asynch GTL+	Input
LINT1	E5	Asynch GTL+	Input
LOCK#	G4	Common Clock	Input/Output
MCERR#	V6	Common Clock	Input/Output
OPTIMIZED/ COMPAT#	AE26	Power/Other	Input
PROCHOT#	C3	Asynch GTL+	Input/Output
PWRGOOD	AB23	Power/Other	Input
REQ0#	J1	Source Synch	Input/Output
REQ1#	K5	Source Synch	Input/Output
REQ2#	J4	Source Synch	Input/Output
REQ3#	J3	Source Synch	Input/Output
REQ4#	H3	Source Synch	Input/Output

Table 23. Alphabetical Pin Assignment

Pin Name	Pin #	Signal Buffer Type	Direction
RESERVED	A22		
RESERVED	A7		
RESERVED	AE21		
RESERVED	AF24		
RESERVED	AF25		
RESET#	AB25	Common Clock	Input
RS0#	F1	Common Clock	Input
RS1#	G5	Common Clock	Input
RS2#	F4	Common Clock	Input
RSP#	AB2	Common Clock	Input
SKTOCC#	AF26	Power/Other	Output
SLP#	AB26	Asynch GTL+	Input
SMI#	B5	Asynch GTL+	Input
STPCLK#	Y4	Asynch GTL+	Input
TCK	D4	TAP	Input
TDI	C1	TAP	Input
TDO	D5	TAP	Output
TESTHI0	AD24	Power/Other	Input
TESTHI1	AA2	Power/Other	Input
TESTHI2	AC21	Power/Other	Input
TESTHI3	AC20	Power/Other	Input
TESTHI4	AC24	Power/Other	Input
TESTHI5	AC23	Power/Other	Input
TESTHI6	AA20	Power/Other	Input
TESTHI7	AB22	Power/Other	Input
TESTHI8	U6	Power/Other	Input
TESTHI9	W4	Power/Other	Input
TESTHI10	Y3	Power/Other	Input
TESTHI11	A6	Power/Other	Input
TESTHI12	AD25	Power/Other	Input
THERMDA	B3	Power/Other	
THERMDC	C4	Power/Other	
THERMTRIP#	A2	Asynch GTL+	Output
TMS	F7	TAP	Input
TRDY#	J6	Common Clock	Input
TRST#	E6	TAP	Input
VCC	A10	Power/Other	
VCC	A12	Power/Other	
VCC	A14	Power/Other	
VCC	A16	Power/Other	
VCC	A18	Power/Other	

Table 23. Alphabetical Pin Assignment

Pin Name	Pin #	Signal Buffer Type	Direction
VCC	A20	Power/Other	
VCC	A8	Power/Other	
VCC	AA10	Power/Other	
VCC	AA12	Power/Other	
VCC	AA14	Power/Other	
VCC	AA16	Power/Other	
VCC	AA18	Power/Other	
VCC	AA8	Power/Other	
VCC	AB11	Power/Other	
VCC	AB13	Power/Other	
VCC	AB15	Power/Other	
VCC	AB17	Power/Other	
VCC	AB19	Power/Other	
VCC	AB7	Power/Other	
VCC	AB9	Power/Other	
VCC	AC10	Power/Other	
VCC	AC12	Power/Other	
VCC	AC14	Power/Other	
VCC	AC16	Power/Other	
VCC	AC18	Power/Other	
VCC	AC8	Power/Other	
VCC	AD11	Power/Other	
VCC	AD13	Power/Other	
VCC	AD15	Power/Other	
VCC	AD17	Power/Other	
VCC	AD19	Power/Other	
VCC	AD7	Power/Other	
VCC	AD9	Power/Other	
VCC	AE10	Power/Other	
VCC	AE12	Power/Other	
VCC	AE14	Power/Other	
VCC	AE16	Power/Other	
VCC	AE18	Power/Other	
VCC	AE20	Power/Other	
VCC	AE6	Power/Other	
VCC	AE8	Power/Other	
VCC	AF11	Power/Other	
VCC	AF13	Power/Other	
VCC	AF15	Power/Other	
VCC	AF17	Power/Other	
VCC	AF19	Power/Other	

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Table 23. Alphabetical Pin Assignment

Pin Name	Pin #	Signal Buffer Type	Direction
VCC	AF2	Power/Other	
VCC	AF21	Power/Other	
VCC	AF5	Power/Other	
VCC	AF7	Power/Other	
VCC	AF9	Power/Other	
VCC	B11	Power/Other	
VCC	B13	Power/Other	
VCC	B15	Power/Other	
VCC	B17	Power/Other	
VCC	B19	Power/Other	
VCC	B7	Power/Other	
VCC	B9	Power/Other	
VCC	C10	Power/Other	
VCC	C12	Power/Other	
VCC	C14	Power/Other	
VCC	C16	Power/Other	
VCC	C18	Power/Other	
VCC	C20	Power/Other	
VCC	C8	Power/Other	
VCC	D11	Power/Other	
VCC	D13	Power/Other	
VCC	D15	Power/Other	
VCC	D17	Power/Other	
VCC	D19	Power/Other	
VCC	D7	Power/Other	
VCC	D9	Power/Other	
VCC	E10	Power/Other	
VCC	E12	Power/Other	
VCC	E14	Power/Other	
VCC	E16	Power/Other	
VCC	E18	Power/Other	
VCC	E20	Power/Other	
VCC	E8	Power/Other	
VCC	F11	Power/Other	
VCC	F13	Power/Other	
VCC	F15	Power/Other	
VCC	F17	Power/Other	
VCC	F19	Power/Other	
VCC	F9	Power/Other	
VCCA	AE23	Power/Other	
VCCIOPLL	AD20	Power/Other	

Table 23. Alphabetical Pin Assignment

Pin Name	Pin #	Signal Buffer Type	Direction
VCC_SENSE	A5	Power/Other	Output
VCCVID	AF4	Power/Other	Input
VCCVIDLB	AF3	Power/Other	Input
VID0	AE5	Power/Other	Output
VID1	AE4	Power/Other	Output
VID2	AE3	Power/Other	Output
VID3	AE2	Power/Other	Output
VID4	AE1	Power/Other	Output
VID5	AD3	Power/Other	Output
VIDPWRGD	AD2	Power/Other	Input
VSS	A11	Power/Other	
VSS	A13	Power/Other	
VSS	A15	Power/Other	
VSS	A17	Power/Other	
VSS	A19	Power/Other	
VSS	A21	Power/Other	
VSS	A24	Power/Other	
VSS	A26	Power/Other	
VSS	A3	Power/Other	
VSS	A9	Power/Other	
VSS	AA1	Power/Other	
VSS	AA11	Power/Other	
VSS	AA13	Power/Other	
VSS	AA15	Power/Other	
VSS	AA17	Power/Other	
VSS	AA19	Power/Other	
VSS	AA23	Power/Other	
VSS	AA26	Power/Other	
VSS	AA4	Power/Other	
VSS	AA7	Power/Other	
VSS	AA9	Power/Other	
VSS	AB10	Power/Other	
VSS	AB12	Power/Other	
VSS	AB14	Power/Other	
VSS	AB16	Power/Other	
VSS	AB18	Power/Other	
VSS	AB20	Power/Other	
VSS	AB21	Power/Other	
VSS	AB24	Power/Other	
VSS	AB3	Power/Other	
VSS	AB6	Power/Other	

Table 23. Alphabetical Pin Assignment

Pin Name	Pin #	Signal Buffer Type	Direction
VSS	AB8	Power/Other	
VSS	AC11	Power/Other	
VSS	AC13	Power/Other	
VSS	AC15	Power/Other	
VSS	AC17	Power/Other	
VSS	AC19	Power/Other	
VSS	AC2	Power/Other	
VSS	AC22	Power/Other	
VSS	AC25	Power/Other	
VSS	AC5	Power/Other	
VSS	AC7	Power/Other	
VSS	AC9	Power/Other	
VSS	AD10	Power/Other	
VSS	AD12	Power/Other	
VSS	AD14	Power/Other	
VSS	AD16	Power/Other	
VSS	AD18	Power/Other	
VSS	AD21	Power/Other	
VSS	AD23	Power/Other	
VSS	AD4	Power/Other	
VSS	AD8	Power/Other	
VSS	AE11	Power/Other	
VSS	AE13	Power/Other	
VSS	AE15	Power/Other	
VSS	AE17	Power/Other	
VSS	AE19	Power/Other	
VSS	AE22	Power/Other	
VSS	AE24	Power/Other	
VSS	AE7	Power/Other	
VSS	AE9	Power/Other	
VSS	AF1	Power/Other	
VSS	AF10	Power/Other	
VSS	AF12	Power/Other	
VSS	AF14	Power/Other	
VSS	AF16	Power/Other	
VSS	AF18	Power/Other	
VSS	AF20	Power/Other	
VSS	AF6	Power/Other	
VSS	AF8	Power/Other	
VSS	B10	Power/Other	
VSS	B12	Power/Other	

Table 23. Alphabetical Pin Assignment

Pin Name	Pin #	Signal Buffer Type	Direction
VSS	B14	Power/Other	
VSS	B16	Power/Other	
VSS	B18	Power/Other	
VSS	B20	Power/Other	
VSS	B23	Power/Other	
VSS	B26	Power/Other	
VSS	B4	Power/Other	
VSS	B8	Power/Other	
VSS	C11	Power/Other	
VSS	C13	Power/Other	
VSS	C15	Power/Other	
VSS	C17	Power/Other	
VSS	C19	Power/Other	
VSS	C2	Power/Other	
VSS	C22	Power/Other	
VSS	C25	Power/Other	
VSS	C5	Power/Other	
VSS	C7	Power/Other	
VSS	C9	Power/Other	
VSS	D10	Power/Other	
VSS	D12	Power/Other	
VSS	D14	Power/Other	
VSS	D16	Power/Other	
VSS	D18	Power/Other	
VSS	D20	Power/Other	
VSS	D21	Power/Other	
VSS	D24	Power/Other	
VSS	D3	Power/Other	
VSS	D6	Power/Other	
VSS	D8	Power/Other	
VSS	E1	Power/Other	
VSS	E11	Power/Other	
VSS	E13	Power/Other	
VSS	E15	Power/Other	
VSS	E17	Power/Other	
VSS	E19	Power/Other	
VSS	E23	Power/Other	
VSS	E26	Power/Other	
VSS	E4	Power/Other	
VSS	E7	Power/Other	
VSS	E9	Power/Other	

Table 23. Alphabetical Pin Assignment

Pin Name	Pin #	Signal Buffer Type	Direction
VSS	F10	Power/Other	
VSS	F12	Power/Other	
VSS	F14	Power/Other	
VSS	F16	Power/Other	
VSS	F18	Power/Other	
VSS	F2	Power/Other	
VSS	F22	Power/Other	
VSS	F25	Power/Other	
VSS	F5	Power/Other	
VSS	F8	Power/Other	
VSS	G21	Power/Other	
VSS	G24	Power/Other	
VSS	G3	Power/Other	
VSS	G6	Power/Other	
VSS	H1	Power/Other	
VSS	H23	Power/Other	
VSS	H26	Power/Other	
VSS	H4	Power/Other	
VSS	J2	Power/Other	
VSS	J22	Power/Other	
VSS	J25	Power/Other	
VSS	J5	Power/Other	
VSS	K21	Power/Other	
VSS	K24	Power/Other	
VSS	K3	Power/Other	
VSS	K6	Power/Other	
VSS	L1	Power/Other	
VSS	L23	Power/Other	
VSS	L26	Power/Other	
VSS	L4	Power/Other	
VSS	M2	Power/Other	
VSS	M22	Power/Other	
VSS	M25	Power/Other	
VSS	M5	Power/Other	

Table 23. Alphabetical Pin Assignment

Pin Name	Pin #	Signal Buffer Type	Direction
VSS	N21	Power/Other	
VSS	N24	Power/Other	
VSS	N3	Power/Other	
VSS	N6	Power/Other	
VSS	P2	Power/Other	
VSS	P22	Power/Other	
VSS	P25	Power/Other	
VSS	P5	Power/Other	
VSS	R1	Power/Other	
VSS	R23	Power/Other	
VSS	R26	Power/Other	
VSS	R4	Power/Other	
VSS	T21	Power/Other	
VSS	T24	Power/Other	
VSS	T3	Power/Other	
VSS	T6	Power/Other	
VSS	U2	Power/Other	
VSS	U22	Power/Other	
VSS	U25	Power/Other	
VSS	U5	Power/Other	
VSS	V1	Power/Other	
VSS	V23	Power/Other	
VSS	V26	Power/Other	
VSS	V4	Power/Other	
VSS	W21	Power/Other	
VSS	W24	Power/Other	
VSS	W3	Power/Other	
VSS	W6	Power/Other	
VSS	Y2	Power/Other	
VSS	Y22	Power/Other	
VSS	Y25	Power/Other	
VSS	Y5	Power/Other	
VSSA	AD22	Power/Other	
VSS_SENSE	A4	Power/Other	Output

Table 24. Numerical Pin Assignment

Pin #	Pin Name	Signal Buffer Type	Direction
A2	THERMTRIP#	Asynch GTL+	Output
A3	VSS	Power/Other	
A4	VSS_SENSE	Power/Other	Output
A5	VCC_SENSE	Power/Other	Output
A6	TESTHI11	Power/Other	Input
A7	RESERVED		
A8	VCC	Power/Other	
A9	VSS	Power/Other	
A10	VCC	Power/Other	
A11	VSS	Power/Other	
A12	VCC	Power/Other	
A13	VSS	Power/Other	
A14	VCC	Power/Other	
A15	VSS	Power/Other	
A16	VCC	Power/Other	
A17	VSS	Power/Other	
A18	VCC	Power/Other	
A19	VSS	Power/Other	
A20	VCC	Power/Other	
A21	VSS	Power/Other	
A22	RESERVED		
A23	D2#	Source Synch	Input/Output
A24	VSS	Power/Other	
A25	D3#	Source Synch	Input/Output
A26	VSS	Power/Other	
B2	IGNNE#	Asynch GTL+	Input
B3	THERMDA	Power/Other	
B4	VSS	Power/Other	
B5	SMI#	Asynch GTL+	Input
B6	FERR#/PBE#	Asynch AGL+	Output
B7	VCC	Power/Other	
B8	VSS	Power/Other	
B9	VCC	Power/Other	
B10	VSS	Power/Other	
B11	VCC	Power/Other	
B12	VSS	Power/Other	
B13	VCC	Power/Other	
B14	VSS	Power/Other	
B15	VCC	Power/Other	
B16	VSS	Power/Other	
B17	VCC	Power/Other	

Table 24. Numerical Pin Assignment

Pin #	Pin Name	Signal Buffer Type	Direction
B18	VSS	Power/Other	
B19	VCC	Power/Other	
B20	VSS	Power/Other	
B21	D0#	Source Synch	Input/Output
B22	D1#	Source Synch	Input/Output
B23	VSS	Power/Other	
B24	D6#	Source Synch	Input/Output
B25	D9#	Source Synch	Input/Output
B26	VSS	Power/Other	
C1	TDI	TAP	Input
C2	VSS	Power/Other	
C3	PROCHOT#	Asynch GTL+	Input/Output
C4	THERMDC	Power/Other	
C5	VSS	Power/Other	
C6	A20M#	Asynch GTL+	Input
C7	VSS	Power/Other	
C8	VCC	Power/Other	
C9	VSS	Power/Other	
C10	VCC	Power/Other	
C11	VSS	Power/Other	
C12	VCC	Power/Other	
C13	VSS	Power/Other	
C14	VCC	Power/Other	
C15	VSS	Power/Other	
C16	VCC	Power/Other	
C17	VSS	Power/Other	
C18	VCC	Power/Other	
C19	VSS	Power/Other	
C20	VCC	Power/Other	
C21	D4#	Source Synch	Input/Output
C22	VSS	Power/Other	
C23	D7#	Source Synch	Input/Output
C24	D8#	Source Synch	Input/Output
C25	VSS	Power/Other	
C26	D12#	Source Synch	Input/Output
D1	LINT0	Asynch GTL+	Input
D2	BPRI#	Common Clock	Input
D3	VSS	Power/Other	
D4	TCK	TAP	Input
D5	TDO	TAP	Output
D6	VSS	Power/Other	

Table 24. Numerical Pin Assignment

Pin #	Pin Name	Signal Buffer Type	Direction
D7	VCC	Power/Other	
D8	VSS	Power/Other	
D9	VCC	Power/Other	
D10	VSS	Power/Other	
D11	VCC	Power/Other	
D12	VSS	Power/Other	
D13	VCC	Power/Other	
D14	VSS	Power/Other	
D15	VCC	Power/Other	
D16	VSS	Power/Other	
D17	VCC	Power/Other	
D18	VSS	Power/Other	
D19	VCC	Power/Other	
D20	VSS	Power/Other	
D21	VSS	Power/Other	
D22	D5#	Source Synch	Input/Output
D23	D13#	Source Synch	Input/Output
D24	VSS	Power/Other	
D25	D15#	Source Synch	Input/Output
D26	D23#	Source Synch	Input/Output
E1	VSS	Power/Other	
E2	DEFER#	Common Clock	Input
E3	HITM#	Common Clock	Input/Output
E4	VSS	Power/Other	
E5	LINT1	Asynch GTL+	Input
E6	TRST#	TAP	Input
E7	VSS	Power/Other	
E8	VCC	Power/Other	
E9	VSS	Power/Other	
E10	VCC	Power/Other	
E11	VSS	Power/Other	
E12	VCC	Power/Other	
E13	VSS	Power/Other	
E14	VCC	Power/Other	
E15	VSS	Power/Other	
E16	VCC	Power/Other	
E17	VSS	Power/Other	
E18	VCC	Power/Other	
E19	VSS	Power/Other	
E20	VCC	Power/Other	
E21	DBI0#	Source Synch	Input/Output

Pin #	Pin Name	Signal Buffer Type	Direction
E22	DSTBN0#	Source Synch	Input/Output
E23	VSS	Power/Other	
E24	D17#	Source Synch	Input/Output
E25	D21#	Source Synch	Input/Output
E26	VSS	Power/Other	
F1	RS0#	Common Clock	Input
F2	VSS	Power/Other	
F3	HIT#	Common Clock	Input/Output
F4	RS2#	Common Clock	Input
F5	VSS	Power/Other	
F6	GTLREF	Power/Other	Input
F7	TMS	TAP	Input
F8	VSS	Power/Other	
F9	VCC	Power/Other	
F10	VSS	Power/Other	
F11	VCC	Power/Other	
F12	VSS	Power/Other	
F13	VCC	Power/Other	
F14	VSS	Power/Other	
F15	VCC	Power/Other	
F16	VSS	Power/Other	
F17	VCC	Power/Other	
F18	VSS	Power/Other	
F19	VCC	Power/Other	
F20	GTLREF	Power/Other	Input
F21	DSTBP0#	Source Synch	Input/Output
F22	VSS	Power/Other	
F23	D19#	Source Synch	Input/Output
F24	D20#	Source Synch	Input/Output
F25	VSS	Power/Other	
F26	D22#	Source Synch	Input/Output
G1	ADS#	Common Clock	Input/Output
G2	BNR#	Common Clock	Input/Output
G3	VSS	Power/Other	
G4	LOCK#	Common Clock	Input/Output
G5	RS1#	Common Clock	Input
G6	VSS	Power/Other	
G21	VSS	Power/Other	
G22	D10#	Source Synch	Input/Output
G23	D18#	Source Synch	Input/Output
G24	VSS	Power/Other	

Table 24. Numerical Pin Assignment

Pin #	Pin Name	Signal Buffer Type	Direction
G25	DBI1#	Source Synch	Input/Output
G26	D25#	Source Synch	Input/Output
H1	VSS	Power/Other	
H2	DRDY#	Common Clock	Input/Output
H3	REQ4#	Source Synch	Input/Output
H4	VSS	Power/Other	
H5	DBSY#	Common Clock	Input/Output
H6	BR0#	Common Clock	Input/Output
H21	D11#	Source Synch	Input/Output
H22	D16#	Source Synch	Input/Output
H23	VSS	Power/Other	
H24	D26#	Source Synch	Input/Output
H25	D31#	Source Synch	Input/Output
H26	VSS	Power/Other	
J1	REQ0#	Source Synch	Input/Output
J2	VSS	Power/Other	
J3	REQ3#	Source Synch	Input/Output
J4	REQ2#	Source Synch	Input/Output
J5	VSS	Power/Other	
J6	TRDY#	Common Clock	Input
J21	D14#	Source Synch	Input/Output
J22	VSS	Power/Other	
J23	DSTBP1#	Source Synch	Input/Output
J24	D29#	Source Synch	Input/Output
J25	VSS	Power/Other	
J26	DP0#	Common Clock	Input/Output
K1	A6#	Source Synch	Input/Output
K2	A3#	Source Synch	Input/Output
K3	VSS	Power/Other	
K4	A4#	Source Synch	Input/Output
K5	REQ1#	Source Synch	Input/Output
K6	VSS	Power/Other	
K21	VSS	Power/Other	
K22	DSTBN1#	Source Synch	Input/Output
K23	D30#	Source Synch	Input/Output
K24	VSS	Power/Other	
K25	DP1#	Common Clock	Input/Output
K26	DP2#	Common Clock	Input/Output
L1	VSS	Power/Other	
L2	A9#	Source Synch	Input/Output
L3	A7#	Source Synch	Input/Output

Table 24. Numerical Pin Assignment

Pin #	Pin Name	Signal Buffer Type	Direction
L4	VSS	Power/Other	
L5	ADSTB0#	Source Synch	Input/Output
L6	A5#	Source Synch	Input/Output
L21	D24#	Source Synch	Input/Output
L22	D28#	Source Synch	Input/Output
L23	VSS	Power/Other	
L24	COMP0	Power/Other	Input
L25	DP3#	Common Clock	Input/Output
L26	VSS	Power/Other	
M1	A13#	Source Synch	Input/Output
M2	VSS	Power/Other	
M3	A10#	Source Synch	Input/Output
M4	A11#	Source Synch	Input/Output
M5	VSS	Power/Other	
M6	A8#	Source Synch	Input/Output
M21	D27#	Source Synch	Input/Output
M22	VSS	Power/Other	
M23	D32#	Source Synch	Input/Output
M24	D35#	Source Synch	Input/Output
M25	VSS	Power/Other	
M26	D37#	Source Synch	Input/Output
N1	A12#	Source Synch	Input/Output
N2	A14#	Source Synch	Input/Output
N3	VSS	Power/Other	
N4	A15#	Source Synch	Input/Output
N5	A16#	Source Synch	Input/Output
N6	VSS	Power/Other	
N21	VSS	Power/Other	
N22	D33#	Source Synch	Input/Output
N23	D36#	Source Synch	Input/Output
N24	VSS	Power/Other	
N25	D39#	Source Synch	Input/Output
N26	D38#	Source Synch	Input/Output
P1	COMP1	Power/Other	Input
P2	VSS	Power/Other	
P3	A19#	Source Synch	Input/Output
P4	A20#	Source Synch	Input/Output
P5	VSS	Power/Other	
P6	A24#	Source Synch	Input/Output
P21	D34#	Source Synch	Input/Output
P22	VSS	Power/Other	

Table 24. Numerical Pin Assignment

Pin #	Pin Name	Signal Buffer Type	Direction
P23	DSTBP#2	Source Synch	Input/Output
P24	D41#	Source Synch	Input/Output
P25	VSS	Power/Other	
P26	DBI2#	Source Synch	Input/Output
R1	VSS	Power/Other	
R2	A18#	Source Synch	Input/Output
R3	A21#	Source Synch	Input/Output
R4	VSS	Power/Other	
R5	ADSTB1#	Source Synch	Input/Output
R6	A28#	Source Synch	Input/Output
R21	D40#	Source Synch	Input/Output
R22	DSTBN#2	Source Synch	Input/Output
R23	VSS	Power/Other	
R24	D43#	Source Synch	Input/Output
R25	D42#	Source Synch	Input/Output
R26	VSS	Power/Other	
T1	A17#	Source Synch	Input/Output
T2	A22#	Source Synch	Input/Output
T3	VSS	Power/Other	
T4	A26#	Source Synch	Input/Output
T5	A30#	Source Synch	Input/Output
T6	VSS	Power/Other	
T21	VSS	Power/Other	
T22	D46#	Source Synch	Input/Output
T23	D47#	Source Synch	Input/Output
T24	VSS	Power/Other	
T25	D45#	Source Synch	Input/Output
T26	D44#	Source Synch	Input/Output
U1	A23#	Source Synch	Input/Output
U2	VSS	Power/Other	
U3	A25#	Source Synch	Input/Output
U4	A31#	Source Synch	Input/Output
U5	VSS	Power/Other	
U6	TESTHI8	Power/Other	Input
U21	D52#	Source Synch	Input/Output
U22	VSS	Power/Other	
U23	D50#	Source Synch	Input/Output
U24	D49#	Source Synch	Input/Output
U25	VSS	Power/Other	
U26	D48#	Source Synch	Input/Output
V1	VSS	Power/Other	

Table 24. Numerical Pin Assignment

Pin #	Pin Name	Signal Buffer Type	Direction
V2	A27#	Source Synch	Input/Output
V3	A32#	Source Synch	Input/Output
V4	VSS	Power/Other	
V5	AP1#	Common Clock	Input/Output
V6	MCERR#	Common Clock	Input/Output
V21	DBI3#	Source Synch	Input/Output
V22	D53#	Source Synch	Input/Output
V23	VSS	Power/Other	
V24	D54#	Source Synch	Input/Output
V25	D51#	Source Synch	Input/Output
V26	VSS	Power/Other	
W1	A29#	Source Synch	Input/Output
W2	A33#	Source Synch	Input/Output
W3	VSS	Power/Other	
W4	TESTHI9	Power/Other	Input
W5	INIT#	Asynch GTL+	Input
W6	VSS	Power/Other	
W21	VSS	Power/Other	
W22	DSTBN3#	Source Synch	Input/Output
W23	DSTBP3#	Source Synch	Input/Output
W24	VSS	Power/Other	
W25	D57#	Source Synch	Input/Output
W26	D55#	Source Synch	Input/Output
Y1	A34#	Source Synch	Input/Output
Y2	VSS	Power/Other	
Y3	TESTHI10	Power/Other	Input
Y4	STPCLK#	Asynch GTL+	Input
Y5	VSS	Power/Other	
Y6	BPM3#	Common Clock	Input/Output
Y21	D60#	Source Synch	Input/Output
Y22	VSS	Power/Other	
Y23	D58#	Source Synch	Input/Output
Y24	D59#	Source Synch	Input/Output
Y25	VSS	Power/Other	
Y26	D56#	Source Synch	Input/Output
AA1	VSS	Power/Other	
AA2	TESTHI1	Power/Other	Input
AA3	BINIT#	Common Clock	Input/Output
AA4	VSS	Power/Other	
AA5	BPM4#	Common Clock	Input/Output
AA6	GTLREF	Power/Other	Input

Table 24. Numerical Pin Assignment

Pin #	Pin Name	Signal Buffer Type	Direction
AA7	VSS	Power/Other	
AA8	VCC	Power/Other	
AA9	VSS	Power/Other	
AA10	VCC	Power/Other	
AA11	VSS	Power/Other	
AA12	VCC	Power/Other	
AA13	VSS	Power/Other	
AA14	VCC	Power/Other	
AA15	VSS	Power/Other	
AA16	VCC	Power/Other	
AA17	VSS	Power/Other	
AA18	VCC	Power/Other	
AA19	VSS	Power/Other	
AA20	TESTHI6	Power/Other	Input
AA21	GTLREF	Power/Other	Input
AA22	D62#	Source Synch	Input/Output
AA23	VSS	Power/Other	
AA24	D63#	Source Synch	Input/Output
AA25	D61#	Source Synch	Input/Output
AA26	VSS	Power/Other	
AB1	A35#	Source Synch	Input/Output
AB2	RSP#	Common Clock	Input
AB3	VSS	Power/Other	
AB4	BPM5#	Common Clock	Input/Output
AB5	BPM1#	Common Clock	Input/Output
AB6	VSS	Power/Other	
AB7	VCC	Power/Other	
AB8	VSS	Power/Other	
AB9	VCC	Power/Other	
AB10	VSS	Power/Other	
AB11	VCC	Power/Other	
AB12	VSS	Power/Other	
AB13	VCC	Power/Other	
AB14	VSS	Power/Other	
AB15	VCC	Power/Other	
AB16	VSS	Power/Other	
AB17	VCC	Power/Other	
AB18	VSS	Power/Other	
AB19	VCC	Power/Other	
AB20	VSS	Power/Other	
AB21	VSS	Power/Other	

Table 24. Numerical Pin Assignment

Pin #	Pin Name	Signal Buffer Type	Direction
AB22	TESTHI7	Power/Other	Input
AB23	PWRGOOD	Power/Other	Input
AB24	VSS	Power/Other	
AB25	RESET#	Common Clock	Input
AB26	SLP#	Asynch GTL+	Input
AC1	AP0#	Common Clock	Input/Output
AC2	VSS	Power/Other	
AC3	IERR#	Asynch GTL+	Output
AC4	BPM2#	Common Clock	Input/Output
AC5	VSS	Power/Other	
AC6	BPM0#	Common Clock	Input/Output
AC7	VSS	Power/Other	
AC8	VCC	Power/Other	
AC9	VSS	Power/Other	
AC10	VCC	Power/Other	
AC11	VSS	Power/Other	
AC12	VCC	Power/Other	
AC13	VSS	Power/Other	
AC14	VCC	Power/Other	
AC15	VSS	Power/Other	
AC16	VCC	Power/Other	
AC17	VSS	Power/Other	
AC18	VCC	Power/Other	
AC19	VSS	Power/Other	
AC20	TESTHI3	Power/Other	Input
AC21	TESTHI2	Power/Other	Input
AC22	VSS	Power/Other	
AC23	TESTHI5	Power/Other	Input
AC24	TESTHI4	Power/Other	Input
AC25	VSS	Power/Other	
AC26	ITP_CLK0	TAP	Input
AD1	BOOTSELECT	Power/Other	Input
AD2	VIDPWRGD	Power/Other	Input
AD3	VID5	Power/Other	Output
AD4	VSS	Power/Other	
AD5	BSEL1	Power/Other	Output
AD6	BSEL0	Power/Other	Output
AD7	VCC	Power/Other	
AD8	VSS	Power/Other	
AD9	VCC	Power/Other	
AD10	VSS	Power/Other	

Table 24. Numerical Pin Assignment

Pin #	Pin Name	Signal Buffer Type	Direction
AD11	VCC	Power/Other	
AD12	VSS	Power/Other	
AD13	VCC	Power/Other	
AD14	VSS	Power/Other	
AD15	VCC	Power/Other	
AD16	VSS	Power/Other	
AD17	VCC	Power/Other	
AD18	VSS	Power/Other	
AD19	VCC	Power/Other	
AD20	VCCIOPLL	Power/Other	
AD21	VSS	Power/Other	
AD22	VSSA	Power/Other	
AD23	VSS	Power/Other	
AD24	TESTHI0	Power/Other	Input
AD25	TESTHI12	Power/Other	Input
AD26	ITP_CLK1	TAP	Input
AE1	VID4	Power/Other	Output
AE2	VID3	Power/Other	Output
AE3	VID2	Power/Other	Output
AE4	VID1	Power/Other	Output
AE5	VID0	Power/Other	Output
AE6	VCC	Power/Other	
AE7	VSS	Power/Other	
AE8	VCC	Power/Other	
AE9	VSS	Power/Other	
AE10	VCC	Power/Other	
AE11	VSS	Power/Other	
AE12	VCC	Power/Other	
AE13	VSS	Power/Other	
AE14	VCC	Power/Other	
AE15	VSS	Power/Other	
AE16	VCC	Power/Other	
AE17	VSS	Power/Other	
AE18	VCC	Power/Other	

Table 24. Numerical Pin Assignment

Pin #	Pin Name	Signal Buffer Type	Direction
AE19	VSS	Power/Other	
AE20	VCC	Power/Other	
AE21	RESERVED		
AE22	VSS	Power/Other	
AE23	VCCA	Power/Other	
AE24	VSS	Power/Other	
AE25	DBR#	Power/Other	Output
AE26	OPTIMIZED/COMPAT#	Power/Other	Input
AF1	VSS	Power/Other	
AF2	VCC	Power/Other	
AF3	VCCVIDLB	Power/Other	Input
AF4	VCCVID	Power/Other	Input
AF5	VCC	Power/Other	
AF6	VSS	Power/Other	
AF7	VCC	Power/Other	
AF8	VSS	Power/Other	
AF9	VCC	Power/Other	
AF10	VSS	Power/Other	
AF11	VCC	Power/Other	
AF12	VSS	Power/Other	
AF13	VCC	Power/Other	
AF14	VSS	Power/Other	
AF15	VCC	Power/Other	
AF16	VSS	Power/Other	
AF17	VCC	Power/Other	
AF18	VSS	Power/Other	
AF19	VCC	Power/Other	
AF20	VSS	Power/Other	
AF21	VCC	Power/Other	
AF22	BCLK0	Bus Clock	Input
AF23	BCLK1	Bus Clock	Input
AF24	RESERVED		
AF25	RESERVED		
AF26	SKTOCC#	Power/Other	Output