ZR8 SYSTEM DIAGRAM

AMD Smarter Choice

RAMP

PCB STACK UP

LAYER 1 : TOP
LAYER 2 : GND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : IN3
LAYER 7 : GND
LAYER 8 : BOT

SGN@----->Internal CLK GEN.
GN@ ----->External CLK GEN.
IV@ -----> iGPU
SW@ -----> dGPU
SP@ -----> iGPU & dGPU notice
SPE@ ----->Only for dGPU notice
SIDE@ ----> Side port

DDR3-SODIMM1 P5
DDR3-SODIMM2 P6
DDR3 channel A
DDR3 channel B

AMD Champlain
35mm X 35mm
S1G4 Processor
638P (PGA)45W/35W
P2 ~ 4

CPU THERMAL SENSOR P4

CPU_CLK
NBGFX_CLK
NBGPP_CLK
SBLINK_CLK

CLOCK GEN From SB P11

HT3

PCI-E

NORTH BRIDGE
RS880
A12
21mm X 21mm, 528pin BGA
P7 ~ 10

PCI-Express 16X

ATI
Madison LP
128-bit M2 Pkg
29mm X 29mm
P16 ~ 20

HDMI
CRT
LVDS

HDMI P25
CRT P24
LVDS P24

MUXs (S.G) P24

SIDE port P7

DDR3 800MHz
VRAM
64MX16X4,64 bit
64MX16X8,128 bit
P22,23

CRT
LVDS

LAN
Atheros
PCIE-LAN
AR8151
(10/100/1000)
P26

Mini PCI-E Card
(Wireless LAN)
P27

RJ45 P26

ALINK X4

SATA - HDD1 P28
SATA - ODD P28
SATA0 150MB
SATA1 150MB

SOUTH BRIDGE
SB820
21mm X 21mm, 528pin BGA
4.5W(Ext)
4.3W(Int)
P11 ~ 14

BT P31

USB1.1
USB2.0

USB2.0 Ports X1 P31
Webcam P24
CardReader AU6433/AU6437 P30

USB BOARD
USB2.0 Ports x 3
P31

LPC
Azalia

Winbond KBC
NPCE781L
P34

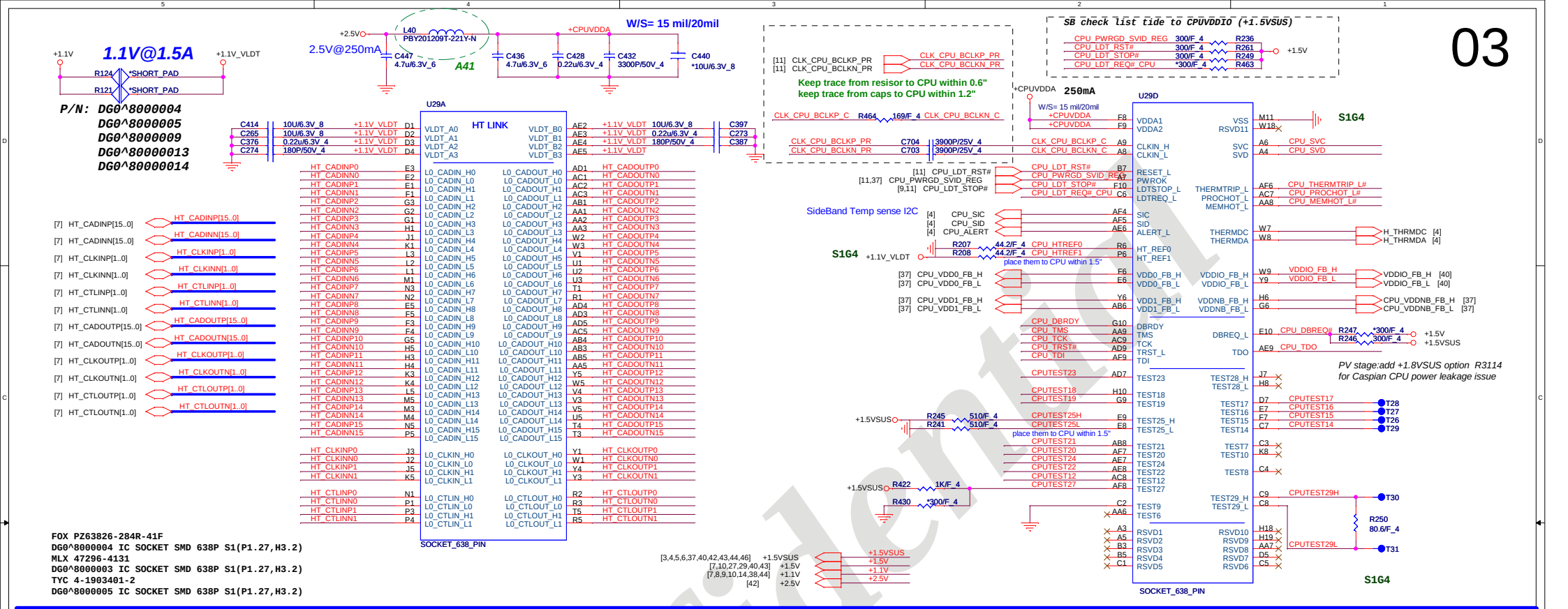
Codec
RTL ALC271X
P29

Keyboard Touch Pad P33 P31
FAN P33
SPI P34
Digital MIC P24
AUDIO CONN (Phone/ MIC) P29
Speaker P29

Charger (ISL88731A) P35
DC/DC (3VPCU / 5VPCU) RT8206B P36
CPU_VCORE (VCORE) ISL6265A P37
DC/DC (+1.1V_S5) UP6111AQD P38
DC/DC (NB_CORE) UP6111AQD P39
DC/DC (+1.5VSUS) RT8207A P40
DC/DC (GPU_CORE) MAX8792ETD+T P41
DC/DC (+1.8V/+1V/+2.5V) HPA00835RTER / RT9018A / RT9025-25PSP P42
DC/DC (CPU_VDDR) RT9025-25PSP P43

PROJECT : ZR8
Quanta Computer Inc.

Size	Document Number	Rev
	Block Diagram	1A
Date: Wednesday, May 27, 2009	Sheet 1 of 49	


03
1.1V@1.5A
P/N: DG0^8000004
DG0^8000005
DG0^8000009
DG0^80000013
DG0^80000014
2.5V@250mA
A41
W/S= 15 mil/20mil
U29A
HT LINK
SOCKET_638_PIN
Keep trace from resisor to CPU within 0.6"
keep trace from caps to CPU within 1.2"
SB check list tide to CPUVDDIO (+1.5VSUS)
250mA
U29D
S1G4
SideBand Temp sense I2C
PV stage:add +1.8VSUS option R3114
for Caspian CPU power leakage issue
FOX PZ63826-284R-41F
DG0^8000004 IC SOCKET SMD 638P S1(P1.27,H3.2)
MLX 47296-4131
DG0^8000003 IC SOCKET SMD 638P S1(P1.27,H3.2)
TYC 4-1903401-2
DG0^8000005 IC SOCKET SMD 638P S1(P1.27,H3.2)
The RS880 family does not support CLMC architecture
The LDTREQ# connection from the CPU to ALLOW_LDTSTOP
of the Northbridge is no longer required.
for debug only
S1g4 does not support MEMHOT#
Serial VID
VFIX MODE
VID Override Circuit
SVC
SVD
Voltage Output
0 0 1.1V
0 1 1.0V
1 0 0.9V
1 1 0.8V
HDT Connector
CN7
*HDT_CONN
PROJECT : ZR8
Quanta Computer Inc.
S1G4 HT,CTL I/F 1/3
Wednesday, May 27, 2009
Sheet 2 of 49
Confidential

Processor Memory Interface

VDDR=>1.75A

```
VDDR=> 0.9V support  1066 / 800 DDR
VDDR= >1.05V support 1333 / 1066 / 800 DDR
```

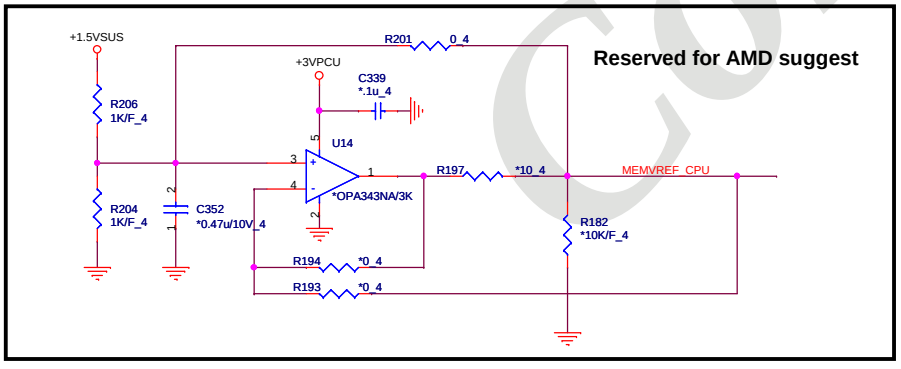
PLACE THEM CLOSE TO CPU WITHIN 1"

U29B — MEM:CMD/CTRL/CLK — SOCKET_638_PIN

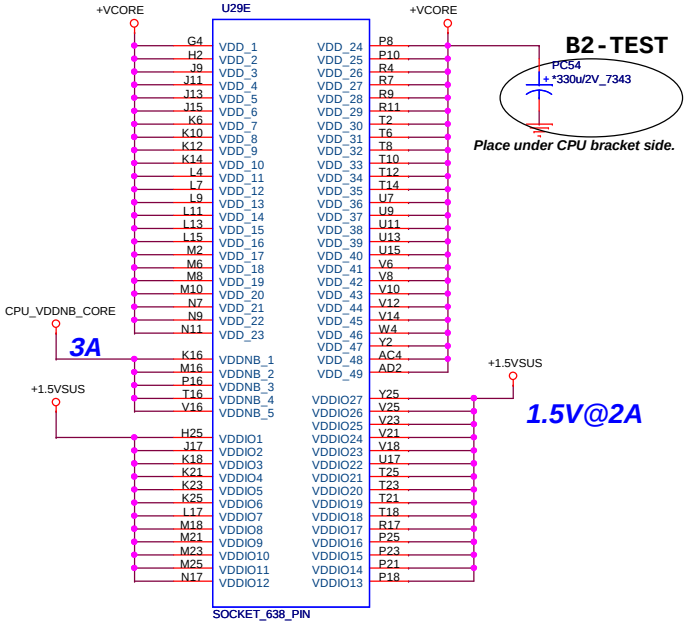
U29C — MEM:DATA — SOCKET_638_PIN

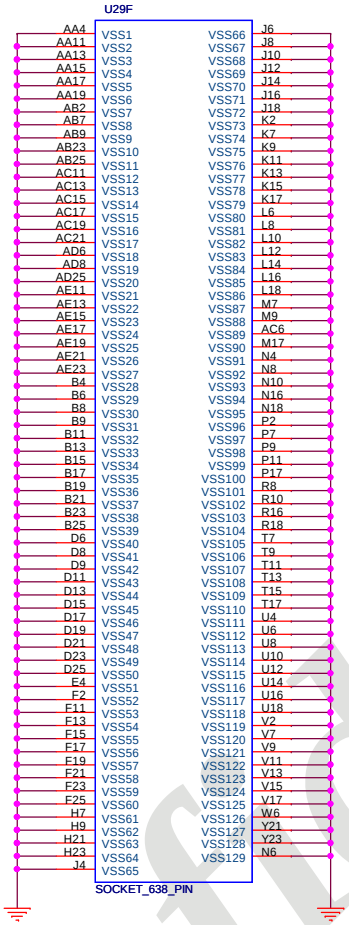
Place close to socket

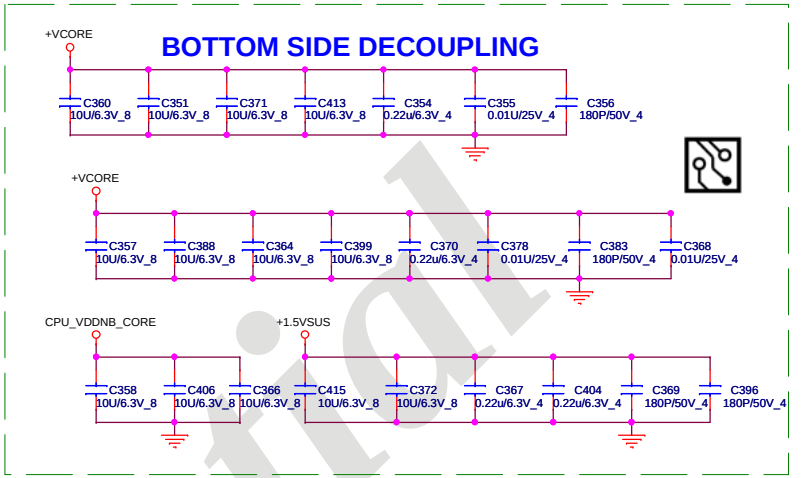
Reserved for AMD suggest

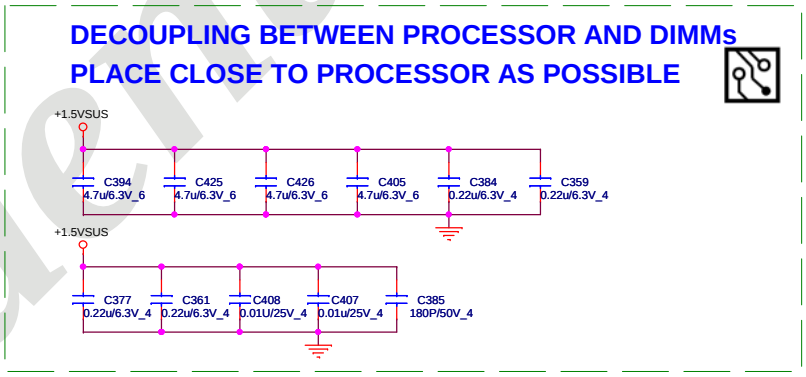


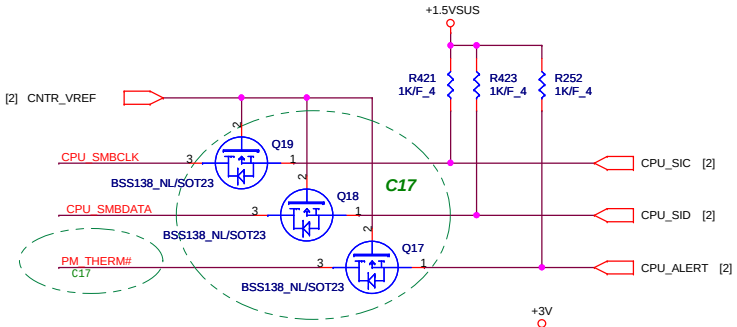
PROJECT : ZR8			
Quanta Computer Inc.			
Size	Document Number		Rev
	S1G4 DDRIII MEMORY I/F 2/3		1A
Date: Wednesday, May 27, 2009	Sheet 3 of 49		



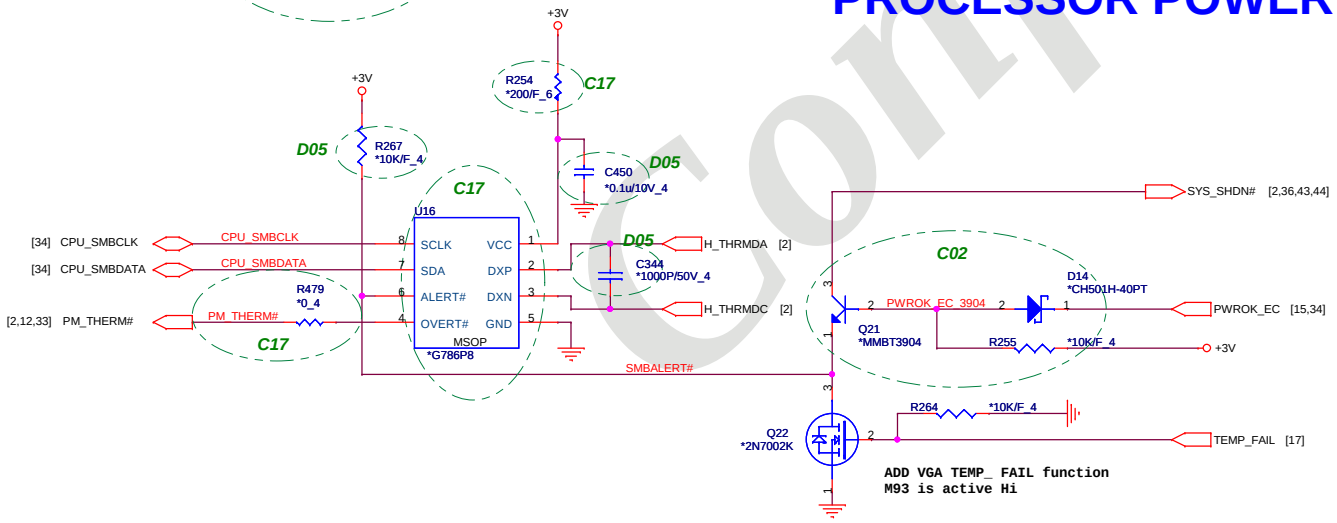




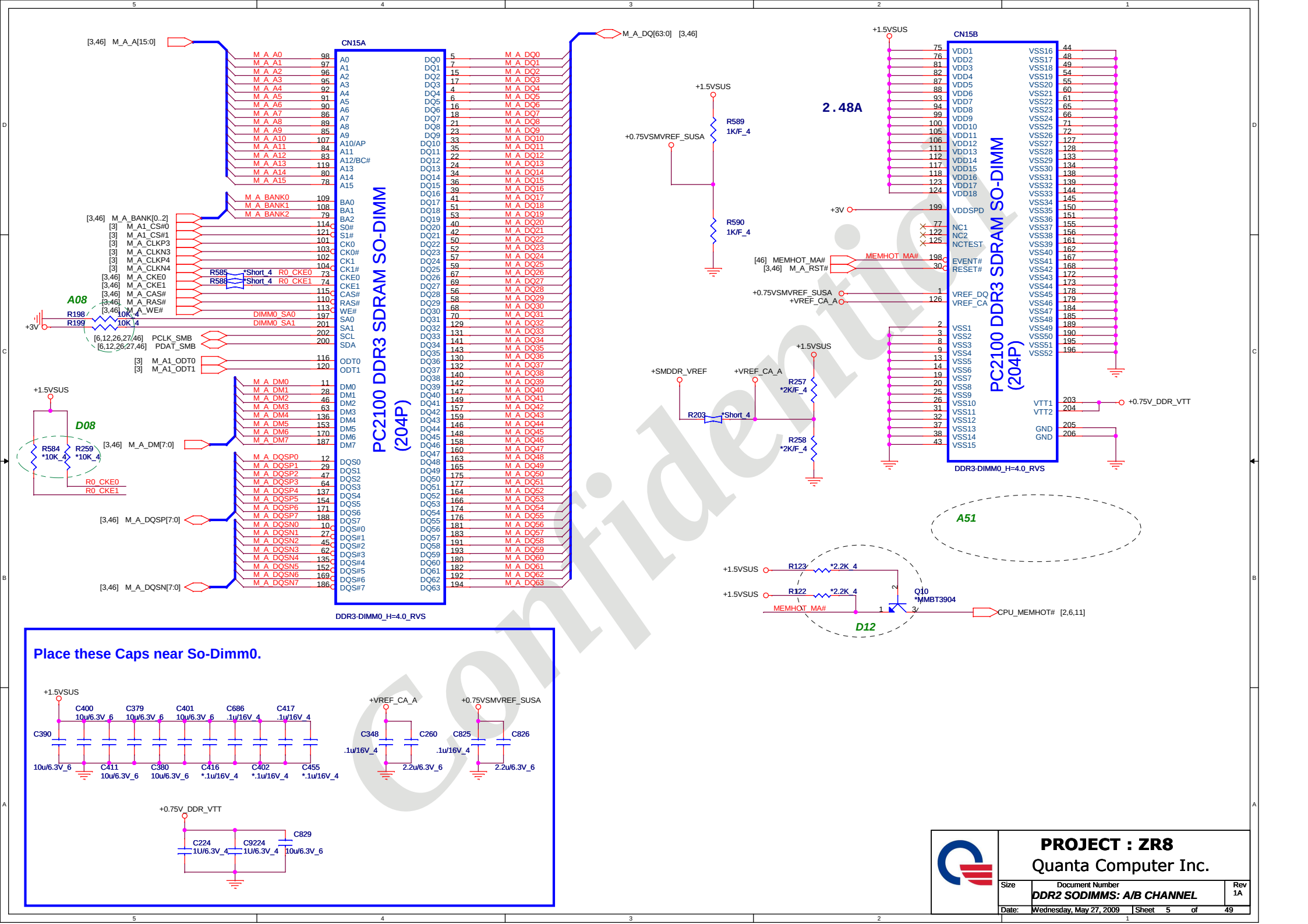


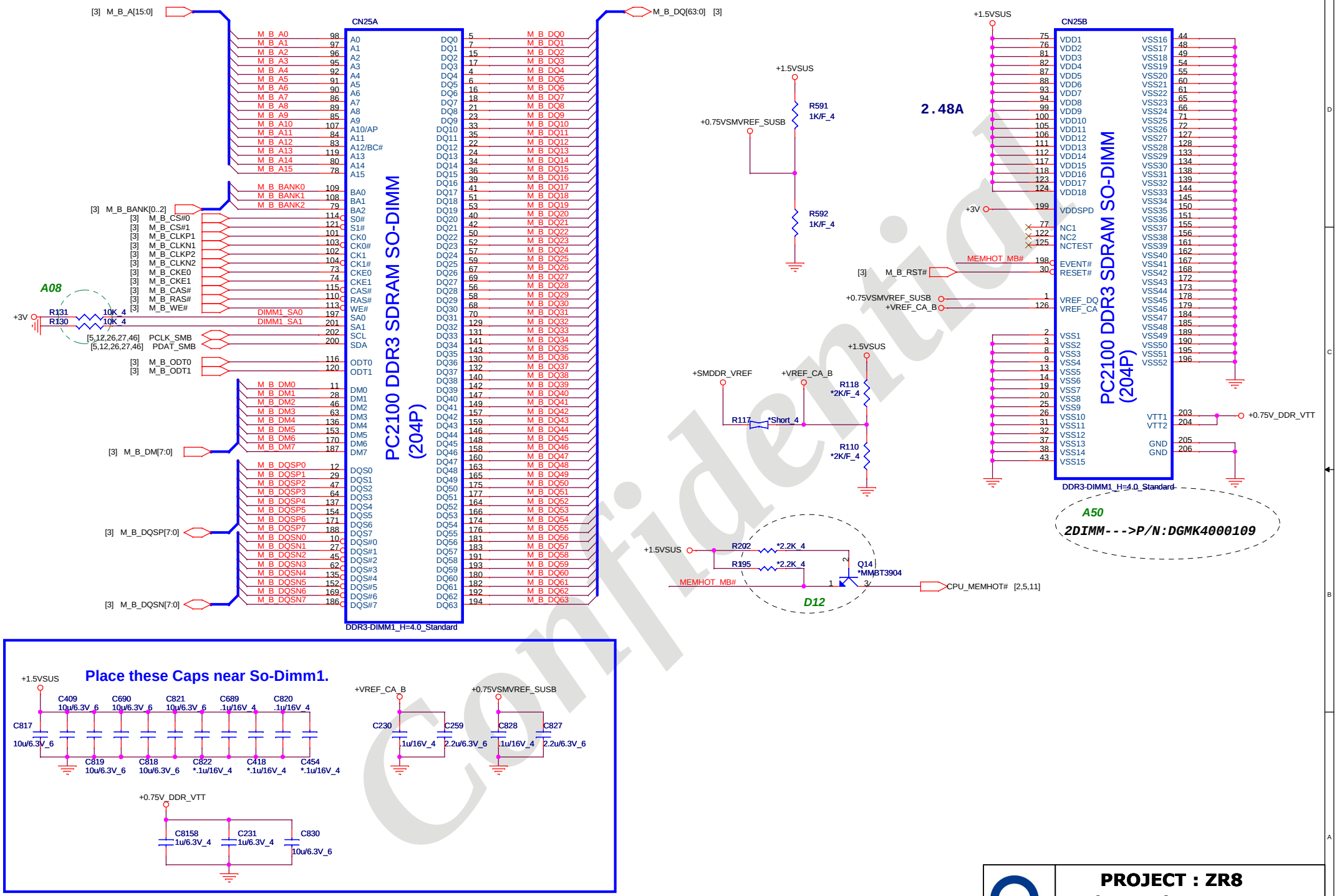


PROCESSOR POWER AND GROUND



PROJECT : ZR8		
Quanta Computer Inc.		
Size	Document Number: S1G4 PWR & GND 3/3	Rev: 1A
Date: Wednesday, May 27, 2009	Sheet 4 of 49	




CN25A
PC2100 DDR3 SDRAM SO-DIMM
(204P)
DDR3-DIMM1_H=4.0_Standard
CN25B
PC2100 DDR3 SDRAM SO-DIMM
(204P)
DDR3-DIMM1_H=4.0_Standard
2.48A
A08
A50
2DIMM-->P/N:DGMK4000109
D12
Place these Caps near So-Dimm1.
Confidential
PROJECT : ZR8
Quanta Computer Inc.
DDR2 SODIMMS: A/B CHANNEL
Wednesday, May 27, 2009
Sheet 6 of 49

SIDE PORT

11/4

08

+1.5V_MEM_VDDQ

C9788 SIDE@0.1u/10V_4 — R599 SIDE@1K/F_4 — SPM_VREFDQ — C9790 SIDE@0.1u/10V_4 — R601 SIDE@1K/F_4

C9789 SIDE@0.1u/10V_4 — R600 SIDE@1K/F_4 — SPM_VREFCA — C9791 SIDE@0.1u/10V_4 — R602 SIDE@1K/F_4

U28A

PART 1 OF 6

HYPER TRANSPORT CPU I/F

HT_CADOUTP0	Y25	HT_RXCAD0P	HT_TXCAD0P	D24	HT_CADINP0
HT_CADOUTN0	Y24	HT_RXCAD0N	HT_TXCAD0N	D25	HT_CADINN0
HT_CADOUTP1	V22	HT_RXCAD1P	HT_TXCAD1P	E24	HT_CADINP1
HT_CADOUTN1	V23	HT_RXCAD1N	HT_TXCAD1N	E25	HT_CADINN1
HT_CADOUTP2	V25	HT_RXCAD2P	HT_TXCAD2P	F24	HT_CADINP2
HT_CADOUTN2	V24	HT_RXCAD2N	HT_TXCAD2N	F25	HT_CADINN2
HT_CADOUTP3	U24	HT_RXCAD3P	HT_TXCAD3P	F23	HT_CADINP3
HT_CADOUTN3	U25	HT_RXCAD3N	HT_TXCAD3N	F22	HT_CADINN3
HT_CADOUTP4	T25	HT_RXCAD4P	HT_TXCAD4P	H23	HT_CADINP4
HT_CADOUTN4	T24	HT_RXCAD4N	HT_TXCAD4N	H22	HT_CADINN4
HT_CADOUTP5	P22	HT_RXCAD5P	HT_TXCAD5P	J25	HT_CADINP5
HT_CADOUTN5	P23	HT_RXCAD5N	HT_TXCAD5N	J24	HT_CADINN5
HT_CADOUTP6	P25	HT_RXCAD6P	HT_TXCAD6P	K24	HT_CADINP6
HT_CADOUTN6	P24	HT_RXCAD6N	HT_TXCAD6N	K25	HT_CADINN6
HT_CADOUTP7	N24	HT_RXCAD7P	HT_TXCAD7P	K23	HT_CADINP7
HT_CADOUTN7	N25	HT_RXCAD7N	HT_TXCAD7N	K22	HT_CADINN7
HT_CADOUTP8	AC24	HT_RXCAD8P	HT_TXCAD8P	F21	HT_CADINP8
HT_CADOUTN8	AC25	HT_RXCAD8N	HT_TXCAD8N	G21	HT_CADINN8
HT_CADOUTP9	AB25	HT_RXCAD9P	HT_TXCAD9P	G20	HT_CADINP9
HT_CADOUTN9	AB24	HT_RXCAD9N	HT_TXCAD9N	H21	HT_CADINN9
HT_CADOUTP10	AA24	HT_RXCAD10P	HT_TXCAD10P	J20	HT_CADINP10
HT_CADOUTN10	AA25	HT_RXCAD10N	HT_TXCAD10N	J21	HT_CADINN10
HT_CADOUTP11	Y22	HT_RXCAD11P	HT_TXCAD11P	J18	HT_CADINP11
HT_CADOUTN11	Y23	HT_RXCAD11N	HT_TXCAD11N	K17	HT_CADINN11
HT_CADOUTP12	W21	HT_RXCAD12P	HT_TXCAD12P	L19	HT_CADINP12
HT_CADOUTN12	W20	HT_RXCAD12N	HT_TXCAD12N	J19	HT_CADINN12
HT_CADOUTP13	V21	HT_RXCAD13P	HT_TXCAD13P	M19	HT_CADINP13
HT_CADOUTN13	V20	HT_RXCAD13N	HT_TXCAD13N	L18	HT_CADINN13
HT_CADOUTP14	U20	HT_RXCAD14P	HT_TXCAD14P	M21	HT_CADINP14
HT_CADOUTN14	U21	HT_RXCAD14N	HT_TXCAD14N	P21	HT_CADINN14
HT_CADOUTP15	U19	HT_RXCAD15P	HT_TXCAD15P	P18	HT_CADINP15
HT_CADOUTN15	U18	HT_RXCAD15N	HT_TXCAD15N	M18	HT_CADINN15
HT_CLKOUTP0	T22	HT_RXCLK0P	HT_TXCLK0P	H24	HT_CLKINP0
HT_CLKOUTN0	T23	HT_RXCLK0N	HT_TXCLK0N	H25	HT_CLKINN0
HT_CLKOUTP1	AB23	HT_RXCLK1P	HT_TXCLK1P	L21	HT_CLKINP1
HT_CLKOUTN1	AA22	HT_RXCLK1N	HT_TXCLK1N	L20	HT_CLKINN1
HT_CTLOUTP0	M22	HT_RXCTL0P	HT_TXCTL0P	M24	HT_CTLINP0
HT_CTLOUTN0	M23	HT_RXCTL0N	HT_TXCTL0N	M25	HT_CTLINN0
HT_CTLOUTP1	R21	HT_RXCTL1P	HT_TXCTL1P	P19	HT_CTLINP1
HT_CTLOUTN1	R20	HT_RXCTL1N	HT_TXCTL1N	R18	HT_CTLINN1
		HT_RXCALP	HT_TXCALP	B24	HT_TXCALP
		HT_RXCALN	HT_TXCALN	B25	HT_TXCALN

RS880M_A11

Ra: R183 301/F_4 — HT_RXCALP / HT_RXCALN

Rb: HT_TXCALP — R192 301/F_4 — HT_TXCALN

HT_CADOUTP[15..0] HT_CADOUTP[15..0] [2]
HT_CADOUTN[15..0] HT_CADOUTN[15..0] [2]
HT_CLKOUTP[1..0] HT_CLKOUTP[1..0] [2]
HT_CLKOUTN[1..0] HT_CLKOUTN[1..0] [2]
HT_CTLOUTP[1..0] HT_CTLOUTP[1..0] [2]
HT_CTLOUTN[1..0] HT_CTLOUTN[1..0] [2]
HT_CADINP[15..0] HT_CADINP[15..0] [2]
HT_CADINN[15..0] HT_CADINN[15..0] [2]
HT_CLKINP[1..0] HT_CLKINP[1..0] [2]
HT_CLKINN[1..0] HT_CLKINN[1..0] [2]
HT_CTLINP[1..0] HT_CTLINP[1..0] [2]
HT_CTLINN[1..0] HT_CTLINN[1..0] [2]

signals	RS880	RX880
HT_TXCALP	Ra 301 ohm 1%	Ra 1.21k ohm 1%
HT_TXCALN		
HT_RXCALP	Rb 301 ohm 1%	Rb 1.21k ohm 1%
HT_RXCALN		

RES CHIP 1.21K 1/16W +-1%(0402)
P/N : CS21212FB18

This block is for UMA only , Discrete can remove all component

[9,10,15,24,37,42,43,44] +1.8V
[2,8,9,10,14,38,44] +1.1V

U39

SPM_VREFCA	M9	VREFCA	DQL0	E4	SPM_DQ5
SPM_VREFDQ	H2	VREFDQ	DQL1	F8	SPM_DQ3
		DQL2	DQL2	F3	SPM_DQ4
SPM_A0	N4	A0	DQL3	F9	SPM_DQ0
SPM_A1	P8	A1	DQL4	H4	SPM_DQ6
SPM_A2	P4	A2	DQL5	H9	SPM_DQ1
SPM_A3	N3	A3	DQL6	G3	SPM_DQ7
SPM_A4	P9	A4	DQL7	H8	SPM_DQ2
SPM_A5	P3	A5			
SPM_A6	R9	A6			
SPM_A7	R3	A7	DQU0	D8	SPM_DQ14
SPM_A8	T9	A8	DQU1	C4	SPM_DQ9
SPM_A9	R4	A9	DQU2	C9	SPM_DQ15
SPM_A10	L8	A10/AP	DQU3	C3	SPM_DQ8
SPM_A11	R8	A11	DQU4	A8	SPM_DQ10
SPM_A12	N8	A12/BC	DQU5	A3	SPM_DQ11
SPM_A13	T4	A13	DQU6	B9	SPM_DQ13
	T8	A14	DQU7	A4	SPM_DQ12
	M8	A15			
SPM_BA0	M3	BA0	VDD#B3	B3	+1.5V_MEM_VDDQ
SPM_BA1	N9	BA1	VDD#D10	D10	
SPM_BA2	M4	BA2	VDD#G8	G8	
			VDD#K3	K3	
			VDD#K9	K9	
			VDD#N2	N2	
SPM_CLKP	J8	CK	VDD#N10	N10	
R593 *SIDE@100/F_4	SPM_CLKN K8	CK	VDD#R2	R2	
SPM_CKE	K10	CKE	VDD#R10	R10	
SPM_ODT	K2	ODT	VDDQ#A2	A2	+1.5V_MEM_VDDQ
SPM_CS#	L3	CS	VDDQ#A9	A9	
SPM_RAS#	J4	RAS	VDDQ#C2	C2	
SPM_CAS#	K4	CAS	VDDQ#C10	C10	
SPM_WE#	L4	WE	VDDQ#D3	D3	
			VDDQ#E10	E10	
			VDDQ#F2	F2	
SPM_DQS0P	F4	DQSL	VDDQ#H3	H3	
SPM_DQS1P	C8	DQSU	VDDQ#H10	H10	
SPM_DM0	E8	DML	VSS#A10	A10	
SPM_DM1	D4	DMU	VSS#B4	B4	
			VSS#E2	E2	
			VSS#G9	G9	
SPM_DQS0N	G4	DQSL	VSS#J3	J3	
SPM_DQS1N	B8	DQSU	VSS#J9	J9	
			VSS#M2	M2	
			VSS#M10	M10	
			VSS#P2	P2	
[12] SP_DDR3_RST#	T3	RESET	VSS#P10	P10	
VMA_ZQ	L9	ZQ	VSS#T2	T2	
			VSS#T10	T10	
			VSSQ#B2	B2	
			VSSQ#B10	B10	
			VSSQ#D2	D2	
			VSSQ#D9	D9	
			VSSQ#E3	E3	
			VSSQ#E9	E9	
			VSSQ#F10	F10	
			VSSQ#G2	G2	
			VSSQ#G10	G10	
	J2	NC#J2			
	L2	NC#L2			
	J10	NC#J10			
	L10	NC#L10			

100-BALL SDRAM DDR3
SIDE@H5TQ1G63AFR-14C

+1.5V_MEM_VDDQ — R603 SIDE@10K/F_4

R604 SIDE@240/F_4

A09

U28D

PART 4 OF 6

SBD_MEM/DVO_I/F

SPM_A0	AB12	MEM_A0(NC)	MEM_DQ0/DVO_VSYNC(NC)	AA18	SPM_DQ0
SPM_A1	AE16	MEM_A1(NC)	MEM_DQ1/DVO_HSYNC(NC)	AA20	SPM_DQ1
SPM_A2	V11	MEM_A2(NC)	MEM_DQ2/DVO_DE(NC)	AA19	SPM_DQ2
SPM_A3	AE15	MEM_A3(NC)	MEM_DQ3/DVO_D0(NC)	Y19	SPM_DQ3
SPM_A4	AA12	MEM_A4(NC)	MEM_DQ4(NC)	V17	SPM_DQ4
SPM_A5	AB16	MEM_A5(NC)	MEM_DQ5/DVO_D1(NC)	AA17	SPM_DQ5
SPM_A6	AB14	MEM_A6(NC)	MEM_DQ6/DVO_D2(NC)	AA15	SPM_DQ6
SPM_A7	AD14	MEM_A7(NC)	MEM_DQ7/DVO_D4(NC)	Y15	SPM_DQ7
SPM_A8	AD13	MEM_A8(NC)	MEM_DQ8/DVO_D3(NC)	AC20	SPM_DQ8
SPM_A9	AD15	MEM_A9(NC)	MEM_DQ9/DVO_D5(NC)	AD19	SPM_DQ9
SPM_A10	AC16	MEM_A10(NC)	MEM_DQ10/DVO_D6(NC)	AE22	SPM_DQ10
SPM_A11	AE13	MEM_A11(NC)	MEM_DQ11/DVO_D7(NC)	AC18	SPM_DQ11
SPM_A12	AC14	MEM_A12(NC)	MEM_DQ12(NC)	AB20	SPM_DQ12
SPM_A13	Y14	MEM_A13(NC)	MEM_DQ13/DVO_D9(NC)	AD22	SPM_DQ13
			MEM_DQ14/DVO_D10(NC)	AC22	SPM_DQ14
SPM_BA0	AD16	MEM_BA0(NC)	MEM_DQ15/DVO_D11(NC)	AD21	SPM_DQ15
SPM_BA1	AE17	MEM_BA1(NC)			
SPM_BA2	AD17	MEM_BA2(NC)	MEM_DQS0P/DVO_IDCKP(NC)	Y17	SPM_DQS0P
			MEM_DQS0N/DVO_IDCKN(NC)	W18	SPM_DQS0N
SPM_RAS#	W12	MEM_RASb(NC)	MEM_DQS1P(NC)	AD20	SPM_DQS1P
SPM_CAS#	Y12	MEM_CASb(NC)	MEM_DQS1N(NC)	AE21	SPM_DQS1N
SPM_WE#	AD18	MEM_WEb(NC)			
SPM_CS#	AB13	MEM_CSb(NC)	MEM_DM0(NC)	W17	SPM_DM0
SPM_CKE	AB18	MEM_CKE(NC)	MEM_DM1/DVO_D8(NC)	AE19	SPM_DM1
SPM_ODT	V14	MEM_ODT(NC)			
			IOPLLVDD18(NC)	AE23	IOPLLVDD18_SIDE_PORT
SPM_CLKP	V15	MEM_CKP(NC)	IOPLLVDD(NC)	AE24	IOPLLVDD_SIDE_PORT
SPM_CLKN	W14	MEM_CKN(NC)			
			IOPLLVSS(NC)	AD23	
SPM_COMPP	AE12	MEM_COMPP(NC)			
SPM_COMPN	AD12	MEM_COMPN(NC)	MEM_VREF(NC)	AE18	SPM_VREF1

RS880M_A11

+1.5V_MEM_VDDQ — R597 SIDE@40.2/F_4 — R607 SIDE@40.2/F_4

A41

L75 PBY160808T-221Y-N — L73 PBY160808T-221Y-N — +1.8V 15mA — +1.1V 26mA

C9794 SIDE@2.2u/6.3V_6

C9781 SIDE@2.2u/6.3V_6

IOPLLVDD18 - memory PLL not applicable to RX881

+1.5V_MEM_VDDQ

C9792 SIDE@0.1u/10V_4 — R605 SIDE@1K/F_4

SPM_VREF1

C9793 SIDE@0.1u/10V_4 — R606 SP@1K/F_4

R606
W/O side port
--->change to 0 Ohm
CS00002JB38

40 mil~50 mil

+1.5V_MEM_VDDQ

SIDE@0.1u/10V_4 — C9782
SIDE@0.1u/10V_4 — C9783
SIDE@10u/6.3V_6 — C9784
SIDE@1u/6.3V_4 — C9785
SIDE@1u/6.3V_4 — C9786
SIDE@10u/6.3V_6 — C9787

+1.5V — R598 SIDE@0_6

PROJECT : ZR8
Quanta Computer Inc.

Size	Document Number	Rev
	RS880M-HT LINK I/F 1/5	1A
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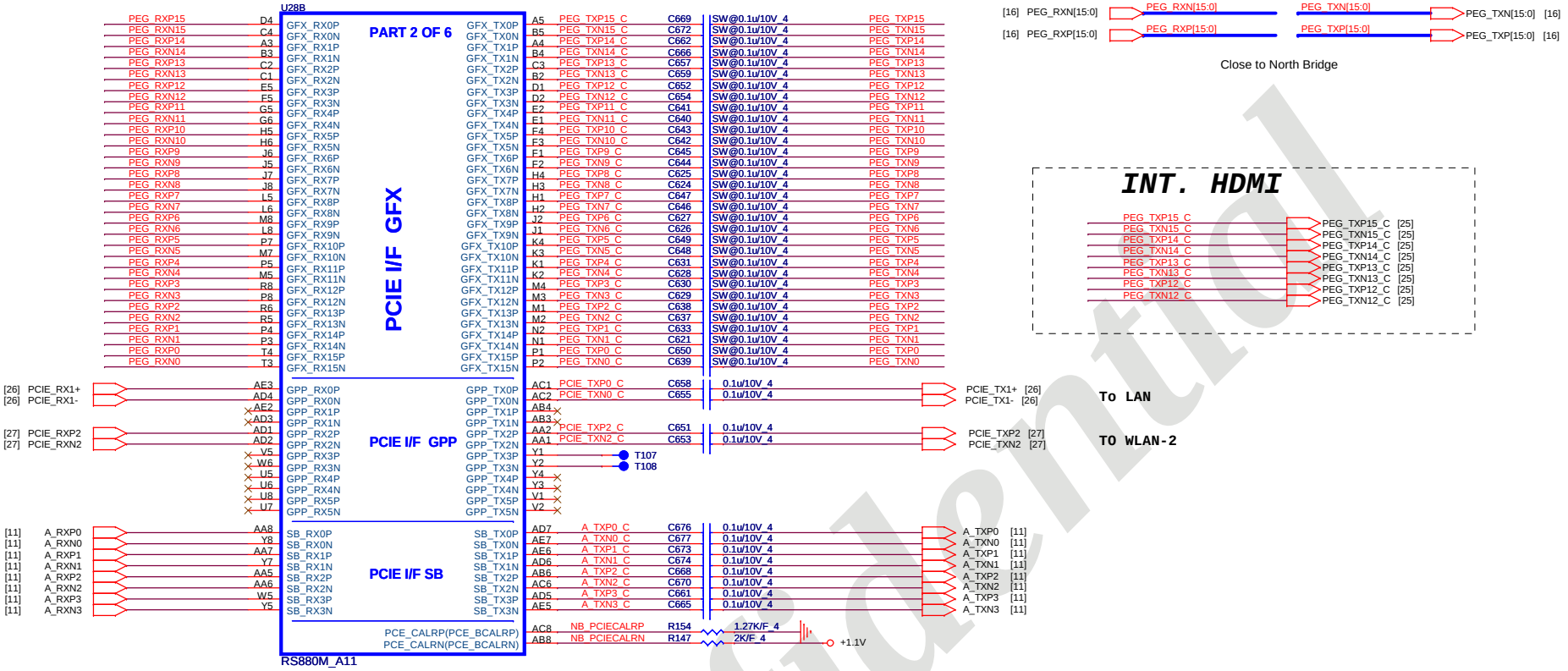

RS880 Display Port Support (muxed on GFX)

DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1

PROJECT : ZR8
Quanta Computer Inc.

Size	Document Number	Rev
	RS880M-PCIE I/F 2/5	1A
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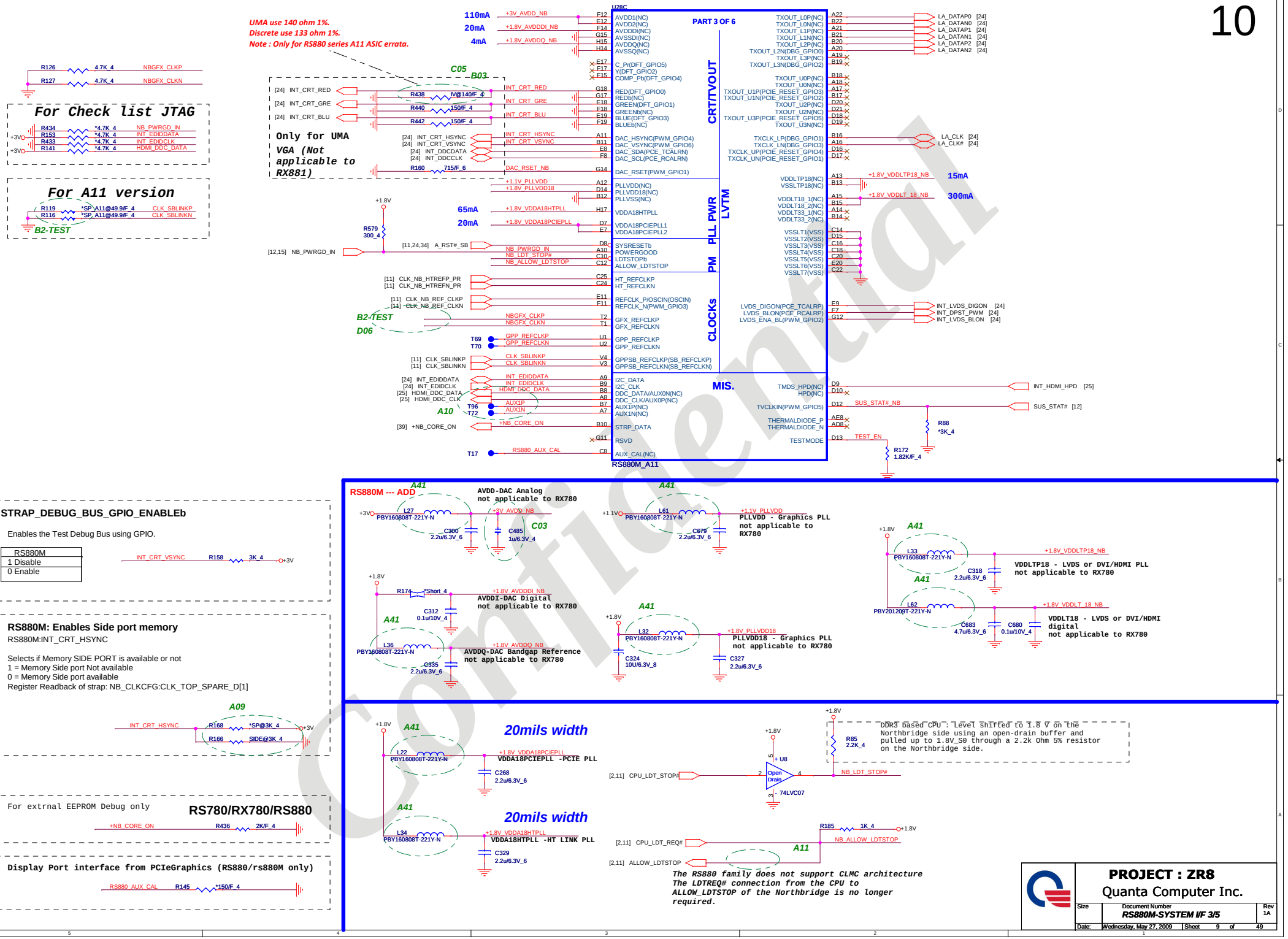

U28F

PART 6/6

GROUND

VSSAPCIE1 VSSAPCIE2 VSSAPCIE3 VSSAPCIE4 VSSAPCIE5 VSSAPCIE6 VSSAPCIE7 VSSAPCIE8 VSSAPCIE9 VSSAPCIE10 VSSAPCIE11 VSSAPCIE12 VSSAPCIE13 VSSAPCIE14 VSSAPCIE15 VSSAPCIE16 VSSAPCIE17 VSSAPCIE18 VSSAPCIE19 VSSAPCIE20 VSSAPCIE21 VSSAPCIE22 VSSAPCIE23 VSSAPCIE24 VSSAPCIE25 VSSAPCIE26 VSSAPCIE27 VSSAPCIE28 VSSAPCIE29 VSSAPCIE30 VSSAPCIE31 VSSAPCIE32 VSSAPCIE33 VSSAPCIE34 VSSAPCIE35 VSSAPCIE36 VSSAPCIE37 VSSAPCIE38 VSSAPCIE39 VSSAPCIE40

VSSAHT1 VSSAHT2 VSSAHT3 VSSAHT4 VSSAHT5 VSSAHT6 VSSAHT7 VSSAHT8 VSSAHT9 VSSAHT10 VSSAHT11 VSSAHT12 VSSAHT13 VSSAHT14 VSSAHT15 VSSAHT16 VSSAHT17 VSSAHT18 VSSAHT19 VSSAHT20 VSSAHT21 VSSAHT22 VSSAHT23 VSSAHT24 VSSAHT25 VSSAHT26 VSSAHT27

VSS1 VSS2 VSS3 VSS4 VSS5 VSS6 VSS7 VSS8 VSS9 VSS10

VSS11 VSS12 VSS13 VSS14 VSS15 VSS16 VSS17 VSS18 VSS19 VSS20 VSS21 VSS22 VSS23 VSS24 VSS25 VSS26 VSS27 VSS28 VSS29 VSS30 VSS31 VSS32 VSS33 VSS34

RX881/RS880 POWER DIFFERENCE TABLE

PIN NAME	RX881	RS880	PIN NAME	RX881	RS880
VDDHT	+1.1V	+1.1V	IOPLLVDD	+1.1V	+1.1V
VDDHTRX	+1.1V	+1.1V	AVDD	GND	+3.3V
VDDHTTX	+1.2V	+1.2V	AVDDDI	GND	+1.8V
VDDA18PCIE	+1.8V	+1.8V	AVDDQ	GND	+1.8V
VDDG18	+1.8V	+1.8V	PLLVDD	GND	+1.1V
VDD18_MEM	GND	+1.8V	PLLVDD18	GND	+1.8V
VDDPCIE	+1.1V	+1.1V	VDDA18PCIEPLL	+1.8V	+1.8V
VDDC	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V
VDD_MEM	GND	+1.8V/1.5V	VDDLTP18	GND	+1.8V
VDDG33	+3.3V	+3.3V	VDDLT18	GND	+1.8V
IOPLLVDD18	+1.8V	+1.8V	VDDLT33	NC	NC

+1.1V 2A for RS880M
+1.1V 1.3A for RX881

+1.1V

0.6A L31 *Short_8 +1.1V_VDDHT

C317 4.7u/6.3V_6 C321 0.1u/10V_4 C322 0.1u/10V_4 C323 0.1u/10V_4

0.7A L37 *Short_8 +1.1V_VDDHTRX

C362 4.7u/6.3V_6 C338 0.1u/10V_4 C340 0.1u/10V_4 C334 0.1u/10V_4

+1.1V 2A for RS880M
+1.2V 0.4A for Rx881

+1.1V L35 *Short_8 **2A** +1.1V_VDDHTTX

C333 4.7u/6.3V_6 C331 0.1u/10V_4 C337 0.1u/10V_4 C332 0.1u/10V_4 C341 0.1u/10V_4

B2 - TEST

+1.8V 1A for RS780M+SB700
+1.8V 1A for RX881

A41

+1.8V L24 PBY201209T-221Y-N **0.7A** +1.8V_VDDA18PCIE

C299 4.7u/6.3V_6 C297 4.7u/6.3V_6 C292 0.1u/10V_4 C295 0.1u/10V_4 C287 0.1u/10V_4 C301 0.1u/10V_4

U28E

PART 5/6

POWER

VDDHT_1 VDDHT_2 VDDHT_3 VDDHT_4 VDDHT_5 VDDHT_6 VDDHT_7 — J17 K16 L16 M16 P16 R16 T16

VDDHTRX_1 VDDHTRX_2 VDDHTRX_3 VDDHTRX_4 VDDHTRX_5 VDDHTRX_6 VDDHTRX_7 — H18 G19 F20 E21 D22 B23 A23

VDDHTTX_1 VDDHTTX_2 VDDHTTX_3 VDDHTTX_4 VDDHTTX_5 VDDHTTX_6 VDDHTTX_7 VDDHTTX_8 VDDHTTX_9 VDDHTTX_10 VDDHTTX_11 VDDHTTX_12 VDDHTTX_13 — AE25 AD24 AC23 AB22 AA21 Y20 W19 V18 U17 T17 R17 P17 M17

VDDA18PCIE_1 VDDA18PCIE_2 VDDA18PCIE_3 VDDA18PCIE_4 VDDA18PCIE_5 VDDA18PCIE_6 VDDA18PCIE_7 VDDA18PCIE_8 VDDA18PCIE_9 VDDA18PCIE_10 VDDA18PCIE_11 VDDA18PCIE_12 VDDA18PCIE_13 VDDA18PCIE_14 VDDA18PCIE_15 — J10 P10 K10 M10 L10 W9 H9 T10 R10 Y9 AA9 AB9 AD9 AE9 U10

VDDG18_1(VDD18_1) VDDG18_2(VDD18_2) VDD18_MEM1(NC) VDD18_MEM2(NC) — F9 G9 AE11 AD11

RS880M_A11

VDDPCIE_1 VDDPCIE_2 VDDPCIE_3 VDDPCIE_4 VDDPCIE_5 VDDPCIE_6 VDDPCIE_7 VDDPCIE_8 VDDPCIE_9 VDDPCIE_10 VDDPCIE_11 VDDPCIE_12 VDDPCIE_13 VDDPCIE_14 VDDPCIE_15 VDDPCIE_16 VDDPCIE_17 — A6 B6 C6 D6 E6 F6 G7 H8 J9 K9 M9 L9 P9 R9 T9 V9 U9

VDDC_1 VDDC_2 VDDC_3 VDDC_4 VDDC_5 VDDC_6 VDDC_7 VDDC_8 VDDC_9 VDDC_10 VDDC_11 VDDC_12 VDDC_13 VDDC_14 VDDC_15 VDDC_16 VDDC_17 VDDC_18 VDDC_19 VDDC_20 VDDC_21 VDDC_22 — K12 J14 U16 J11 K15 M12 L14 L11 M13 M15 N12 N14 P11 P13 P14 R12 R15 T11 T15 U12 T14 J16

VDD_MEM1(NC) VDD_MEM2(NC) VDD_MEM3(NC) VDD_MEM4(NC) VDD_MEM5(NC) VDD_MEM6(NC) — AE10 AA11 Y11 AD10 AB10 AC10

VDDG33_1(NC) VDDG33_2(NC) — H11 H12

+1.8V R136 *Short_6 **25mA** +1.8V_VDDG18_NB

VDD18-RS880 I/O Transform

C286 1U/10V_4

+1.8V R171 SIDE@0_6 **25mA** +1.8V_VDD18_MEM

A09

C835 SP@1U/10V_4

C835
W/O side port
-->stuff 0 Ohm
CS00002JB38

+1.1V_VDD_PCIE **2.5A** R115 *Short_8 +1.1V

VDDPCIE - PCIE-E Main power

C243 0.1u/10V_4 C291 0.1u/10V_4 C293 1U/10V_4 C294 1U/10V_4 C290 4.7u/6.3V_6

0.95~1.1V 10A

VDDC - Core Logic power

NB_CORE

C315 0.1u/10V_4 C311 0.1u/10V_4 C310 0.1u/10V_4 C307 0.1u/10V_4 C314 10U/6.3V_8

C316 0.1u/10V_4 C308 0.1u/10V_4 C306 0.1u/10V_4 C305 10U/6.3V_8

A09

C831
W/O side port
-->stuff 0 Ohm
CS00002JB38

+1.5V_VDD_MEM SIDE@0.1u/10V_4 C832 C833 C831 SIDE@0.1u/10V_4 C836 L74 SIDE@0_8 +1.5V

C834 SIDE@4.7u/6.3V_6

SIDE@0.1u/10V_4 SP@0.1u/10V_4

+3V_VDDG33 R169 *Short_4 +3V **60mA**

C302 0.1u/10V_4 C303 0.1u/10V_4

VDD33 - 3.3V I/O
Not applicable to RX780

VDD_MEM For UMA RS780 only
Not applicable to RX780
memory I/O transform

+1.1V
+1.8V
NB_CORE

+1.1V [2,7,8,9,14,38,44]
+1.8V [7,9,15,24,37,42,43,44]
NB_CORE [39,44]

PROJECT : ZR8
Quanta Computer Inc.

Size	Document Number	Rev
	RS880M-POWER5/5	1A
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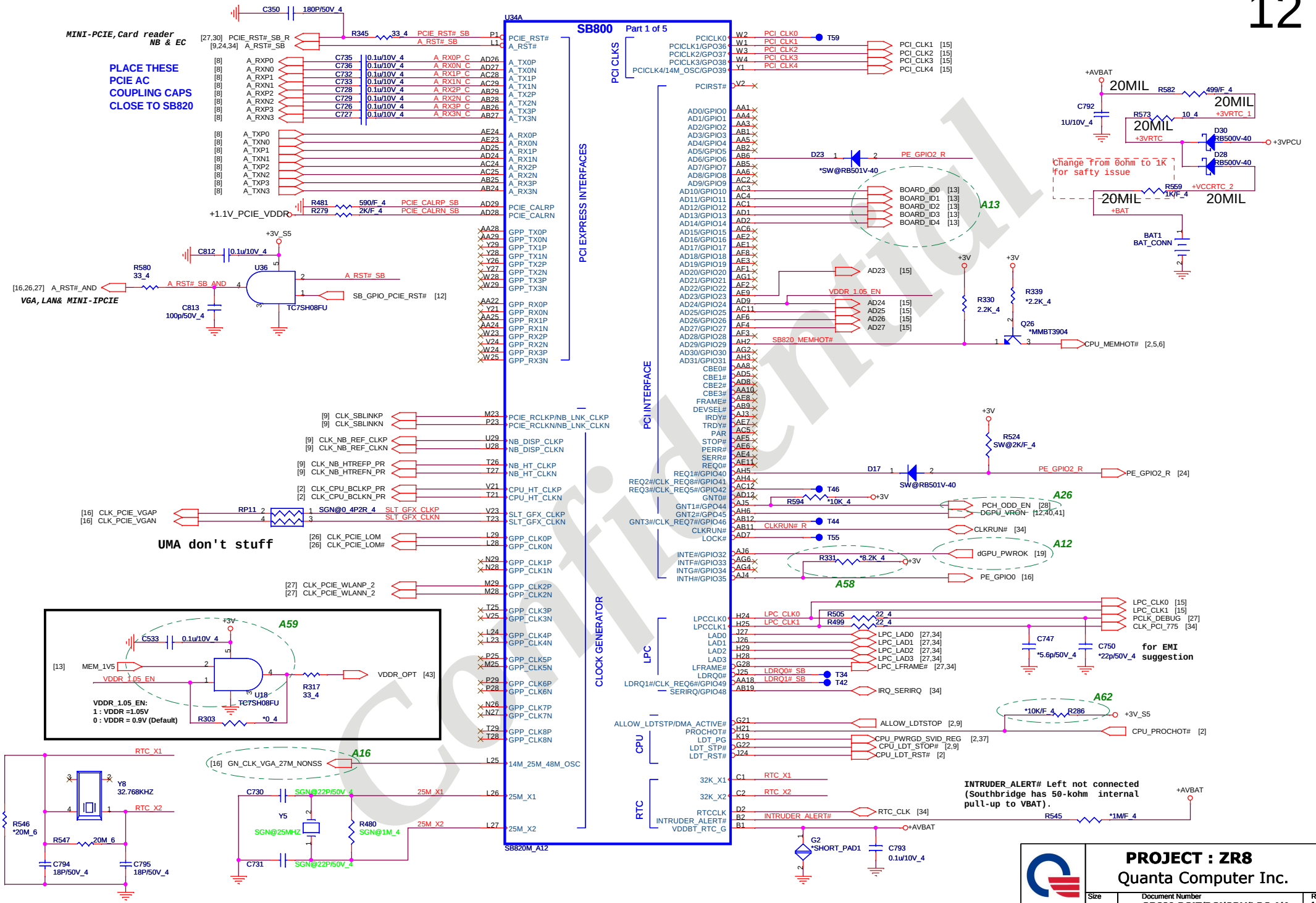

NC only ,Can't be install

+3V_S5 R352 *2.2K_4 SB_TEST0
R350 *2.2K_4 SB_TEST1
R347 *2.2K_4 SB_TEST2

+3V SCL0/SDATA0 is 3V tolerance
AMD datasheet define it
R288 2.2K_4 PCLK_SMB
R287 2.2K_4 PDAT_SMB
Clock gen/Robson/TV tuner /DDR2/DDR2 thermal/Accelerometer

+3V_S5 SCL1/SDATA1 is 3V/S5 tolerance
AMD datasheet define it
R348 10K_4 SB_SMBCLK1
R346 10K_4 SB_SMBDATA1

+3V_S5 SCL2/SDATA2 is 3V/S5 tolerance
AMD datasheet define it
R290 10K_4 SB_SCLK2
R283 10K_4 SB_SDATA2

+3V R338 4.7K_4 SUS_STAT#

B2-TEST
dGPU_VRON 2ms
MXM_PWR_EN
[19] MXM_PWREN
[11,40,41] DGPU_VRON
+3V R307 SW@4.7K_4
D19 SW@RB501V-40
MXM_PWR_EN 1 2
C538 SW@0.1u/10V_4
D18 *SW@RB501V-40
>1mS delay is required between all MXM power rail stable and MXM_PWREN(enables the module internal power)
A14

+3V A61
R474 8.2K_4 CLK_PCIE_LAN_REQ#
R486 8.2K_4 CLK_PCIE_2_REQ#

ACZ_SDOUT R570 33_4 ACZ_SDOUT_AUDIO [29]
C815 *10P/50V_4
ACZ_SYNC R552 33_4 ACZ_SYNC_AUDIO [29]
C800 *10P/50V_4
ACZ_BCLK R569 33_4 ACZ_BITCLK_AUDIO [29]
C814 *10P/50V_4
ACZ_RST# R554 33_4 ACZ_RST#_AUDIO [29]
ACZ_SDIN0 ACZ_SDIN0 [29]
If the VDDIO_AZ_S power rail is configured for 1.5V_S5 then AZ_SDIN[3:0] can not be connected to 3.3-V devices.

[11,13,14,15,24,26,31,32,36,44] +3V_S5 +3V_S5
[2,4,5,6,9,10,11,13,14,15,19,24,25,27,29,30,32,33,34,36,37,38,39,41,42,43,44,46] +3V +3V

USBCLK/41M_25M_48M_OSC pin is CLK input pin when EXT CLKGEN mode.
It is output CLK source when INT CLKGEN mode.

U34D
SB800 Part 4 of 5
SB820M_A12

PCI_PME#/GEVENT4# J2
RI#/GEVENT22# K1
SPI_CS3#/GBE_STAT1/GEVENT21# D3
SLP_S3# F1
SLP_S5# H1
PWR_BTN# F2
PWR_GOOD H5
SUS_STAT# G6
TEST0 B3
TEST1/TMS C4
TEST2 F6
GA20IN/GEVENT0# AD21
KBRST#/GEVENT1# AE21
LPC_PME#/GEVENT3# K2
LPC_SMI#/GEVENT23# J29
GEVENT5# H2
SYS_RESET#/GEVENT19# J1
WAKE#/GEVENT8# H6
IR_RX1/GEVENT20# E3
THRMTRIP#/SMBALERT#/GEVENT2# J6
NB_PWRGD AC19
RSMRST# G1
ACPI / WAKE UP EVENTS
USB 1.1 USB MISC

[34] SUSB# [34] SUSC# [34] DNBSWON# [15] SB_PWRGD_IN [9] SUS_STAT#
SB_TEST0 SB_TEST1 SB_TEST2
[34] SIO_A20GATE [34] SIO_RCIN#
T94 LANLINK_STATE#
[34] SIO_EXT_SMI# [34] SIO_EXT_SCI#
T95 SYS_RST#
[26] PCIE_WAKE#
T58 IR_RX1
[2] CPU_THERMTRIP# [9,15] NB_PWRGD_IN
[34] ICH_RSMRST#
PCIE_WAKE#
SB_THERMTRIP#

CLK_REQ4#/SATA_IS0#/GPIO64 AD19
CLK_REQ3#/SATA_IS1#/GPIO63 AA16
SMARTVOLT1/SATA_IS2#/GPIO50 AB21
CLK_REQ0#/SATA_IS3#/GPIO60 AC18
SATA_IS4#/FANOUT3/GPIO55 AE20
SATA_IS5#/FANIN3/GPIO59 AE19
SPKR/GPIO66 AE19
SCL0/GPIO43 AD22
SDA0/GPIO47 AE22
SCL1/GPIO227 E5
SDA1/GPIO228 F4
CLK_REQ2#/FANIN4/GPIO62 AH21
CLK_REQ1#/FANOUT4/GPIO61 AB18
IR_LED#/LLB#/GPIO184 E1
SMARTVOLT2/SHUTDOWN#/GPIO51 AJ21
DDR3_RST#/GEVENT7# H4
GBE_LED0/GPIO183 D5
GBE_LED1/GEVENT9# D7
GBE_LED2/GEVENT10# G5
GBE_STAT0/GEVENT11# K3
CLK_REQG#/GPIO65/OSCIN AA20
GPIO
USB 2.0

[11] SB_GPIO_PCIE_RST# [26] CLK_PCIE_LAN_REQ#
MXM_PWR_EN
T37 SB_GPIO59
[29] SPKR [5,6,26,27,46] PCLK_SMB [5,6,26,27,46] PDAT_SMB
PCLK_SMB
PDAT_SMB
SB_SMBCLK1
SB_SMBDATA1
[27] CLK_PCIE_2_REQ# [17] VGA_REQ#
R306 *0_4 VGA_REQ#_GPIO61
C04
[7] SP_DDR3_RST#
T41

BLINK/USB_OC7#/GEVENT18# H3
USB_OC6#/IR_TX1/GEVENT6# D1
USB_OC5#/IR_TX0/GEVENT17# E4
USB_OC4#/IR_RX0/GEVENT16# D4
USB_OC3#/AC_PRESTDO/GEVENT15# E8
USB_OC2#/TCK/GEVENT14# E7
USB_OC1#/TDI/GEVENT13# E7
USB_OC0#/TRST#/GEVENT12# F8
USB OC

[31] OC_7# [31] OC_6# [2,4,33] PM_THERM# [31] OC_4#
R149 *Short_4
SB_JTAG_TDO
SB_JTAG_TCK
SB_JTAG_TDI
SB_JTAG_RST#

HD audio interface is +3VS5 voltage

[15] ACZ_SDOUT
R555 *10K/F_4 ACZ_BCLK
R337 *10K/F_4 ACZ_SDOUT
R336 *10K/F_4 ACZ_SDIN0
R571 *10K/F_4 ACZ_SDIN1
R327 *10K/F_4 ACZ_SDIN2
ACZ_SDIN3
ACZ_SYNC
ACZ_RST#

AZ_BITCLK M3
AZ_SDOUT N1
AZ_SDIN0/GPIO167 L2
AZ_SDIN1/GPIO168 M2
AZ_SDIN2/GPIO169 M1
AZ_SDIN3/GPIO170 M4
AZ_SYNC N2
AZ_RST# P2
HD AUDIO

+3V_S5
R553 10K_4 GBE_COL
R322 10K_4 GBE_CRS
R558 10K_4 GBE_MDIO
D03
R343 10K_4 GBE_RXERR
R344 10K_4 GBE_PHY_INTR

GBE_COL T1
GBE_CRS T4
GBE_MDCK L6
GBE_MDIO L5
GBE_RXCLK T9
GBE_RXD3 U1
GBE_RXD2 U3
GBE_RXD1 T2
GBE_RXD0 U2
GBE_RXCTL/RXDV T5
GBE_RXERR V5
GBE_TXCLK P5
GBE_TXD3 M5
GBE_TXD2 P9
GBE_TXD1 T7
GBE_TXD0 P7
GBE_TXCTL/TXEN M7
GBE_PHY_PD P4
GBE_PHY_RST# M9
GBE_PHY_INTR V7
GBE LAN

T35 ADP_PRES0
PS2_DAT/SDA4/GPIO187 E23
PS2_CLK/SCL4/GPIO188 E24
SPI_CS2#/GBE_STAT2/GPIO166 F21
FC_RST#/GPO160 G29
PS2KB_DAT/GPIO189 D27
PS2KB_CLK/GPIO190 F28
PS2M_DAT/GPIO191 F29
PS2M_CLK/GPIO192 E27
EMBEDDED CTRL

B2-TEST
CN24
+3V_S5
SB_JTAG_TCK
SB_JTAG_TDO
SB_JTAG_TDI
SB_TEST1
SB_JTAG_RST#
*S/W_JTAG_DEBUG
SB JTAG
DEL C816

USBCLK/14M_25M_48M_OSC A10 T106
USB_RCOMP G19 USB_RCOMP_SB R293 11.8K/F_6

USB_FSD1P/GPIO186 J10
USB_FSD1N H11
USB_FSD0P/GPIO185 H9 USB_FSD12P T47
USB_FSD0N J8 USB_FSD12N T49

USB_HSD13P B12 USBP13+ [31]
USB_HSD13N A12 USBP13- [31] USB board
USB_HSD12P F11 USBP12+ [31]
USB_HSD12N E11 USBP12- [31] USB board
USB_HSD11P E14
USB_HSD11N E12
USB_HSD10P J12 USBP10+ [30]
USB_HSD10N J14 USBP10- [30] USB card reader
USB_HSD9P A13 USBP9+ [31]
USB_HSD9N B13 USBP9- [31] BLUETOOTH
USB_HSD8P D13 USBP8+ [31]
USB_HSD8N C13 USBP8- [31] USB board
USB_HSD7P G12 USBP7+ [27]
USB_HSD7N G14 USBP7- [27] WLAN MINI CARD
USB_HSD6P G16 T61
USB_HSD6N G18 T105
USB_HSD5P D16
USB_HSD5N C16
USB_HSD4P B14
USB_HSD4N A14
USB_HSD3P E18
USB_HSD3N E16
USB_HSD2P J16
USB_HSD2N J18
USB_HSD1P B17 USBP1+ [24]
USB_HSD1N A17 USBP1- [24] USB CAMERA
USB_HSD0P A16 USBP0+ [31]
USB_HSD0N B16 USBP0- [31] On board USB connect
B2-TEST

SCL2/GPIO193 D25 SB_SCLK2
SDA2/GPIO194 E23 SB_SDATA2
SCL3_LV/GPIO195 B26 SB_GPIO195
SDA3_LV/GPIO196 E26 SB_GPIO196
EC_PWM0/EC_TIMER0/GPIO197 F25
EC_PWM1/EC_TIMER1/GPIO198 E22
EC_PWM2/EC_TIMER2/GPIO199 F22 GPIO199 [15]
EC_PWM3/EC_TIMER3/GPIO200 E21 GPIO200 [15]

KSI_0/GPIO201 G24
KSI_1/GPIO202 G25
KSI_2/GPIO203 E28
KSI_3/GPIO204 E29
KSI_4/GPIO205 D29
KSI_5/GPIO206 D28
KSI_6/GPIO207 C29
KSI_7/GPIO208 C28
KSO_0/GPIO209 B28
KSO_1/GPIO210 A27
KSO_2/GPIO211 B27
KSO_3/GPIO212 D26
KSO_4/GPIO213 A26
KSO_5/GPIO214 C26
KSO_6/GPIO215 A24
KSO_7/GPIO216 B25
KSO_8/GPIO217 A25
KSO_9/GPIO218 D24
KSO_10/GPIO219 B24
KSO_11/GPIO220 C24
KSO_12/GPIO221 B23
KSO_13/GPIO222 A23
KSO_14/GPIO223 D22
KSO_15/GPIO224 C22
KSO_16/GPIO225 A22
KSO_17/GPIO226 B22
EMBEDDED CTRL

SB_GPIO195 R489 10K_4
SB_GPIO196 R275 10K_4

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Quanta Computer Inc.
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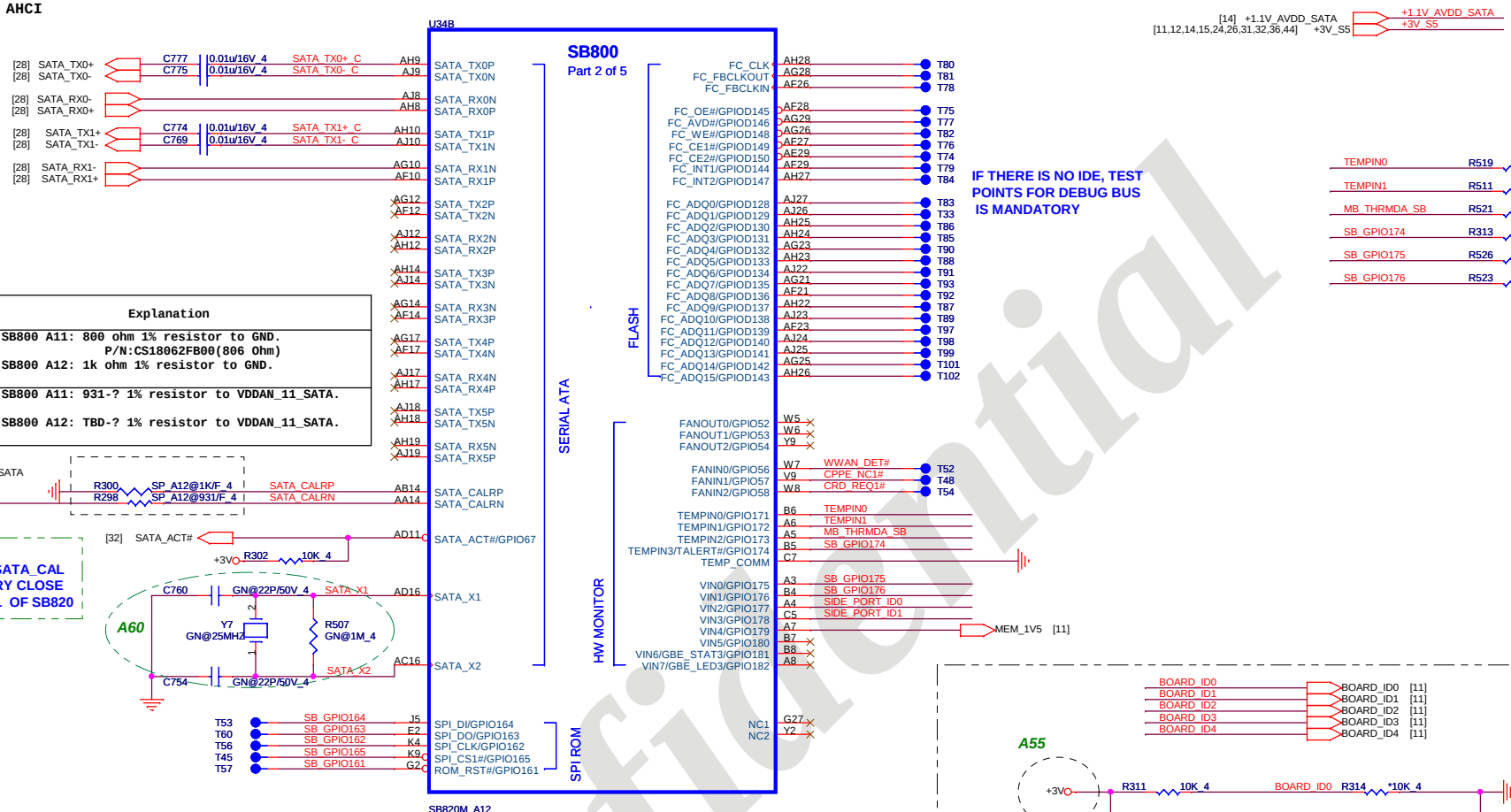
SATA PORT 0,1,2,3
can support AHCI
mode

SATA1

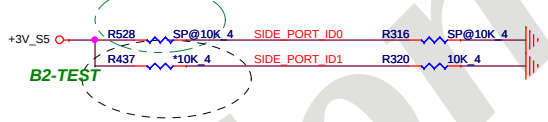
SATA ODD



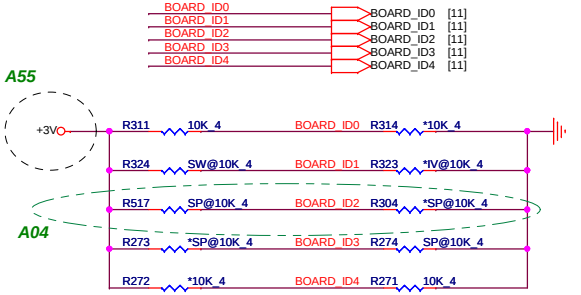
IF THERE IS NO IDE, TEST POINTS FOR DEBUG BUS IS MANDATORY

Signal Name	Explanation
SATA_CALRP	SB800 A11: 800 ohm 1% resistor to GND. P/N:CS18062FB00(806 Ohm) SB800 A12: 1k ohm 1% resistor to GND.
SATA_CALRN	SB800 A11: 931-? 1% resistor to VDDAN_11_SATA. SB800 A12: TBD-? 1% resistor to VDDAN_11_SATA.

PLACE SATA_CAL RES VERY CLOSE TO BALL OF SB820



	ID1	ID0
HYX	0	0
SAM	0	1
ATI	1	0



DDR3 Sideport Memory Device

Vendor	Vendor P/N	STN B/S P/N	Size	BOARD_ID2 GPIO12	SIDE_PORT_ID1 GPIO178	SIDE_PORT_ID0 GPIO177
Hynix	H5TQ1G63BFR-12C	AKD5LZGTW04 (64M*16)	1GB	0 (WO/Sideport)	0	0
Samsung	K4W1G1646E-HC12	AKD5LGGT506 (64M*16)	1GB	1 (W/Sideport)	0	1

Board ID

	BOARD_ID4 GPIO14	BOARD_ID3 GPIO13	BOARD_ID2 GPIO12	BOARD_ID1 GPIO11	BOARD_ID0 GPIO10
0	N/A (Default)	JV51-DN (3-DIMM) (Default)	WO/Sideport	UMA	14"
1	N/A	JM51-DN (2-DIMM)	W/Sideport (Default)	Discrete (Default)	15.6" (Default)

PROJECT : ZR8
Quanta Computer Inc.

Size	Document Number	Rev
	SATA/IDE/HWM/SPI 3/4	1A
Date: Wednesday, May 27, 2009	Sheet 13 of 49	

PLACE ALL THE DECOUPLING CAPS ON
THIS SHEET CLOSE TO SB AS POSSIBLE.

VDDQ--3.3V I/O power

VDD-- S/B CORE power

U34C

SB800

Part 3 of 5

POWER

SB820M_A12

SB820 without GBE: Connected to GND plane.

U34E

SB800

GROUND

Part 5 of 5

SB820M_A12

If the VDDIO_AZ_S power rail is configured for 1.5V_S5 then AZ_SDIN[3:0] can not be connected to 3.3-V devices.

For support USB wakeup-->3V_S5

[2,4,5,6,9,10,11,12,13,15,19,24,25,27,29,30,32,33,34,36,37,38,39,41,42,43,44,46] +3V
[2,7,8,9,10,38,44] +1.1V
[11,12,13,15,24,26,31,32,36,44] +3V_S5
[38] +1.1V_S5

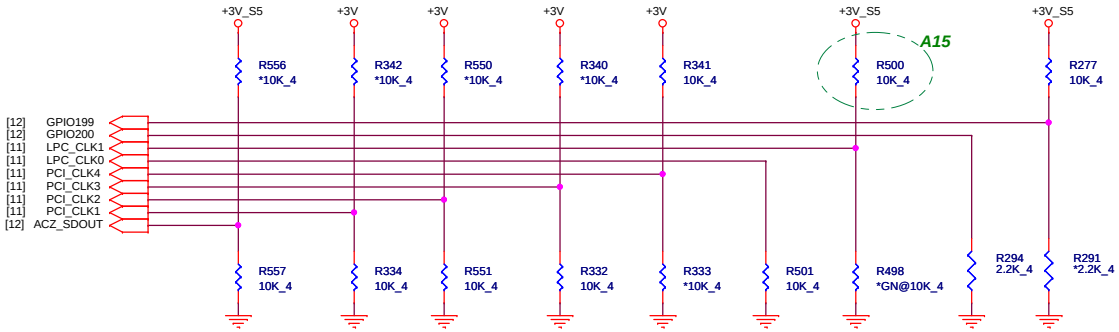
PROJECT :	ZR8
Quanta Computer Inc.	
Size	Document Number: SB820-PWR/DECOUPLING 4/4 — Rev: 1A
Date: Wednesday, May 27, 2009	Sheet 14 of 49

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

REQUIRED STRAPS

SB820M is supported Gen1 mode only.

For internal clock GEN.

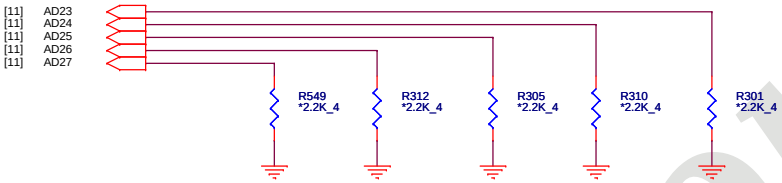


	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200 GPIO199
D02 PULL HIGH	This is required as the low power mode is not supported on the SB8xx	ALLOW PCIE Gen2	Watchdog Timer Enable	USE DEBUG STRAPS	non_Fusion CLOCK MODE DEFAULT	EC ENABLED	INT. CLKGEN ENABLED DEFAULT	H, H=Reserved H, L=SPI ROM
PULL LOW	PERFORMANCE MODE DEFAULT	FORCE PCIE Gen1 DEFAULT	Watchdog Timer Disable DEFAULT	IGNORE DEBUG STRAPS DEFAULT	Fusion CLOCK MODE	EC DISABLED DEFAULT	EXT. CLKGEN ENABLE	L,H=LPC ROM DEFAULT L, L=FWH ROM

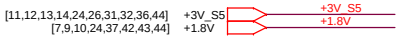
internal have pull Hi 10K

DEBUG STRAPS

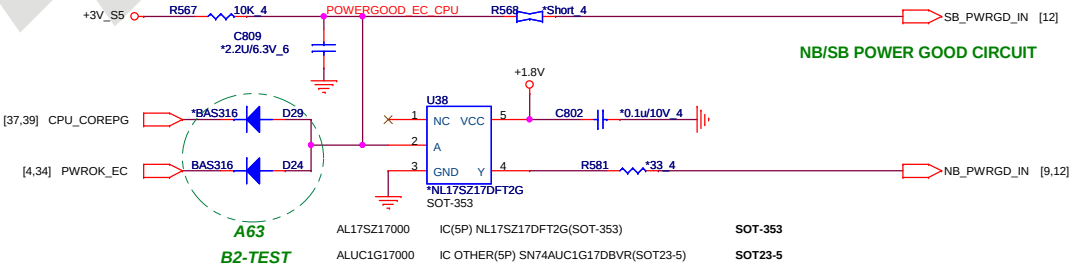
SB800 HAS 15K INTERNAL PU FOR PCI_AD[27:23]



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	DISABLE I2C ROM DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	ENABLE I2C ROM use REQ3# as SDA use GNT3# as SCL	ENABLE PCI MEM BOOT



NB_PWRGD_IN:
RS880/RX881 = 1.8V;
Do NOT share it with SB_PWRGD when use Internal Clk Gen (Need SB PLL initialize firstly)



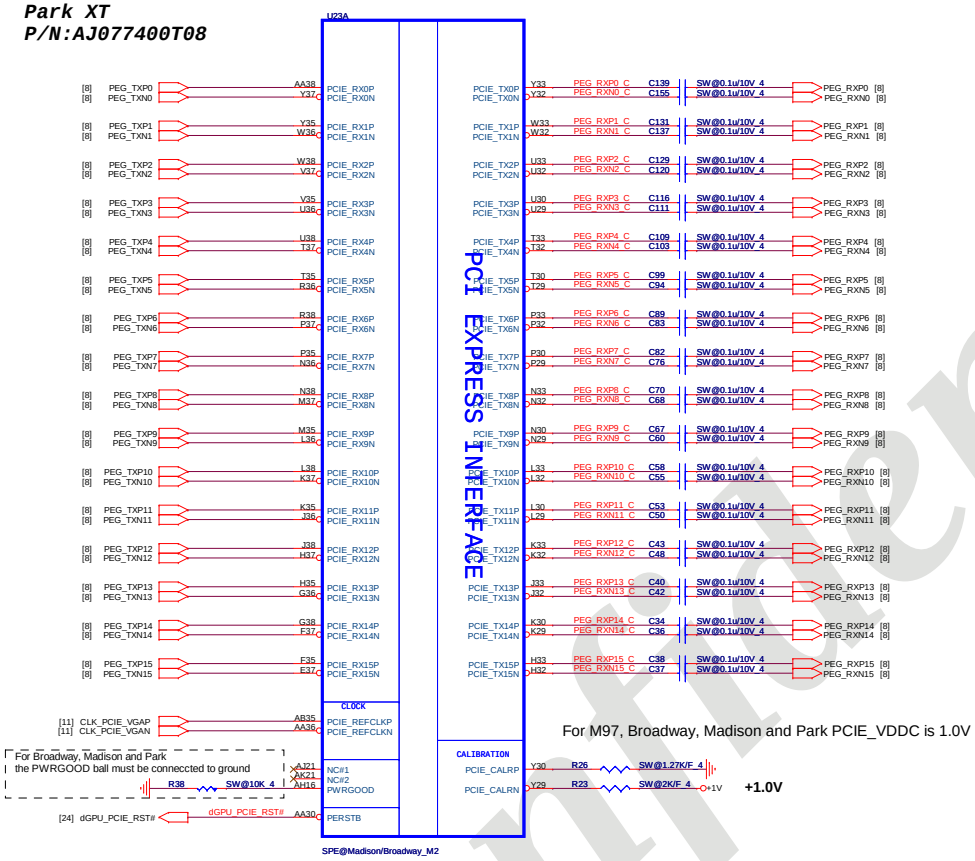
A63 B2-TEST

AL17SZ17000	IC(5P) NL17SZ17DFT2G(SOT-353)	SOT-353
ALUC1G17000	IC OTHER(5P) SN74AUC1G17DBVR(SOT23-5)	SOT23-5

PROJECT : ZR8
Quanta Computer Inc.

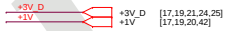
Size	Document Number	Rev
	SB820-STRAPS	1A
Date: Wednesday, May 27, 2009	Sheet 15 of 49	

Park XT
P/N:AJ077400T08

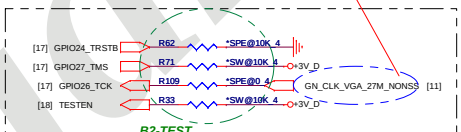


For M97, Broadway, Madison and Park PCIE_VDDC is 1.0V

+1.0V



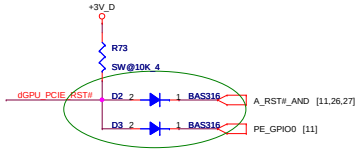
Add extra OSC for use SB clock.



B2-TEST

JTAG SIGNAL STUFF OPTION FOR OPTION2

SIGNALS	NORMAL MODE	JTAG MODE (DEBUG)
GPIO24_TRSTB	"0" (PD)	"1" (PU)
GPIO27_TMS	"1" (PU)	"1" (PU)
GPIO26_TCK	CLK	"1" (PU)
TESTEN	"1" (PU)	"1" (PU)



B2-TEST
FORM RB501 CHANGE TO BAS316

PROJECT : ZR8	
Quanta Computer Inc.	
Size	Document Number: Madison/Broadway-PCIE I/F — Rev 1A
Date: Wednesday, May 27, 2009	Sheet 16 of 49

GPU Power-on sequence

1 => +3V_D
2 => +VGPU_CORE
3 => +VGPU_IO
4 => +1V
5 => +1.5V_GPU
6 => +1.8V_GPU
7 => dGPU_PWROK

A17

1.8V GPIO

For Park-M2 NC pin

For Park-M2 NC pin
DVPDATA_17 ~ DVPDATA_23

For Park-M2 is NC pin

DP Channel D is NC on PARK

DDCXX_AUX4X is NC on PARK

DDCXX_AUX7X is NC on PARK and M9X

For dual link panel

For Singal link panel

HDMI

LVDS

CRT

U23B

SPE@Madison/Broadway_M2

U23G

SPE@Madison/Broadway_M2

JTAG DEBUG PORT

(1.8V@70mA AVDD)

(1.8V@100mA VDD1DI)

(1.8V@2mA A2VDDQ)

+1.8V(75mA)

+1.0V(125mA)

+1.8V(5mA)

(3.3V@130mA A2VDD)

PROJECT : ZR8	
Quanta Computer Inc.	
Size	Document Number: Madison/Broadway-HOST I/F
Rev	1A
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	For PARK	For Madison
MEM_CALRNP0		stuff
MEM_CALRNP1	stuff	
MEM_CALRNP2		stuff

DDR3/GDDR3 Memory Stuff Option

	GDDR5	GDDR3	DDR3(Default)
+1.5V_VGA	1.5V	1.8V/1.5V	1.5V
Ra	40.2R	40.2R	40.2R
Rb	100R	100R	100R

For SSTL-1.8/SSTL-2/DDR1/GDDR1: 0.5 * VDDR1.
For DDR3/GDDR3/GDDR4/GDDR5: 0.7 * VDDR1.

Broadway no daul rank support for GDDR5

Designator	For M97-M2	For Mannhatton
Rc	10K	10K
Rd	0R/Short	51R
Re	DNI	DNI
Ca	2.2nF	68pF

This basic topology should be used for DRAM_RST for DDR3/GDDR3/GDDR5.These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.

PROJECT : ZR8
Quanta Computer Inc.
Size | Document Number: Madison/Broadway-MEM I/F | Rev 1A
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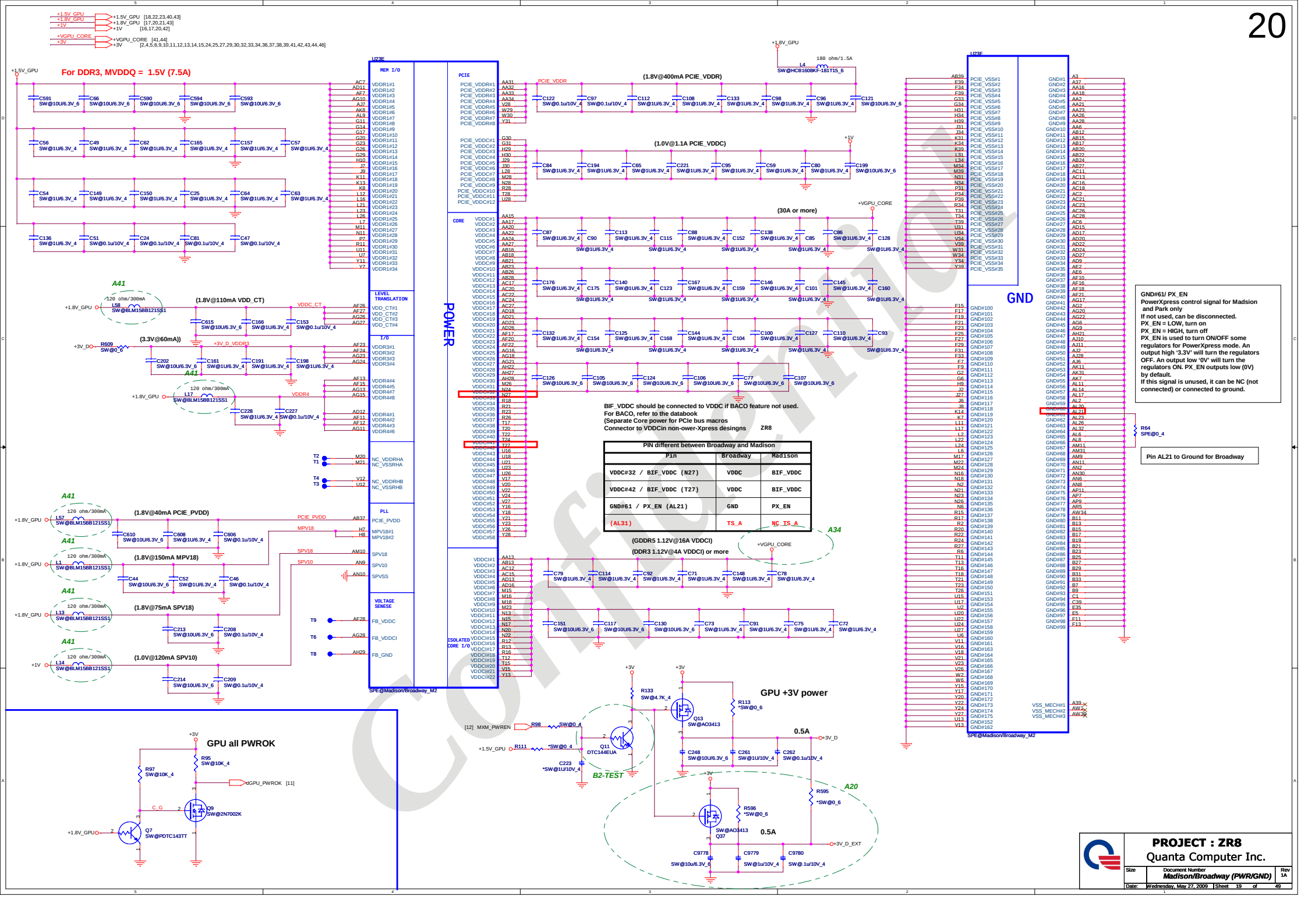

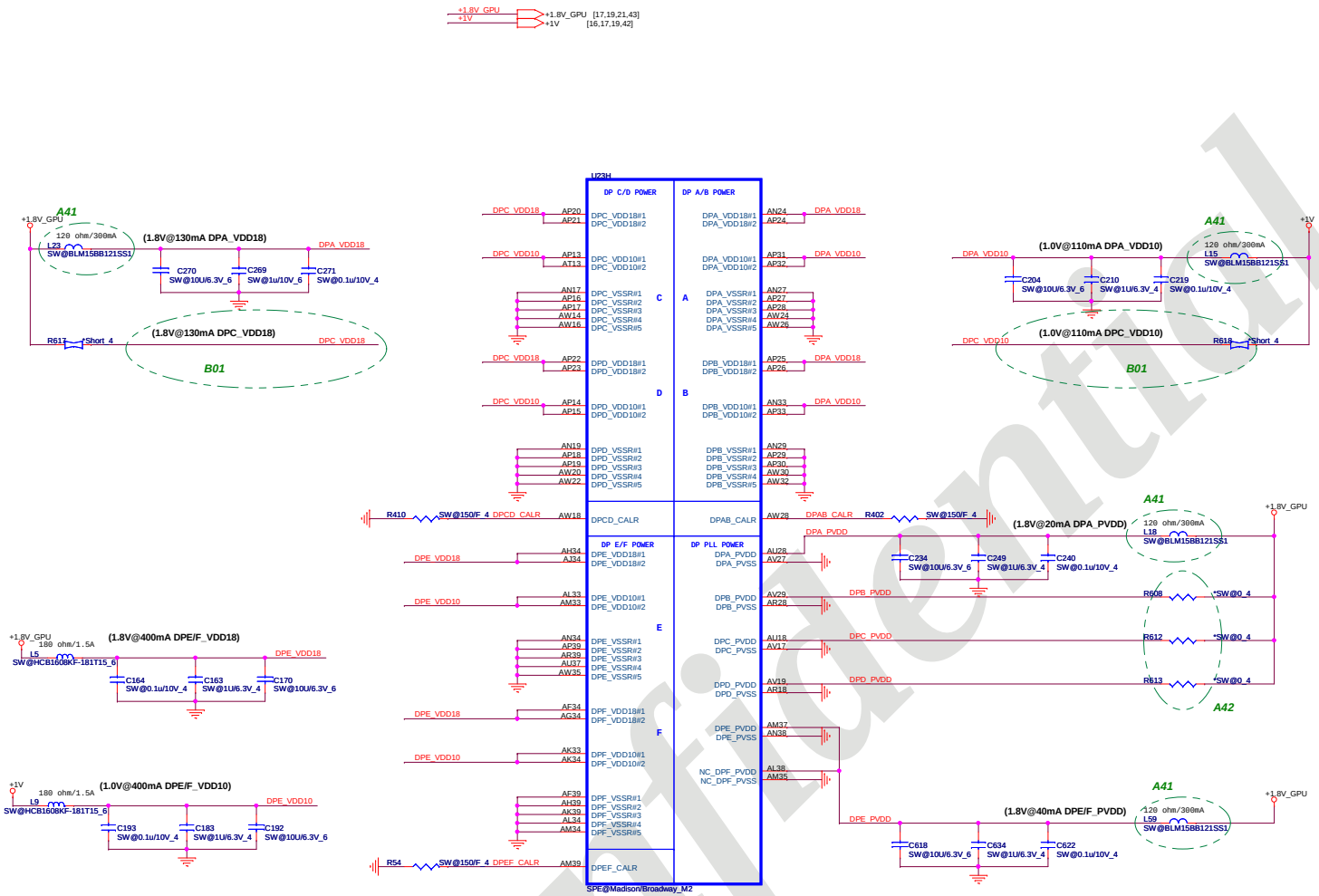

PROJECT : ZR8		
Quanta Computer Inc.		
Size	Document Number: Madison/Broadway (DP_PWR/GND)	Rev: 1A
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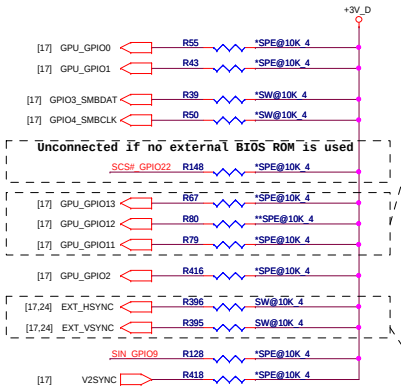
PIN STRAPS



Memory Aperture size	
GPIO[13:11]	Size
000	128MB
001	256MB
010	64MB
011	32MB

Function Table		
EXT_HSYNC	EXT_VSYNC	Discription
0	0	No Audio
0	1	Any one by dectec
1	0	DP only
1	1	Both DP & HDMI

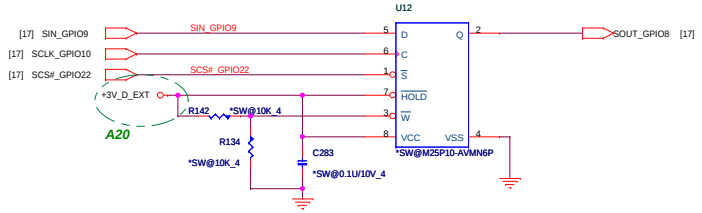
CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

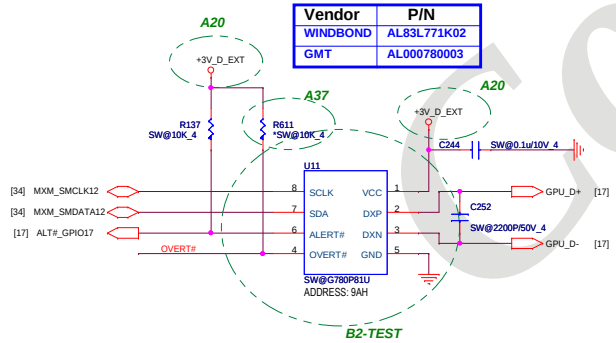
ZR8

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	DEFAULT	REMARK
TX_PWRS_ENB	GPIO0	0 = 50% TX OUTPUT SWING 1 = FULL TX OUTPUT SWING	0	
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0 = TX DE-EMPHASIS DISABLED 1 = TX DE-EMPHASIS ENABLED	0	
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM 0 = DISABLE 1 = ENABLE	0	
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT NUMONYX M25P10A : 101	000	See ROM table
BIF_GEN2_EN_A	GPIO2	0 = PCIE DEVICE AS 2.5GT/S CAPABLE 1 = PCIE DEVICE AS 5GT/S CAPABLE	0	(Recommended setting as 5.0 GT/s capability will be controlled by software.)
GPIO_8_ROMSO H2SYNC GPIO_21_BB_EN	GPIO8 H2SYNC GPIO21	Reserved Only	0	
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1:0] 00: NO AUDIO FUNCTION. 01: AUDIO FOR DISPLAYPORT AND HDMI IF ADAPTER IS DETECTED. 10: AUDIO FOR DISPLAYPORT ONLY. 11: AUDIO FOR BOTH DISPLAYPORT AND HDMI.	11	See Audio table
GPIO_9_ROMSI	GPIO9	0 = VGA controller capacity enable 1 = VGA controller capacity disenable (The device will not be recognized as the system's VGA controller.)	0	
VIP_DEVICE_STRAP_ENA	V2SYNC	0 = DRIVER would ignore the value sample on VHAD_0 during RESET. 1 = DRIVER would use the value sample on VHAD_0 during RESET.	0	

SERIAL ROM



Thermal Sensor



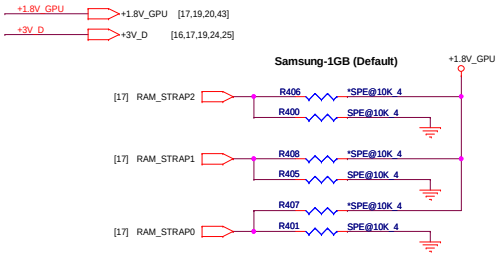
Vendor	P/N
WINDBOND	AL83L771K02
GMT	AL000780003

DDR3 Memory Aperture size

DDR3 Memory Aperture size

Vendor	Vendor P/N	STN B/S P/N	GPU	RAM_STRAP2 DVPDATA_2	RAM_STRAP1 DVPDATA_1	RAM_STRAP0 DVPDATA_0
Hynix			Park	1	1	0
	H5TQ1G63BFR-12C	AKD5LZGTW04 (64M*16)	Madison	1	0	0
			2Gb	1	1	1
Samsung			Park	0	1	0
	K4W1G1646E-HC12	AKD5LGGT506 (64M*16)	Madison	0	0	0
	K4W2G1646B-HC12	AKD5MGGT500	2Gb	0	0	1
AMD			Park	0	1	1
	23EY2387MA12-SZ	AKD5LGGT700	Madison	1	0	1

C14
D10



RAM_STRAP2 SET DDR3 Vendor
RAM_STRAP[1:0] SET SIZE.

PROJECT : ZR8
Quanta Computer Inc.

Size	Document Number	Rev
	Strip/Thermal	1A
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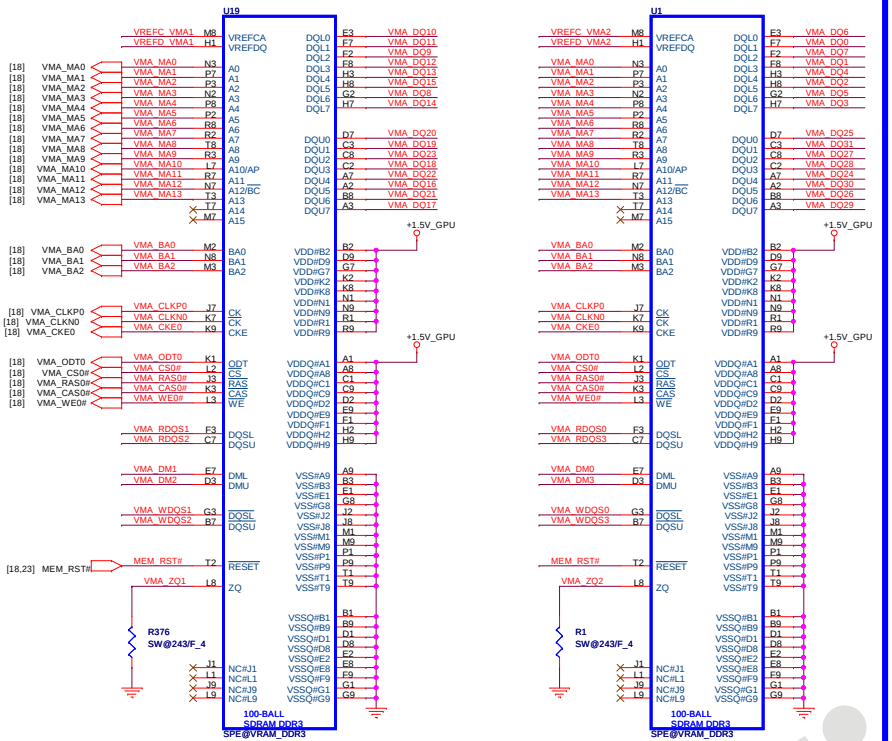
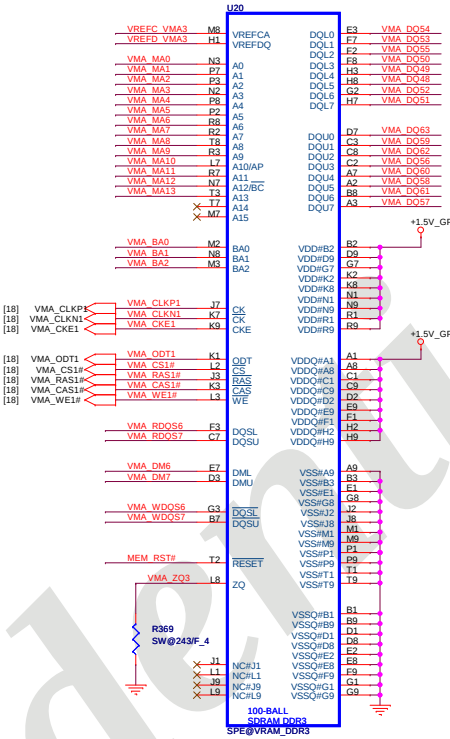
CHANNEL A: 512MB DDR3 (64M*16*4pcs)

[18] VMA_DQ[63..0] — VMA_DQ[63..0]
[18] VMA_DM[7..0] — VMA_DM[7..0]
[18] VMA_RDQS[7..0] — VMA_RDQS[7..0] QSA[7..0]
[18] VMA_WDQS[7..0] — VMA_WDQS[7..0] QSA#[7..0]

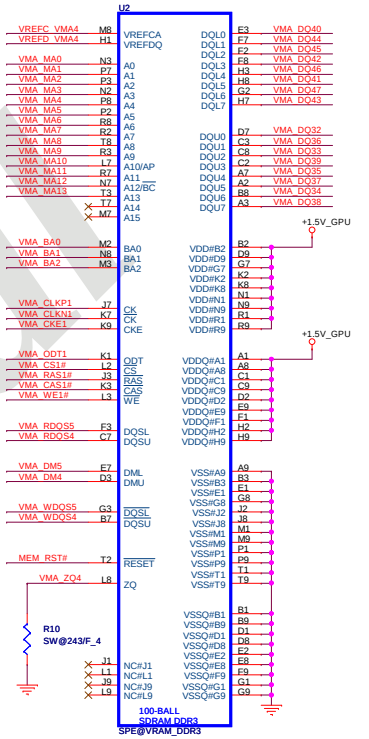


TOP Left

BOT Left

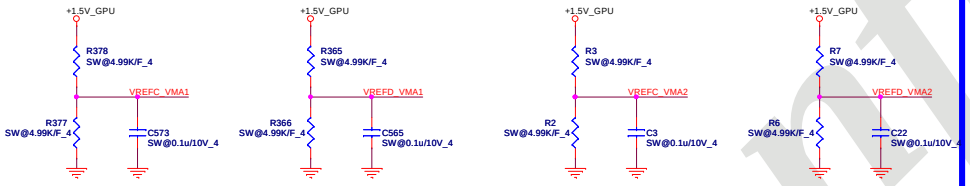


BOT Right

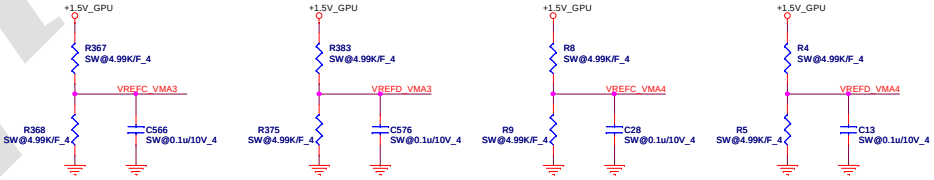


TOP Right

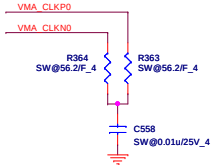
Group-A0 VREF



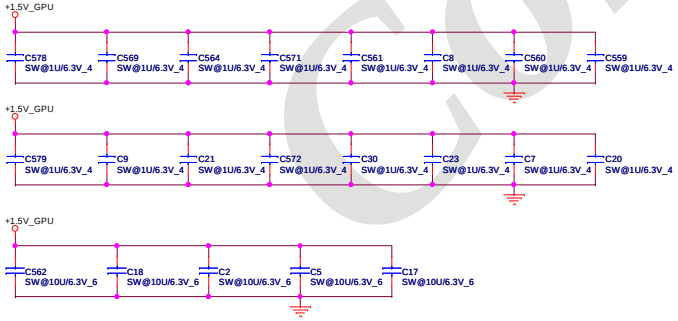
Group-A1 VREF



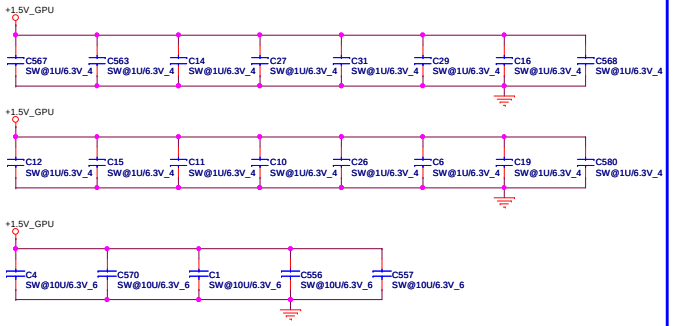
MEM_A0 CLK



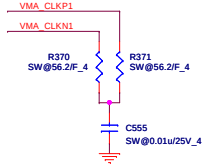
Group-A0 decoupling CAP



Group-A1 decoupling CAP



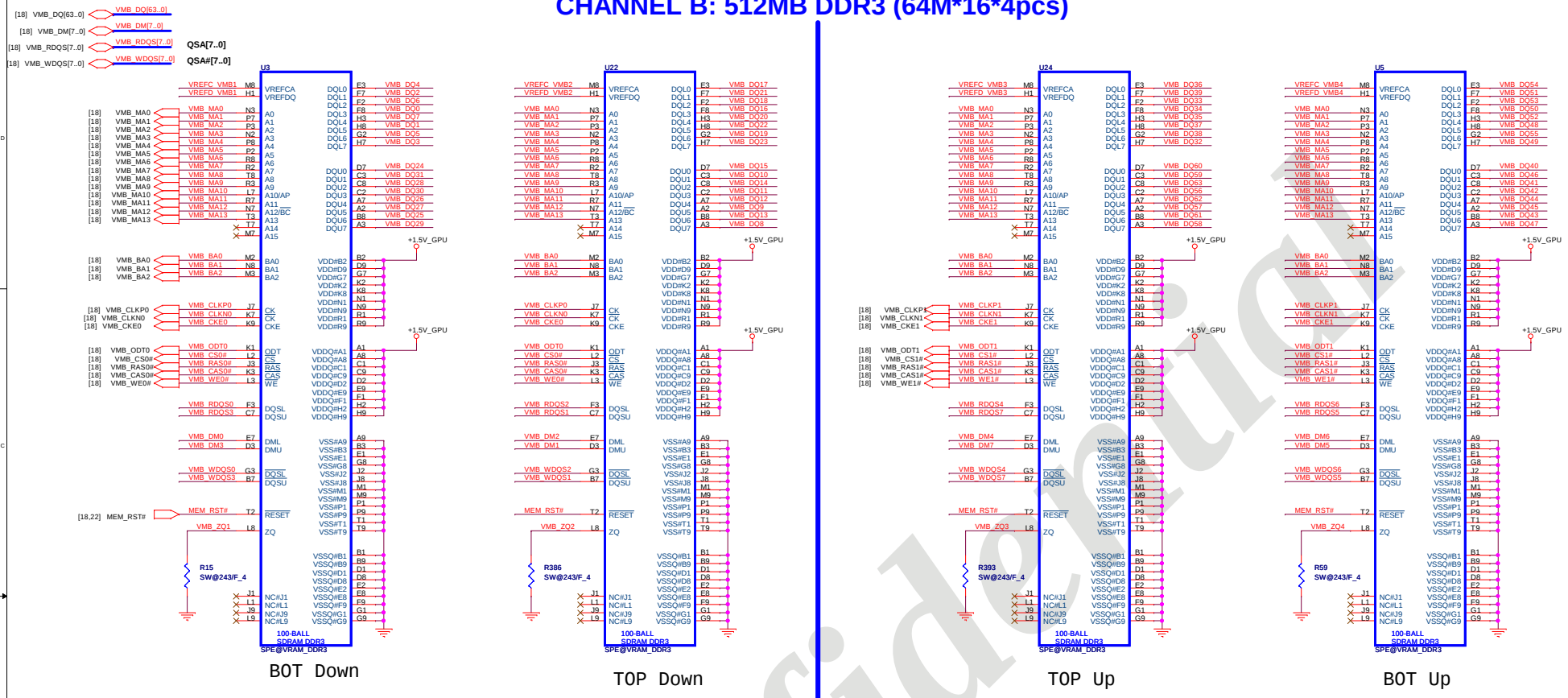
MEM_A1 CLK

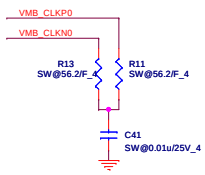


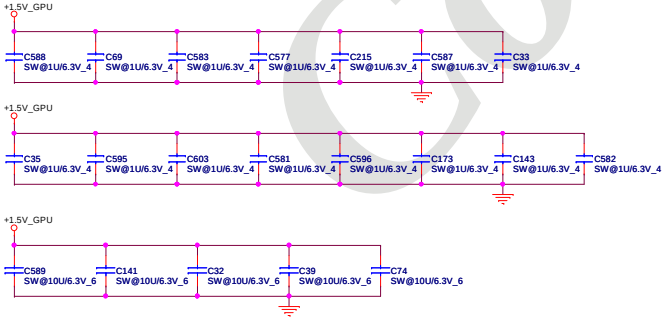
PROJECT : ZR8
Quanta Computer Inc.

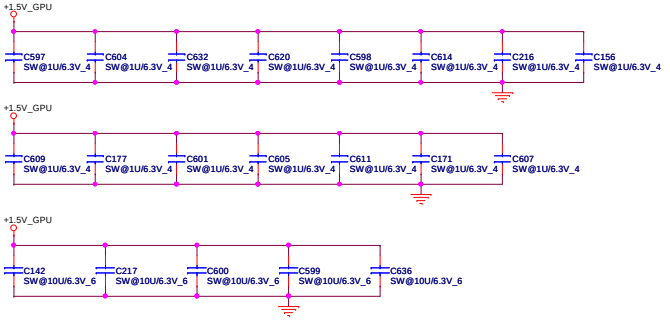
Size	Document Number	Rev
	MEMORY 1 channel A	1A
Date: Wednesday, May 27, 2009	Sheet 22 of 49	

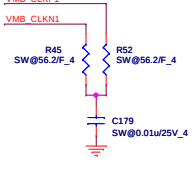
CHANNEL B: 512MB DDR3 (64M*16*4pcs)







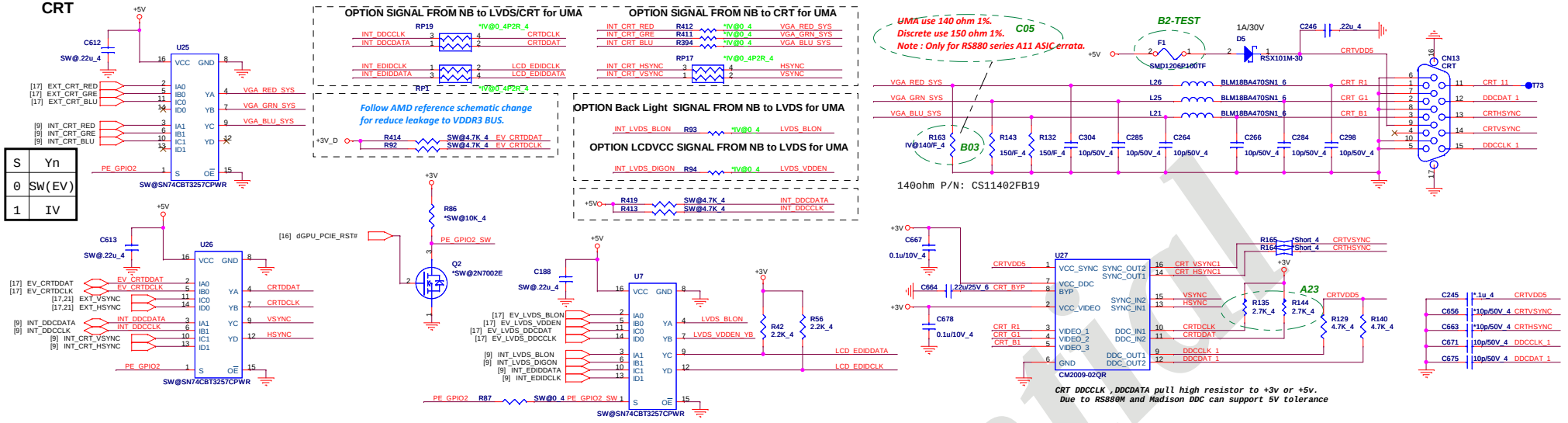




PROJECT : ZR8
Quanta Computer Inc.

Size	Document Number	Rev
	MEMORY 2 channel B	1A
Date: Wednesday, May 27, 2009	Sheet 23 of 49	

CRT

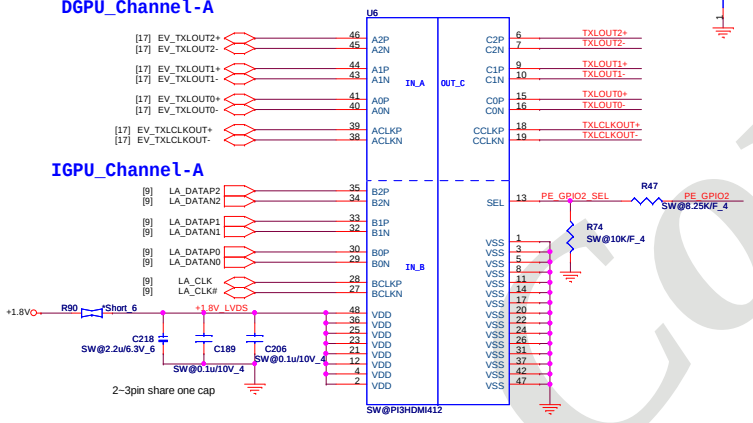


S	Yn
0	SW(EV)
1	IV

S	Yn
0	SW(EV)
1	IV

DGPU_Channel-A

IGPU_Channel-A

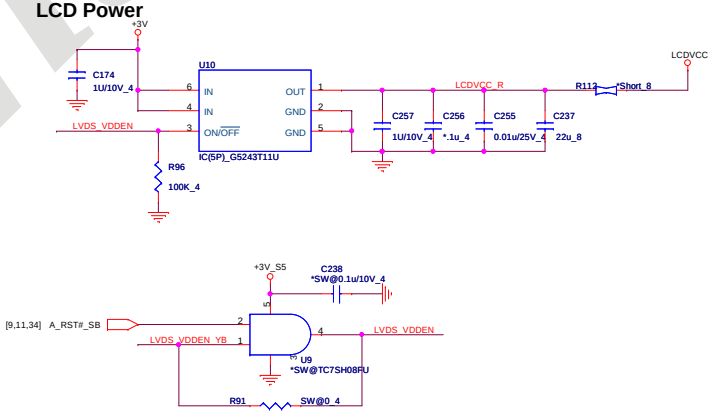


PE_GPIO2	Output
L	EV_LVDS
H	INT_LVDS

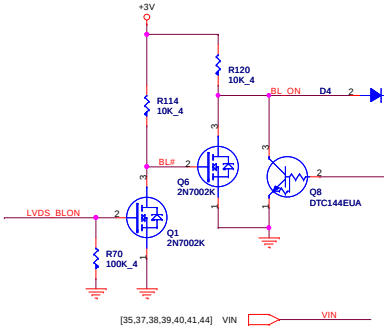
OPTION SIGNAL FROM NB to LVDS for UMA

OPTION DPST SIGNAL FROM NB to LVDS for UMA

LCD Power



Backlight Control



CAMERA Module(CCD)

PROJECT : ZR8			
Quanta Computer Inc.			
Size	Document Number		Rev
	CRT/LVDS/LID		1A
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UMA/DISCRETE select for HDMI

From RS880M

for Layout concern ,placement close north bridge

for Layout concern ,placement close HDMI conn

[8] PEG_TXN15_C / [8] PEG_TXP15_C — C280 / C272 *IV@0.1U/10V_4 — TX2_HDMI-L / TX2_HDMI+L — RP10 — *IV@0_4P2R_4 — TX2_HDMI- / TX2_HDMI+

[8] PEG_TXN14_C / [8] PEG_TXP14_C — C267 / C263 *IV@0.1U/10V_4 — TX1_HDMI-L / TX1_HDMI+L — RP9 — *IV@0_4P2R_4 — TX1_HDMI- / TX1_HDMI+

[8] PEG_TXN13_C / [8] PEG_TXP13_C — C253 / C247 *IV@0.1U/10V_4 — TX0_HDMI-L / TX0_HDMI+L — RP8 — *IV@0_4P2R_4 — TX0_HDMI- / TX0_HDMI+

[8] PEG_TXN12_C / [8] PEG_TXP12_C — C239 / C232 *IV@0.1U/10V_4 — TXC_HDMI-L / TXC_HDMI+L — RP7 — *IV@0_4P2R_4 — TXC_HDMI- / TXC_HDMI+

From dGPU

[17] EXT_HDMITX2N / [17] EXT_HDMITX2P — C698 / C697 SW@0.1u/10V_4 — TX2_HDMI- / TX2_HDMI+

[17] EXT_HDMITX1N / [17] EXT_HDMITX1P — C696 / C695 SW@0.1u/10V_4 — TX1_HDMI- / TX1_HDMI+

[17] EXT_HDMITX0N / [17] EXT_HDMITX0P — C694 / C693 SW@0.1u/10V_4 — TX0_HDMI- / TX0_HDMI+

[17] EXT_HDMICLK- / [17] EXT_HDMICLK+ — C692 / C691 SW@0.1u/10V_4 — TXC_HDMI- / TXC_HDMI+

for Layout concern ,placement close HDMI conn

+5V — Q34 2N7002K — R460 100K/F_4

R457 SP_715@499/F_4 TX2_HDMI+
R459 SP_715@499/F_4 TX2_HDMI-
R454 SP_715@499/F_4 TX1_HDMI+
R456 SP_715@499/F_4 TX1_HDMI-
R451 SP_715@499/F_4 TX0_HDMI+
R453 SP_715@499/F_4 TX0_HDMI-
R448 SP_715@499/F_4 TXC_HDMI+
R450 SP_715@499/F_4 TXC_HDMI-

UMA RS880M
上 715 ohm CS17152FB17

DIS Park-M2
上 499 ohm CS14992FB24

Close to HDMI Connector

EMI reserve for HDMI(HDM)

Close connector

TX2_HDMI+ — R458 *100/F_4 — TX2_HDMI-
TX1_HDMI+ — R455 *100/F_4 — TX1_HDMI-
TX0_HDMI+ — R452 *100/F_4 — TX0_HDMI-
TXC_HDMI+ — R449 *100/F_4 — TXC_HDMI-

HDMI HPD SENSE

UMA use +3V for the detect pin
Dis use +3V_DELAY for the detect pin

+3V_D — R444 SW@10K_4 — [17] EXT_HDMI_HPD — Q33 SW@2N7002K

+3V — R187 10K/F_4 — Q16 2N7002K — R177 200K/F_4 — HDMI_DET — R176 200K/F_4

+3V — R186 10K_4 — [9] INT_HDMI_HPD — Q15 2N7002K — HDMI_HPD_EC# [34]

Close to HDMI Connector

[9] HDMI_DDC_DATA / [9] HDMI_DDC_CLK — RP20 *IV@0_4P2R_4 — HDMI_SDATA / HDMI_SCLK

UMA

DIS

+3V — R443 SW@4.7K_4 — [17] EV_HDMI_DDCCK — Q41 SW@2N7002K — HDMI_SCLK — R445 *SW@0_4

+3V — R614 SW@4.7K_4 — [17] EV_HDMI_DDCDAT — Q42 SW@2N7002K — HDMI_SDATA — R534 *SW@0_4

A54

HDMI PORT

CN17 SP@HDMI

TX2_HDMI+ / TX2_HDMI- / TX1_HDMI+ / TX1_HDMI- / TX0_HDMI+ / TX0_HDMI- / TXC_HDMI+ / TXC_HDMI-
D2+ / D2 Shield / D2- / D1+ / D1 Shield / D1- / D0+ / D0 Shield / D0- / CK+ / CK Shield / CK- / CE Remote / NC / DDC CLK / DDC DATA / GND / +5V / HP DET
SHELL1 / SHELL2 / GND / GND

B2-TEST — +5VO — F2 SMD1206P100TF — D6 RSX101M-30 — +5V_HDMI — HDMI_DET — C363 0.22u/6.3V_4

HDMI_SCLK — D21 CH501H-40PT — R446 2K/F_4
HDMI_SDATA — D22 CH501H-40PT — R447 2K/F_4

P/N: AOP---->DFHD19MR083
LTS---->DFHD19MR085

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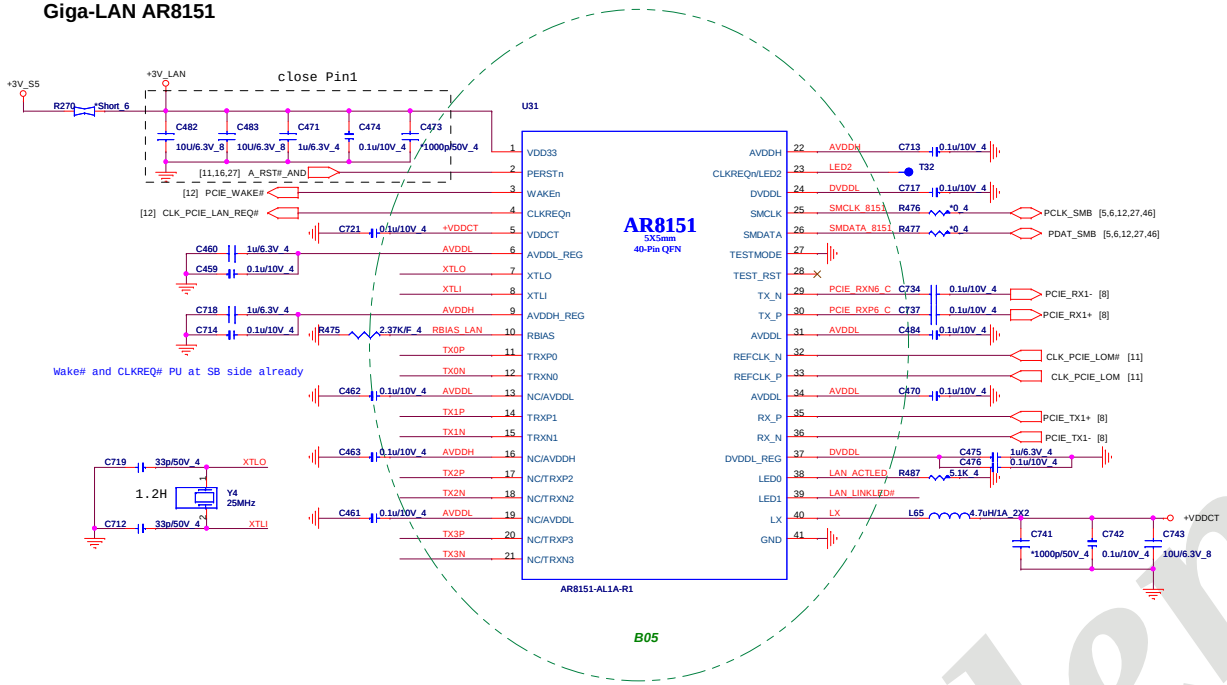
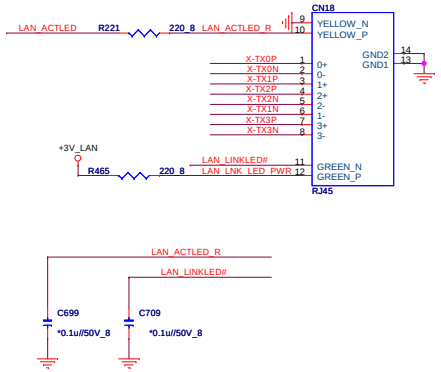
PROJECT : ZR8
Quanta Computer Inc.

Size	Document Number	Rev
	HDMI	1A
Date: Wednesday, May 27, 2009	Sheet 25 of 49	

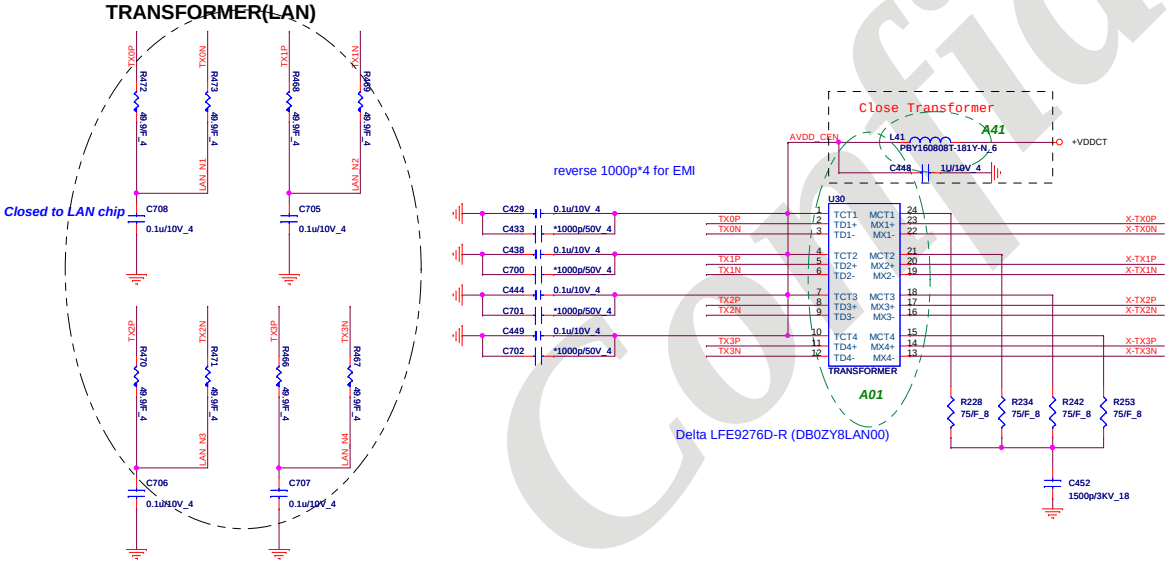
Giga-LAN AR8151



RJ45(LAN)



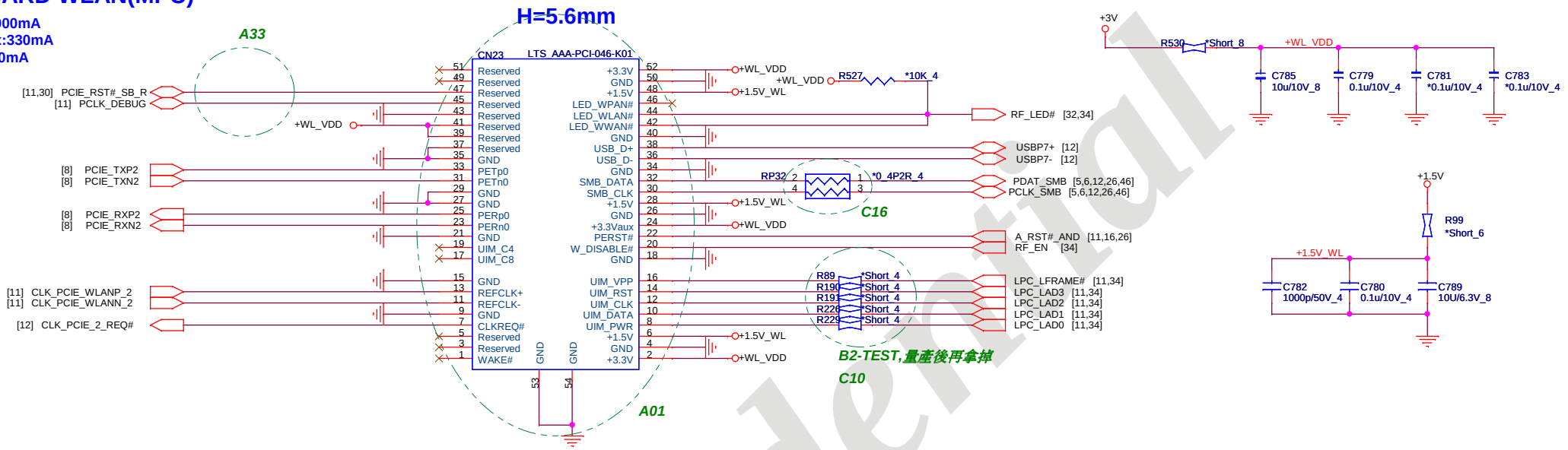
TRANSFORMER(LAN)



PROJECT : ZR8		
Quanta Computer Inc.		
Size	Document Number: LAN (AR8151)	Rev: 1A
Date: Wednesday, May 27, 2009	Sheet 26 of 49	

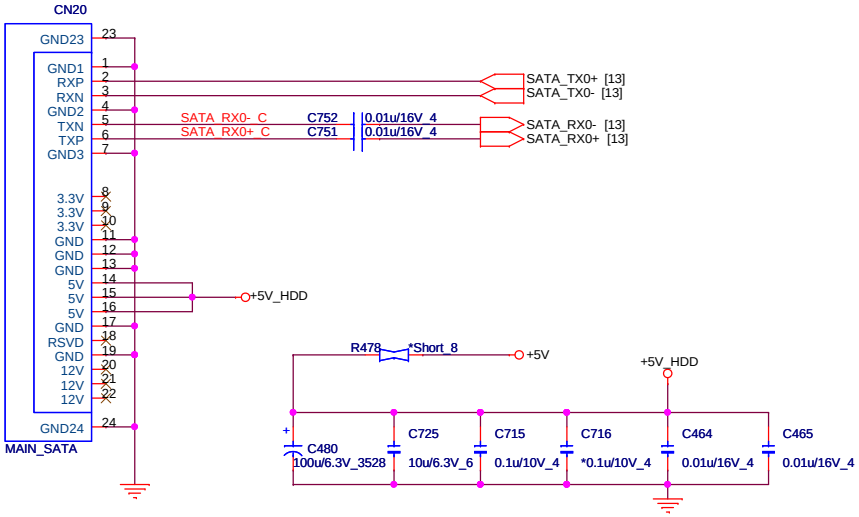
MINI-CARD WLAN(MPC)

+3.3V: 1000mA
+3.3Vaux:330mA
+1.5V:500mA



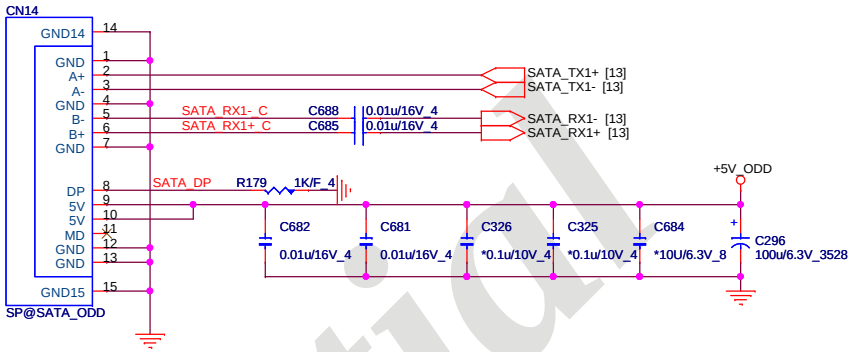
PROJECT : ZR8		
Quanta Computer Inc.		
Size	Document Number: *Mini-Card/WL/3G/SIM*	Rev 1A
Date: Wednesday, May 27, 2009	Sheet 27 of 49	

SATA HDD(HDD)



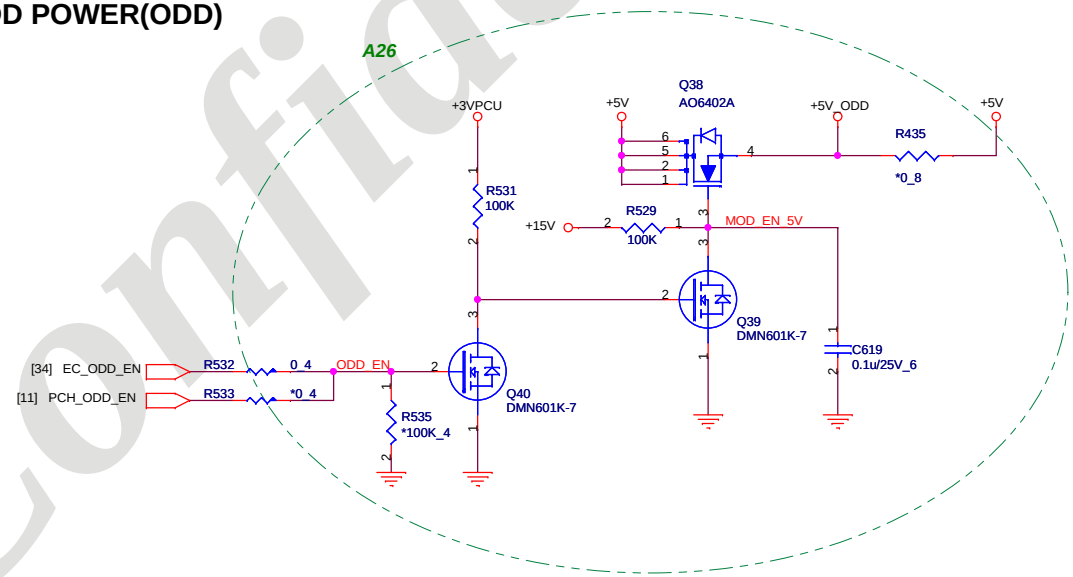
HOLE(OTH)

SATA ODD (ODD)



JM51(2-DIMM)-->CN14 P/N:DFHS13FR075
JV51(3-DIMM)-->CN14 P/N:DFHS13FR017
DFHS13FR022
DFHS13FR005
DFHS13FR006

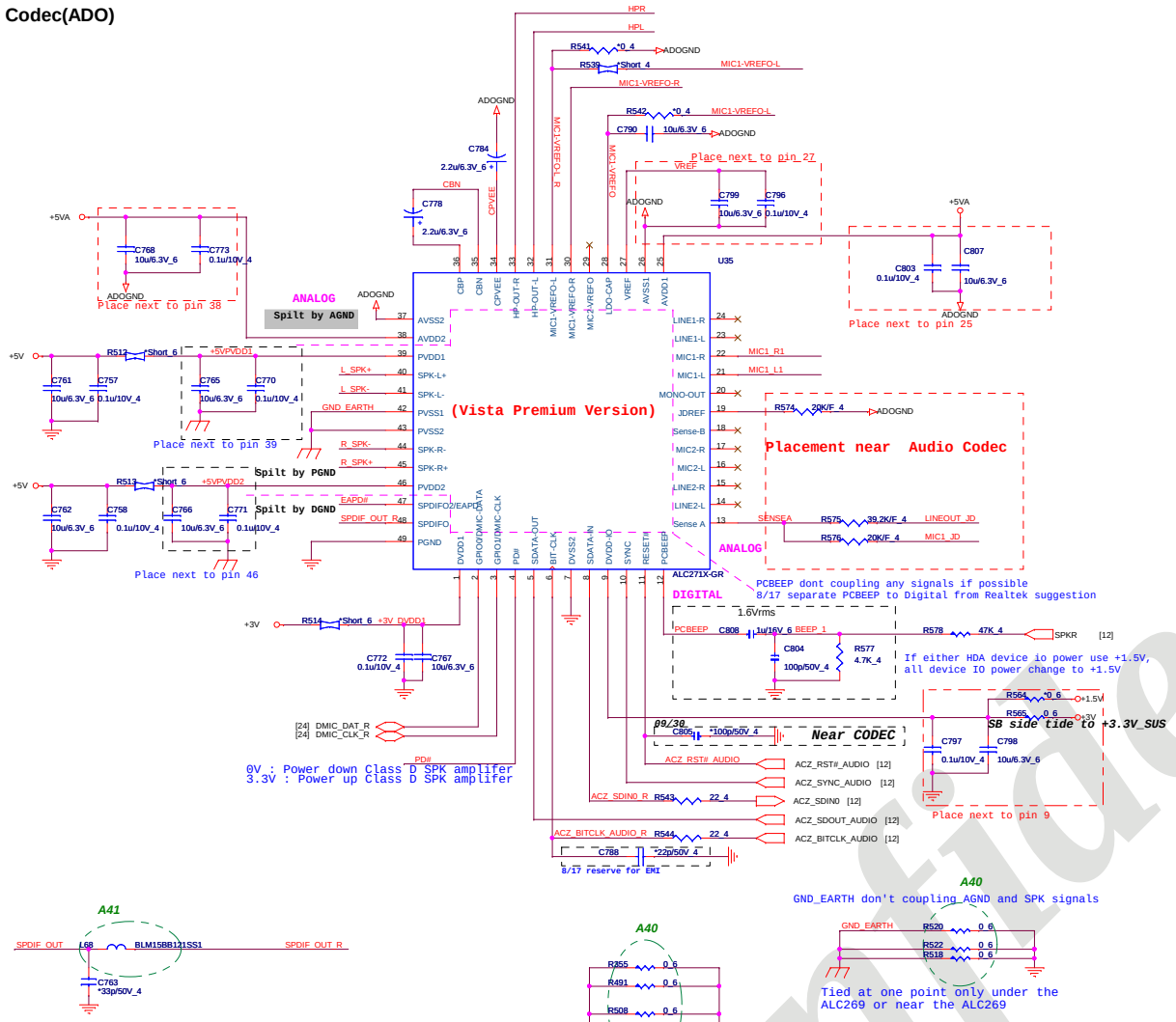
ODD POWER(ODD)



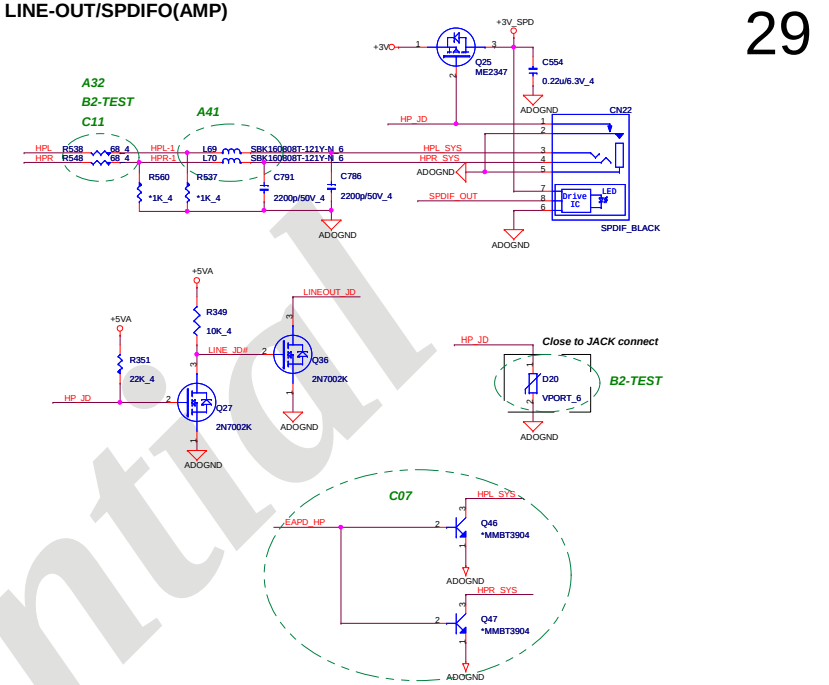
PROJECT : ZR8
Quanta Computer Inc.

Size	Document Number	Rev
	SATA-HDD/ODD	1A
Date: Wednesday, May 27, 2009	Sheet 28 of 49	

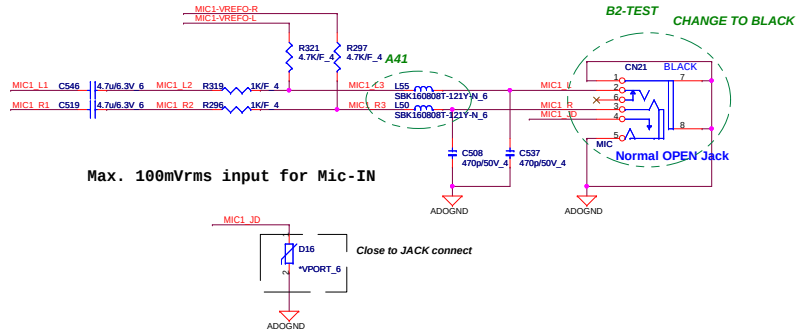
Codec(ADO)



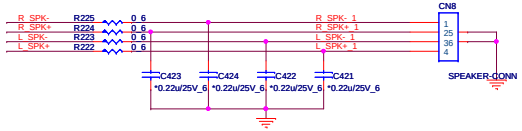
LINE-OUT/SPDIFO(AMP)



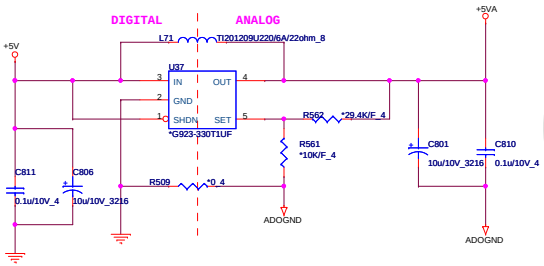
MIC(AMP)



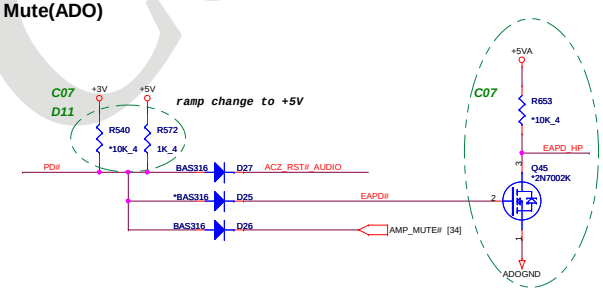
Internal Speaker(AMP)



Power (ADO)



Mute(ADO)



PROJECT : ZR8
Quanta Computer Inc.

Size	Document Number	Rev
	ALC271X / AMP / SPK	1A
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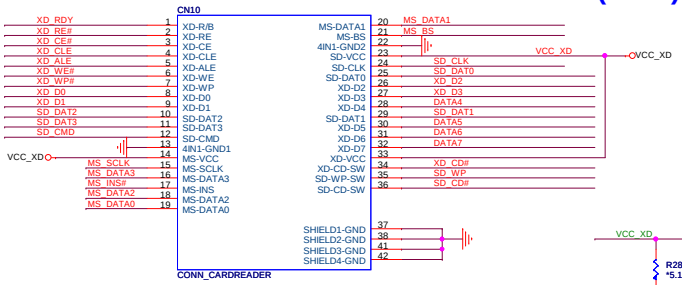
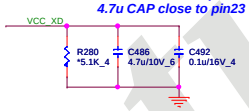
4 IN 1 CARD READER (MMC)



Close to Connect pin 14 & pin23
4.7u CAP close to pin23



Clock input selection
'1' for 48MHz input [Default]
'0' for 12MHz input

Main	DFHD36MS006
Second	DFHD36MS012

CTRL0, CRTL 1 trace length shorter , and surround with GND.

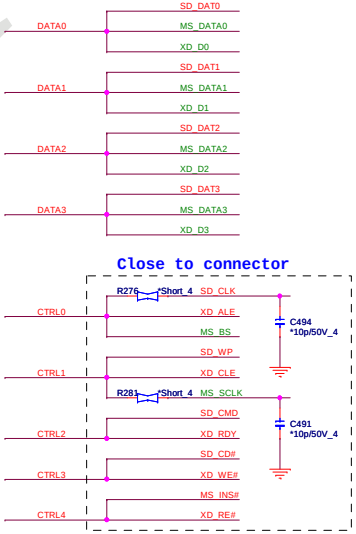
crystal trace width needs at least 10 mils.

pin13 output 20mils
CAP close PIN11,12

pin14 output 15mils

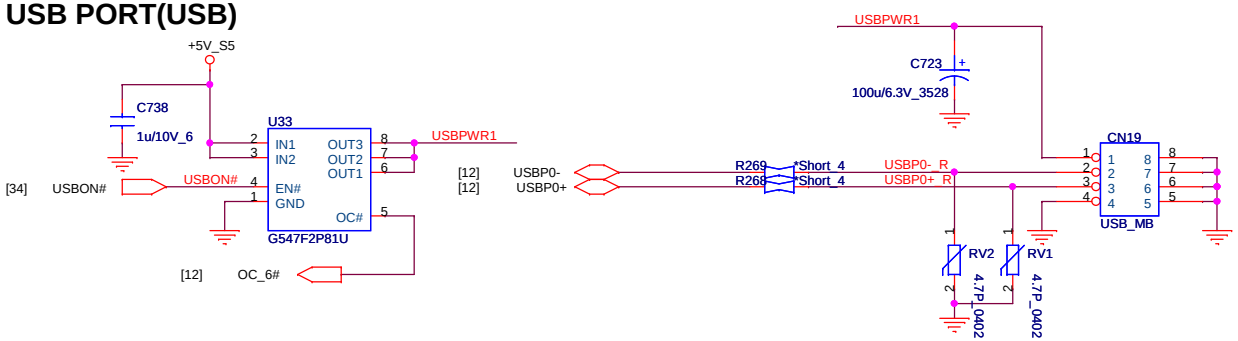
SD write protect
1:decided by SDWP[Default]
0:letting SD always write-able

Close to connector

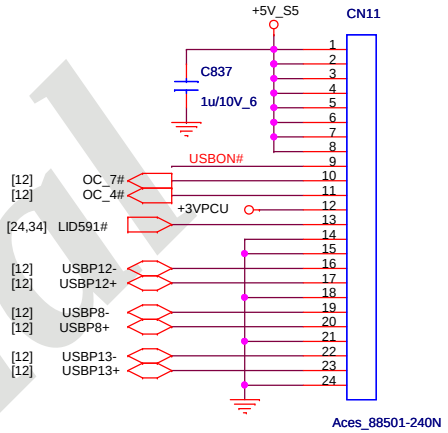


PROJECT : ZR8			
Quanta Computer Inc.			
Size	Document Number		Rev
	AU6437 CardReader		1A
Date:	Wednesday, May 27, 2009	Sheet 30 of	49

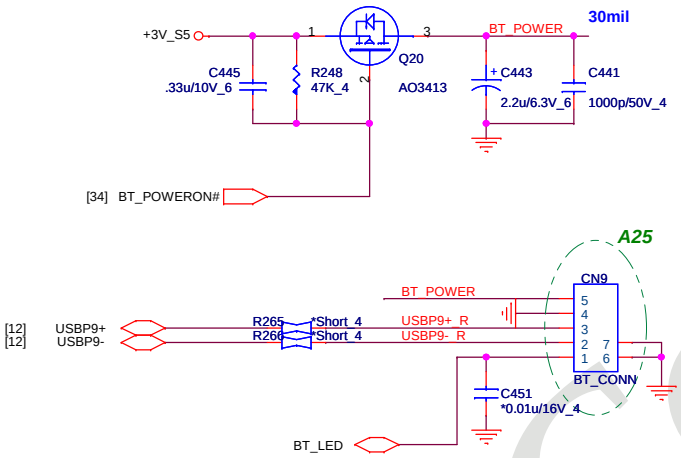
USB PORT(USB)



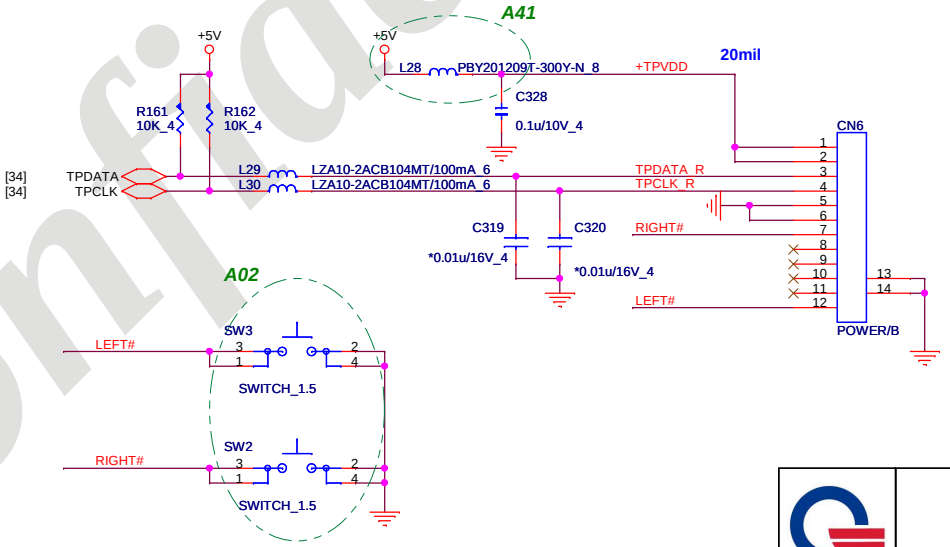
USB BOARD CONN(USB)



BLUETOOTH CONN(BTM)



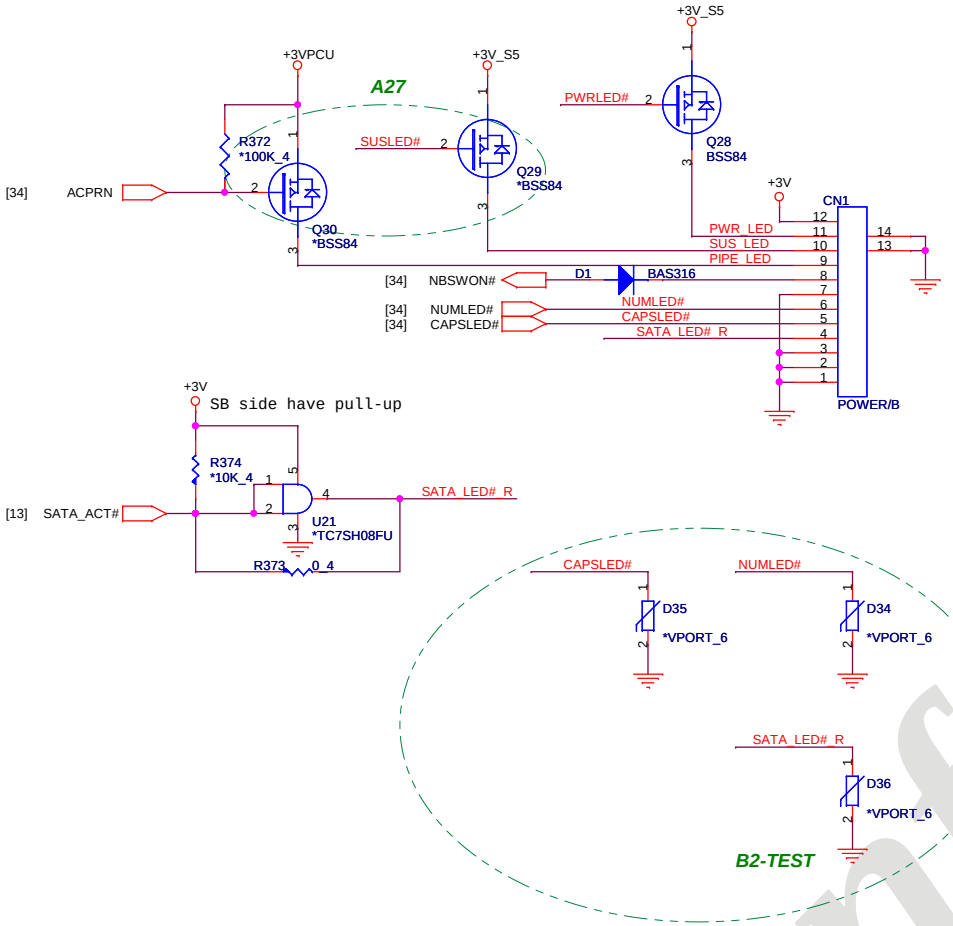
TOUCHPAD BOARD CONN(TPD)



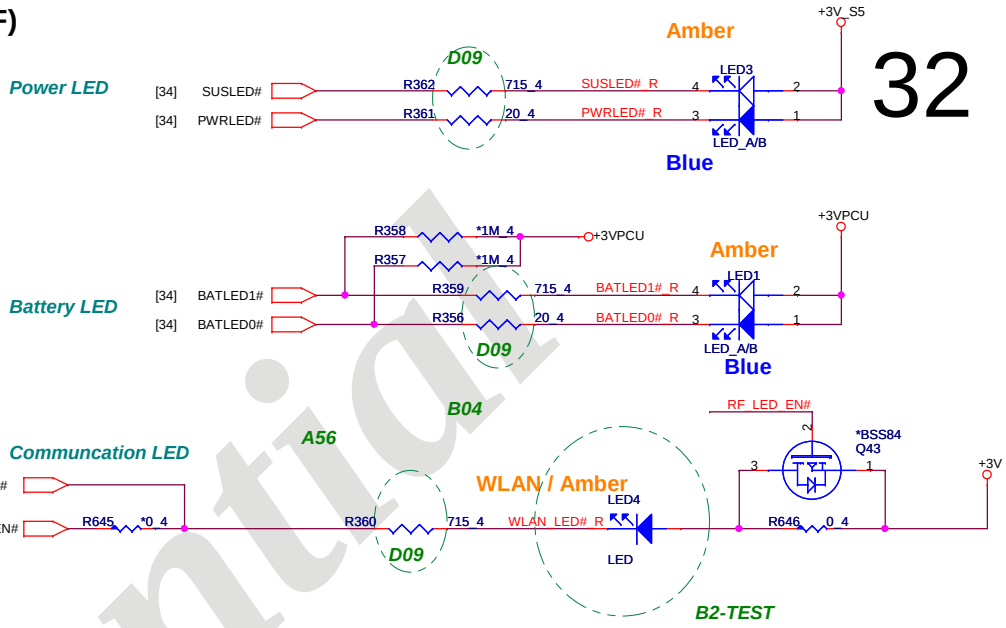
PROJECT : ZR8
Quanta Computer Inc.

Size	Document Number	Rev
	eSATA/USB	1A
Date: Wednesday, May 27, 2009	Sheet 31 of 49	

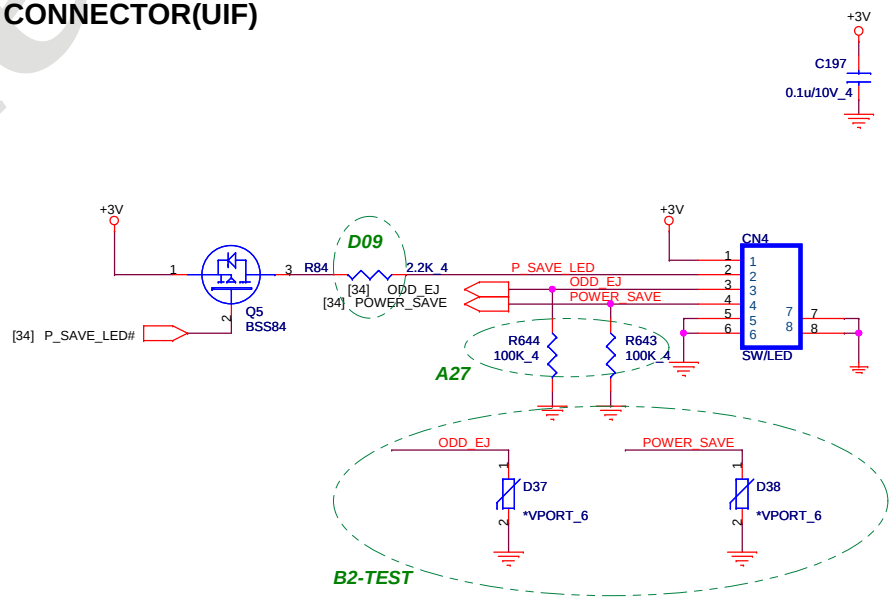
POWER BOARD CONN(UIF)



LED(UIF)



LED BOARD CONNECTOR(UIF)

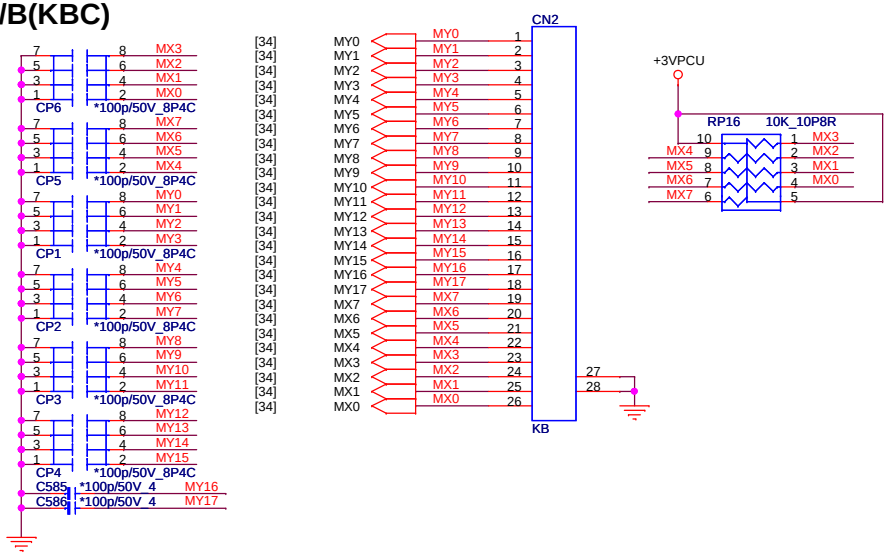


PROJECT : ZR8

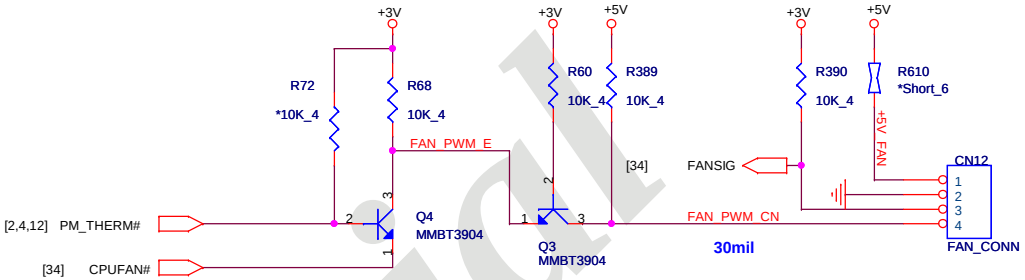
Quanta Computer Inc.

Size	Document Number	Rev
	POWER/USB/BT/TP/MDC	1A
Date: Wednesday, May 27, 2009	Sheet 32 of 49	

K/B(KBC)

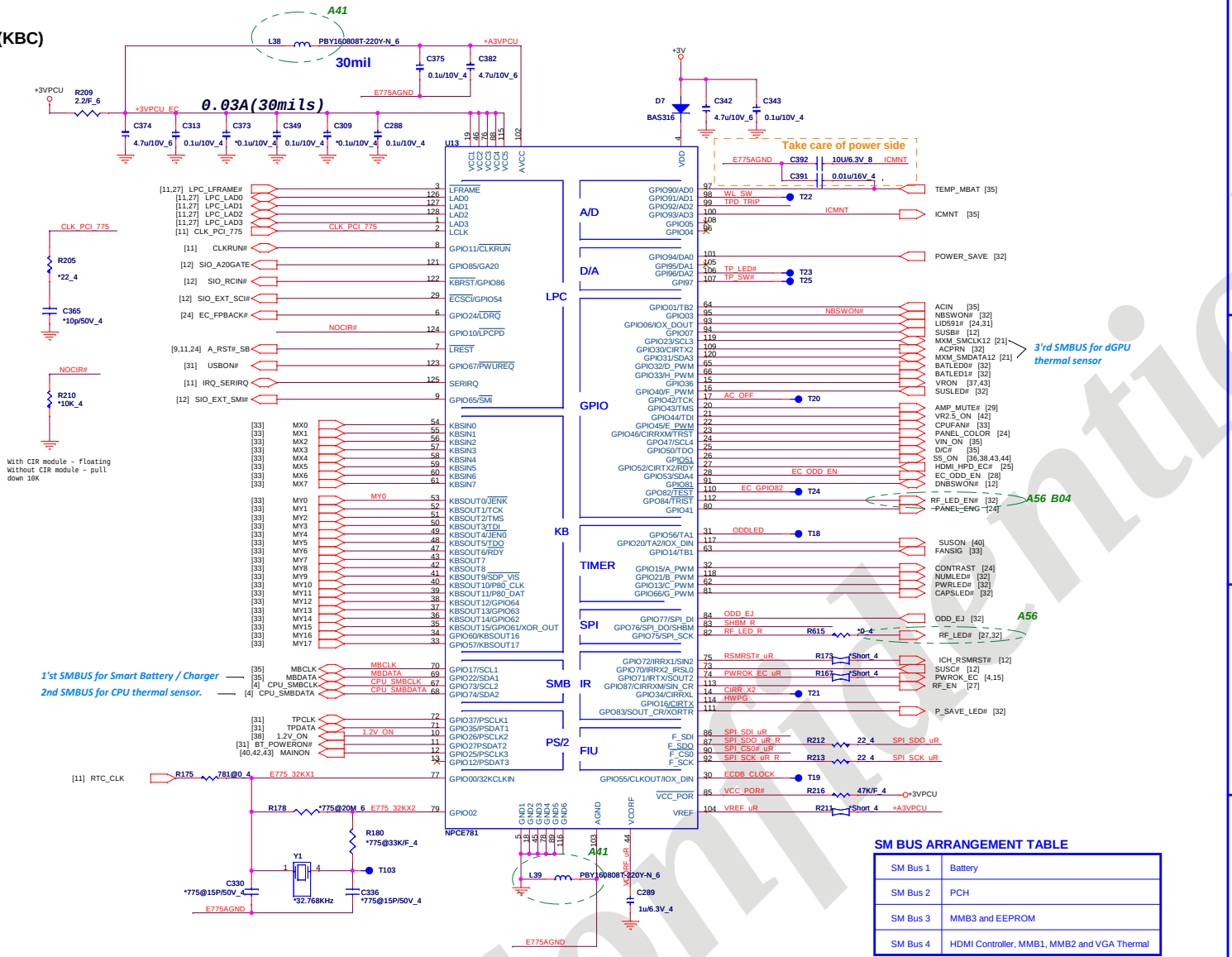


CPU FAN(THM)



PROJECT : ZR8		
Quanta Computer Inc.		
Size	Document Number: KB/FAN/EE RETURN CAP	Rev 1A
Date: Wednesday, May 27, 2009	Sheet 33 of 49	

EC(KBC)

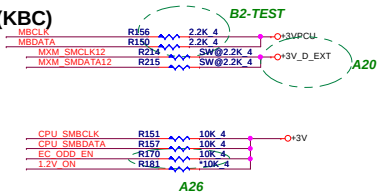


I/O ADDRESS SETTING(KBC)

SHBM=0: Enable shared memory with host BIOS

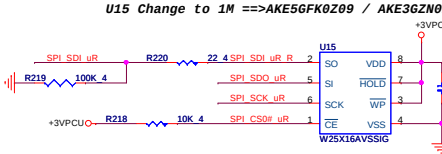
1/13 Comfirm by vendor mail :
Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware

SM BUS PU(KBC)



SPI FLASH(KBC)

U15 Change to 1M ==>AKE5GFK0Z09 / AKE3GZN0N00 / AKE3GZP0801

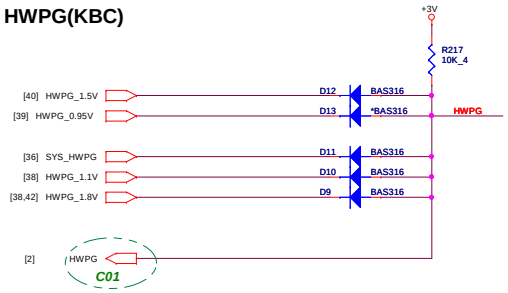


1/13 Comfirm by vendor mail :
If the Southbridge enables 'Long Wait Abort' by
default, the flash device should be 50MHz (or faster)

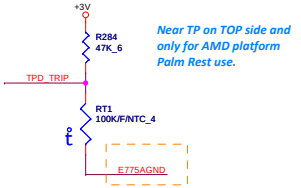
SM BUS ARRANGEMENT TABLE

SM Bus 1	Battery
SM Bus 2	PCH
SM Bus 3	MMB3 and EEPROM
SM Bus 4	HDMI Controller, MMB1, MMB2 and VGA Thermal

HWPG(KBC)

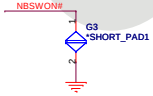


Palm Rest Thermal Sensor(THM)



Near TP on TOP side and only for AMD platform Palm Rest use.

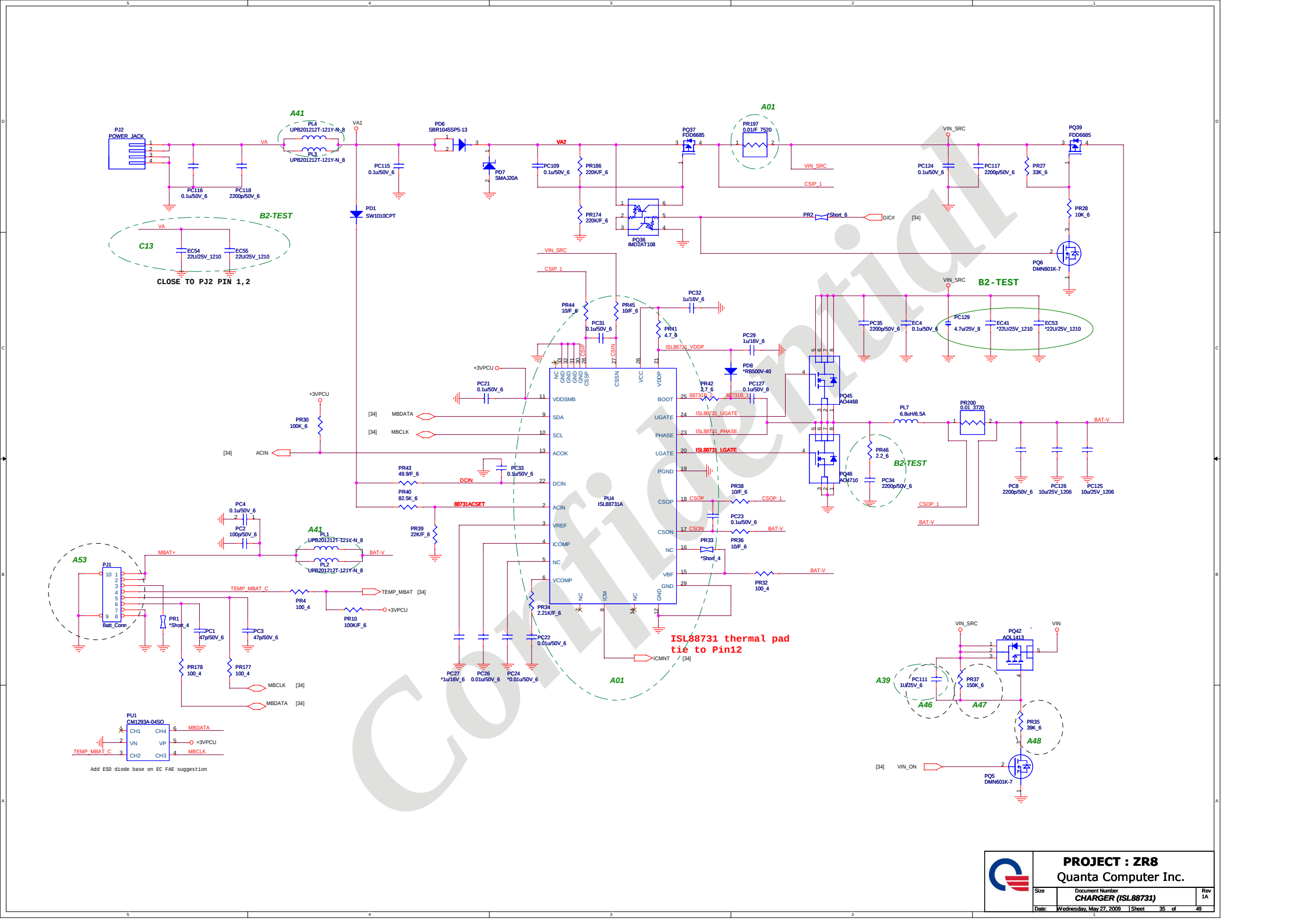
POWER-ON Switch(KBC)

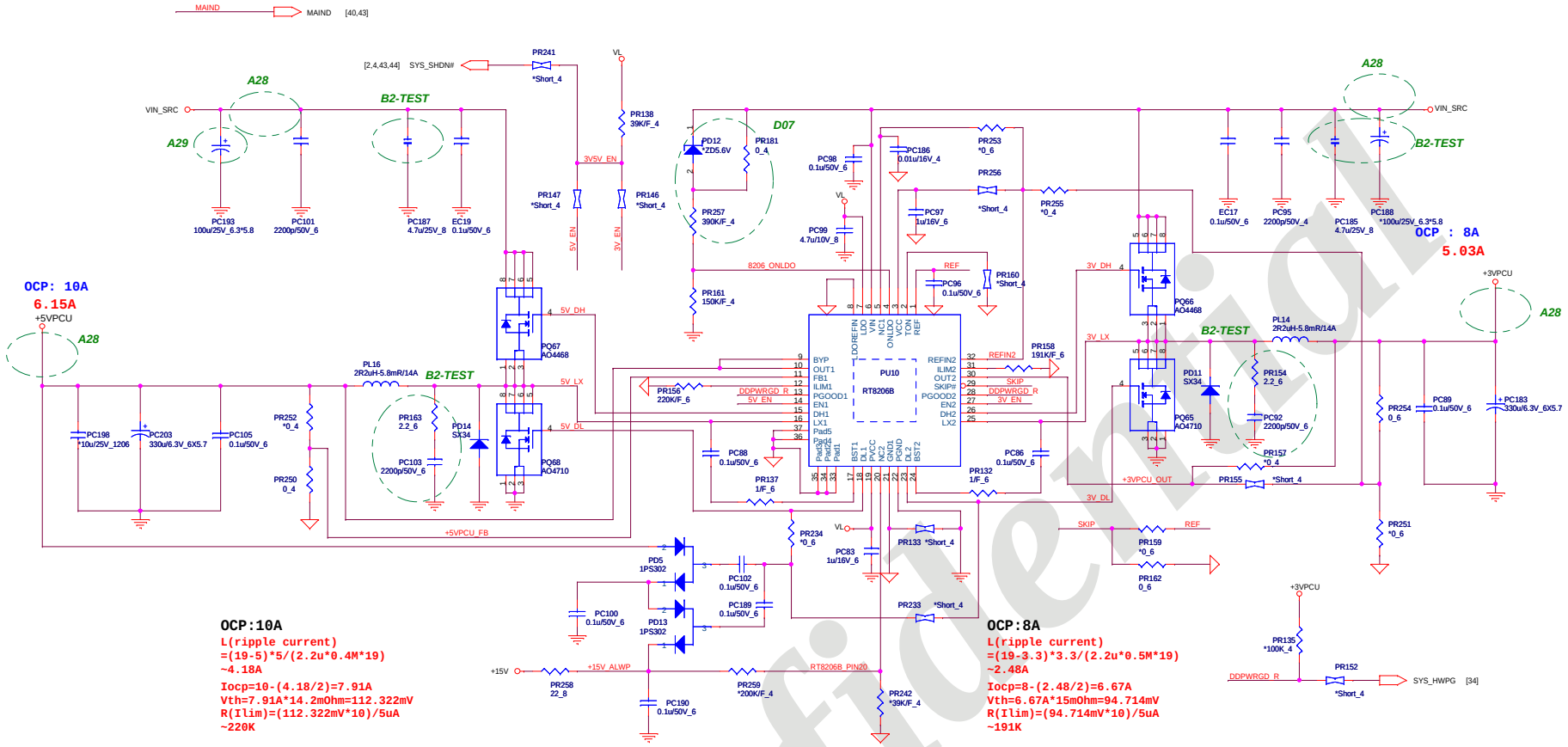


INTERNAL KEYBOARD STRIP SET(KBC)

PROJECT : ZR8
Quanta Computer Inc.

Size	Document Number	Rev
	WPCE775C_0DG & FLASH	1A
Date: Wednesday, May 27, 2009	Sheet 34 of 49	





PROJECT : ZR8		
Quanta Computer Inc.		
Size	Document Number: SYSTEM 5V/3V (RT8206)	Rev 1A
Date: Wednesday, May 27, 2009	Sheet 36 of 49	

OFS/VFIXEN	Offset & Droop	SVI	VFIX
GND	O	O	X
+3.3V	X	X	O
+5V	X	O	X

Metal VID Codes

SVC	SVD	Output
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

VFIXEN VID Codes

SVC	SVD	Output
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8

3A

20A

20A

Pin 49 is GND Pin

Close to CPU socket

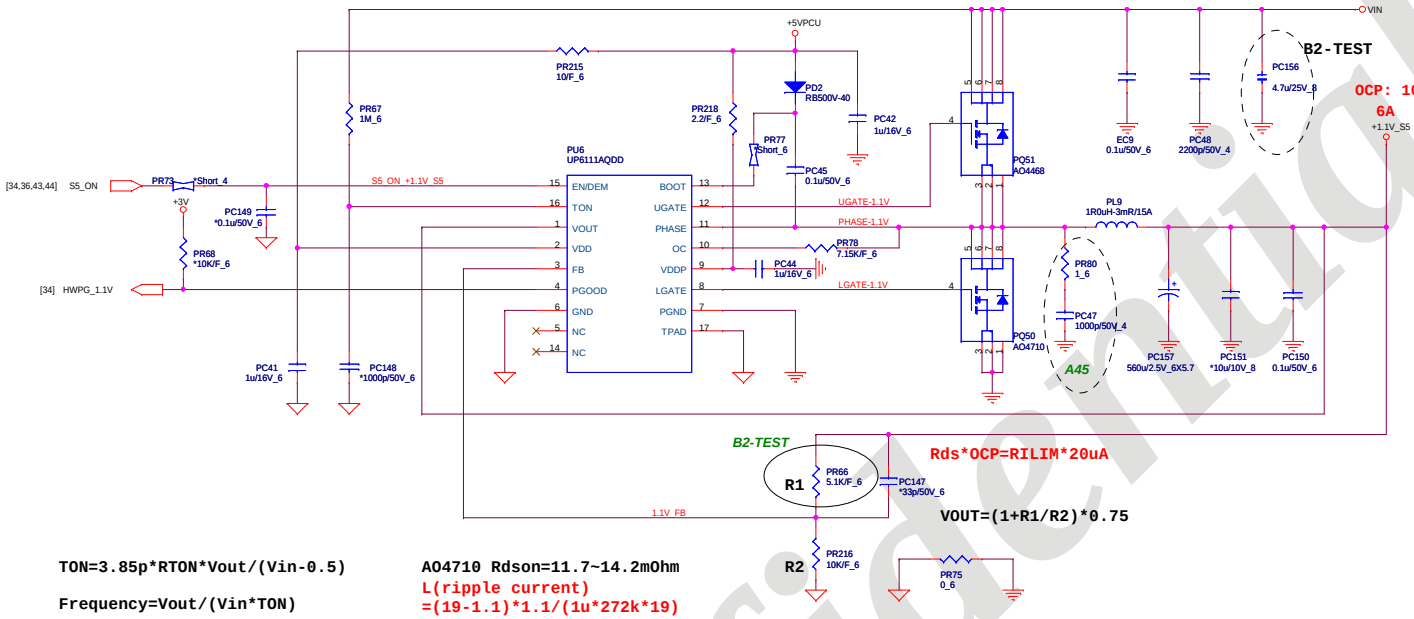
Close to CPU socket

Parallel

PROJECT : ZR8

Quanta Computer Inc.

Size	Document Number	Rev
	CPU_CORE	1A
Date: Wednesday, May 27, 2009	Sheet 37 of 49	



TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)

TON=3.85p*1M*1/(Vin-0.5)

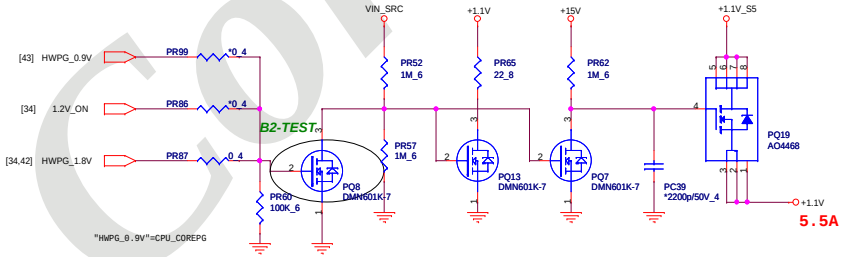
Frequency=1/(0.0036767)=272K

AO4710 Rdson=11.7~14.2mOhm

L(ripple current)
=(19-1.1)*1.1/(1u*272k*19)
~3.81A

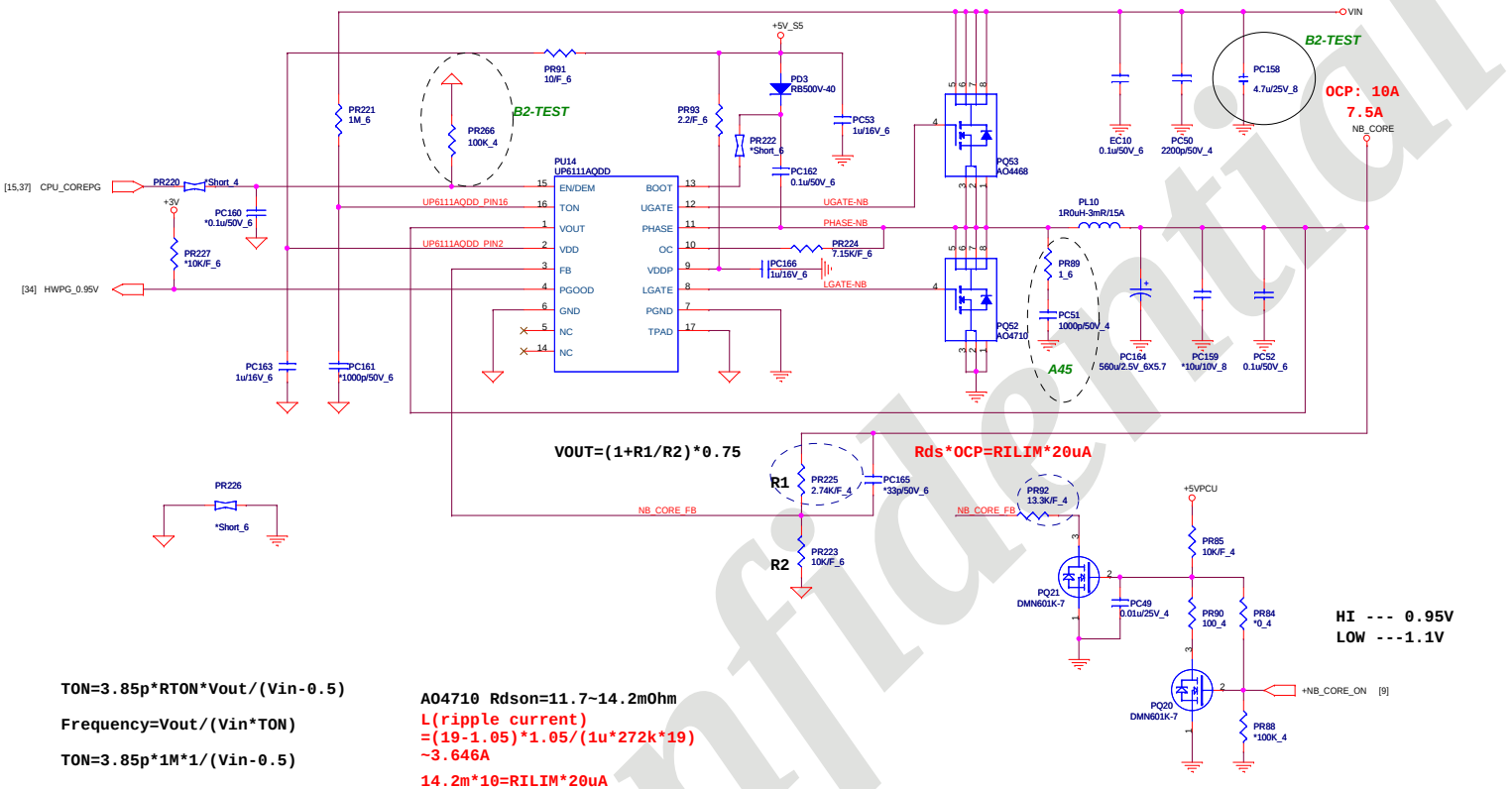
14.2m*10=RILIM*20uA

RILIM=7.1K--- 7.15K



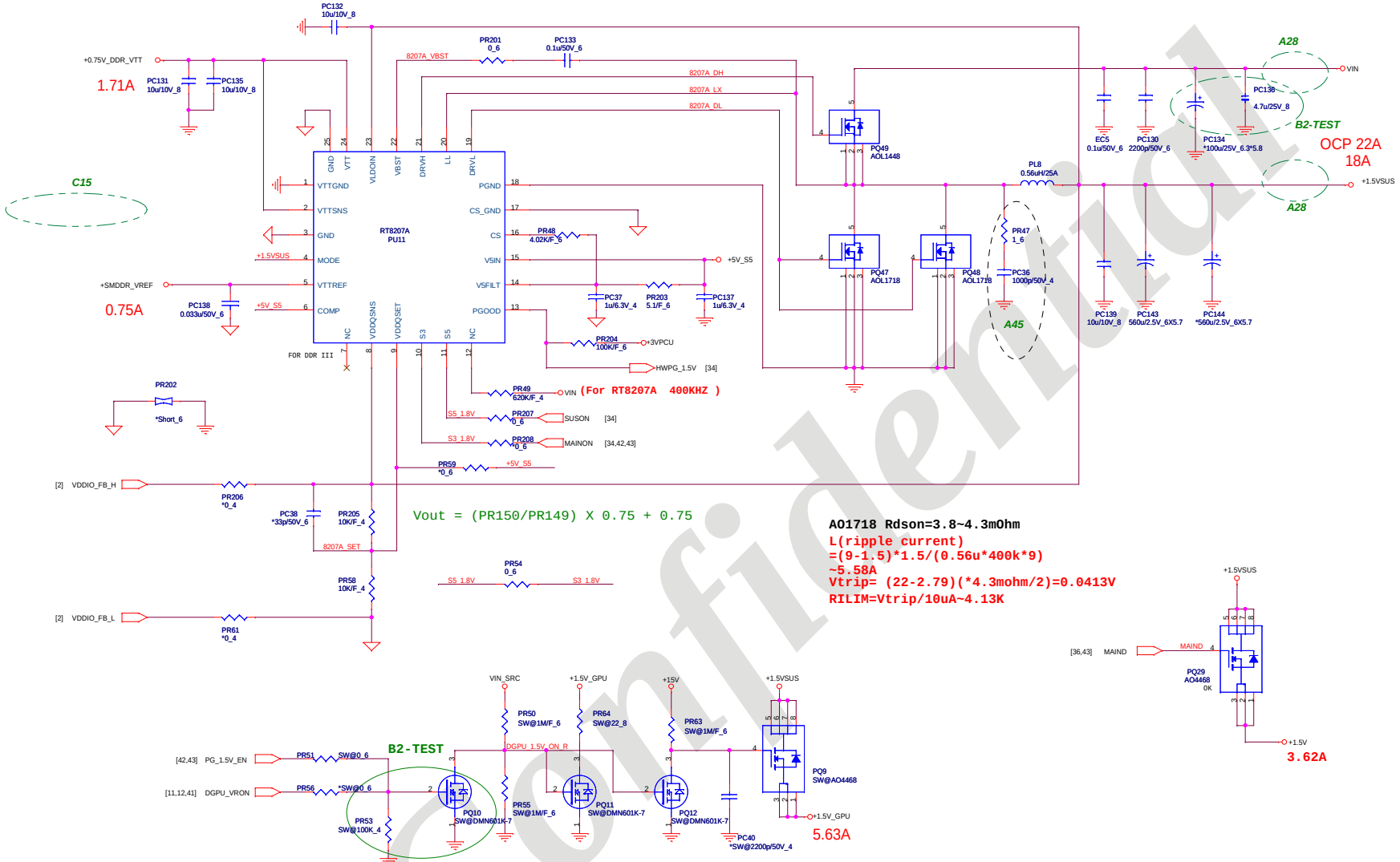
PROJECT : ZR8
Quanta Computer Inc.

Size	Document Number	Rev
	VCCP 1.1V(UP6111A)	1A
Date: Wednesday, May 27, 2009	Sheet 38 of 49	

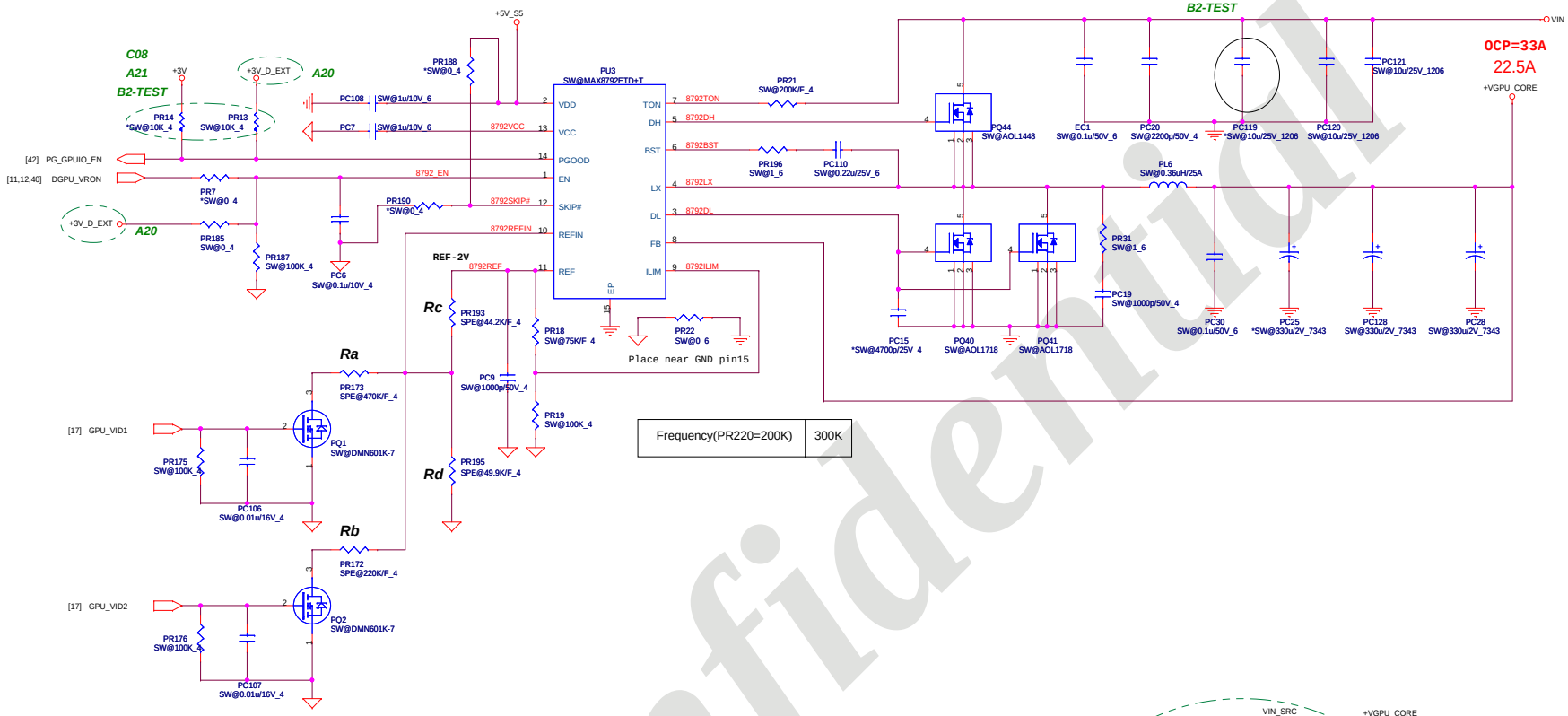


PROJECT : ZR8		
Quanta Computer Inc.		
Size	Document Number: NB_CORE(UP6111A)	Rev: 1A
Date: Wednesday, May 27, 2009	Sheet 39 of 49	

[PWM]



PROJECT : ZR8		
Quanta Computer Inc.		
Size	Document Number	Rev
	DDR 1.5V(TPS51116)	1A
Date: Wednesday, May 27, 2009	Sheet 40 of 49	



Frequency(PR220=200K)	300K

Madison -Pro		
GPU_VID1 (GPIO15)	GPU_VID2 (GPIO20)	+VGPU_CORE
0	0	1.05V
1	0	1.0V
0	1	0.95V
1	1	0.9V

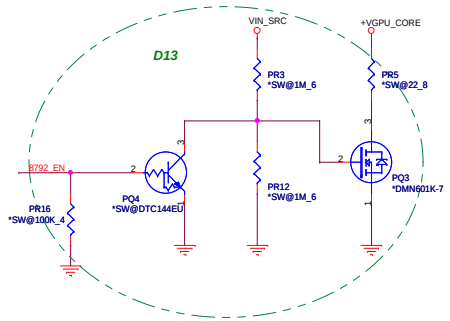
Ra	Rb	Rc	Rd	VREF
470K	220K	44.2K	49.9K	2V

Park -XT		
GPU_VID1 (GPIO15)	GPU_VID2 (GPIO20)	+VGPU_CORE
0	0	1.12V
1	0	1.05V
0	1	0.95V
1	1	0.9V

Ra	Rb	Rc	Rd	VREF
332K	130K	39.2K	49.9K	2V

A03

Rc --> 39.2K/F_4 (CS33922FB15)
Ra --> 332K/F_4 (CS43322FB15)
Rb --> 130K/F_4 (CS41302FB00)



PROJECT : ZR8
Quanta Computer Inc.

Size	Document Number	Rev
	GPU CORE(MAX8792)	1A
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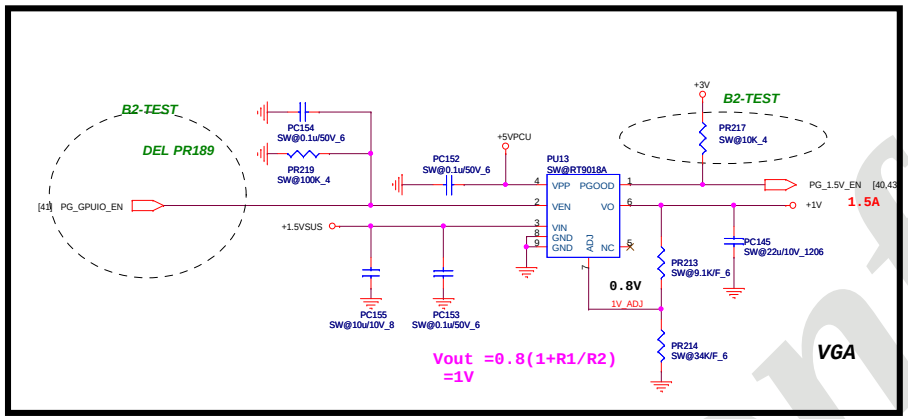

PROJECT : ZR8	
Quanta Computer Inc.	
Size	Document Number: Discharge (2.5V/1.8V) — Rev 1A
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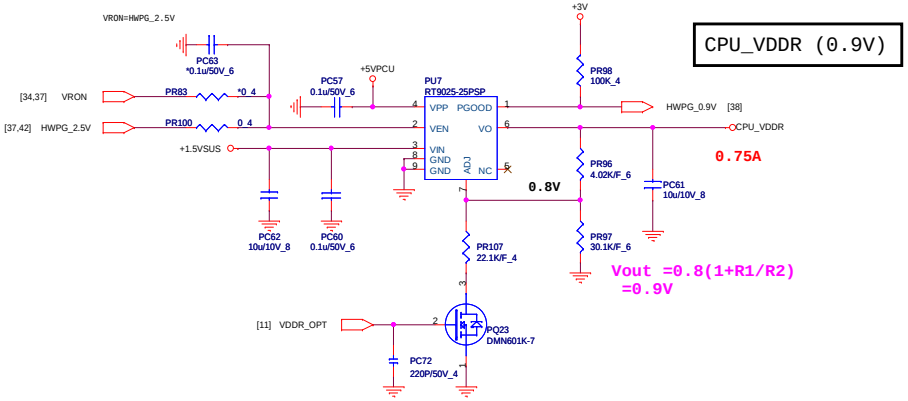

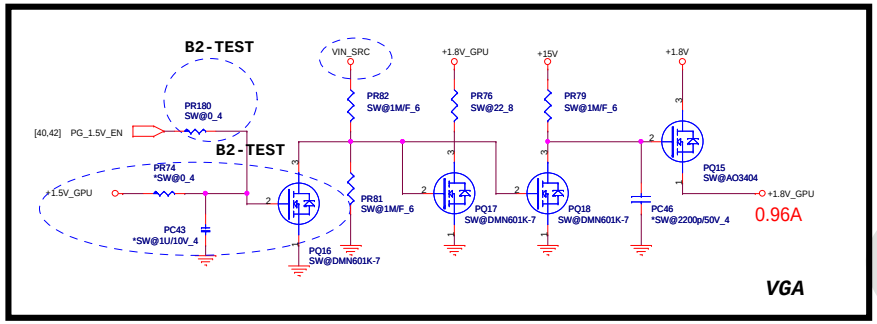

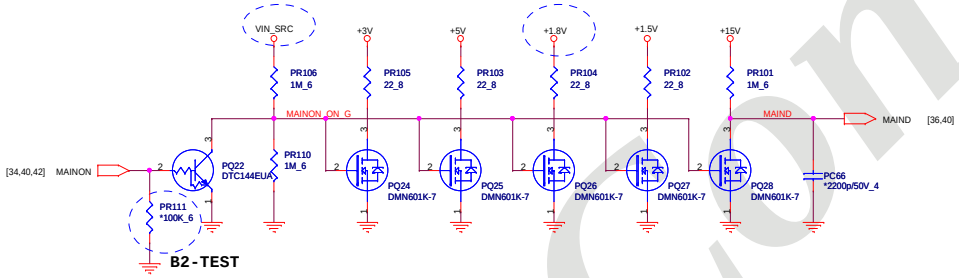

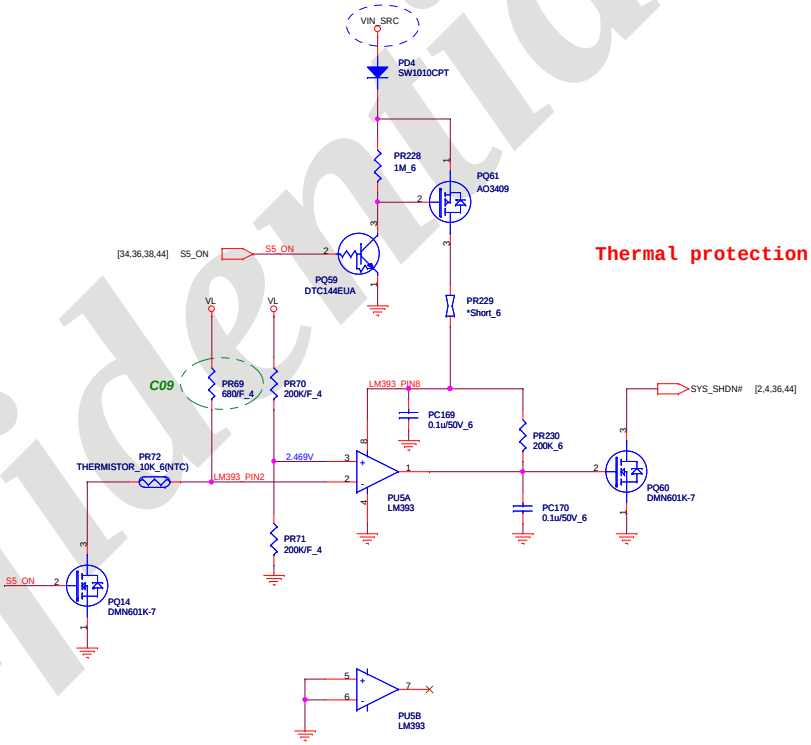

Thermal protection

For EC control thermal protection (output 3.3V)

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Quanta Computer Inc.		
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HOLE26 *H-C276D110P2-8
HOLE21 *H-CT236B315D110P2
HOLE7 *O-ZR8-10
HOLE17 *H-C276D110P2-8
HOLE1 *H-C276D110P2-8
HOLE27 *HG-C315D110P2

CPU

HOLE11 *H-C236D142PB
HOLE12 *H-C236D142PB
HOLE15 *H-C236D142PB
HOLE16 *H-C236D142PB

HOLE3 *H-C276D110P2-8
HOLE2 *HG-C315D110P2
HOLE22 *H-C91D91N

HOLE25 * H-C276D110P2-8
HOLE19 *H-C236D161PB
HOLE13 *H-C236D161PB
HOLE18 *H-C236D161PB

HOLE14 *hg-c355d110p2
HOLE28 *hg-c394d110p2
HOLE30 *hg-c236d110p2

HOLE9 *H-C236D157P2

VGA

HOLE10 *H-TC197BC122D122P2
HOLE4 *H-C197D122PB
HOLE5 *H-TC197BC122D122P2

HOLE23 *H-C236D161PB
HOLE8 *H-C236D157P2
HOLE20 *H-C91D91N
HOLE6 * H-C236D142P2

HOLE29 *H-C157D79PT
HOLE24 *H-C157D102PT

HOLE31 *H-TC236BC161D161P2
HOLE32 *H-C276D110P2-8

B2-TEST

VIN — EC52 0.1u/25V_4 — VIN — EC51 0.1u/25V_4

B2-TEST

+5V — EC50 0.1u/10V_4 — EC49 0.1u/10V_4 — EC48 0.1u/10V_4 — EC47 0.1u/10V_4 — EC46 0.1u/10V_4 — EC45 0.1u/10V_4 — EC44 0.1u/10V_4

For EMI

NB_CORE — EC11 *0.1u/25V_4
+VGPU_CORE — EC3 *0.1u/25V_4
+5VA — EC32 *0.1u/25V_4
+5VPCU — EC18 *0.1u/25V_4

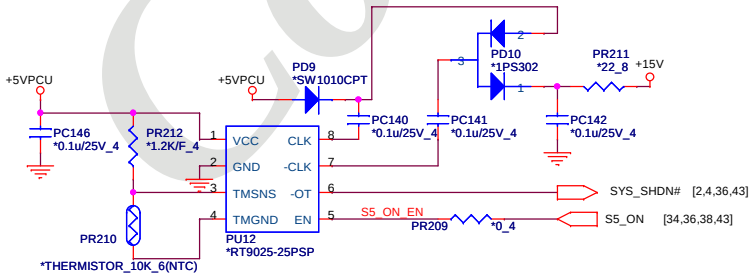
VIN_SRC — EC26 *0.1u/25V_4 — EC20 *0.1u/25V_4
+1.8V — EC12 *0.1u/25V_4 — EC31 *0.1u/25V_4
+3V_S5 — EC21 *0.1u/10V_4
+3V_S5 — EC22 *0.1u/10V_4
+3V — EC6 *0.1u/10V_4

+1.1V — EC8 *0.1u/25V_4 — EC23 *0.1u/25V_4
+1.5VSUS — EC14 *0.1u/25V_4 — EC7 *0.1u/25V_4
+3V — EC43 *0.1u/10V_4
+3V — EC42 *0.1u/10V_4

+5V — EC40 *0.1u/25V_4 — EC30 *0.1u/25V_4 — EC24 *0.1u/25V_4
+3VPCU — EC28 *0.1u/25V_4 — EC35 *0.1u/25V_4 — EC39 *0.1u/25V_4 — EC29 *0.1u/25V_4

+3V — EC16 *0.1u/25V_4 — EC15 *0.1u/25V_4 — EC38 *0.1u/25V_4 — EC36 *0.1u/25V_4 — EC34 *0.1u/25V_4 — EC27 *0.1u/25V_4 — EC37 *0.1u/25V_4 — EC33 *0.1u/25V_4

POWER TEST



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Quanta Computer Inc.		
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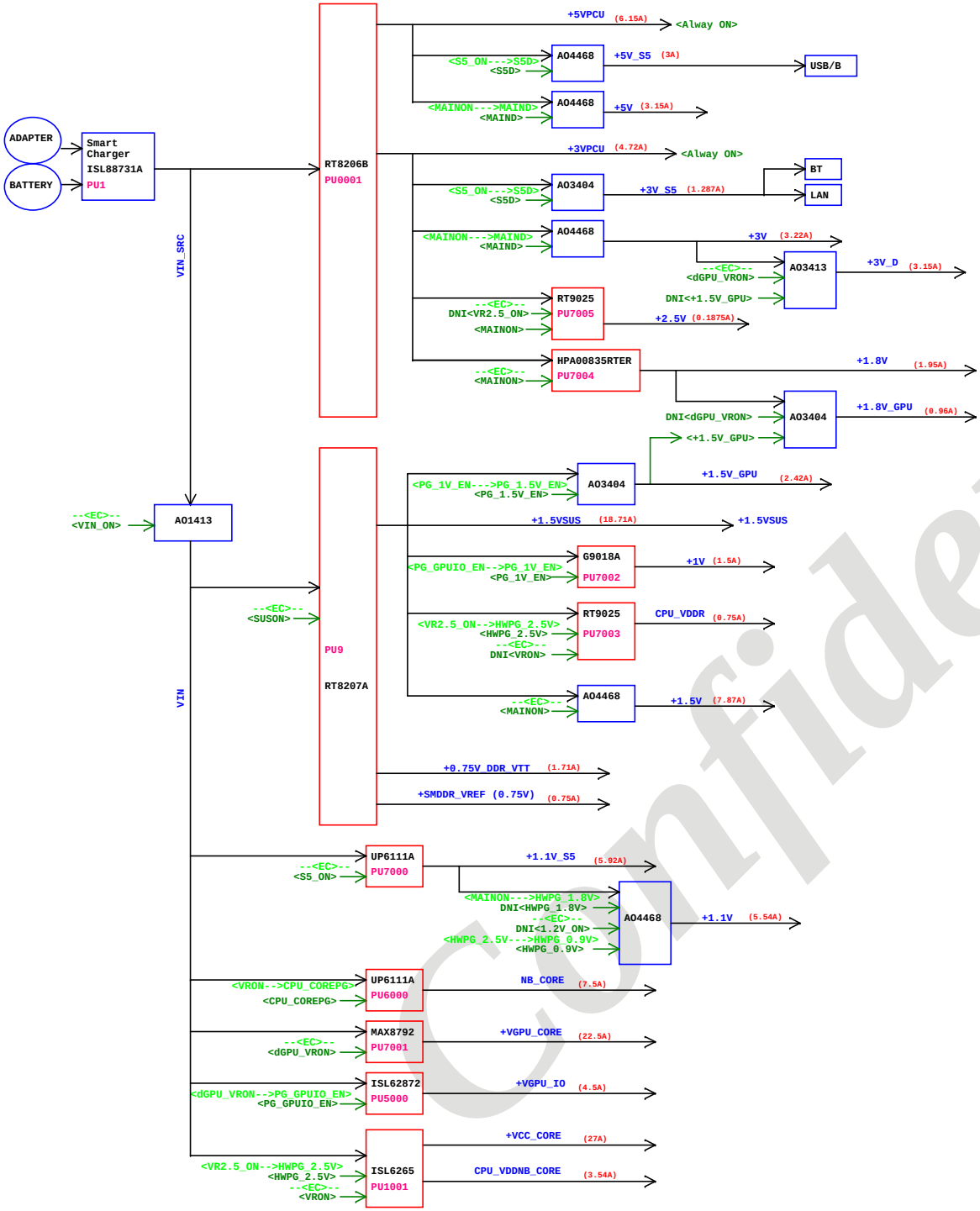
ZR8 Power tree



PROJECT : ZR8
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Power Tree
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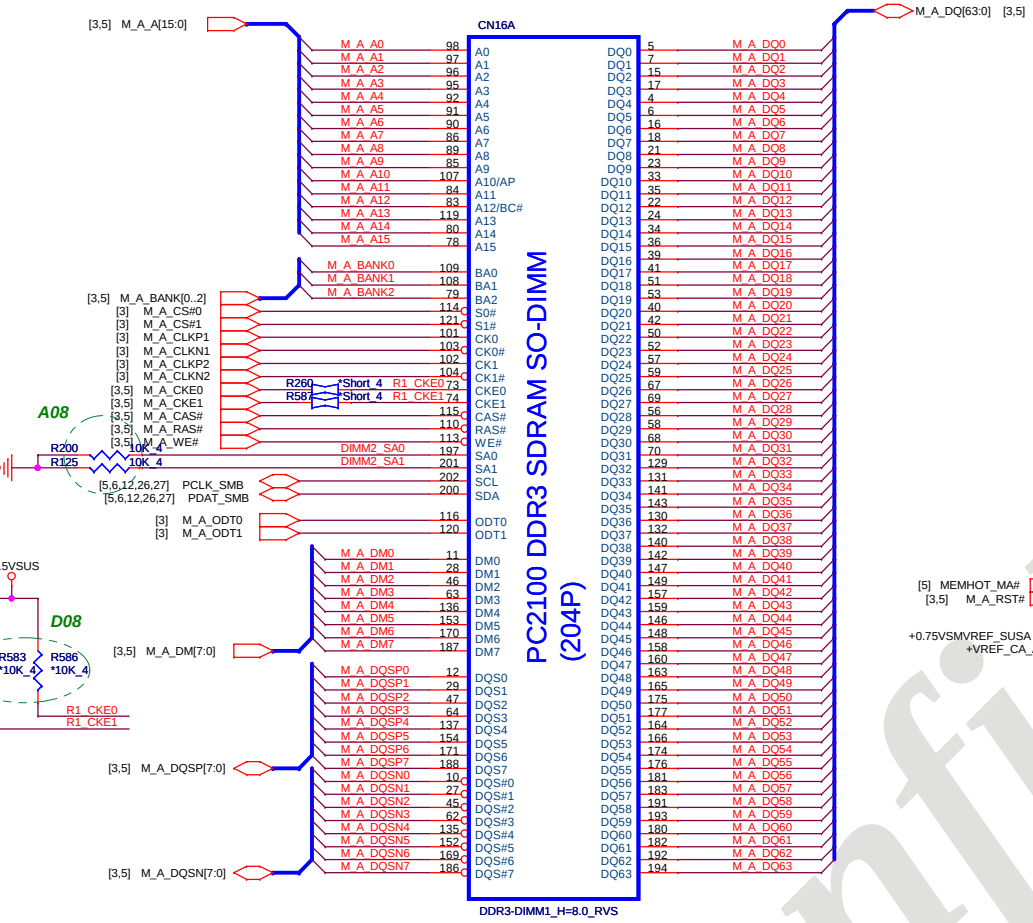
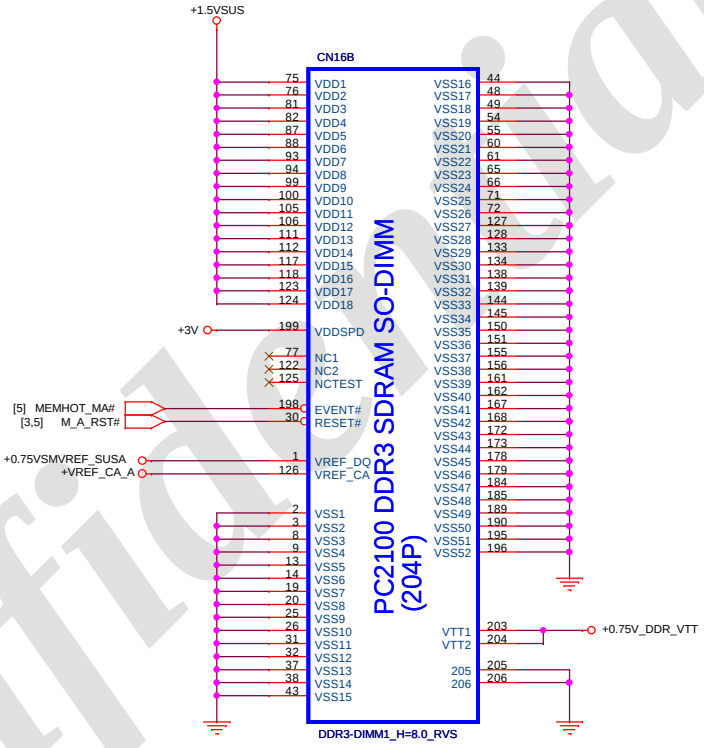
DDR3 (DDR)

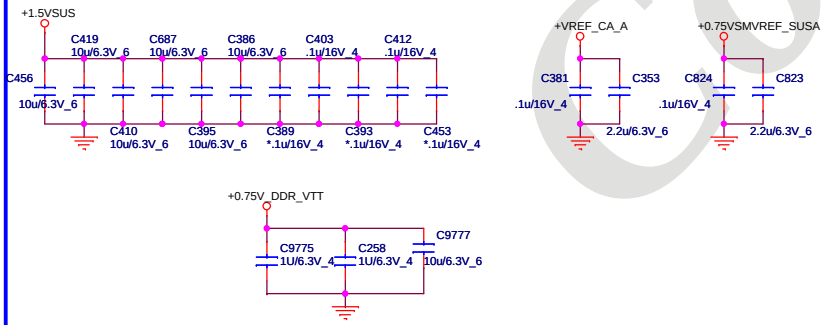




A52

2DIMM--->P/N:DGMK4000145

Place these Caps near So-Dimm0.



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Quanta Computer Inc.		
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ZR8 Schematic EC Tracking Record A (For A TEST) Nov.17 , 2009

EC / Page / Item / Description

A01 Page25/27/28/31/32/36/38/44 Change footprint , due to SMT open issue highlight.
A02 Page32 Change T/P switch P/N, due to SMT open issue highlight.
A03 Page42 Modify Madison-Pro & Park-XT VID table.
A04 Page14 Modify board ID table and R517,R304 support Side-port function.
A05 Page14 Add R528 support different Side-port VRAM type.
A06 Page44 Support CPU 45W solution.
A07 Page02 Change clock gen to no stuff, due to use internal clock source.
A08 Page06/07/48 Change SO-DIMM SMBUS address.
A09 Page08/10/11 Add Side-port function.
A10 Page10 Chane HDMI DDC CLK/DATA port.
A11 Page10 Stuff R190.
A12 Page12 Change dGPU_PWROK from GPIO1 to GPIO32.
A13 Page12 Change board ID GPIO pin.
A14 Page13 1. Stuff D19,R307,C538 and no stuff D18. 2. Change pull high power rail from +3V_D to +3V.
A15 Page16 Change R500 from 0ohm to 10k.
A16 Page12 Connect 25Mhz for GPU workaround design.
A17 Page18 Modify GPU Power-on sequence table.
A18 Page18 Remove GPU_IO VID contron pin and change GPU_CORE GPIO pin to GPIO15/20.
A19 Page19 Change R107 from 680ohm to 51 ohm and modify design of MEM_RST#. Also change R30 to no stuff.
A20 Page20/22/35/42 Reserve +3V_D_ZR8 power rail for GPU leakage issue.
A21 Page18 Reserve VGA_REQ# pin.
A22 Page25 Delete brightness switch IC control and change to 0ohm solution.
A23 Page25 Stuff R135,R144 ,due to some CRT monitor can't display.
A24 Page25 Stuff C776,C787 for EMI request.
A25 Page25/32 Change connect footprint and P/N.
A26 Page29/35 Add ODD power switch design and stuff R170.
A27 Page33 Change Q29,Q30 to no stuff.
A28 Page37/41/44 Remove jmuper.
A29 Page37 Change PC193 P/N to low highlimit, due to ME thermal door impact.
A30 Page38 Change PC179,PC180 from 22uF/25V to 100uF/25V.
A31 Page38 Change CPU_CORE enable from VRON to HWPG_2.5V.
A32 Page30 Change R538,R548 from 48ohm to 68ohm for audio performance.
A33 Page28 Change R572,R563 to short pad for debug use.
A34 Page20 Change +VGPU_IO power rail to +VGPU_CORE.
A35 Page25 Connect CN5 LCD connect shielding pin to GND for ESD issue.
A36 Page18 Change R65 to no stuff.
A37 Page22 Reserve OVERT# pull high resistor prevent noise.
A38 Page33 Add pull low 100k ohm for ODD_EJ,POWER_SAVE signal.
A39 Page36 Reserve cap for power team request.
A40 Page30 Stuff 0 ohm resistor for ESD protect use.
A41 Page02/03/10/11/15/18/20/21/27/30/32/35/36 Change bead P/N for EMI request, the reason is cost down and not STD parts.
A42 Page21 Reserve 0 ohm for PLL power use.
A43 Page38 Remove PR153 & change to 0402 package
A44 Page44 Change PR113 from 0 to 10K Ohm & Change enable source to +3V
A45 Page38/39/40/41 Stuff PR80,PR89,PR94,PR95,PR47 to 1 Ohm & PC47,PC51,PC64,PC65,PC36 of value to 1000p for EMI request
A46 Page36 Change PC111 of value to 1U/25V
A47 Page36 Change PR37 of value, from 33K to 150K
A48 Page36 Change PR35 of value, from 10K to 39K
A49 Page26 Change HDMI connector PN
A50 Page7 Change P/N for 3-DIMM H=4.0 STD
A51 Page6 Change P/N for 3-DIMM H=4.0 RVS
A52 Page48 Change P/N for 3-DIMM H=8.0 RVS
A53 Page36 Change battery connector P/N to DFHD08MR099
A54 Page26 Modify HDMI's I2C for DIS.

ZR8 Schematic EC Tracking Record A (For A TEST) Nov.17 , 2009
EC / Page / Item / Description

A55 Page14 Change board ID power rail from +3V_S5 to +3V.
A56 Page33/35 Modify WLAN RF_LED control design.
A57
A58 Page12 Remove R331 only for A11 version.
A59 Page12 Add U18,C533 & remove R303 for power sequence.
A60 Page14 Remove C760,C754,R507& Y7, due to it's for external clock use.
A61 Page2 Stuff R474,R486 for LAN & WLAN of REQ#.
A62 Page3/12 Stuff R424 and no stuff R286, due to CPU_PRPCHOT# is +1.5VSUS level.
A63 Page16 Change D29 package & Add D24.

Note : Change 0ohm to short pad
R276,R281,R415,R443,R445,R531,R532,R533,R534,R535,R539,R566,R174,R512,R513,R263,R437,R439,R441,R99

ZR8 Schematic EC Tracking Record B1 (For B1 TEST) Dec.09 , 2009
EC / Page / Item / Description

B01 Page21 Remove DP/TMDS Output Driver Analog Supply from port C&D. Due to it's don't to use.
B02 Page25 Stuff R48 for Discrete platform use.
B03 Page/10/25 Modify R signal pull low resistor value to 140ohm, due to keep 70 ohm trace impedance.
B04 Page33 Modify WLAN LED design and change from GPIO82 to GPIO84.
B05 Page27 Change LAN layout footprint for "SAW" new package.
B06 Page13/25 Reserve CCD USB host from for Port2, due to CCD issue.
B07 Page33 Reserve blue LED power source to 5V, due to White/Blue LED max Vf is more than Green/Orange LED.

ZR8 Schematic EC Tracking Record C (For C TEST) Jan.28 , 2010
EC / Page / Item / Description

C01 Page02/34 Remove "CPU_THERMTRIP#" control from SB820, due to BIOS don't support this function. Add another "SYS_SHDN#" for H/W shutdown function and add HWPG shutdown design.
C02 Page04 No stuff Q21,D14,R255 for thermal sensor Alert fnction and change to EC or H/W shutdown function.
C03 Page09 Add 1uF for monitor test noise issue.
C04 Page12 Add 0ohm to separate VGA_REQ function, due to it's don't support the function and cause by leakage current concern.
C05 Page24 Modify VGA note text for R signal impedance control.
C06 Page24 Add brightness switch control by iGPU switch mode. Due to BIOS for C test already support.
C07 Page29 Reserve EAPD# audio design for "Bo" sound.
C08 Page41 Change PG_GPUIO_EN pull high power rail from +3V to +3V_D_EXT. For Park GPU SG mode hang up issue.
C09 Page43 Change PR69 FROM 1.2K to 680ohm , the reason is for SDA high temperature (40 degree/20% humidity) auto shutdown issue.
C10 Page27 Short LPC signal for debug card use.
C11 Page29 Change R538,R548 from 56ohm to 68ohm for audio performance test FSOV spec requirement.
C12 Page42 Change PR113 from 10k to 0ohm.
C13 Page35 Change EC54,EC55 to stuff for ISN issue.
C14 Page21 Modify DDR3 Memory Aperture size table.
C15 Page03/40 Reserve VDDR_SENSE signal to controller IC.
C16 Page27 Change RP32 to no stuff.
C17 Page04 Modify CPU thermal control design from EC or BIOS control and change U16,R254 to no stuff ,Q17,Q18,Q19 to stuff.
C18 Page03 No stuff R189.

Note : Change 0ohm to short pad
R124,R121,R174,L31,L37,L35,R136,R115,R169,R325,R315,R295,R292,R278,R31,R90,R21,R112,R24,R25,R270,R530,R99,R478,R512,R513,R514,R326,R269,R268,R265,R266,R610,PR73,PR220,PR261
,PR229

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ZR8 Schematic EC Tracking Record A (For Ramp) Feb.25 , 2010

EC / Page / Item / Description

D01 Page03 Change CPU VDDR_SENSE pull high power rail to CPU_VDDR and remove trace connect to controller IC.

D02 Page15 Modify text note.

D03 Page12 Change "GBE_COL" ,"GBE_CRS" ,"GBE_RXERR" to GND follow SCL V1.04 version.

D04 Page14 Change USB PLL power rail source to separate VDDPL_33_USB_S follow SCL V1.04 version.

D05 Page04 No stuff R267,C450,C344.

D06 Page09 Delete R149,R152 layout pad.

D07 Page36 No stuff PD12 and add PR181, change PR257 from 1k to 390k. The purpose is for panasonic battery low power protect issue.

D08 Page05/46 No stuff R584,R259,R583,R586 for CKE signal.

D09 Page32 Change LED current sense resistor value for LED light measure requirement. (Follow ZR7B)

D10 Page21 Modify VRAM table.

D11 Page05/06 Change R123,R122,Q10,R202,R195,Q14 to no stuff, due to S1g4 don't support MEMHOT function.

D12 Page02 Reserve prochot# for FAN control.

D13 Page41 No stuff PR16,PQ4,PR3,PR12,PR5,PQ3. Due to MAX8792 had integrate discharge design.

D14 Page37 Change some component to no stuff, dut to for S1g4 use the same VDD power don't need to compensation difference voltage.

Note : Change 0ohm to hort pad.
R203,117,R585,R588,R260,R587,PR1,PR2,PR33,PR241,PR147,PR146,PR160,PR256,PR133,PR233,PR152,PR155,PR128,PR142,PR143,PR144,PR145,PR130,PR131,PR115,PR120,PR77,PR226,PR222,PR202,PR262.

	PROJECT : ZR8 Quanta Computer Inc.	
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