THOMSON

Service Manual

CHASSIS MT35

Contents

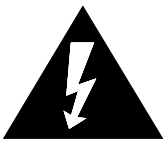
1. Caution……2
2. Product Specification……6
3. Test and Alignment……9
4. Main IC Brief Instruction

MT5335PU……16
MT5133……22
MT8295……24
WL6702F……25
WM8501……30
SiL9185A……33
RT8110……47
MP1411……50
TDA7266……54
AO4459……55
13N03LT……56
5. Block Diagram……57
6. Schematic Diagram……58
7. Exploded View

26E90……86
26E92……87
32E90……88
32E92……89

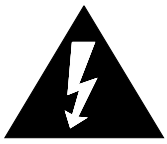
This manual is the latest at the time of printing, and does not include the modification which may be made after the printing, by the constant improvement of product.

1 **CAUTION:**
Use of controls, adjustments or procedures other than those specified herein may result in hazardous radiation exposure.



CAUTION
RISK OF ELECTRIC SHOCK DO NOT OPEN.

CAUTION: TO REDUCE THE RISK OF ELECTRICAL SHOCK, DO NOT REMOVE COVER (OR BACK). NO USER SERVICEABLE PARTS INSIDE. REFER SERVICING TO QUALIFIED SERVICE PERSONNEL.



The lighting flash with arrowhead symbol, with an equilateral triangle is intended to alert the user to the presence of uninsulated "dangerous voltage" within the product's enclosure that may be of sufficient magnitude to constitute a risk of electric shock to the person.

The exclamation point within an equilateral triangle is intended to alert the user to the presence of important operating and maintenance (servicing) instructions in the literature accompanying the appliance.

WARNING: TO REDUCE RISK OF FIRE OR ELECTRIC SHOCK, DO NOT EXPOSE THIS APPLIANCE TO RAIN OR MOISTURE.

IMPORTANT SAFETY INSTRUCTIONS

CAUTION:

Read all of these instructions. Save these instructions for later use. Follow all Warnings and Instructions marked on the audio equipment.

1. Read Instructions- All the safety and operating instructions should be read before the product is operated.
2. Retain Instructions- The safety and operating instructions should be retained for future reference.
3. Heed Warnings- All warnings on the product and in the operating instructions should be adhered to.
4. Follow Instructions- All operating and use instructions should be followed.

FOR YOUR PERSONAL SAFETY

1. When the power cord or plug is damaged or frayed, unplug this television set from the wall outlet and refer servicing to qualified service personnel.
2. Do not overload wall outlets and extension cords as this can result in fire or electric shock.
3. Do not allow anything to rest on or roll over the power cord, and do not place the TV where power cord is subject to traffic or abuse. This may result in a shock or fire hazard.
4. Do not attempt to service this television set yourself as opening or removing covers may expose you to dangerous voltage or other hazards. Refer all servicing to qualified service personnel.
5. Never push objects of any kind into this television set through cabinet slots as they may touch dangerous voltage points or short out parts that could result in a fire or electric shock. Never spill liquid of any kind on the television set.
6. If the television set has been dropped or the cabinet has been damaged, unplug this television set from the wall outlet and refer servicing to qualified service personnel.
7. If liquid has been spilled into the television set, unplug this television set from the wall outlet and refer servicing to qualified service personnel.
8. Do not subject your television set to impact of any kind. Be particularly careful not to damage the picture tube surface.
9. Unplug this television set from the wall outlet before cleaning. Do not use liquid cleaners or aerosol cleaners. Use a damp cloth for cleaning.

10.1. Do not place this television set on an unstable cart, stand, or table. The television set may fall, causing serious injury to a child or an adult, and serious damage to the appliance. Use only with a cart or stand recommended by the manufacturer, or sold with the television set. Wall or shelf mounting should follow the manufacturer's instructions, and should use a mounting kit approved by the manufacturer.

10.2. An appliance and cart combination should be moved with care. Quick stops, excessive force, and uneven surfaces may cause the appliance and cart combination to overturn.

PROTECTION AND LOCATION OF YOUR SET

11. • Do not use this television set near water ... for example, near a bathtub, washbowl, kitchen sink, or laundry tub, in a wet basement, or near a swimming pool, etc.
    • Never expose the set to rain or water. If the set has been exposed to rain or water, unplug the set from the wall outlet and refer servicing to qualified service personnel.

12. Choose a place where light (artificial or sunlight) does not shine directly on the screen.

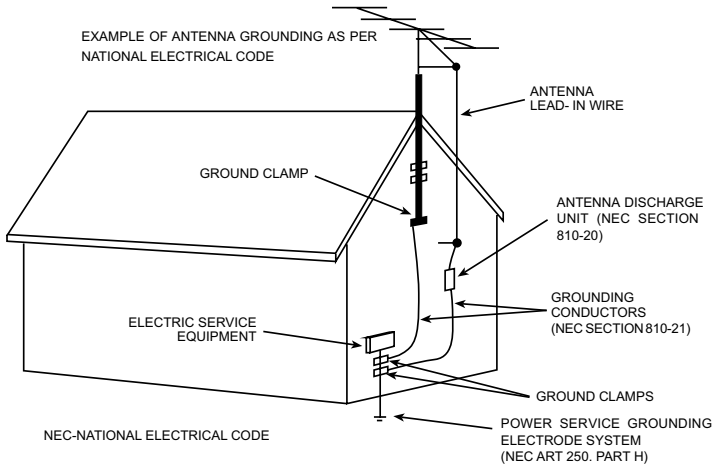
13. Avoid dusty places, since piling up of dust inside TV chassis may cause failure of the set when high humidity persists.

14. The set has slots, or openings in the cabinet for ventilation purposes, to provide reliable operation of the receiver, to protect it from overheating. These openings must not be blocked or covered.
    • Never cover the slots or openings with cloth or other material.
    • Never block the bottom ventilation slots of the set by placing it on a bed, sofa, rug, etc.
    • Never place the set near or over a radiator or heat register.
    • Never place the set in a "built-in" enclosure, unless proper ventilation is provided.

PROTECTION AND LOCATION OF YOUR SET

15.1. If an outside antenna is connected to the television set, be sure the antenna system is grounded so as to provide some protection against voltage surges and built up static charges, Section 810 of the National Electrical Code, NFPA No. 70-1975, provides information with respect to proper grounding of the mast and supporting structure, grounding of the lead-in wire to an antenna discharge unit, size of grounding conductors, location of antenna discharge unit, connection to grounding electrode, and requirements for the grounding electrode.

EXAMPLE OF ANTENNA GROUNDING AS PER NATIONAL ELECTRICAL CODE INSTRUCTIONS



15.2. Note to CATV system installer : (Only for the television set with CATV reception)

This reminder is provided to call the CATV system installer's attention to Article 820-40 of the NEC that provides guidelines for proper grounding and, in particular, specifies that the cable ground shall be connected to the grounding system of the building, as close to the point of cable entry as practical.

16. An outside antenna system should not be located in the vicinity of overhead power lines or other electric lights or power circuits, or where it can fall into such power lines or circuits. When installing an outside antenna system, extreme care should be taken to keep from touching such power lines or circuits as contact with them might be fatal.

17. For added protection for this television set during a lightning storm, or when it is left unattended and unused for long periods of time, unplug it from the wall outlet and disconnect the antenna. This will prevent damage due to lightning and power-line surges.

OPERATION OF YOUR SET

18. This television set should be operated only from the type of power source indicated on the marking label. If you are not sure of the type of power supply at your home, consult your television dealer or local power company. For television sets designed to operate from battery power, refer to the operating instructions.
19. If the television set does not operate normally by following the operating instructions, unplug this television set from the wall outlet and refer servicing to qualified service personnel. Adjust only those controls that are covered in the operating instructions as improper adjustment of other controls may result in damage and will often require extensive work by a qualified technician to restore the television set to normal operation.
20. When going on a holiday : If your television set is to remain unused for a period of time, for instance, when you go on a holiday, turn the television set "off" and unplug the television set from the wall outlet.

IF THE SET DOES NOT OPERATE PROPERLY

21. If you are unable to restore normal operation by following the detailed procedure in your operating instructions, do not attempt any further adjustment. Unplug the set and call your dealer or service technician.
22. Whenever the television set is damaged or fails, or a distinct change in performance indicates a need for service, unplug the set and have it checked by a professional service technician.
23. It is normal for some TV sets to make occasional snapping or popping sounds, particularly when being turned on or off. If the snapping or popping is continuous or frequent, unplug the set and consult your dealer or service technician.

FOR SERVICE AND MODIFICATION

24. Do not use attachments not recommended by the television set manufacturer as they may cause hazards.
25. When replacement parts are required, be sure the service technician has used replacement parts specified by the manufacturer that have the same characteristics as the original part. Unauthorized substitutions may result in fire, electric shock, or other hazards.
26. Upon completion of any service or repairs to the television set, ask the service technician to perform routine safety checks to determine that the television is in safe operating condition.

MT35-EU Product Specification

Model #	22E92NH22	26E90NH22	26E92NH22	32E90NH22	32E92NH22
Brand	THOMSON	THOMSON	THOMSON	THOMSON	THOMSON
Panel technology (LCD / PDP)	LCD	LCD	LCD	LCD	LCD
Cabinet Design (Example: SC VII, V 6,,,)	E9B	E9A	E9B	E9A	E9B
PJO Nb	22E92	26E90	26E92	32E90	32E92
EAN Code	3244480284643	3244480284629	3244480284636	3244480284445	3244480284612
Chassis name	MT5335	MT5335	MT5335	MT5335	MT5335
Certification(Gostandard/CE/MPTT/…)	CE	CE	CE	CE	CE
COUNTRIES					
France	Yes	Yes	Yes	Yes	Yes
Germany	Yes	Yes	Yes	Yes	Yes
Italy, Greece	Yes	Yes	Yes	Yes	Yes
Spain, Portugal	Yes	Yes	Yes	Yes	Yes
Benelux (Belgium, Netherland, Luxemburg)	Yes	Yes	Yes	Yes	Yes
Northern Europe (Sweden, Norway, Denmark, Finland)	Yes	Yes	Yes	Yes	Yes
Eastern Europe (Russia, Poland, Czech, Hungary)	Yes	Yes	Yes	Yes	Yes
PICTURE					
Screen size : diagonale (inch)	22"	26"	26"	32"	32"
Aspect ratio (16/9 // 4/3 // 15/9)	16/9	16/9	16/9	16/9	16/9
Color depth (8/10/12 bits)	8	8	8	8	8
1st panel supplier : panel suppliers	AUO	CMO	CMO	LG-Philips	LG-Philips
1st panel supplier : panel reference	T220SW01 V0	V260B1-L02	V260B1-L02	LC320WXN-SAC1	LC320WXN-SAC1
1st panel supplier : resolution	1680x1050	1366x768	1366x768	1366x768	1366x768
1st panel supplier : pixel Pitch (mmxmm)	0.282x0.282	0.1405x0.4215	0.1405x0.4215	0.17x0.51	0.17x0.51
1st panel supplier : Horizontal and vertical viewing angle	170(H)/160(V)	160(H)/150(V)	160(H)/150(V)	178(H)/178(V)	178(H)/178(V)
1st panel supplier : Typical response time (Grey to Grey)	5mS	8mS	8mS	8mS	8mS
1st panel supplier : Typical white luminance (Nits)	300	400	400	500	500
1st panel supplier : Contrast VESA std	1000:1	800:1	800:1	1100:1	1100:1
1st panel supplier : Typical panel Life Time (Hours)	50000	50000	50000	50000	50000
VIDEO					
Noise Reduction (adaptative/…)	Yes	Yes	Yes	Yes	Yes
Comb Filter (2D/3D)	3D	3D	3D	3D	3D
Deinterlacer (no/linerar/motion adaptive/motion compensative)	Frame buffer	Frame buffer	Frame buffer	Frame buffer	Frame buffer
Film mode / reverse 3:2 pull down	Yes/Yes	Yes/Yes	Yes/Yes	Yes/Yes	Yes/Yes
Format control (Pin8/WSS)	Yes/Yes	Yes/Yes	Yes/Yes	Yes/Yes	Yes/Yes
Zoom type : 4/3 format	Yes	Yes	Yes	Yes	Yes
Zoom type : 14/9 Zoom	Yes	Yes	Yes	Yes	Yes
Zoom type : 16/9 Zoom	Yes	Yes	Yes	Yes	Yes
Zoom type : 16/9 Zoom up/down	Yes	Yes	Yes	Yes	Yes
Zoom type : Cinerama	Yes	Yes	Yes	Yes	Yes
Zoom type : 16/9Format	Yes	Yes	Yes	Yes	Yes
Colour preset (Cool/Normal/Warm/Favourite)	Cool/Normal/Warm	Cool/Normal/Warm	Cool/Normal/Warm	Cool/Normal/Warm	Cool/Normal/Warm
Contrast expend (low/medium/high)	high	high	high	high	high
Picture Reset	Yes	Yes	Yes	Yes	Yes
Backlight Adjust	on factory menu	on factory menu	on factory menu	on factory menu	on factory menu
Dynamic Contrast	Dynamic Backlight adjustment	Dynamic Backlight adjustment	Dynamic Backlight adjustment	Dynamic Backlight adjustment	Dynamic Backlight adjustment
Picture Autoadjustment (PC mode)	Yes	Yes	Yes	Yes	Yes
Picture presets : Standard / Film / Studio / Sport / Personal / Game / Video Camera	Vivid/Standard /Movie/ Power saver/ Personal	Vivid/Standard /Movie/ Power saver/ Personal	Vivid/Standard /Movie/ Power saver/ Personal	Vivid/Standard /Movie/ Power saver/ Personal	Vivid/Standard /Movie/ Power saver/ Personal
Sound					
RMS Power (Watt)	2x3W	2x6W	2x6W	2x6W	2x6W
Treble, Bass, Balance, Volume, Mute Control	Yes/Yes/Yes/Yes/Yes	Yes/Yes/Yes/Yes/Yes	Yes/Yes/Yes/Yes/Yes	Yes/Yes/Yes/Yes/Yes	Yes/Yes/Yes/Yes/Yes
Sound presets (My sound/Music/Film/Voice/Flat/Standard/Panorama)	personal/speech/music/movies/Multimedia	personal/speech/music/movies/Multimedia	personal/speech/music/movies/Multimedia	personal/speech/music/movies/Multimedia	personal/speech/music/movies/Multimedia
Sound techno (Stereo Nicam/Virtual Dolby Surround/SRS Trusurround XT/BBE Viva/SRS WoW /…)	NICAM,German Stereo/AVL/Wide stereo/Visually Impaired	NICAM,German Stereo/AVL/Wide stereo/Visually Impaired	NICAM,German Stereo/AVL/Wide stereo/Visually Impaired	NICAM,German Stereo/AVL/Wide stereo/Visually Impaired	NICAM,German Stereo/AVL/Wide stereo/Visually Impaired
Loudspeakers built in (T/M/B)	-/2/-	-/2/-	-/2/-	-/2/-	-/2/-
Decoding capability					
Standard	BG/DK/I/LL`	BG/DK/I/LL`	BG/DK/I/LL`	BG/DK/I/LL`	BG/DK/I/LL`

Color System (PAL/SECAM/NTSC)	PAL/SECAM/NTSC(AV)	PAL/SECAM/NTSC(AV)	PAL/SECAM/NTSC(AV)	PAL/SECAM/NTSC(AV)	PAL/SECAM/NTSC(AV)
DVBT (yes/no)	Yes(MPEG 2)	Yes(MPEG 2)	Yes(MPEG 2)	Yes(MPEG 2)	Yes(MPEG 2)
Video standard NTSC 3.58 / 4.43 (AV)	Yes	Yes	Yes	Yes	Yes
HD capability	YES (720p, 1080i; 1080P 480i/p; 576i/p)	YES (720p, 1080i; 1080P 480i/p; 576i/p)	YES (720p, 1080i; 1080P 480i/p; 576i/p)	YES (720p, 1080i; 1080P 480i/p; 576i/p)	YES (720p, 1080i; 1080P 480i/p; 576i/p)
PC capability (up to maximum format)	UXGA	UXGA	UXGA	UXGA	UXGA
User convenience					
IB languages	English\Czech\German\Spanish\Finnish\French\Greek\Hungarian\Italian\Dutch\Polish\Portuguese\Russian\Swedish\Slovak\Ukrainian\Estonian\Latvian\Lithuanian\Turkish\Norwegian	English\Czech\German\Spanish\Finnish\French\Greek\Hungarian\Italian\Dutch\Polish\Portuguese\Russian\Swedish\Slovak\Ukrainian\Estonian\Latvian\Lithuanian\Turkish\Norwegian	English\Czech\German\Spanish\Finnish\French\Greek\Hungarian\Italian\Dutch\Polish\Portuguese\Russian\Swedish\Slovak\Ukrainian\Estonian\Latvian\Lithuanian\Turkish\Norwegian	English\Czech\German\Spanish\Finnish\French\Greek\Hungarian\Italian\Dutch\Polish\Portuguese\Russian\Swedish\Slovak\Ukrainian\Estonian\Latvian\Lithuanian\Turkish\Norwegian	English\Czech\German\Spanish\Finnish\French\Greek\Hungarian\Italian\Dutch\Polish\Portuguese\Russian\Swedish\Slovak\Ukrainian\Estonian\Latvian\Lithuanian\Turkish\Norwegian
Program Numbers (example: 99+3AV)	999+1AV+1SVIDEO+1CMP+1VGA+2HDMIs+1SCART	999+1AV+1SVIDEO+1CMP+1VGA+2HDMIs+1SCART	999+1AV+1SVIDEO+1CMP+1VGA+2HDMIs+1SCART	999+1AV+1SVIDEO+1CMP+1VGA+2HDMIs+1SCART	999+1AV+1SVIDEO+1CMP+1VGA+2HDMIs+1SCART
Number of buttons on cabinet (Power; Vol+/-; Pr+/-, Menu)	Power, CH +/–, Vol +/–, Menu	Power, CH +/–, Vol +/–, Menu	Power, CH +/–, Vol +/–, Menu	Power, CH +/–, Vol +/–, Menu	Power, CH +/–, Vol +/–, Menu
Main switch button (yes/no)	No	No	No	No	No
Clock	Yes	Yes	Yes	Yes	Yes
Sleep timer	Yes	Yes	Yes	Yes	Yes
wake-up timer	Yes	Yes	Yes	Yes	Yes
Parent Control - Channel lock (Input code for certain channel)	Yes	Yes	Yes	Yes	Yes
Parent Control - Child lock (set the lock of the keyboard, only the RCU can control the TV)	No	No	No	No	No
Parent Control - Kid pass (preset the ontime, channel for each day of the week)	No	No	No	No	No
Parent Control - Channel lock (For digital transmission and DVD program, to filter some programms)	No	No	No	No	No
Program auto switch off	Yes	Yes	Yes	Yes	Yes
OSD Language*	Bulgarian\Czech\Danish\German\Greek\English\Spanish\French\Croatian\Italian\Hungarian\Dutch\Norwegian\Polish\Portuguese\Romanian\Russian\Slovak\Slovenian\Serbian\Finnish\Swedish\Turkish	Bulgarian\Czech\Danish\German\Greek\English\Spanish\French\Croatian\Italian\Hungarian\Dutch\Norwegian\Polish\Portuguese\Romanian\Russian\Slovak\Slovenian\Serbian\Finnish\Swedish\Turkish	Bulgarian\Czech\Danish\German\Greek\English\Spanish\French\Croatian\Italian\Hungarian\Dutch\Norwegian\Polish\Portuguese\Romanian\Russian\Slovak\Slovenian\Serbian\Finnish\Swedish\Turkish	Bulgarian\Czech\Danish\German\Greek\English\Spanish\French\Croatian\Italian\Hungarian\Dutch\Norwegian\Polish\Portuguese\Romanian\Russian\Slovak\Slovenian\Serbian\Finnish\Swedish\Turkish	Bulgarian\Czech\Danish\German\Greek\English\Spanish\French\Croatian\Italian\Hungarian\Dutch\Norwegian\Polish\Portuguese\Romanian\Russian\Slovak\Slovenian\Serbian\Finnish\Swedish\Turkish
OSD Positioning	No	No	No	No	No
OSD Transparency Adjust	No	No	No	No	No
OSD Timeout Adjust	No	No	No	No	No
Text Standard: (Top, FLOF,,,)	TOP & FLOF	TOP & FLOF	TOP & FLOF	TOP & FLOF	TOP & FLOF
Teletext Level: 2.5 / 1.5	1.5	1.5	1.5	1.5	1.5
Pages for teletext	1000	1000	1000	1000	1000
Teletext character sets ****	Latin Pan-Euro West Latin Pan-Euro East Cyrillic（Russia-Bulgarian/Ukrainian/Byelorussia） Greek Arabic	Latin Pan-Euro West Latin Pan-Euro East Cyrillic（Russia-Bulgarian/Ukrainian/Byelorussia） Greek Arabic	Latin Pan-Euro West Latin Pan-Euro East Cyrillic（Russia-Bulgarian/Ukrainian/Byelorussia） Greek Arabic	Latin Pan-Euro West Latin Pan-Euro East Cyrillic（Russia-Bulgarian/Ukrainian/Byelorussia） Greek Arabic	Latin Pan-Euro West Latin Pan-Euro East Cyrillic（Russia-Bulgarian/Ukrainian/Byelorussia） Greek Arabic
TV Guide	Yes	Yes	Yes	Yes	Yes
Auto Naming/Auto Sorting	Yes/Yes	Yes/Yes	Yes/Yes	Yes/Yes	Yes/Yes
Auto update (for DVBT software ugrades)	No	No	No	No	No
Multipicture : PIP (Double Tuner) / PIP (AV) / PAP / PAT / PIC	only PAT	only PAT	only PAT	only PAT	only PAT
Hotel mode (Y/N)	No	No	No	No	No
Tuner FM (yes/no)	Yes(in DVB-T)	Yes(in DVB-T)	Yes(in DVB-T)	Yes(in DVB-T)	Yes(in DVB-T)
Connectors (if possible, please indicate the position)					
RF Input (Antenna): Analogical / Digital	2 in 1	2 in 1	2 in 1	2 in 1	2 in 1
Scart 1 : CVBS / RGB / S-VIDEO	1/1/-	1/1/-	1/1/-	1/1/-	1/1/-
CINCH audio in / out (No volumpe control on Audio out/can be jack 3,5mm)	1(side)/-	1(side)/-	1(side)/-	1(side)/-	1(side)/-
CINCH video in / out	1(side)/-	1(side)/-	1(side)/-	1(side)/-	1(side)/-
S-video in / out	1(side)/-	1(side)/-	1(side)/-	1(side)/-	1(side)/-

Component Video Input (YCrCb/YPrPb)	1(rear)	1(rear)	1(rear)	1(rear)	1(rear)
Component Audio Input (YCrCb/YPrPb)	1(rear)	1(rear)	1(rear)	1(rear)	1(rear)
VGA in / Audio L/R in / Jack audio in 3.5mm	1/-/1	1/-/1	1/-/1	1/-/1	1/-/1
HDMI1.3	2(1.3)	2(1.3)	2(1.3)	2(1.3)	2(1.3)
DVI-HDCP	Share with HDMI	Share with HDMI	Share with HDMI	Share with HDMI	Share with HDMI
Audio input for DVI – HDCP	share with VGA	share with VGA	share with VGA	share with VGA	share with VGA
CINCH subwoofer out / Coaxial out (SP-DIF)	-/Yes	-/Yes	-/Yes	-/Yes	-/Yes
Headphone connector (mm)	3.5mm,x1 (side)	3.5mm,x1 (side)	3.5mm,x1 (side)	3.5mm,x1 (side)	3.5mm,x1 (side)
RS232 (Y/N)	share with VGA	share with VGA	share with VGA	share with VGA	share with VGA
USB slot (NO/1.1/2)	Yes(only for SW update)	Yes(only for SW update)	Yes(only for SW update)	Yes(only for SW update)	Yes(only for SW update)
DVB-CI (common interface)	Yes	Yes	Yes	Yes	Yes
Accessories included					
Remote control reference	RC1994906	RC1994906	RC1994906	RC1994906	RC1994906
Carton (English/French/Spanish)	Yes(English)	Yes(English)	Yes(English)	Yes(English)	Yes(English)
Batteries	Yes	Yes	Yes	Yes	Yes
IB	Yes	Yes	Yes	Yes	Yes
Product registration Card	No	No	No	No	No
AC power cords	1	1	1	1	1
Audio Cord (Cinch to Jack 3.5mm)	No	No	No	No	No
VGA Cord	No	No	No	No	No
Wallmount	No	No	No	No	No
Antenna Cable	No	No	No	No	No
General Data					
Size (W x H x D, with stand) in mm	529x439x180	663x504x205	663x504x205	796x582x230	796x582x230
Size (W x H x D, without stand) in mm	529x403x73.5	663x461x108	663x461x108	796x535x102	796x535x102
Package Size (W x H x D, with stand but not mount) in mm	640x520x202	771x548x237	771x548x237	915x652x249	915x652x249
Net Weight in kg	4.9	12	12	15.5	15.5
Gross Weight in Kg	7	14	14	18	18
Power supply	220-240V 50HZ	220-240V 50HZ	220-240V 50HZ	220-240V 50HZ	220-240V 50HZ
Power consumption working / standby / Annual	53W/1W/85KWH	85W/<1W/132KWH	85W/<1W/132KWH	130W/<1W/197KWh	130W/<1W/198KWh
Design / Mechanical					
Wallmount VESA compatible (standard reference)	VESA compatible	VESA compatible	VESA compatible	VESA compatible	VESA compatible
Wallmount VESA Size	100mmx100mm	100mmx100mm	100mmx100mm	200mmx100mm	200mmx100mm
Adaptor for VESA wallmount compatibility (accessory ref)	No	No	No	No	No
Desktop Stand (included/optionnal + ref/NO)	Yes	Yes	Yes	Yes	Yes
Panel Tilt (Fowards/Backwards/Rotation)	No	No	No	No	No
Swivel function desktop stand (yes/no) + motorized?	No	No	No	No	No
Docking station (yes/no)	No	No	No	No	No
Floor Stand (included/optionnal + ref/NO)	No	No	No	No	No
Glass shield (yes/no)	No	No	No	No	No
Finish on Front	HG Spray paint(Black Q8257)	Half translucent as moulded (high glossy black)	HG Spray paint(Black Q8257)	Half translucent as moulded (high glossy black)	HG Spray paint(Black Q8257)
Finish on side	Black A8252 as moulded	Black A8252 as moulded	Black A8252 as moulded	Black A8252 as moulded	Black A8252 as moulded
Finish on back	Black A8252 as moulded	Black A8252 as moulded	Black A8252 as moulded	Black A8252 as moulded	Black A8252 as moulded
Finish on stand	HG Spray paint(Black Q8257)	HG Spray paint(Black Q0003)	HG Spray paint(Black Q8257)	HG Spray paint(Black Q0003)	HG Spray paint(Black Q8257)
number of colors on carton box	1	1	1	1	1
Brand logo	THOMSON	THOMSON	THOMSON	THOMSON	THOMSON
External AC/DC Power with DC power cord (yes/no)	No/No grounded plug	No/No grounded plug	No/No grounded plug	No/No grounded plug	No/No grounded plug
Number of Speaker	2	2	2	2	2
Rating Label langages	DE, FR, IT, ES, EN, PL, CS, HU, RU, PT, EL, NL, SV, DA, FI, NO	DE, FR, IT, ES, EN, PL, CS, HU, RU, PT, EL, NL, SV, DA, FI, NO	DE, FR, IT, ES, EN, PL, CS, HU, RU, PT, EL, NL, SV, DA, FI, NO	DE, FR, IT, ES, EN, PL, CS, HU, RU, PT, EL, NL, SV, DA, FI, NO	DE, FR, IT, ES, EN, PL, CS, HU, RU, PT, EL, NL, SV, DA, FI, NO
Rating Label Logos/Icons (GOST, Bin, Recycling, Caution, …)	CE, GOST, Recycling, Class II,DTB, WEEE bin, Caution	CE, GOST, Recycling, Class II,DTB, WEEE bin, Caution	CE, GOST, Recycling, Class II,DTB, WEEE bin, Caution	CE, GOST, Recycling, Class II,DTB, WEEE bin, Caution	CE, GOST, Recycling, Class II,DTB, WEEE bin, Caution

Test and Alignment Specification for MT35-V0.20

The **xxE90/E92NH22** models are Europe LCD platform with DVB-T designed for driving below panels:

- 32” LPL (LVDS)
- 26” CMO(LVDS)
- 22” AUO(DUAL LVDS)

The main chip is from Mediatec (MTK5335 series) and supports below inputs:

- one analog and digital mixed RF (PAL B/G D/K I, SECAM B/G D/K L/L’,DVB-T)
- one SCART (CVBS & RGB)
- one CMP (YPrPb can support from 480i up to 1080p)
- one VGA
- two HDMI (can support 480i/p, 576i/p, 720p up to 1080i/p) compliant v1.2. with HDCP, audio included as EIA-861B standard
- one S-Video input
- one Headphone output
- one SPDIF output

More relevant details are listed into the Spec.

INFO:

↳ All tests and measurements mentioned hereafter have to be carried out at a normal mains voltage (**110 ~ 240 VAC**)
↳ All voltages have to be measured with respect to ground, unless otherwise stated
↳ All final tests have to be done on a complete set including LCD panel in a room with temperature of **25+/-7°C**
↳ The White Balance (color temperature) has to be performed into subdued lighted room after at least **1 hour** of warm-up/burn-in. This is applicable for both Alignment and Picture Performance evaluation at OQA in order to be set free of any temperature drift (colorimetry vs time)

1. Electrical Assembly Alignment

1.1. *Preconditions – DC/DC Check*

Before Power On the chassis, please check and make sure that U801,U802,U805, U809, U803, U804, U811,U201,C817(positive) outputs are not shorted to ground.
Supply 12v and 5v to P804 and test the relative voltage.

position	value
U811	3.3V +/-5%
U801	3.3V +/-5%
U802	9V +/-5%
U803	1.2V +/-5%
U804	2.5V +/-5%
U805	5V +/-5%
U809	3.3V +/-5%

U201	2.6V +/-5%
C817(+)	1.19V +/-5%

Download latest release MCU_SW into the Standby CPU(U810) using WT_MCU_ISP SW tool. See Appendix❶ "**How to download MCU SW**".
Download latest release SW into the flash using MTK SW tool. See Appendix❷ "**How to download FLASH SW**". Or download the SW from USB port.

1.2. Functional Test

Once the boards (chassis, FAV, KB, IR, PSU…) and the panel are well interconnected, connect all external generator devices to relevant inputs/outputs below according to their respective test patterns format and check picture content and sound quality accordingly:

Source	**Test signal** (generator)	**Test pattern** (format/image)
Analog /Digital Tuner	RF cable	Full Band (VHF/UHF) + CATV DVB-T
SCART1 (CVBS)	Chroma/Fluke	PAL Half Color & Gray bars
Side av (cvbs)– SVideo(Y/C)	Chroma/Fluke	PAL Half Color & Gray bars
SCART1 (RGB)	Chroma/Fluke	Half Color & Gray bars
SCART1 (CVBSOut)	RF cable	First channel
HDMI	DVD with HDMI compliancy	Movie 720p@60Hz
VGA	Chroma/QuantumData	1024x768@60Hz Half Color & Gray bars
Headphone	RF cable	First channel
Loud Speakers	RF cable	First channel
CMP (YPrPb)	Chroma/QuantumData	1080i@60Hz Half Color & Gray bars

Audio tones can be defined by the factory (ie: 1KHz & 3KHz, sweep, …).
Picture video formats can be changed by the factory according to their own standard.

1.3. ADC Calibration

Two inputs require an ADC calibration for the time being, That are:

- **VGA**

Provide a test signal **1024×768@60Hz** with **White Black squares**.
Select the corresponding "**Auto Color**" submenu item from "**Factory Menu**", then press "**OK**" to start.
When VGA channel is aligned, SCART-RGB is also aligned, so it is not necessary for RGB to be separately aligned.

- **CMP**

Provide a test signal **576i@50Hz** with **100% 8 steps Color Bar**.
Select the corresponding "**Auto Color**" submenu item from "**Factory Menu**", then press "**OK**" to start.

The ADC is well performed when it's displayed "**CMP**" after few seconds.

1.4. DDC & EDID Test

The E-EDID data structure are according to VESA Enhanced EDID 1.3 (and EIA/CEA-861B for HDMI).
Both VGA and HDMI have their own separate bin files:
For EDID check, it's needed to check whether the correct EDID is downloaded by checking corresponding EDID NVM Checksum or read them out to check bit by bit if it is in line with the released EDID bin file.

- ****Before check the EDID please ensure the "Factory Key" in factory menu is *disabled***

1.5. HDCP Test

For HDCP compliancy, it's needed to check whether the HDCP key has been well set.

2. Final Assembly Alignment

2.1. Entering to "Factory Menu"

To enter into Factory Menu in case of "**Factory Key**" is *disabled*, please to follow below steps:
- press Remote Control key "**MENU**" to display main menu
- press the subsequence Remote Control keys "**7**", "**9**", "**1**" and "**5**"
- press Remote Control key "**MENU**" to exit main menu
- press Remote Control key "**MENU**" to display main menu again

The main menu will display "**FACTCORY**" at the last item
To pop-up Factory Menu in case of "**Factory Key**" is *enabled*, please to follow below step:
- press Remote Control key "**Blue**"

To *enable/disable* "**Factory Key**", please to follow below steps:
- press Remote Control "**OK**" key to enter into "System" submenu
- press Remote Control "**RIGHT** "or "**LEFT**" key till "**Factory Key**" item
- press Remote Control "**OK**" key to toggle mode

To exit "**Factory Menu**", press "**Exit**" key from Remote Control.
To comeback to "**Factory Menu**" root when you are into a submenu:
- press Remote Control "**RED**" key.

2.2. Entering to "P" Mode

To enter into "**P**" mode, an external serial 3.3VDC device is required for sending relevant commands. See appendix❸ "**Serial Command Protocol for MTKxx**".

2.3. White Balance Alignment

Only **VGA** input requires color temperature adjustment as all other inputs or relative ones. Both **Warm** and **Cool** Color Coordinates are also relatives to **Normal** Color Temperature mode ones. See appendix❹ "**CVBS/RGB/CMP/HDMI Relative Matrix Offsets**" and "**WARM/COOL Relative**

Matrix Offsets". Those offsets values don't require any alignment but can be fine-tuned in Factory Menu as well.
<The appendix is just a template, Every lot the relative offset is different. We need to align 5 sets first to get the relative offset data every lot. >

- **Expected Targets and Tolerances**

The measured parameters should be "x, y" coordinates.

The White Balance alignment should be performed using a contact less analyzer (ei: Minolta CA-210). The analyzer may not touch the screen surface, and measurement must be performed in a dark environment keeping the probe(s) at 90+/-2° from the panel.

The alignment has to fulfill the requirements in Application Form.

2.4. High Pot. and Insulating Resistance Tests

At the end of the process, a High Pot. and an Insulating Resistance tests are required for matching Safety Electrical requirements (ei: xxxx)

- **High Voltage Withstanding requirements**

- "Voltage" ⇨ **4240 VDC**
- "Max Leakage Current" ⇨ **1 mA**
- "Test Time" ⇨ **3 sec**

- **Insulating Resistance requirements**

- "Voltage" ⇨ **DC500V**
- "Threshold Max" ⇨
- "Threshold Min" ⇨ **4MΩ**
- "Test Time" ⇨ **3 sec**

3. "Factory Menu" Definition

1). System

Item	Sub-item	
	Factory Key	OFF： Factory Key is invalidation ON ： Factory Key is availability, and BLUE key is the shortcut key. Note: option step 1） Enter menu 2） 7915 3） Exit/Enter menu 4） Enter Factory Item Enter Factory menu .(Or Enter Factory mode by hotkey)
	Burning Mode	Off/On
	Power Mode	Boot/Standby/Previous Boot: Enter power on mode Standby: Enter standby mode

		Previous: power on according to last status
	Pre- frequency table	HuiZhou/ Poland Note:Pre-Frequency table(HuiZhou/ Poland)
	Reset	Reset EEPROM data, and load the default value of EEPROM All: clear NVM values， and set to default value。 User: Clear date of NVM in user menu, except the value of language / related installation/Factory setting, then set to the default value. Shop: Clear date of NVM in user menu, include the value related installation, and Clear date of factory menu except the item of Balance and sound ,set to default value
	TECI command	Note:Priority below basic function of Factory menu

2). Balance

Item	Sub-item	
Balance	Source	For balance source Note:Switch SOURCE used left/right key
	Tone	Normal/Warm/Cool Note: RGB gain range is 0-255 The value of Warm and cool is the offset of Normal mode, their range is -128－127, if the offset value beyond the boundary， set to max or min value.
	Auto Color	Note:display the completed source name on the right of item,If all the sourcs is ok ,show “All”
	White R	R White balance
	White G	G White balance
	White B	B White balance
	Gray R	R Gray balance
	Gray G	G Gray balance
	Gray B	B Gray balance

3). Sound Volume Curve

Item	Sub-item		
Sound	VOL_0	0	
	VOL_10	2	
	VOL_50	14	Note:mapping volume value to 0—255 of the MCU register
	VOL_90	135	
	VOL_100	255	

	TV Pre	186	
	AV Pre	186	

4). INFO SW version information

Info	Project	LCD_5335_TCL
	MTK Version	XXXXXX
	Version	IDTV-XXXXXX_XX
	DATE	2008-XX-XX

5). Factory default settings

Followed as OOB setting.

Appendix ❶ "How to download MCU SW"

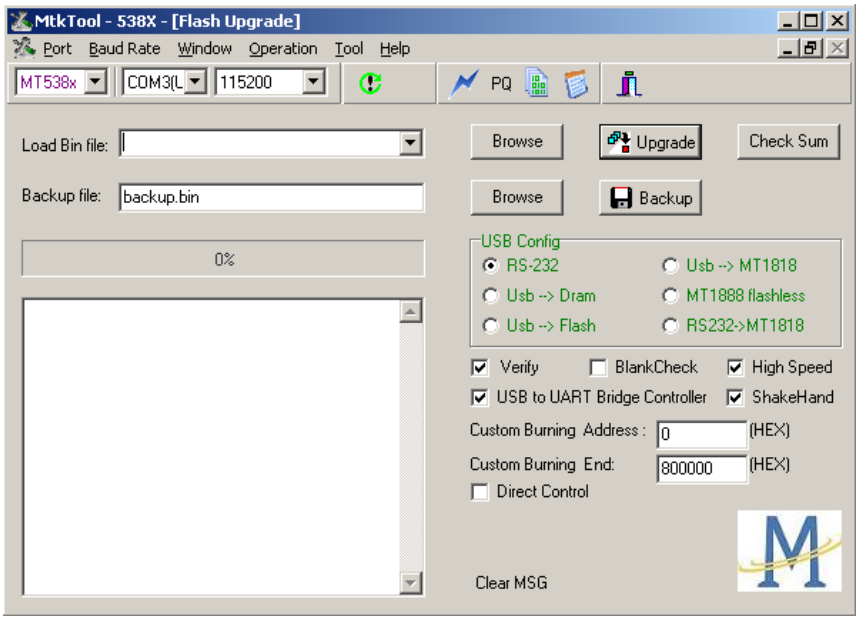
Prepare WT_MCU_ISP SW tool for update.

1. Connect the PC to board using MCU updating tool on P802 connector form chassis board.
2. Provide the +5VDC on P804 connector form chassis board and check U811 output voltage should be 3.3V.
3. Start "WT_MCU_ISP.exe" and download the MCU SW. (please see file *ISPToolGuideV33-08-2-17)*

Appendix ❷ "How to download FLASH SW"

Prepare MTK SW tool for update.

1. Connect the PC to the board using an external +3.3VDC serial device (USB or COMx) on P201 connector from chassis board. VGA input can also be used using pin12 (RXD) & pin15 (TXD) just taking care that "**Factory Key**" from Factory Menu is enabled.
2. Provide the +5VDC STB on P804 connector from chassis board
3. Start "**MTKTOOL.exe**" application under MTKxx folder, and set the parameters as below picture:



4. Press “Browse” button to select the corresponding SW bin file to upload
5. Press “Upgrade” button to start downloading the SW and wait the gauge displayed “100%” that means the SW has been successfully downloaded.
   In the meanwhile, all operations such erasing flash and so… are parsed into the debug window script.
6. Once the SW is downloaded, switch-off/on the chassis board and wait few seconds for Eeprom update.

Appendix ❸ “Serial Command Protocol for MTKxx”

1. A serial protocol for driving MTK µchip through external +3.3VDC serial device (USB or COMx) is available. It may facilitate manufacturing process. Thus, both P201 connector from chassis board or either VGA input can also be used using pin12 (RXD) & pin15 (TXD) just taking care that “**Factory Key**” from Factory Menu is enabled.
2. The required serial port settings are as below
   - **115200** bps
   - **8** data bit
   - **1** bit stop
   - **none** parity
3. The command format is like hereafter described into BNS representation:
   - **0xBB** + **Command** + **Data[[..]** + **..]** + **0xEE**

Both **0xBB** and **0xEE** bytes are mandatory and used as header and footer of the transmitted frame. Apart from **INIT** frame that is described further, all sent bytes need to be triggered before by an additional one as **0x50**. So a complete frame might match following one:

- **0x50**+**0xBB**+**0x50**+**Command**+**0x50**+**Data[[..]**+**0x50**+**..]**+**0x50**+**0xEE**

4. At first time, it might be required to initialize MTK µchip by using once below **INIT** command (without any triggering byte):
   - **0x02** + **0x00** + **0x00** + **0x13** + **0x01** + **0x00**
5. A none exhaustive list of commands is already available.

Appendix ❹ “ WARM/COOL Relative Matrix Offsets”

1. These offsets should be done in the production by AOE.

GENERAL DESCRIPTION

The **MediaTek MT5335PU** family consists of a backend decoder and a TV controller and offers high integration for advanced applications. It combines a transport de-multiplexer, a high definition MPEG-2 video decoder, an MPEG2 audio decoder, an LVDS transmitter, and an NTSC/PAL/SECAM TV decoder with a 3D comb filter. The MT5335PU enables consumer electronics manufactures to build high quality, low cost and feature-rich iDTVs.

World-Leading Audio/Video Technology: The MT5335PU family has built-in high resolution and high-quality audio codec. It includes MediaTek MDDi™ de-interlace solution to generate very smooth picture quality for motions. A 3D comb filter added to the TV decoder recovers great detail for still pictures. The special color processing technology provides natural, deep colors and true studio quality graphics.

Rich Features for High Value Products: The MT5335PU family enables a true single-chip experience. It integrates high-quality HDMI1.3, high speed VGA ADC, dual-channel LVDS, and USB2.0 receiver

Reliable Front-end Receiving Capability: Excellent adjacent and co-channel rejection capability grants customers never miss any wonderful stream. Professional error-concealment provides stable, smooth and mosaic-free video quality.

Key Features:

- An transport demultiplexer
- An MPEG2 video decoder
- An AC3 audio decoder
- HDMI1.3 receiver
- Audio codec

Note: All Package are Lead Free

FEATURES

- Host CPU
  - ARM 926EJS
  - 8K I-Cache and 8K D-Cache
  - 4K Instruction TCM
  - JTAG ICE interface
  - Watch Dog timers

- Transport Demultiplexer
  - Supports a serial or parallel transport stream input
  - Supports DVB-T, MPEG-2 transport stream input
  - Supports DES/3-DES/DVB de-scramblers
  - Up to 8-PID even/odd keys for descrambling
  - Supports 32 PID filters and 32 section filters
  - Supports positive/negative/mask section filtering
  - Supports hardware CRC-32 check
  - Supports PCR recovery function
  - Supports a micro-processor for stream process and MPEG start code detection

- MPEG2 Decoder
  - Supports one MPEG-2 HD decoder
  - MPEG MP@ML, MP@HL and MPEG-1 video standards

- 2D Graphics
  - Supports multiple color modes
  - Point, horizontal/vertical line primitive drawings
  - Rectangle fill and gradient fill functions
  - Bitblt with transparent options
  - Alpha blending and alpha composition Bitblt
  - Stretch Bitblt
  - Font rendering by color expansion
  - YCbCr to RGB color space conversion
  - Supports off-line scaler

- OSD Plane
  - Two linking list OSDs with multiple color mode and one of them has scaler

- Video Plane
  - Supports video capture and over scan.
  - Flesh tone management
  - Gamma/anti-Gamma correction
  - Color Transient Improvement (CTI)
  - 2D Peaking
  - Saturation/hue adjustment
  - Brightness and contrast adjustment
  - Black and White level extender
  - Adaptive Luma/Chroma management
  - Automatic detect film or video source
  - 3:2/2:2 pull down source detection
  - The MT5335PU support bob mode de-interlace with excellent low angle image processing.
  - Arbitrary ratio vertical/horizontal scaling of video, from 1/32X to 32X
  - Advanced non-linear panorama scaling.

- Programmable zoom viewer
- Progressive or interlace scan output
- Supports alpha blending
- Dithering processing for flat panel display
- Frame rate conversion.
- The MT5335PU supports up to 1680x1050 panel and VGA dot-to-dot.
- Supports 2 video source PIP/POP feature.

■ LVDS
- MT5335PU supports 6/8/10-bit one–channel or 6/8-bit dual-channel LVDS transmitter, LVDS speeding up to 75 MHz
- Built-in spread spectrum for EMI performance
- Programmable panel timing output

■ CVBS In
- On-chip 54 MHz 10-bit video ADC
- Supports PAL (B,G,D,H,M,N,I,Nc), NTSC, NTSC-4.43, SECAM
- Macrovision detection
- NTSC/PAL support 3D comb filter, SECAM supports 2D comb filter
- Built-in motion-adaptive 3D Noise Reduction
- VBI data slicer for CC/TT decoding
- Supports 2-S-Video.
- The MT5335PU supports 3-channel CVBS.
- Supports SCART connector

■ VGA In
- Supports VGA input up to UXGA 162 MHz
- Supports full VESA standards

■ Component Video In
- Supports two component video inputs
- Supports 480i / 480p / 576i / 576p / 720p / 1080i / 1080p

■ Audio line in interface
- The MT5335PU support 1-bit line in data (two channels)

■ HDMI Receiver
- Mixed 3 channels of HDMI1.3, data rate can be up to 2.25 GHz
- EIA/CEA-861B
- CEC

■ Audio ADC
- The MT5335PU supports 8-channel (4 R/L pairs) analog audio input.

■ TV audio demodulator
- Supports BTSC/EIA-J/A2/NICAM/PAL FM/SECAM world-wide formats
- Standard automatic detection
- Stereo demodulation, SAP demodulation
- Mode selection (Main/SAP/Stereo)

■ Audio DAC
- Four on-chip audio DACs (2 R/L pairs) support R/L channel and subwoofer outputs

■ DRAM Controller

- Supports 64 Mb to 512 Mb DDR DRAM devices
- The MT5335PU supports 16-bit data bus; address offers up to 64 M bytes space.
- Supports DDR1-333, DDR1-400, DDR2-400, DDR2-533, DDR2-667, DDR2-800

Audio DSP

- Supports Dolby Digital AC-3 decoding
- MPEG-1 layer I/II decoding (DVB)
- Dolby Prologic II
- Audio output: 7.1ch + 2ch (down mix)
- Pink noise and white noise generator
- Equalizer
- Bass management
- 3D surround processing with virtual surround
- Audio and video lip synchronization
- Supports reverberation
- Automatic volume control
- One SPDIF out
- If internal audio DAC is disabled, the MT5335PU supports 1-bit (2-channel) main audio I^2S output interface. Each channel is up to 24-bit resolution.

Flash Interface

- The MT5335PU supports two one serial flash
- Serial flash interface supports up to 60 MHz clock rate, depending on the spec. of the flash device (currently 20 MHz at maximum)
- Supports on-the-fly decompression from Serial Flash to DRAM

Peripherals

- The MT5335PU has one dedicated UART and one shared UART with GPIO.
- The MT5335PU has three basic serial interfaces; one is for the tuner, one is the master for general purpose and the other is the slave for HDMI EDID data.
- Three PWMs
- IR blaster and receiver
- Real-time clock and watchdog controller
- 1-port USB2.0/1.1 host supports USB mass storage class devices.
- Supports five-channel servo ADC.

IC Outline

- The MT5335PU is 256-pin LQFP-EPAD Package
- 3.3V/1.1V and 2.5V for DDR1, 1.8V for DDR2

The MT5335PU is designed as an advanced, highly integrated SoC with improved connectivity features including HDMI interface and component/composite signal connections. Figure 1-1 shows the MT5335PU system block diagram while Figure 1-2 shows the MT5335PU functional block diagram.

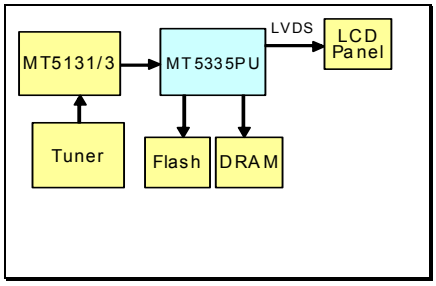


Figure 1-1 System Block Diagram

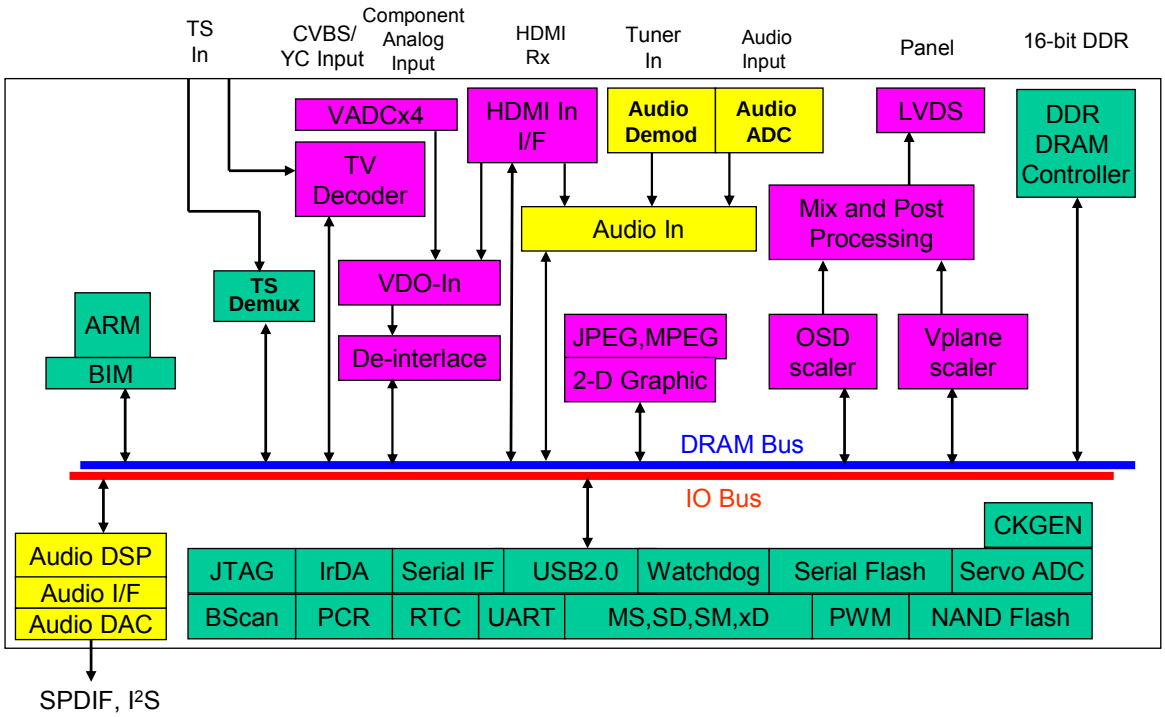


Figure 1-2 Functional Block Diagram

MT5133 DATA SHEET

General Description

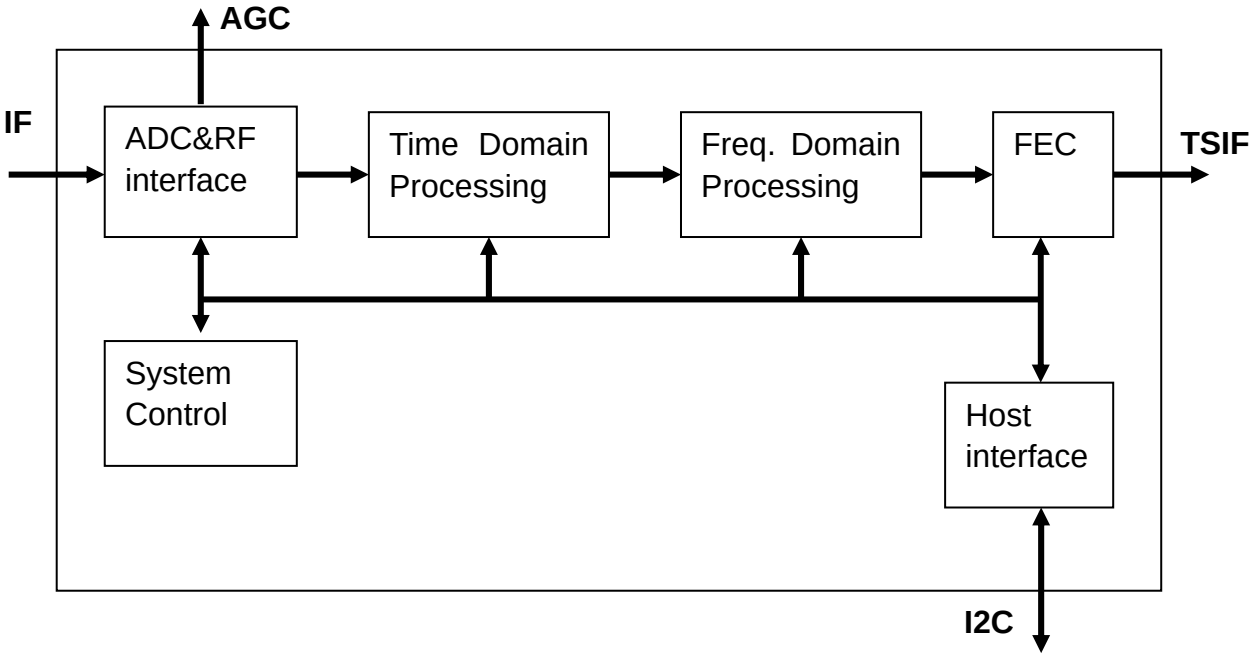
1. Introduction

MT5133 is Media Tak's 2nd generation COFDM (Coded Orthogonal Frequency Division Multiplex) channel demodulator for DVB-T receiver. It is fully compliant with the DVB-T specification (ETSI 300744) and Nordig Unified. MT5133 implements the functions from tuner IF out to MPEG-2 transport stream input. The device can support 2K, 4K or 8K mode with 6, 7, 8MHz channel. By integrating high performance A/D converters into the chip, MT5133 can accept first or second IF signal from conventional tuner thus eliminating the need for an external down-converter. Pure digital synchronization, advance channel estimation and equalization guarantee the wide acquisition range of MT5133. User can easily access on-chip information, including signal-to-noise ratio, Bit Error Ratio (BER) before and after Viterbidecoder. Serial or parallel MPEG transport stream output can be interfaced to all commonly available backend processor chips.

2. Features

- ETSI300744 and Nordig Unified compliant
- Suitable for Single Frequency Network (SFN) operation
- Support 2K, 4K, 8K modes
- Support QPSK, 16QAM,64QAM constellations
- 1/4, 1/8, 1/16, 1/32 Guard interval
- Support hierarchical & non-hierarchical modes
- Automatic mode detection
- Full-digital timing/frequency with wide acquisition range
- Support triple offset
- On-chip high-performance 10-bit ADC
- Excellent adjacent Channel interference (ACI) rejection capability
- Excellent Co-Channel interference (CCI) rejection capability
- Build-in PID filters
- Very low power consumption < 180Mw
- Controlled by I2C interface
- Package: QFN48

3. Block Diagram



Block Diagram of MT5133

MT8295 DATA SHEET

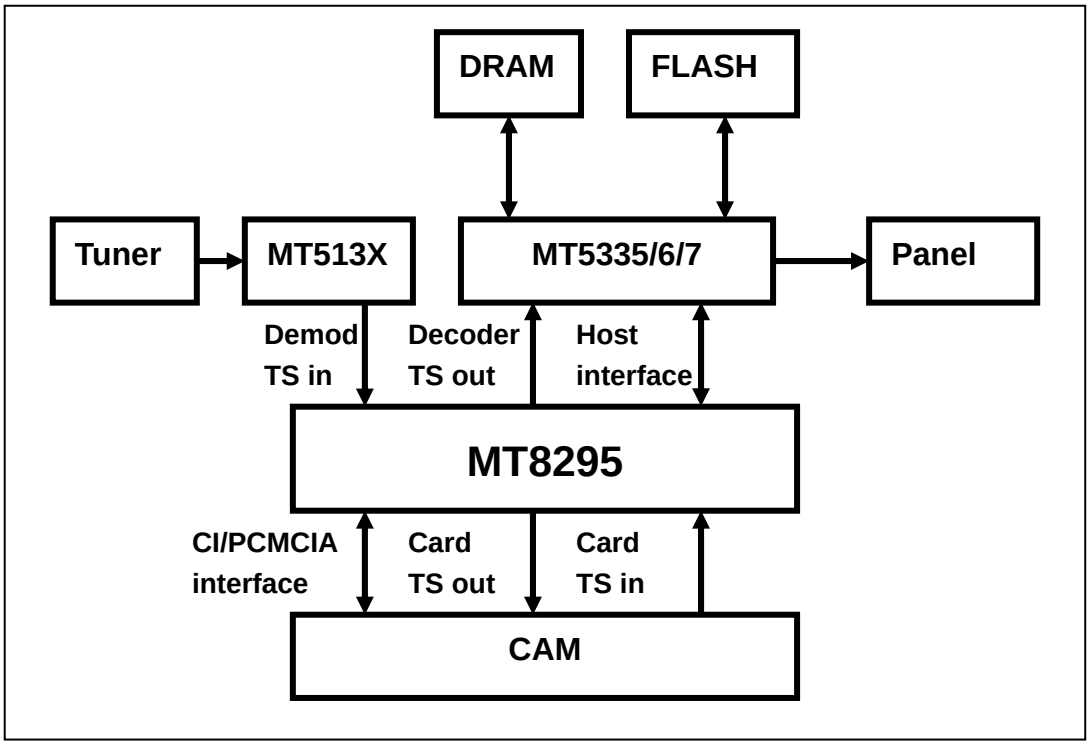
1. Introduction

The MediaTek MT8295 is a companion chip combined with MT533X serial chips to enable Common Interface (CI) and with the second generation of the Common Interface (CIV2) functions. It supports DVB compliant Conditional Access Module (CAM) and PCMCIA type memory cards. A NAND-flash-like bus bridge is built-in to perform the communication between a host and the card.

Highly Flexible Interface: MT8295 supports one parallel or two serial MPEG2 transport stream interfaces from the front end demodulator and a serial MPEG2 transport stream interface to MPEG2 decoder. Also, the MT8295 is designed with highly flexible interface timing to compliant with the maximum vendor's CAMs in the word.

Extra Value for Your TV: MT8295 enables TV to receive DVB-CI protected program. It helps content providers to protect their programs and allows customers to receive more high-value TV programs. Fully tested compliant software is also available for this device.

2. DTV System Use MT8295



1. General Description

The WT6702F is a microcontroller for system power manager with 1)Turbo 8051 compatible (3T) CPU, 2) 8K bytes flash memory, 3) 256 bytes SRAM, 4) 2 PWMs, 5) DPMS detector, 6) 8051 2 timers and UART, 7) Three Slave IIC interface, 8) 4 channel 8-bit A/D converter, 9) Real Time Clock, 10) watch-dog timer, 11) Embedded ISP, 12) Power down mode, 13) Embedded ICE mode.

1.1. Features

- Embedded turbo 8051(3T) CPU
  - Normal operation mode : 12MHz, 2MHz
  - Stand by mode : 32KHz
- Memory :
  - RAM: 256 Bytes
  - Flash memory: 8K Bytes
- Turbo 8051 Timer0, Timer1, & UART
- Sync processor for monitoring DPMS (VGA connector) wake up signal
- 8-bit A/D converter with 4 selectable inputs, shared with IO pin
- 2 PWM pin output
- 3 slave mode IIC interface
- Universal IR Receiver
- INT pin to main chip
- Watch Dog timer
- Low voltage reset
- 32.768KHz crystal Oscillator & build-in RC Oscillator
- Build-in RTC
- Maximum 18 programmable IO pins
  - 18-IO: 24 pin package
  - 14-IO: 20 pin package
  - 11/12-IO: 16 pin package
- Power consumption :
  - Lower than 6mA at 12Mhz mode
  - Lower than 4mA at 2Mhz mode
  - Lower than 2mA at low speed mode(32KHz)
- Operating voltage range : 3.6V – 2.5V
- Package:
  - SOP16
  - SOP20/SSOP20
  - SOP24

1.2. Application

- Display system power management MCU with RTC.
- I/O expander with RTC and ADC.

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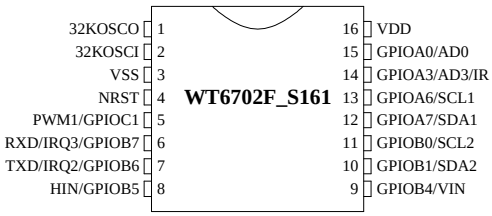
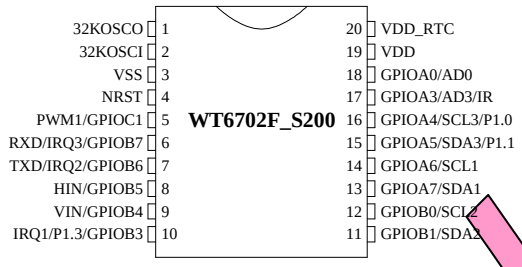
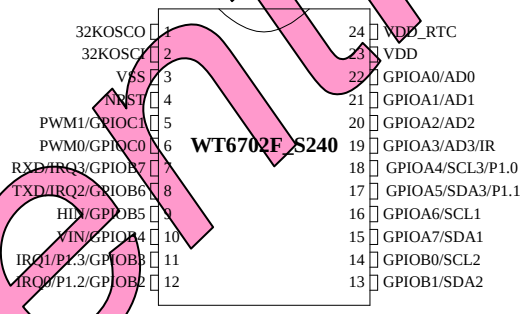
2. Pin Assignment

2.1. Package Type







Package Type	Package Outline
SOP 16 pin	150mil
SOP 20 pin	300mil
SSOP 20 pin	150mil
SOP 24 pin	300mil

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2.2. Pin Description

S240	S200	S161	Pin Name	I/O	Function Description
23	19	16	VDD	PWR	Power 3.3V
24	20	16	VDD_RTC	PWR	RTC Power (<3.3V)
1	1	1	32KOSCO	O	32kHz oscillator output
2	2	2	32KOSCI	I	32kHz oscillator input
3	3	3	VSS	GND	Ground
4	4	4	NRST	I	Reset pin, active low (internal pull high)
5	5	5	GPIOC1	I/O	PWM1 output. Shared with GPIO C1
6			GPIOC0	I/O	PWM0 output. Shared with GPIO C0
7	6	6	GPIOB7	I/O	8051 UART RXD or external IRQ3 interrupt input. Shared with GPIO B7
8	7	7	GPIOB6	I/O	8051 UART TXD or external IRQ2 interrupt input. Shared with GPIO B6
9	8	8	GPIOB5	I/O	HIN input. Shared with GPIO B5
10	9	9	GPIOB4	I/O	VIN input. Shared with GPIO B4
11	10		GPIOB3	I/O	8051 P1.3 or external IRQ1 interrupt input. Shared with GPIO B3
12			GPIOB2	I/O	8051 P1.2 or external IRQ0 interrupt input. Shared with GPIO B2
13	11	10	GPIOB1	I/O	2nd slave IIC SDA2. Shared with GPIO B1
14	12	11	GPIOB0	I/O	2nd slave IIC SCL2. Shared with GPIO B0
15	13	12	GPIOA7	I/O	1st slave IIC SDA1. Shared with GPIO A7
16	14	13	GPIOA6	I/O	1st slave IIC SCL1. Shared with GPIO A6
17	15		GPIOA5	I/O	3rd slave IIC SDA or 8051 P1.1. Shared with GPIO A5
18	16		GPIOA4	I/O	3rd slave IIC SCL or 8051 P1.0. Shared with GPIO A4
19	17	14	GPIOA3	I/O	Key pad ADC input3 or IR detector input. Shared with GPIO A3
20			GPIOA2	I/O	Key pad ADC input2. Shared with GPIO A2
21			GPIOA1	I/O	Key pad ADC input1. Shared with GPIO A1
22	18	15	GPIOA0	I/O	Key pad ADC input0. Shared with GPIO A0

(a) All GPIOs have Schmitt trigger input.
(b) When use Slave IIC or 8051 P1.x (or UART), the external circuit need pull high(4.7kΩ)
(c) GPIOA3, GPIOA2, GPIOA1, GPIOA0 MAX input are +3.6v(=3.3v+0.3v)
and the other GPIOs MAX input is +5v (5v tolerant PAD)

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3. Selection Guide

Part NO.	WT6702F_S240	WT6702F_S200	WT6702F_S161
DPMS Detection	V	V	V
UART	V	V	V
8K Flash Memory	V	V	V
RAM 256 Byte	V	V	V
PWM Output	2	1	1
Slave I^2C	3	3	2
RTC	V	V	V
IO	18max	14max	11 max
Oscillator	32KHz Crystal/ RC OSC	32KHz Crystal/ RC OSC	32KHz Crystal/ RC OSC
8-bit ADC	4 selectable inputs	2 selectable inputs	2 selectable inputs
Package	24-pin SOP	20-pin SOP/SSOP	16-pin SOP

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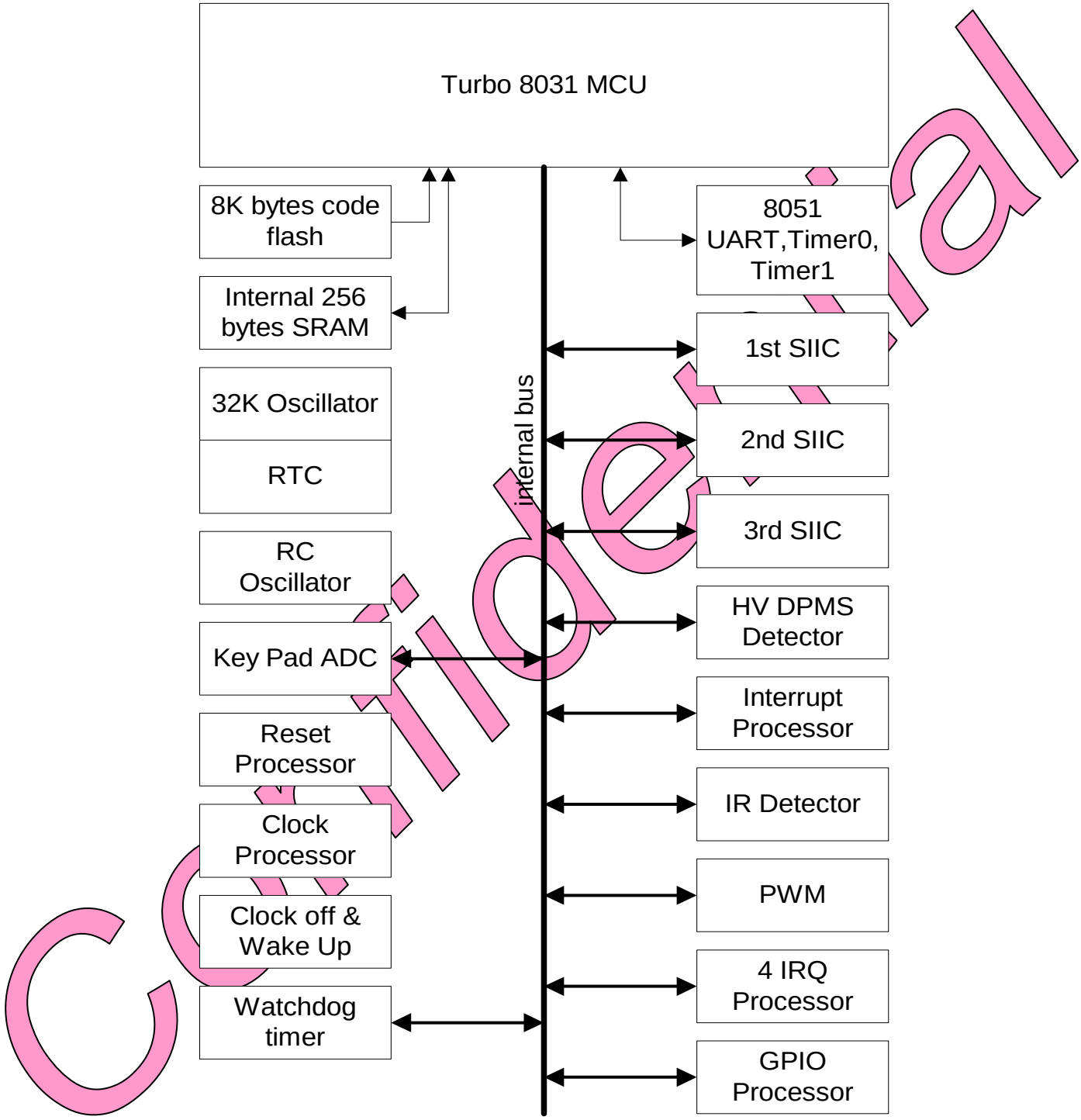
4. Functional Block Diagram



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WM8501

24-bit 192kHz Stereo DAC with 1.7Vrms Line Driver

DESCRIPTION

The WM8501 is a high performance stereo DAC with an integrated 1.7Vrms line driver. It is designed for audio applications that require a high voltage output along with enhanced load drive capability.

The WM8501 supports data input word lengths from 16 to 24-bits and sampling rates up to 192kHz. The WM8501 consists of a serial interface port, digital interpolation filters, multi-bit sigma delta modulators and stereo DAC in a 14-lead SOIC package.

The hardware control interface is used for the selection of audio data interface format, enable and de-emphasis. The WM8501 supports I^2S, right Justified or DSP interfaces.

Operating on separate analog and digital supplies the WM8501 offers very lower power consumption from the digital section, whilst supporting enhanced load drive from the analogue output.

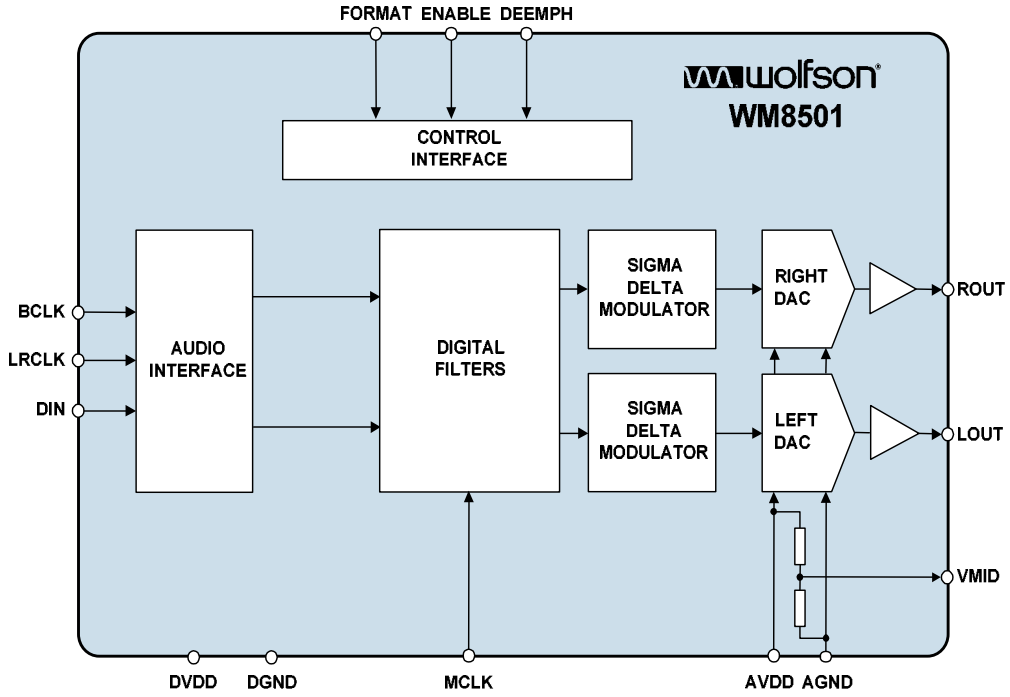
FEATURES

- Stereo DAC with 1.7Vrms line driver from 5V analogue supply
- Audio performance
  - 100dB SNR ('A' weighted @ 48kHz)
  - -88dB THD
- DAC Sampling Frequency: 8kHz – 192kHz
- Pin Selectable Audio Data Interface Format
  - I^2S, 16-bit Right Justified or DSP
- 14-lead SOIC package
- 4.5V - 5.5V analogue, 2.7V - 5.5V digital supply operation

APPLICATIONS

- STB
- DVD
- Digital TV

BLOCK DIAGRAM



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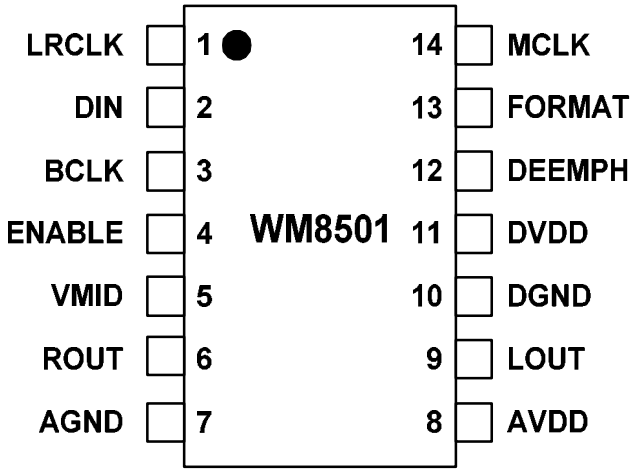
PIN CONFIGURATION



ORDERING INFORMATION

DEVICE	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
WM8501GED/V	-25 to +85°C	14-lead SOIC (Pb-free)	MSL3	260°C
WM8501GED/RV	-25 to +85°C	14-lead SOIC (Pb-free, tape and reel)	MSL3	260°C

Note:
Reel quantity = 3,000

PIN DESCRIPTION

PIN	NAME	TYPE	DESCRIPTION
1	LRCLK	Digital input	Sample rate clock input
2	DIN	Digital input	Serial audio data input
3	BCLK	Digital input	Bit clock input
4	ENABLE	Digital input	Enable input – 0 = powered down, 1 = enabled
5	VMID	Analogue output	Analogue internal reference
6	ROUT	Analogue output	Right channel DAC output
7	AGND	Supply	Ground reference for analog circuits and substrate connection
8	AVDD	Supply	Positive supply for analog circuits
9	LOUT	Analogue output	Left channel DAC output
10	DGND	Digital Supply	Digital ground supply
11	DVDD	Digital Supply	Digital positive supply
12	DEEMPH	Digital input	De-emphasis select, Internal pull down High = de-emphasis ON Low = de-emphasis OFF
13	FORMAT	Digital input	Data input format select, Internal pull up Low = 16-bit right justified or DSP (Mode B) High = 16-24-bit I^2S or DSP (Mode A)
14	MCLK	Digital input	Master clock input

Note:

1. Digital input pins have Schmitt trigger input buffers.

General Description

The SiI9185A is the first generation of TMDS switch device supporting Revision 1.3 of the HDMI Specification (HDMI Consortium; June 2006). With three HDMI inputs and a single output, the SiI9185A provides a low-cost method of adding additional HDMI ports to the latest Digital TVs. New DTVs can easily connect to the many HDMI sources coming on the market, including DVDs, STB, game consoles, PCs, camcorders, and digital still cameras. The SiI9185A is a fully HDMI compliant device providing a simple, low-cost method of retransmitting protected digital audio and video, giving end-users a truly all-digital experience. Built-in backward compatibility with DVI 1.0 allows HDMI systems to connect to any DVI 1.0 source.

The SiI9185A provides additional integrated features to help lower system cost and provide enhanced features to the end consumer. To lower system cost, the SiI9185A provides a complete solution for switching sink-side HDMI signals. This includes DDC switching, individual HPD control, and 5V sense. The addition of these features eliminates additional external components, helping to lower cost. For source-side applications, the SiI9185A DDC switching can be bypassed with an external 4-channel I^2C-bus switch (e.g., Texas Instruments PCA95445) to allow clock stretching.

The SiI9185A is the first generation of device from Silicon Image to integrate the Extended Display Identification Data (EDID). The EDID is stored in on-board RAM that is downloaded from the system microcontroller during power up or initialization. The EDID is reflected on each of the three HDMI ports through the DDC bus. Flexibility is built in to allow mixing different EDID formats in an application. This allows elimination of up to three EDID ROMs while also saving board space.

Finally, the SiI9185A provides a complete, simple solution to enabling Consumer Electronics Control (CEC) in a DTV. CEC is a single-wire bus that transmits remote control commands throughout a home network. The SiI9185A integrates both an HDMI-compliant I/O and Silicon Image's CEC API. The CEC I/O meets all HDMI compliance tests and eliminates the need for additional external components, again saving board space. The CEC API manages reception and transmission of all CEC signals according to the CEC protocol and makes the information available to the system microcontroller. This significantly lowers the system-level control by the system microcontroller, simplifying firmware overhead.

A very low power standby mode is available, allowing DTVs to meet industry low-power requirements such as Energy Star. During this mode both the CEC and EDID are still functional.

Silicon Image's SiI9185A uses the latest generation of TMDS core technology. These TMDS cores are guaranteed to pass all HDMI compliance tests.

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Features

- Three-input, single-output HDMI switch
- Integrated TMDS® receiver and transmitter cores capable of receiving and transmitting 2.25 Gbps:
  - Supports video resolutions up to 1080p, 60 Hz, 12-bit or 720p/1080i, 120 Hz, 12-bit
  - Built-in adaptive equalizer provides long cable support even at deep-color resolutions
  - Pre-emphasis in transmitter
  - DVI 1.0, HDCP 1.1 and HDMI 1.3 compliant receiver and transmitter
  - Uses HDMI-compliant TMDS core for recovery and retransmission, unlike TMDS switches, which use high-speed analog switches and degrade TMDS signals
- Built-in Consumer Electronics Control (CEC) support:
  - HDMI-compliant CEC I/O simplifies and lowers cost for adding CEC support to DTV
  - Integrated CEC API lowers overhead requirements on system microcontroller, speeds design
- Integrated EDID capability to lower system cost
- DDC switching on each input port simplifies board layout and lowers cost
- Individual control of Hot Plug Detect (HPD) for each port
- 5V detect to help speed soft mute of audio during plug-in, plug-out conditions
- Control via local I^2C bus
- Stand-alone mode option:
  - Acts as simple switcher
  - No I^2C control required in this mode
- Low-power standby mode to meet Energy Star and other power saving requirements
- 80-pin QFP package

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SiI9185A Pin Mapping

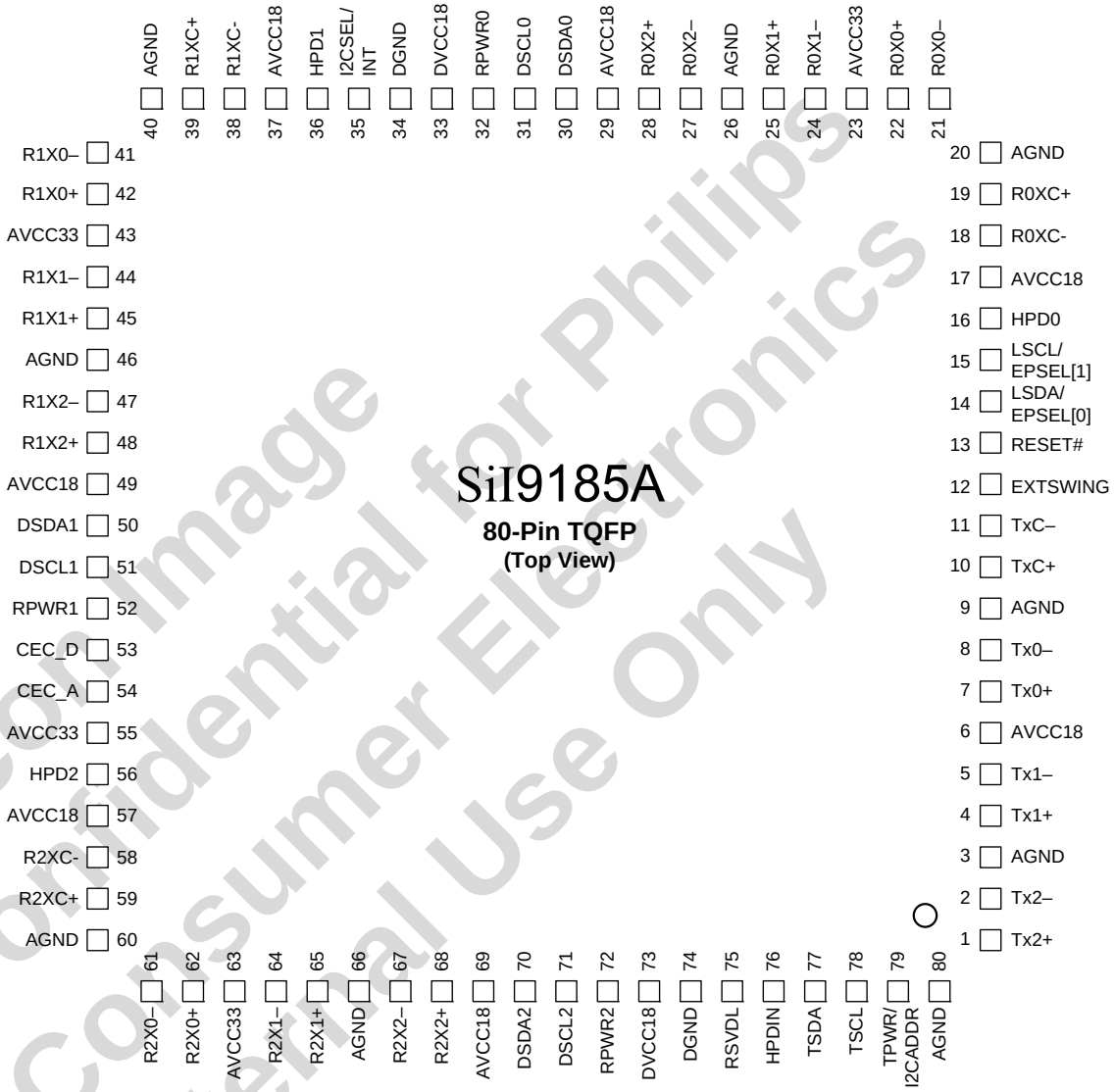

Figure 1. Pin Mapping

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Functional Description

The SiI9185A provides a low-cost method of providing additional HDMI inputs to a DTV. System cost is reduced by integrating DDC and HPD switching along with integrated EDID. Feature enhancements like the embedded CEC API provide a simple method of adding CEC to a DTV without burdening the system microcontroller.

Figure 2 and Figure 3 show the functional blocks of the device as applied to sink and source applications, respectively. Pin descriptions begin on page 20.

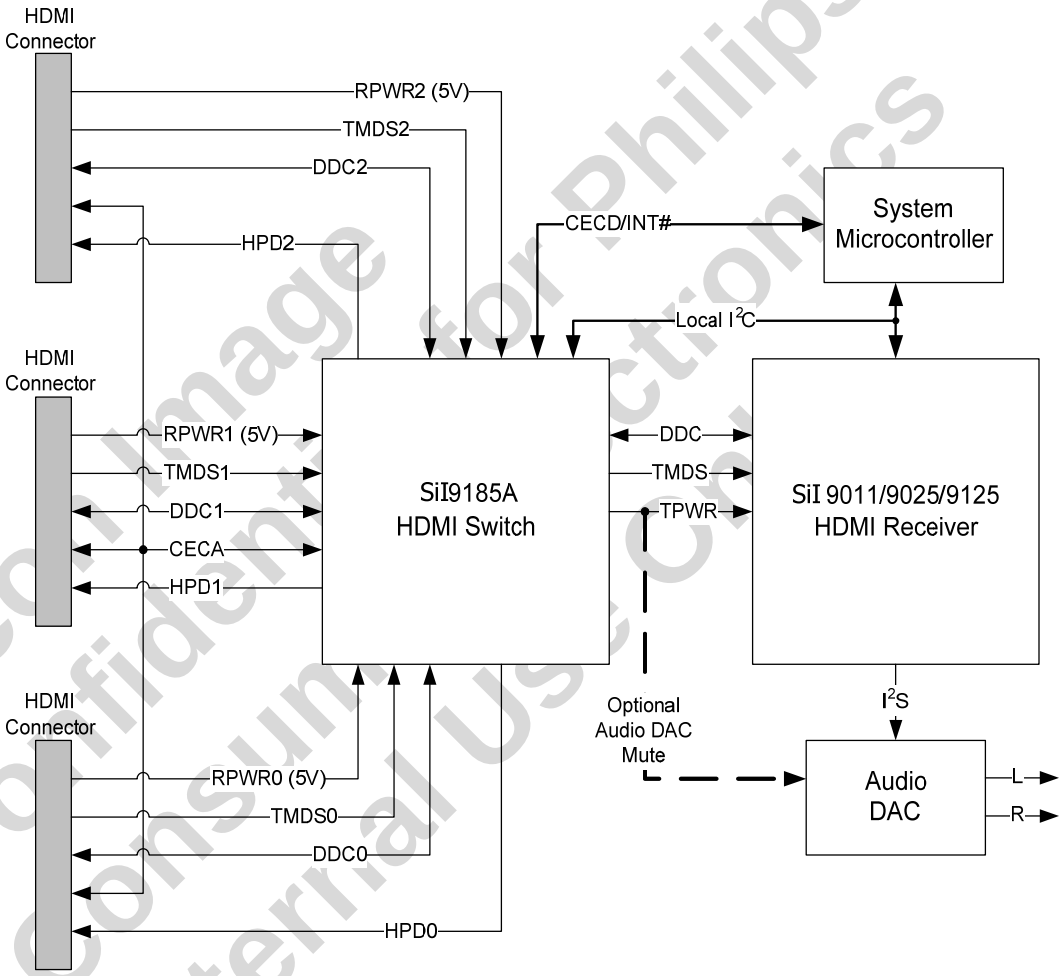

Figure 2. System Architecture, Sink Application

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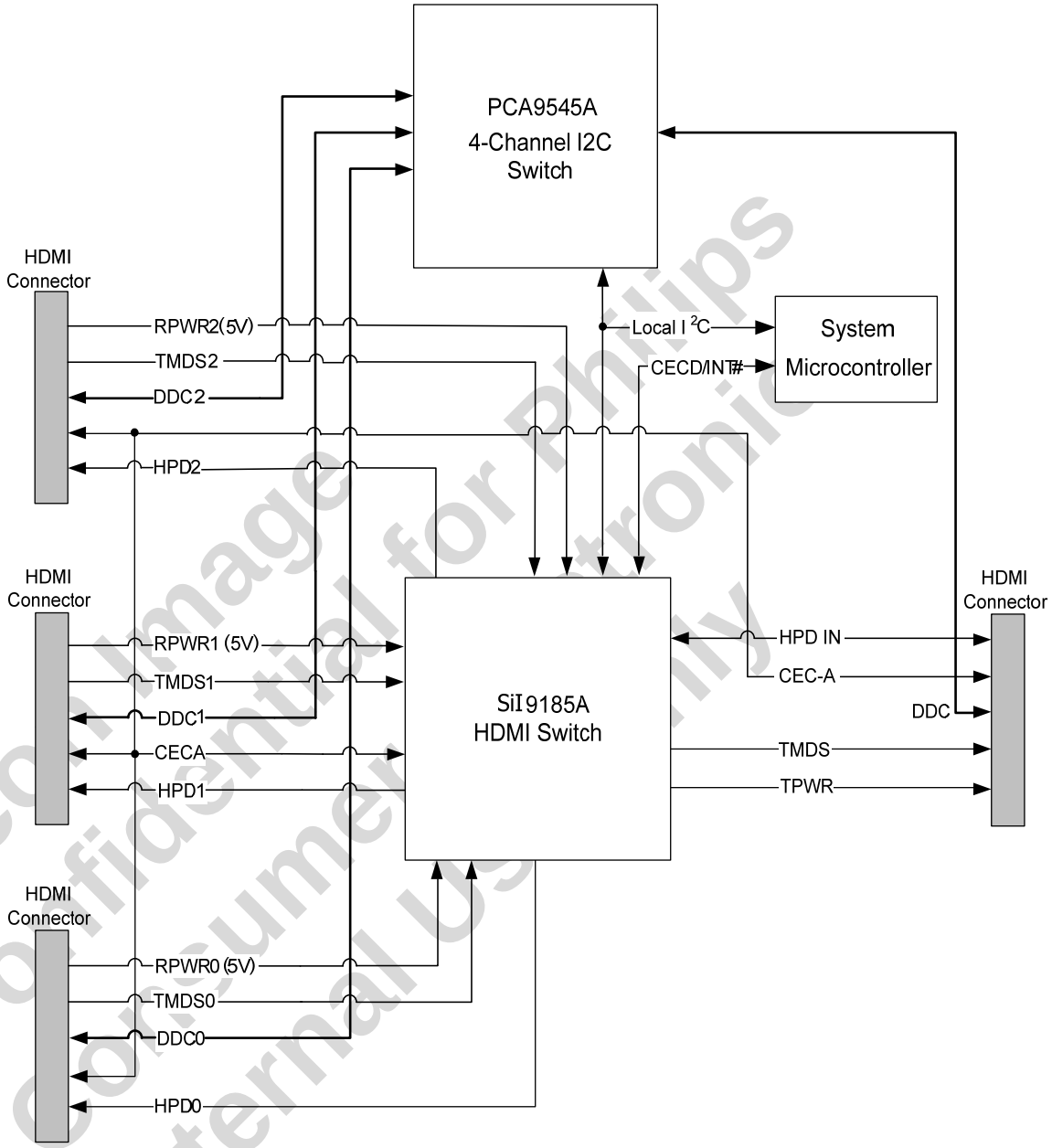

Figure 3. System Architecture, Source Application

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Block Level Functionality

The SiI9185A 3:1 HDMI 1.3 switch is used to select a single set of HDMI/DVI signals from one of three HDMI/DVI receiver-ports, and to generate a fully compliant HDMI/DVI stream as an output. It also provides DDC/HDCP, HPD, and +5V switching to allow full compliance to the HDMI/DVI specifications.

The combination of dynamic equalizer and state-of-the-art DPLL can overcome signal distortion due to the long lengths of HDMI/DVI cables. SiI9185A-based switches can be cascaded many times to regenerate TMDS and HDCP signals.

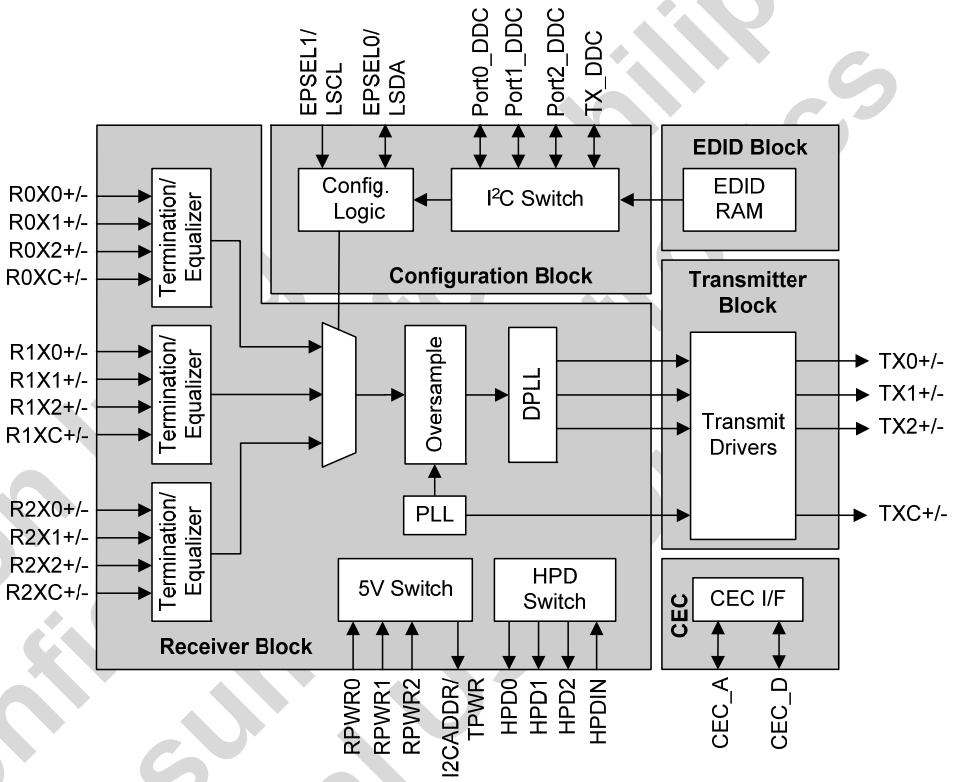

Figure 4. Functional Block Diagram

As shown in Figure 4, the SiI9185A consists of five major blocks:

- Receiver block
- Transmitter block
- CEC Interface block
- EDID RAM block
- Configuration block

Receiver Block

The three HDMI/ DVI receive ports are defined as Port 0, Port 1, and Port 2. Each of the ports is terminated separately and equalized under the control of the receiver digital block and controlled by the local I^2C bus. Port 0, Port 1, Port 2, or power down of all ports are selected by using the Port Select (PSEL[1:0]) signals. PSEL[1:0] can either be controlled by a register in I^2C mode, or pins in stand-alone mode.

The I^2C Switch conveys bidirectional DDC/EDID and HDCP information. In order to comply with the HDMI/DVI and HDCP specifications, the SiI9185A also switches and relays information with correct timing from three bidirectional I^2C Rx-ports to one bidirectional Tx-port. The HDCP switching and relaying operation is also done in the Receive block by monitoring the I^2C/HDCP protocol to decide the right direction of signal transfer. The port selection signal is used to provide correct HDCP data flow between the selected Receiver and the Transmitter port.

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Transmitter Block

The Transmit block consists of a fully compliant, HDMI 1.3 transmitter. This transmitter re-transmits the data received by the selected receiver port.

CEC Interface

The Consumer Electronics Control (CEC) Interface block provides CEC electrically compliant signals between CEC devices and a CEC master. It allows products to meet the electrical specifications of CEC signaling by translating the LVTTL signals of an external microcontroller (CEC host-side or Tx-side) to CEC signaling levels for CEC devices at the Rx-side, and vice versa.

Additionally, a CEC controller compatible with the Silicon Image CEC API is included on-chip. This CEC controller has a high-level register interface accessible through the I^2C interface which can be used to send and receive CEC commands. This controller makes CEC control very easy and straightforward, and removes the burden of having a host CPU perform these low-level transactions on the CEC bus.

In order to use the high-level CEC API, the host must perform a calibration of the internal CEC clock inside the SiI9185A. This calibration is performed by setting the calibration bit, and then sending a 10ms pulse (±1%) on the CEC_D signal input to the SiI9185A. The SiI9185A uses this pulse to calibrate an internal clock that is then used to generate all CEC timing to guarantee CEC compliance to the HDMI specification. This calibration must be repeated at time intervals corresponding to changes in temperature of 15°C.

EDID RAM Block

The EDID RAM block consists of 256 bytes of RAM that is shared by all ports. This means the timing information must be identical among all the ports if the internal EDID is used. Independent registers for the CEC physical address and checksum values for each port are also included, as these are unique to each port. On-board logic controls arbitration when reading the 256 bytes of EDID RAM, CEC physical address, and checksum values. This allows simultaneous reads of all ports from three different source devices if they are connected and attempt an EDID read at the same time.

The internal EDID can be selected on a per-port basis using registers on the local I^2C bus. For example: Port 0 and Port 1 can use the internal EDID, and Port 2 can use a discrete EEPROM for the EDID.

Configuration Block

The Configuration block is used to configure and control the operation of the SiI9185A. The SiI9185A has two modes of operation: I^2C and Standalone. In I^2C mode, all functions of the SiI9185A are controlled and observed with I^2C registers. All of these registers are accessible over the local I^2C Interface. These registers are used to perform port select, HPD control, CEC control, EDID loading, and power-down control.

In Standalone mode, all functions are controlled and observed by using pins on the SiI9185A. The mode is determined by the level of the I2CSEL/INT pin at the rising edge of RESET#. A high indicates I^2C mode, and a low indicates Standalone mode. In Standalone mode, the SiI9185A operates independently, and has no need for an external microprocessor.

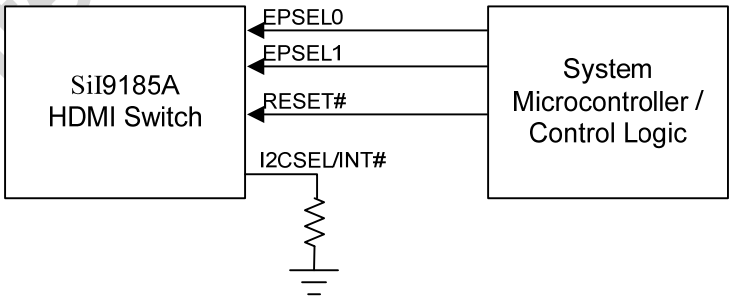

Figure 5. Standalone Mode Configuration

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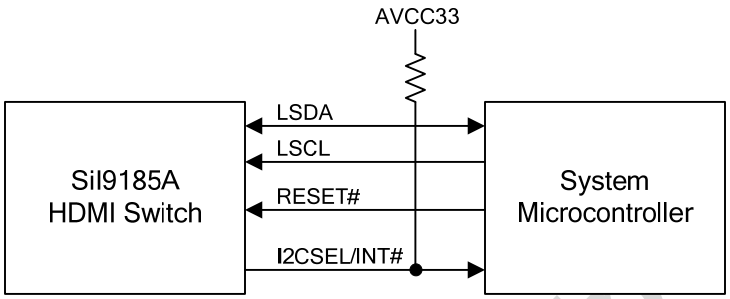

Figure 6. I²C Control Mode Configuration

I²C Interfaces

There are five I²C interfaces in the SiI9185A. There is one local slave I²C port that is used to configure the operation of the SiI9185A in I²C mode. Three slaves are connected to the three DDC receive ports, and one master is connected to the DDC transmit port; these ports are used to transfer DDC and HDPC information. All of the I²C pads are 5V tolerant and compliant to the I²C specification.

Local Slave I²C Interface

The local I²C interface on the SiI9185A (pins LSCL and LSDA) is a slave interface capable of running up to 100 kHz. This bus is used to configure the SiI9185A by reading/writing to necessary registers.

The local I²C interface of the SiI9185A consists of three separate I²C slave addresses. This means the SiI9185A will appear as three separate devices on the I²C local bus. The first of these addresses is used for PHY and Chip Control registers, is fixed, and can only be set to one of two values by using the I2CADDR pin. The other two addresses (used for CEC and EDID) have an I²C register programmable address mapped into the PHY and Chip Control register space, so the default value can be changed if there is a bus conflict with another device.

Table 1. Control of the Default I²C Addresses with the I2CADDR Pin

	I2CADDR=LOW	I2CADDR=HIGH
PHY and Chip Control Registers (fixed)	0xD0	0xD4
EDID Controller (programmable)	0xE0	0xE4
CEC Registers (programmable)	0xC0	0xC4

The PHY and Chip Control I²C address is fixed at boot-up and cannot be changed. The EDID Controller I²C Address and the CEC Controller I²C Address each have a register associated with them that allows the address to be changed. See the *SiI9181/9185 HDMI Switch Programmer's Reference Guide* for more information.

DDC Receiver Ports (Slave) and DDC Transmitter Port (Master) Interfaces

The DDC bus is an I²C interface used in the HDMI interconnection to facilitate bidirectional transfer of DDC/EDID information and perform the HDCP authentication process between source and sink devices. The SiI9185A includes three DDC slave I²C ports, one for each of the receive ports. These are used for direct connection to each of the upstream HDMI transmitters. The SiI9185A also includes a master I²C port for direct connection to the downstream HDMI receiver (Figure 3). The DDC ports support I²C transactions specified by the VESA Enhanced Display Data Channel Standard and supports I²C transactions needed for HDCP.

The DDC master I²C port and the three DDC slave I²C ports comply with the Standard Mode timing of the I²C specification (100 kHz). Due to the relaying function in the SiI9185A, the I²C master in the transmit port does not support SCL clock stretching by the slave to which it is connected. This is not an issue when used in sink applications that use Silicon Image receivers because they do not perform any clock stretching. For other applications it should be confirmed that the sink receiver device that connects to the SiI9185A output does not perform clock stretching on the I²C bus. For source applications an external I²C switch (such as the NXP 9545A) can be used to bypass the master and slave DDC ports of the SiI9185A. This will eliminate the SCL clock stretching issue (see Figure 4).

The SiI9185A will operate between an HDMI source and sink device, so DDC/EDID and HDCP transactions on the DDC bus must flow through the SiI9185A without causing information loss or timing margin degradation. The SiI9185A

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analyzes and regenerates the DDC signal, making it possible to extend the cable length of I²C DDC by cascading multiple SiI9185As together.

Control Pins

The SiI9185A can operate in two distinct modes, depending on the state of the I2CSEL pin at the end of RESET#: Standalone mode, and I²C Control mode. In Standalone mode, the SiI9185A operates independently and has no need for an external microprocessor. The configuration of the switch is set using signals on the external control pins listed below, and after configuration, the switch operates independently.

In I²C Control mode, the SiI9185A requires an external processor and is controlled over the I²C interface.

RESET# Control Pin

The system reset pin (RESET#) is an active-low input. When RESET# is low, all digital logic is reset including the I²C interfaces. When RESET# is high, the SiI9185A operates in normal mode.

Two pins are used to configure bootstrap options on the rising edge of RESET#: I2CSEL/INT and I2CADDR/TPWR. The I2CSEL/INT is sampled on the rising edge of RESET# to determine the operating mode. The I2CADDR/TPWR pin is sampled on the rising edge of RESET# to determine the base address of the I²C interface. These pins are discussed in the sections that follow.

I2CSEL/INT

The dual-purpose I2CSEL/INT pin acts as a configuration input pin for mode selection during the period when RESET# is true (low), and as the interrupt (INT) output during normal operation. The level on the I2CSEL/INT pin is latched when the RESET# signal transitions from low to high. If the I2CSEL/INT value is high on the rising edge of RESET#, the SiI9185A comes up in I²C Control mode. If the I2CSEL/INT value is low at the rising edge of RESET#, the SiI9185A comes up in Standalone mode and the EPSEL[1:0] pins are used as the external port select pins. Note that when I2CSEL is low at the rising edge of RESET#, the local I²C is disabled from that time, but the contents of the local I²C registers are not lost.

After RESET# is deasserted (goes high), the I2CSEL/INT pin becomes the interrupt output pin (INT). When interrupt conditions are met and the particular interrupt is enabled, the INT signal goes low indicating to the host that an interrupt has occurred and that actions are needed.

EPSEL1/LSCL and EPSEL0/LSDA

The EPSEL1/LSCL and EPSEL0/LSDA pins are dual-function pins, and their function depends on whether the SiI9185A is in Standalone mode or in I²C Control mode. In Standalone mode, these pins become the external port selection pins EPSEL[1:0]. In I²C Control mode, the EPSEL1/LSCL becomes the I²C Interface clock signal LSCL, and the EPSEL0/LSDA pin becomes the I²C Data signal LSDA.

The receive port is selected externally using the EPSEL[1:0] pins in Standalone mode, or internally using I²C registers (I²C Control mode). When I2CSEL is high at the end of RESET#, the receive port is selected by the I²C register IPSEL[1:0] (0xD0: 0x08). When I2CSEL is low at the end of RESET#, the receive port is selected using the external pins EPSEL[1:0] as shown in Table 1, and the local I²C interface is disabled.

Table 2. Port Selection Using the EPSEL Pins

	EPSEL1	EPSEL0
Port 0	0	0
Port 1	0	1
Port 2	1	0
Standby Mode	1	1

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Normal and Standby Modes

There are two power modes: P0 for Normal mode and P1 for Standby mode. The Normal mode, P0, is enabled when one of three RX ports is selected to provide audio/visual stream and HDCP/DDC information to the TX port as shown in Table 2. In Normal mode, all power supplies (AVCC33, AVCC18, and DVCC18) must be applied. In P0, all of the functional blocks are active: PLL, data-paths, local I^2C and DDC relaying, and CEC.

Setting PSEL[1:0] = 11 sets the SiI9185A into low-power standby mode (P1). In P1, all of the receive ports transition to the low-power state and the Tx outputs are disabled (Hi-Z). The purpose of P1 is to make the SiI9185A alive to power the DDC and CEC interfaces only, while the data-path of the SiI9185A (analog and digital) consumes minimum power. The I^2C and DDC relay require logic power (DVCC18), I/O power (AVCC33), and OSC power (AVCC18). Because none of the receive ports are selected in P1, the PLL does not get an input clock, and shuts itself down. In Standalone mode P1, the HPD outputs are deasserted (set to 0).

I2CADDR/TPWR Control Pin

The I2CADDR/TPWR pin is sampled on the rising edge of RESET# to determine bit two of the default base address for the I^2C interface. If I2CADDR/TPWR is low on the rising edge of RESET#, the I^2C interface address for the PHY and Chip Control registers is set to 0xD0, the I^2C interface address for the EDID Controller is set to 0xE0, and the I^2C interface address for the CEC Registers is set to 0xC0. If I2CADDR/TPWR is high on the rising edge of RESET#, the I^2C interface addresses are set to 0xD4, 0xE4, and 0xC4, respectively. The actual address values in both modes are shown in Table 1 on page 8.

Once RESET# goes high, the I2CADDR/TPWR pin becomes the normal output Transmit Power (TPWR). TPWR is an output from the SiI9185A that tells the transmit side that the selected receive port is actually connected. The switching time between RPWR0/1/2 and TPWR is determined by the PLL lock behavior and logic that detects the presence of a valid input signal (see RPWR[0:2](+5V) and TPWR(+5V) control pins on page 11 for a description).

CEC Transceiver Control Pins

The CEC (Consumer Electronics Control) interface is composed of the bidirectional signals CEC_D, CEC_A, and a local I^2C interface. CEC_D is the CEC signal from a CEC Master (microcontroller), and CEC_A is an electrical spec-compliant CEC signal connected to all CEC Slave devices. The CEC_A signal drives the CEC pins from all three HDMI/DVI Rx connectors at the same time.

The CEC interface has two modes: CEC_D relay mode and CEC API mode. In CEC_D relay mode, the SiI9185A is simply a CEC transceiver, and all software must be implemented on the host CPU. In CEC API mode, the SiI9185A performs all the low-level CEC control, and the host CPU must read and write to high-level I^2C registers to send and receive CEC commands. In CEC_D relay mode, the CEC interface only monitors the CEC signal direction and provides appropriate timing between events. In CEC API mode, the local I^2C provides CEC commands to the CEC interface block to generate CEC signaling to the CEC_A port, and the local I^2C monitors the CEC value in the register map.

HPD Control Pin

The Hot Plug Detection (HPD) signal is provided in the HDMI/DVI connector to provide a signal to the host that the EDID is readable. In the SiI9185A there are three outputs for the receive side (HPD0, HPD1, and HPD2), and one input from the transmit side (HPDIN). HPDIN from the Tx port can be relayed to the selected Rx port, or the HPD[0:2] outputs can be set using registers. In Standalone mode, the HPD outputs of non-selected Rx ports are set to low, so no EDID transaction or HDCP authentication is initiated for non-selected ports until that port is selected. The default signal level of the HPD output is low and the high signal level is 3.3V CMOS (and is +5V tolerant).

In internal SiI9185A applications, the HPDIN pin may not to be brought out as an external pin. In this case, the local I^2C directly controls the HPD output of selected and/or non-selected ports. But in external HDMI switch applications, the HDMI receiver on the video processing board provides an HPD signal input to the HDMI switch board, and the HPD input is re-directed to one of the selected receive ports.

In I^2C Control mode, the state of the HPD pins is controlled by setting the HP_CTRL_x bits in the Hot Plug Detect Output Control register, where x is the channel number. Each of the HPD0, HPD1, and HPD2 signals is independently controllable. For example, all three signals could be high at the same time.

HPD output pins have 1-kΩ series resistors integrated to comply with the impedance requirement specified in version 1.3 of the HDMI Specification.

Table 3 on page 11 shows the possible states of the HPD control signals.

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Table 3. Hot Plug Control Signal Levels

Condition	HPD[2:0] Level
No power to the SiI9185A. Example: TV unplugged.	Low
SiI9185A out of Reset in I^2C mode	Low (default)
SiI9185A in Standalone mode	Pass-through from HPDIN
SiI9185A in I^2C mode, register programming	Four options: selected by the HP_CTRL_x bits: 0b00 = Low 0b01 = High (3.3V) 0b10 = Tri-state 0b11 = Pass-Through
Port not selected in Standalone mode	Low

Note that to be HDMI compliant, each HPD Output is ANDed with its respective RPWR input. Hence a given HPD Output pin can only reflect a High state when the RPWR input of that port detects a High input (*and* the appropriate HP_CTRL_ bits are set to 01b, or they are set to 11b with the HPDIN signal being detected as High).

RPWR[0:2](+5V) and TPWR(+5V) Control Pins

The three RPWR (+5V) input signals on the receive side of the SiI9185A (RPWR0, RPWR1, and RPWR2) indicate that an HDMI cable is connected and 5V is electrically present. The PWR(+5V) signal on the transmit side of the SiI9185A (TPWR) notifies the receiving device that the transmit port has this 5V present. When the selected receive port is actually connected to a source device (a DVD player, for example), determined by monitoring the active port's RPWR[0:2](+5V) signal, then the transmit port of the SiI9185A sends the receiver-present signal (TPWR) to the HDMI receiver on the video processing board.

The RPWR(+5V) signal of the selected Rx port, (RPWR0, RPWR1, and RPWR2) is transferred to TPWR under the control of PSEL[1:0] signals, which can come from registers in I^2C Control mode, or pins in Standalone mode. The TPWR signal to the transmit port is pulled low for a period of 1 µS when the port selection is changed. After this time, it follows the state of the newly selected port.

RPWR input pins have internal pull-down resistors. When a port is not used, simply leaving them unconnected is sufficient.

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Embedded EDID

The SiI9185A embeds 256 bytes of RAM for EDID and used to eliminate the discrete EEPROM EDID from the system.

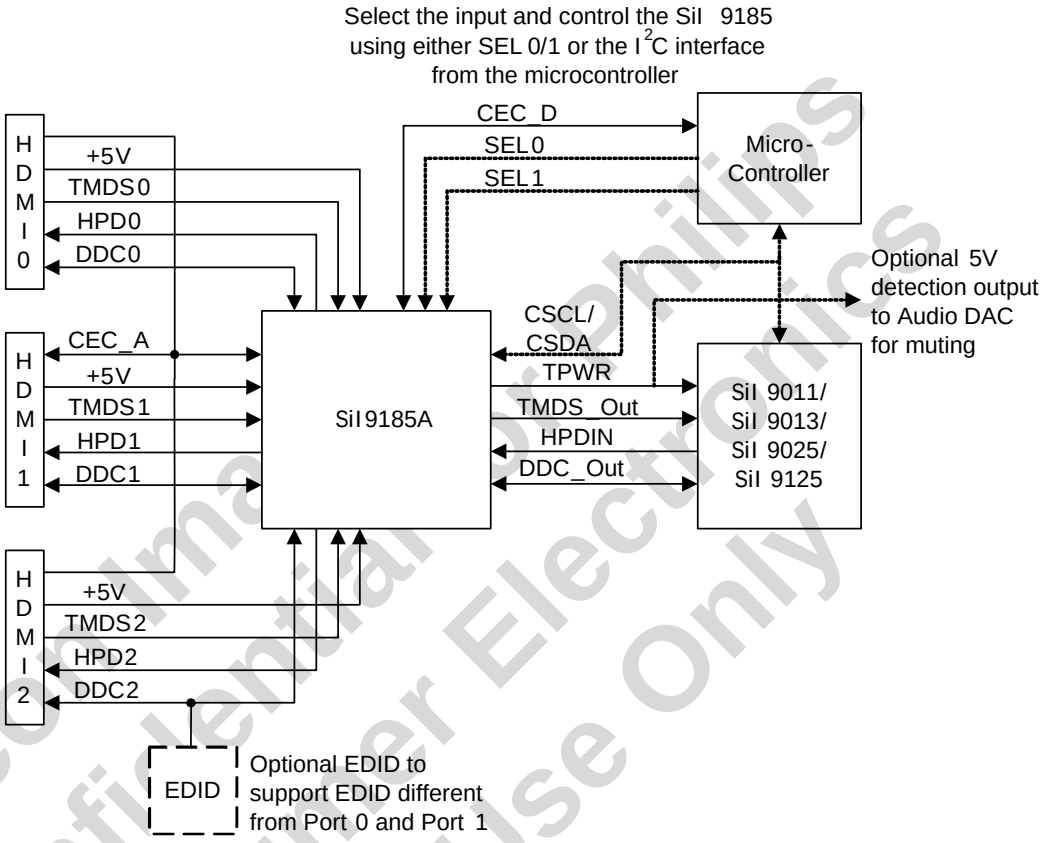

Figure 7. EDID in the SiI9185A

EDID Emulation Function

All of the HDMI input ports have a DDC interface consisting of DSDA# and DSCL# where # is the port number. The SiI9185A device incorporates the function of an HDMI 1.3 compliant EDID in internal registers. The first block must conform to the VESA EDID specification. The second block must conform to the CEA-861D specification.

The SiI9185A supports two blocks of EDID, each 128 bytes long. Table 4 shows the layout of the EDID block as it appears to each of the DDC interface controllers.

Table 4. Layout of the EDID Blocks

Block #	Description	Length	DDC I²C Slave Address	Offset Address Range
0	EDID 1.3 according to VESA	128 bytes	0xA0	0x00 – 0x7F
1	EDID extension according to the CEA 861 specification	128 bytes	0xA0	0x80 – 0xFF

The host writes the desired information into the EDID memory through the local I²C interface.

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EDID Emulation Function Using RAM

The EDID is stored in 256 bytes of on-chip RAM. The SiI9185A contains I²C distributor/arbiter logic to ensure that the EDID can be read by all three DDC input buses simultaneously.

The EDID memory provides identical information to each DDC channel except for the following:

- The CEC physical address for each channel. The location of this physical address in the EDID memory is specified by the contents of the CSCPA_ADDR register (0xE0:0x08) in the EDID controller. When the EDID memory is loaded through the local I²C controller, the CEC physical address contains the value for Channel (Port) 0. When the EDID controller detects that DDC for Channel 1 or Channel 2 is trying to read the CEC physical address location, it automatically replaces the information with the actual CEC1 or CEC2 physical address values stored in the CEC Physical Channel Address registers.
- Checksum. The checksum is always stored in the last register address for the EDID space (location 0xFF). When the EDID memory is loaded through the local I²C controller, the checksum value (location 0xFF) contains the value for Channel (Port) 0. However, the checksum is different for each channel due to the difference in physical CEC addresses for these channels. The host firmware stores different checksums for channels 1 and 2 in two different locations in the EDID controller registers. When the EDID controller logic detects that the DDC for a particular channel is reading the checksum, it responds with the value in one of the two registers, based on the inquiring port.

Figure 8 shows a block diagram of how the EDID function is emulated using RAM.

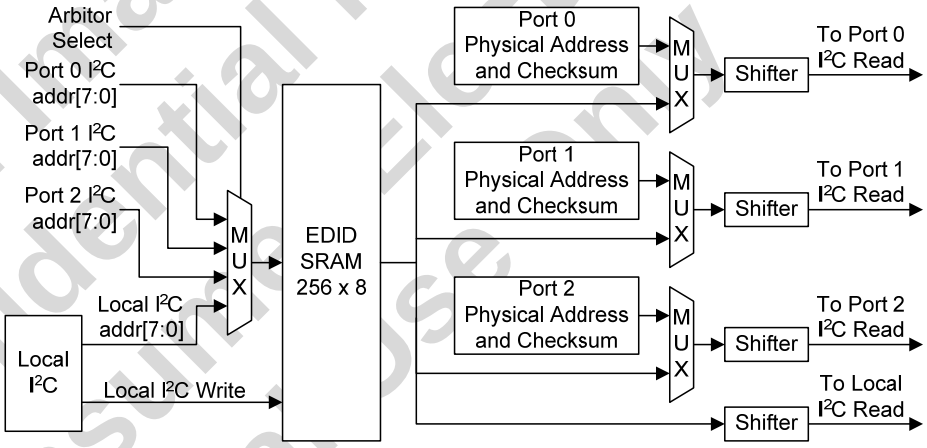

Figure 8. EDID Emulation Using RAM

The EDID contains the CEC physical address and must be loaded before enabling the CEC function. Additionally, HOTPLUG must be controlled to guarantee proper EDID and CEC operation by the host. The basic flow for loading the EDID into SiI9185A is shown below:

1. Power up the system.
2. Reset the SiI9185A.
3. Load the EDID for Port 0 into the SiI9185A.
4. Write the CEC physical addresses for Port 1 and Port 2.
5. Write the checksum values for Port 1 and Port 2.
6. Calibrate the CEC clock if using the CEC API.
7. Initialize the CEC registers if using the CEC API.
8. Enable DDC and CEC for all ports.
9. Write the registers to set HPD0, HPD1, and HPD2 high (now the host can read the EDID).

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CEC API Control

There is hardware assistance in the SiI9185A for CEC control that makes the software development for CEC much easier. CEC control has been implemented according to the internal Silicon Image CEC API (CPI) specification.

The CEC signal has two modes of operation:

1. Pass-through mode: In this mode, an external microcontroller can control the CEC level by using the CEC_D pin. The CEC API function in the SiI9185A is not used.
2. CEC API mode: In this mode, the SiI9185A performs decoding when acting as a follower, and a high-level command interface when acting as an initiator.

Pass-through mode is engaged under the following conditions:

- When the SiI9185A is working in Standalone mode, or
- When the SiI9185A is working in I^2C Control mode but the CEC enable bit is set to 0 (offset 0x08 bit 6)

CEC Reference Clock Calibration

An on-chip ring oscillator is used to send and receive CEC data while meeting the CEC timing specification. However, the ring oscillator frequency can vary on a per device basis, based on manufacturing variables. Therefore, it is necessary to calibrate this internal ring oscillator by applying an externally driven pulse of 10 ms to the CEC_D pin. The procedure for applying this calibration signal is:

1. The host processor should set the CEC_D pin high before starting the calibration cycle.
2. The host processor starts the calibration cycle by setting the CALIB bit in local I^2C offset 0x09 bit 0 to 1. This bit is self-resetting.
3. The host processor should wait for at least 100 ns after writing the CALIB bit.
4. The host processor should then cause the CEC_D pin to go through a high-to-low transition. The signal should stay low for a period of 10 ms ±1%, and then transition back high.
5. At this point calibration is complete.
6. The calibration cycle will be repeated each time the host writes a '1' to the CALIB bit.

A counter is used to count the number of ring oscillator clocks in this 10 ms pulse, and the frequency of the ring oscillator is determined from this count. This is used as the time base to accurately send and receive CEC commands according to the CEC specification. Note that unless the calibration pulse is properly applied to the SiI9185A and the calibration cycle is properly completed, the CEC logic will NOT operate correctly. The host should complete the calibration cycle before setting the CEC enable bit in the local I^2C.

The oscillator used in the CEC timing mechanism may vary slightly with temperature. It is recommended that as a precaution the CEC reference clock calibration process be repeated for every 15°C of change. For example, it may be periodically recalibrated approximately every 10 minutes.

In standalone applications where CEC-relay mode is used, the incoming CEC timing is measured using the internal oscillator clock to reproduce the correct output timing. For example, if the START period of CEC_D is measured to be some number of internal oscillator clocks, that number is used as the basis to re-shape the CEC output timing. Therefore, in CEC-relay mode a calibration pulse is not required.

CEC Programming Interface (CPI)

The CEC application solution involves both low-level and a high-level components. For low-level components, the low-level CEC protocol is handled by the slave I^2C interface of the SiI9185A. For high-level components, the Silicon Image CEC software source code allows command strings to be exchanged over the I^2C interface as discussed above.

For development, Silicon Image provides Windows-based software tools, including a kit that allows a PC to be used to generate I^2C commands over any USB 1.1-capable port.

The I^2C register set used for this solution is referred to as CEC Programming Interface or just CPI. This standard register set is used across all Silicon Image devices and applications, both software and hardware.

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Wide Range Input Voltage Simple Synchronous DC/DC Converter

General Description

The RT8110 is a single power supply PWM DC-DC controller designed to drive N-MOSFET in a synchronous buck topology. The IC integrates the control, output adjustment, monitor and protection functions in a small 8-pin package.

The RT8110 uses an internal compensation high DC gain voltage mode PWM control for simple application design. An internal 0.8V reference allows the output voltage to be precisely regulated for low voltage requirement. A fixed 400kHz oscillator reduces the component size for saving board space.

The RT8110 features over current protection, and under voltage lock-out. The output current is monitored by sensing the voltage drop across the Low side MOSFET's $R_{DS(ON)}$, which eliminates the need for a current sensing resistor.

Ordering Information

RT8110-□□

- Package Type
  V8 : SOT-23-8
- Operating Temperature Range
  P : Pb Free with Commercial Standard
  G : Green (Halogen Free with Commercial Standard)

Note :

RichTek Pb-free and Green products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.
- 100% matte tin (Sn) plating.

Marking Information

For marking information, contact our sales representative directly or through a RichTek distributor located in your area, otherwise visit our website for detail.

Features

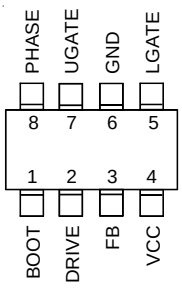
- **Wide Input Operation Voltage 5V to 23V**
- **0.8V Internal Reference**
- **Drive Two N-MOSFETs**
- **High DC gain Voltage Mode PWM Control**
- **Fast Transient Response**
- **Fixed 400kHz Oscillator Frequency**
- **Fully Dynamic 0 to 80% Duty Cycle**
- **Internal Soft Start**
- **Adaptive Non-Overlapping Gate Driver**
- **Over-Current Protection Under Voltage Lockout**
- **RoHS Compliant and 100% Lead (Pb)-Free**

Applications

- Motherboard Power Regulation for Computers
- Subsystems Power Supplies
- Cable Modems, Set Top Boxes, and DSL Modems
- DSP and Core Communication processor Supplies
- Memory Power Supplies
- Personal Computer Peripherals
- Industrial Power Supplies
- 5V-Input DC-DC Regulators
- Low Voltage Distributed Power Supplies

Pin Configurations

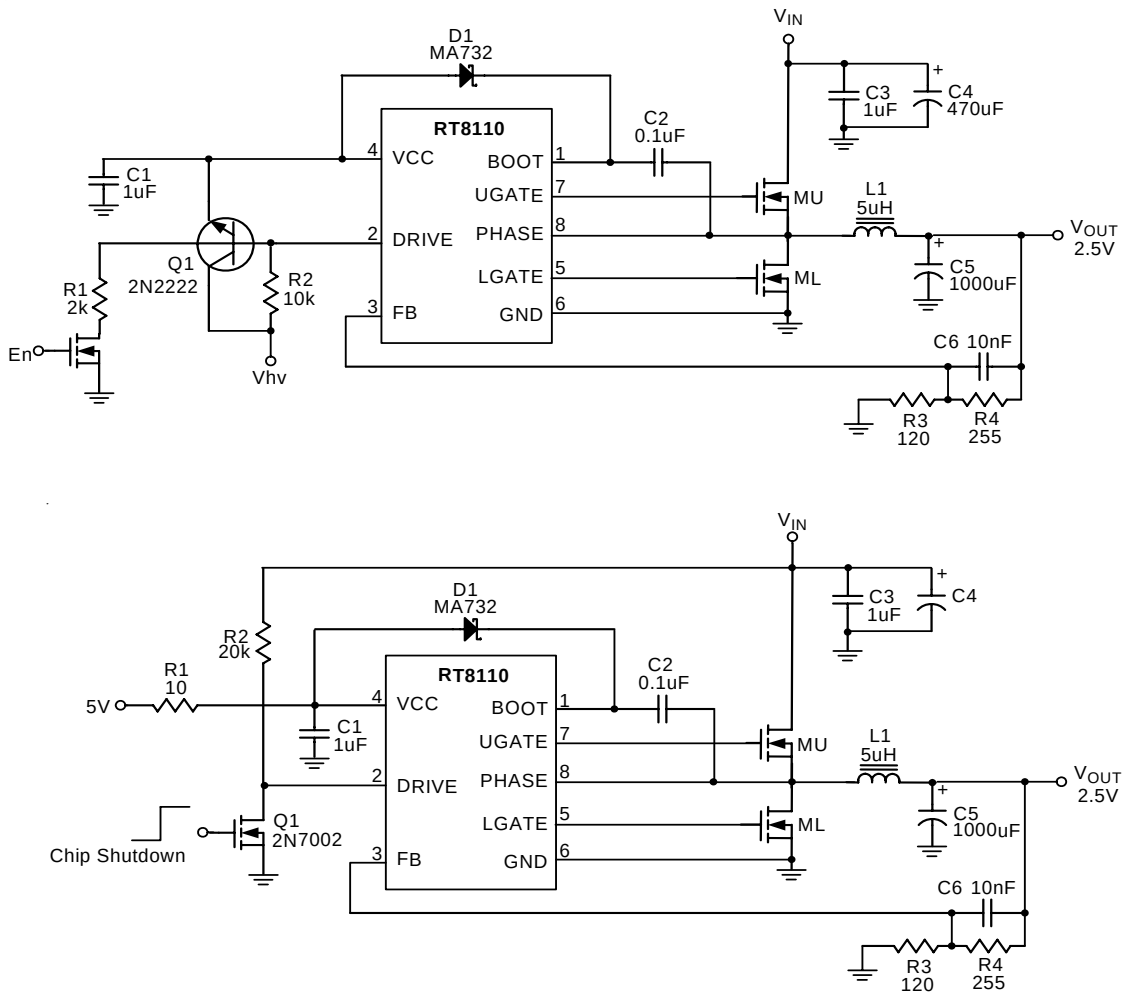
(TOP VIEW)



SOT-23-8

Note : There is no pin1 indicator on top mark for SOT-23-8 type, and pin 1 will be lower left pin when reading top mark from left to right.

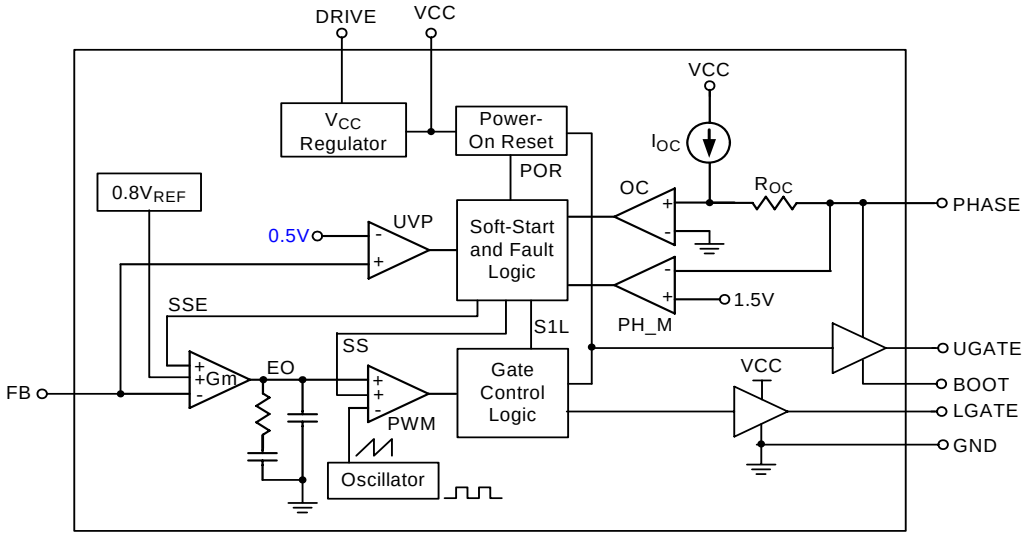
Typical Application Circuit



Functional Pin Description

Pin No.	Pin Name	Pin Function
1	BOOT	This pin provides ground referenced bias voltage to the upper MOSFET driver. A bootstrap circuit is used to create a voltage suitable to drive a logic-level N-MOSFET when operating at a single 5V power supply.
2	DRIVE	This pin connects to the base of the external BJT(2N2222), which is designed to withstand to 23V and provides a regulated 5.3V voltage to VCC pin as the power of the PWM controller. The pin also can function as shut down with two different application circuits. The one can pull low the pin to gnd, the other can pull low drive to make V_{DD} lower than POR threshold.
3	FB	This pin is connected to the PWM controller's output divider. This pin also connects to internal PWM error amplifier inverting input and protection monitor.
4	VCC	This is the main bias supply for the RT8110. This pin also provides the gate bias charge for the lower MOSFET gate. The voltage at this pin is monitored for power-on reset (POR) purpose.
5	LGATE	Connect LGATE to the PWM controller's lower MOSFET gate. This pin provides the gate drive for the lower MOSFET.
6	GND	Signal and power ground for the IC. All voltage levels are measured with respect to this pin.
7	UGATE	Connect UGATE pin to the PW M controller's upper MOSFET gate. This pin provides the gate drive for the upper MOSFET.
8	PHASE	This pin is used to monitor the voltage drop across the lower MOSFET for over-current protection.

Function Block Diagram



MP1411

2A, 18V, 380KHz Step-Down Converter

The Future of Analog IC Technology™

DESCRIPTION

The MP1411 is a monolithic step-down switch mode converter with a built in internal power MOSFET. It achieves 2A continuous output current over a wide input supply range with excellent load and line regulation.

Current mode operation provides fast transient response and eases loop stabilization.

Fault condition protection includes cycle-by-cycle current limiting and thermal shutdown. In shutdown mode the regulator draws 23µA of supply current. Programmable soft-start minimizes the inrush supply current and the output overshoot at initial startup.

The MP1411 requires a minimum number of readily available standard external components.

FEATURES

- 2A Output Current
- 0.2Ω Internal Power MOSFET Switch
- Stable with Low ESR Output Ceramic Capacitors
- Up to 95% Efficiency
- 23µA Shutdown Mode
- Fixed 380KHz Frequency
- Thermal Shutdown
- Cycle-by-Cycle Over Current Protection
- Wide 4.75V to 18V Operating Input Range
- Output Adjustable from 0.92V to 16V
- Programmable Under Voltage Lockout
- Available in an MSOP10 with Exposed Pad Package

APPLICATIONS

- Distributed Power Systems
- Battery Charger
- DSL Modems
- Pre-Regulator for Linear Regulators

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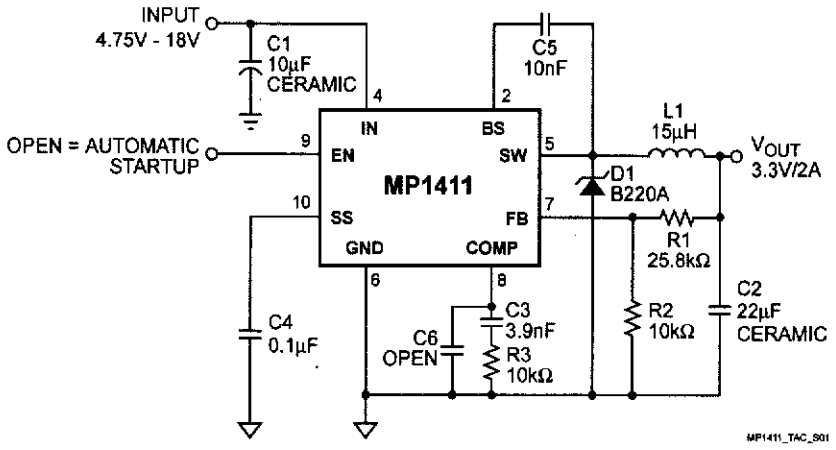
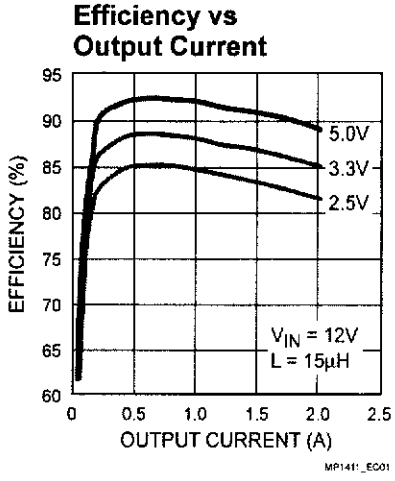
TYPICAL APPLICATION





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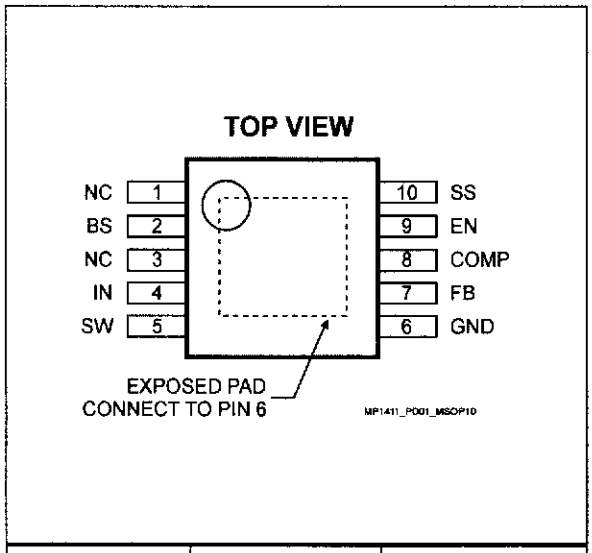
PACKAGE REFERENCE



Part Number*	Package	Temperature
MP1411DH	MSOP10	–40°C to +85°C

* For Tape & Reel, add suffix –Z (eg. MP1411DH–Z)
For Lead Free, add suffix –LF (eg. MP1411DH–LF–Z)

ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage (V_{IN}) 20V
Switch Node Voltage (V_{SW}) 21V
Bootstrap Voltage (V_{BS}) ..... V_{SW} + 6V
Feedback Voltage (V_{FB}) .....–0.3V to +6V
Enable/UVLO Voltage (V_{EN}).....–0.3V to +6V
Comp Voltage (V_{COMP}) .....–0.3V to +6V
SS Voltage (V_{SS}).....–0.3V to +6V
Junction Temperature.....+150°C
Lead Temperature .....+260°C
Storage Temperature .....–65°C to +150°C

Recommended Operating Conditions (2)

Supply Voltage (V_{IN}) .....4.75V to 18V
Operating Temperature.....–40°C to +85°C

Thermal Resistance (3) θ_{JA} θ_{JC}

MSOP10 with Exposed Pad .. 105 ..... 19... °C/W

Notes:
1) Exceeding these ratings may damage the device.
2) The device is not guaranteed to function outside of its operating conditions.
3) Measured on approximately 1" square of 1 oz copper.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_A = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Feedback Voltage	V_{FB}	4.75V ≤ V_{IN} ≤ 18V	0.892	0.920	0.948	V
Upper Switch On Resistance	$R_{DS(ON)1}$			0.2		Ω
Lower Switch On Resistance	$R_{DS(ON)2}$			10		Ω
Upper Switch Leakage		V_{EN} = 0V, V_{SW} = 0V		0	10	μA
Current Limit (4)			2.8	3.4		A
Current Sense Transconductance Output Current to Comp Pin Voltage	G_{CS}			1.95		A/V
Error Amplifier Voltage Gain	A_{VEA}			400		V/V
Error Amplifier Transconductance	G_{EA}	ΔI_C = ±10μA	550	830	1150	μA/V
Oscillator Frequency	f_S			380		KHz
Short Circuit Frequency		V_{FB} = 0V		240		KHz
Soft-Start Pin Equivalent Output Resistance				9		kΩ

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_A = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Maximum Duty Cycle	D_{MAX}	V_{FB} = 0.8V		90		%
Minimum On Time	t_{ON}			100		ns
EN Shutdown Threshold		I_{CC} > 100μA	0.7	1.0	1.3	V
Enable Pull Up Current		V_{EN} = 0V		1.0		μA
EN UVLO Threshold Rising		V_{EN} Rising	2.37	2.50	2.62	V
EN UVLO Threshold Hysteresis				210		mV
Supply Current (Shutdown)		$V_{EN} \leq 0.4V$		23	36	μA
Supply Current (Quiescent)		$V_{EN} \geq 3V$		1.1	1.3	mA
Thermal Shutdown				160		°C

Note:
4) Slope compensation changes current limit above 40% duty cycle.

PIN FUNCTIONS

Pin #	Name	Description
1	NC	No Connect.
2	BS	Bootstrap. This capacitor (C5) is needed to drive the power switch's gate above the supply voltage. It is connected between the SW and BS pins to form a floating supply across the power switch driver. The voltage across C5 is about 5V and is supplied by the internal +5V supply when the SW pin voltage is low.
3	NC	No Connect.
4	IN	Supply Voltage. The MP1411 operates from a +4.75V to +18V unregulated input. C1 is needed to prevent large voltage spikes from appearing at the input.
5	SW	Switch. This connects the inductor to either IN through M1 or to GND through M2.
6	GND	Ground. This pin is the voltage reference for the regulated output voltage. For this reason care must be taken in its layout. This node should be placed outside of the D1 to C1 ground path to prevent switching current spikes from inducing voltage noise into the part.
7	FB	Feedback. An external resistor divider from the output to GND, tapped to the FB pin, sets the output voltage. To prevent current limit runaway during a short circuit fault condition the frequency foldback comparator lowers the oscillator frequency when the FB voltage is below 400mV.
8	COMP	Compensation. This node is the output of the transconductance error amplifier and the input to the current comparator. Frequency compensation is done at this node by connecting a series R-C to ground. See the compensation section for exact details.
9	EN	Enable/UVLO. A voltage greater than 2.62V enables operation. Leave EN unconnected for automatic startup. An Under Voltage Lockout (UVLO) function can be implemented by the addition of a resistor divider from V_{IN} to GND. For complete low current shutdown the EN pin voltage needs to be less than 700mV.
10	SS	Soft-Start. Connect SS to an external capacitor to program the soft-start. If unused, leave it open.

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OPERATION

The MP1411 is a current mode regulator. That is, the COMP pin voltage is proportional to the peak inductor current. At the beginning of a cycle: the upper transistor M1 is off; the lower transistor M2 is on (see Figure 1); the COMP pin voltage is higher than the current sense amplifier output; and the current comparator's output is low. The rising edge of the 380KHz CLK signal sets the RS Flip-Flop. Its output turns off M2 and turns on M1 thus connecting the SW pin and inductor to the input supply. The increasing inductor current is sensed and amplified by the Current Sense Amplifier. Ramp compensation is summed to Current Sense Amplifier output and compared to the Error Amplifier output by the Current Comparator. When the Current Sense Amplifier plus Slope Compensation signal exceeds the COMP pin voltage, the RS Flip-Flop is reset and the MP1411 reverts to its initial M1 off, M2 on state. If the Current Sense Amplifier plus Slope Compensation signal does not exceed the COMP voltage, then the falling edge of the CLK resets the Flip-Flop.

The output of the Error Amplifier integrates the voltage difference between the feedback and the 0.92V bandgap reference. The polarity is such that an FB pin voltage lower than 0.92V increases the COMP pin voltage. Since the COMP pin voltage is proportional to the peak inductor current an increase in its voltage increases current delivered to the output. The lower 10Ω switch ensures that the bootstrap capacitor voltage is charged during light load conditions. External Schottky Diode D1 carries the inductor current when M1 is off.

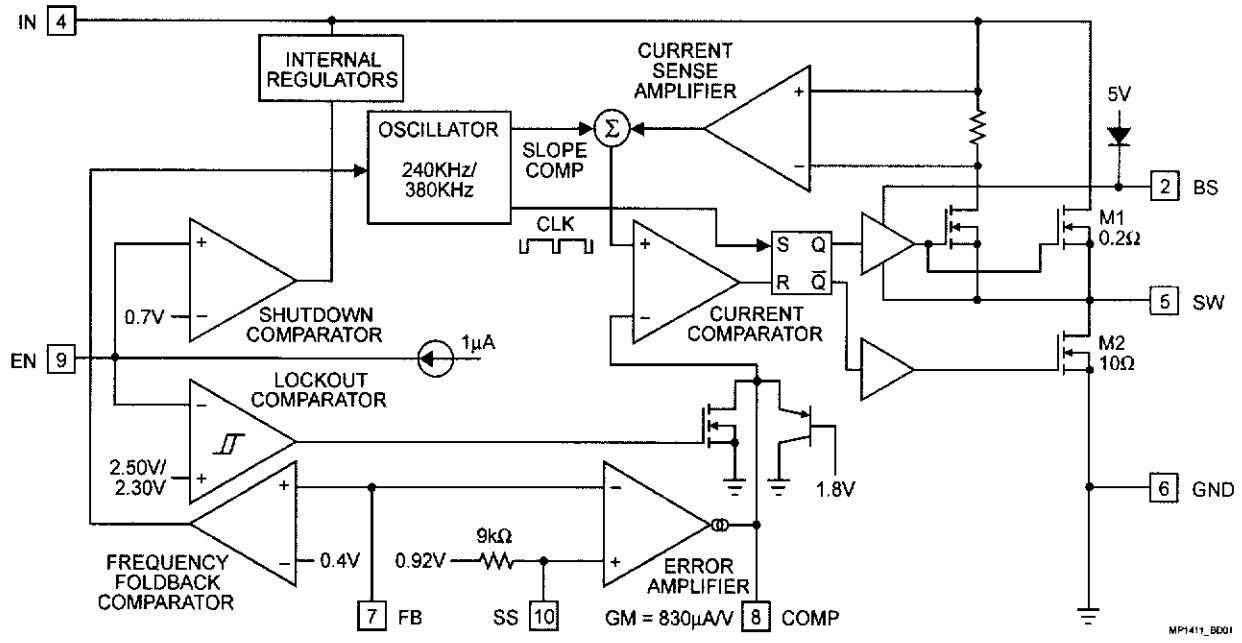

Figure 1—Functional Block Diagram

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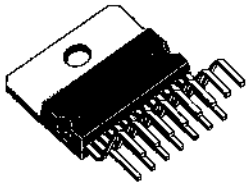
SGS-THOMSON MICROELECTRONICS

TDA7266

7+7W DUAL BRIDGE AMPLIFIER

- WIDE SUPPLY VOLTAGE RANGE (3-18V)
- MINIMUM EXTERNAL COMPONENTS
  - NO SWR CAPACITOR
  - NO BOOTSTRAP
  - NO BOUCHEROT CELLS
  - INTERNALLY FIXED GAIN
- STAND-BY & MUTE FUNCTIONS
- SHORT CIRCUIT PROTECTION
- THERMAL OVERLOAD PROTECTION

TECHNOLOGY BI20II



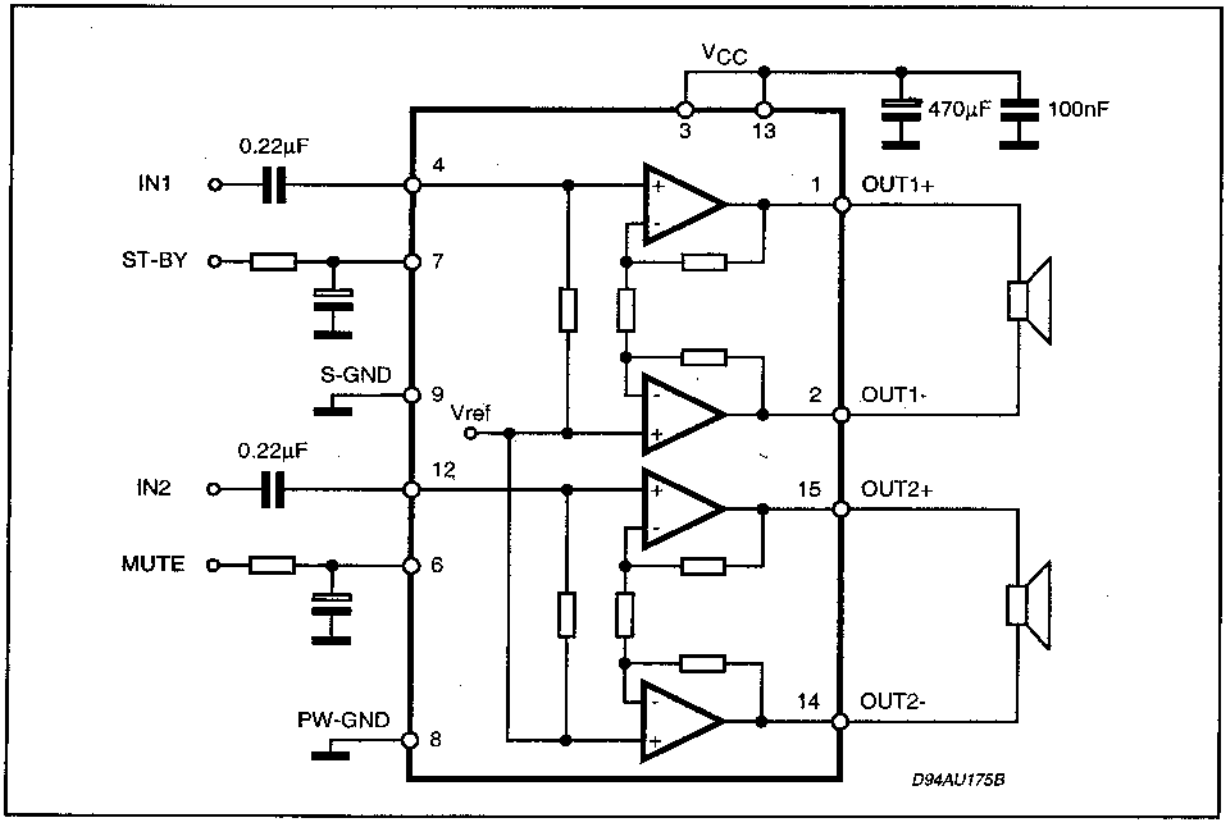
Multiwatt 15

ORDERING NUMBER: TDA7266

DESCRIPTION

The TDA7266 is a dual bridge amplifier specially designed for TV and Portable Radio applications.

BLOCK AND APPLICATION DIAGRAM



ALPHA & OMEGA SEMICONDUCTOR

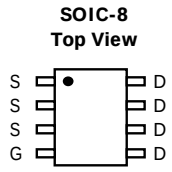
AO4459
P-Channel Enhancement Mode Field Effect Transistor

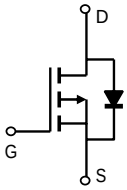
General Description

The AO4459 uses advanced trench technology to provide excellent $R_{DS(ON)}$ with low gate charge. This device is suitable for use as a load switch or in PWM applications. *Standard product AO4459 is Pb-free (meets ROHS & Sony 259 specifications). AO4459L is a Green Product ordering option. AO4459 and AO4459L are electrically identical*.

Features

V_{DS} (V) = -30V
I_D = -6.5A (V_{GS} = -10V)
$R_{DS(ON)}$ < 46mΩ (V_{GS} = -10V)
$R_{DS(ON)}$ < 72mΩ (V_{GS} = -4.5V)





Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	-30	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current [A]	T_A=25°C	I_D	-6.5	A
	T_A=70°C		-5.3	
Pulsed Drain Current [B]		I_{DM}	-30	
Power Dissipation [A]	T_A=25°C	P_D	3.1	W
	T_A=70°C		2	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	°C

Thermal Characteristics

Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	33	40	°C/W
Maximum Junction-to-Ambient [A]	Steady-State		62	75	°C/W
Maximum Junction-to-Lead [C]	Steady-State	$R_{\theta JL}$	18	24	°C/W

PHKD13N03LT

Dual TrenchMOS™ logic level FET

Rev. 01 — 23 June 2003 **Product data**

1. Product profile

1.1 Description

Dual N-channel enhancement mode field-effect transistor in a plastic package using TrenchMOS™ technology.

Product availability:

PHKD13N03LT in SOT96-1 (SO8).

1.2 Features

- Low gate charge
- Low on-state resistance
- Surface mount package
- Fast switching.

1.3 Applications

- Portable appliances
- Lithium-ion battery chargers
- Notebook computers
- DC-to-DC converters.

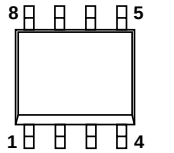
1.4 Quick reference data

- $V_{DS} \leq 30$ V
- $P_{tot} \leq 3.57$ W
- $I_D \leq 10.4$ A
- $R_{DSon} \leq 20$ mΩ

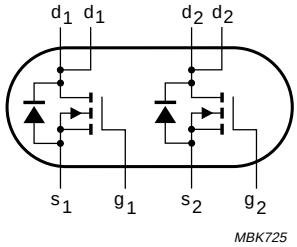
2. Pinning information

Table 1: Pinning - SOT96-1 (SO8), simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1	source1 (s1)		
2	gate1 (g1)		
3	source2 (s2)		
4	gate2 (g2)		
5,6	drain2 (d2)		
7,8	drain1 (d1)		



SOT96-1 (SO8)



MT35 BLOCK DIAGRAM V2.0

DC-DC
12V to 5V RT8110

+12V

POWER
SUPPLY CONNECTOR

+5V/
Standby+5v

VCC

ON

OFF

TUNER_I2C

IF+/IF-

8051 MCU
15 KEY 9 POWERON
11 STANDBY 14 IR

EEPROM
M24C16MN

TUNER

SAW-Sif

SAW-Vif

IF
amplif
ier

DVB-T
demodulat
or

PARALLEL TS

CI function Chip

PARALLEL TS

CI
CARD

PARALLEL TS

I2C

Main Chip

205 SCL
206 SDA

132 TV_CVBS
164 SIF

SERIAL TS

PANEL

KEY BOARD

152 KEY
93 IR

LVDS
To
TTL
386

LV
DS

TTL

FLASH
32Mbit

DDR
32Mb
x16

LVDS

Broken line is option for TTL interface panel!

62 OSCL1 63OSDA1
73 HDMI_5V
79 RX0_CB 80 RX0_C
81 RX0_0B 82 RXO_0
83 RX0_1B 84RXO_1
85 RX0_2B 86 RX0_2
205 DDC_SCL
204 DDC_SDA

104 R
98 B
102 G
96 VSYNC
97 HSYNC

120 Y_IN
121 Pb_IN
123 Pr_IN
173 YPbPr_L
174 YPbPr_R
176 VGA_R
177 VGA_L

170 SCT_R_IN
171 SCT_L_IN
116 SCT_R
108 SCT_G
114 SCT_B
149 SCT_FS
107 SCT_FB
187 SCT_R_OUT
189 SCT_L_OUT

201
SPDIF
_OUT

129 CVBS
172 R_IN
173 L_IN
126 SY
125 SC

185
HP_R_OUT
186
HP_L_OUT

R/L

PRE AUDIO
AMP

R

L

AUDIO
AMP

HEAD PHONE

CEC
COMMAND

HDMI SWITCH

EDID

EDID

EDID

O/P

HDMI1

HDM2

VGA

YPbPr

SCART

SPDIF

AV

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Z100
ANTPWR B1 NC/GND1 NC/GND2 NC/RFAGC NC TU GND1 NC1 SCL SDA AS ANALOG_IF IFAGC XTALOUT IFOUT2 IFOUT1
R124 100R
R125 100R
FAT_IN-
FAT_IN+
R148 0R
RF-AGC
C129 0.1U
R132 NC\0R
R135 4K7
IF_AGC
R127 100R
R126 100R
TUNER_SDA0_5V
TUNER_SCL0_5V
C125 22P
C124 22P
C100 1U
L103 120R
C130 0.01U
C122 0.1U
C102 100U
TUNER_5V
TUNER_5V
MT5133-GPIO-AD
C137 0.1U
C138 0.1U
U101 VCC GND 74LVC1G66GV
RF-AGC
R149 NC\0R
R153 0R
Q106 BC847C
R152 47K
C140 0.1U
L108 30R
AV_5V
R145 12K
ATV-IF-AGC
D110 LL4148
C139 0.1U
C2 47U
5V-OUT
R139 6K8
R140 6K8
R141 22K
D103 BA982
R137 220K
Q102 BC847C
R100 680K
C109 0.01U
R123 0R
X102 IN IN/GND GND OUT1 OUT2
D101 BA982
D102 BA982
C123 0.01U
R118 NC
L100 1UH
R113 6K8
R120 NC
R112 33R
L106 0
C104 0.01U
R109 2K2
R110 2K2
R108 5K6
C118 1000P
X101 IN IN/GND GND OUT1 OUT2
D100 BA592
C105 1000P
R111 2K2
R117 NC
L101 0.56UH
Q103 C124ET
R133 33R
C106 1000P
R119 5K6
0.01U C108
C107 390P
C116 0.01U
C117 0.47U
1000P C128
R101 330R
22K R121
R146 12K
ATV-IF-AGC
C119 NC/0.01U
C111 1500P
C110 0.22U
C114 0.47U
4M
X100
C112 20P
C115 0.1U
R114 22K
R147 NC/100K
C3 NC/0.01U
5V-OUT
L102 120R
TUNER_5V
C113 0.01U
C101 100U
BC847C
Q100
TV_CVBS
R129 75R
CVBS0
75R
R130
C121 47P
R131 0R
GND_TUNER
L107 120R
SIF
R128 0R
C131 0.01U
SIFP
C120 1P5
SIFN
C132 0.01U
R116 100R
TUNER_SCL0_5V
R115 100R
TUNER_SDA0_5V
R105
R103 NC\1K5
R104 NC\47R
NC/2K2
R138 220R
TUNER_SCL0
OSCL0
NC\100R
R93
TUNER_SDA0
OSDA0
R94 NC\100R
CVBS-OUT
SIF1 SIF2 OP2 AFC VP VPLL AGND CVBS VAGC REF TAGC NC
TDA9886T
U100 VIF1 VIF2 OP1 FMPLL DEEM AFD DGND AUD TOP SDA SCL SIOMAD
R106 NC\6K8
R102 NC\180R
C127 0.1U
Q101 NC\BC847C
R107 0R
AV_5V
R828 10K
Q105 2N7002
TUNER_SDA0
TUNER_SDA0_5V
DV33
AV_5V
R829 10K
Q104 2N7002
TUNER_SCL0
TUNER_SCL0_5V
DV33

Index-Lab	DATE	NAME	DESCRIPTION	Last modif

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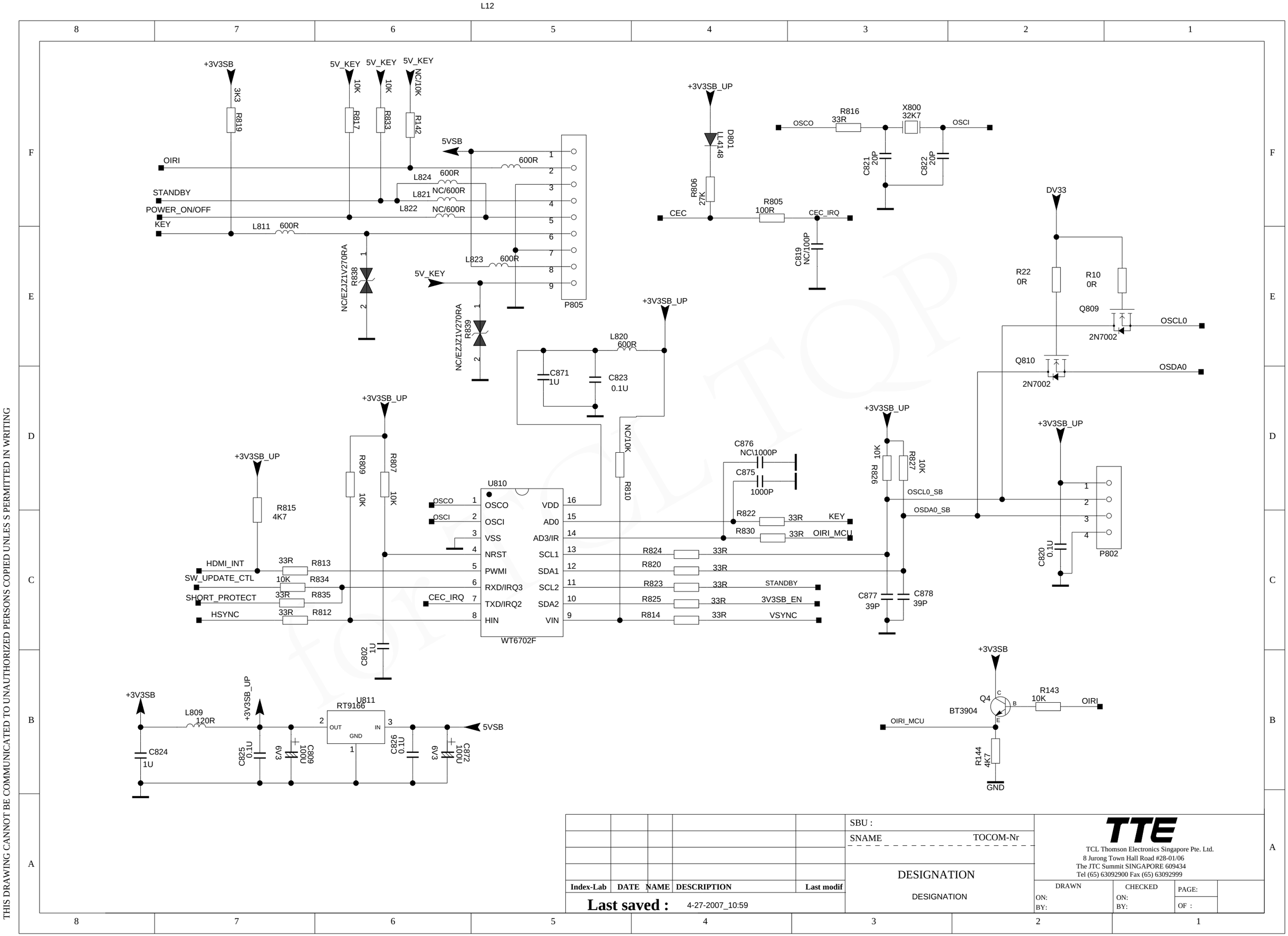

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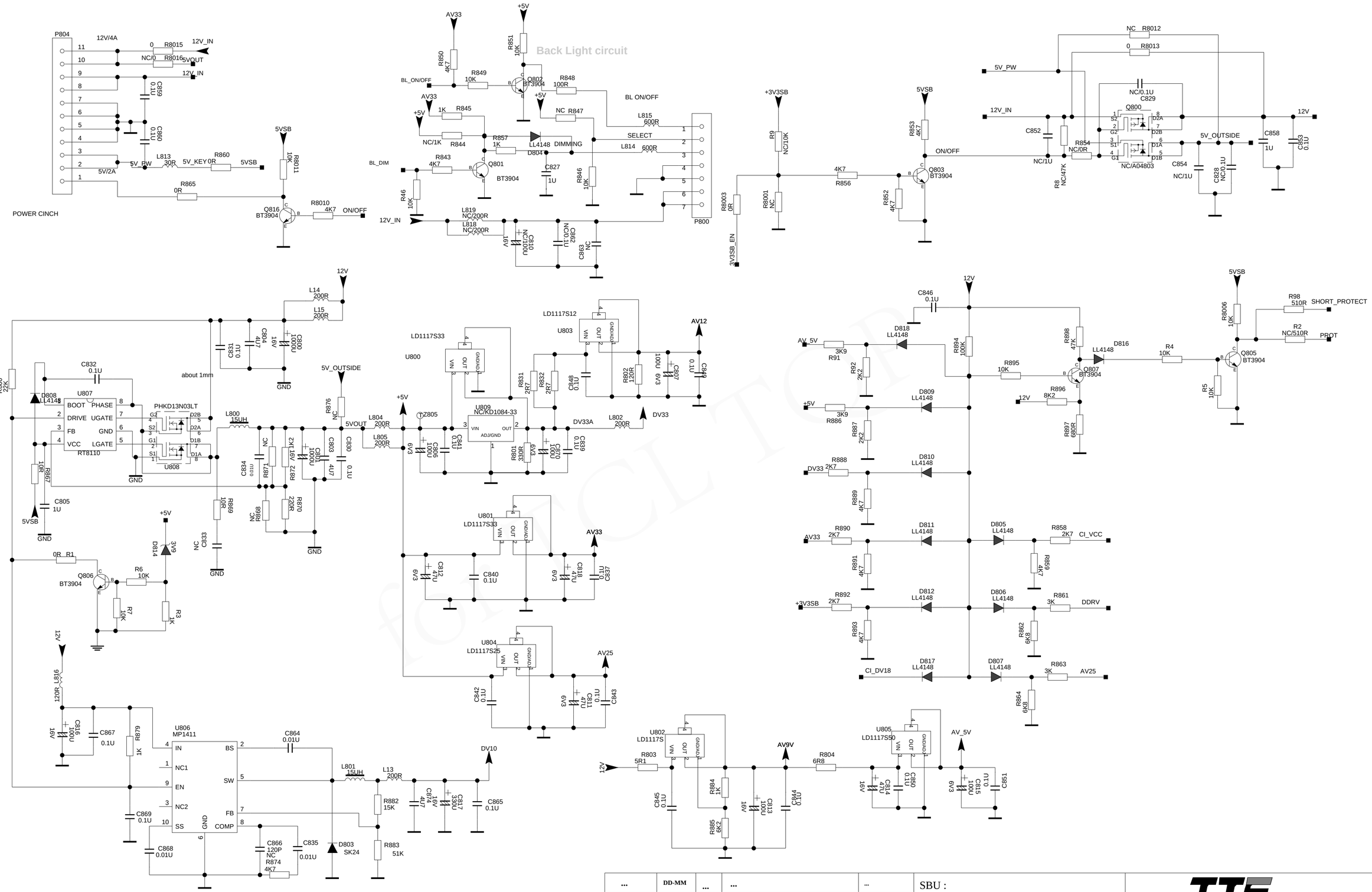

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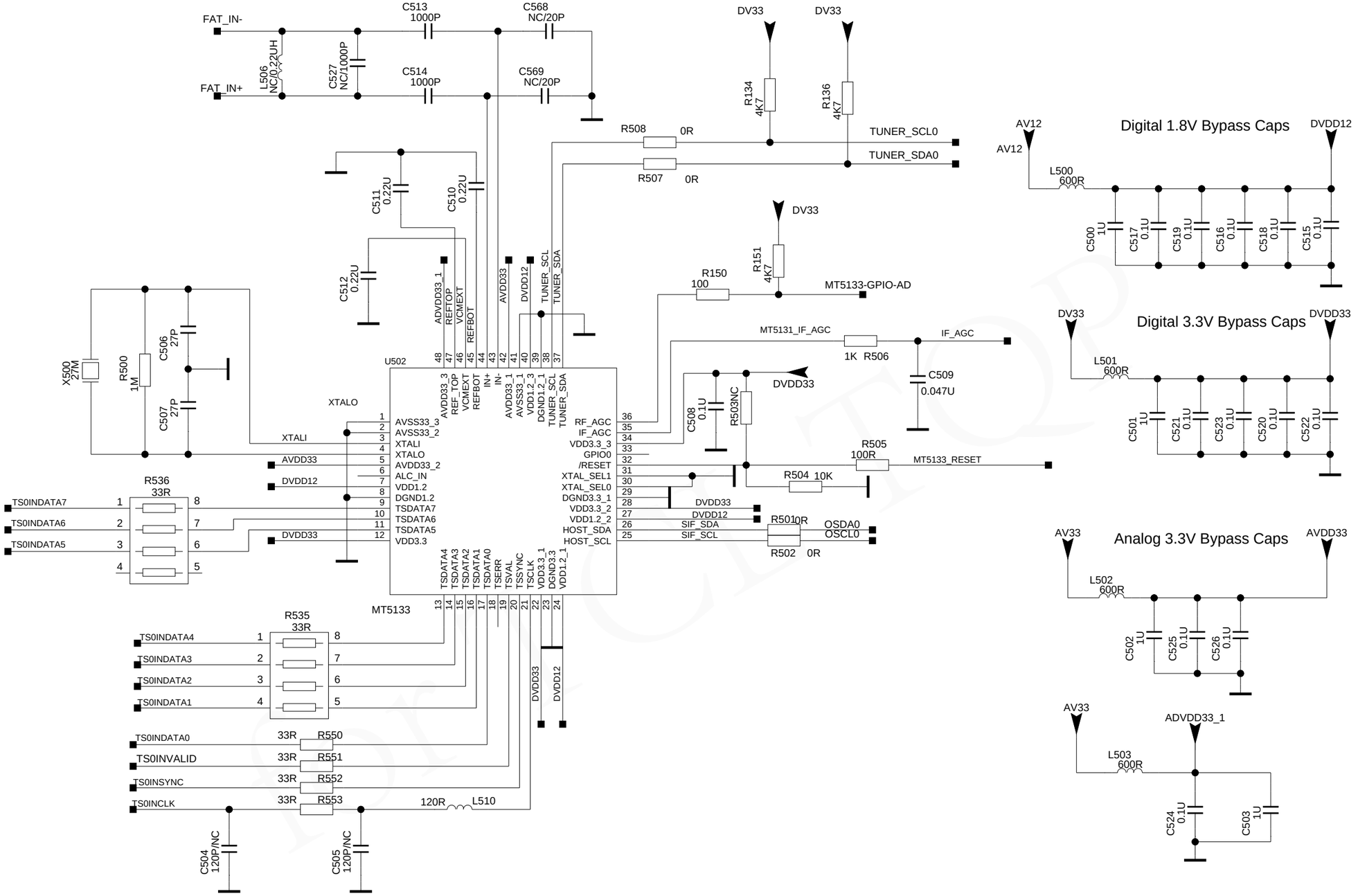

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Index-Lab	DATE	NAME	DESCRIPTION	Last modif	DESIGNATION	

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BY:	BY:	OF :

FORMAT DIN A3

CLOSE TO CI CONNECTOR

CI_VCC
CI_VCC
R517 NC/10K
R519 NC/10K
CI_INPACK#
CI_IOIS16#
R516 10K
R518 10K

CI_VCC
CI_VCC
CI_VCC
CI_DV33
R521 10K
R525 NC/10K
R522 10K
R541 4K7
CI_IREQ#
CI_VS2#
CI_WAIT#
CI_POCE1#

+5V
+5V
+5V
R520 10K
R523 10K
R524 10K
CI_CD1#
CI_VS1#
CI_CD2#

CI_CD1#
CI_CD2#
C561 0.1U
C562 0.1U

DV33
L508 600R
CI_DV33
C556 47U 6V3
LD1117S18
U500
VIN
OUT
GND/ADJ
CI_DV18
C557 47U 6V3

3.3V: 0.2W (60mA)
1.8V: 0.2W
(100mA)

CI_DV33
CI_AV33
L504 600R
C551 1U
C543 0.1U
C542 0.1U

CI_DV33
CLOSE TO MT8295
C1 1U
C533 0.1U
C531 0.1U
C532 0.1U
C539 0.1U
C538 0.1U
C535 0.1U
C534 0.1U
C537 0.1U
C536 0.1U

CI_DV18
C554 1U
C540 0.1U
C541 0.1U

CI_DV18
CI_AV18
L505 600R
C552 1U
C544 0.1U
C545 0.1U

CLOSE TO MT8295
C530 10P
TS_SYNCO
TS_DATAO
TS_CKO
TS_VALIDO
R538 33R
R539 33R
R540 33R
R554 33R
L511 120R

CLOSE TO MT8295
C528 27P
C529 27P
R509 1M
X501 27M

CI_DV33
R510 4K7
CI_GPIO0
R511 4K7
CI_GPIO1

DV33
NC/10K R512
CLOSE TO MT8295
0R R513
MTK_IC_RESET
4K7 R542

OPWM1
OPWM2
CI_DV33
4K7 R514

GND
Z501
RESET_N
GND

U501
CI_GPIO0 1
CI_GPIO1 2
HDMIED_WP 3
HPDIN 4
CI_DV33 5
VCC33 6
CI_INSYNC 7
CI_INVALID 8
CI_INDATA0 9
GND 10
CI_INDATA1 11
CI_INDATA2 12
CI_INDATA3 13
CI_INDATA4 14
CI_DV18 15
CI_INDATA5 16
CI_INDATA6 17
CI_INDATA7 18
HDMI_SEL 19
YPBPR_SW_IN 20
21
GND 22
CI_CD1# 23
CI_D3 24
CI_OUTDATA3 25
CI_D4 26
CI_OUTDATA4 27
CI_D5 28
CI_OUTDATA5 29
CI_D6 30
CI_OUTDATA6 31
CI_D7 32

GPIO0 GPIO1 GPIO2 GPIO3 VCC33 T0CLK_I T0SYNC_I T0VALID_I T0DATA0_I GND33 T0DATA1_I T0DATA2_I T0DATA3_I T0DATA4_I VCC18 T0DATA5_I T0DATA6_I T0DATA7_I GPIO4 GPIO5 GPIO6 GND18 CD1# D3 D11 D4 D12 D5 D13 D6 D14 D7

GPIO14 GPIO13 GPIO15 TS_SYNCO TS_DATAO TS_CKO TS_VALIDO GPIO12 GPIO11 GPIO10 GPIO9 CI_DATA0 CI_DATA1 CI_INT AVSS18_PLL AVDD18_PLL AVSS33_XTAL XTALI XTALO AVDD33_XTAL RESET# CI_RB CI_CLE GND33_4 CI_ALE CI_DATA3 CI_DATA4 CI_DATA5 CI_DATA6 CI_DATA7 VCC33_4

CI_WEB 96
CI_DATA2 95
CI_CEB 94
GPIO9 93
GPIO8 92
GPIO7 91
GND18_1 90
WP 89
CD2# 88
D2 87
D10 86
D1 85
D9 84
D0 83
VCC18_1 82
D8 81
A0 80
BVD1 79
A1 78
BVD2 77
GND33_2 76
A2 75
REG# 74
A3 73
INPACK# 72
A4 71
WAIT# 70
A5 69
VCC33_3 68
RESET 67
A6 66
VS2# 65

CI_PDD2 96
CI_PDD6 95
CI_PDD7 94
CI_VCC_EN 93
CI_VPP33_EN 92
CI_VPP5_EN 91
GND 90
CI_IOIS16# 89
CI_CD2# 88
CI_D2 87
CI_OUTDATA2 86
CI_D1 85
CI_OUTDATA1 84
CI_D0 83
CI_DV18 82
CI_OUTDATA0 81
CI_A0 80
CI_OUTSYNC 79
CI_A1 78
CI_OUTVALID 77
GND 76
CI_A2 75
CI_REG# 74
CI_A3 73
CI_INPACK# 72
CI_A4 71
CI_WAIT# 70
CI_A5 69
CI_DV33 68
CI_RESET 67
CI_A6 66
CI_OUTCLK 65

MT8295

VCC33_1 D15 CE1# CE2# A10 VS1# IOR# IOWR# A11 A9 A8 A13 A18 A19 A14 A20 VCC33_2 WE# A21 READY A22 A16 A15 GND33_3 A24 A12 A25 A7

CI_DV33 CI_OUTDATA7 CI_CE1## CI_CE2## CI_VS1# CI_OE## CI_IORD## CI_IOWR## GND CI_INSYNC CI_A9 CI_INDATA0 CI_A13 CI_INDATA1 CI_A14 CI_INDATA2 CI_A20 CI_INDATA3 CI_WE## CI_IREQ# CI_INVALID CI_A11 CI_INDATA4 CI_INDATA5

GND CI_INDATA6 CI_A12 CI_INDATA7 CI_A7

R515 100R
CI_INCLK
C563 10P

CI_CE1##
R543 100R
CI_CE1#
C564 10P

CI_IORD##
R547 100R
CI_IORD#
C549 10P

CI_WE##
R545 100R
CI_WE#
C566 10P

CI_OE##
R544 100R
CI_OE#
C565 10P

CI_IOWR##
R548 100R
CI_IOWR#
C548 10P

CLOSE TO CI CONNECTOR

+5V
C547 1U
C546 0.1U
R526 10K
L509 NC/30R
U503
R19711
VIN
EN/EN#
GND
VOUT
FLG
C559 0.1U
L507 30R
L512 30R
CI_VPP
CI_VCC
C560 100U 6V3
C558 0.1U
CI_VCC_EN
R527 NC/0R

P500
CI_D3 1
CI_D4 2
CI_D5 3
CI_D6 4
CI_D7 5
CI_CE1# 6
CI_A10 7
CI_OE# 8
CI_A11 9
CI_A9 10
CI_A8 11
CI_A13 12
CI_A14 13
CI_WE# 14
CI_IREQ# 15
16
17
CI_INVALID 18
CI_INCLK 19
CI_A12 20
CI_A7 21
CI_A6 22
CI_A5 23
CI_A4 24
CI_A3 25
CI_A2 26
CI_A1 27
CI_A0 28
CI_D0 29
CI_D1 30
CI_D2 31
32
CI_IOIS16# 33
34

35 CI_CD1#
36 CI_OUTDATA3
37 CI_OUTDATA4
38 CI_OUTDATA5
39 CI_OUTDATA6
40 CI_OUTDATA7
41 CI_CE2#
42 CI_VS1#
43 CI_IORD#
44 CI_IOWR#
45 CI_INSYNC
46 CI_INDATA0
47 CI_INDATA1
48 CI_INDATA2
49 CI_INDATA3
50
51
52 CI_INDATA4
53 CI_INDATA5
54 CI_INDATA6
55 CI_INDATA7
56 CI_VS2#
57 CI_RESET
58 CI_WAIT#
59
60
61 CI_REG#
62 CI_OUTVALID
63 CI_OUTSYNC
64 CI_OUTDATA0
65 CI_OUTDATA1
66 CI_OUTDATA2
67 CI_CD2#
68

CI_VCC
CI_VPP
CI_VCC
CI_VPP
R533 100R
NC\0R
R532
CI_OUTCLK
C567 10P
CI_INPACK#
NC/0R
R531

CLOSE TO MT8295

...	DD-MM	...	...	...	SBU :	
...	DD-MM	...	...	...	TCLNO:	
...	DD-MM	...	...	...	.....	
...	DD-MM	...	...	...	DESIGNATION	
Index-Lab	DATE	NAME	DESCRIPTION	Last modif	.....	

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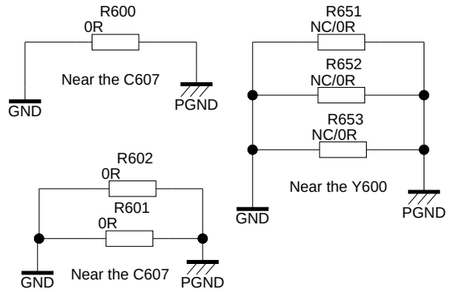

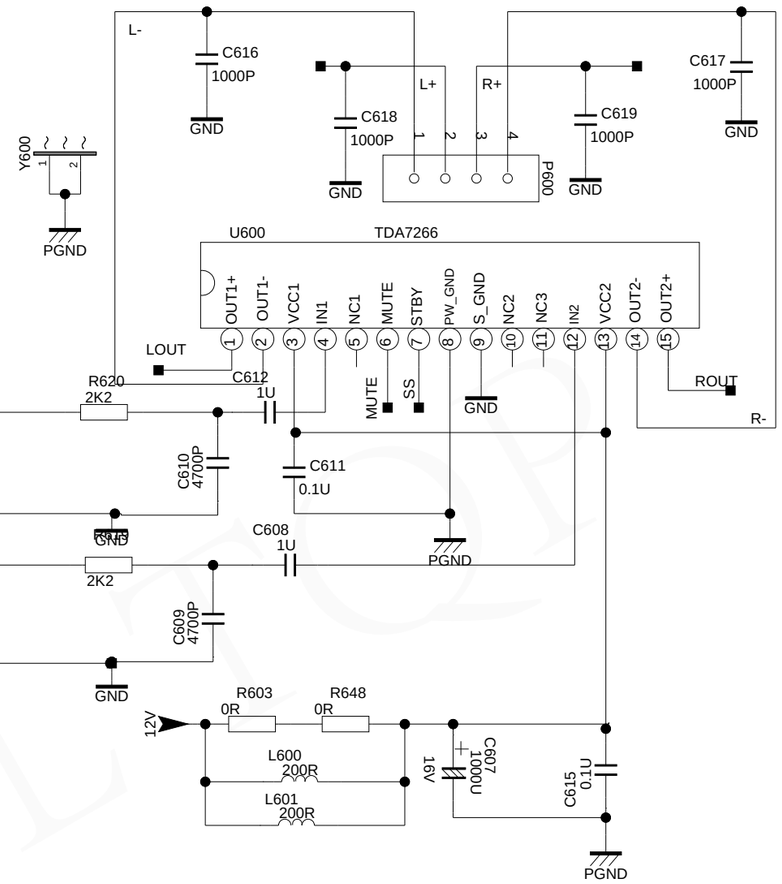

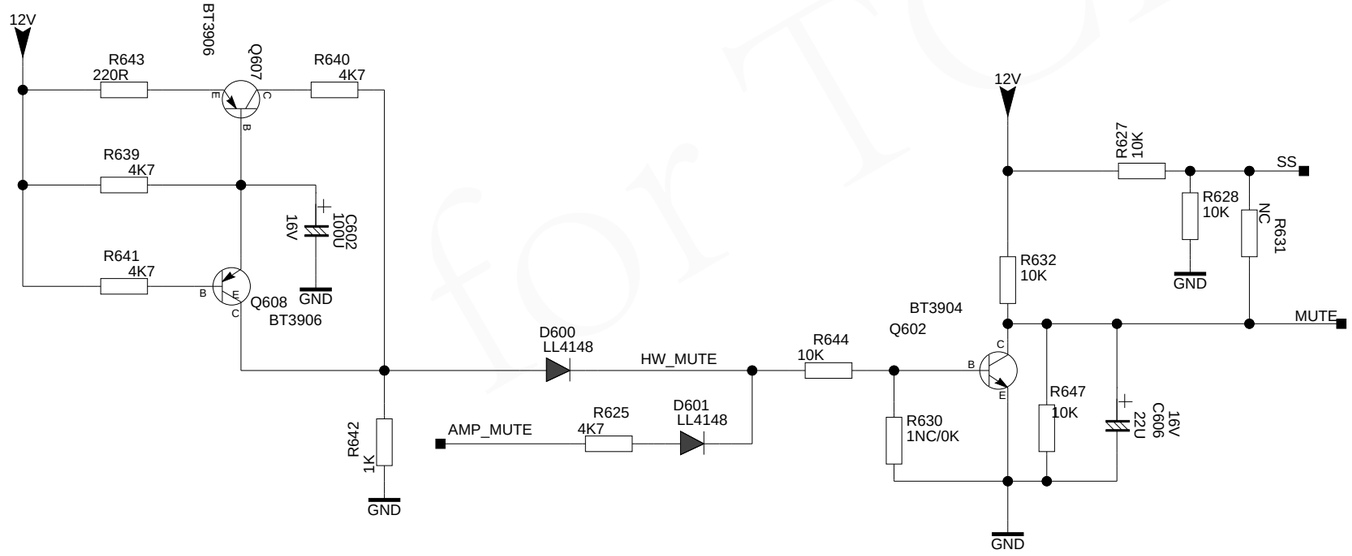

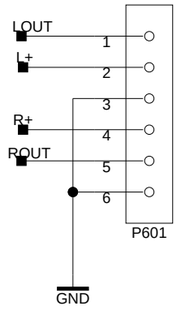

Index-Lab	DATE	NAME	DESCRIPTION	Last modif

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SBU :

SNAME TOCOM-Nr

DESIGNATION

DESIGNATION

TCL Thomson Electronics Singapore Pte. Ltd.
8 Jurong Town Hall Road #28-01/06
The JTC Summit SINGAPORE 609434
Tel (65) 63092900 Fax (65) 63092999

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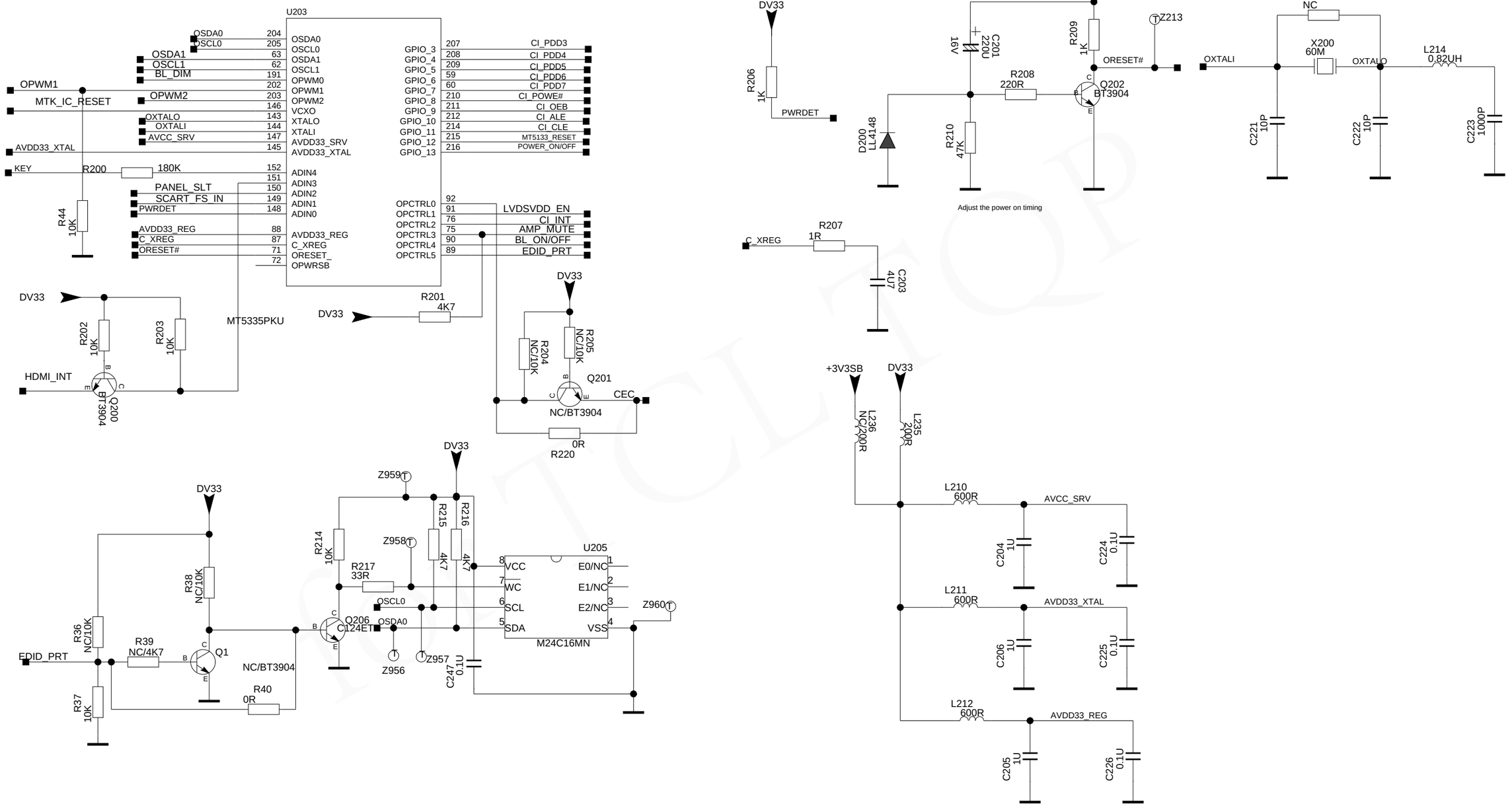

Index-Lab	DATE	NAME	DESCRIPTION	Last modif

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SBU :

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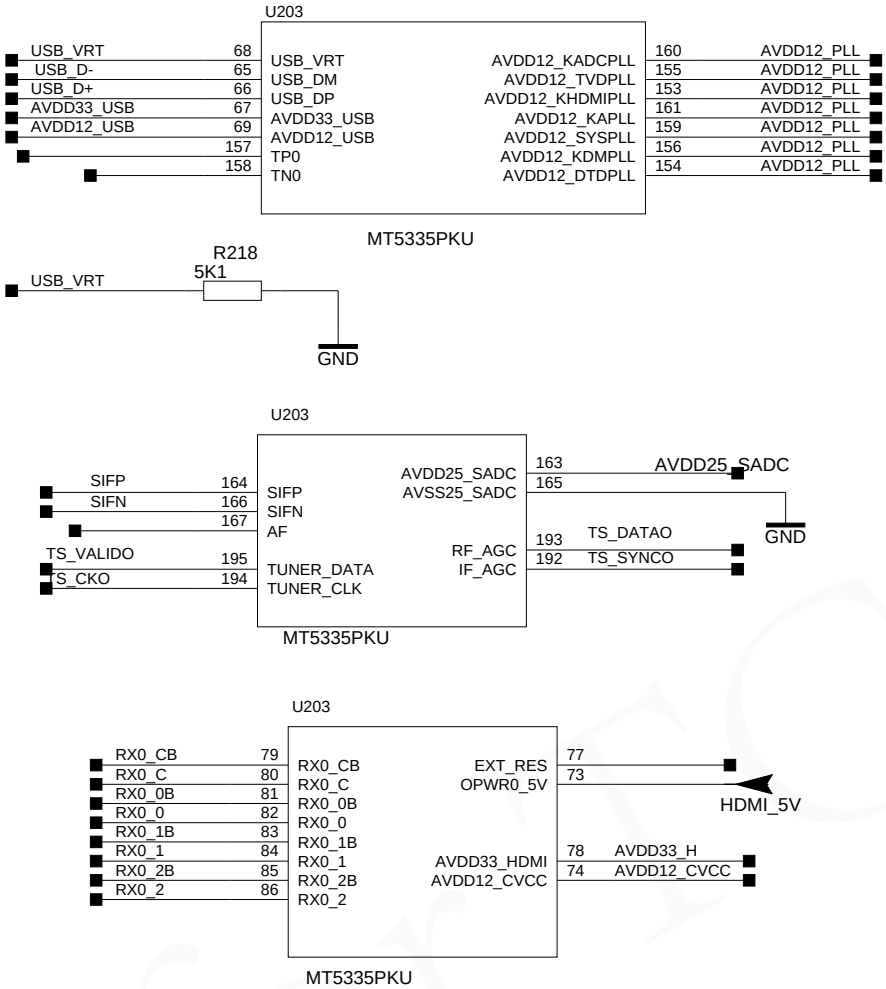
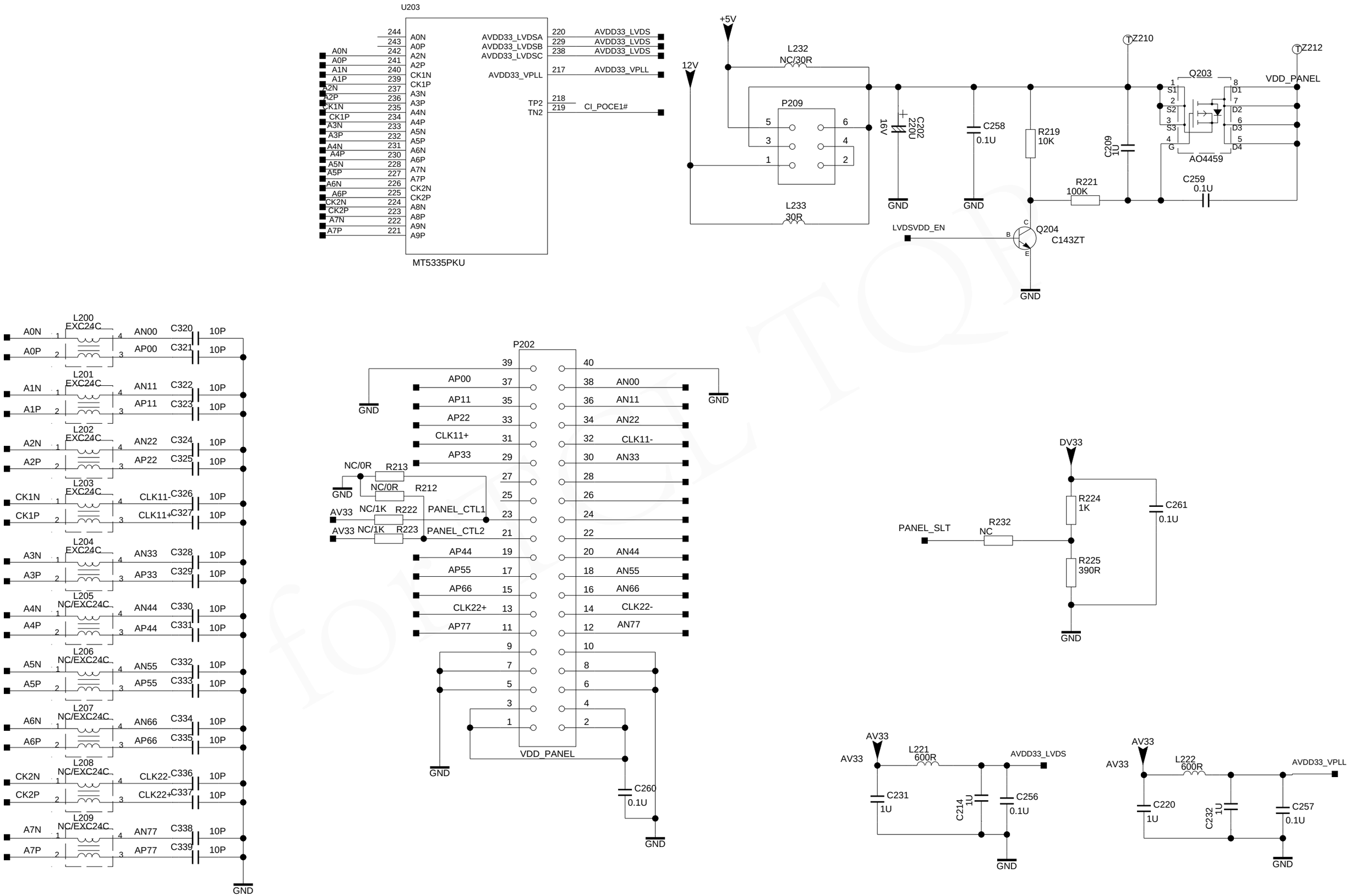
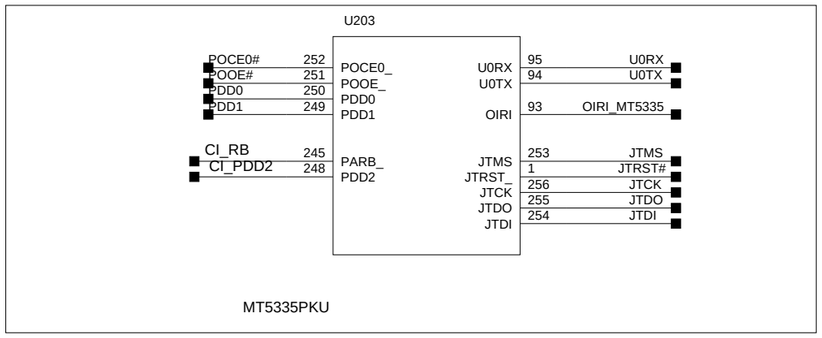
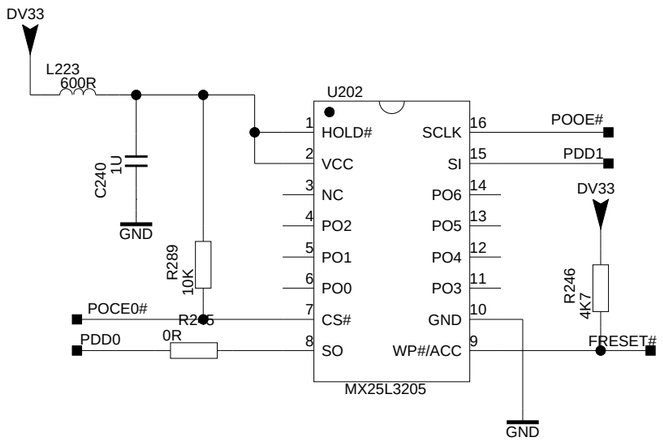
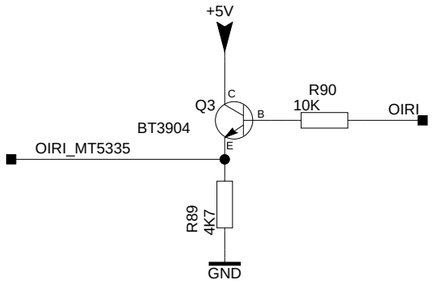
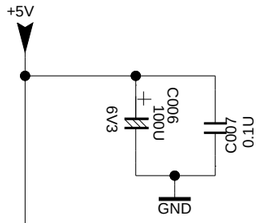

U203
USB_VRT 68
USB_D- 65
USB_D+ 66
AVDD33_USB 67
AVDD12_USB 69
157
158
USB_VRT
USB_DM
USB_DP
AVDD33_USB
AVDD12_USB
TP0
TN0
AVDD12_KADCPLL 160
AVDD12_TVDPLL 155
AVDD12_KHDMIPLL 153
AVDD12_KAPLL 161
AVDD12_SYSPLL 159
AVDD12_KDMPLL 156
AVDD12_DTDPLL 154
AVDD12_PLL
MT5335PKU
R218
5K1
USB_VRT
GND
U203
SIFP 164
SIFN 166
167
TS_VALIDO 195
S_CKO 194
SIFP
SIFN
AF
TUNER_DATA
TUNER_CLK
AVDD25_SADC 163
AVSS25_SADC 165
RF_AGC
IF_AGC
193 TS_DATAO
192 TS_SYNCO
AVDD25_SADC
GND
MT5335PKU
U203
RX0_CB 79
RX0_C 80
RX0_0B 81
RX0_0 82
RX0_1B 83
RX0_1 84
RX0_2B 85
RX0_2 86
RX0_CB
RX0_C
RX0_0B
RX0_0
RX0_1B
RX0_1
RX0_2B
RX0_2
EXT_RES 77
OPWR0_5V 73
AVDD33_HDMI 78
AVDD12_CVCC 74
AVDD33_H
AVDD12_CVCC
HDMI_5V
MT5335PKU
AV12
L217
600R
AVDD12_USB
C210
1U
C252
0.1U
GND
AV33
L216
600R
AVDD33_USB
C208
1U
C251
0.1U
GND
AV33
L219
600R
AVDD33_H
C230
1U
C212
1U
C255
0.1U
GND
AV12
L220
600R
AVDD12_CVCC
C213
1U
C248
0.1U
GND
AV25
L218
600R
AVDD25_SADC
C229
1U
C211
1U
C253
0.01U
C254
0.1U
GND
AV12
L215
600R
AVDD12_PLL
C228
1U
C207
1U
C249
0.01U
C250
0.1U
GND

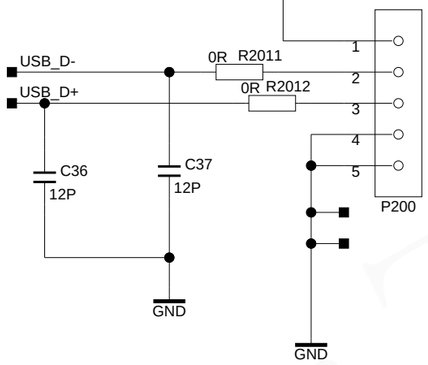

U203
MT5335PKU
AVDD33_LVDSA
AVDD33_LVDSB
AVDD33_LVDSC
AVDD33_VPLL
TP2
TN2
AVDD33_LVDS
AVDD33_LVDS
AVDD33_LVDS
AVDD33_VPLL
CI_POCE1#
+5V
12V
L232
NC/30R
P209
L233
30R
C202
220U
16V
C258
0.1U
R219
10K
R221
100K
C209
1U
Z210
Z212
Q203
AO4459
VDD_PANEL
C259
0.1U
LVDSVDD_EN
Q204
C143ZT
GND
L200
EXC24C
L201
EXC24C
L202
EXC24C
L203
EXC24C
L204
EXC24C
L205
NC/EXC24C
L206
NC/EXC24C
L207
NC/EXC24C
L208
NC/EXC24C
L209
NC/EXC24C
P202
VDD_PANEL
C260
0.1U
NC/0R
R213
R212
NC/1K
R222
R223
PANEL_CTL1
PANEL_CTL2
AV33
DV33
R224
1K
R225
390R
R232
NC
PANEL_SLT
C261
0.1U
L221
600R
AVDD33_LVDS
C231
1U
C214
1U
C256
0.1U
L222
600R
AVDD33_VPLL
C220
1U
C232
1U
C257
0.1U

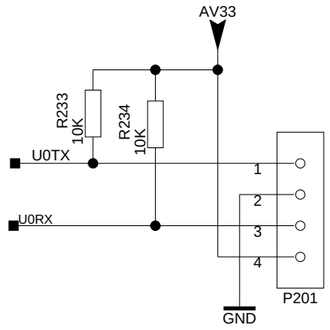


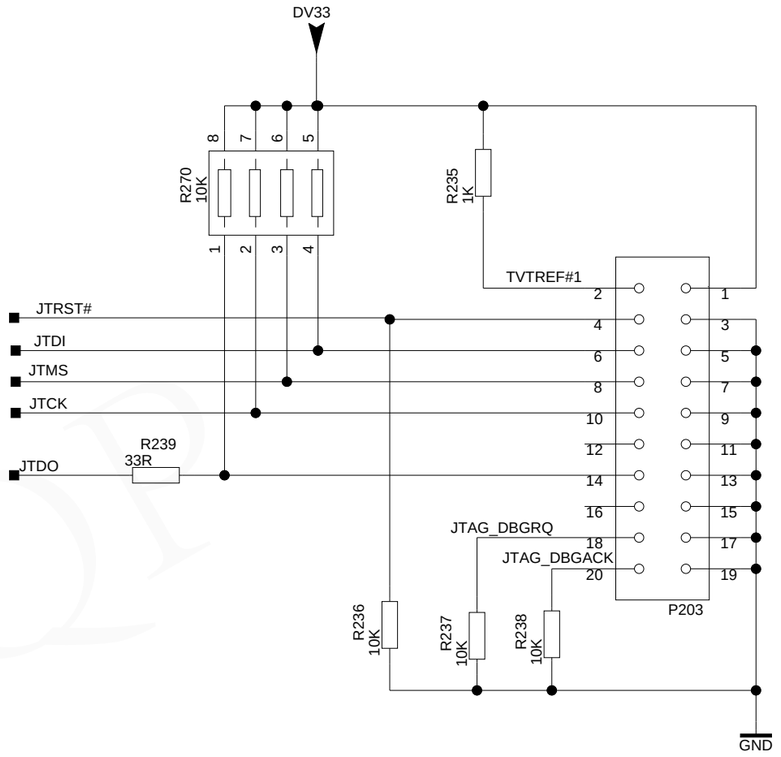


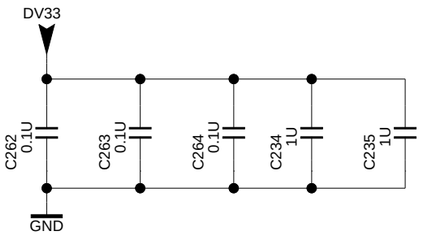


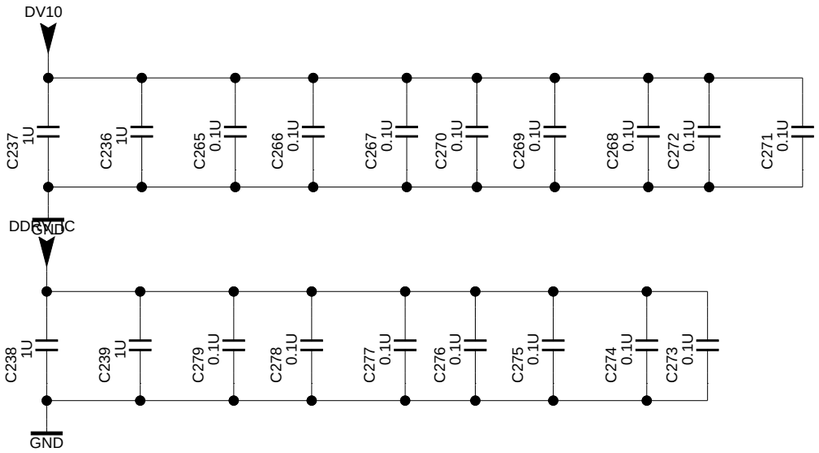


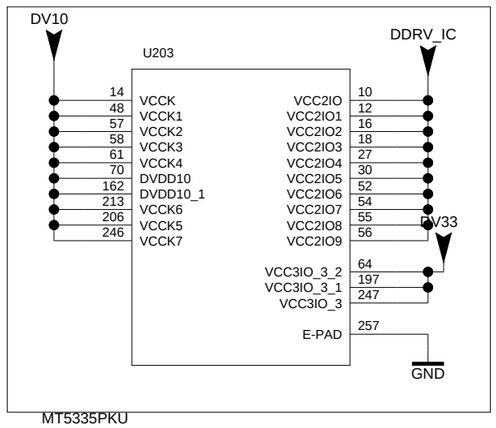


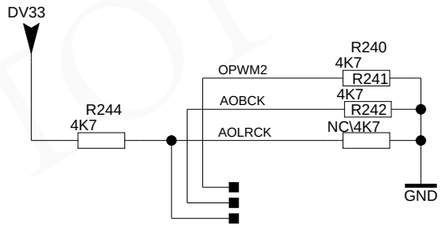










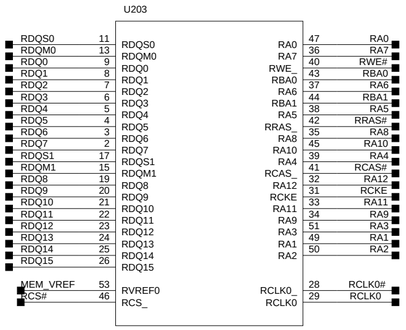


Trap MODE	OPWM2	AOBLK	AOLRCK
NORMAL MODE	0	0	0
ICE MODE	0	0	1

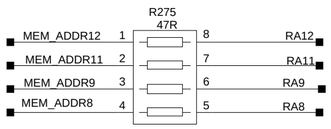
TRAP MODE	OPCTRL5	OPCTRL4
CORE RESET 1 US	0	1

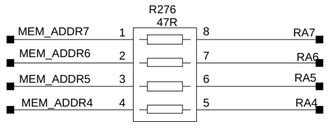
forTOP

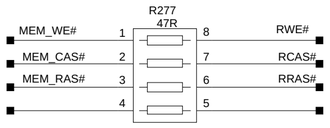
5 4 3 2 1

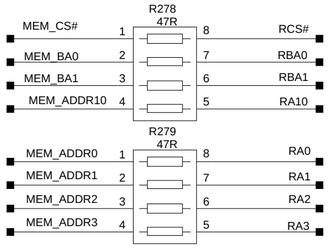

U203
RDQS0 11
RDQM0 13
RDQ0 9
RDQ1 8
RDQ2 7
RDQ3 6
RDQ4 5
RDQ5 4
RDQ6 3
RDQ7 2
RDQS1 17
RDQM1 15
RDQ8 19
RDQ9 20
RDQ10 21
RDQ11 22
RDQ12 23
RDQ13 24
RDQ14 25
RDQ15 26
MEM_VREF 53
RCS# 46
RDQS0
RDQM0
RDQ0
RDQ1
RDQ2
RDQ3
RDQ4
RDQ5
RDQ6
RDQ7
RDQS1
RDQM1
RDQ8
RDQ9
RDQ10
RDQ11
RDQ12
RDQ13
RDQ14
RDQ15
RVREF0
RCS_
RA0 47
RA7 36
RWE_ 40
RBA0 43
RA6 37
RBA1 44
RA5 38
RRAS_ 42
RA8 35
RA10 45
RA4 39
RCAS_ 41
RA12 32
RCKE 31
RA11 33
RA9 34
RA3 51
RA1 49
RA2 50
RCLK0_ 28
RCLK0 29
RA0
RA7
RWE_
RBA0
RA6
RBA1
RA5
RRAS_
RA8
RA10
RA4
RCAS_
RA12
RCKE
RA11
RA9
RA3
RA1
RA2
RCLK0_
RCLK0

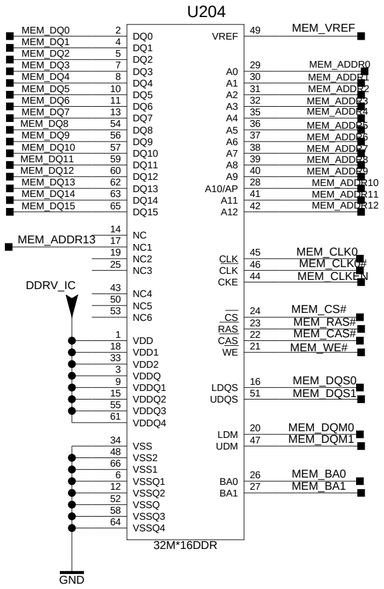
MT5335PKU

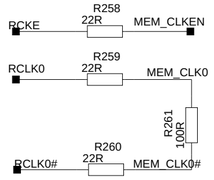

R275
47R
MEM_ADDR12 1
MEM_ADDR11 2
MEM_ADDR9 3
MEM_ADDR8 4
8 RA12
7 RA11
6 RA9
5 RA8

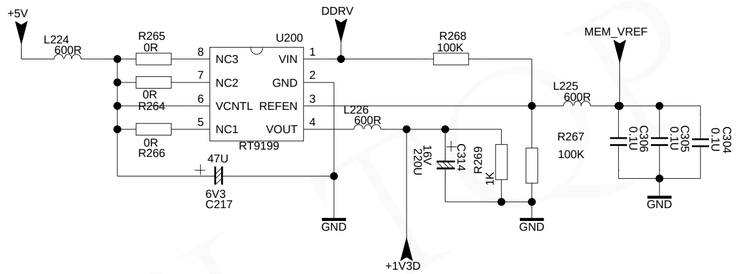

R276
47R
MEM_ADDR7 1
MEM_ADDR6 2
MEM_ADDR5 3
MEM_ADDR4 4
8 RA7
7 RA6
6 RA5
5 RA4

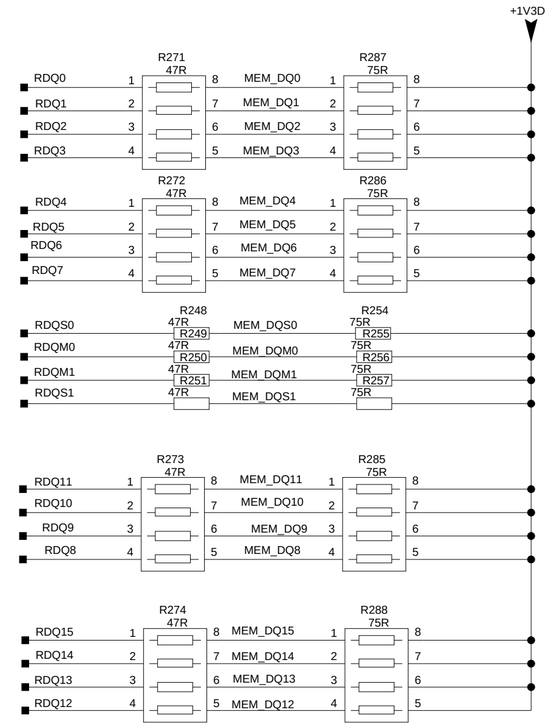

R277
47R
MEM_WE# 1
MEM_CAS# 2
MEM_RAS# 3
4
8 RWE#
7 RCAS#
6 RRAS#
5

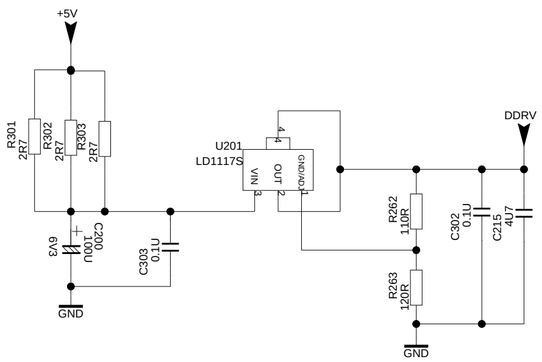

R278
47R
MEM_CS# 1
MEM_BA0 2
MEM_BA1 3
MEM_ADDR10 4
8 RCS#
7 RBA0
6 RBA1
5 RA10
R279
47R
MEM_ADDR0 1
MEM_ADDR1 2
MEM_ADDR2 3
MEM_ADDR3 4
8 RA0
7 RA1
6 RA2
5 RA3

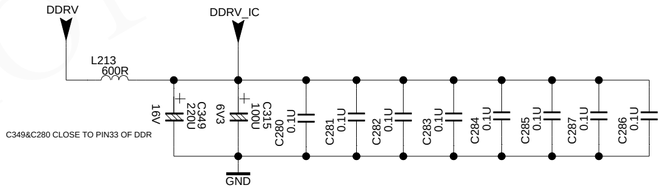

U204
MEM_DQ0 2
MEM_DQ1 4
MEM_DQ2 5
MEM_DQ3 7
MEM_DQ4 8
MEM_DQ5 10
MEM_DQ6 11
MEM_DQ7 13
MEM_DQ8 54
MEM_DQ9 56
MEM_DQ10 57
MEM_DQ11 59
MEM_DQ12 60
MEM_DQ13 62
MEM_DQ14 63
MEM_DQ15 65
MEM_ADDR13 14
DDRV_IC
43
50
53
1
18
33
3
9
15
55
61
34
48
66
6
12
52
58
64
GND
DQ0
DQ1
DQ2
DQ3
DQ4
DQ5
DQ6
DQ7
DQ8
DQ9
DQ10
DQ11
DQ12
DQ13
DQ14
DQ15
NC
NC1
NC2
NC3
NC4
NC5
NC6
VDD
VDD1
VDD2
VDDQ
VDDQ1
VDDQ2
VDDQ3
VDDQ4
VSS
VSS2
VSS1
VSSQ1
VSSQ2
VSSQ
VSSQ3
VSSQ4
32M*16DDR
VREF 49
MEM_VREF
A0 29
A1 30
A2 31
A3 32
A4 35
A5 36
A6 37
A7 38
A8 39
A9 40
A10/AP 28
A11 41
A12 42
MEM_ADDR0
MEM_ADDR1
MEM_ADDR2
MEM_ADDR3
MEM_ADDR4
MEM_ADDR5
MEM_ADDR6
MEM_ADDR7
MEM_ADDR8
MEM_ADDR9
MEM_ADDR10
MEM_ADDR11
MEM_ADDR12
CLK 45
CLK 46
CKE 44
MEM_CLK0
MEM_CLK0#
MEM_CLKEN
CS 24
RAS 23
CAS 22
WE 21
MEM_CS#
MEM_RAS#
MEM_CAS#
MEM_WE#
LDQS 16
UDQS 51
MEM_DQS0
MEM_DQS1
LDM 20
UDM 47
MEM_DQM0
MEM_DQM1
BA0 26
BA1 27
MEM_BA0
MEM_BA1

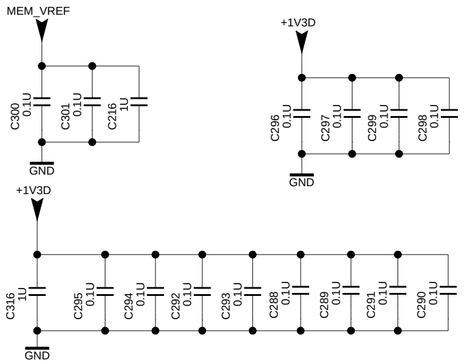

RCKE
R258
22R
MEM_CLKEN
RCLK0
R259
22R
MEM_CLK0
R261
10R
RCLK0#
R260
22R
MEM_CLK0#

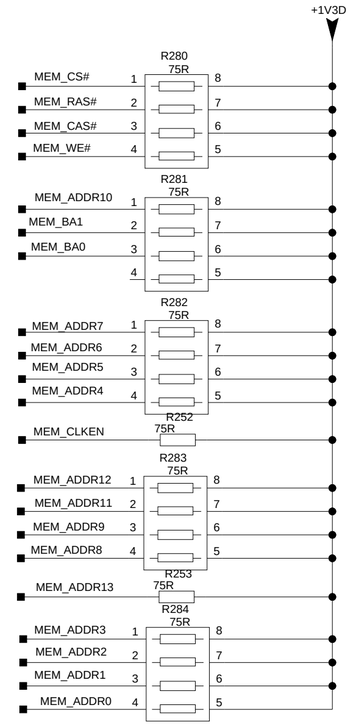

+5V
L224
600R
R265
0R
R264
0R
R266
0R
U200
NC3
NC2
VCNTL
NC1
VIN
GND
REFEN
VOUT
RT9199
DDRV
R268
100K
L226
600R
47U
6V3
C217
GND
+1V3D
L225
600R
MEM_VREF
R267
100K
C306
0.1U
C305
0.1U
C304
0.1U
GND
16V
220U
C314
6V3
R262
1K
GND

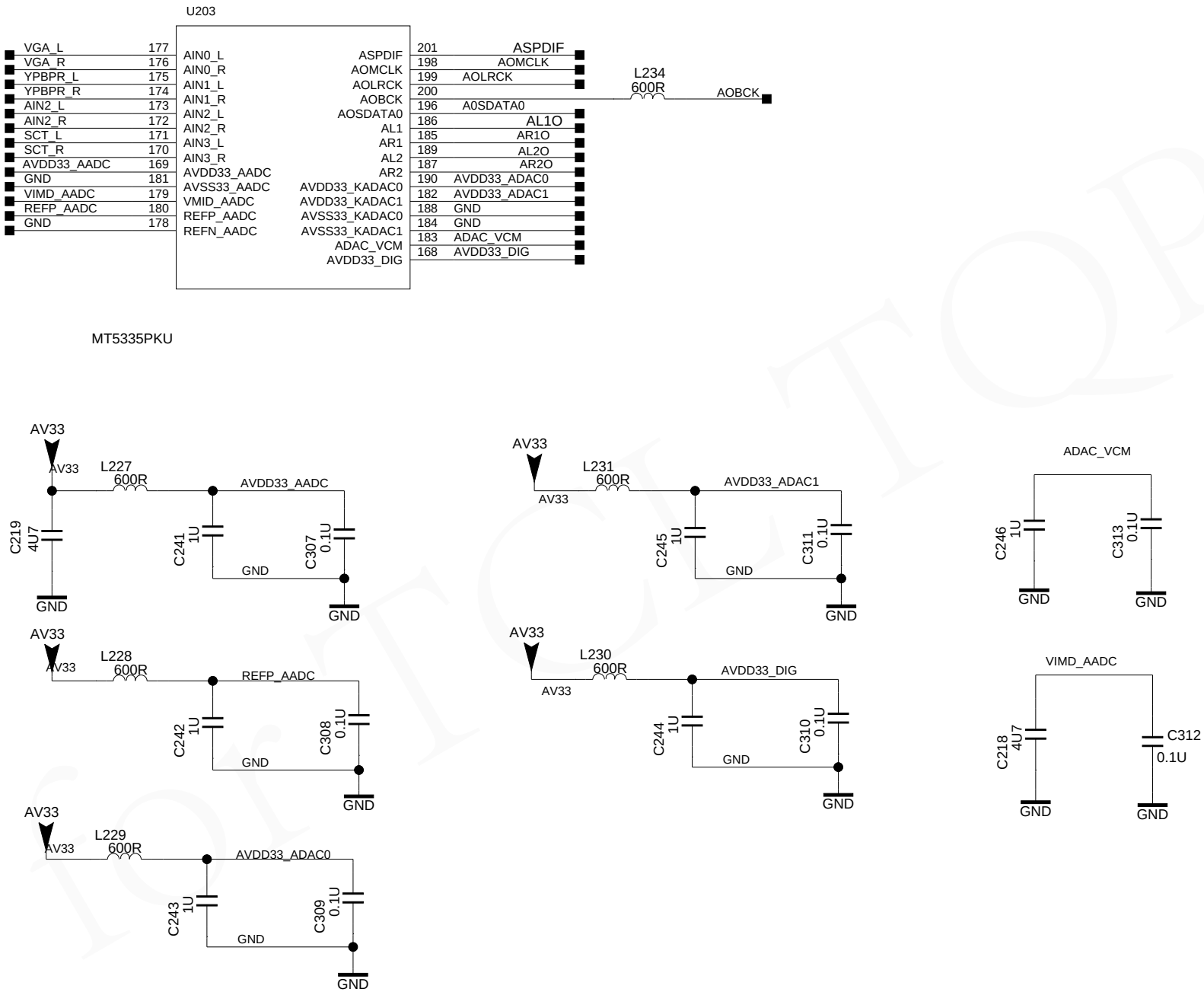

+1V3D
R271
47R
RDQ0 1
RDQ1 2
RDQ2 3
RDQ3 4
MEM_DQ0 1
MEM_DQ1 2
MEM_DQ2 3
MEM_DQ3 4
R287
75R
R272
47R
RDQ4 1
RDQ5 2
RDQ6 3
RDQ7 4
MEM_DQ4 1
MEM_DQ5 2
MEM_DQ6 3
MEM_DQ7 4
R286
75R
R248
47R
R249
RDQS0 1
R250
RDQM0 2
R251
RDQM1 3
RDQS1 4
MEM_DQS0 1
MEM_DQM0 2
MEM_DQM1 3
MEM_DQS1 4
R254
75R
R255
R256
R257
R273
47R
RDQ11 1
RDQ10 2
RDQ9 3
RDQ8 4
MEM_DQ11 1
MEM_DQ10 2
MEM_DQ9 3
MEM_DQ8 4
R285
75R
R274
47R
RDQ15 1
RDQ14 2
RDQ13 3
RDQ12 4
MEM_DQ15 1
MEM_DQ14 2
MEM_DQ13 3
MEM_DQ12 4
R288
75R


+5V
R301
2R7
R302
2R7
R303
2R7
U201
LD1117S
VIN 3
OUT 2
GND/ADJ 1
4
C200
100U
6V3
C303
0.1U
GND
R262
10R
R263
120R
C302
0.1U
C215
4U7
DDRV
GND


DDRV
DDRV_IC
L213
600R
C349
220U
16V
C350
100U
6V3
C280
0.1U
C281
0.1U
C282
0.1U
C283
0.1U
C284
0.1U
C285
0.1U
C287
0.1U
C286
0.1U
C349&C280 CLOSE TO PIN33 OF DDR
GND

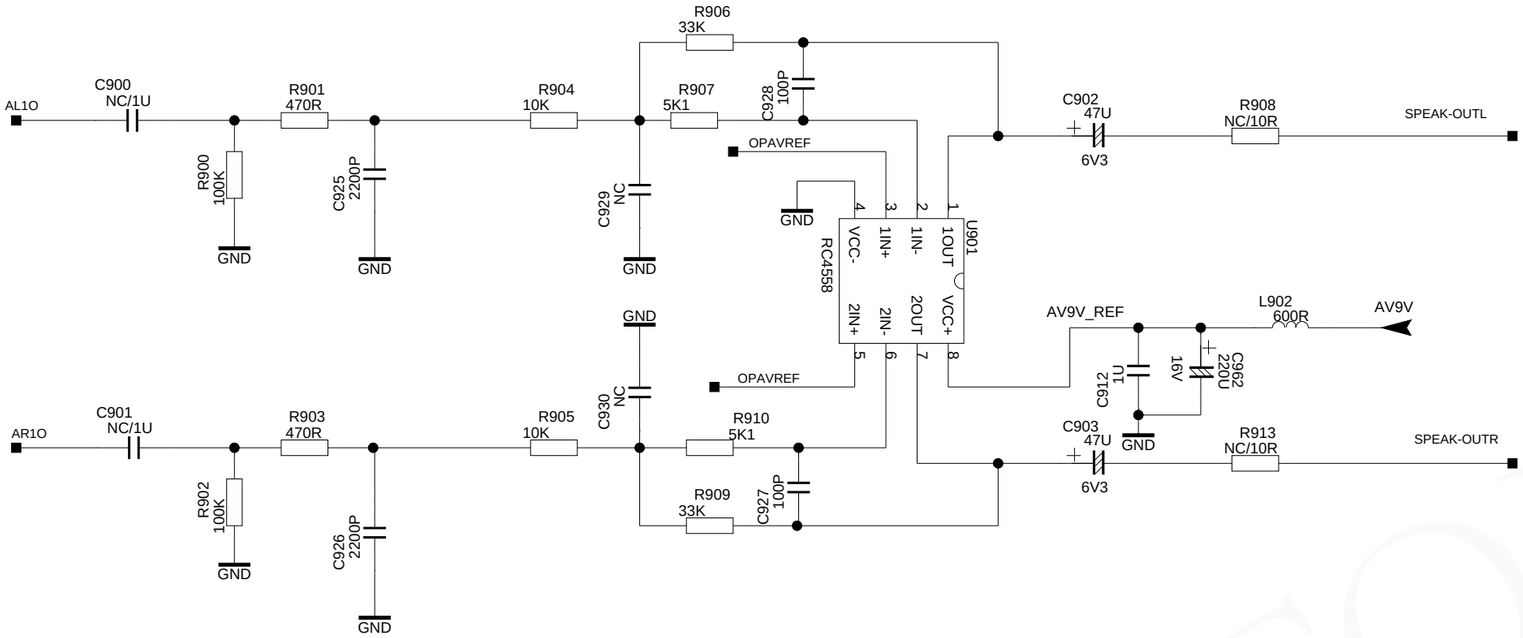

MEM_VREF
C300
0.1U
C301
0.1U
C216
1U
GND
+1V3D
C296
0.1U
C297
0.1U
C299
0.1U
C298
0.1U
GND
+1V3D
C316
1U
C295
0.1U
C294
0.1U
C292
0.1U
C293
0.1U
C288
0.1U
C289
0.1U
C291
0.1U
C290
0.1U
GND

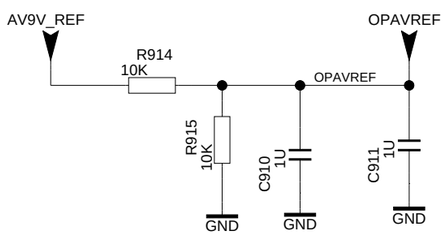

+1V3D
R280
75R
MEM_CS# 1
MEM_RAS# 2
MEM_CAS# 3
MEM_WE# 4
R281
75R
MEM_ADDR10 1
MEM_BA1 2
MEM_BA0 3
4
R282
75R
MEM_ADDR7 1
MEM_ADDR6 2
MEM_ADDR5 3
MEM_ADDR4 4
R252
75R
MEM_CLKEN
R283
75R
MEM_ADDR12 1
MEM_ADDR11 2
MEM_ADDR9 3
MEM_ADDR8 4
R253
75R
MEM_ADDR13
R284
75R
MEM_ADDR3 1
MEM_ADDR2 2
MEM_ADDR1 3
MEM_ADDR0 4

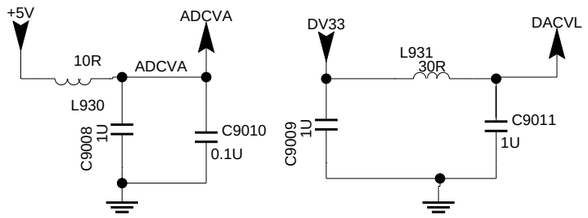

U203
VGA_L 177 AIN0_L
VGA_R 176 AIN0_R
YPBPR_L 175 AIN1_L
YPBPR_R 174 AIN1_R
AIN2_L 173 AIN2_L
AIN2_R 172 AIN2_R
SCT_L 171 AIN3_L
SCT_R 170 AIN3_R
AVDD33_AADC 169 AVDD33_AADC
GND 181 AVSS33_AADC
VIMD_AADC 179 VMID_AADC
REFP_AADC 180 REFP_AADC
GND 178 REFN_AADC
ASPDIF 201 ASPDIF
AOMCLK 198 AOMCLK
AOLRCK 199 AOLRCK
AOBCK 200
AOSDATA0 196 A0SDATA0
AL1 186 AL1O
AR1 185 AR1O
AL2 189 AL2O
AR2 187 AR2O
AVDD33_KADAC0 190 AVDD33_ADAC0
AVDD33_KADAC1 182 AVDD33_ADAC1
AVSS33_KADAC0 188 GND
AVSS33_KADAC1 184 GND
ADAC_VCM 183 ADAC_VCM
AVDD33_DIG 168 AVDD33_DIG
L234
600R
AOBCK
MT5335PKU
AV33
L227
600R
AVDD33_AADC
C219
4U7
C241
1U
C307
0.1U
GND
L228
600R
REFP_AADC
C242
1U
C308
0.1U
L229
600R
AVDD33_ADAC0
C243
1U
C309
0.1U
L231
600R
AVDD33_ADAC1
C245
1U
C311
0.1U
L230
600R
AVDD33_DIG
C244
1U
C310
0.1U
ADAC_VCM
C246
1U
C313
0.1U
VIMD_AADC
C218
4U7
C312
0.1U

A

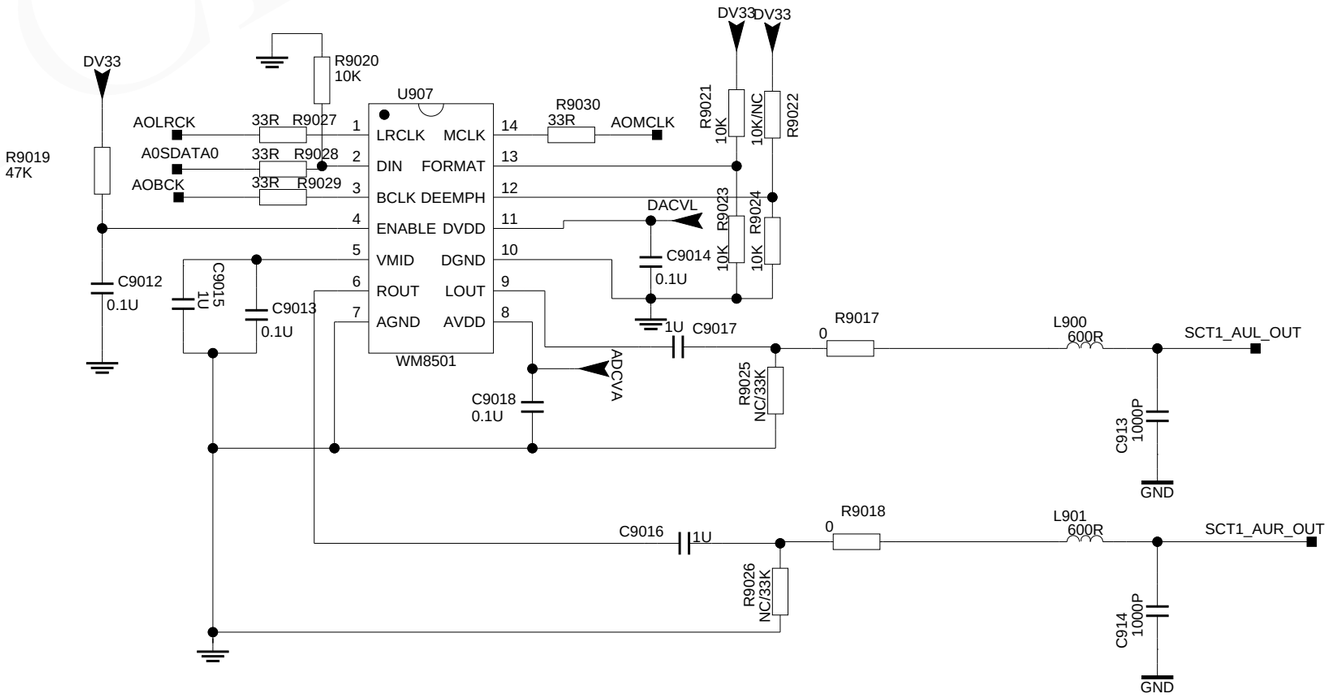
A

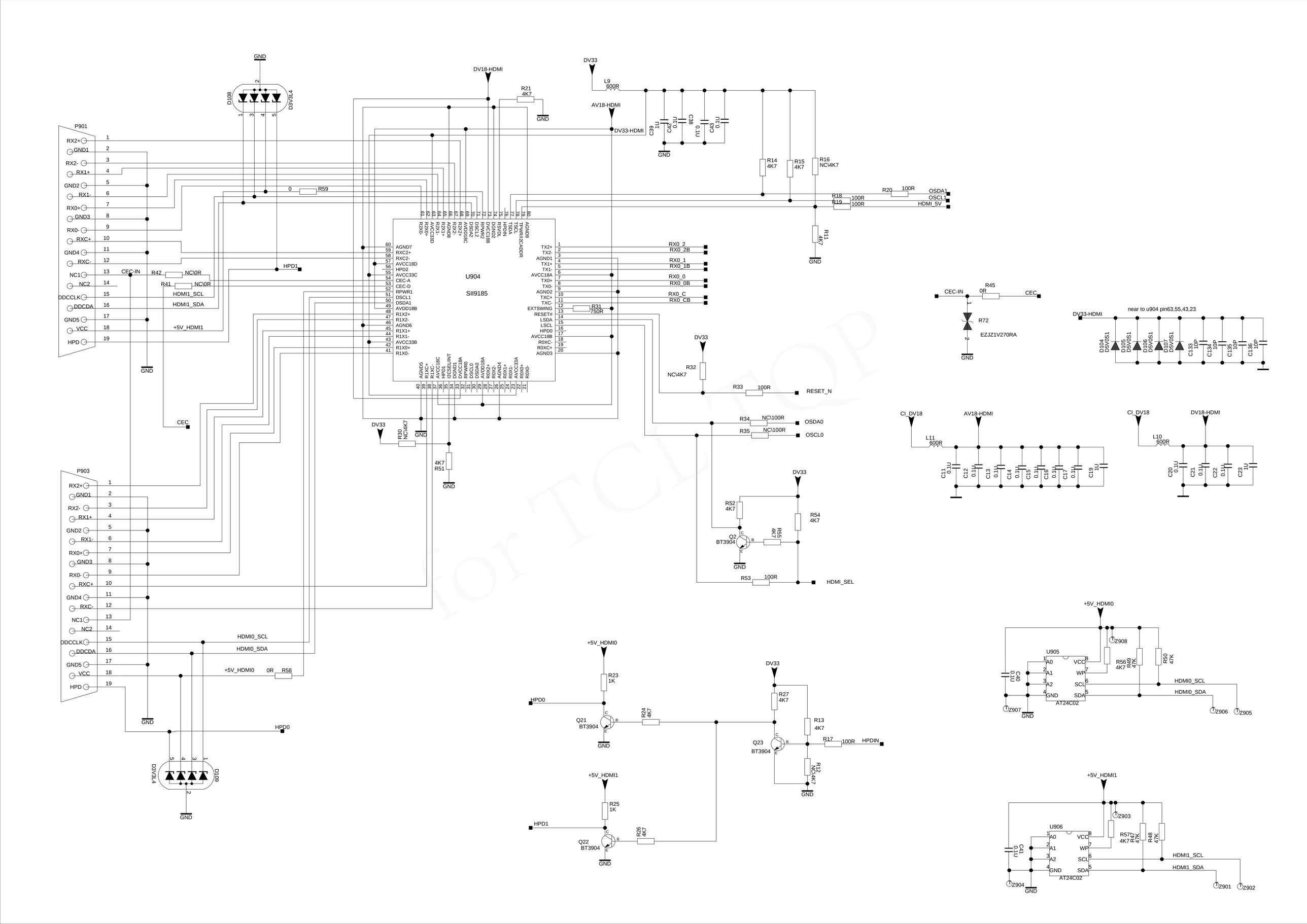

AL1O
C900
NC/1U
R901
470R
R900
100K
GND
C925
2200P
GND
R904
10K
R906
33K
R907
5K1
C928
100P
C929
NC
GND
OPAVREF
GND
RC4558
U901
VCC-
1IN+
1IN-
1OUT
2IN+
2IN-
2OUT
VCC+
C902
47U
6V3
R908
NC/10R
SPEAK-OUTL
AV9V_REF
L902
600R
AV9V
C912
1U
16V
C962
220U
GND
AR1O
C901
NC/1U
R903
470R
R902
100K
GND
C926
2200P
GND
R905
10K
R910
5K1
R909
33K
C927
100P
C930
NC
GND
OPAVREF
C903
47U
6V3
R913
NC/10R
SPEAK-OUTR


AV9V_REF
R914
10K
OPAVREF
R915
10K
GND
C910
1U
GND
C911
1U
GND

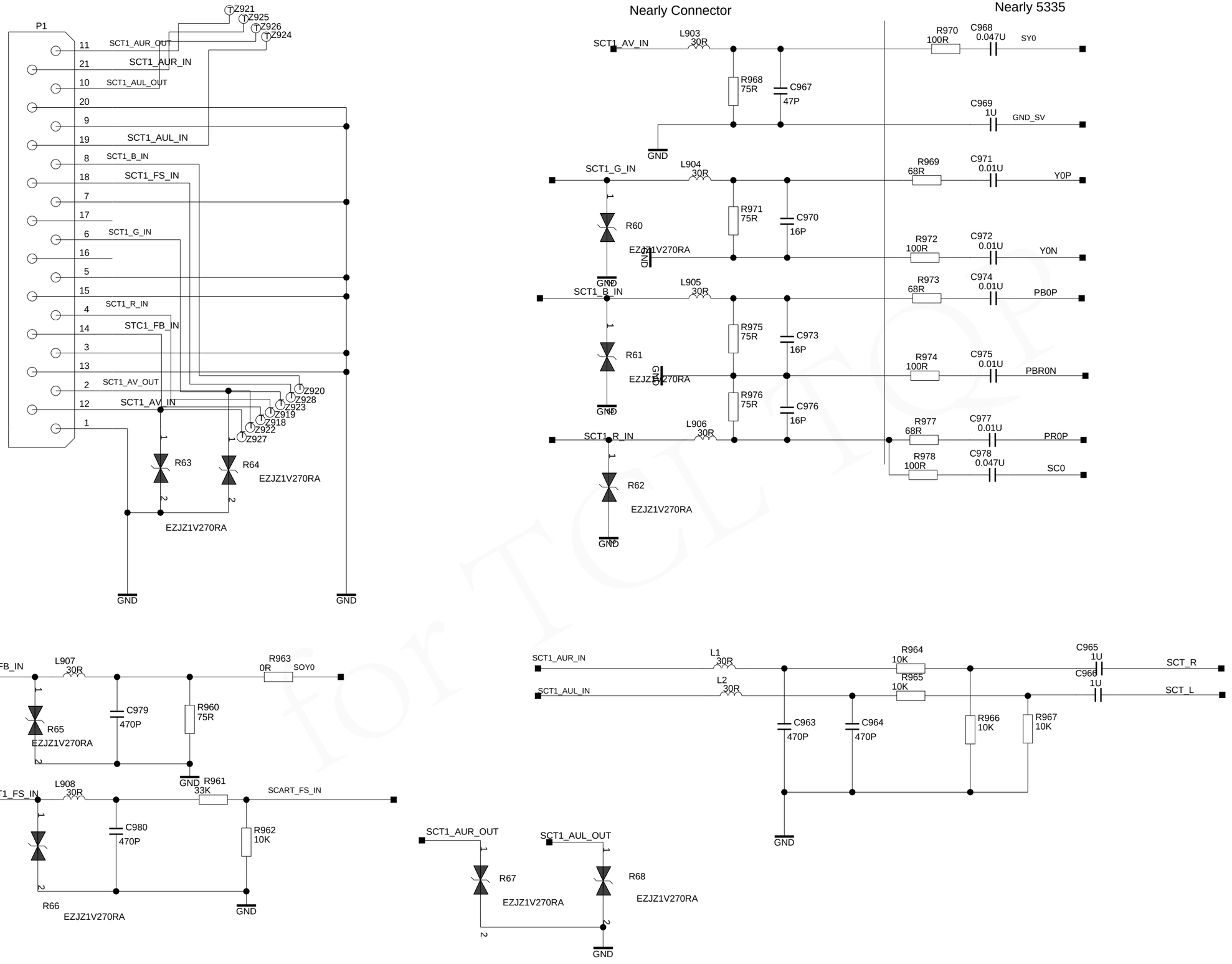

+5V
10R
ADCVA
L930
C9008
1U
C9010
0.1U
DV33
L931
30R
DACVL
C9009
1U
C9011
1U

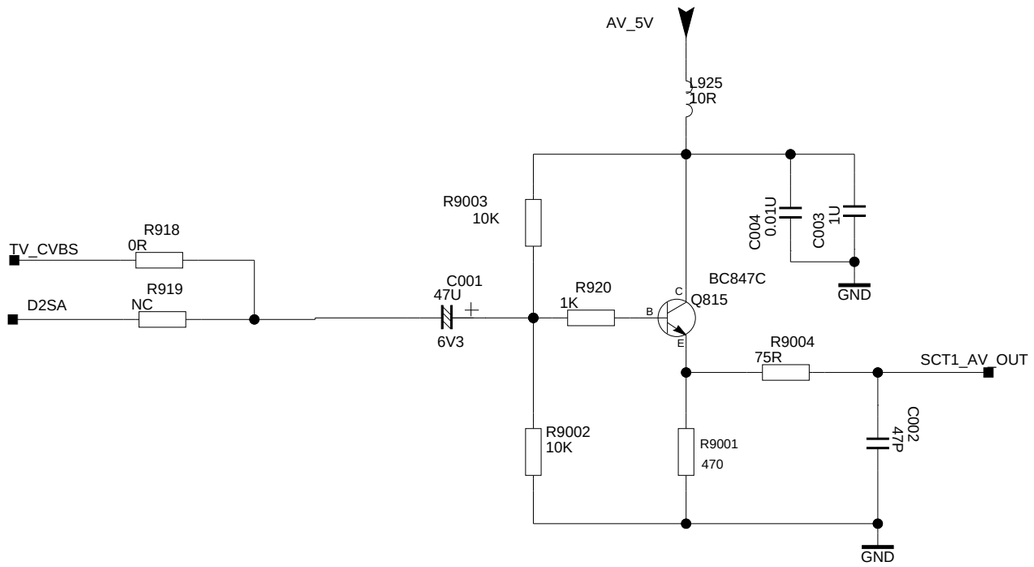
DAC

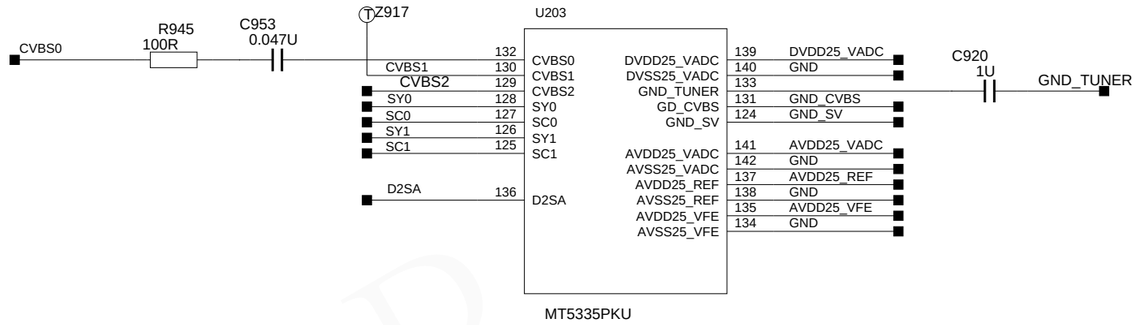

DV33
DV33
DV33
R9020
10K
R9019
47K
U907
AOLRCK
33R R9027
A0SDATA0
33R R9028
AOBCK
33R R9029
LRCLK
DIN
BCLK
ENABLE
VMID
ROUT
AGND
MCLK
FORMAT
DEEMPH
DVDD
DGND
LOUT
AVDD
WM8501
R9030
33R
AOMCLK
R9021
10K
10K/NC
R9022
R9023
10K
R9024
10K
DACVL
C9014
0.1U
C9012
0.1U
C9015
1U
C9013
0.1U
1U
C9017
R9017
0
L900
600R
SCT1_AUL_OUT
ADCVA
C9018
0.1U
R9025
NC/33K
C913
1000P
GND
C9016
1U
R9018
0
L901
600R
SCT1_AUR_OUT
R9026
NC/33K
C914
1000P
GND



P901
P903
U904
SII9185
D108
D3V3L4
D109
D3V3L4
DV18-HDMI
DV33
AV18-HDMI
DV33-HDMI
L9
600R
R21
4K7
R14
4K7
R15
4K7
R16
NC\4K7
R20
100R
OSDA1
OSCL1
HDMI_5V
R18
100R
R19
100R
R11
4K7
R59
0
HPD1
CEC-IN
R42
NC\0R
R41
NC\0R
HDMI1_SCL
HDMI1_SDA
+5V_HDMI1
RX0_2
RX0_2B
RX0_1
RX0_1B
RX0_0
RX0_0B
RX0_C
RX0_CB
R31
750R
R32
NC\4K7
R33
100R
RESET_N
R34
NC\100R
OSDA0
R35
NC\100R
OSCL0
R30
NC\4K7
4K7
R51
R52
4K7
R54
4K7
Q2
BT3904
R55
4K7
R53
100R
HDMI_SEL
CEC
R45
0R
R72
EZJZ1V270RA
near to u904 pin63,55,43,23
D104
D5V0S1
D105
D5V0S1
D106
D5V0S1
D107
D5V0S1
C133
10P
C134
10P
C135
10P
C136
10P
CI_DV18
AV18-HDMI
L11
600R
C11
0.1U
C12
0.1U
C13
0.1U
C14
0.1U
C15
0.1U
C16
0.1U
C17
0.1U
C19
1U
CI_DV18
DV18-HDMI
L10
600R
C20
0.1U
C21
0.1U
C22
0.1U
C23
1U
HDMI0_SCL
HDMI0_SDA
+5V_HDMI0
0R
R58
HPD0
+5V_HDMI0
R23
1K
Q21
BT3904
R24
4K7
DV33
R27
4K7
R13
4K7
Q23
BT3904
R17
100R
HPDIN
R12
NC\4K7
+5V_HDMI1
R25
1K
Q22
BT3904
R26
4K7
+5V_HDMI0
U905
AT24C02
Z908
R56
4K7
R49
47K
R50
47K
C40
0.1U
HDMI0_SCL
HDMI0_SDA
Z907
Z906
Z905
+5V_HDMI1
U906
AT24C02
Z903
R57
4K7
R47
47K
R48
47K
C41
0.1U
HDMI1_SCL
HDMI1_SDA
Z904
Z901
Z902

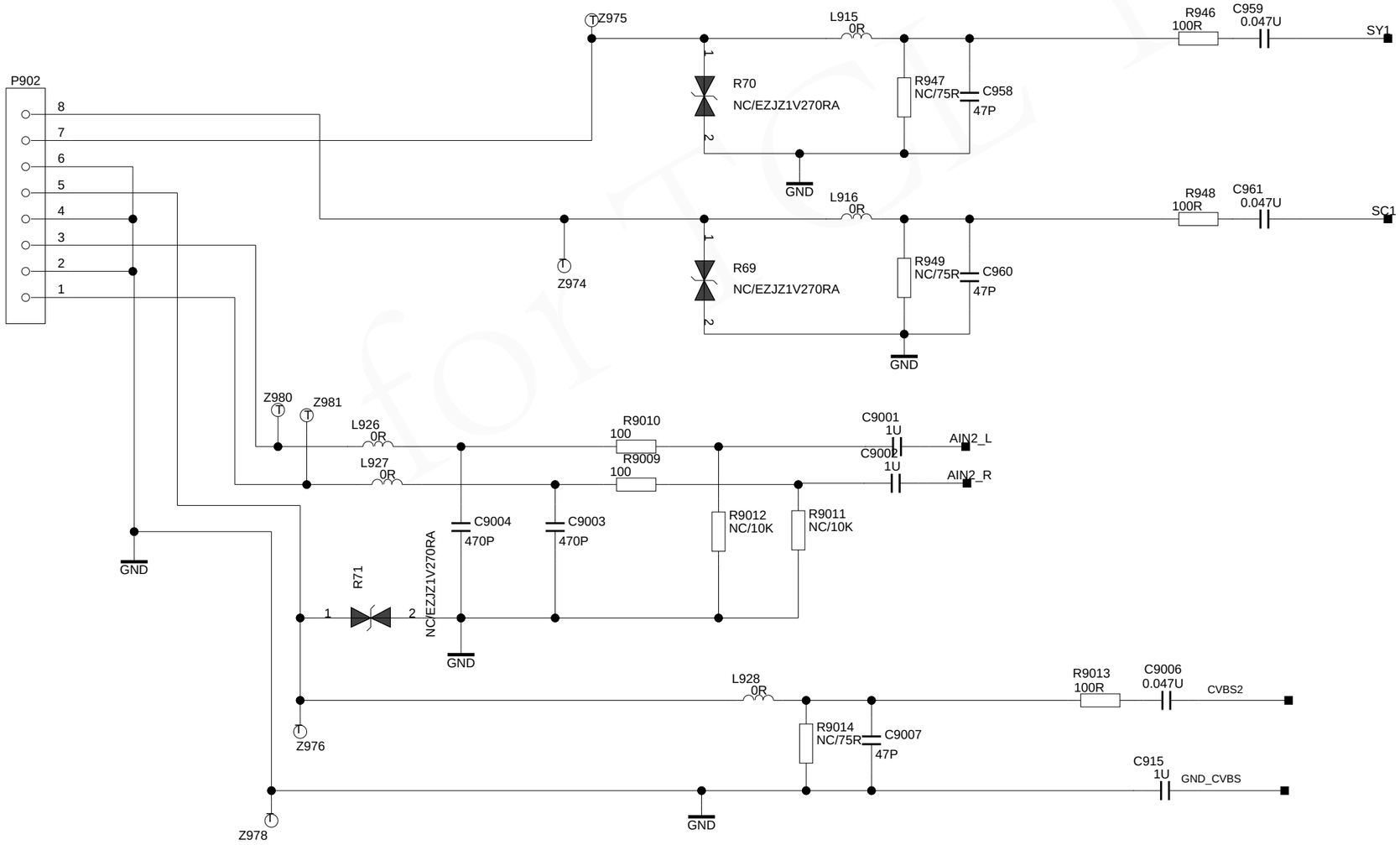

P1
11 SCT1_AUR_OUT
21 SCT1_AUR_IN
10 SCT1_AUL_OUT
20
9
19 SCT1_AUL_IN
8 SCT1_B_IN
18 SCT1_FS_IN
7
17
6 SCT1_G_IN
16
5
15
4 SCT1_R_IN
14 STC1_FB_IN
3
13
2 SCT1_AV_OUT
12 SCT1_AV_IN
1
TZ921
TZ925
TZ926
TZ924
TZ920
TZ928
TZ923
TZ919
TZ918
TZ922
TZ927
R63
R64
EZJZ1V270RA
EZJZ1V270RA
GND
GND
Nearly Connector
Nearly 5335
SCT1_AV_IN
L903 30R
R968 75R
C967 47P
GND
R970 100R
C968 0.047U
SY0
C969 1U
GND_SV
SCT1_G_IN
L904 30R
R971 75R
C970 16P
R60
EZJZ1V270RA
GND
R969 68R
C971 0.01U
Y0P
R972 100R
C972 0.01U
Y0N
SCT1_B_IN
L905 30R
R975 75R
C973 16P
R61
EZJZ1V270RA
GND
R973 68R
C974 0.01U
PB0P
R974 100R
C975 0.01U
PBR0N
SCT1_R_IN
L906 30R
R976 75R
C976 16P
R62
EZJZ1V270RA
GND
R977 68R
C977 0.01U
PR0P
R978 100R
C978 0.047U
SC0
STC1_FB_IN
L907 30R
R963 0R
SOY0
R65
EZJZ1V270RA
C979 470P
R960 75R
GND
SCT1_FS_IN
L908 30R
R961 33K
SCART_FS_IN
C980 470P
R962 10K
R66
EZJZ1V270RA
GND
SCT1_AUR_IN
L1 30R
SCT1_AUL_IN
L2 30R
R964 10K
R965 10K
C965 1U
C966 1U
SCT_R
SCT_L
C963 470P
C964 470P
R966 10K
R967 10K
GND
SCT1_AUR_OUT
SCT1_AUL_OUT
R67
R68
EZJZ1V270RA
EZJZ1V270RA
GND

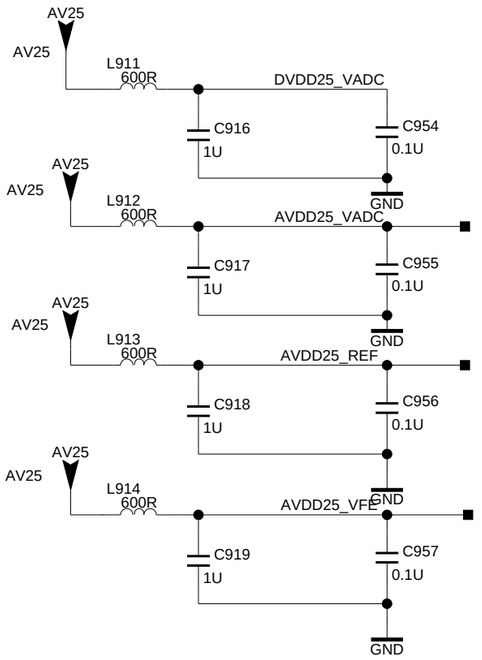




Nearly Connector

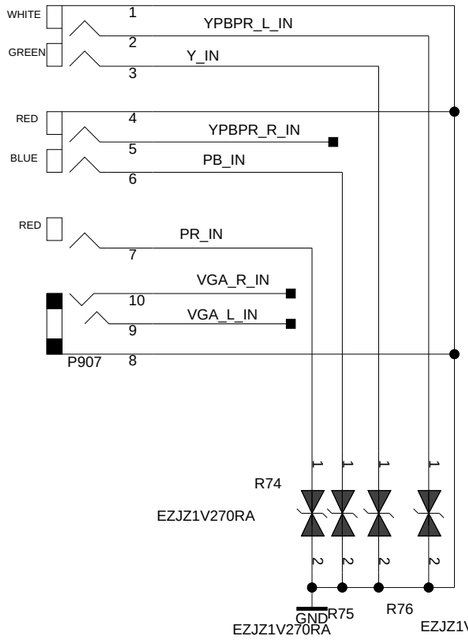
Nearly 5335

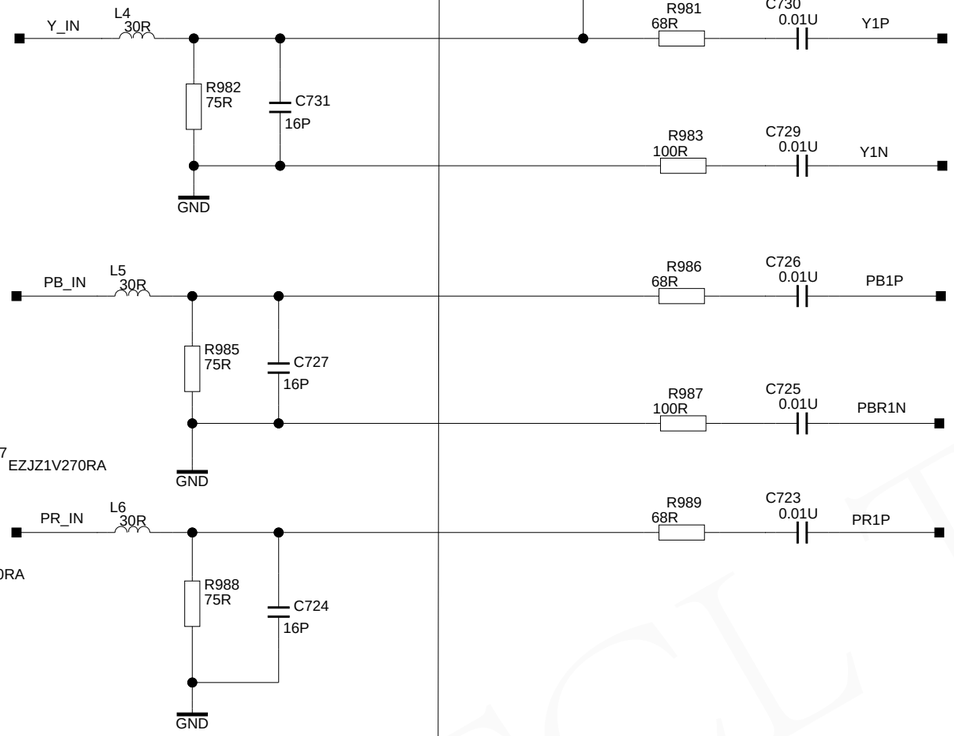


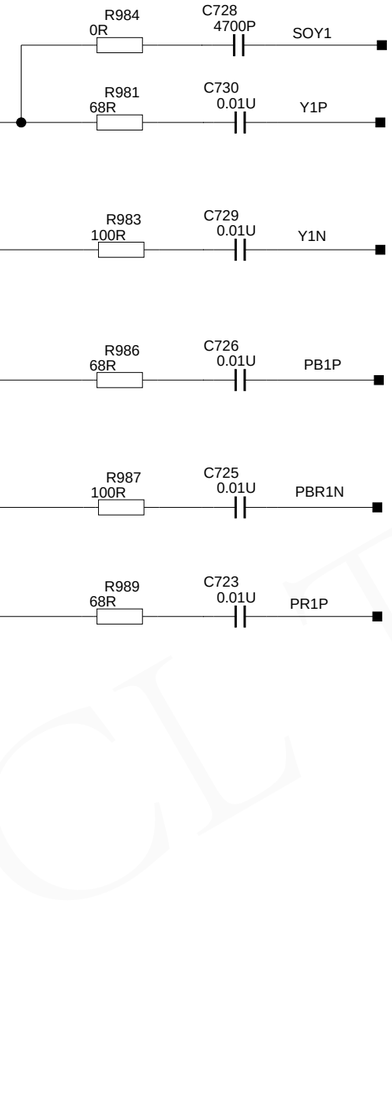


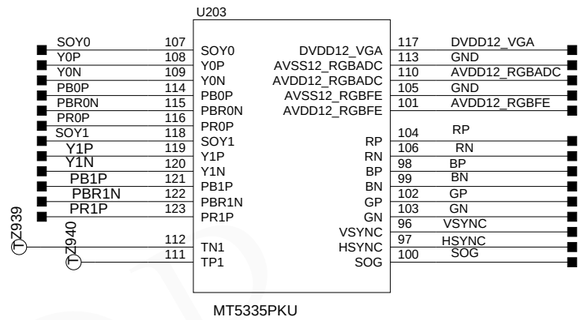
Nearly 5335

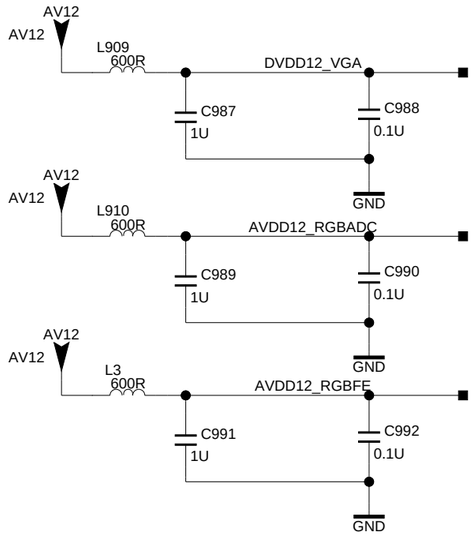
Nearly Connector

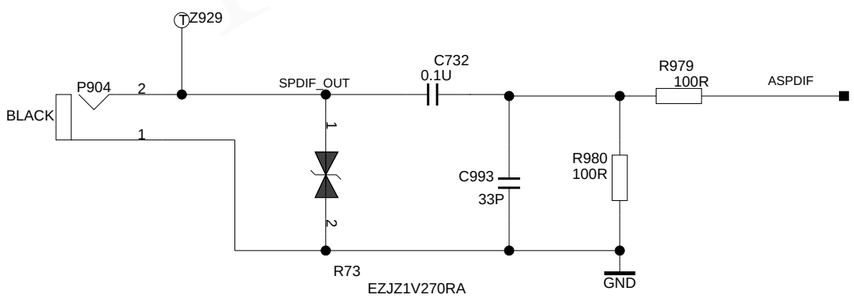


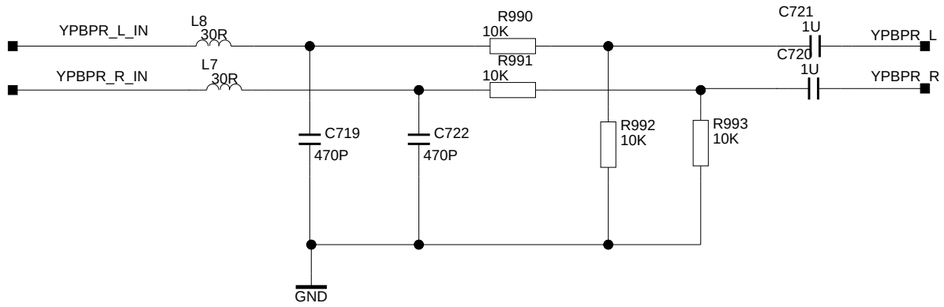












for TCL

Nearly 5335

Nearly Connector

P908

VGASCL_IN

W/P_CTR

VSYNC_IN

BLUE

HSYNC_IN

GREEN

VGASDA_IN

RED

R716 0R W/P

VGA_PLUGPWR

+5V

D913 BAV70

C005 ESD_0402

GND

EZJZ1V270RA

R84

R86

R85

Z945 Z941 Z942 Z943 Z944 Z946 Z948 Z947 Z955

Z949 Z950

VGA_R_IN

VGA_L_IN

L924 30R

L923 30R

R704 10K

R705 10K

C702 1U VGA_R

C701 1U VGA_L

C999 470P

C703 470P

R706 10K

R707 10K

HSYNC_IN

L921 30R

HSYNC

R82

R718 4K7

C705 10P

VSYNC_IN

L922 30R

VSYNC

R83

R717 4K7

C704 10P

GREEN L918 30R

BLUE L919 30R

RED L920 30R

R996 75R

R999 75R

R702 75R

C715 16P

C711 16P

C708 16P

R998 0R

R719 33R

R997 100R

R720 33R

R701 100R

R721 33R

R703 100R

C712 4700P SOG

C714 0.01U GP

C713 0.01U GN

C710 0.01U BP

C709 0.01U BN

C707 0.01U RP

C706 0.01U RN

5VSB

R708 10K

VGASCL_IN

R709 100R

VGASCL

R80

C998 16P

R710 10K

VGASDA_IN

R711 100R

VGASDA

R81

C997 16P

VGA_PLUGPWR

Z973

C996 0.1U

U903 AT24C02

A0 A1 A2 GND VCC WP SCL SDA

R715 10K

Z972 Z971 Z970

W/P VGASCL VGASDA

VGASCL_IN

5VSB

VGASDA_IN

R712 100R

R714 10K

R713 100R

U0TX

U0RX

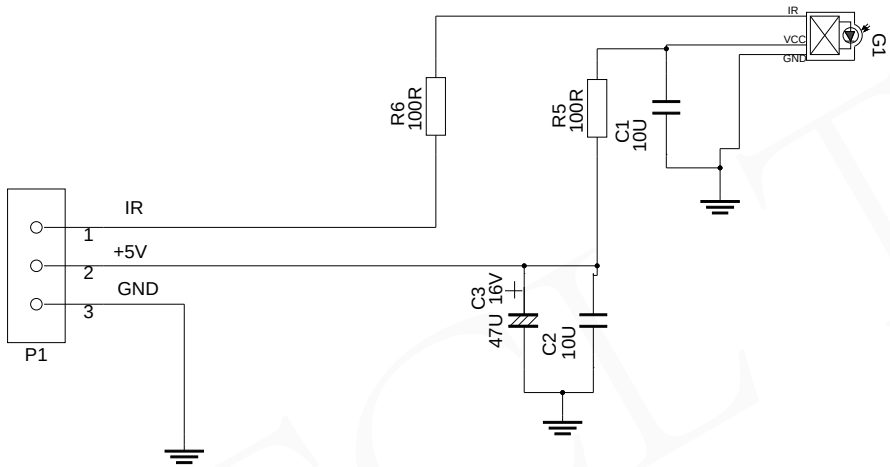
Q903 C143ZT

Q904 C143ZT

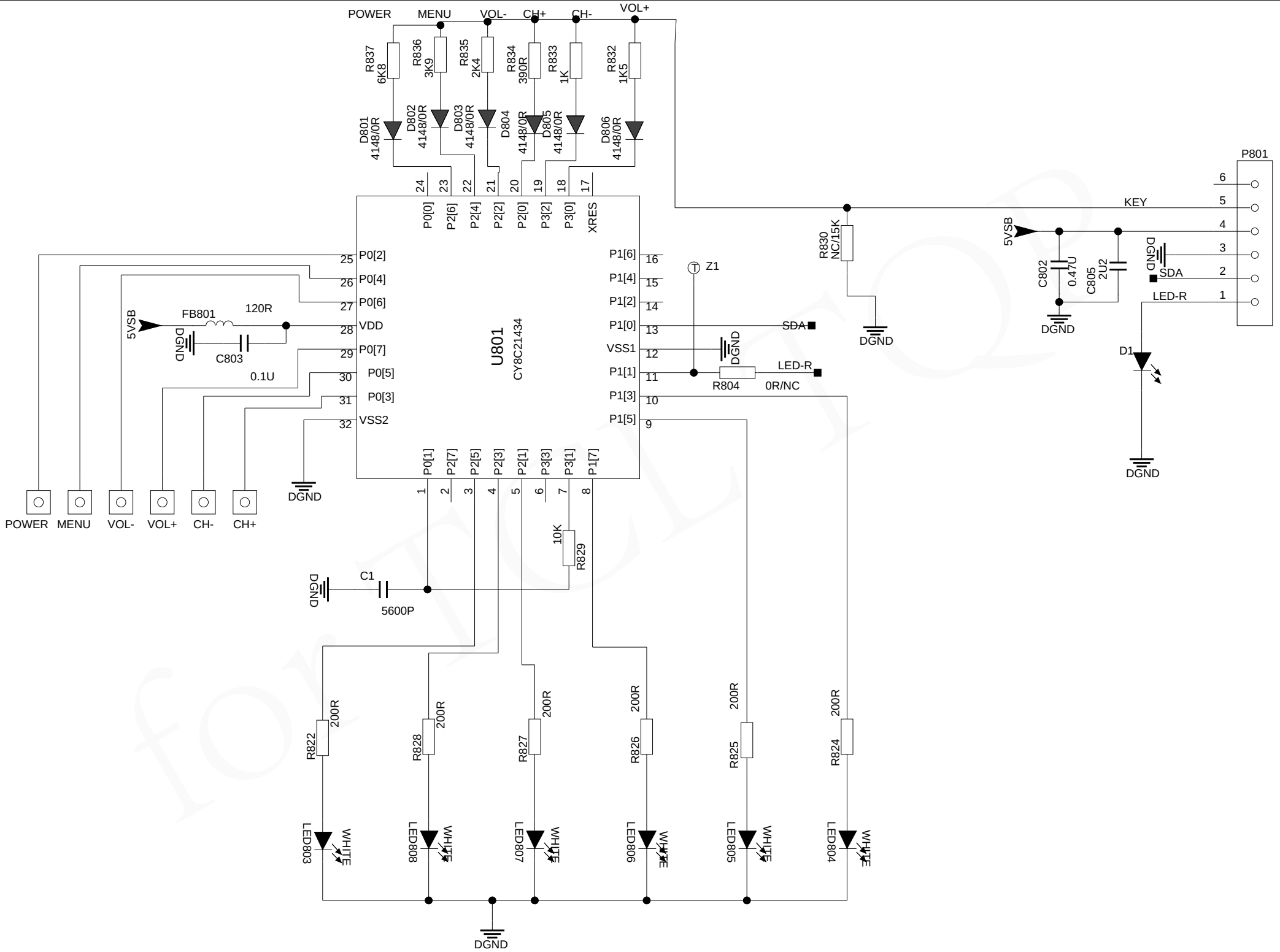
SW_UPDATE_CTL

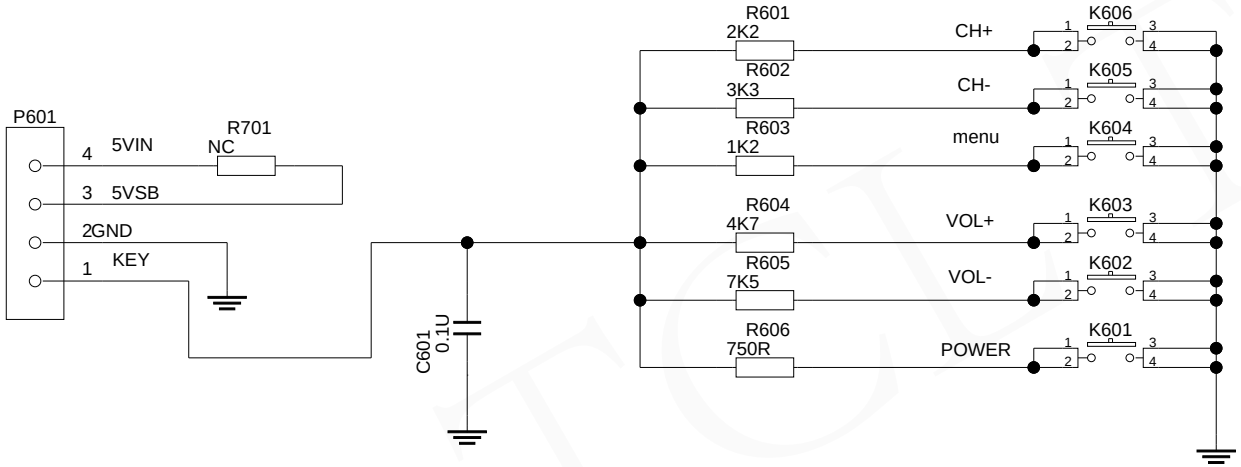
Q905 C143ZT

R725 10K


IR
VCC
GND
G1
R6
100R
R5
100R
C1
10U
IR
1
+5V
2
GND
3
P1
C3
47U 16V
C2
10U

forTOP


POWER
MENU
VOL-
CH+
CH-
VOL+
R837 6K8
R836 3K9
R835 2K4
R834 390R
R833 1K
R832 1K5
D801 4148/0R
D802 4148/0R
D803 4148/0R
D804 4148/0R
D805 4148/0R
D806 4148/0R
U801
CY8C21434
P0[0]
P0[1]
P0[2]
P0[3]
P0[4]
P0[5]
P0[6]
P0[7]
P1[0]
P1[1]
P1[2]
P1[3]
P1[4]
P1[5]
P1[6]
P1[7]
P2[0]
P2[1]
P2[2]
P2[3]
P2[4]
P2[5]
P2[6]
P2[7]
P3[0]
P3[1]
P3[2]
P3[3]
VDD
VSS1
VSS2
XRES
5VSB
FB801 120R
C803 0.1U
DGND
C1 5600P
R829 10K
Z1
R804 0R/NC
LED-R
SDA
R830 NC/15K
KEY
C802 0.47U
C805 2U2
P801
D1
R822 200R
R828 200R
R827 200R
R826 200R
R825 200R
R824 200R
LED803 WHITE
LED808 WHITE
LED807 WHITE
LED806 WHITE
LED805 WHITE
LED804 WHITE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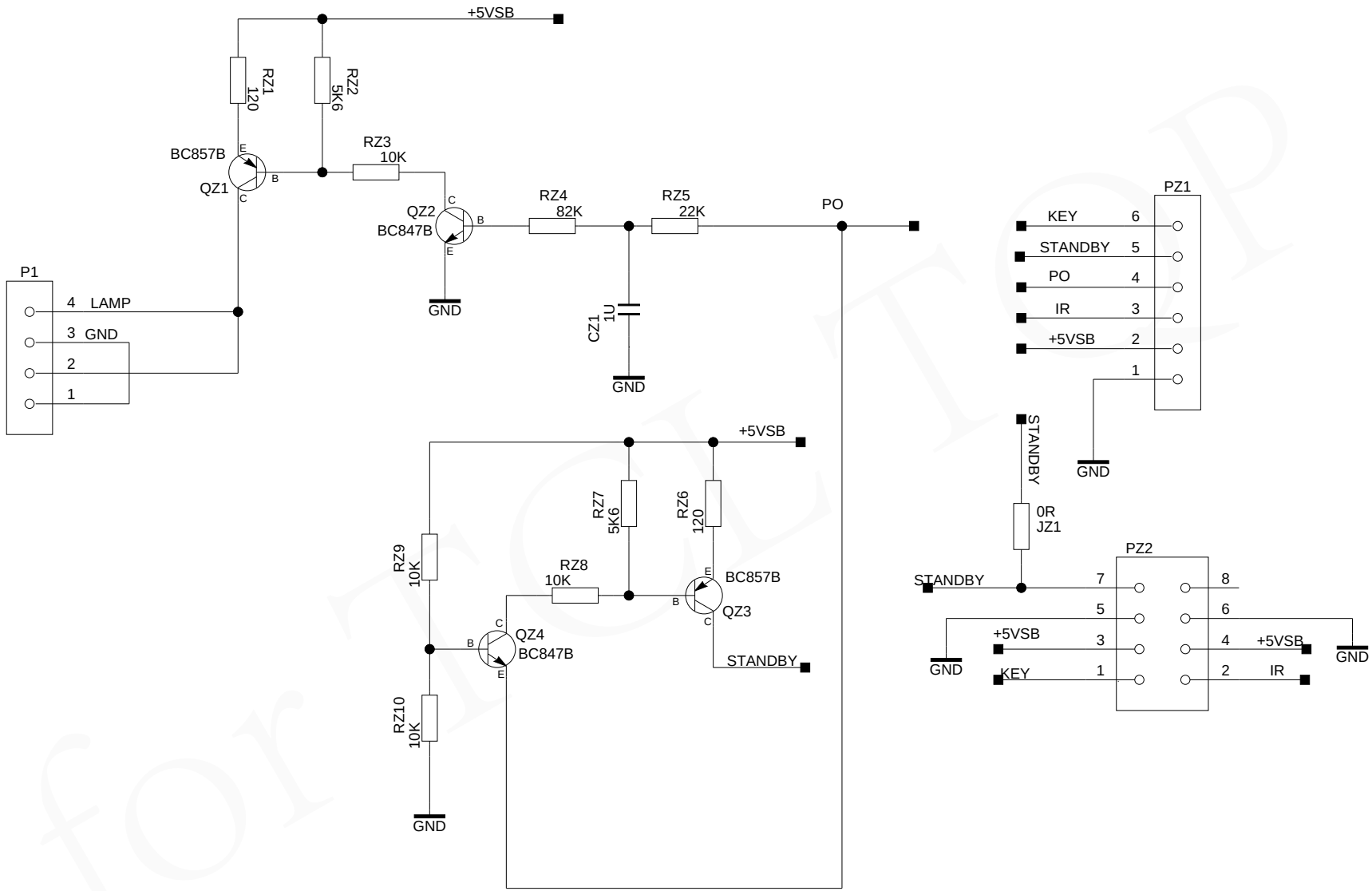
4
5VIN
R701
NC
3
5VSB
2GND
1
KEY
C601
0.1U
R601
2K2
R602
3K3
R603
1K2
R604
4K7
R605
7K5
R606
750R
CH+
CH-
menu
VOL+
VOL-
POWER
K606
K605
K604
K603
K602
K601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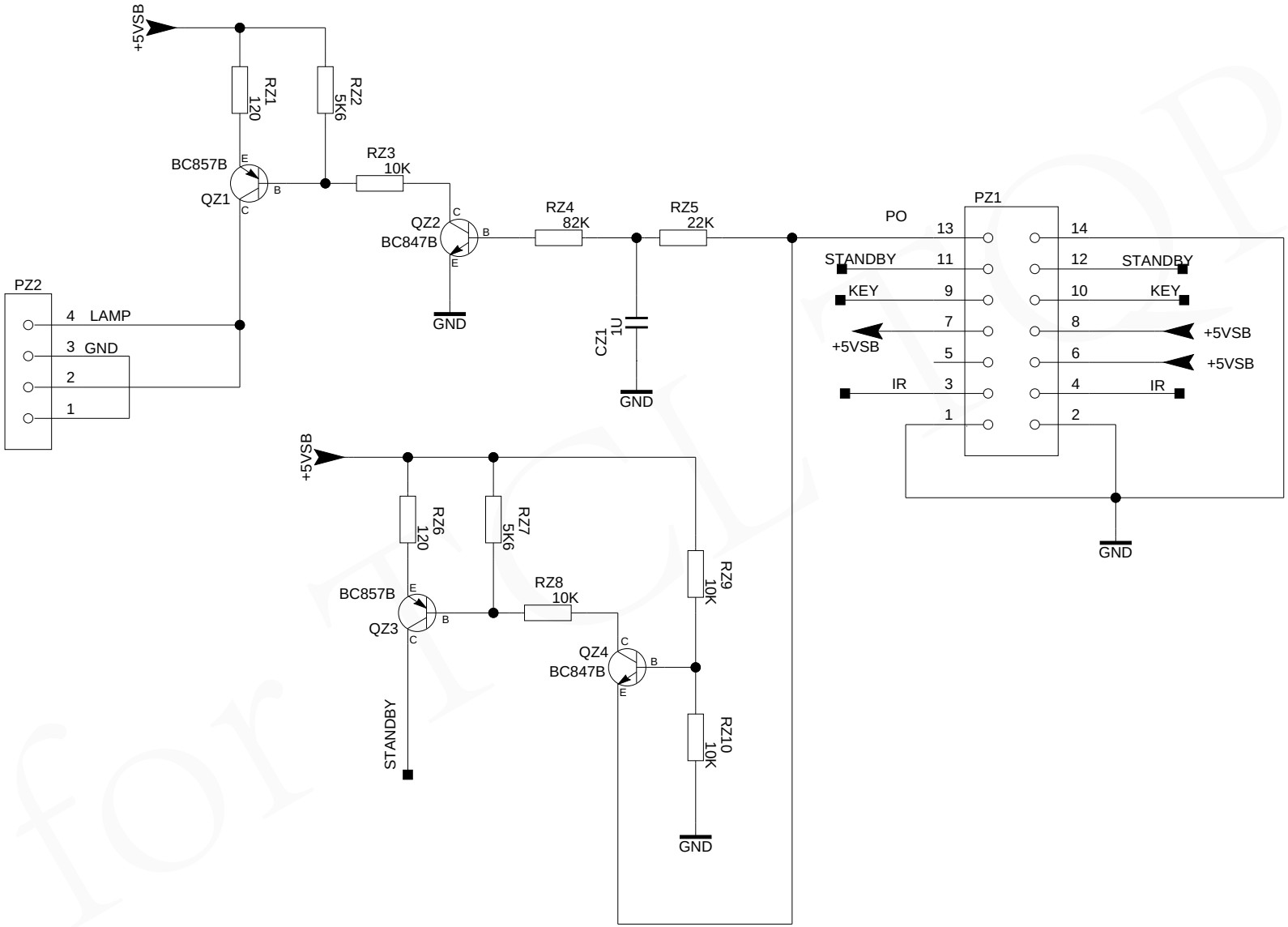
RZ1
120
RZ2
5K6
BC857B
QZ1
RZ3
10K
QZ2
BC847B
RZ4
82K
RZ5
22K
PO
P1
4 LAMP
3 GND
2
1
GND
CZ1
1U
GND
+5VSB
RZ7
5K6
RZ6
120
RZ9
10K
RZ8
10K
BC857B
QZ3
QZ4
BC847B
STANDBY
RZ10
10K
GND
PZ1
KEY 6
STANDBY 5
PO 4
IR 3
+5VSB 2
1
GND
STANDBY
0R
JZ1
PZ2
STANDBY 7
8
5
6
+5VSB 3
4 +5VSB
GND
GND
KEY 1
2 IR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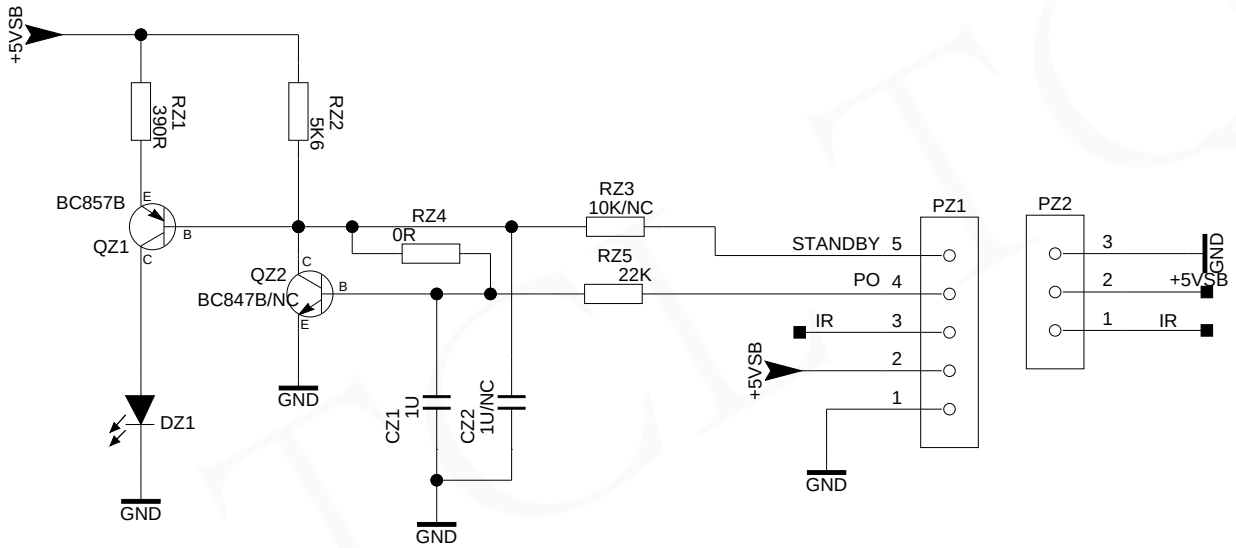
RZ1
120
RZ2
5K6
BC857B
QZ1
RZ3
10K
QZ2
BC847B
RZ4
82K
RZ5
22K
PO
PZ1
PZ2
4 LAMP
3 GND
2
1
GND
CZ1
1U
STANDBY
KEY
+5VSB
IR
RZ6
120
RZ7
5K6
BC857B
QZ3
RZ8
10K
QZ4
BC847B
RZ9
10K
RZ10
10K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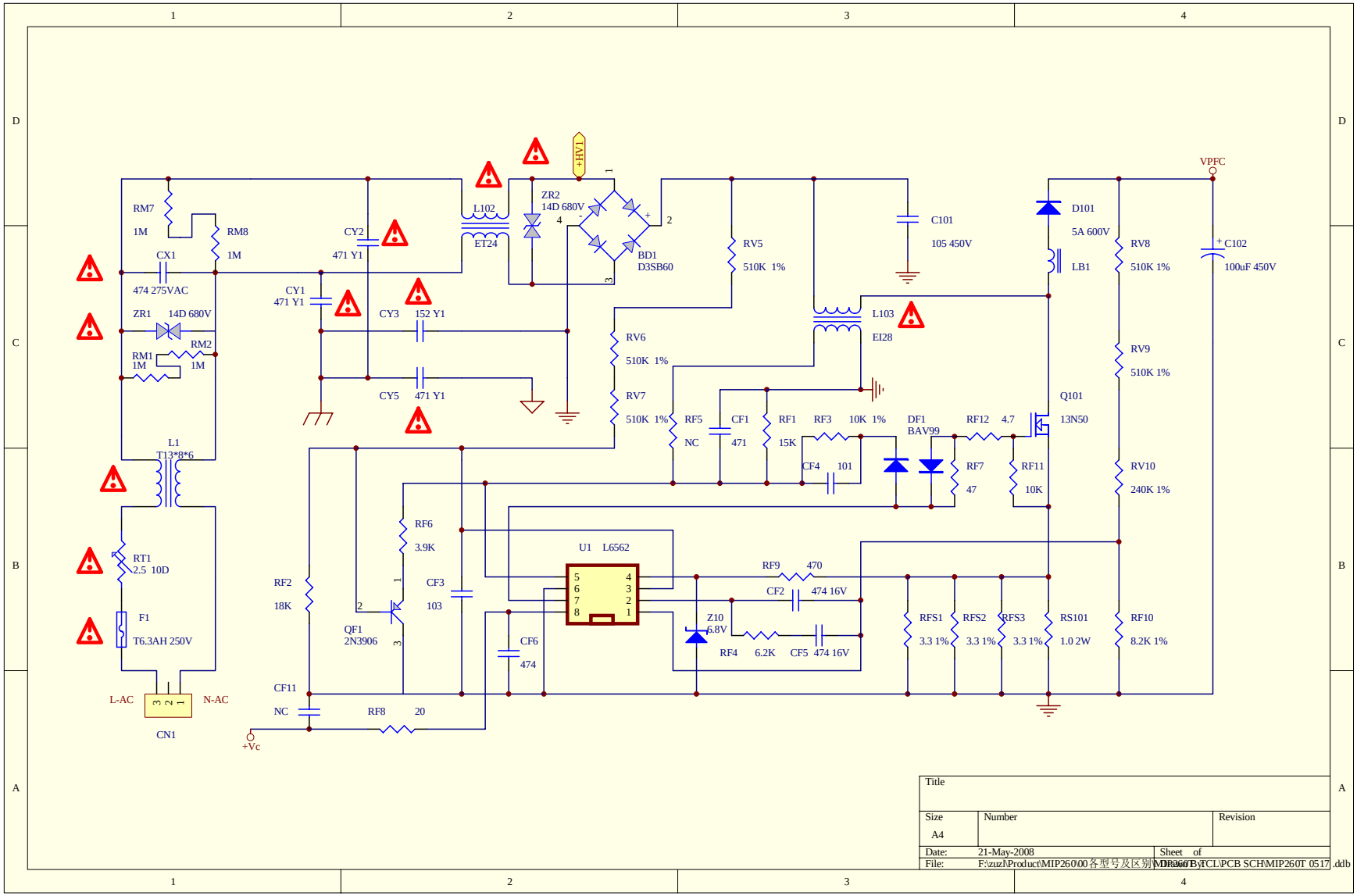
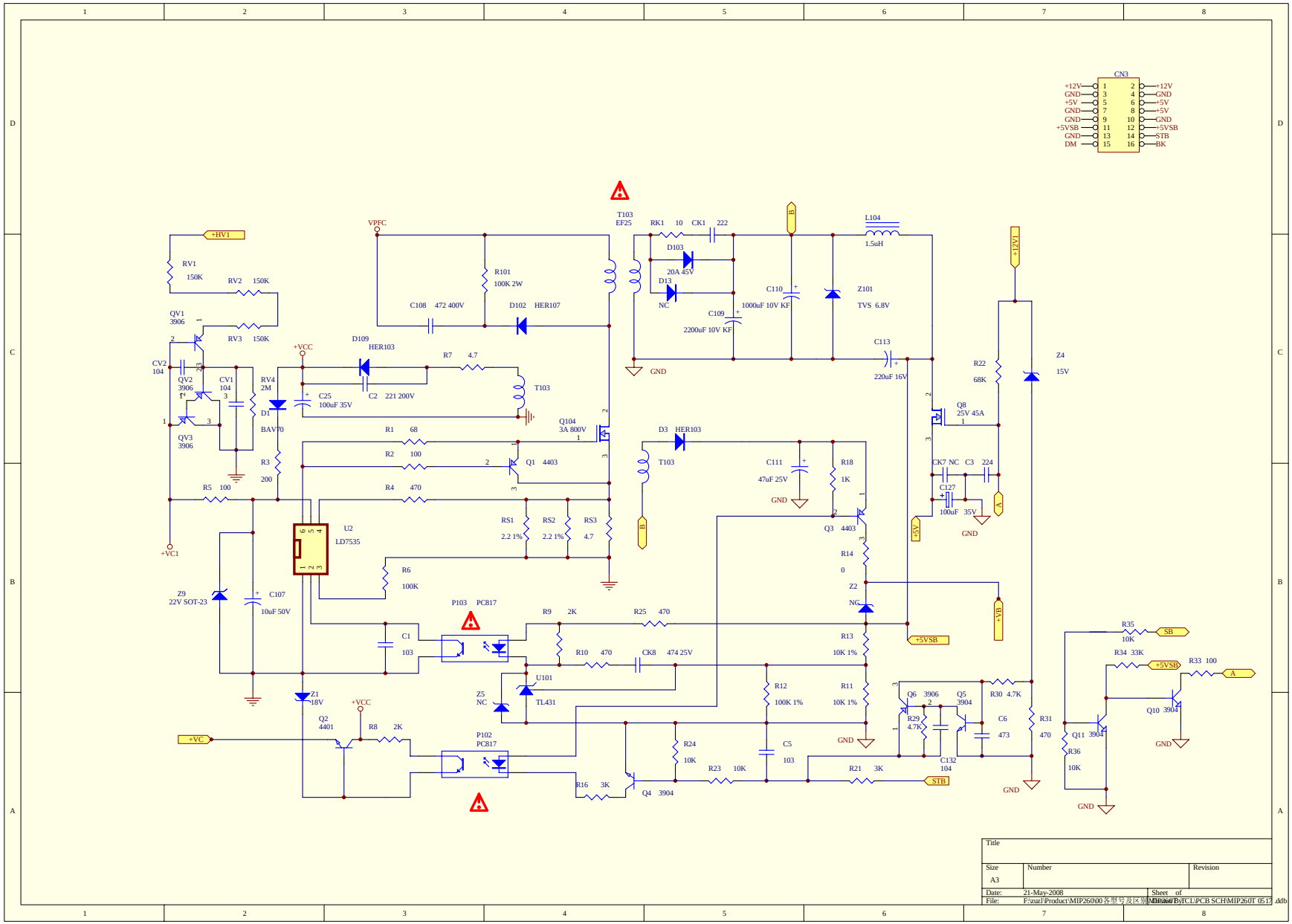
RZ1
390R
RZ2
5K6
BC857B
QZ1
E
B
C
QZ2
BC847B/NC
C
B
E
RZ4
0R
RZ3
10K/NC
RZ5
22K
GND
DZ1
GND
CZ1
1U
CZ2
1U/NC
GND
PZ1
STANDBY 5
PO 4
IR 3
2
1
+5VSB
GND
PZ2
3
2
1
GND
+5VSB
IR


RM7
1M
RM8
1M
CX1
474 275VAC
ZR1
14D 680V
RM1
1M
RM2
1M
L1
T13*8*6
RT1
2.5 10D
F1
T6.3AH 250V
L-AC
N-AC
CN1
CY1
471 Y1
CY2
471 Y1
CY3
152 Y1
CY5
471 Y1
L102
ET24
ZR2
14D 680V
+HV1
BD1
D3SB60
RV5
510K 1%
RV6
510K 1%
RV7
510K 1%
C101
105 450V
L103
EI28
D101
5A 600V
LB1
RV8
510K 1%
RV9
510K 1%
RV10
240K 1%
VPFC
C102
100uF 450V
Q101
13N50
RF5
NC
CF1
471
RF1
15K
RF3
10K 1%
CF4
101
DF1
BAV99
RF12
4.7
RF7
47
RF11
10K
U1 L6562
RF6
3.9K
RF2
18K
CF3
103
QF1
2N3906
CF6
474
RF9
470
CF2
474 16V
Z10
6.8V
RF4
6.2K
CF5
474 16V
RFS1
3.3 1%
RFS2
3.3 1%
RFS3
3.3 1%
RS101
1.0 2W
RF10
8.2K 1%
CF11
NC
RF8
20
+Vc
Title
Size
A4
Number
Revision
Date:
21-May-2008
Sheet of
File:
F:\zuzl\Product\MIP260\00各型号及区别\MIP260T\PCL\PCB SCH\MIP260T 0517 .ddb


CN3
+12V
GND
+5V
GND
GND
+5VSB
GND
DM
+12V
GND
+5V
+5V
GND
+5VSB
STB
BK
+HV1
RV1 150K
RV2 150K
RV3 150K
QV1 3906
QV2 3906
QV3 3906
CV2 104
CV1 104
RV4 2M
D1 BAV70
R3 200
R5 100
+VC1
Z9 22V SOT-23
C107 10uF 50V
VPFC
R101 100K 2W
C108 472 400V
D102 HER107
D109 HER103
+VCC
R7 4.7
C25 100uF 35V
C2 221 200V
T103
Q104 3A 800V
R1 68
R2 100
R4 470
Q1 4403
U2 LD7535
RS1 2.2 1%
RS2 2.2 1%
RS3 4.7
R6 100K
C1 103
P103 PC817
R9 2K
R25 470
R10 470
CK8 474 25V
U101 TL431
Z5 NC
Z1 18V
Q2 4401
R8 2K
+VC
P102 PC817
R16 3K
Q4 3904
R24 10K
R23 10K
C5 103
R12 100K 1%
R11 10K 1%
R13 10K 1%
R21 3K
STB
T103 EF25
RK1 10
CK1 222
D103 20A 45V
D13 NC
C109 2200uF 10V KF
C110 1000uF 10V KF
L104 1.5uH
Z101 TVS 6.8V
C113 220uF 16V
GND
D3 HER103
T103
C111 47uF 25V
R18 1K
Q3 4403
R14 0
Z2 NC
+5VSB
+VB
+12V1
R22 68K
Z4 15V
Q8 25V 45A
CK7 NC
C3 224
C127 100uF 35V
+5V
Q6 3906
Q5 3904
R29 4.7K
C132 104
R30 4.7K
C6 473
R31 470
R35 10K
SB
R34 33K
+5VSB
R33 100
A
Q10 3904
Q11 3904
R36 10K
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Size A3
Number
Revision
Date: 21-May-2008
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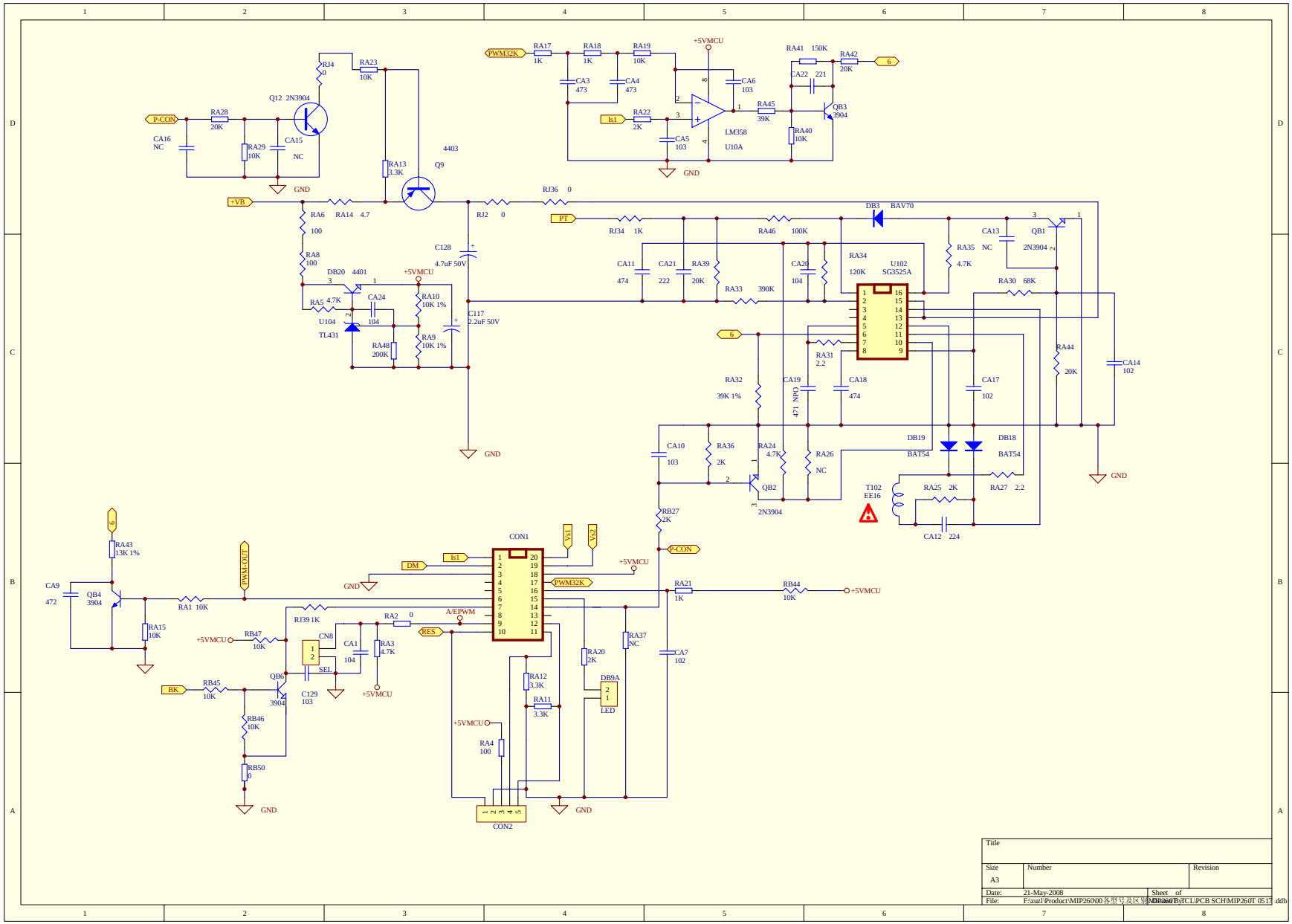

P-CON
RA28 20K
CA16 NC
RA29 10K
CA15 NC
Q12 2N3904
RJ4 0
RA23 10K
RA13 3.3K
Q9 4403
GND
+VB
RA6 100
RA14 4.7
RA8 100
DB20 4401
RA5 4.7K
U104 TL431
CA24 104
RA10 10K 1%
RA9 10K 1%
RA48 200K
C128 4.7uF 50V
C117 2.2uF 50V
RJ2 0
RJ36 0
PWM32K
RA17 1K
RA18 1K
RA19 10K
CA3 473
CA4 473
+5VMCU
CA6 103
Is1
RA22 2K
CA5 103
LM358 U10A
RA41 150K
RA42 20K
CA22 221
RA45 39K
QB3 3904
RA40 10K
PT
RJ34 1K
RA46 100K
DB3 BAV70
CA11 474
CA21 222
RA39 20K
RA33 390K
CA20 104
RA34 120K
U102 SG3525A
RA35 4.7K
CA13 NC
QB1 2N3904
RA30 68K
RA31 2.2
RA32 39K 1%
CA19 471 NPO
CA18 474
CA17 102
RA44 20K
CA14 102
CA10 103
RA36 2K
RA24 4.7K
RA26 NC
QB2 2N3904
DB19 BAT54
DB18 BAT54
T102 EE16
RA25 2K
RA27 2.2
CA12 224
RB27 2K
CON1
Vs1
Vs2
DM
PWM32K
RA21 1K
RB44 10K
RA43 13K 1%
CA9 472
QB4 3904
RA1 10K
RA15 10K
PWM-OUT
RJ39 1K
RA2 0
A/EPWM
RES
RB47 10K
CN8
CA1 104
RA3 4.7K
SEL
BK
RB45 10K
QB6 3904
C129 103
RB46 10K
RB50 0
RA12 3.3K
RA11 3.3K
RA4 100
RA20 2K
RA37 NC
DB9A LED
CA7 102
CON2
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Number
Revision
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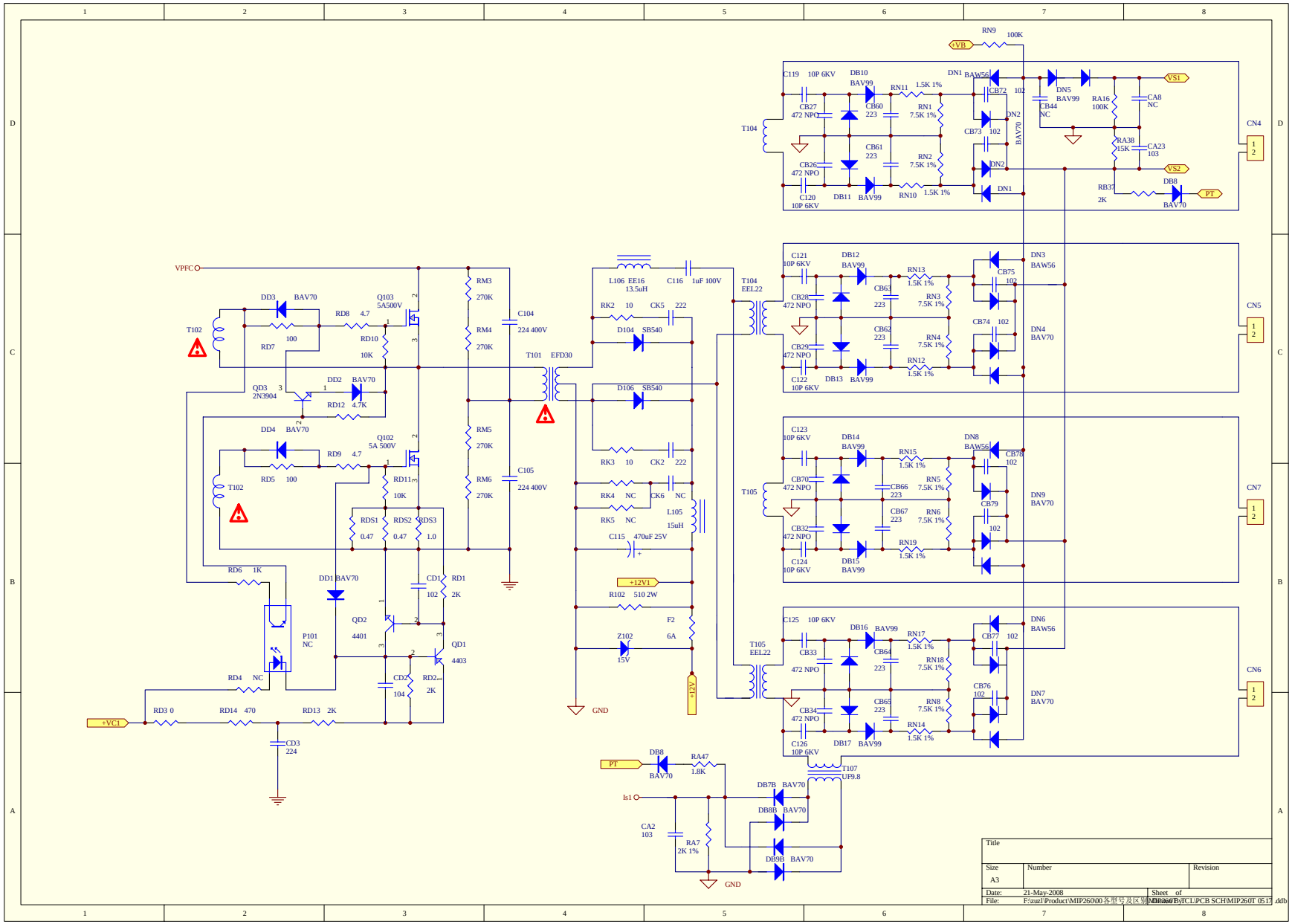

VPFC
T102
DD3 BAV70
RD8 4.7
Q103 5A500V
RD7 100
RD10 10K
QD3 2N3904
DD2 BAV70
RD12 4.7K
DD4 BAV70
RD9 4.7
Q102 5A 500V
RD5 100
RD11 10K
RDS1 0.47
RDS2 0.47
RDS3 1.0
RD6 1K
DD1 BAV70
CD1 102
RD1 2K
QD2 4401
QD1 4403
P101 NC
RD4 NC
CD2 104
RD2 2K
+VC1
RD3 0
RD14 470
RD13 2K
CD3 224
RM3 270K
RM4 270K
RM5 270K
RM6 270K
C104 224 400V
C105 224 400V
T101 EFD30
L106 EE16 13.5uH
C116 1uF 100V
RK2 10
CK5 222
D104 SB540
D106 SB540
RK3 10
CK2 222
RK4 NC
CK6 NC
RK5 NC
L105 15uH
C115 470uF 25V
+12V1
R102 510 2W
F2 6A
Z102 15V
+12V
GND
T104 EEL22
T105 EEL22
T107 UF9.8
PT
DB8 BAV70
RA47 1.8K
Is1
CA2 103
RA7 2K 1%
DB7B BAV70
DB8B BAV70
DB9B BAV70
+VB
RN9 100K
C119 10P 6KV
DB10 BAV99
RN11 1.5K 1%
DN1 BAW56
CB72 102
DN5 BAV99
RA16 100K
CA8 NC
VS1
CB27 472 NPO
CB60 223
RN1 7.5K 1%
CB44 NC
CB73 102
DN2 BAV70
RA38 15K
CA23 103
CB61 223
RN2 7.5K 1%
VS2
CB26 472 NPO
DN2
DB8 BAV70
RB37 2K
C120 10P 6KV
DB11 BAV99
RN10 1.5K 1%
DN1
CN4
C121 10P 6KV
DB12 BAV99
RN13 1.5K 1%
DN3 BAW56
CB75 102
CB28 472 NPO
CB63 223
RN3 7.5K 1%
CB74 102
DN4 BAV70
CB62 223
RN4 7.5K 1%
CB29 472 NPO
RN12 1.5K 1%
C122 10P 6KV
DB13 BAV99
CN5
C123 10P 6KV
DB14 BAV99
RN15 1.5K 1%
DN8 BAW56
CB78 102
CB70 472 NPO
CB66 223
RN5 7.5K 1%
CB79 102
DN9 BAV70
CB67 223
RN6 7.5K 1%
CB32 472 NPO
RN19 1.5K 1%
C124 10P 6KV
DB15 BAV99
CN7
C125 10P 6KV
DB16 BAV99
RN17 1.5K 1%
DN6 BAW56
CB77 102
CB33 472 NPO
CB64 223
RN18 7.5K 1%
CB76 102
DN7 BAV70
CB34 472 NPO
CB65 223
RN8 7.5K 1%
C126 10P 6KV
DB17 BAV99
RN14 1.5K 1%
CN6
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Number
Revision
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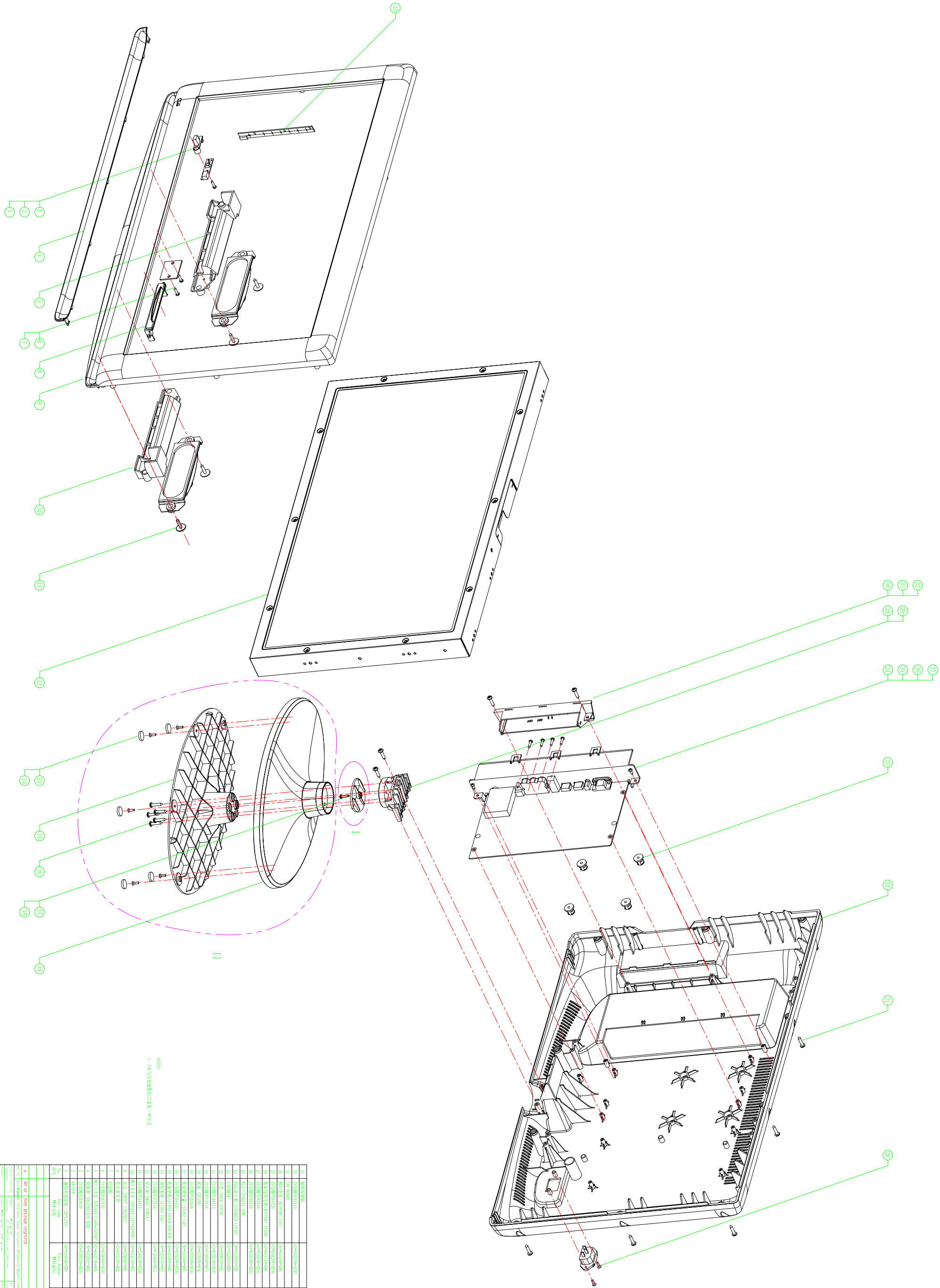
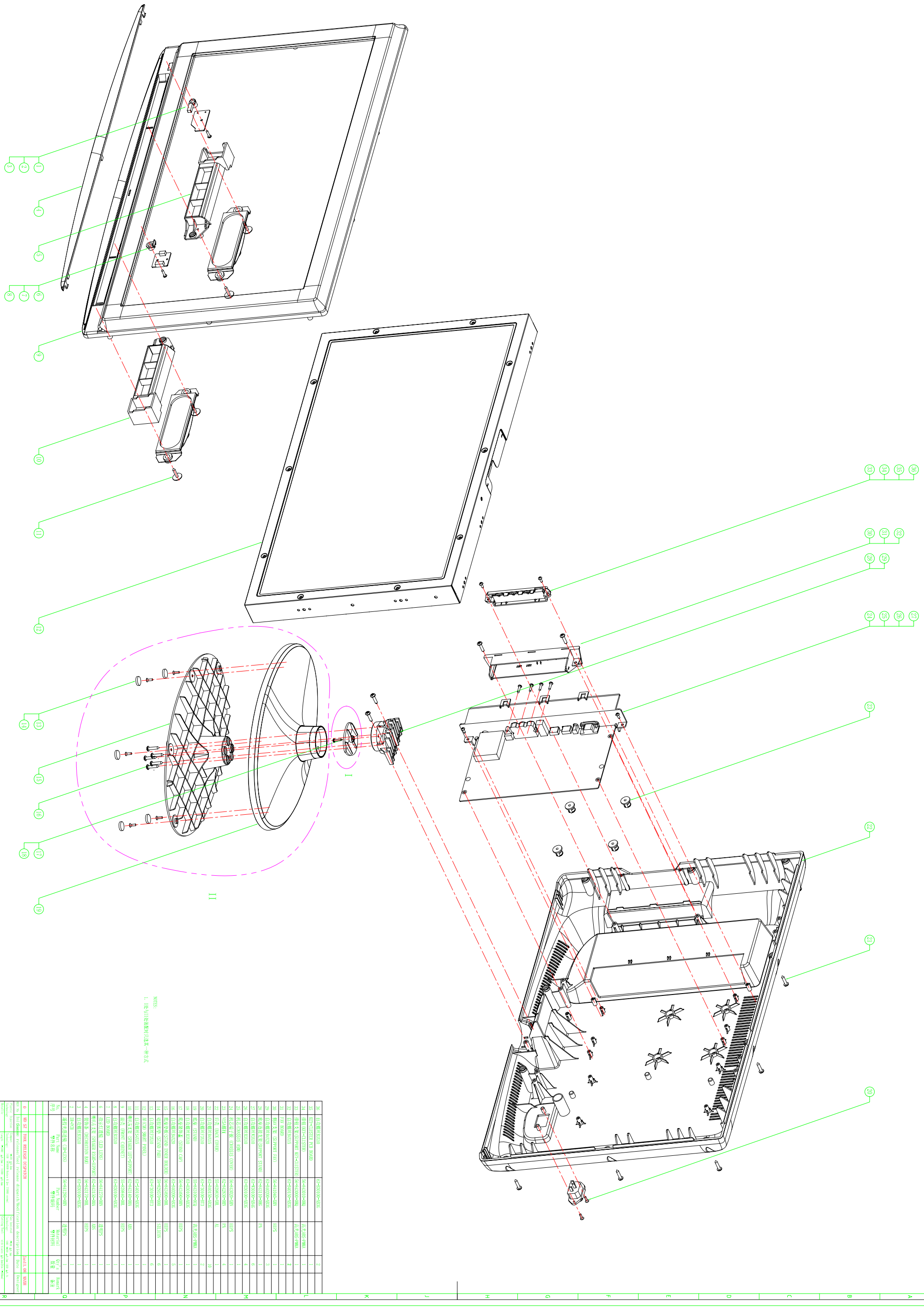


NOTES:
1. 1处与1处装配时只选其一种方式

No.	Part No.	Part Name 零件名称	Material 材料	Qty's 数量	Remark 备注
1	35-C00000-00X	遥控器前壳组 CAP-LENS	按需物	1	
2	03-200100-0036	自攻螺丝BA3X10		1	
3	03-200100-0036	自攻螺丝BA3X10		1	
4	04-010100-00X	电池盖 BACK COVER	ABS	1	
5	35-C00000-00X	喇叭盖板 SPEAKER RIGHT+LEFT	ABS	2	
6	03-200100-0036	自攻螺丝BA3X10		2	
7	35-C00000-00X	按键板		1	
8	35-C00000-00X	遥控器主板		1	
9	35-C00000-00X	遥控 (FRONT CAP/RIGHT)	ABS	1	
10	03-200100-0036	自攻螺丝BA3X10		1	
11	35-C00000-00X	喇叭盖板 SPEAKER LEFT+RIGHT	ABS	1	
12	03-200100-0036	自攻螺丝BA3X10		6	
13	03-200100-0036	自攻螺丝BA3X10		1	
14	35-C00000-00X	电池盖 STAND		1	
15	35-C00000-00X	电池架(STAND) POWER HOLDER	ABS	1	
16	35-C00000-00X	电池盖(STAND CAP)	ABS	1	
17	35-C00000-00X	电池盖(STAND CAP)	ABS	1	
18	03-200100-0036	自攻螺丝BA3X10		1	
19	35-C00000-00X	电池盖 STAND		1	
20	03-200100-0036	自攻螺丝BA3X10		2	
21	35-C00000-00X	底壳(CHASSIS ASSY)		1	
22	35-C00000-00X	底壳 (BACK COVER)		1	
23	03-200100-0036	自攻螺丝BA3X10		10	
24	03-200100-0036	自攻螺丝BA3X10		1	
25	35-C00000-00X	按键板		1	
26	03-200100-0036	自攻螺丝BA3X10		4	
27	03-200100-0036	自攻螺丝BA3X10		6	
28	35-C00000-00X	电池盖(STAND) POWER HOLDER	ABS	1	
29	03-200100-0036	自攻螺丝BA3X10		1	
30	03-200100-0036	自攻螺丝BA3X10		1	
31	03-200100-0036	自攻螺丝BA3X10		1	
32	35-C00000-00X	电池盖(STAND) POWER HOLDER	ABS	1	
33	03-200100-0036	自攻螺丝BA3X10		1	

0	MD SZ	TOOL RELEASE DISPATCH		Dec11.08	MAXM
No.	Modification	release/Tool release dispatch/modification description	Date		Designer

Part Name: 26634 EXPLODING DRAWING
Drawing No.: ********
Mechanical Department
Check: ******
Approve: ******
Material: ****
Scale: 1:1
Sheet 1/1



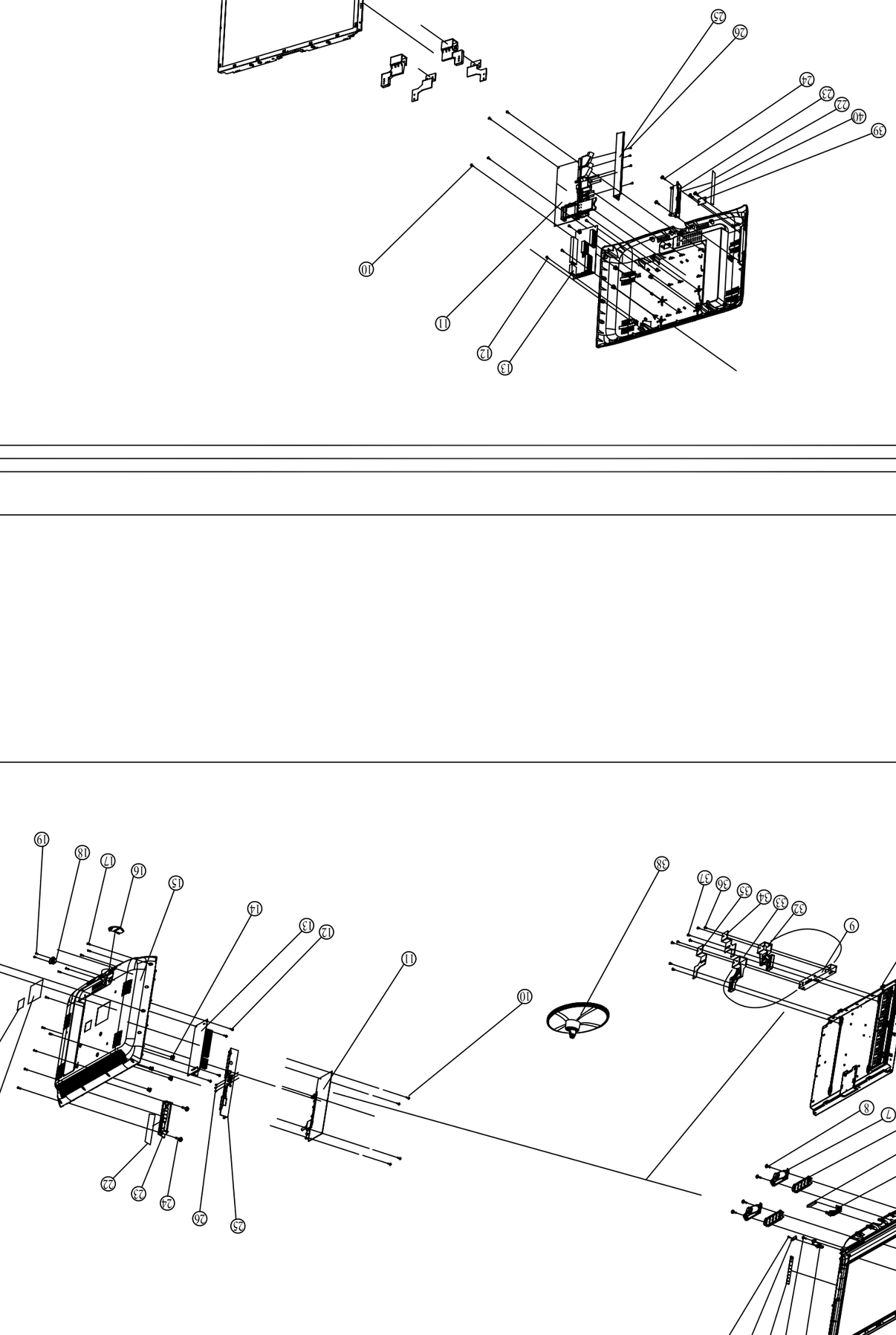
NOTES:
1. 结构与装配配制作法其一种方式

Item	Part No	Description	Qty	Remark
36	03-01000-0036	自攻螺丝BX3X10	2	
35	KEY-CLUSTER	按键-CLUSTER	1	
34	95-03000-0006	按键LOCD-CLUSTER	1	亮光ABS+PMMA
33	95-03000-0004	挂钩支架SUPPORT KEY-CLUSTER	1	亮光ABS+PMMA
32	03-00018-0036	自攻螺丝BA3X6	2	
31	95-04100-0006	PAD POWER	1	0.8THS
30	95-04100-0036	橡胶垫 减震PAD POWER	1	
29	03-00018-0036	自攻螺丝BA3X6	3	
28	95-04100-0004	橡胶垫支架减震PAD SUPPORT STAND	1	PA
27	03-00018-0036	自攻螺丝BA3X6	6	
26	03-00018-0036	自攻螺丝BA3X10	4	
25	03-04100-0036	减震垫 CHASSIS ASSY	1	
24	95-03000-0003	前后盖子板 CHASSIS COVER	1	0.8THS
23	95-03000-0036	铭牌贴纸1	1	PET
22	95-03000-0036	铭牌贴纸2	1	PET
21	95-03000-0036	铭牌贴纸3	1	PET
20	03-00018-0036	自攻螺丝BA3X6	10	
19	95-03100-0004	喇叭支架 STAND	2	亮光ABS+PMMA
18	03-00100-0036	自攻螺丝BA3X8	1	
17	95-03000-0004	电池盖挂钩A STAND CAP	1	0.8THS
16	03-00100-0036	自攻螺丝BA3X8	3	
15	95-03100-0004	电池盖挂钩B STAND CAP	1	0.8THS
14	95-03000-0004	电池盖 BATTERY COVER	1	0.8THS
13	95-03000-0003	电池盖铰链STAND CAP	1	0.8THS
12	03-00100-0036	自攻螺丝BA3X8	6	
11	03-00100-0036	自攻螺丝BA3X5	1	
10	95-03100-0003	喇叭支架 SPEAKER LEFT+RIGHT	2	亮光ABS+PMMA
9	95-03000-0004	遮光 CONTRAST	1	0.8THS
8	03-00100-0036	自攻螺丝BA3X8	1	
7	95-04100-0004	LED 导光柱 LED LENS	1	透明PC
6	95-04100-0004	指示灯支架 LED HOLDER ASSY	1	ABS
5	95-04100-0004	喇叭支架 SPEAKER ASSY+RIGHT	1	ABS
4	95-04100-0004	按键支架 DECORATION BAR	1	0.8THS
3	03-00100-0036	自攻螺丝BX3X8	1	
2	95-01200-0004	11P-CTB	1	
1	95-01200-0004	遥控发射器装配 CUP-LENS	1	透明PC
No. 序号	Part Number 型号/编码	Part Name 零件名称	Q'ty/S 数量	Remark 备注

0	WD S2	TOOL RELEASE DISPATCH				Dec11.08	WANG
No.	Modification	release/Tool release dispatch/modification description	Date	Designer			

Plastic Injection Enclosure	Color: Pantone 877C Texture: Sand Blasting	Gen. Material: ABS+PC Technology: 2K Molding	Plastic Injection Enclosure	Color: Pantone 877C Texture: Sand Blasting	Gen. Material: ABS+PC Technology: 2K Molding	Plastic Injection Enclosure	Color: Pantone 877C Texture: Sand Blasting

Top Name: **********	P/O No.: *******	Date No.: *******	Top Name: **********	P/O No.: *******	Date No.: *******	Top Name: **********	P/O No.: *******
Part Name:	Drawn: *******	Check: *******	Part Name:	Drawn: *******	Check: *******	Part Name:	Drawn: *******
2H598 EXPLODING DRAWING	Approve: *******	Material: ****	2H598 EXPLODING DRAWING	Approve: *******	Material: ****	2H598 EXPLODING DRAWING	Approve: *******
TCL Mechanical Department	Scale: 1:1	Sheet: 1/1	TCL Mechanical Department	Scale: 1:1	Sheet: 1/1	TCL Mechanical Department	Scale: 1:1



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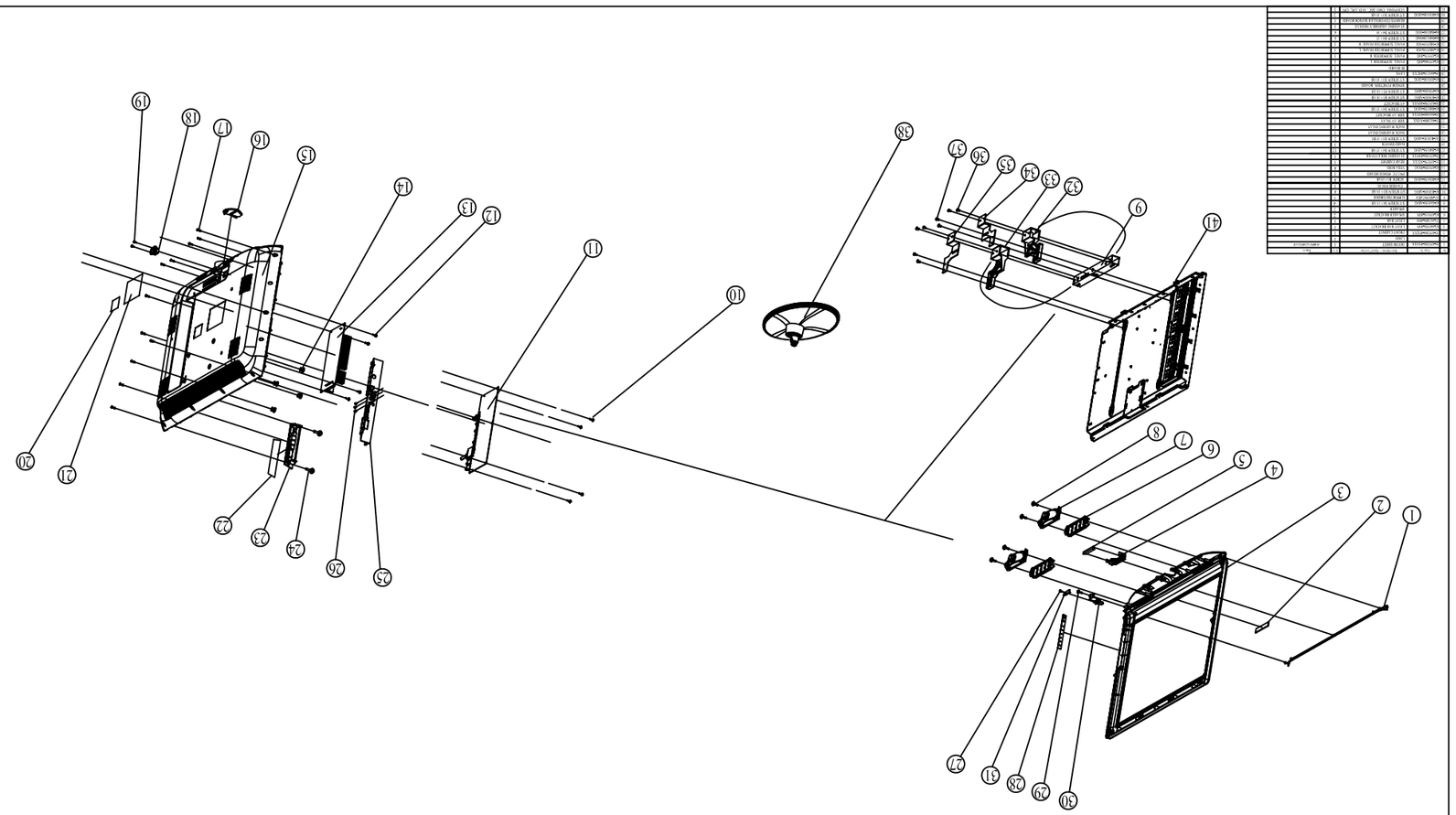

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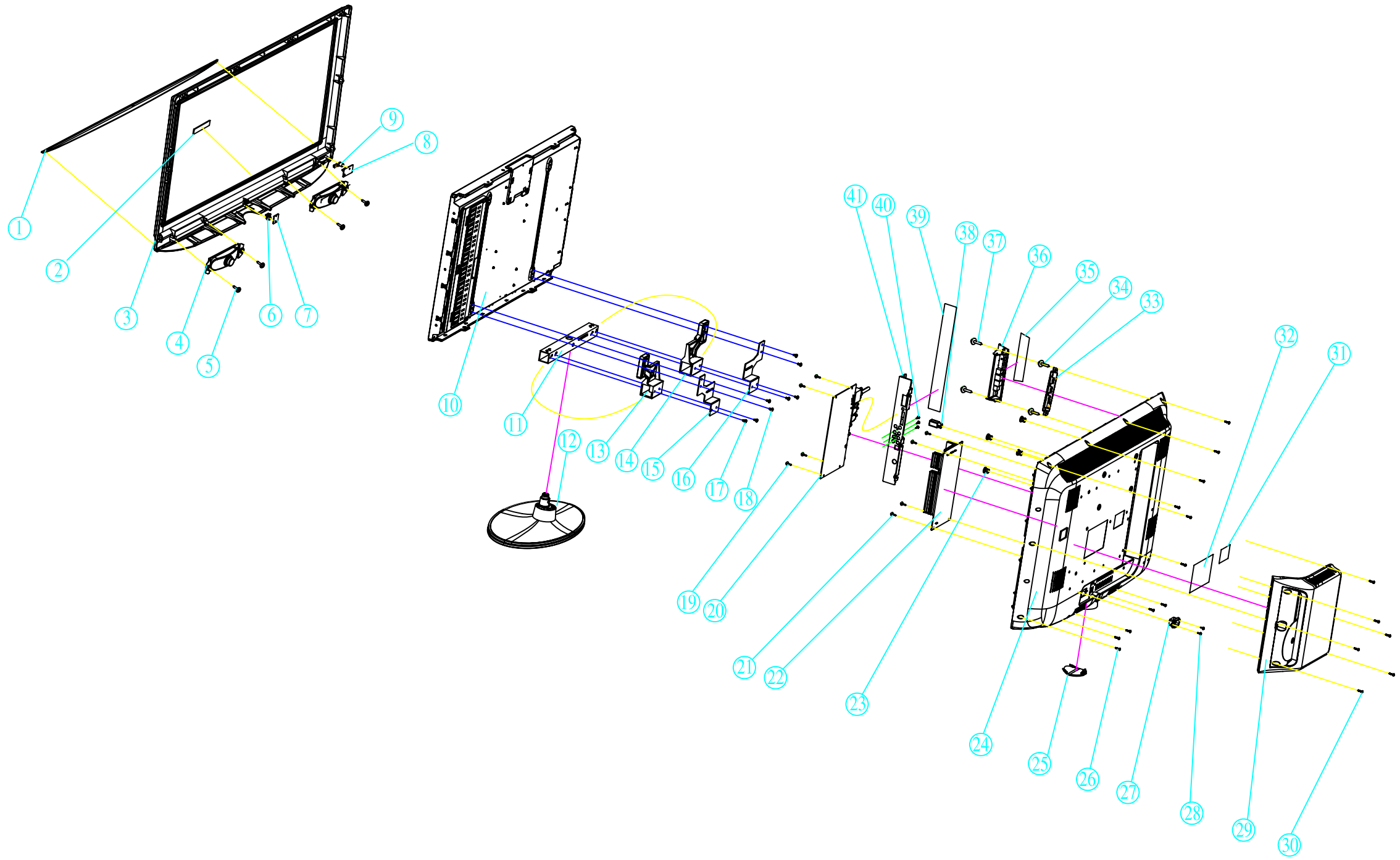

No.	Code No.	Description ; Specification	Qty	Remark
1	56-01175-06-01-XXXX	DECOR SHEET	1	
2	56-01175-06-01-XXXX	LOGO	1	
3	55-01175-06-01-XXXX	FRONT CABINET	1	
4	55-01175-06-XXXX	SPEAKER	1	
5	55-01175-06-XXXX	2.0X8 X 4 X 4	1	
6	56-01175-06-XXXX	Indicator LENS	1	
7	56-01175-06-XXXX	Indicator PCB	1	
8	56-01175-06-XXXX	REMOTE CONTROL PCB	1	
9	56-01175-06-XXXX	Remote LENS	1	
10	56-01175-06-XXXX	LCD PANEL	1	
11	55-01175-06-01-X	SUPPORTER CORDER	1	
12	55-01175-06-01-X	STANDING ASSEMBLY MODULE	1	
13	55-01175-06-01-X	PANEL SUPPORTER L	1	
14	55-01175-06-01-X	PANEL SUPPORTER R	1	
15	55-01175-06-01-X	PANEL SUPPORTER FRAME L	1	
16	55-01175-06-01-X	PANEL SUPPORTER FRAME R	1	
17	55-01175-06-01-X	ST SCREW B4 X 12	1	
18	55-01175-06-01-X	ST SCREW B4 X 12	1	
19	55-01175-06-01-X	ST SCREW W3 X 12 AB	1	
20	55-01175-06-01-X	ST SCREW W3 X 12 AB	1	
21	55-01175-06-01-X	MINI - CHASSIS	1	
22	55-01175-06-01-X	ST SCREW W3 X 12 AB	1	
23	55-01175-06-01-X	PWTUC POWER BOARD	1	
24	55-01175-06-01-X	VESA BOSS	1	
25	55-01175-06-01-XXXX	REAR CABINET	1	
26	55-01175-06-01-XXXX	STANDING HOLE COVER	1	ONLY BE USED IF NO STANDING
27	55-01175-06-01-X	ST SCREW B4 X 15 AB	1	
28	55-01175-06-01-X	AC INLET SOCKET	1	
29	55-01175-06-01-X	ST SCREW B4 X 15 AB	1	
30	55-01175-06-01-X	DVD COMBO MODULE	1	ACCORDING TO MARKET NEEDING
31	55-01175-06-01-X	ST SCREW B4 X 30 AB	1	ACCORDING TO MARKET NEEDING
32	55-01175-06-01-X	BACK WARNING INLAY	1	
33	55-01175-06-01-X	BACK WARNING INLAY	1	
34	55-01175-06-01-XXXX	Keypad	1	LEFT-CLUSTER ASSEMBLY MODULE
35	55-01175-06-01-X	ST SCREW B4 X 15 AB	1	
36	55-01175-06-01-XXXX	SIDE AV INLAY	1	
37	55-01175-06-01-XXXX	SIDE AV BRACKET	1	SIDE AV BRACKET ASSEMBLY MODULE
38	55-01175-06-01-X	ST SCREW B4 X 15 AB	1	
39	55-01175-06-01-X	RUBBER SPACER FOR PANEL	1	
40	55-01175-06-01-XXXX	AV BRACKET INLAY	1	ONLY BE USED IN CN MARKET
41	55-01175-06-01-X	ST SCREW B4 X 15 AB	1	ACCORDING TO CHASSIS NEEDING
42	55-01175-06-01-XXXX	AV BRACKET	1	