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MS-7529

Version 1.1

CPU:

Intel Conroe (65W Dual core)

System Chipset:

Intel Bearlake - MCH (North Bridge)

Intel ICH7R (South Bridge)

On Board Chipset:

BIOS -- SPI

HD -- ALC888

LPC Super I/O -- F71882FG

LAN-- REALTEK RTL8111C Co-lay RTL8101E

CLOCK -- RTM876-665

Main Memory:

DDR II *2 (Max 4GB)


Expansion Slots:

PCI2.3 SLOT * 2

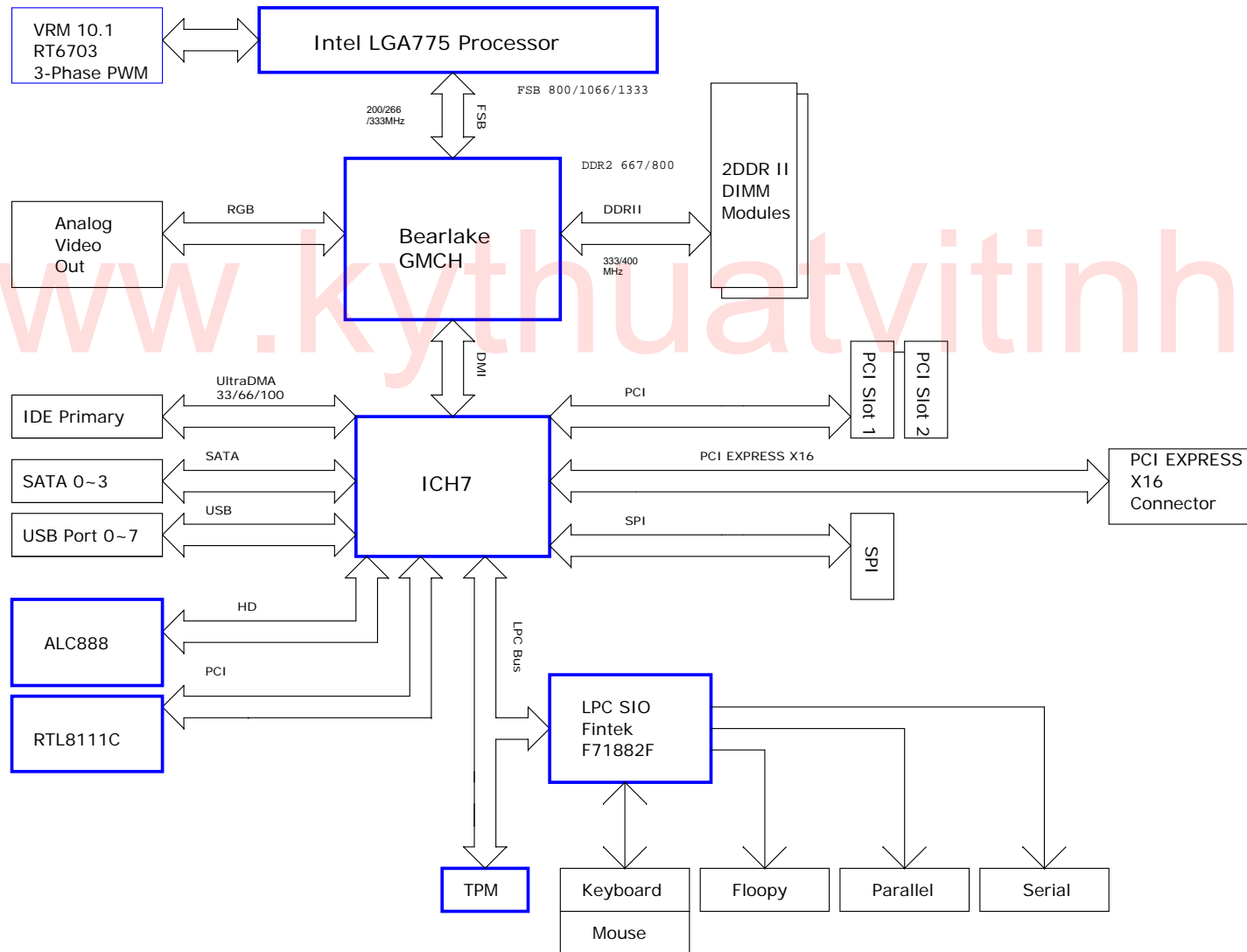
PCI EXPRESS X16 SLOT

ST PWM:

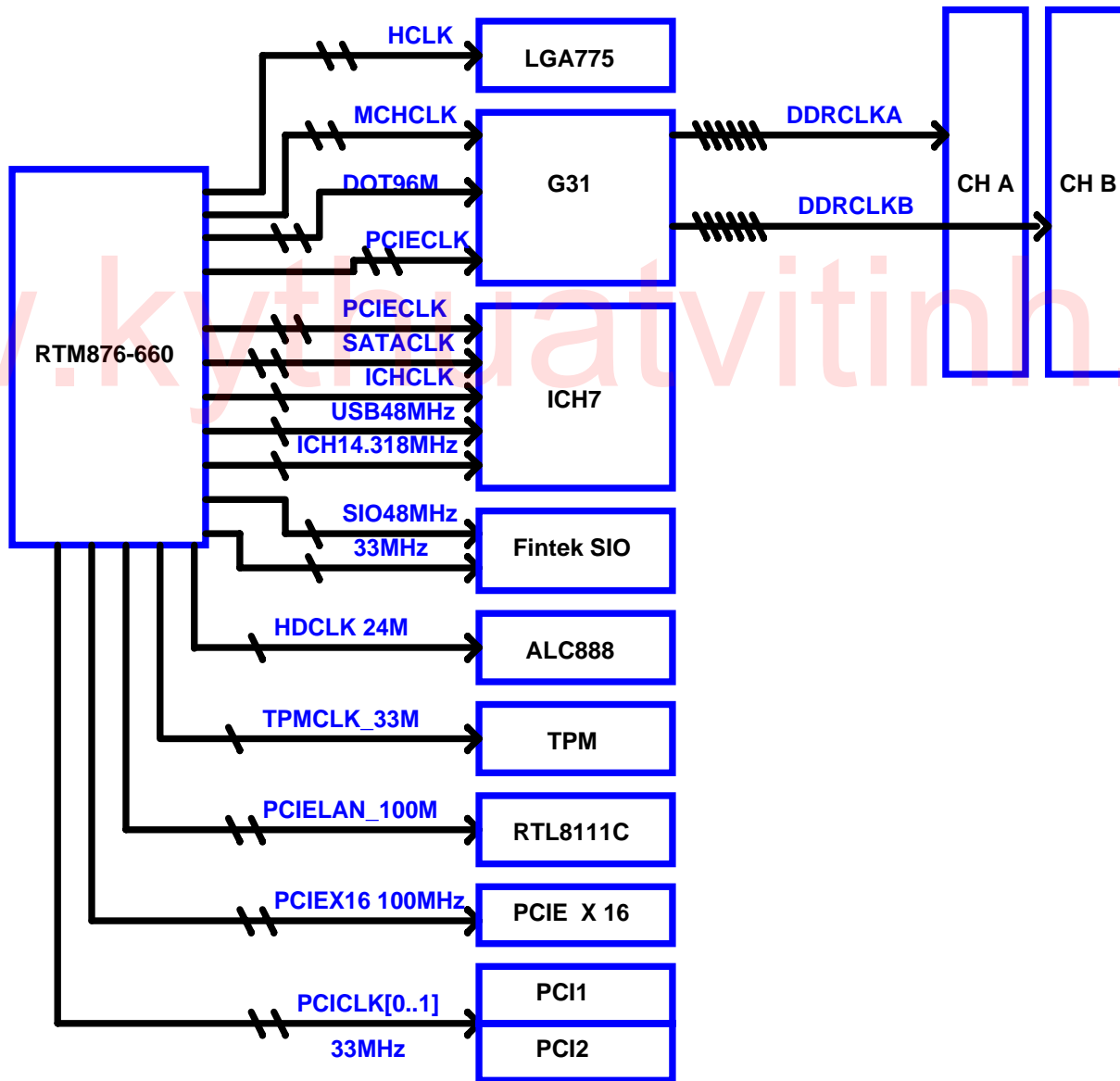
Controller: 3 PHASES

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Block Diagram



CLOCK MAP

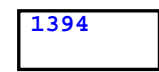
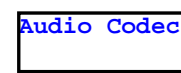
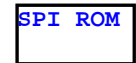
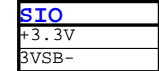
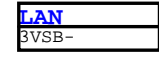
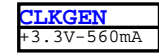
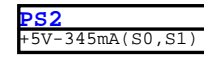
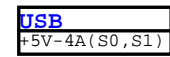
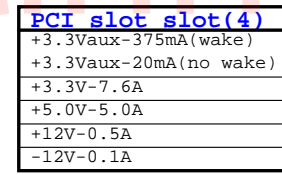
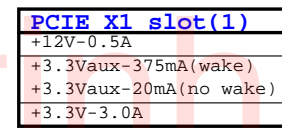
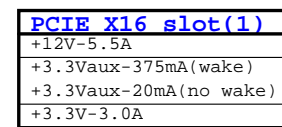
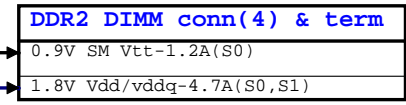
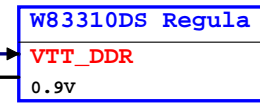
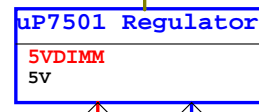
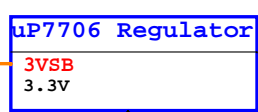
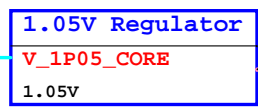
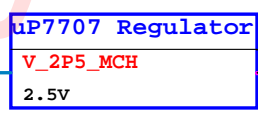
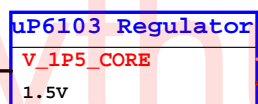
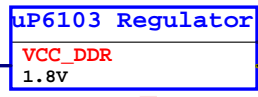
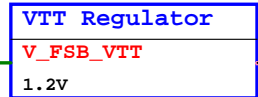
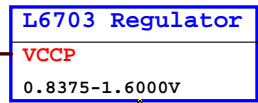
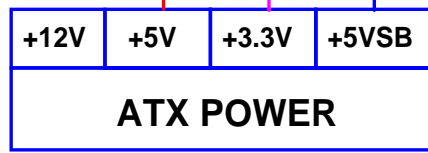
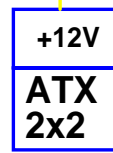


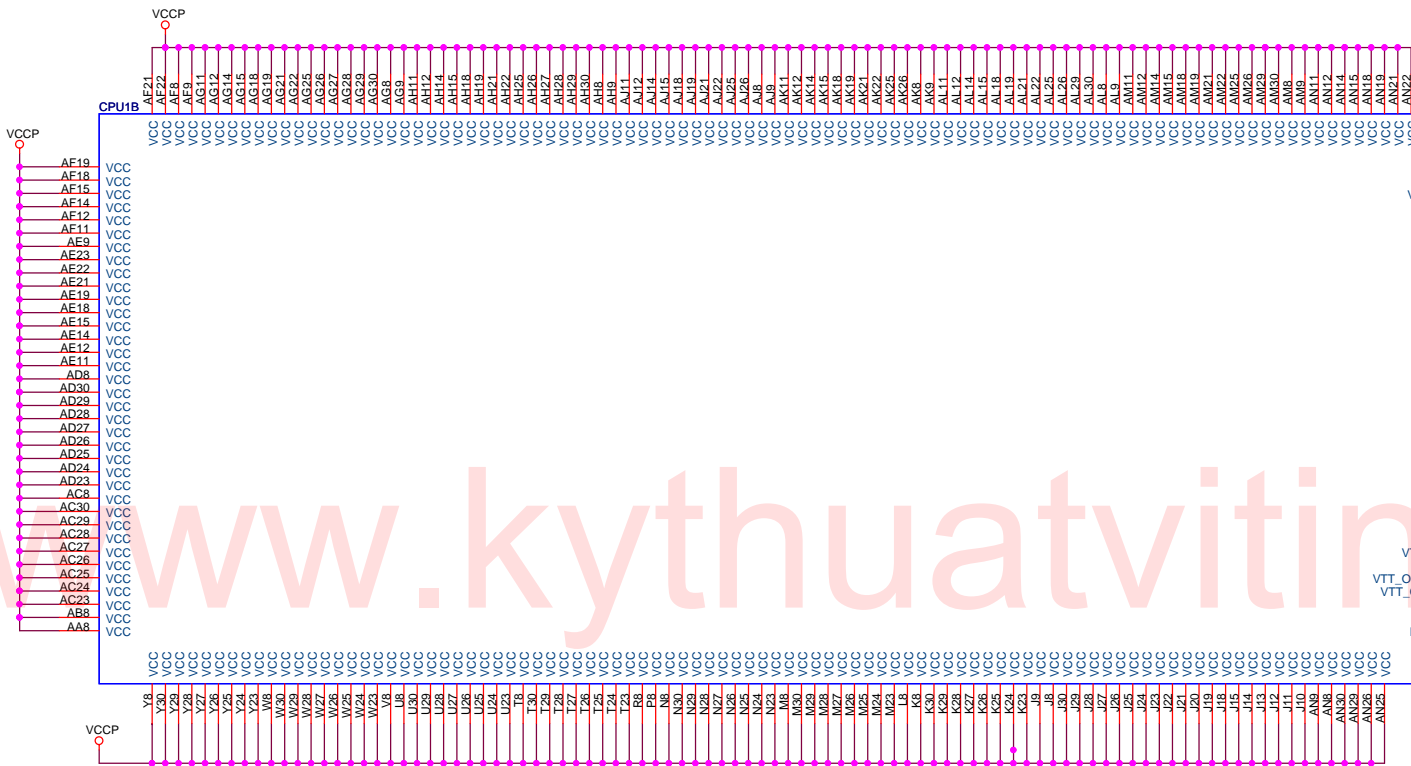
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MS-7529		
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Processor
0.8375-1.6000V Core-125A
1.2V FSB Vtt-5.3A
VCCPLL
VCC-IOPLL & VCCA

G31 MCH
1.2V FSB Vtt-0.9A
1.8V DDR2 I/O-4.4A(S0,S1)
1.8V DDR2 I/O-25mA(S3)
0.9V DDR2 VREF-2mA
0.9V DDR2 SB_VREF-10uA
DDR2 Resister Comp V-36mA
DDR2 Resis Comp SB_V-10uA
1.5V Core-13.8A(Integrated)
1.5V Core-8.9A(Discrete)
1.5V PCI Express&DMI-1.5A
1.5V PCIE&DMI PLL-45mA
1.5V HOST PLL-45mA
1.5V VCCA_DPLLA&B-55mA
1.5V MPLL-66mA
2.5V DAC-70mA*
2.5V HV-3mA
2.5V CMOS-2.0mA

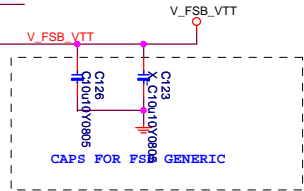
ICH7
1.2V VCC_CPU-14mA
1.05V Core-0.86A
VCC1_5A*-1.01A
VCC1_5B*-0.77A
5VRef-6mA
5VrefSus-10mA
+3.3V-0.33A
RTC-6uA(G3)
3.3V VccSus*-52mA
VccSus1_05V-See Note 1
VccUSBPLL-10mA
VccDMIPLL-50mA
VccSATAIPLL-50mA



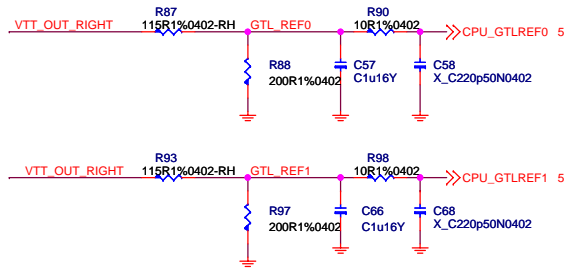


VCCA A23 H VCCA
 VSSA B23 H VSSA
 VCCPLL D23 H VCCPLL
 VCC-IOPLL C23 H VCCA

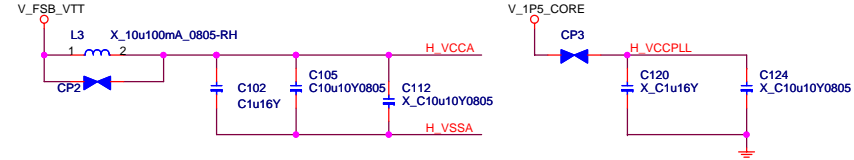
VTT A25
 VTT A26
 VTT A27
 VTT A28
 VTT A29
 VTT A30
 VTT B25
 VTT B26
 VTT B27
 VTT B28
 VTT B29
 VTT B30
 VTT C25
 VTT C26
 VTT C27
 VTT C28
 VTT C29
 VTT D25
 VTT D26
 VTT D27
 VTT D28
 VTT D29
 VTT D30
 VTT AM6 VTT_PWG
 VTT_OUT_RIGHT AA1 VTT_OUT_RIGHT
 VTT_OUT_LEFT VTT_OUT_LEFT
 VTT_SEL F27 VTT_SEL
 RSVD#F29 F29 X



*GTLREF VOLTAGE SHOULD BE 0.67 * VTT = 0.8V (At VTT=1.2V)

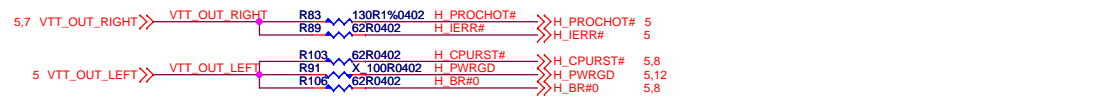


*PLACE COMPONENTS AS CLOSE AS POSSIBLE TO PROCESSOR SOCKET
 *TRACE WIDTH TO CAPS MUST BE NO SMALLER THAN 12MILS

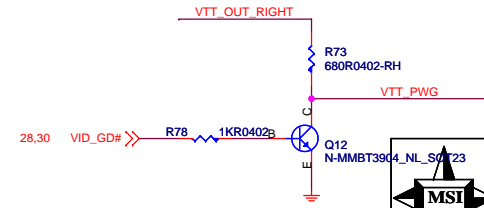


ZIF-SOCK775-15U-IN,ZIF-SOCK775-15U-IN_TH

PLACE AT CPU END OF ROUTE



VTT_PWRGOOD



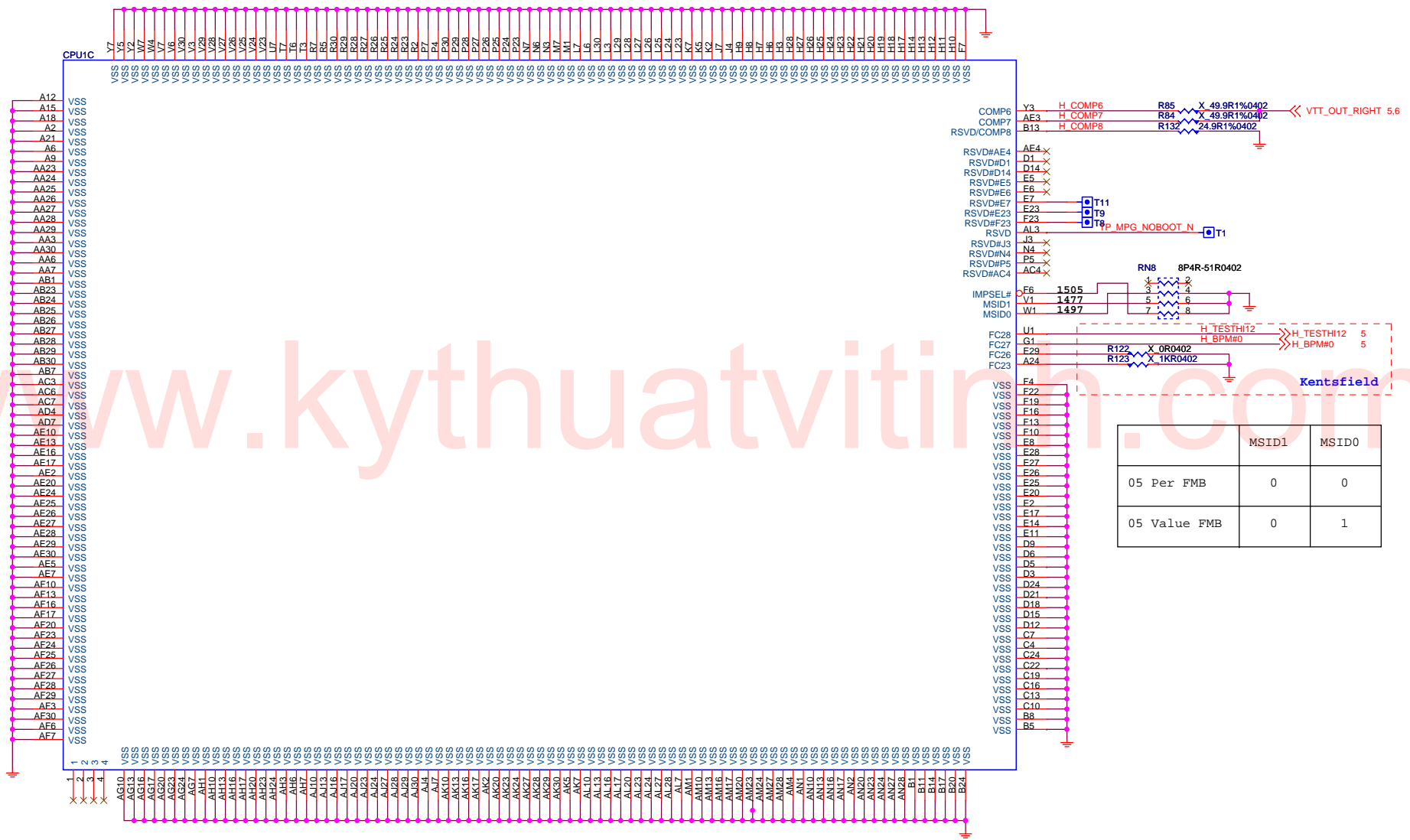
VTT_PWG SPEC :
 High > 0.9V
 Low < 0.3V
 Trise < 150ns

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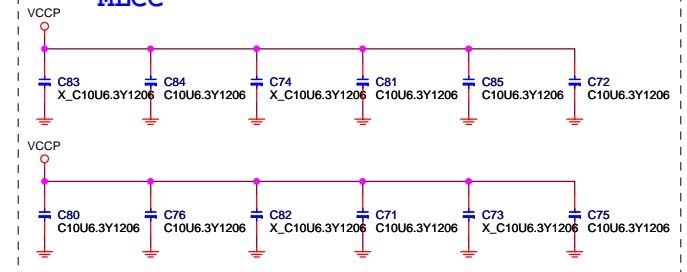
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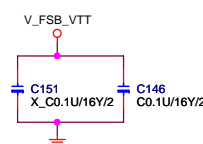
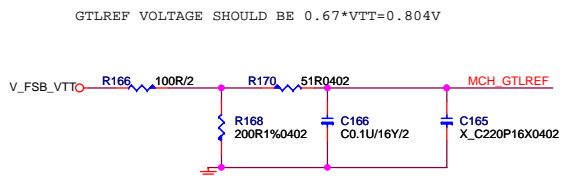
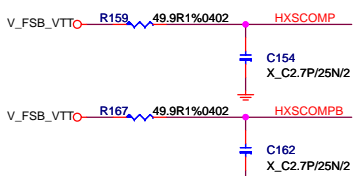
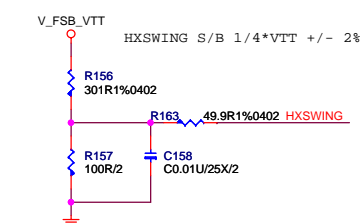
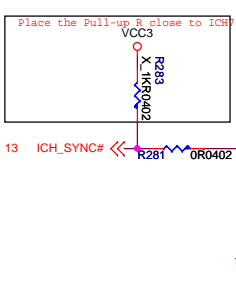
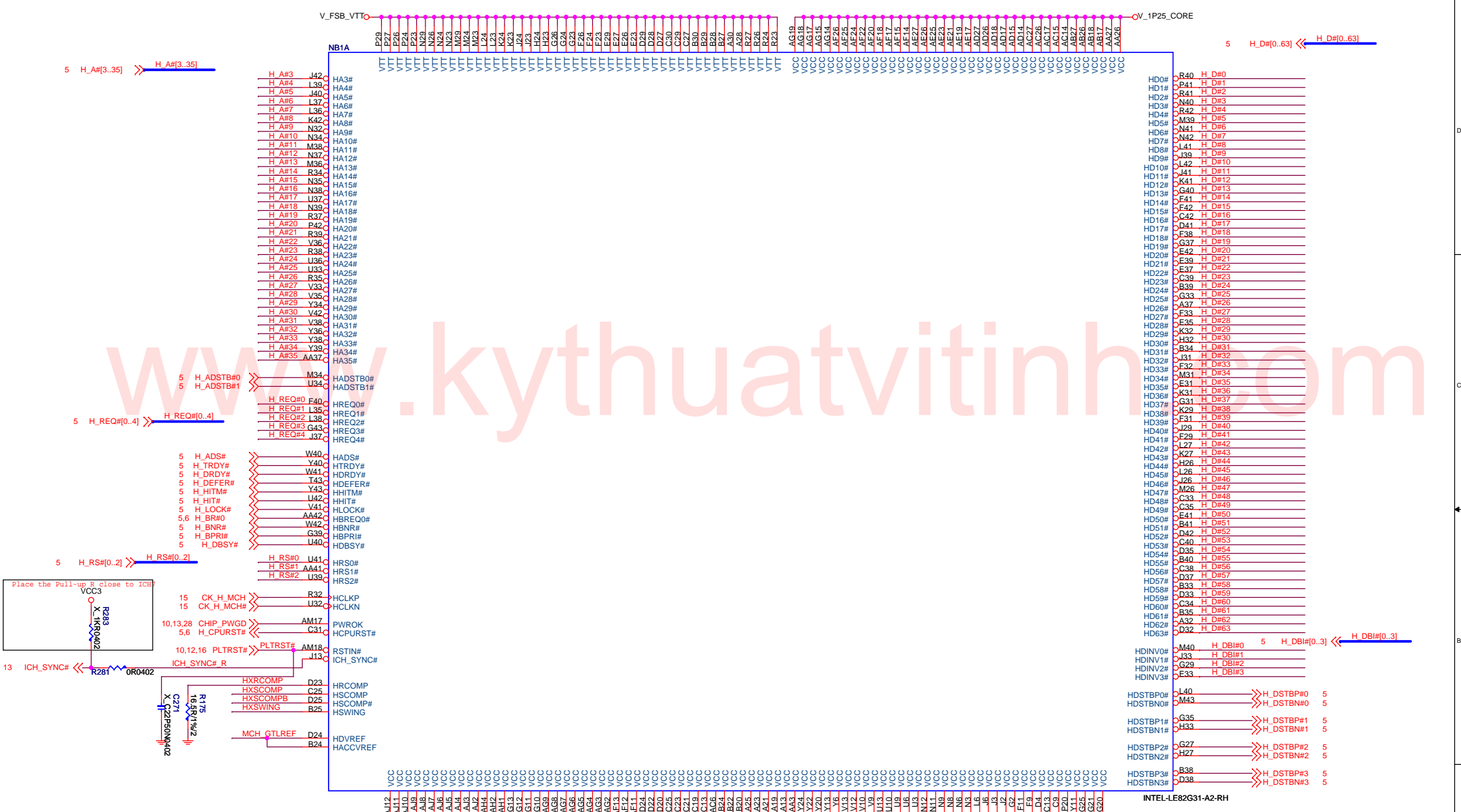


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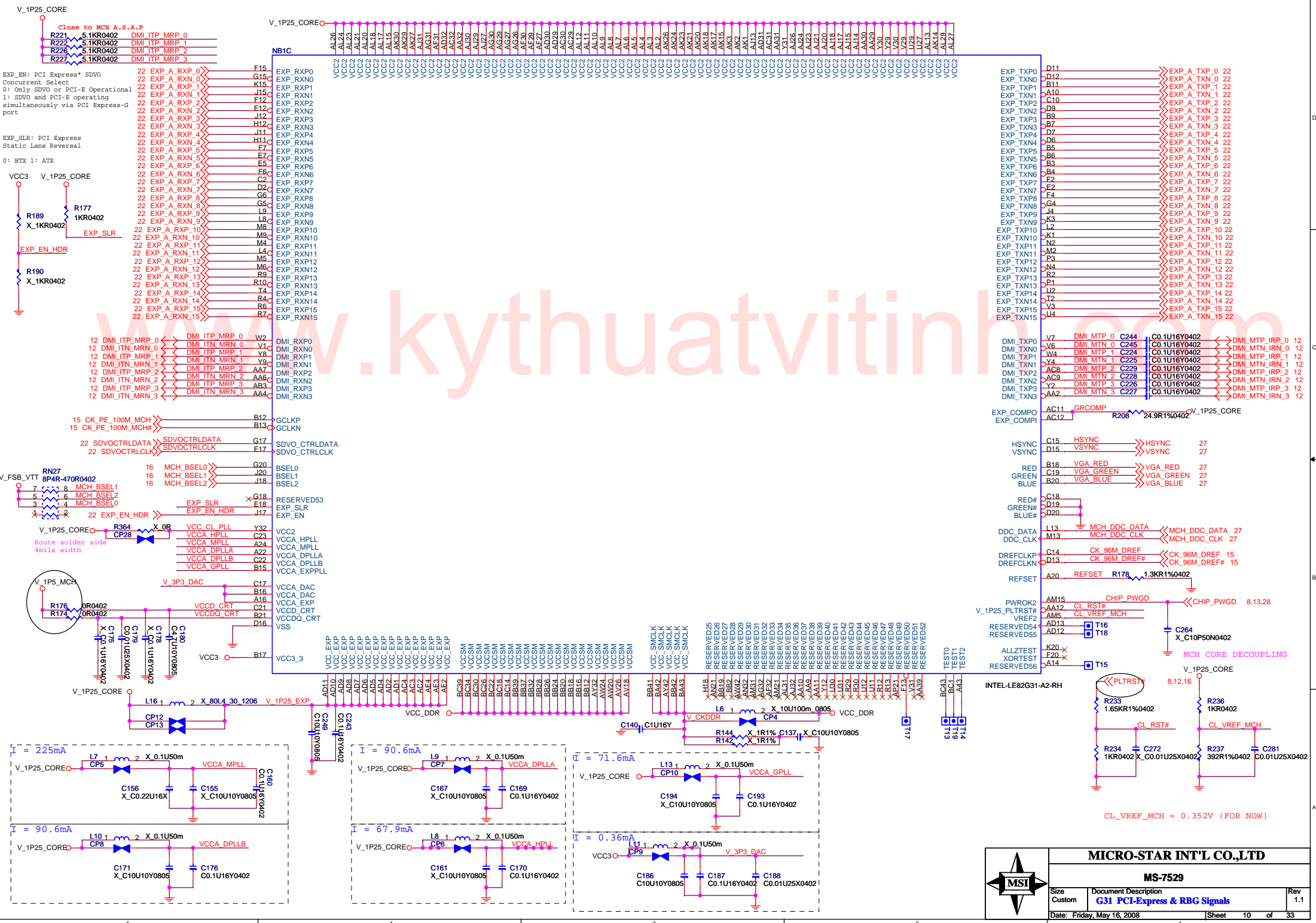
ZIF-SOCK775-15U-IN,ZIF-SOCK775-15U-IN_TH (Place into CPU Socket Cavity)



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V_1P25_CORE

V_1P25_CORE

Close to MCH A.S.A.P
 R221 5.1KR0402 DMI ITP MRP 0
 R222 5.1KR0402 DMI ITP MRP 1
 R226 5.1KR0402 DMI ITP MRP 2
 R227 5.1KR0402 DMI ITP MRP 3

EXP_EN: PCI Express* SDVO
 Concurrent Select
 0: Only SDVO or PCI-E Operational
 1: SDVO and PCI-E operating
 simultaneously via PCI Express-G
 port

EXP_SLR: PCI Express
 Static Lane Reversal
 0: BTX 1: ATX

VCC3 V_1P25_CORE
 R189 X_1KR0402
 EXP EN HDR
 R190 X_1KR0402

12 DMI ITP_MRP_0 DMI ITP_MRP_0 W2
 12 DMI ITN_MRN_0 DMI ITN_MRN_0 V1
 12 DMI ITP_MRP_1 DMI ITP_MRP_1 Y8
 12 DMI ITN_MRN_1 DMI ITN_MRN_1 Y3
 12 DMI ITP_MRP_2 DMI ITP_MRP_2 AA7
 12 DMI ITN_MRN_2 DMI ITN_MRN_2 AA6
 12 DMI ITP_MRP_3 DMI ITP_MRP_3 AB3
 12 DMI ITN_MRN_3 DMI ITN_MRN_3 AA4

15 OK_PE_100M_MCH G12 GCLKP
 15 OK_PE_100M_MCH+ B13 GCLKN

22 SDVOCTRLDATA G17 SDVO_CTRLDATA
 22 SDVOCTRLCLK E17 SDVO_CTRLCLK

V_FSB_VTT R27 8P4R-470R0402
 7 MCH BSEL1
 5 MCH BSEL2
 3 MCH BSEL0

V_1P25_CORE R364 X_0R
 CP28 VCC CL PLL Y32
 VCCA_HPLL C23
 VCCA_MPLL A24
 VCCA_DPLLA A22
 VCCA_DPLLB C22
 VCCA_GPLL B15
 VCCA_EXP C17
 VCCA_DAC B16
 VCCD_CRT A16
 VCCDQ_CRT B21
 VSS D16

V_1P5_MCH R176 DR0402
 R174 DR0402
 C176 X_C0.1U10Y0805
 C179 X_C0.1U16Y0402
 C180 X_C0.1U10Y0805

V_1P25_CORE L161 2 X 80L4_30_1206 V_1P25_EXP
 CP12
 CP13

V_1P25_CORE L7 1 CP5 2 X 0.1U50m VCCA_MPLL
 C156 X_C0.22U16X
 C155 X_C0.1U10Y0805
 C180 X_C0.1U16Y0402

V_1P25_CORE L10 1 CP8 2 X 0.1U50m VCCA_DPLLB
 C171 X_C0.1U10Y0805
 C176 X_C0.1U16Y0402

V_1P25_CORE L9 1 CP7 2 X 0.1U50m VCCA_DPLLA
 C167 X_C0.1U10Y0805
 C169 X_C0.1U16Y0402

V_1P25_CORE L8 1 CP6 2 X 0.1U50m VCCA_HPLL
 C161 X_C0.1U10Y0805
 C170 X_C0.1U16Y0402

VCC3 V_1P25_CORE
 L11 1 CP9 2 X 0.1U50m V_3P3_DAC
 C186 X_C0.1U10Y0805
 C187 X_C0.1U16Y0402
 C188 X_C0.0125X0402

AL26	VCC2	EXP_RXP0	F16	EXP_RXP0
AL24	VCC2	EXP_RXN0	G18	EXP_RXN0
AL23	VCC2	EXP_RXM1	K15	EXP_RXM1
AL21	VCC2	EXP_RXN1	J15	EXP_RXN1
AL20	VCC2	EXP_RXP2	F12	EXP_RXP2
AL18	VCC2	EXP_RXN2	E12	EXP_RXN2
AK30	VCC2	EXP_RXP3	J12	EXP_RXP3
AK29	VCC2	EXP_RXN3	H12	EXP_RXN3
AK27	VCC2	EXP_RXP4	J11	EXP_RXP4
AG30	VCC2	EXP_RXN4	H11	EXP_RXN4
AG27	VCC2	EXP_RXP5	F7	EXP_RXP5
AG26	VCC2	EXP_RXN5	E7	EXP_RXN5
AG24	VCC2	EXP_RXP6	F6	EXP_RXP6
AG23	VCC2	EXP_RXN6	C2	EXP_RXN6
AG22	VCC2	EXP_RXP7	D2	EXP_RXP7
AG21	VCC2	EXP_RXN7	G2	EXP_RXN7
AG20	VCC2	EXP_RXP8	G6	EXP_RXP8
AG19	VCC2	EXP_RXN8	G5	EXP_RXN8
AG18	VCC2	EXP_RXP9	L8	EXP_RXP9
AG17	VCC2	EXP_RXN9	M8	EXP_RXN9
AG16	VCC2	EXP_RXM10	M9	EXP_RXM10
AG15	VCC2	EXP_RXP11	M4	EXP_RXP11
AG14	VCC2	EXP_RXN11	L4	EXP_RXN11
AG13	VCC2	EXP_RXP12	M5	EXP_RXP12
AG12	VCC2	EXP_RXN12	M6	EXP_RXN12
AG11	VCC2	EXP_RXP13	R10	EXP_RXP13
AG10	VCC2	EXP_RXN13	R9	EXP_RXN13
AG9	VCC2	EXP_RXP14	T4	EXP_RXP14
AG8	VCC2	EXP_RXN14	R4	EXP_RXN14
AG7	VCC2	EXP_RXP15	R6	EXP_RXP15
AG6	VCC2	EXP_RXN15	R7	EXP_RXN15

VCC2	EXP_RXM15	W2	DMI_RXP0
VCC2	EXP_RXN15	V1	DMI_RXN0
VCC2	EXP_RXM16	Y8	DMI_RXP1
VCC2	EXP_RXN16	Y3	DMI_RXN1
VCC2	EXP_RXM17	AA7	DMI_RXP2
VCC2	EXP_RXN17	AA6	DMI_RXN2
VCC2	EXP_RXM18	AB3	DMI_RXP3
VCC2	EXP_RXN18	AA4	DMI_RXN3

B12	GCLKP	B12	OK_PE_100M_MCH
B13	GCLKN	B13	OK_PE_100M_MCH+
G17	SDVO_CTRLDATA	G17	SDVOCTRLDATA
E17	SDVO_CTRLCLK	E17	SDVOCTRLCLK
G20	BSEL0	G20	MCH_BSEL0
J20	BSEL1	J20	MCH_BSEL1
J18	BSEL2	J18	MCH_BSEL2
G18	RESERVED53	G18	EXP_SLR
F18	EXP_SLR	F18	EXP EN HDR
J17	EXP_EN	J17	EXP EN HDR

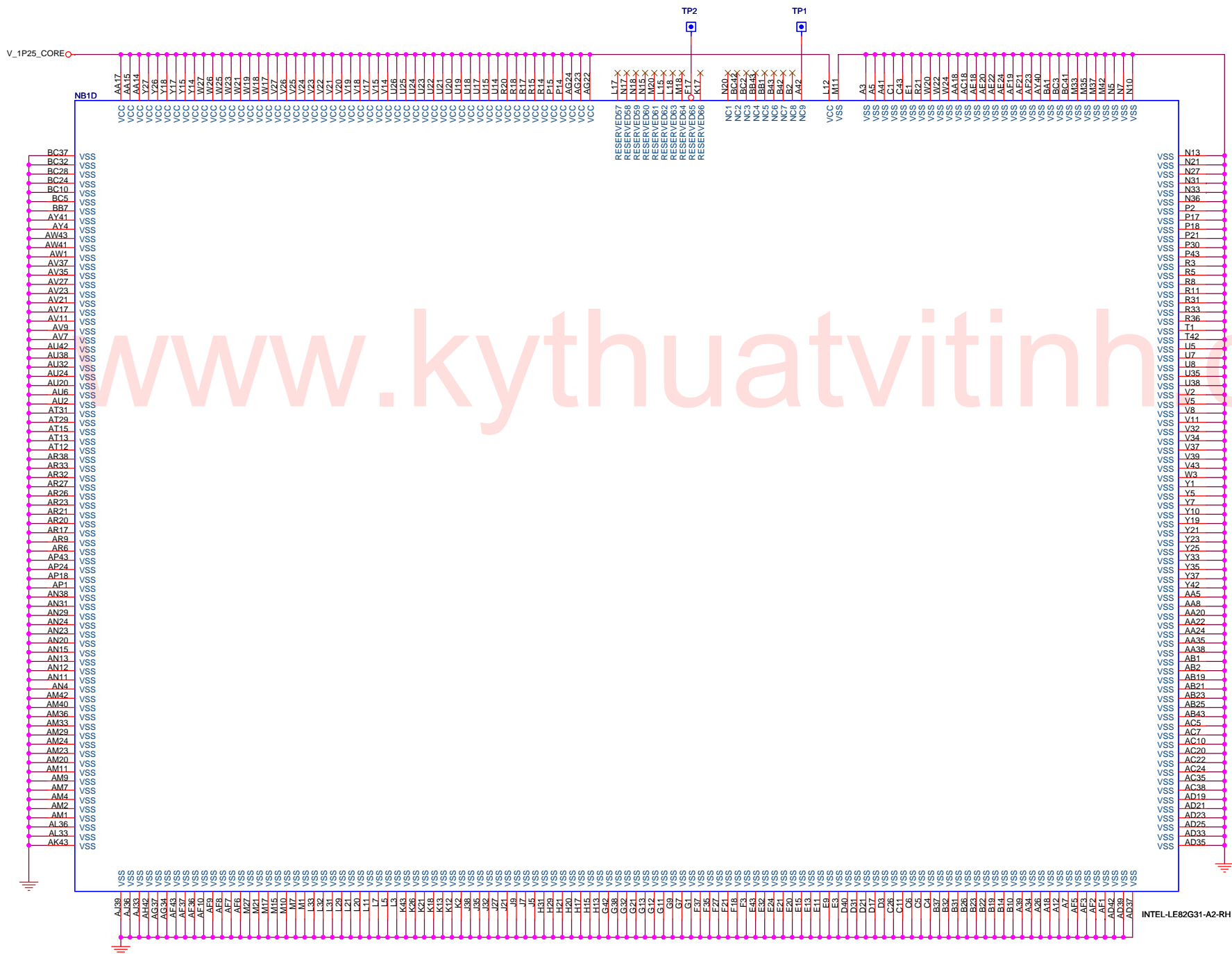
VCC2	EXP_RXM19	Y32	VCC CL PLL
C23	EXP_RXN19	C23	VCCA_HPLL
A24	EXP_RXM20	A24	VCCA_MPLL
A22	EXP_RXN20	A22	VCCA_DPLLA
C22	EXP_RXM21	C22	VCCA_DPLLB
B15	EXP_RXN21	B15	VCCA_GPLL
C17	EXP_RXM22	C17	VCCA_EXP
B16	EXP_RXN22	B16	VCCA_DAC
A16	EXP_RXM23	A16	VCCD_CRT
B21	EXP_RXN23	B21	VCCDQ_CRT
D16	EXP_RXM24	D16	VSS

VCC3	EXP_RXM25	B17	VCC3_3
VCC3	EXP_RXN25	B17	VCC3_3
VCC3	EXP_RXM26	B17	VCC3_3
VCC3	EXP_RXN26	B17	VCC3_3
VCC3	EXP_RXM27	B17	VCC3_3
VCC3	EXP_RXN27	B17	VCC3_3
VCC3	EXP_RXM28	B17	VCC3_3
VCC3	EXP_RXN28	B17	VCC3_3
VCC3	EXP_RXM29	B17	VCC3_3
VCC3	EXP_RXN29	B17	VCC3_3
VCC3	EXP_RXM30	B17	VCC3_3
VCC3	EXP_RXN30	B17	VCC3_3
VCC3	EXP_RXM31	B17	VCC3_3
VCC3	EXP_RXN31	B17	VCC3_3
VCC3	EXP_RXM32	B17	VCC3_3
VCC3	EXP_RXN32	B17	VCC3_3
VCC3	EXP_RXM33	B17	VCC3_3
VCC3	EXP_RXN33	B17	VCC3_3
VCC3	EXP_RXM34	B17	VCC3_3
VCC3	EXP_RXN34	B17	VCC3_3
VCC3	EXP_RXM35	B17	VCC3_3
VCC3	EXP_RXN35	B17	VCC3_3
VCC3	EXP_RXM36	B17	VCC3_3
VCC3	EXP_RXN36	B17	VCC3_3
VCC3	EXP_RXM37	B17	VCC3_3
VCC3	EXP_RXN37	B17	VCC3_3
VCC3	EXP_RXM38	B17	VCC3_3
VCC3	EXP_RXN38	B17	VCC3_3
VCC3	EXP_RXM39	B17	VCC3_3
VCC3	EXP_RXN39	B17	VCC3_3
VCC3	EXP_RXM40	B17	VCC3_3
VCC3	EXP_RXN40	B17	VCC3_3
VCC3	EXP_RXM41	B17	VCC3_3
VCC3	EXP_RXN41	B17	VCC3_3
VCC3	EXP_RXM42	B17	VCC3_3
VCC3	EXP_RXN42	B17	VCC3_3
VCC3	EXP_RXM43	B17	VCC3_3
VCC3	EXP_RXN43	B17	VCC3_3
VCC3	EXP_RXM44	B17	VCC3_3
VCC3	EXP_RXN44	B17	VCC3_3
VCC3	EXP_RXM45	B17	VCC3_3
VCC3	EXP_RXN45	B17	VCC3_3
VCC3	EXP_RXM46	B17	VCC3_3
VCC3	EXP_RXN46	B17	VCC3_3
VCC3	EXP_RXM47	B17	VCC3_3
VCC3	EXP_RXN47	B17	VCC3_3
VCC3	EXP_RXM48	B17	VCC3_3
VCC3	EXP_RXN48	B17	VCC3_3
VCC3	EXP_RXM49	B17	VCC3_3
VCC3	EXP_RXN49	B17	VCC3_3
VCC3	EXP_RXM50	B17	VCC3_3
VCC3	EXP_RXN50	B17	VCC3_3
VCC3	EXP_RXM51	B17	VCC3_3
VCC3	EXP_RXN51	B17	VCC3_3
VCC3	EXP_RXM52	B17	VCC3_3
VCC3	EXP_RXN52	B17	VCC3_3

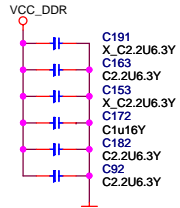
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VCC3	EXP_RXM55	B17	VCC3_3
VCC3	EXP_RXN55	B17	VCC3_3
VCC3	EXP_RXM56	B17	VCC3_3
VCC3	EXP_RXN56	B17	VCC3_3
VCC3	EXP_RXM57	B17	VCC3_3
VCC3	EXP_RXN57	B17	VCC3_3
VCC3	EXP_RXM58	B17	VCC3_3
VCC3	EXP_RXN58	B17	VCC3_3
VCC3	EXP_RXM59	B17	VCC3_3
VCC3	EXP_RXN59	B17	VCC3_3
VCC3	EXP_RXM60	B17	VCC3_3
VCC3	EXP_RXN60	B17	VCC3_3
VCC3	EXP_RXM61	B17	VCC3_3
VCC3	EXP_RXN61	B17	VCC3_3
VCC3	EXP_RXM62	B17	VCC3_3
VCC3	EXP_RXN62	B17	VCC3_3
VCC3	EXP_RXM63	B17	VCC3_3
VCC3	EXP_RXN63	B17	VCC3_3
VCC3	EXP_RXM64	B17	VCC3_3
VCC3	EXP_RXN64	B17	VCC3_3
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VCC3	EXP_RXN65	B17	VCC3_3
VCC3	EXP_RXM66	B17	VCC3_3
VCC3	EXP_RXN66	B17	VCC3_3
VCC3	EXP_RXM67	B17	VCC3_3
VCC3	EXP_RXN67	B17	VCC3_3
VCC3	EXP_RXM68	B17	VCC3_3
VCC3	EXP_RXN68	B17	VCC3_3
VCC3	EXP_RXM69	B17	VCC3_3
VCC3	EXP_RXN69	B17	VCC3_3
VCC3	EXP_RXM70	B17	VCC3_3
VCC3	EXP_RXN70	B17	VCC3_3
VCC3	EXP_RXM71	B17	VCC3_3
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VCC3	EXP_RXM72	B17	VCC3_3
VCC3	EXP_RXN72	B17	VCC3_3
VCC3	EXP_RXM73	B17	VCC3_3
VCC3	EXP_RXN73	B17	VCC3_3
VCC3	EXP_RXM74	B17	VCC3_3
VCC3	EXP_RXN74	B17	VCC3_3
VCC3	EXP_RXM75	B17	VCC3_3
VCC3	EXP_RXN75	B17	VCC3_3
VCC3	EXP_RXM76	B17	VCC3_3
VCC3	EXP_RXN76	B17	VCC3_3
VCC3	EXP_RXM77	B17	VCC3_3
VCC3	EXP_RXN77	B17	VCC3_3
VCC3	EXP_RXM78	B17	VCC3_3
VCC3	EXP_RXN78	B17	VCC3_3
VCC3	EXP_RXM79	B17	VCC3_3
VCC3	EXP_RXN79	B17	VCC3_3
VCC3	EXP_RXM80	B17	VCC3_3
VCC3	EXP_RXN80	B17	VCC3_3
VCC3	EXP_RXM81	B17	VCC3_3
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VCC3	EXP_RXM82	B17	VCC3_3
VCC3	EXP_RXN82	B17	VCC3_3
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VCC3	EXP_RXM100	B17	VCC3_3
VCC3	EXP_RXN100	B17	VCC3_3

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VCC3	EXP_RXN101	B17	VCC3_3
VCC3	EXP_RXM102	B17	VCC3_3
VCC3	EXP_RXN102	B17	VCC3_3
VCC3	EXP_RXM103	B17	VCC3_3
VCC3	EXP_RXN103	B17	VCC3_3
VCC3	EXP_RXM104	B17	VCC3_3
VCC3	EXP_RXN104	B17	VCC3_3
VCC3	EXP_RXM105	B17	VCC3_3
VCC3	EXP_RXN105	B17	VCC3_3
VCC3	EXP_RXM106	B17	VCC3_3
VCC3	EXP_RXN106	B17	VCC3_3
VCC3	EXP_RXM107	B17	VCC3_3
VCC3	EXP_RXN107	B17	VCC3_3
VCC3	EXP_RXM108	B17	VCC3_3
VCC3	EXP_RXN108	B17	VCC3_3
VCC3	EXP_RXM109	B17	VCC3_3
VCC3	EXP_RXN109	B17	VCC3_3
VCC3	EXP_RXM110	B17	VCC3_3
VCC3	EXP_RXN110	B17	VCC3_3
VCC3	EXP_RXM111	B17	VCC3_3
VCC3	EXP_RXN111	B17	VCC3_3
VCC3	EXP_RXM112	B17	VCC3_3
VCC3	EXP_RXN112	B17	VCC3_3
VCC3	EXP_RXM113	B17	VCC3_3
VCC3	EXP_RXN113	B17	VCC3_3
VCC3	EXP_RXM114	B17	VCC3_3
VCC3	EXP_RXN114	B17	VCC3_3
VCC3	EXP_RXM115	B17	VCC3_3
VCC3	EXP_RXN115	B17	VCC3_3
VCC3	EXP_RXM116	B17	VCC3_3
VCC3	EXP_RXN116	B17	VCC3_3
VCC3	EXP_RXM117	B17	VCC3_3
VCC3	EXP_RXN117	B17	VCC3_3
VCC3	EXP_RXM118	B17	VCC3_3
VCC3	EXP_RXN118	B17	VCC3_3
VCC3	EXP_RXM119	B17	VCC3_3
VCC3	EXP_RXN119	B17	VCC3_3
VCC3	EXP_RXM120	B17	VCC3_3
VCC3	EXP_RXN120	B17	VCC3_3

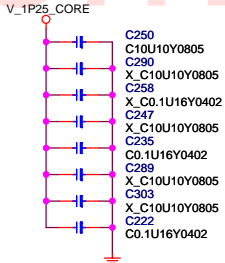
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VCC3	EXP_RXN121	B17	VCC3_3
VCC3	EXP_RXM122	B17	VCC3_3
VCC3	EXP_RXN122	B17	VCC3_3
VCC3			



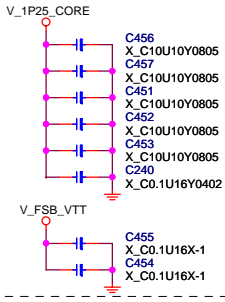
Place close to GMCH



MCH CORE DECOUPLING



5020 Parts



INTEL-LE82G31-A2-RH



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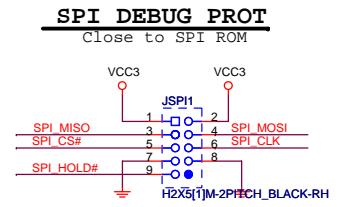
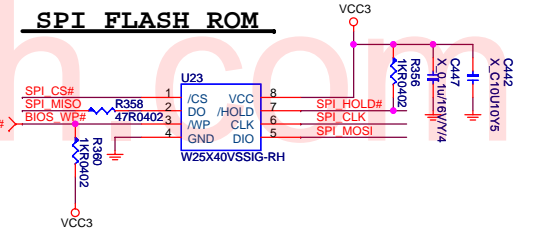
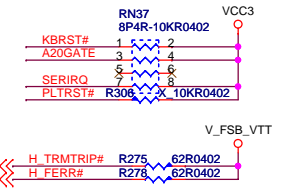
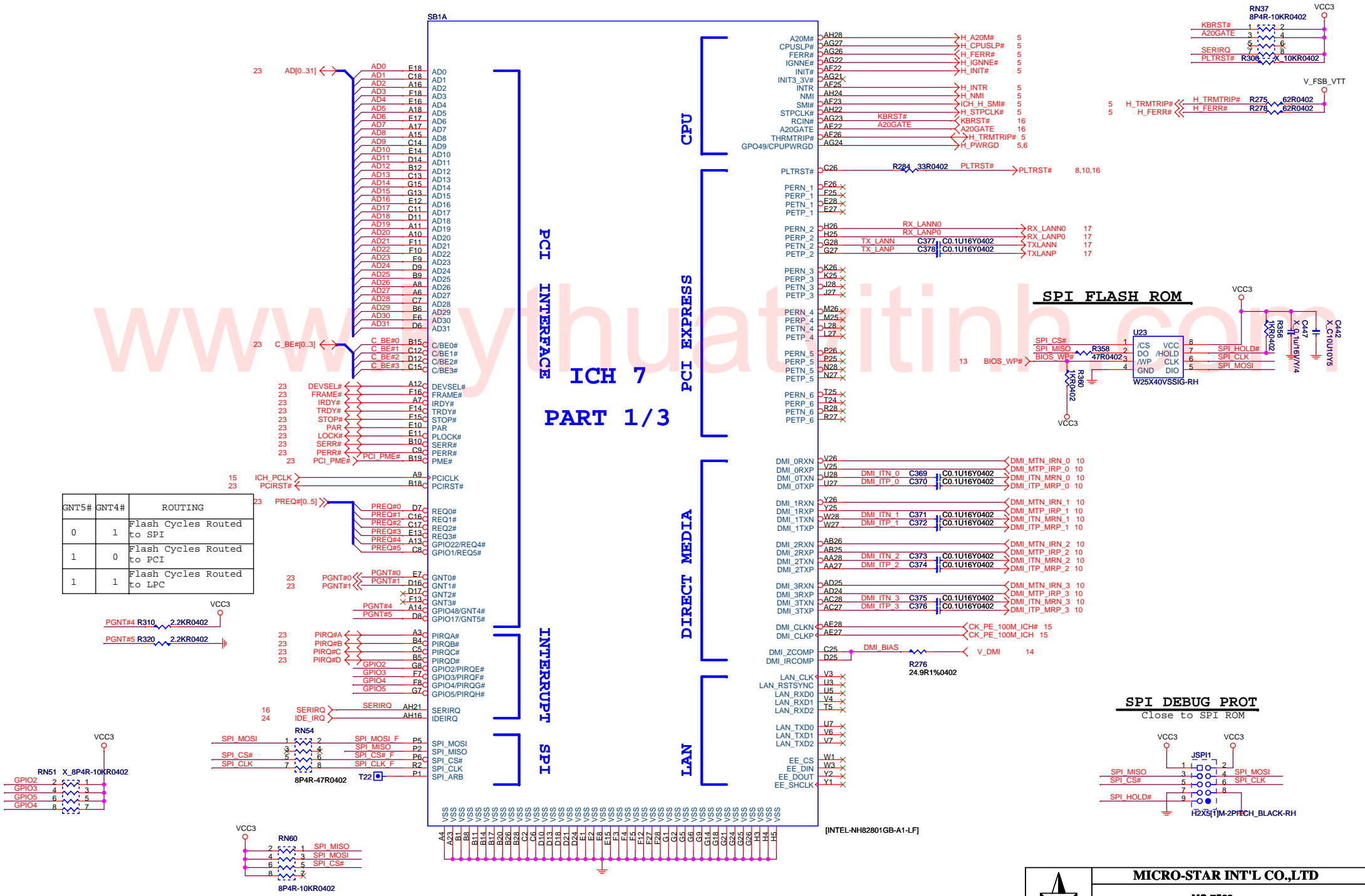
MS-7529

Size	Document Description	Rev
Custom	Intel.G31 - GND	1.1

Date: Friday, May 16, 2008 | Sheet 11 of 33

ICH 7 PART 1/3

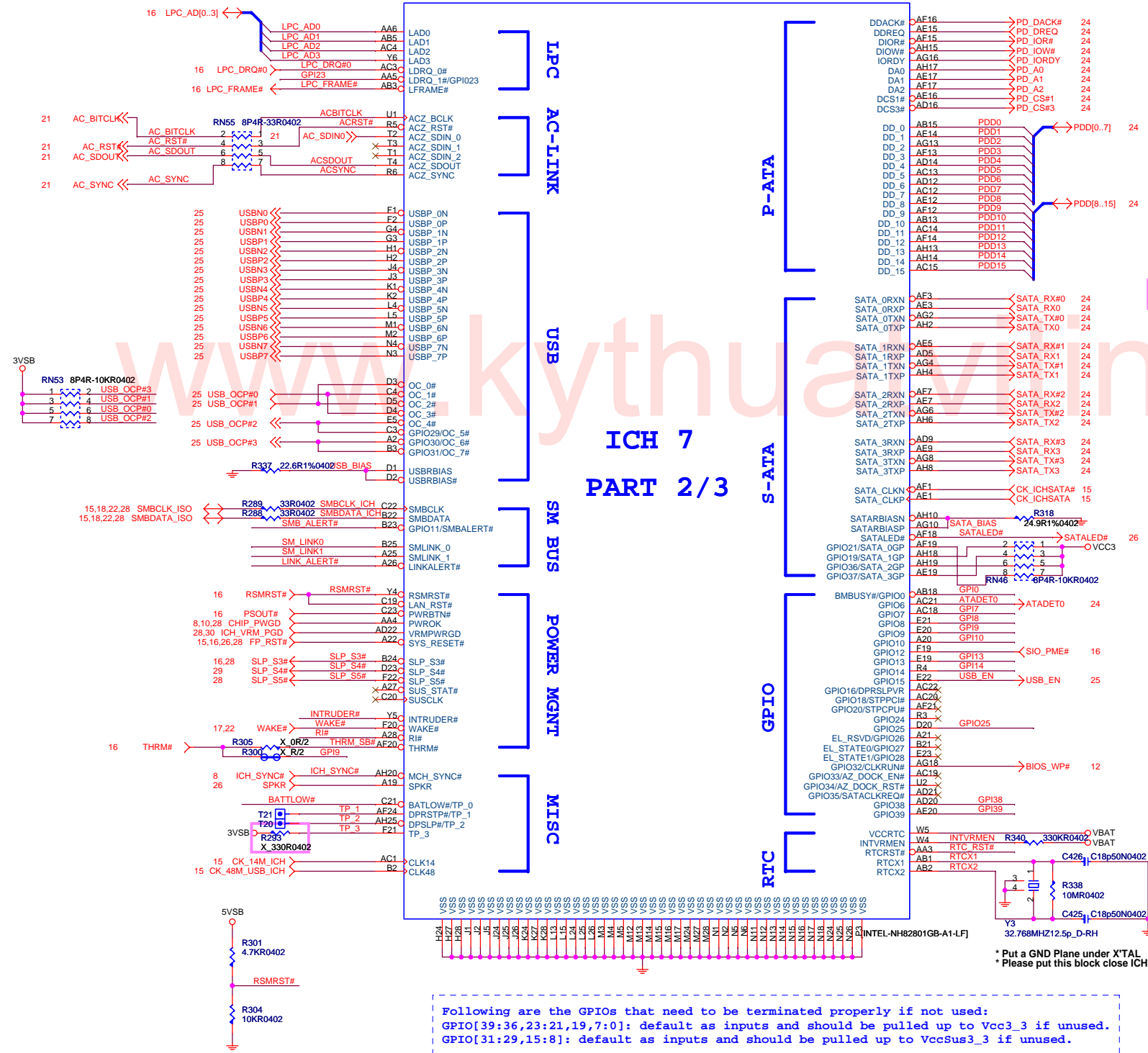
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0	1	Flash Cycles Routed to SPI
1	0	Flash Cycles Routed to PCI
1	1	Flash Cycles Routed to LPC



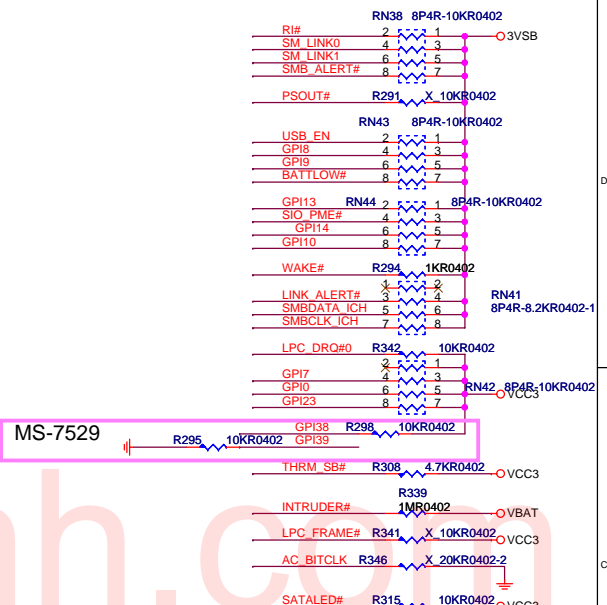
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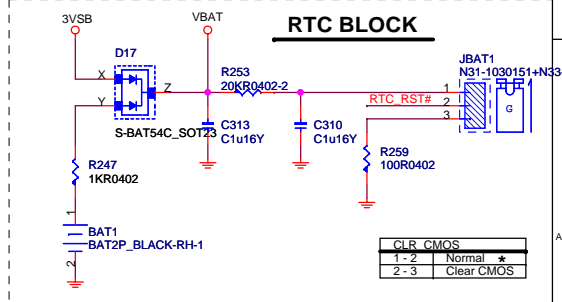
Size	Document Description	Rev
Custom	Intel ICH7 - PCI & DMI & CPU & IRQ	1.1
Date:	Tuesday, June 03, 2008	Sheet 12 of 33



**ICH 7
PART 2/3**



DESIGN NOTE:
GPIO 25 SELECT DMI MODE:
HI =DMI DC MODE (Internal pull-up)
LOW=DMI AC MODE



Following are the GPIOs that need to be terminated properly if not used:
GPIO[39:36,23:21,19,7:0]: default as inputs and should be pulled up to Vcc3_3 if unused.
GPIO[31:29,15:8]: default as inputs and should be pulled up to VccSus3_3 if unused.

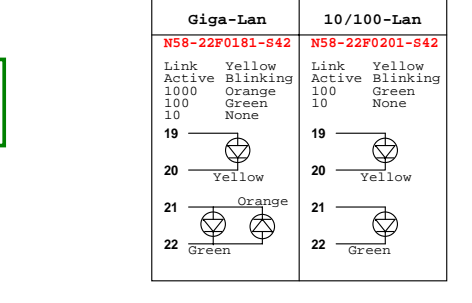
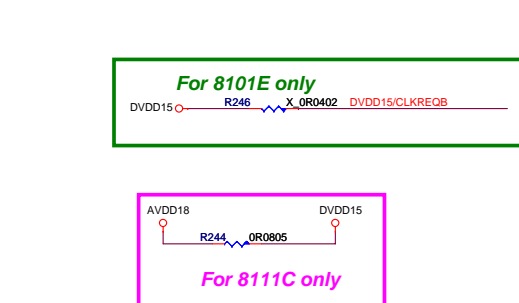
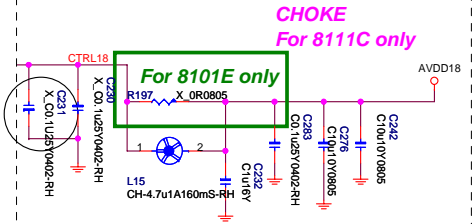
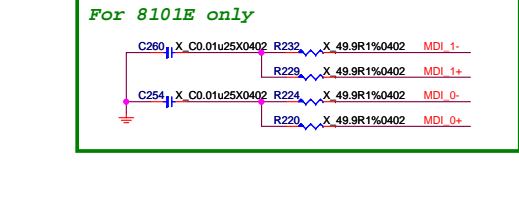
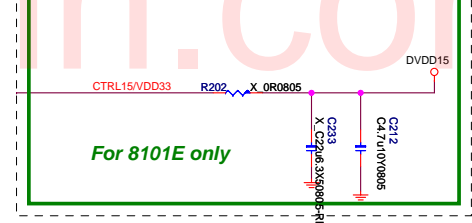
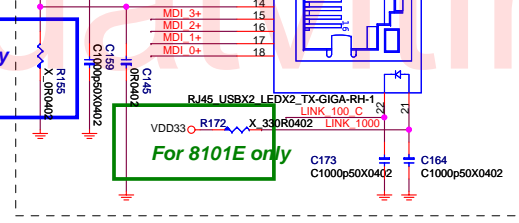
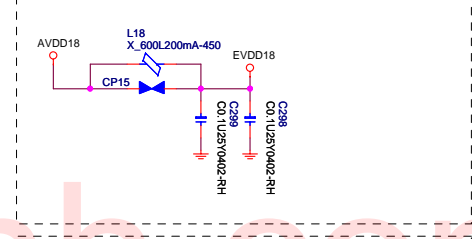
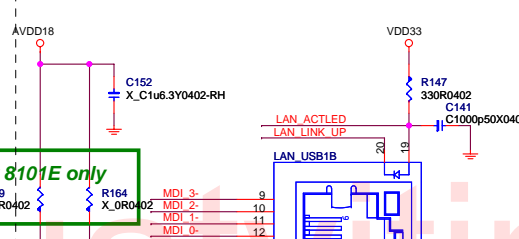
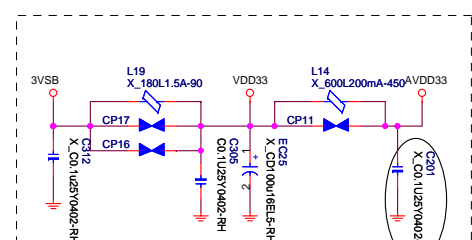
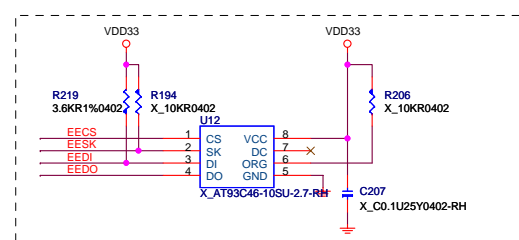
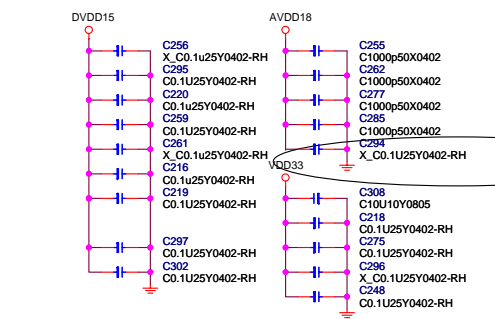
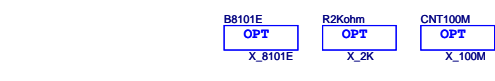
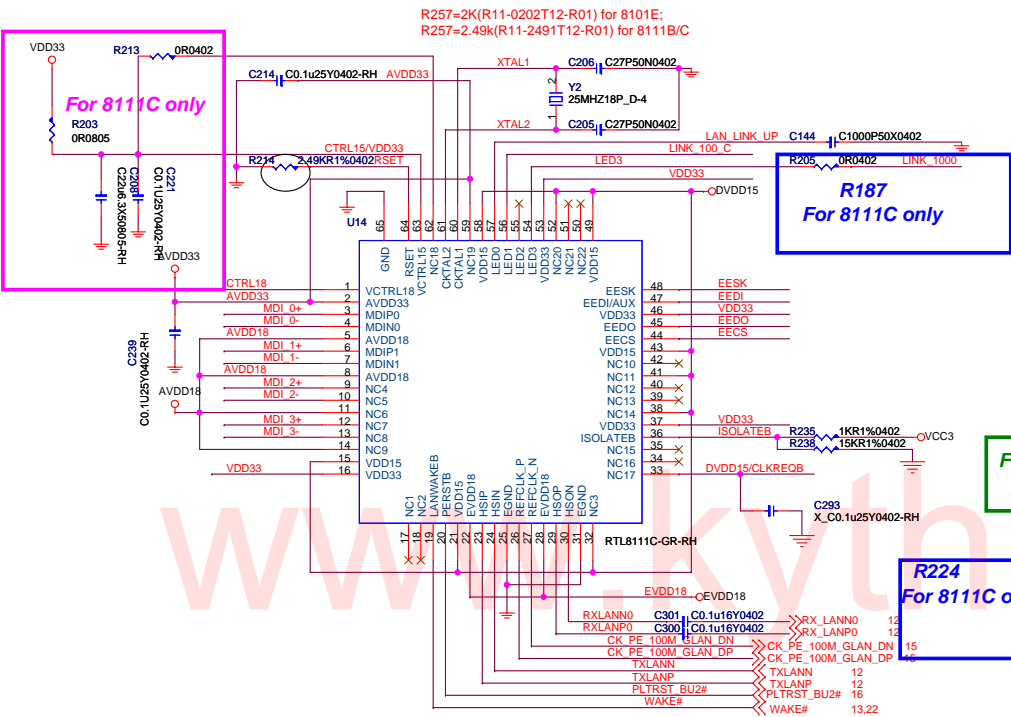
* Put a GND Plane under X'TAL
* Please put this block close ICH7

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Size: Custom | Document Description: Intel ICH7 - LPC & ATA & USB & GPIO | Rev: 1.1

Date: Wednesday, May 21, 2008 | Sheet: 13 of 33

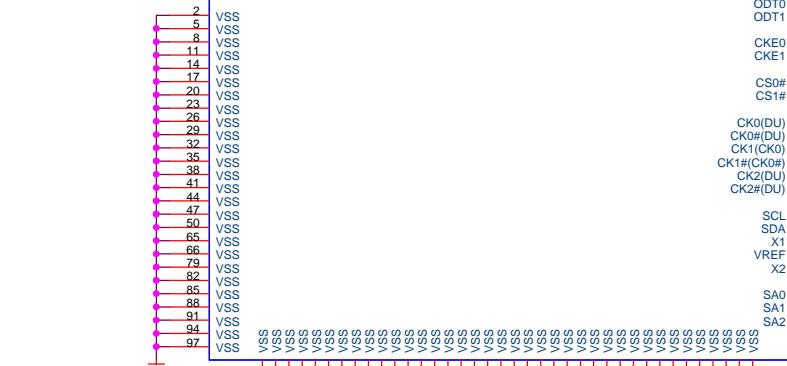


Giga-Lan		10/100-Lan	
N58-22F0181-S42		N58-22F0201-S42	
Link	Yellow	Link	Yellow
Active	Blinking	Active	Blinking
1000	Orange	100	Green
100	Green	10	None
10	None	10	None
19		19	
20	Yellow	20	Yellow
21	Orange	21	
22	Green	22	Green

MEM_MA_DATA[0..63] MEM_MA_DATA[0..63] VCC_DDR DDR2 DIMM A VCC3

MEM_MA_DATA0	3	DO0
MEM_MA_DATA1	4	DO1
MEM_MA_DATA2	5	DO2
MEM_MA_DATA3	9	DO3
MEM_MA_DATA4	122	DO4
MEM_MA_DATA5	123	DO5
MEM_MA_DATA6	128	DO6
MEM_MA_DATA7	129	DO7
MEM_MA_DATA8	12	DO8
MEM_MA_DATA9	13	DO9
MEM_MA_DATA10	21	DO10
MEM_MA_DATA11	22	DO11
MEM_MA_DATA12	141	DO12
MEM_MA_DATA13	132	DO13
MEM_MA_DATA14	140	DO14
MEM_MA_DATA15	141	DO15
MEM_MA_DATA16	24	DO16
MEM_MA_DATA17	25	DO17
MEM_MA_DATA18	30	DO18
MEM_MA_DATA19	31	DO19
MEM_MA_DATA20	143	DO20
MEM_MA_DATA21	144	DO21
MEM_MA_DATA22	149	DO22
MEM_MA_DATA23	150	DO23
MEM_MA_DATA24	33	DO24
MEM_MA_DATA25	34	DO25
MEM_MA_DATA26	39	DO26
MEM_MA_DATA27	40	DO27
MEM_MA_DATA28	152	DO28
MEM_MA_DATA29	153	DO29
MEM_MA_DATA30	158	DO30
MEM_MA_DATA31	159	DO31
MEM_MA_DATA32	80	DO32
MEM_MA_DATA33	81	DO33
MEM_MA_DATA34	86	DO34
MEM_MA_DATA35	87	DO35
MEM_MA_DATA36	199	DO36
MEM_MA_DATA37	200	DO37
MEM_MA_DATA38	205	DO38
MEM_MA_DATA39	206	DO39
MEM_MA_DATA40	89	DO40
MEM_MA_DATA41	90	DO41
MEM_MA_DATA42	95	DO42
MEM_MA_DATA43	96	DO43
MEM_MA_DATA44	208	DO44
MEM_MA_DATA45	209	DO45
MEM_MA_DATA46	214	DO46
MEM_MA_DATA47	215	DO47
MEM_MA_DATA48	98	DO48
MEM_MA_DATA49	99	DO49
MEM_MA_DATA50	107	DO50
MEM_MA_DATA51	108	DO51
MEM_MA_DATA52	217	DO52
MEM_MA_DATA53	218	DO53
MEM_MA_DATA54	228	DO54
MEM_MA_DATA55	227	DO55
MEM_MA_DATA56	110	DO56
MEM_MA_DATA57	111	DO57
MEM_MA_DATA58	116	DO58
MEM_MA_DATA59	117	DO59
MEM_MA_DATA60	229	DO60
MEM_MA_DATA61	230	DO61
MEM_MA_DATA62	235	DO62
MEM_MA_DATA63	236	DO63

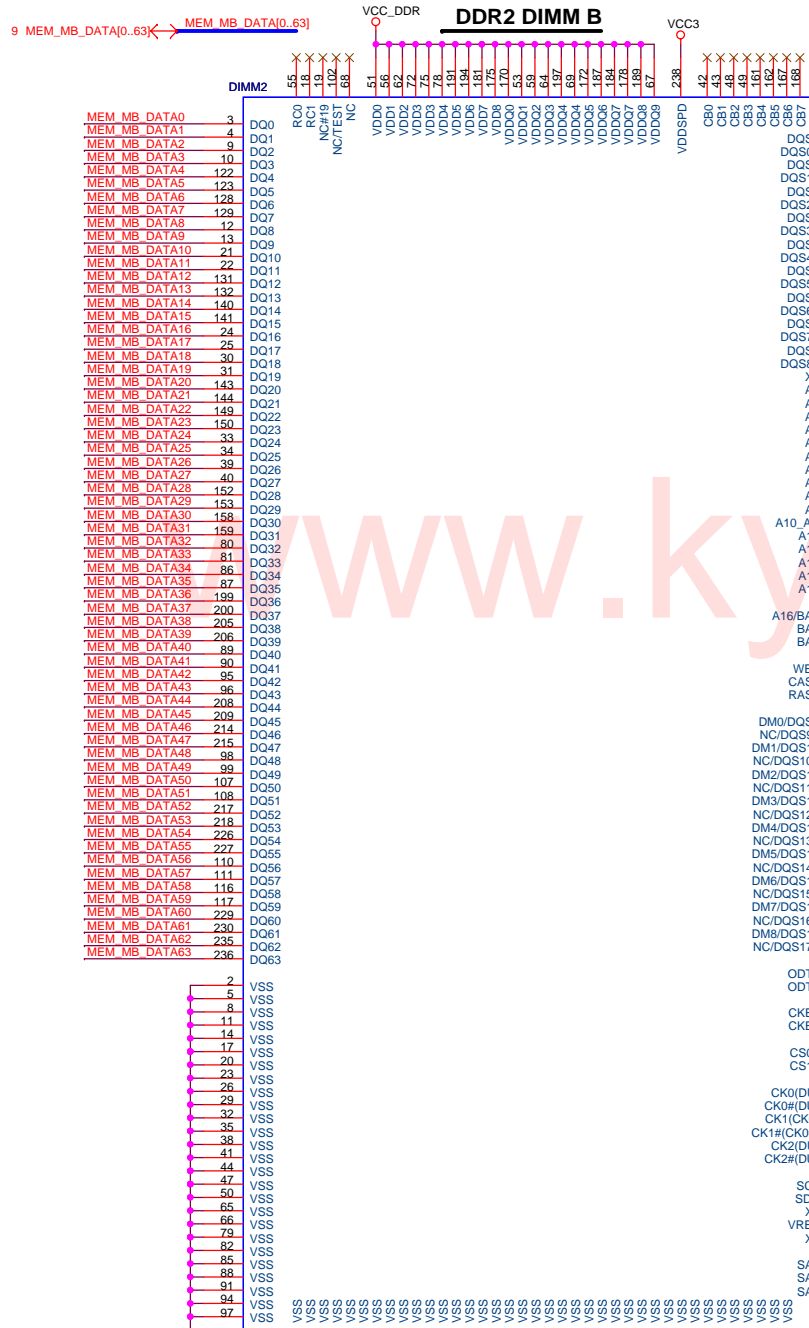
MEM_MA_DQS_H[0..7]	MEM_MA_DQS_H[0..7]
MEM_MA_DQS_L[0..7]	MEM_MA_DQS_L[0..7]
MEM_MA_ADD[0..14]	MEM_MA_ADD[0..14]
MEM_MA_BANK[0..2]	MEM_MA_BANK[0..2]
MEM_MA_WE_L	MEM_MA_WE_L 9,20
MEM_MA_CAS_L	MEM_MA_CAS_L 9,20
MEM_MA_RAS_L	MEM_MA_RAS_L 9,20
MEM_MA_DM[0..7]	MEM_MA_DM[0..7]
MEM_MA_ODT0	MEM_MA_ODT0 9,20
MEM_MA_ODT1	MEM_MA_ODT1 9,20
MEM_MA_CKE0	MEM_MA_CKE0 9,20
MEM_MA_CKE1	MEM_MA_CKE1 9,20
MEM_MA_CS_LO	MEM_MA_CS_LO 9,20
MEM_MA_CS_L1	MEM_MA_CS_L1 9,20
MEM_MA_CLK_H0	MEM_MA_CLK_H0 9
MEM_MA_CLK_L0	MEM_MA_CLK_L0 9
MEM_MA_CLK_H1	MEM_MA_CLK_H1 9
MEM_MA_CLK_L1	MEM_MA_CLK_L1 9
MEM_MA_CLK_H2	MEM_MA_CLK_H2 9
MEM_MA_CLK_L2	MEM_MA_CLK_L2 9
SMBCLK_DDR	SMBCLK_DDR 19
SMBDATA_DDR	SMBDATA_DDR 19
MEM_MA_ADD0	MEM_MA_ADD0
MEM_MA_ADD1	MEM_MA_ADD1
MEM_MA_ADD2	MEM_MA_ADD2
MEM_MA_ADD3	MEM_MA_ADD3
MEM_MA_ADD4	MEM_MA_ADD4
MEM_MA_ADD5	MEM_MA_ADD5
MEM_MA_ADD6	MEM_MA_ADD6
MEM_MA_ADD7	MEM_MA_ADD7
MEM_MA_ADD8	MEM_MA_ADD8
MEM_MA_ADD9	MEM_MA_ADD9
MEM_MA_ADD10	MEM_MA_ADD10
MEM_MA_ADD11	MEM_MA_ADD11
MEM_MA_ADD12	MEM_MA_ADD12
MEM_MA_ADD13	MEM_MA_ADD13
MEM_MA_ADD14	MEM_MA_ADD14
MEM_MA_BANK0	MEM_MA_BANK0
MEM_MA_BANK1	MEM_MA_BANK1
MEM_MA_BANK2	MEM_MA_BANK2
MEM_MA_DM0	MEM_MA_DM0
MEM_MA_DM1	MEM_MA_DM1
MEM_MA_DM2	MEM_MA_DM2
MEM_MA_DM3	MEM_MA_DM3
MEM_MA_DM4	MEM_MA_DM4
MEM_MA_DM5	MEM_MA_DM5
MEM_MA_DM6	MEM_MA_DM6
MEM_MA_DM7	MEM_MA_DM7
MEM_MA_CS_L0	MEM_MA_CS_L0
MEM_MA_CS_L1	MEM_MA_CS_L1
MEM_MA_CLK_H0	MEM_MA_CLK_H0
MEM_MA_CLK_L0	MEM_MA_CLK_L0
MEM_MA_CLK_H1	MEM_MA_CLK_H1
MEM_MA_CLK_L1	MEM_MA_CLK_L1
MEM_MA_CLK_H2	MEM_MA_CLK_H2
MEM_MA_CLK_L2	MEM_MA_CLK_L2
SMBCLK_DDR	SMBCLK_DDR
SMBDATA_DDR	SMBDATA_DDR



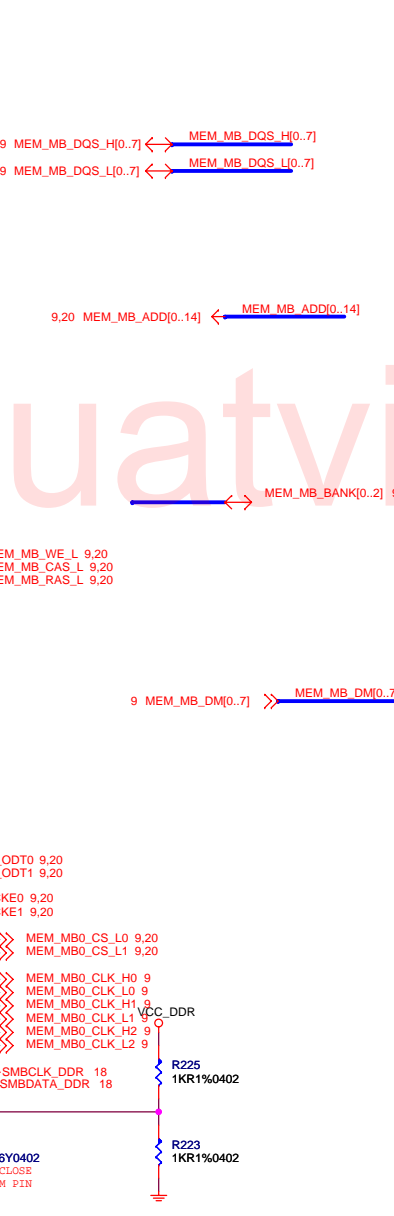
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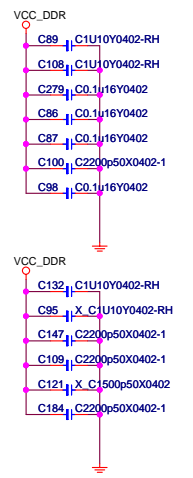
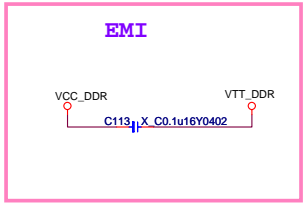
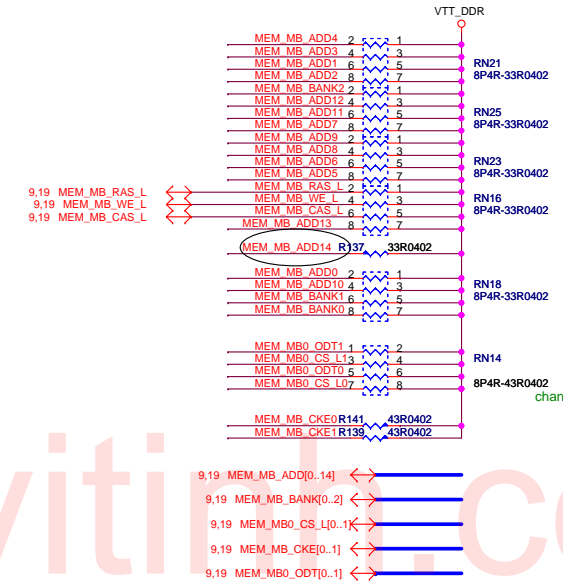
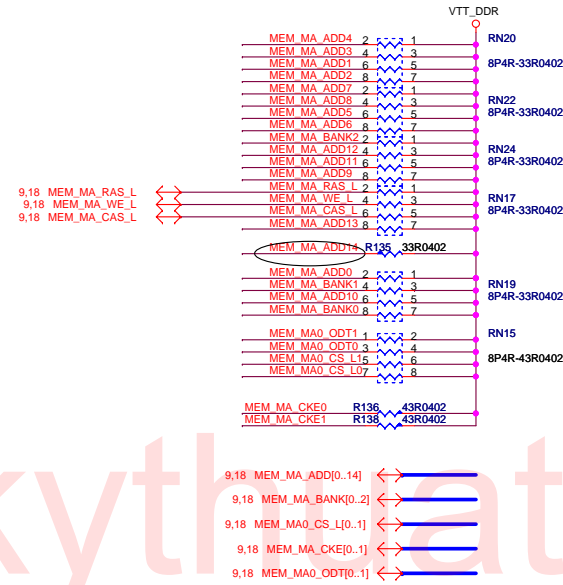
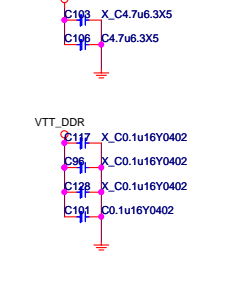
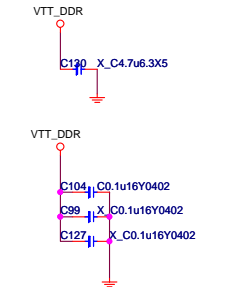
19 SMBCLK_DDR <-> SMBCLK_DDR R74 <-> 22R0402 <-> SMBCLK_ISO 13,15,22,28
 19 SMBDATA_DDR <-> SMBDATA_DDR R82 <-> 22R0402 <-> SMBDATA_ISO 13,15,22,28



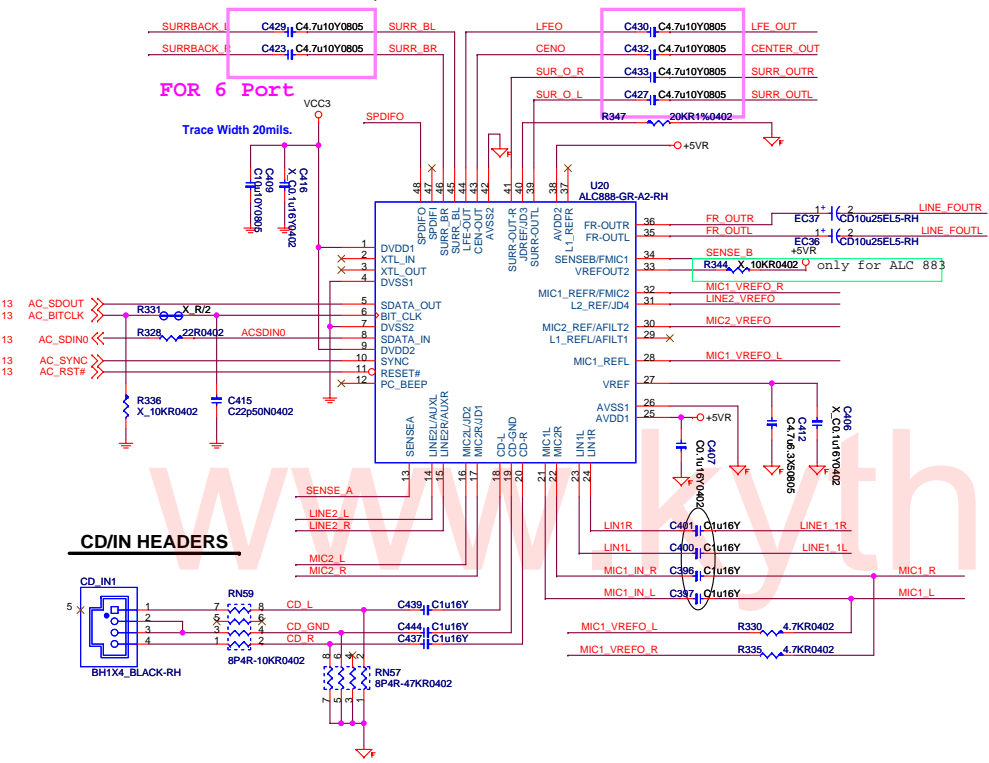


MEM_MB_DATA0	3	DO0	7	MEM_MB_DQS_H0
MEM_MB_DATA1	4	DO1	6	MEM_MB_DQS_L0
MEM_MB_DATA2	9	DO2	16	MEM_MB_DQS_H1
MEM_MB_DATA3	10	DO3	15	MEM_MB_DQS_L1
MEM_MB_DATA4	122	DO4	28	MEM_MB_DQS_H2
MEM_MB_DATA5	123	DO5	27	MEM_MB_DQS_L2
MEM_MB_DATA6	128	DO6	37	MEM_MB_DQS_H3
MEM_MB_DATA7	129	DO7	36	MEM_MB_DQS_L3
MEM_MB_DATA8	12	DO8	84	MEM_MB_DQS_H4
MEM_MB_DATA9	13	DO9	83	MEM_MB_DQS_L4
MEM_MB_DATA10	21	DO10	93	MEM_MB_DQS_H5
MEM_MB_DATA11	22	DO11	92	MEM_MB_DQS_L5
MEM_MB_DATA12	131	DO12	105	MEM_MB_DQS_H6
MEM_MB_DATA13	132	DO13	104	MEM_MB_DQS_L6
MEM_MB_DATA14	140	DO14	114	MEM_MB_DQS_H7
MEM_MB_DATA15	141	DO15	113	MEM_MB_DQS_L7
MEM_MB_DATA16	24	DO16	46	
MEM_MB_DATA17	25	DO17	45	
MEM_MB_DATA18	30	DO18	X3	
MEM_MB_DATA19	31	DO19	X3	
MEM_MB_DATA20	143	DO20	188	MEM_MB_ADD0
MEM_MB_DATA21	144	DO21	183	MEM_MB_ADD1
MEM_MB_DATA22	149	DO22	63	MEM_MB_ADD2
MEM_MB_DATA23	150	DO23	182	MEM_MB_ADD3
MEM_MB_DATA24	33	DO24	A3	MEM_MB_ADD4
MEM_MB_DATA25	34	DO25	A4	MEM_MB_ADD5
MEM_MB_DATA26	39	DO26	A5	MEM_MB_ADD6
MEM_MB_DATA27	40	DO27	A6	MEM_MB_ADD7
MEM_MB_DATA28	152	DO28	A7	MEM_MB_ADD8
MEM_MB_DATA29	153	DO29	A8	MEM_MB_ADD9
MEM_MB_DATA30	158	DO30	A9	MEM_MB_ADD10
MEM_MB_DATA31	159	DO31	A10	MEM_MB_ADD11
MEM_MB_DATA32	80	DO32	A11	MEM_MB_ADD12
MEM_MB_DATA33	81	DO33	A12	MEM_MB_ADD13
MEM_MB_DATA34	86	DO34	A13	MEM_MB_ADD14
MEM_MB_DATA35	87	DO35	A14	MEM_MB_ADD14
MEM_MB_DATA36	199	DO36	A15	MEM_MB_ADD14
MEM_MB_DATA37	200	DO37	54	MEM_MB_BANK2
MEM_MB_DATA38	205	DO38	190	MEM_MB_BANK1
MEM_MB_DATA39	206	DO39	71	MEM_MB_BANK0
MEM_MB_DATA40	89	DO40		
MEM_MB_DATA41	90	DO41	WE#	MEM_MB_WE_L 9,20
MEM_MB_DATA42	95	DO42	CAS#	MEM_MB_CAS_L 9,20
MEM_MB_DATA43	96	DO43	RAS#	MEM_MB_RAS_L 9,20
MEM_MB_DATA44	208	DO44		
MEM_MB_DATA45	209	DO45	125	MEM_MB_DM0
MEM_MB_DATA46	214	DO46	126	
MEM_MB_DATA47	215	DO47	134	MEM_MB_DM1
MEM_MB_DATA48	98	DO48	135	
MEM_MB_DATA49	99	DO49	146	MEM_MB_DM2
MEM_MB_DATA50	107	DO50	147	
MEM_MB_DATA51	108	DO51	155	MEM_MB_DM3
MEM_MB_DATA52	217	DO52	156	
MEM_MB_DATA53	218	DO53	202	MEM_MB_DM4
MEM_MB_DATA54	226	DO54	203	
MEM_MB_DATA55	227	DO55	211	MEM_MB_DM5
MEM_MB_DATA56	110	DO56	212	
MEM_MB_DATA57	111	DO57	223	MEM_MB_DM6
MEM_MB_DATA58	116	DO58	224	
MEM_MB_DATA59	117	DO59	232	MEM_MB_DM7
MEM_MB_DATA60	229	DO60	233	
MEM_MB_DATA61	230	DO61	164	
MEM_MB_DATA62	235	DO62	165	
MEM_MB_DATA63	236	DO63		
		ODT0	195	MEM_MB_ODT0 9,20
		ODT1	77	MEM_MB_ODT1 9,20
		CKE0	52	MEM_MB_CKE0 9,20
		CKE1	171	MEM_MB_CKE1 9,20
		CS0#	193	MEM_MB_CS_L0 9,20
		CS1#	76	MEM_MB_CS_L1 9,20
		CK0(DU)	185	MEM_MB_CLK_H0 9
		CK0#(DU)	186	MEM_MB_CLK_L0 9
		CK1(CK0)	137	MEM_MB_CLK_H1 9
		CK1#(CK0#)	138	MEM_MB_CLK_L1 9
		CK2(DU)	220	MEM_MB_CLK_H2 9
		CK2#(DU)	221	MEM_MB_CLK_L2 9
		SCL	120	SMBCLK_DDR 18
		SDA	119	SMBDATA_DDR 18
		X1	1	
		VREF	X2	
		SA0	239	VCC3
		SA1	240	C234 CO.1u16Y0402
		SA2	101	PLACE CLOSE TO DIMM PIN
				SPD Add. = A4

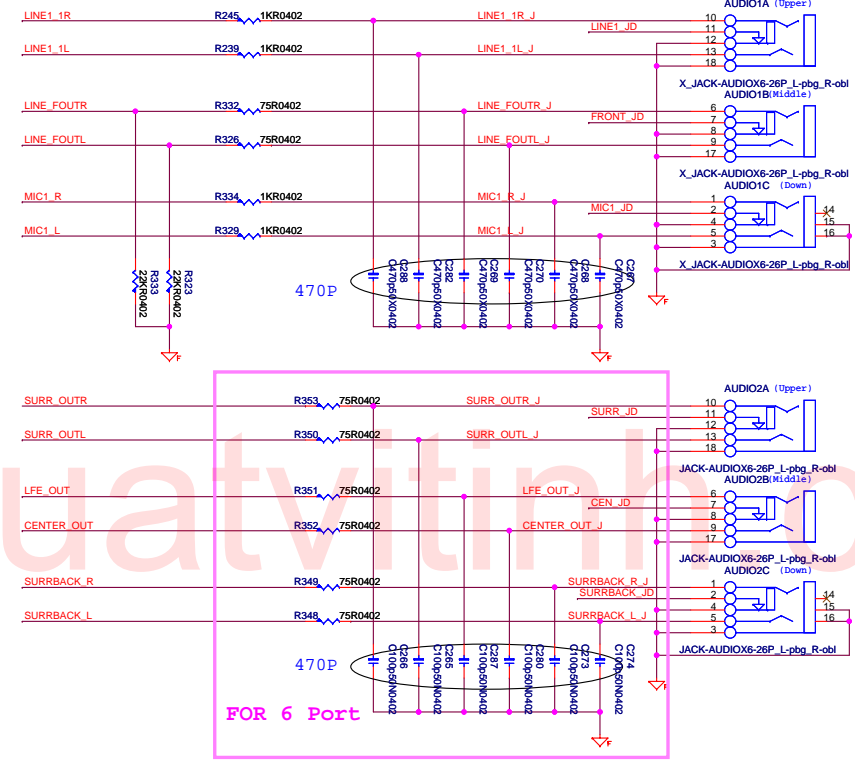




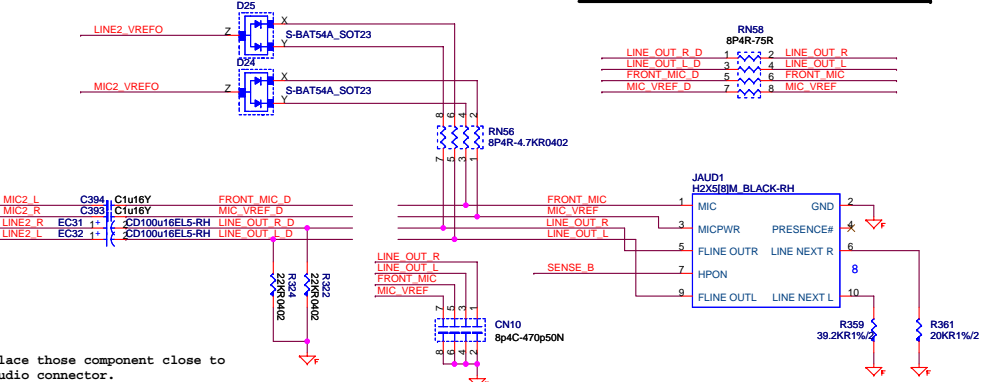
ALC888 CODEC



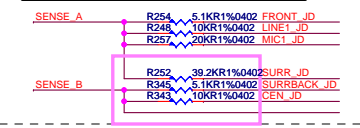
ALC888 JACK



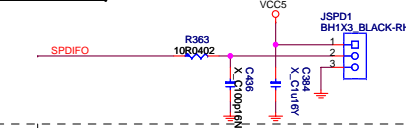
Azalia Front Audio Connector



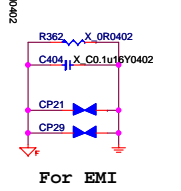
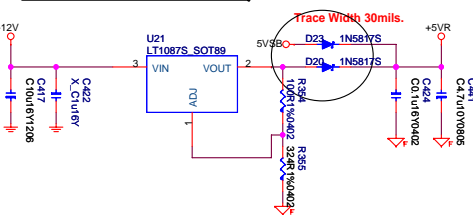
ALC883 JACK DETECT



SPDIF OUT

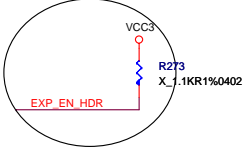
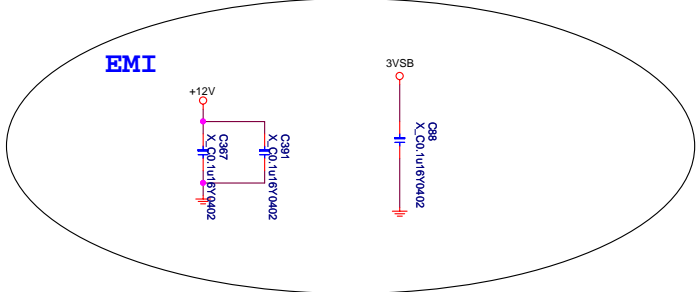
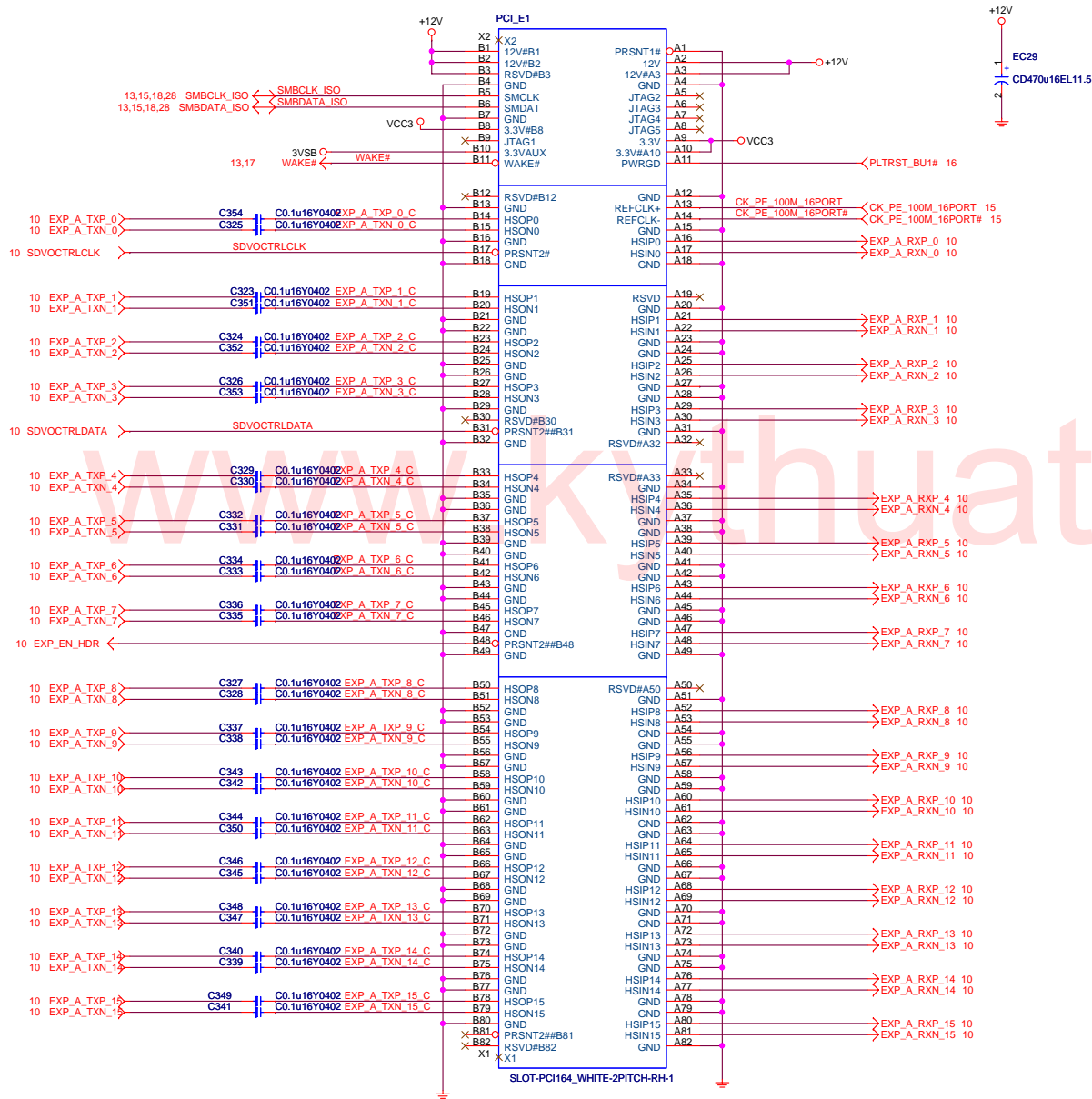


AUDIO CODE REGULATORS FOR 6 Port



Place those component close to audio connector.

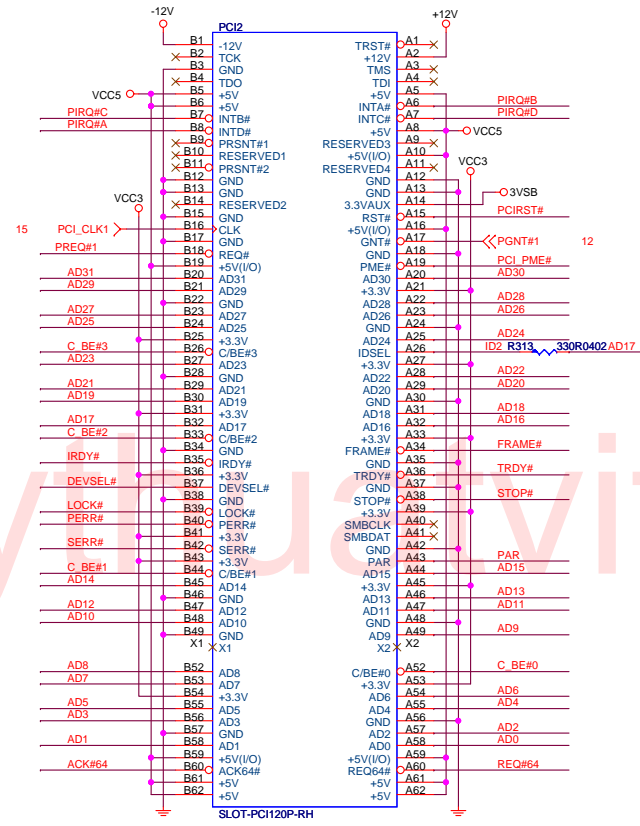
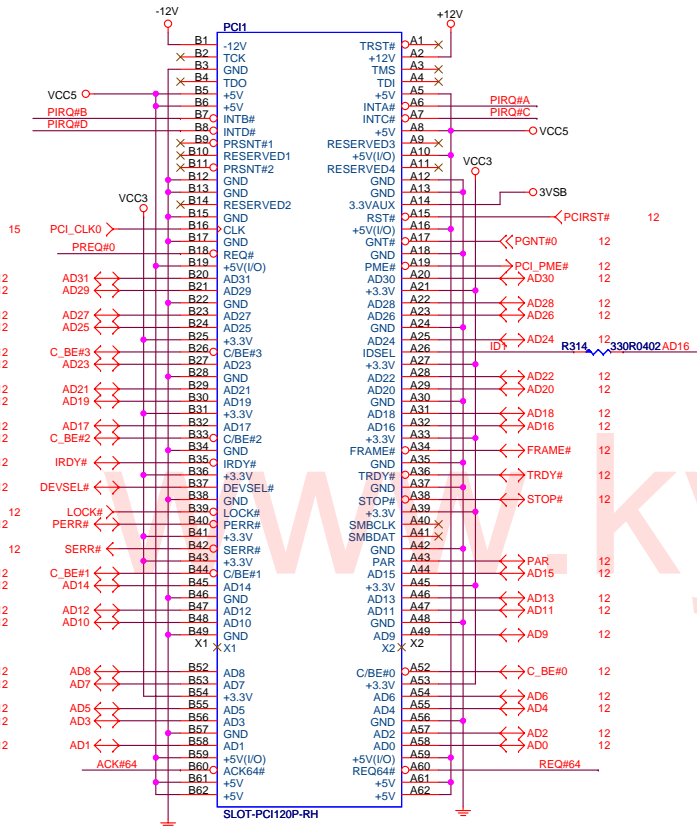
PCI EXPRESS X16 PORT



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PCI SLOT 1 (PCI VER: 2.2 COMPLY)

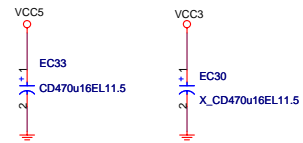
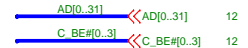
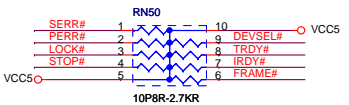
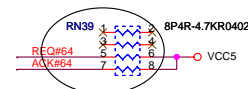
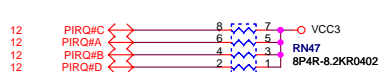
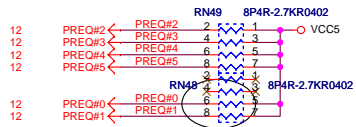
PCI SLOT 2 (PCI VER: 2.2 COMPLY)



**IDSEL = AD16
MASTER = PREQ#0
PIRQ#A**

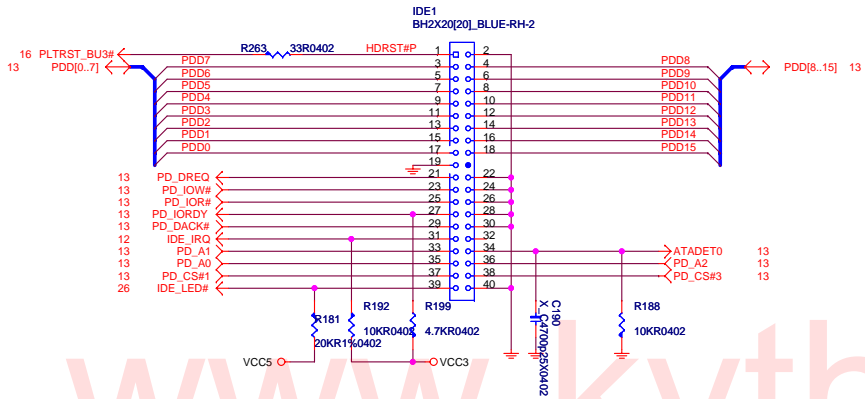
**IDSEL = AD17
MASTER = PREQ#1
PIRQ#B**

PCI PULL-UP / DOWN RESISTORS

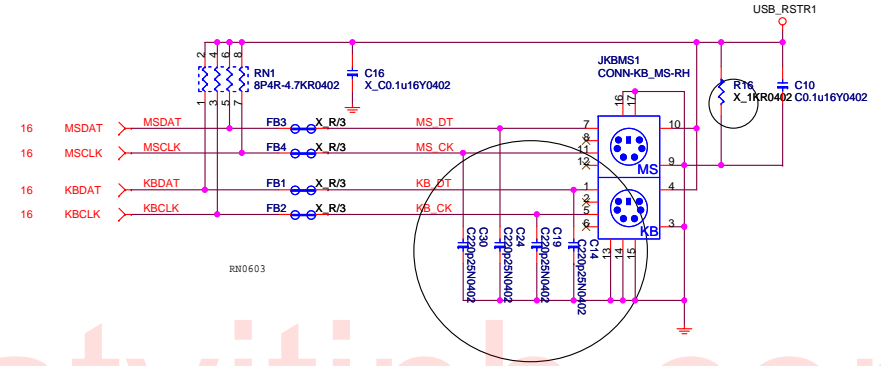


MICRO-STAR INT'L CO.,LTD		
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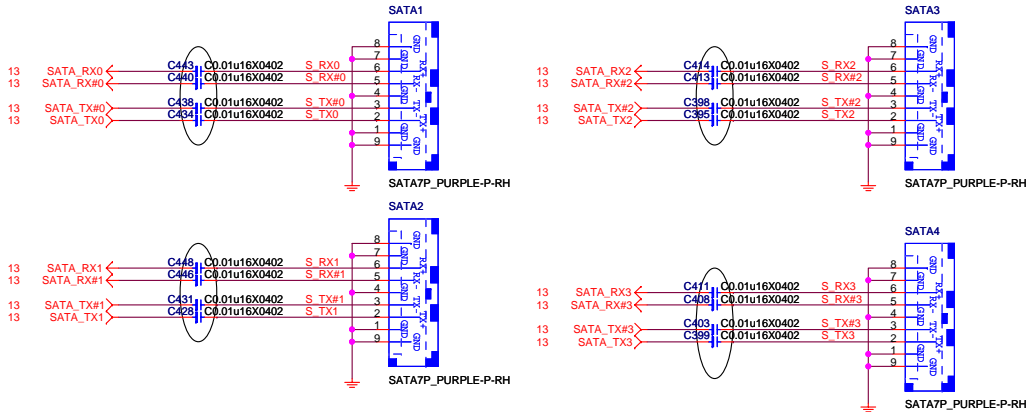
ATA 33/66/100 IDE Connectors



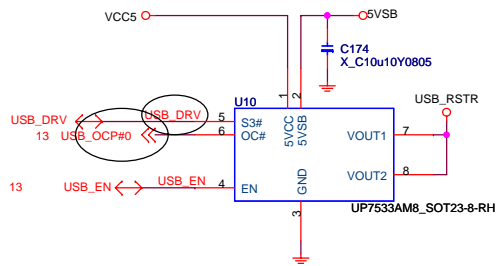
PS2 KEYBOARD & MOUSE CONNECTOR



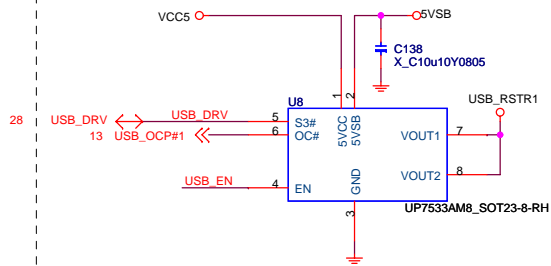
SERIAL ATA CONNECTOR BLOCK



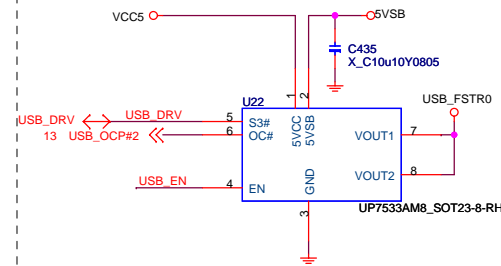
POWER CIRCUIT FOR USB PORT 0,1



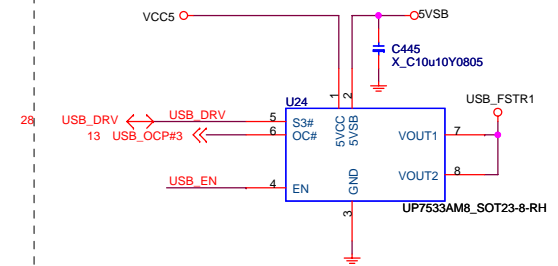
POWER CIRCUIT FOR USB PORT 2,3



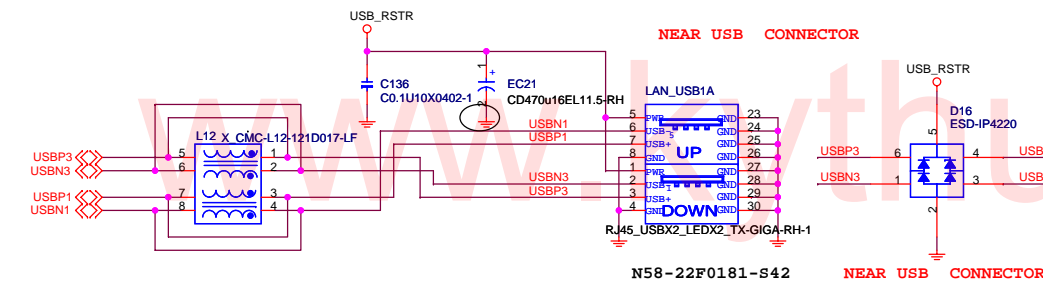
POWER CIRCUIT FOR USB PORT 4,5



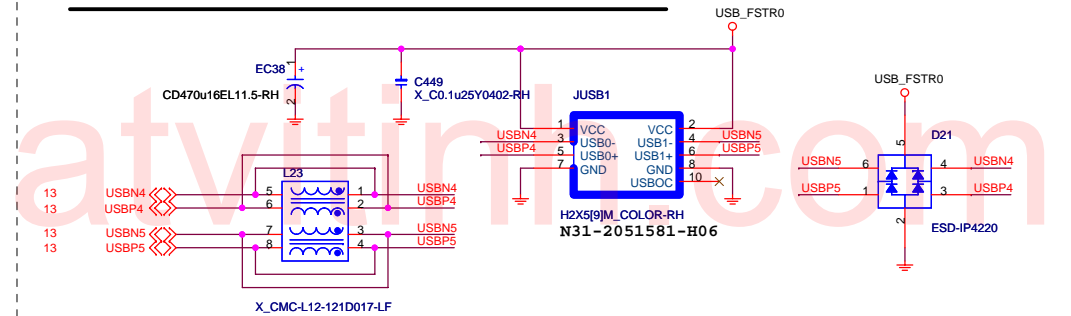
POWER CIRCUIT FOR USB PORT 6,7



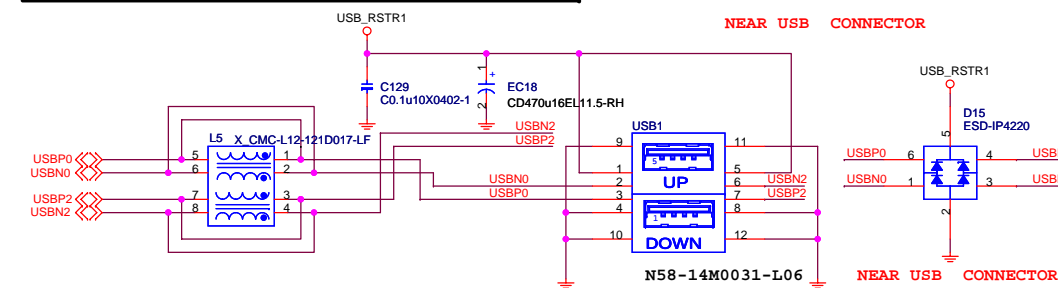
REAR PANEL USB CONNECTOR FOR USB PORT 0,1



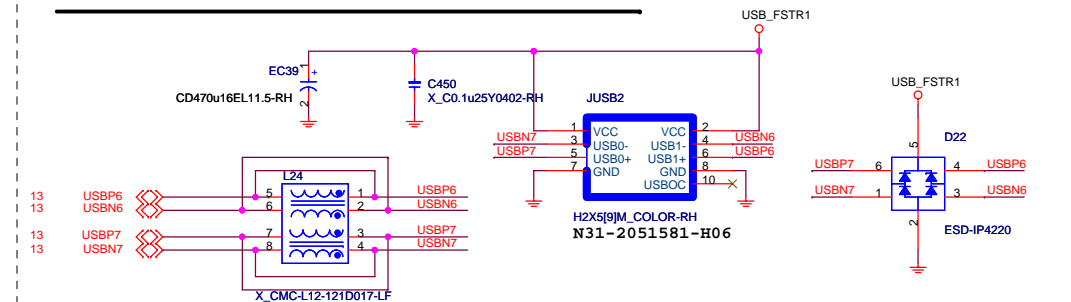
FRONT PANEL USB CONNECTOR FOR USB PORT 4,5



REAR PANEL USB CONNECTOR FOR USB PORT 2,3



FRONT PANEL USB CONNECTOR FOR USB PORT 6,7

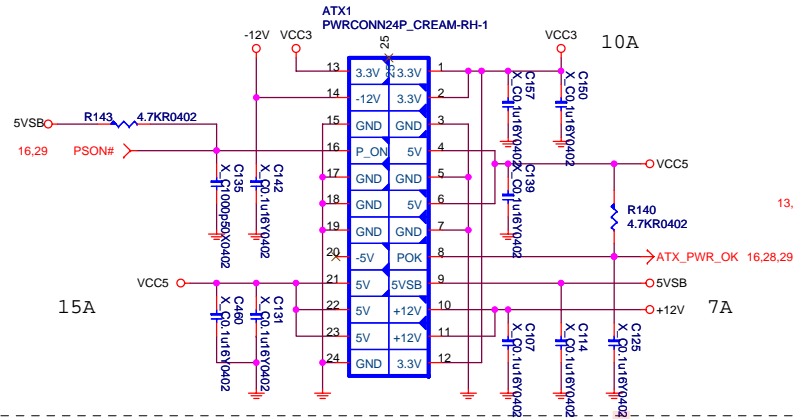


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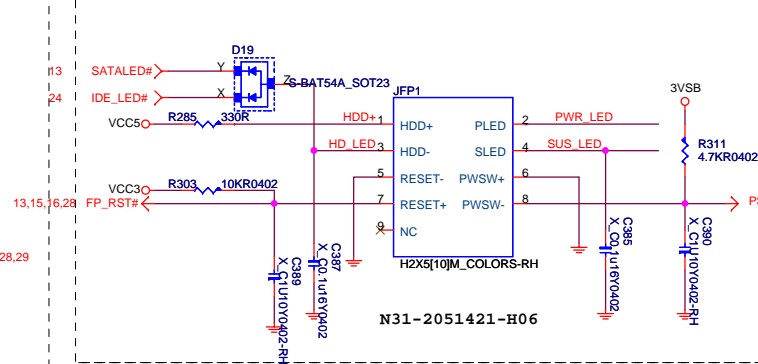
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Custom	USB CONNECTORS	1.1
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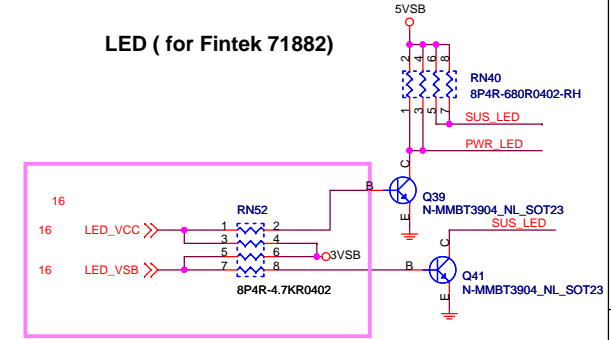
ATX Connector



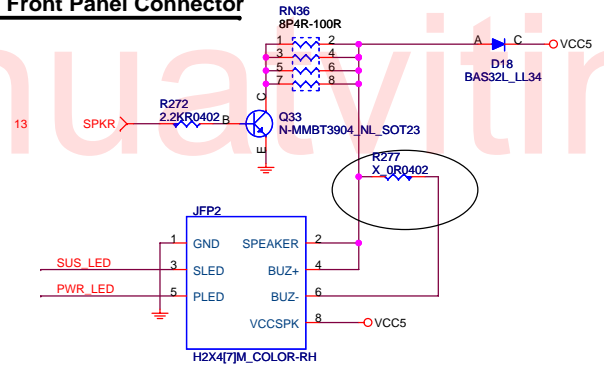
INTEL/PB Front Panel Connector



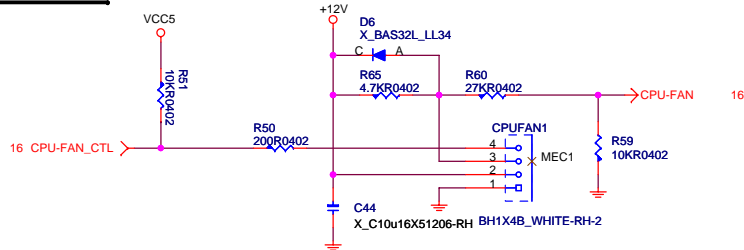
LED (for Fintek 71882)



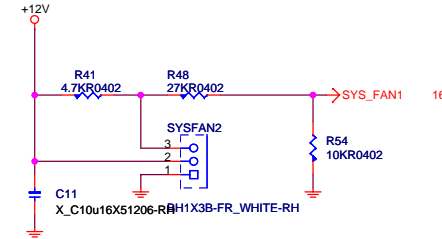
MSI Front Panel Connector



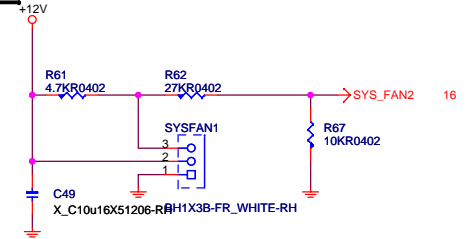
CPU FAN



SYSTEM FAN



PWR FAN

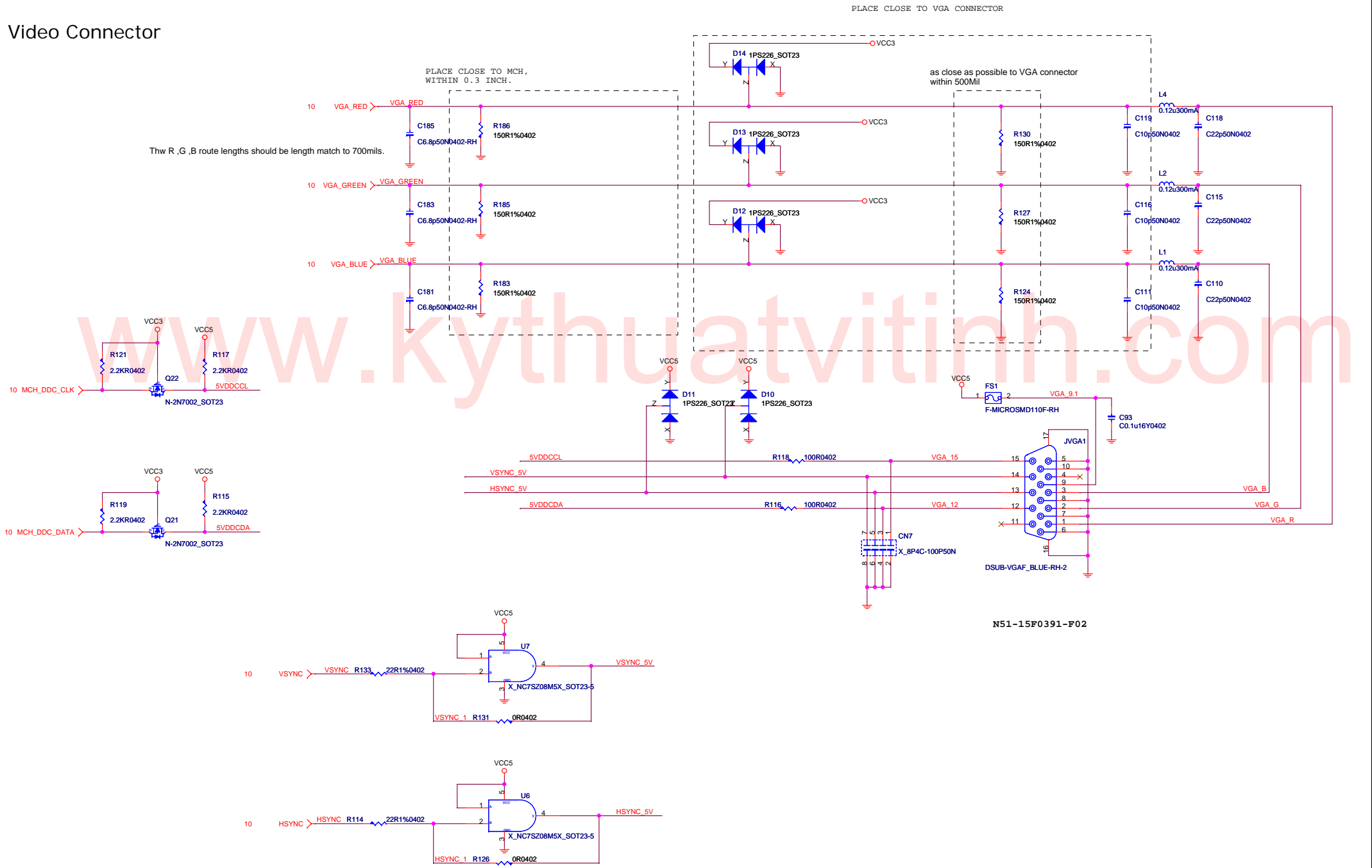


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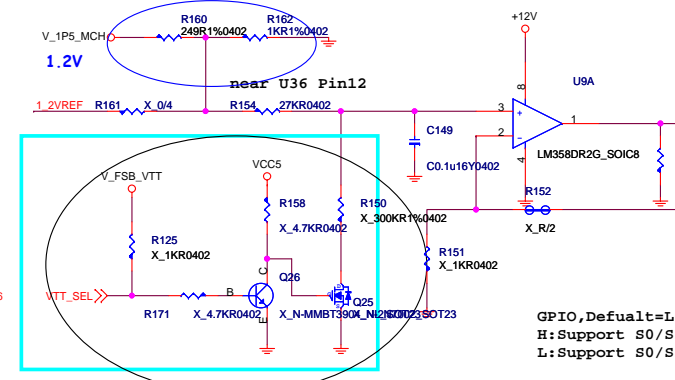
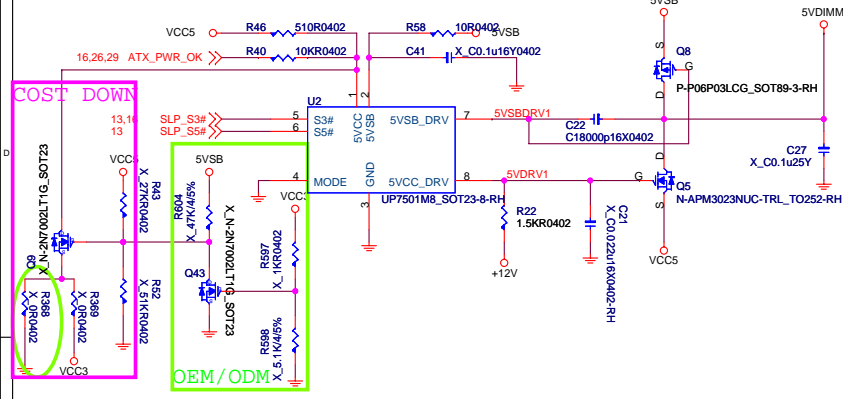
MS-7529

Size	Document Description	Rev
Custom	ATX & Front Panel & FAN	1.1
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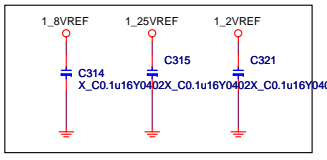
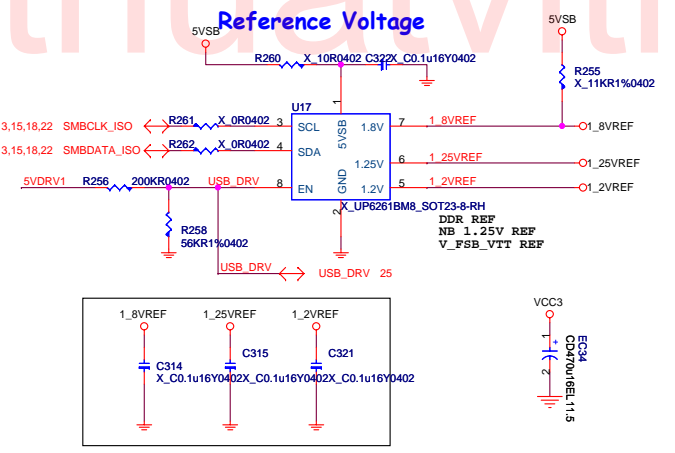
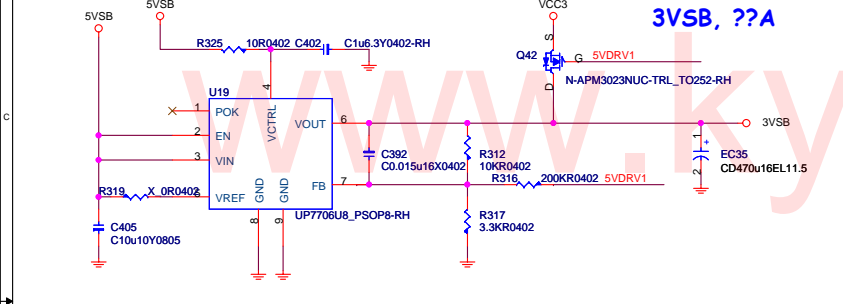
Video Connector



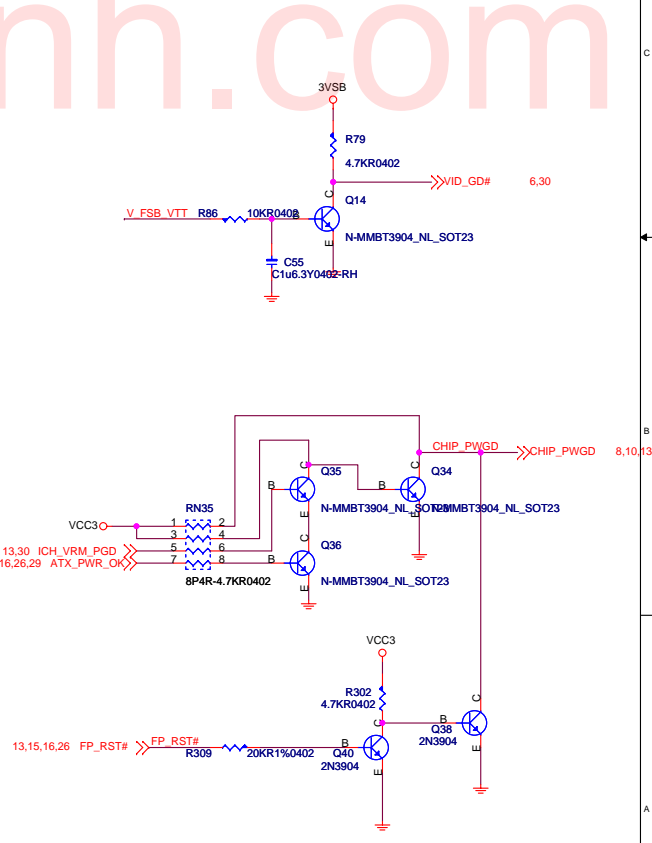
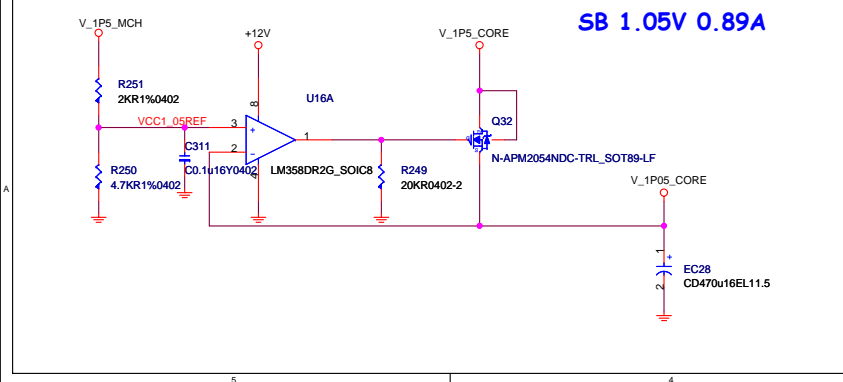
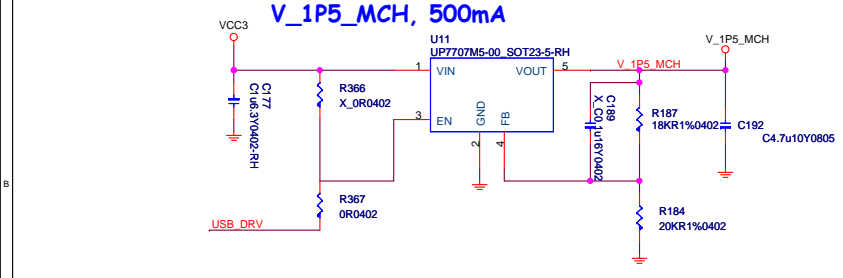
5VDIMM FOR DDR



VTT_SEL = L	V_FSB_VTT=1.1V	For future KENTSFIELD processor. (FSB1333, Quad-Core)
VTT_SEL = H	V_FSB_VTT=1.2V	For normal processors.



PLACE NEAR PIN OUT

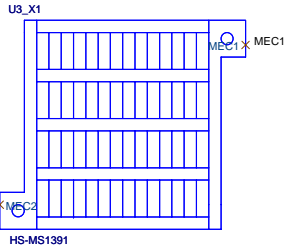


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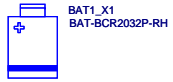
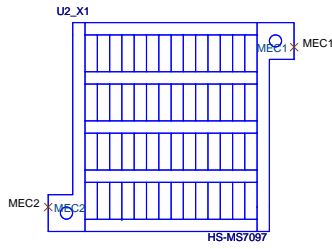
MS-7529

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ICH7 HEATSINK

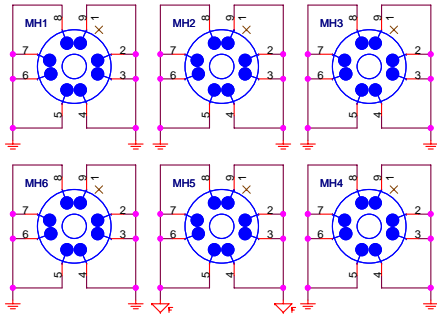


MCH HEATSINK

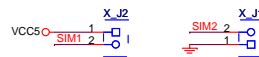


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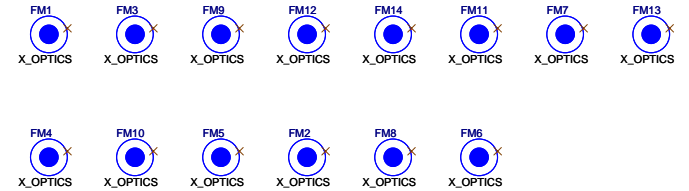
Mounting Holes



Simulation



Optics Orientation Holes



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ICH7									
GPIO	Alt Func	PIN	I/O/NC	POWER	PU	SMI	TOL	DEFAULT	SIGNAL NAME
GPIO0	Unmultiplexed	AB18	I/O	CORE	N	Y	3.3V	GPI	GPIO(pull high)
GPIO1	REQ5#	C8	I/O	CORE	N	Y	5V	GPI	PREQ#5
GPIO2	PIRQE#	G8	I/OD	CORE	N	Y	5V	GPI	GPIO2(pull high)
GPIO3	PIRQF#	F7	I/OD	CORE	N	Y	5V	GPI	GPIO3(pull high)
GPIO4	PIRQG#	F8	I/OD	CORE	N	Y	5V	GPI	GPIO4(pull high)
GPIO5	PIRQH#	G7	I/OD	CORE	N	Y	5V	GPI	GPIO5(pull high)
GPIO6	Unmultiplexed	AC21	I/O	CORE	N	Y	3.3V	GPI	ATADET0
GPIO7	Unmultiplexed	AC18	I/O	CORE	N	Y	3.3V	GPI	STRAPPED HI
GPIO8	Unmultiplexed	E21	I/O	Resume	N	Y	3.3V	GPI	STRAPPED HI
GPIO9	Unmultiplexed	E20	I/O	Resume	N	Y	3.3V	GPI	STRAPPED HI
GPIO10	Unmultiplexed	A20	I/O	Resume	N	Y	3.3V	GPI	STRAPPED HI
GPIO11	SMBALERT#	B23	I/O	Resume	N	Y	3.3V	Native	STRAPPED HI
GPIO12	Unmultiplexed	F19	I/O	Resume	N	Y	3.3V	GPI	SIO_PME#
GPIO13	Unmultiplexed	E19	I/O	Resume	N	Y	3.3V	GPI	STRAPPED HI
GPIO14	Unmultiplexed	R4	I/O	Resume	N	Y	3.3V	GPI	STRAPPED HI
GPIO15	Unmultiplexed	E22	I/O	Resume	N	Y	3.3V	GPI	STRAPPED HI
GPIO16	Unmultiplexed	AC22	I/O	CORE	N	N	3.3V	GPO	NC
GPIO17	GNT5#	D8	I/O	CORE	N	N	3.3V	GPO	STRAPPED L
GPIO18	Unmultiplexed	AC20	I/O	CORE	N	N	3.3V	GPO	NC
GPIO19	SATA_1GP	AH18	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO20	Unmultiplexed	AF21	I/O	CORE	N	N	3.3V	GPO	NC
GPIO21	SATA_0GP	AF19	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO22	REQ4#	A13	I/O	CORE	N	N	3.3V	Native	STRAPPED HI
GPIO23	LDRQ_1#	AA5	I/O	CORE	N	N	3.3V	Native	STRAPPED HI
GPIO24	Unmultiplexed	R3	I/O	Resume	N	N	3.3V	GPO	NC
GPIO25	Unmultiplexed	D20	I/O	Resume	Y	N	3.3V	GPO	GPIO25(high 7507,low 7398)
GPIO26	Unmultiplexed	A21	I/O	Resume	N	N	3.3V	GPO	USB_EN
GPIO27	Unmultiplexed	B21	I/O	Resume	N	N	3.3V	GPO	NC
GPIO28	Unmultiplexed	E23	I/O	Resume	N	N	3.3V	GPO	NC
GPIO29	OC5#	C3	I/O	Resume	N	N	3.3V	GPI	USB_OCP#2
GPIO30	OC6#	A2	I/O	Resume	N	N	3.3V	GPI	USB_OCP#3
GPIO31	OC7#	B3	I/O	Resume	N	N	3.3V	GPI	USB_OCP#3
GPIO32	Unmultiplexed	AG18	I/O	CORE	N	N	3.3V	GPO	BIOS_WP#(fill with 1)
GPIO33	Unmultiplexed	AC19	I/O	CORE	N	N	3.3V	GPO	NC
GPIO34	Unmultiplexed	U2	I/O	CORE	N	N	3.3V	GPO	NC
GPIO35	SATACLKREQ#	AD21	I/O	CORE	N	N	3.3V	GPO	NC
GPIO36	SATA2GP	AH19	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO37	SATA3GP	AE19	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO38	Unmultiplexed	AD20	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO39	Unmultiplexed	AE20	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO48	GNT4#	A14	I/O	CORE	N	N	3.3V	Native	STRAPPED HI
GPIO49	CPUPWRGD	AG24	I/O	V_CPU_IO	N	N	V_CPU_IO	Native	H_PWRGD

Following are the GPIOs that need to be terminated properly if not used:
GPIO[39:36,23:21,19,7:0]: default as inputs and should be pulled up to Vcc3_3 if unused.
GPIO[31:29,15:8]: default as inputs and should be pulled up to VccSus3_3 if unused.

SIO Fintek71882FG(CONTINUE)

GPIO	Alt Func	PIN	Usage	Input/Output	NOTES
GPIO0	VIDOUT0	49	MCH_BSEL0	O12	
GPIO1	VIDOUT1	50	MCH_BSEL1	O12	
GPIO2	VIDOUT2	51	MCH_BSEL2	O12	
GPIO3	VIDOUT3	52	NC	O12	
GPIO4	VIDOUT4	53	NC	O12	
GPIO5	VIDOUT5/SIC	54	NC	I/OOD12t	
GPIO6	SLOT0CC#	55	GPO	I/OOD12t	
GPIO7	Turbo1#/WDTRST#	56	WDTRST#	OD12-5v	
GPIO15	LED_VSB/ALERT#	64	LED_VSB	OD12	
GPIO16	LED_VCC/Turbo2#	65	LED_VCC	OD12	
GPIO20	PCIRST1#	74	PCIRST1#	OD12	
GPIO21	PCIRST2#	75	PCIRST2#	O12	
GPIO22	PCIRST3#	76	PCIRST3#	O12	
GPIO23	RSTCON#	77	RSTCON#	OD12	
GPIO24	ATXPG_IN	78	ATXPG_IN	AIN	
GPIO32	PWROK	84	PWROK	OD12	
GPIO26	PWSIN#	80	PWSIN#	INts5v	
GPIO27	PWSOUT#	80	PWSOUT#	OD12	
GPIO30	S3#	82	S3#	INts5v	
GPIO31	PSON#	83	PSON#	OD12-5v	
GPIO33	RSMRST#	85	RSMRST#	OD12	
GPIO40	FANIN3	25	FANIN3	INts5v	
GPIO41	FAN_CTL3	26	FAN_CTL3(NC)	OD12-5v	
GPIO25	PME#	79	PME#	OD12-5v	
GPIO10	SPI_SLK/FANIN4	59	GPIO10(NC)	I/OOD12t	
GPIO11	SPI_CS0#/FANCTL4	60	GPIO11(NC)	I/OOD12t	
GPIO12	SPI_MISO/FANCTL1_1	61	GPIO12(NC)	I/OOD12t	
GPIO13	SPI_MOS/BEEP	62	BEEP(NC)	OD24	
GPIO14	FWH_DIS/WDTRST#/SPI_CS1#	63	GPIO14	I/OOD12t	
GPIO42	IRTX	27	IRTX	O12	
GPIO43	IRRX	28	IRRX	INts	
GPIO17		66	NC	I/OOD12t	

PCI Config.

DEVICEMCP1	INT	PIN REQ#/GNT#	IDSEL	CLOCK
PCI1	PIRQ#A PIRQ#B PIRQ#C PIRQ#D	PREQ#0 PGNT#0	AD16	PCI_CLK0
PCI2	PIRQ#B PIRQ#C PIRQ#D PIRQ#A	PREQ#1 PGNT#1	AD17	PCI_CLK1

DDR II DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM A	A0H	P_DDR0_A/N_DDR0_A P_DDR1_A/N_DDR1_A P_DDR2_A/N_DDR2_A
DIMM B	A4H	P_DDR0_B/N_DDR0_B P_DDR1_B/N_DDR1_B P_DDR2_B/N_DDR2_B

JCI1	Chassis Intrusion
Open	Normal
(1-2)	Chassis Open

JUMPER SETTING

JBAT1	(1-2)NORMAL	(2-3)CLEAR
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0A Change list:

1. Add DMI Audio net name
2. Change LED Power pull high to 680 Change r20 to 1.5K
3. Change D10 D11 Power pull VCC5, Q20 Pull up VCC3
4. Delet R252 R254 C132 R22 C60,change U5 to I95-7523212-T07
5. Modify footprint : C_P3_5_D8_H9 NC_0402_6 NC_0603_10 C0805MSB C0603MS_BOT
6. Swap RN65 RN61 RN23 RN64 RN63 RN24 RN28 RN25 RN66 ; Delet EC20,
7. Add 5VCC TO 3VCC sequence
8. change TESTPIN30 to TPC20B
9. RENAME ,Swap RN37, X_J1 Change to GND , Change C300 C301 to 0.22UF
10. Modify V_1P25_CORE to G31

1.0 Change list:

1. U11 EN(pin3)change to USB_DRV
2. Add SIO pin55 SKTOCC# pull up to 3vsb
3. Swap RN26
4. add Control UP7501 power sequece

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