MS-7529

Version 1.1

CPU:

Intel Conroe (65W Dual core)

System Chipset:

Intel Bearlake - MCH (North Bridge)
Intel ICH7R (South Bridge)

On Board Chipset:

BIOS -- SPI
HD -- ALC888
LPC Super I/O -- F71882FG
LAN-- REALTEK RTL8111C Co-lay RTL8101E
CLOCK -- RTM876-665

Main Memory:

DDR II *2 (Max 4GB)

Expansion Slots:

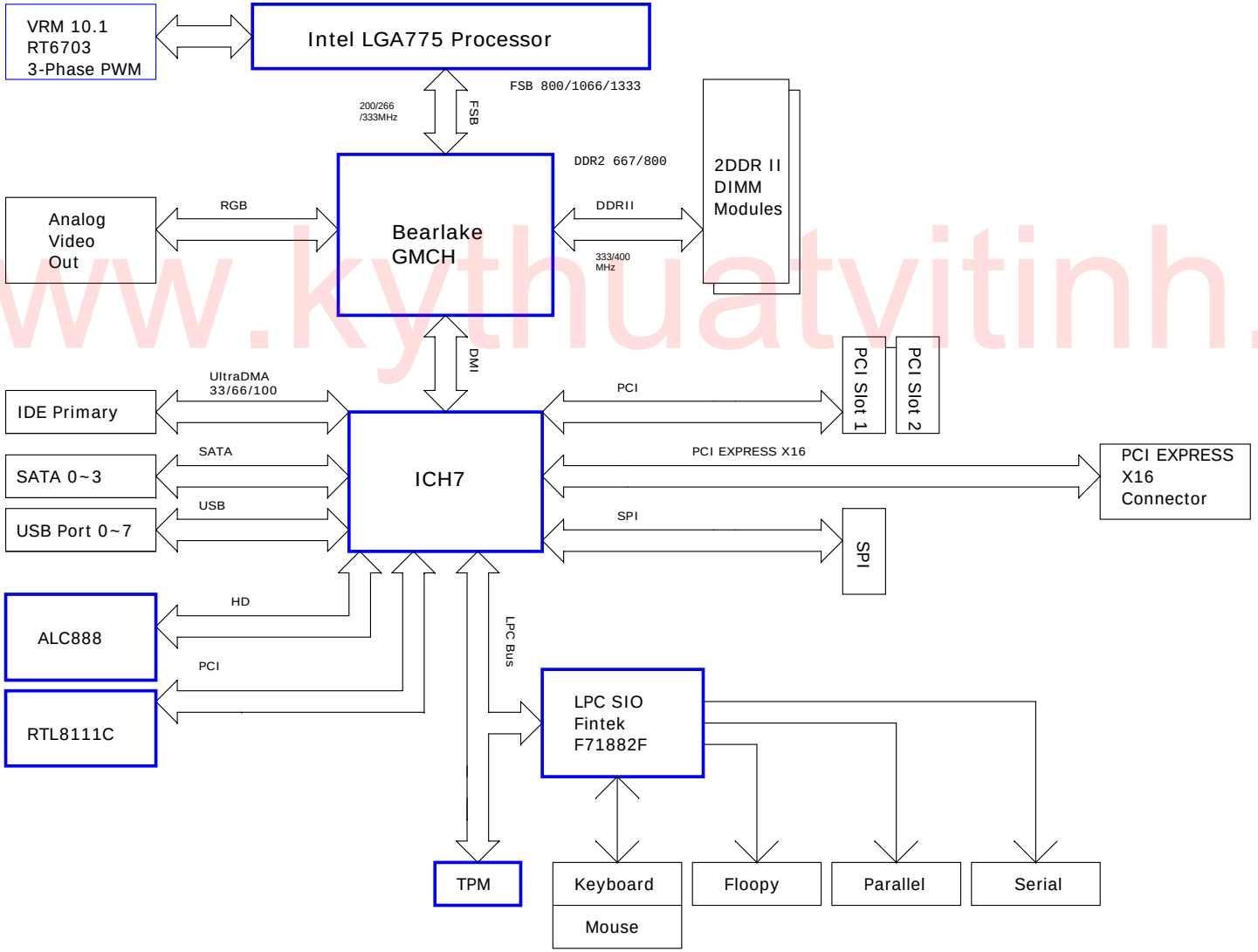
PCI2.3 SLOT * 2

PCI EXPRESS X16 SLOT

ST PWM:

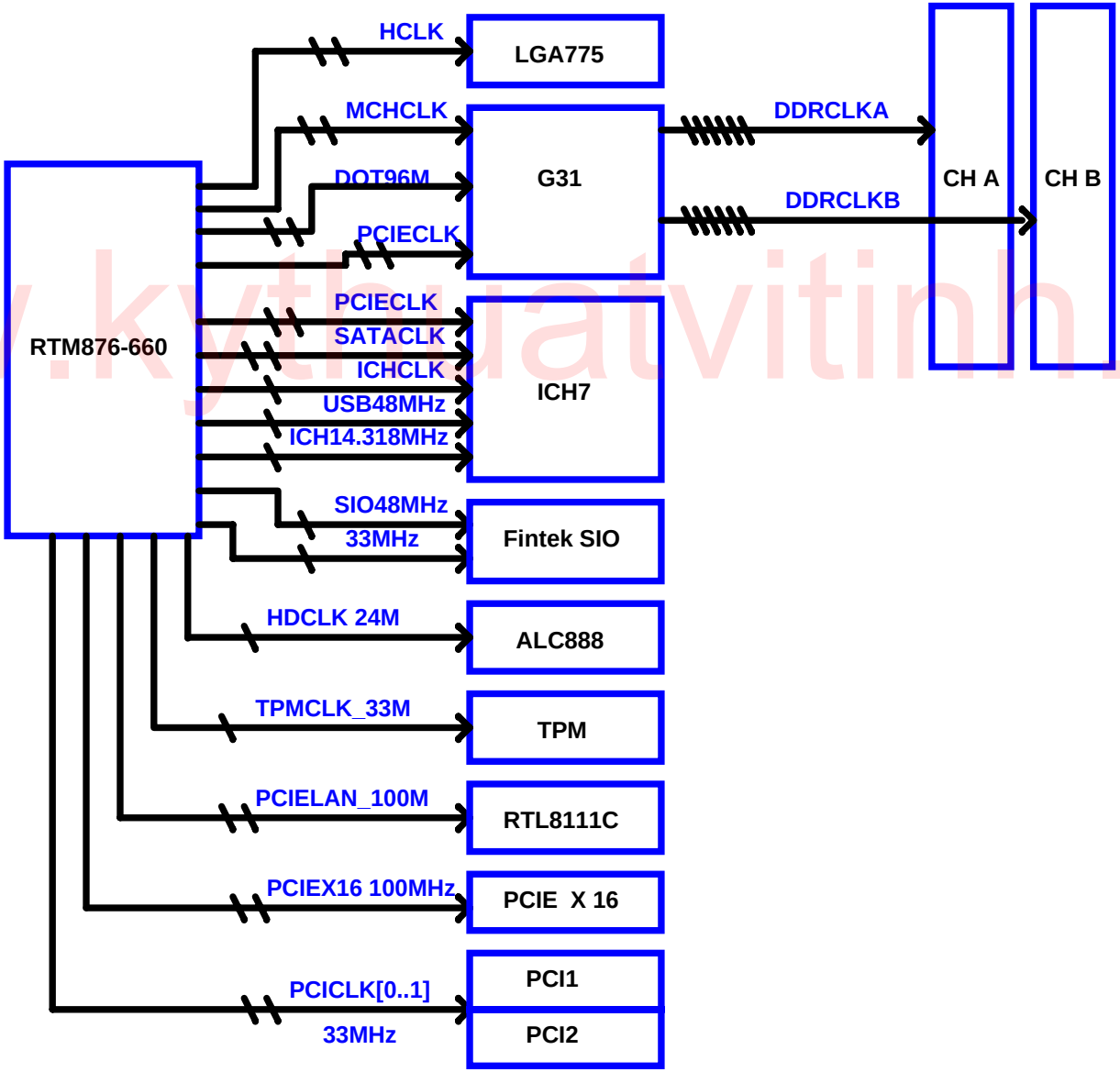
Controller: 3 PHASES

Block Diagram

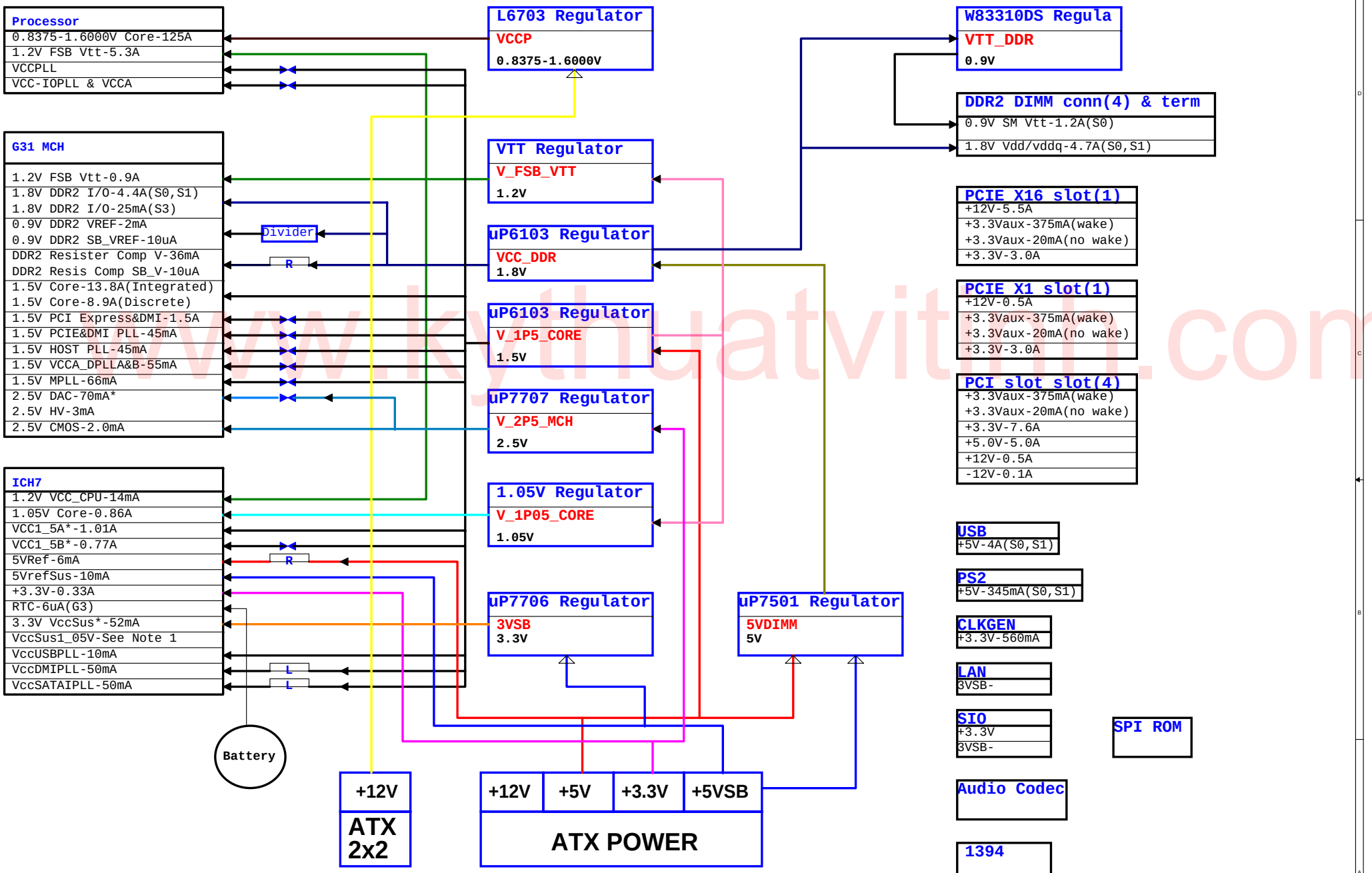


MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7529	
Size: Custom	Document Description: BLOCK DIAGRAM	Rev: 1.1
Date: Friday, May 16, 2008	Sheet 2 of 33	

CLOCK MAP



MICRO-STAR INT'L CO.,LTD		
MS-7529		
Size: Custom	Document Description: CLOCK MAP	Rev: 1.1
Date: Friday, May 16, 2008	Sheet 3 of 33	



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MS-7529

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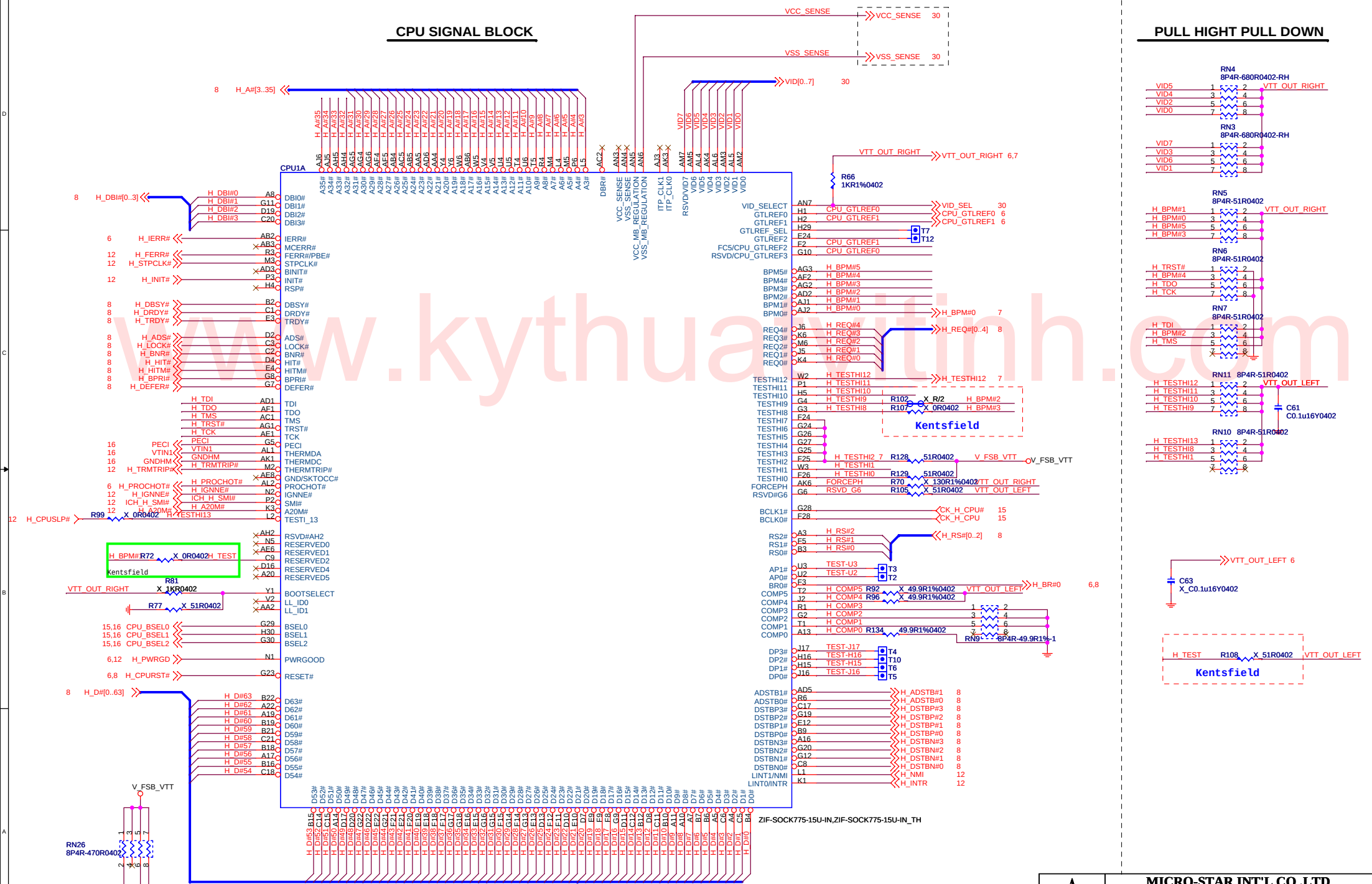
Custom	LGA775 - Signal	1.1

Date: Friday, May 16, 2008 Sheet 4 of 33

CPU SIGNAL BLOCK



PULL HIGHT PULL DOWN

MICRO-STAR INT'L CO.,LTD

MS-7529

Size	Document Description	Rev
Custom	LGA775 - Signal	1.1

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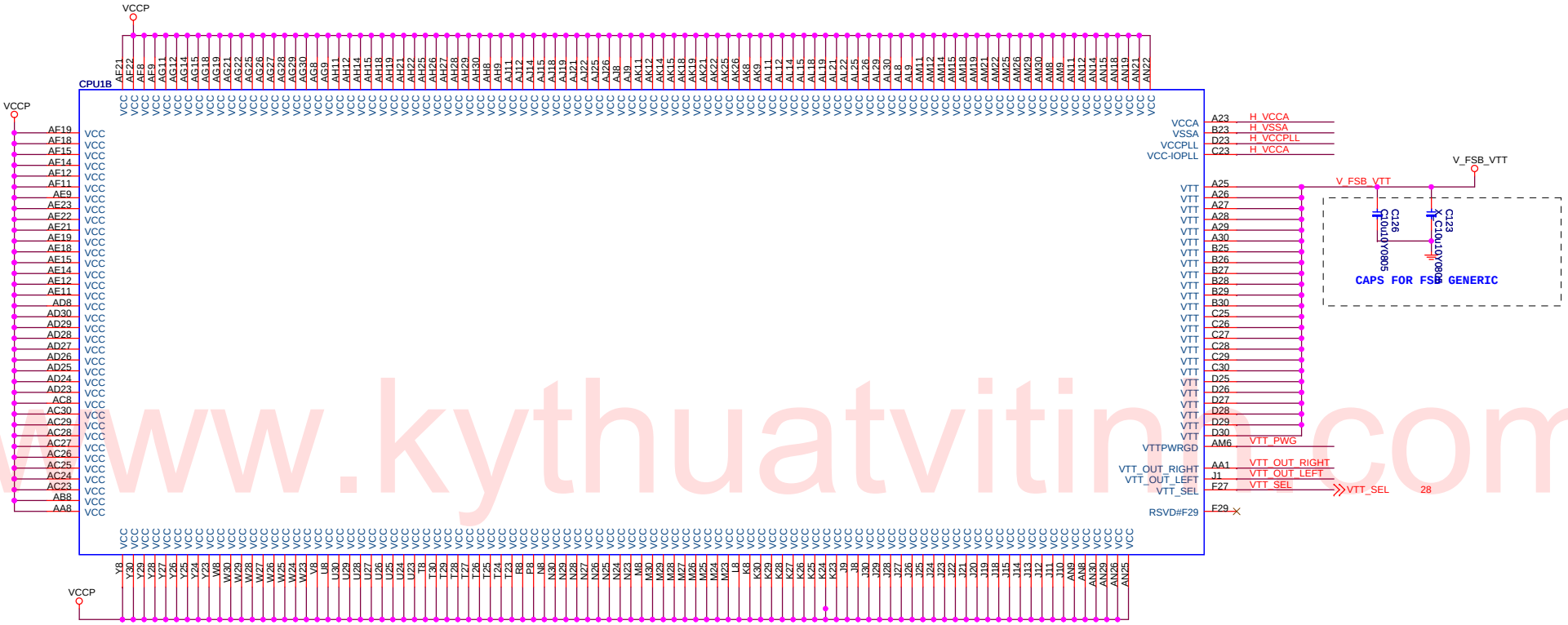
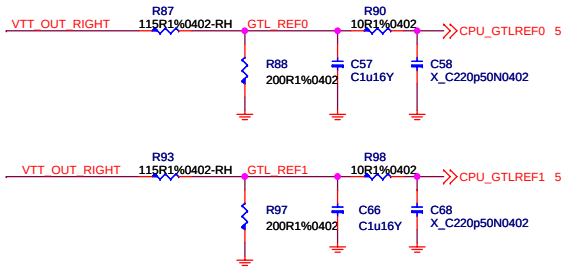
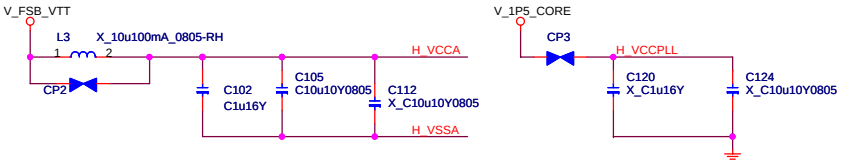


*GTLREF VOLTAGE SHOULD BE 0.67 * VTT = 0.8V (At VTT=1.2V)

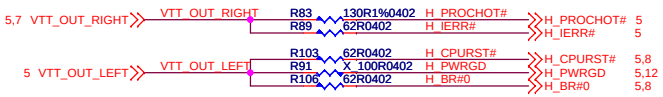


*PLACE COMPONENTS AS CLOSE AS POSSIBLE TO PROCESSOR SOCKET
*TRACE WIDTH TO CAPS MUST BE NO SMALLER THAN 12MILS

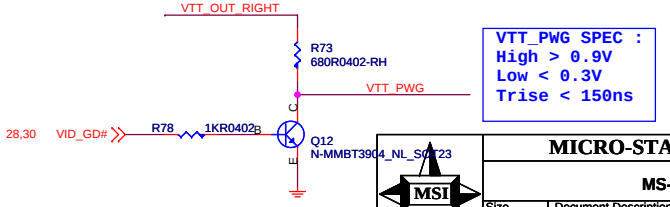


ZIF-SOCK775-15U-IN,ZIF-SOCK775-15U-IN_TH

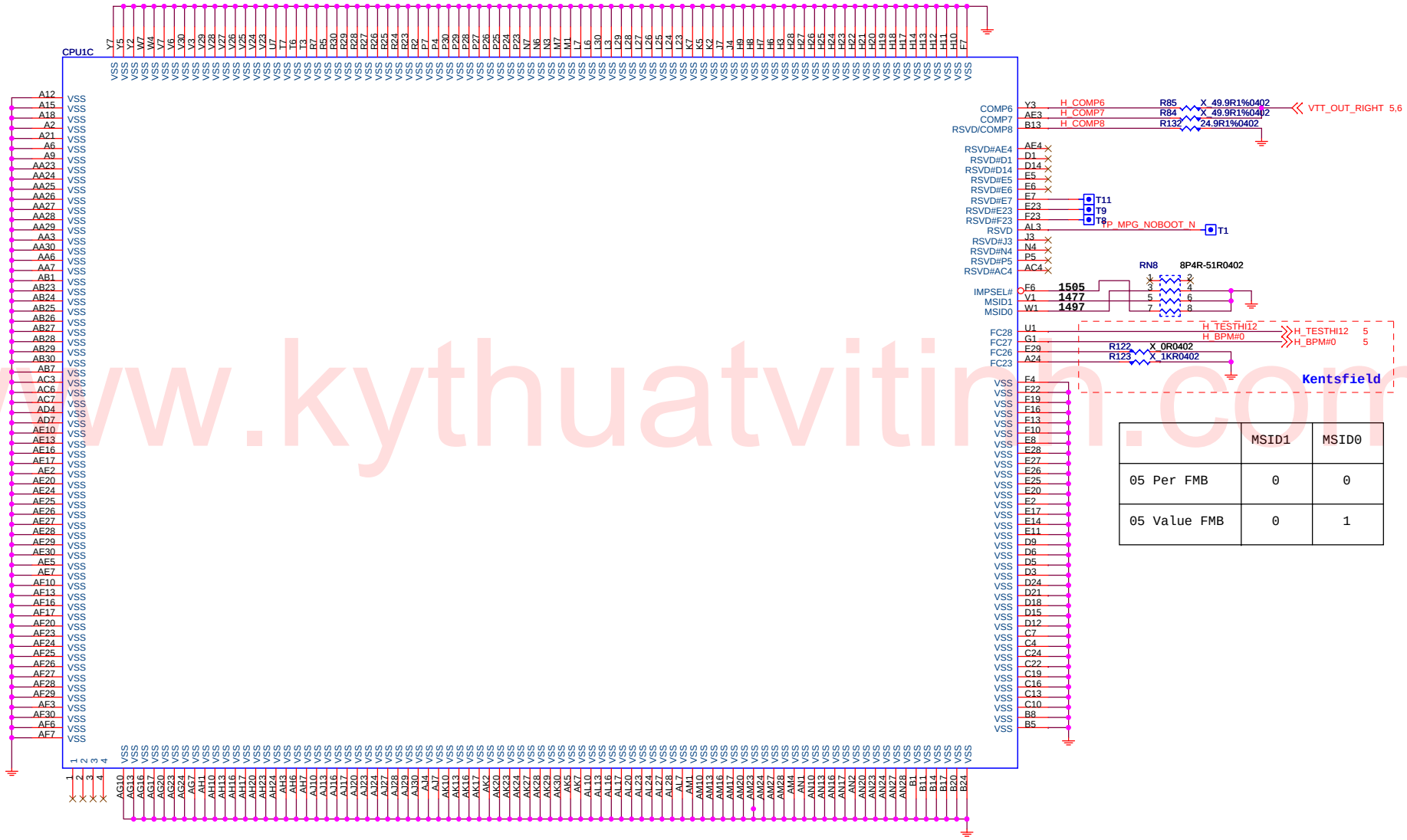
PLACE AT CPU END OF ROUTE



VTT_PWRGOOD



MICRO-STAR INT'L CO.,LTD			
MS-7529			
Size: Custom	Document Description: LGA775 - Power		Rev: 1.1
Date: Friday, May 16, 2008		Sheet 6 of 33	



	MSID1	MSID0
05 Per FMB	0	0
05 Value FMB	0	1

MICRO-STAR INT'L CO.,LTD

MS-7529

Size	Document Description	Rev
Custom	LGA775 - GND	1.1

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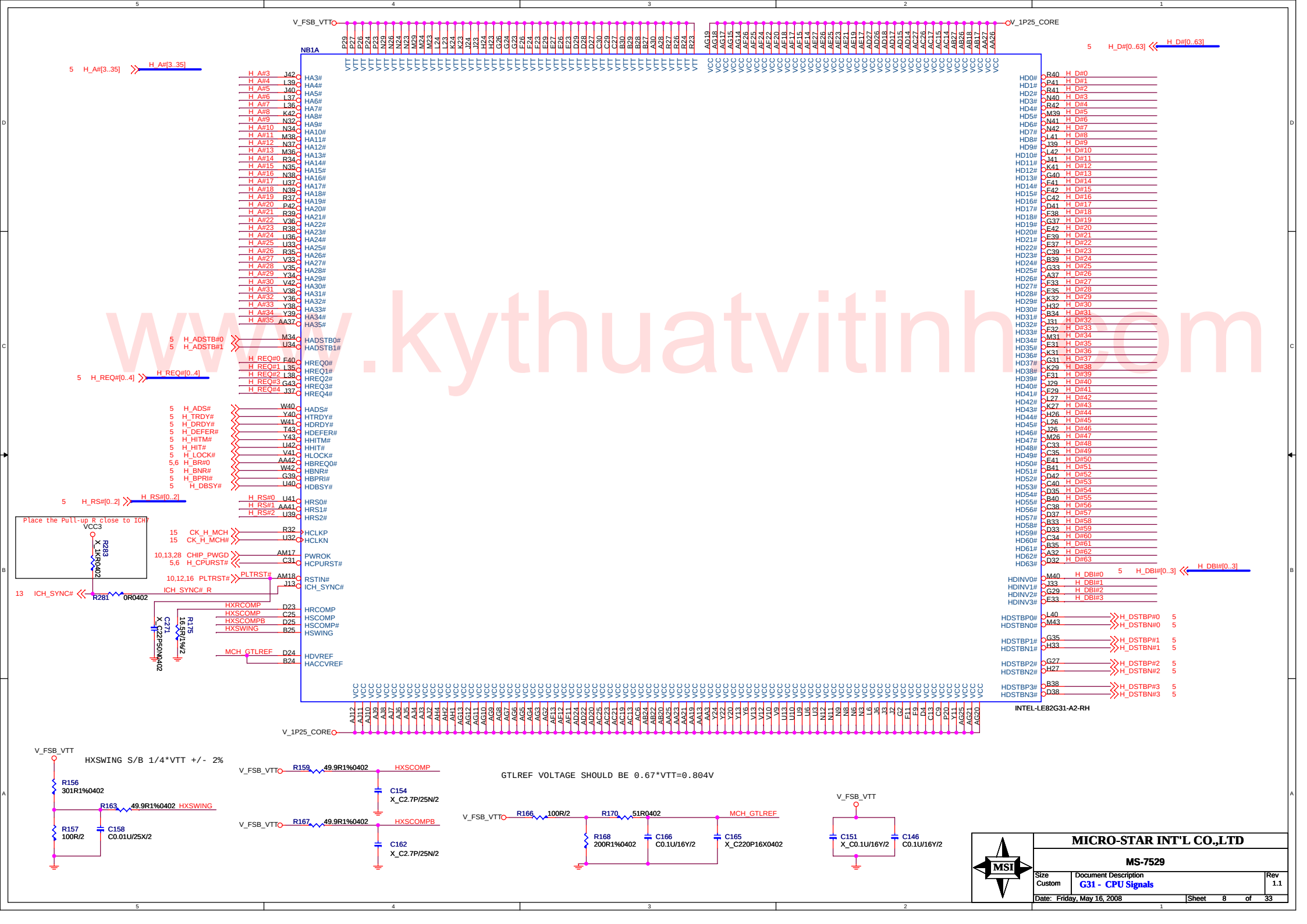

MICRO-STAR INT'L CO.,LTD

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Size	Document Description	Rev
Custom	G31 - CPU Signals	1.1

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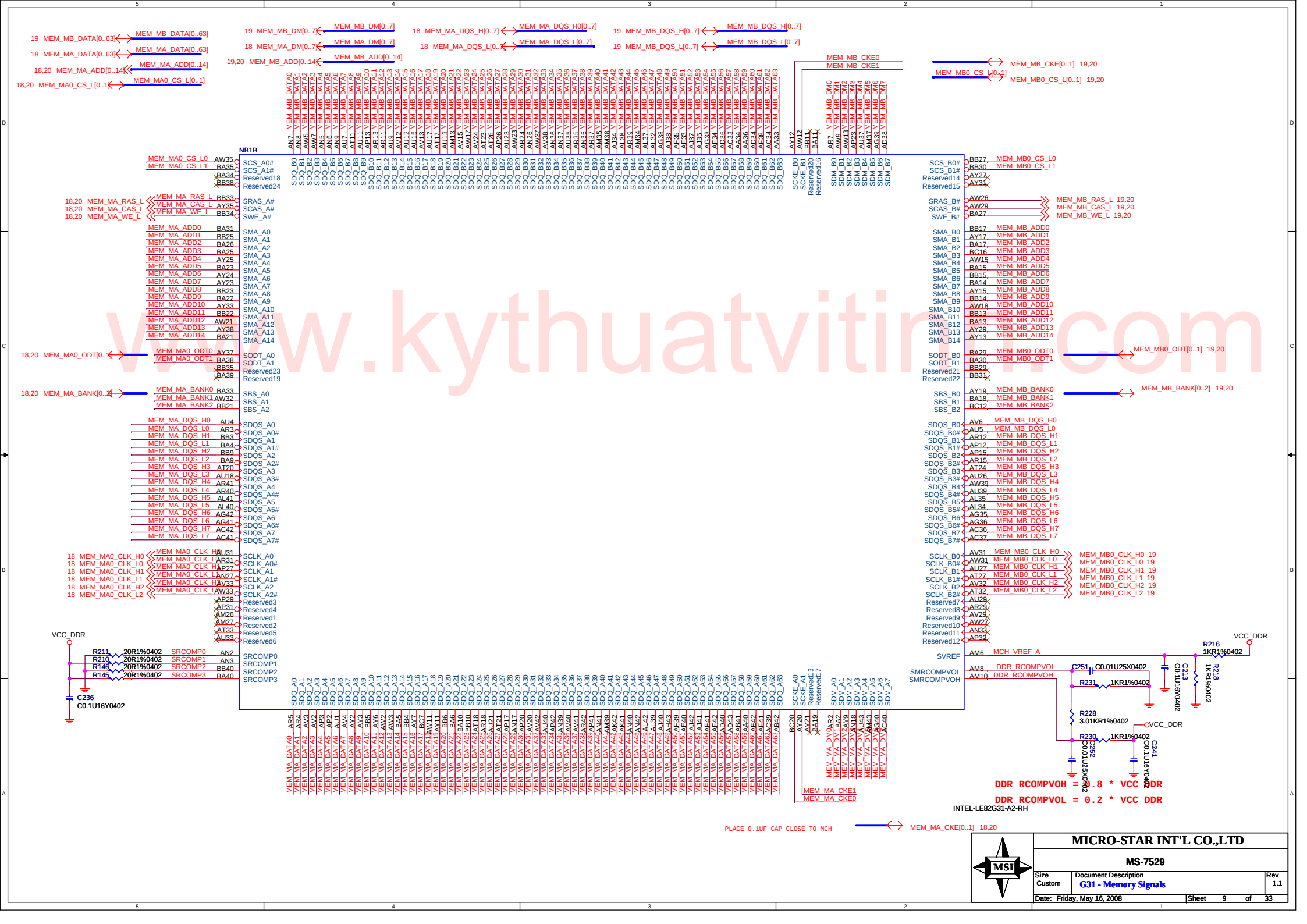
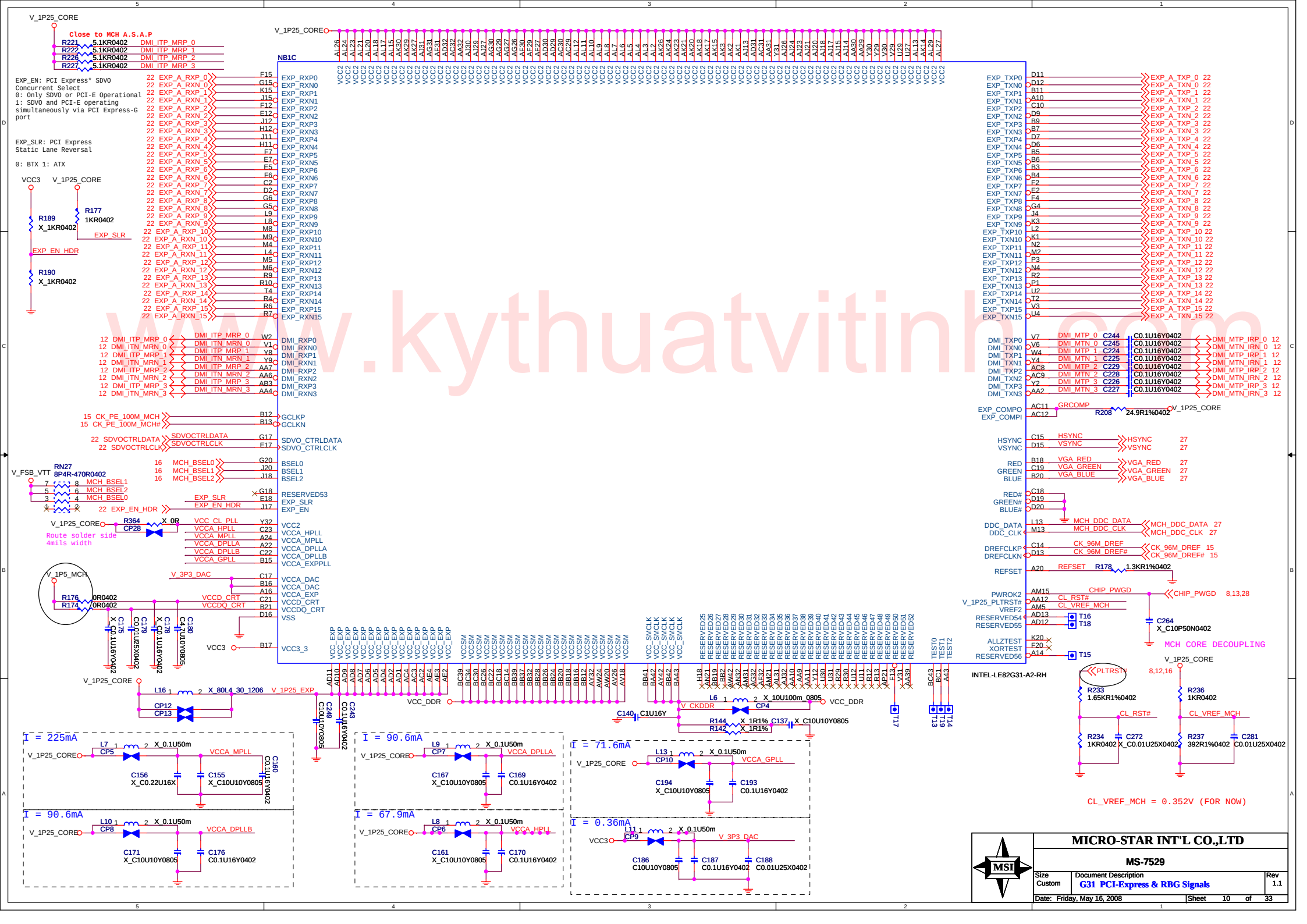
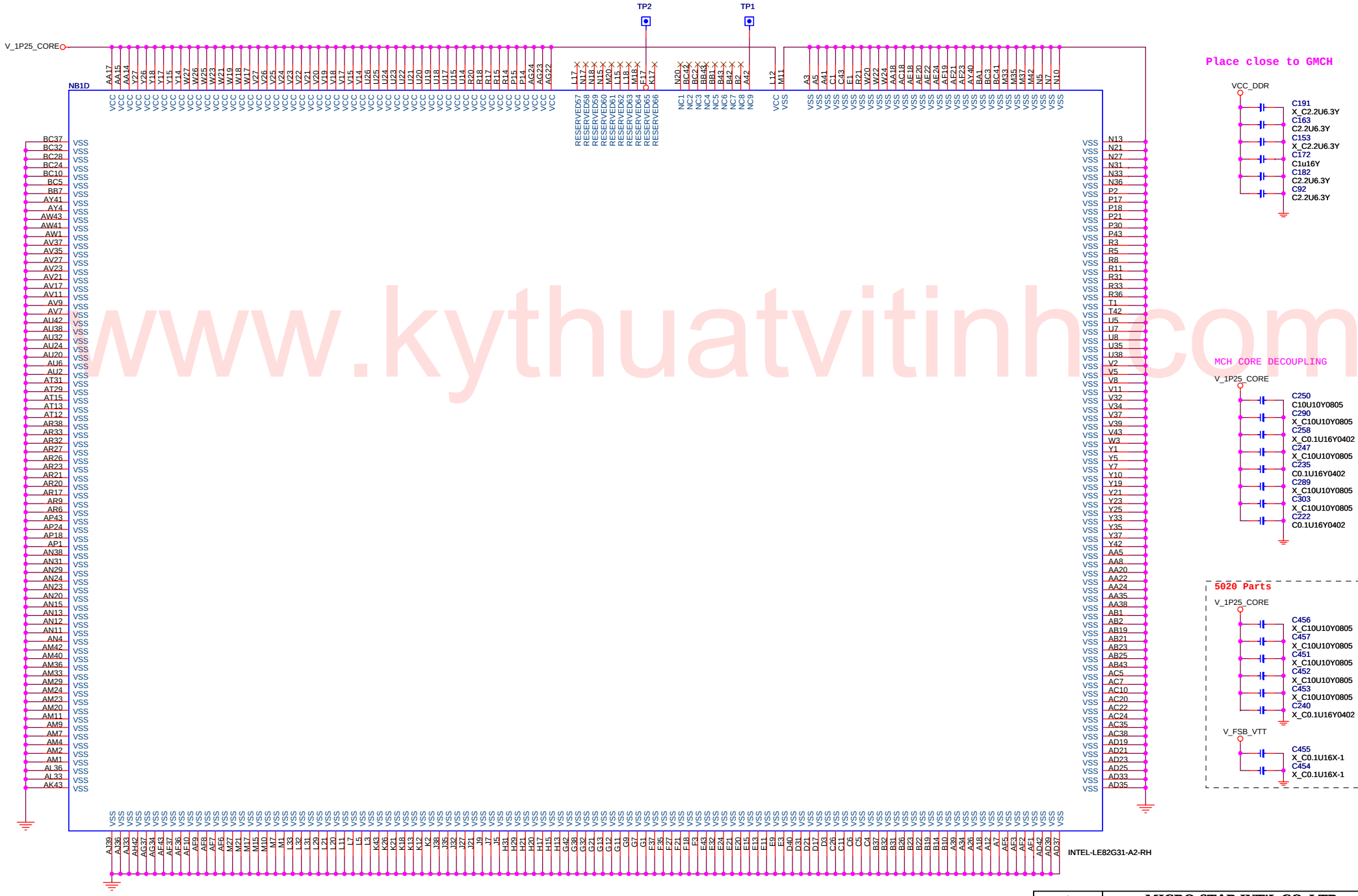
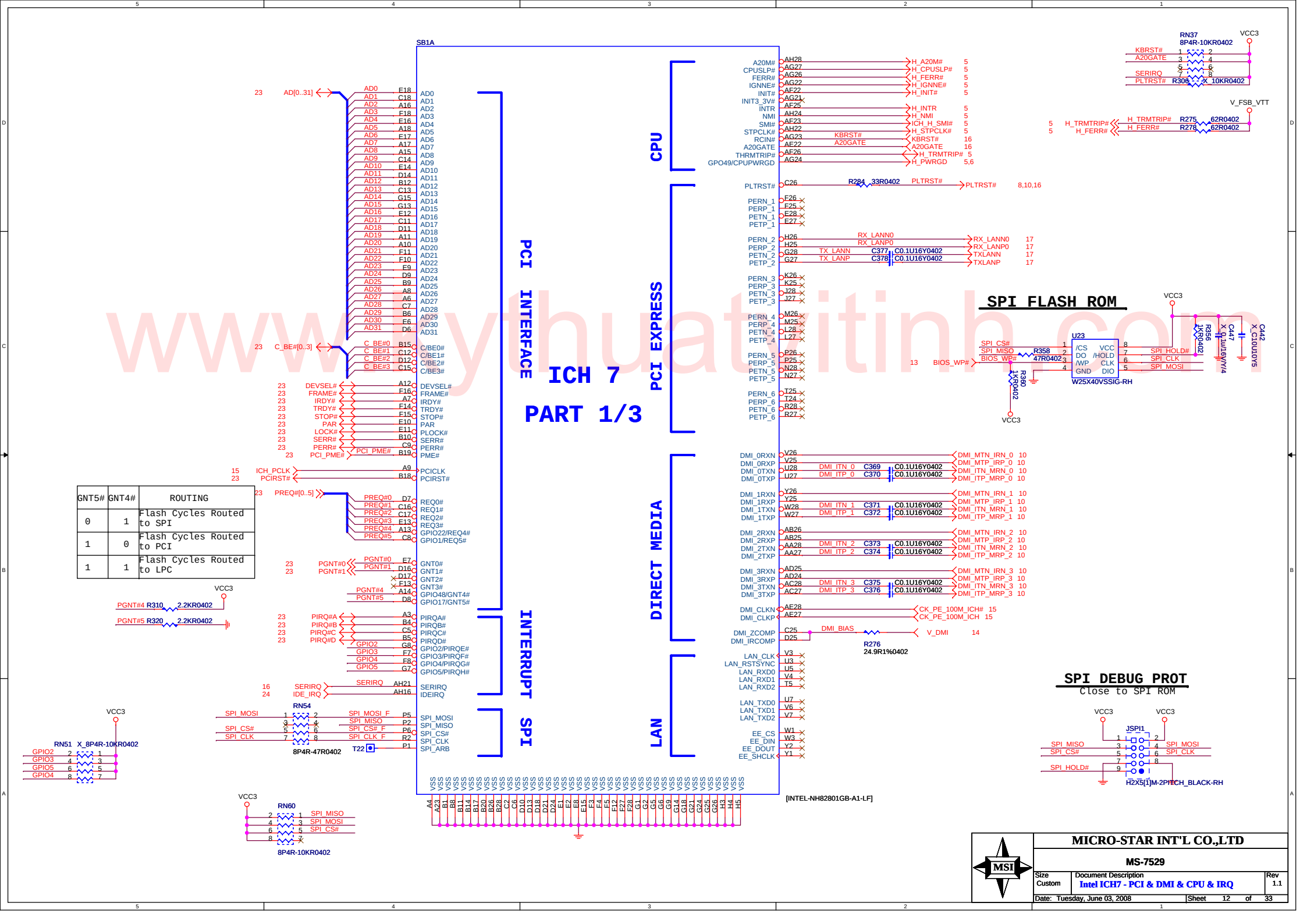






MICRO-STAR INT'L CO.,LTD		
MS-7529		
Size: Custom	Document Description: Intel .G31 - GND	Rev: 1.1
Date: Friday, May 16, 2008	Sheet 11 of 33	


SB1A
ICH 7
PART 1/3
PCI INTERFACE
PCI EXPRESS
DIRECT MEDIA
INTERRUPT
SPI
LAN
CPU
SPI FLASH ROM
SPI DEBUG PROT
Close to SPI ROM
W25X40VSSIG-RH
[INTEL-NH82801GB-A1-LF]
GNT5# GNT4# ROUTING
0 1 Flash Cycles Routed to SPI
1 0 Flash Cycles Routed to PCI
1 1 Flash Cycles Routed to LPC
MICRO-STAR INT'L CO.,LTD
MS-7529
Intel ICH7 - PCI & DMI & CPU & IRQ
Rev 1.1
Date: Tuesday, June 03, 2008
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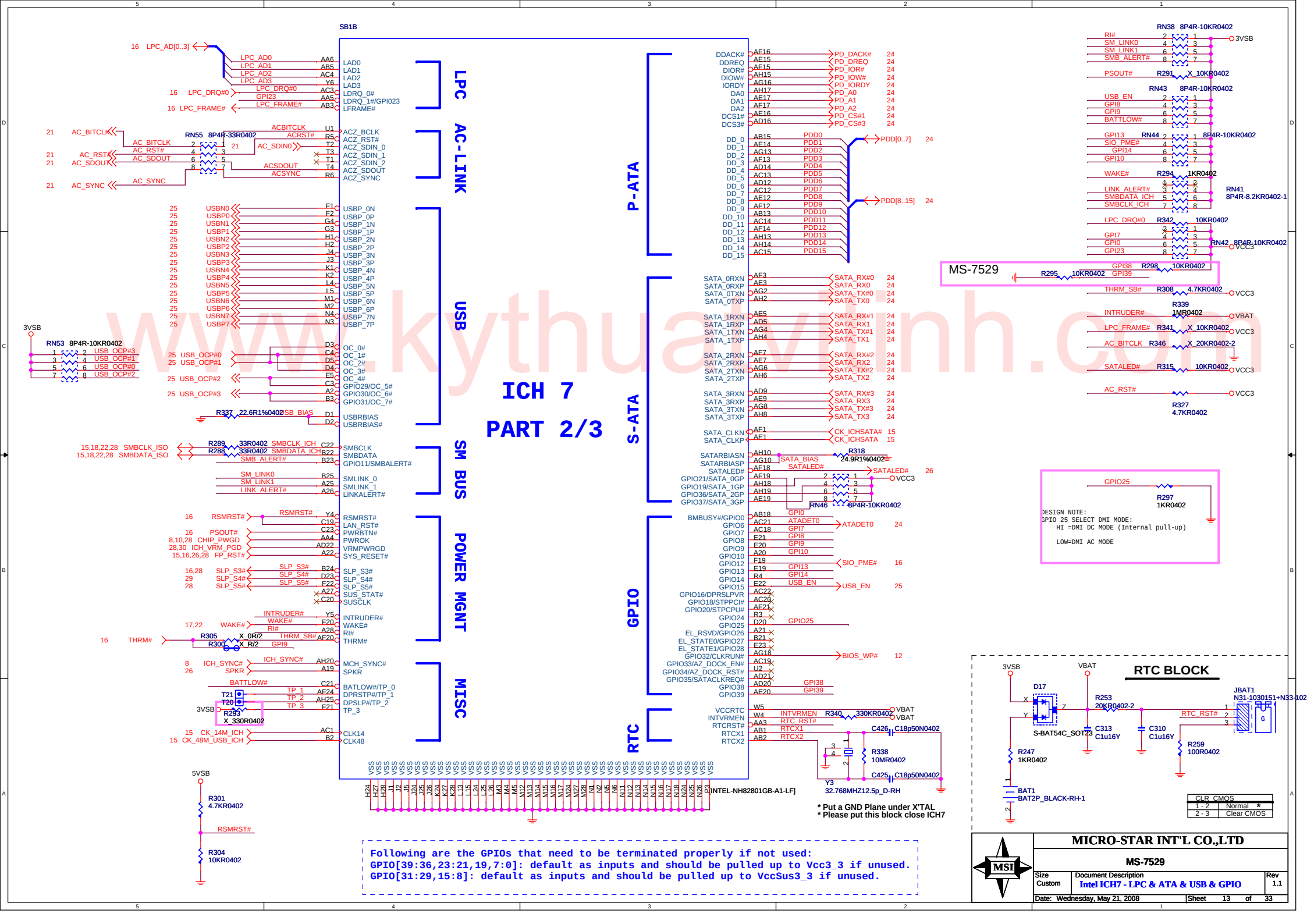
SB1B
LPC AC-LINK
USB
SM BUS
POWER MGNT
MISC
P-ATA
S-SATA
GPIO
RTC
ICH 7
PART 2/3
LPC_AD[0..3]
LPC_DRQ#0
LPC_FRAME#
AC_BITCLK
AC_RST#
AC_SDOUT
AC_SYNC
USBN0
USBP0
USBN1
USBP1
USBN2
USBP2
USBN3
USBP3
USBN4
USBP4
USBN5
USBP5
USBN6
USBP6
USBN7
USBP7
USB_OCP#0
USB_OCP#1
USB_OCP#2
USB_OCP#3
SMBCLK_ISO
SMBDATA_ISO
SMB_ALERT#
SM_LINK0
SM_LINK1
LINK_ALERT#
RSMRST#
PSOUT#
CHIP_PWGD
ICH_VRM_PGD
FP_RST#
SLP_S3#
SLP_S4#
SLP_S5#
WAKE#
RI#
THRM#
ICH_SYNC#
SPKR
BATTLOW#
CK_14M_ICH
CK_48M_USB_ICH
PD_DACK#
PD_DREQ
PD_IOR#
PD_IOW#
PD_IORDY
PD_A0
PD_A1
PD_A2
PD_CS#1
PD_CS#3
PDD[0..7]
PDD[8..15]
SATA_RX#0
SATA_RX0
SATA_TX#0
SATA_TX0
SATA_RX#1
SATA_RX1
SATA_TX#1
SATA_TX1
SATA_RX#2
SATA_RX2
SATA_TX#2
SATA_TX2
SATA_RX#3
SATA_RX3
SATA_TX#3
SATA_TX3
CK_ICHSATA#
CK_ICHSATA
SATA_BIAS
SATALED#
GPIO21/SATA_0GP
GPIO19/SATA_1GP
GPIO36/SATA_2GP
GPIO37/SATA_3GP
BMBUSY#/GPIO0
GPIO6
GPIO7
GPIO8
GPIO9
GPIO10
GPIO12
GPIO13
GPIO14
GPIO15
GPIO16/DPRSLPVR
GPIO18/STPPCI#
GPIO20/STPCPU#
GPIO24
GPIO25
EL_RSVD/GPIO26
EL_STATE0/GPIO27
EL_STATE1/GPIO28
GPIO32/CLKRUN#
GPIO33/AZ_DOCK_EN#
GPIO34/AZ_DOCK_RST#
GPIO35/SATACLKREQ#
GPIO38
GPIO39
ATADET0
SIO_PME#
USB_EN
BIOS_WP#
VCCRTC
INTVRMEN
RTCRST#
RTCX1
RTCX2
RTC_RST#
INTRUDER#
THERM_SB#
MCH_SYNC#
BATLOW#/TP_0
DPRSTP#/TP_1
DPSLP#/TP_2
TP_3
CLK14
CLK48
RN55 8P4R-33R0402
RN53 8P4R-10KR0402
RN46 8P4R-10KR0402
R337 22.6R1%0402
R289 33R0402
R288 33R0402
R305 X_0R/2
R300 X_R/2
R293 X_330R0402
R318 24.9R1%0402
R340 330KR0402
R338 10MR0402
Y3 32.768MHZ12.5p_D-RH
C426 C18p50N0402
C425 C18p50N0402
R301 4.7KR0402
R304 10KR0402
[INTEL-NH82801GB-A1-LF]
* Put a GND Plane under X'TAL
* Please put this block close ICH7
Following are the GPIOs that need to be terminated properly if not used:
GPIO[39:36,23:21,19,7:0]: default as inputs and should be pulled up to Vcc3_3 if unused.
GPIO[31:29,15:8]: default as inputs and should be pulled up to VccSus3_3 if unused.
RN38 8P4R-10KR0402
RN43 8P4R-10KR0402
RN44 8P4R-10KR0402
RN41 8P4R-8.2KR0402-1
RN42 8P4R-10KR0402
R291 X_10KR0402
R294 1KR0402
R342 10KR0402
R298 10KR0402
R295 10KR0402
R308 4.7KR0402
R339 1MR0402
R341 X_10KR0402
R346 X_20KR0402-2
R315 10KR0402
R327 4.7KR0402
MS-7529
GPIO25
R297 1KR0402
DESIGN NOTE:
GPIO 25 SELECT DMI MODE:
HI =DMI DC MODE (Internal pull-up)
LOW=DMI AC MODE
RTC BLOCK
D17
S-BAT54C_SOT23
R253 20KR0402-2
C313 C1u16Y
C310 C1u16Y
R259 100R0402
R247 1KR0402
BAT1 BAT2P_BLACK-RH-1
JBAT1 N31-1030151+N33-102
CLR_CMOS
1 - 2 Normal
2 - 3 Clear CMOS
MICRO-STAR INT'L CO.,LTD
MS-7529
Size Custom
Document Description Intel ICH7 - LPC & ATA & USB & GPIO
Rev 1.1
Date: Wednesday, May 21, 2008
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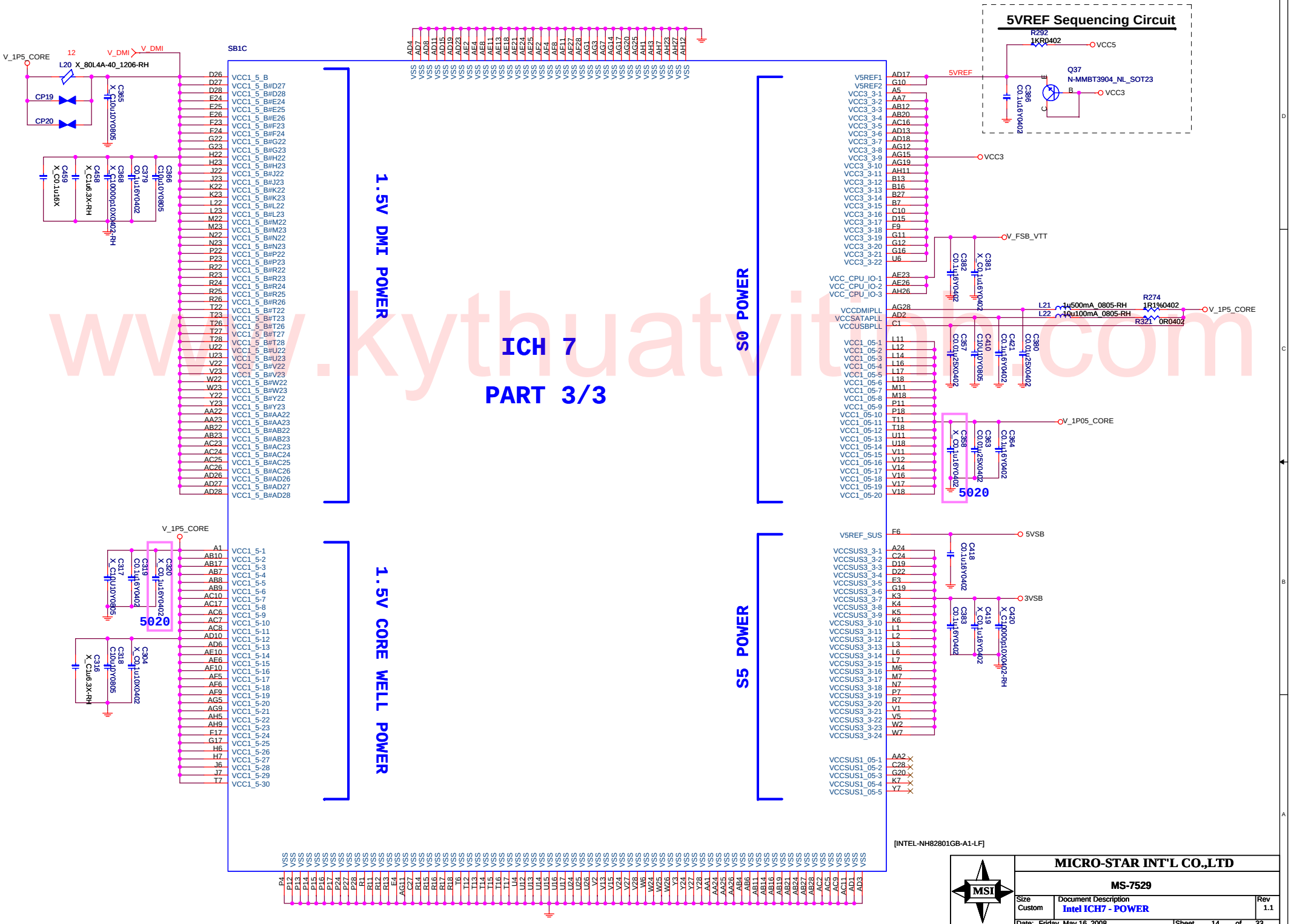
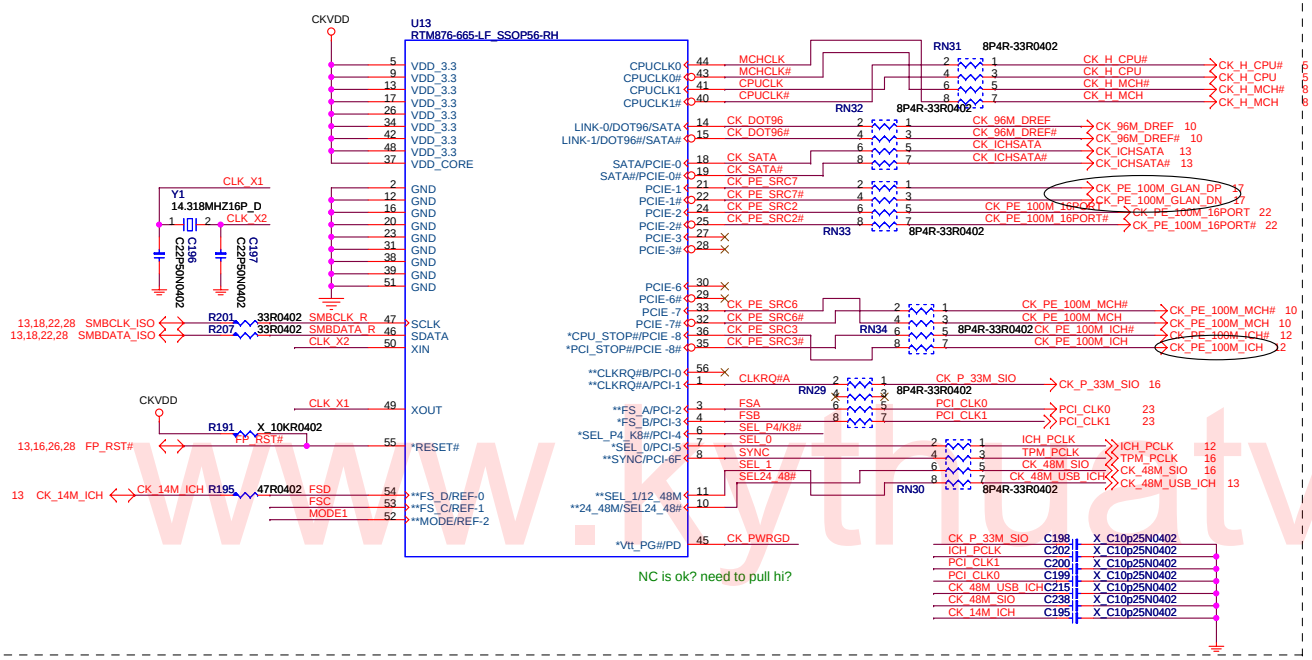
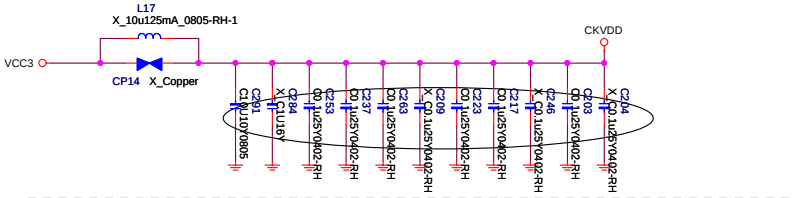


Clock Generator - RTM876-665





STRAPPING RESISTOR

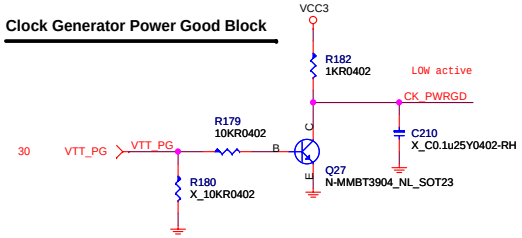
SEL_1	SEL_0	Chipset Support
0	0	SIS
1	0	VIA
0	1	Intel W/GFX
1	1	Intel

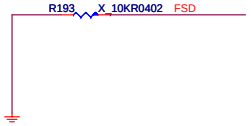
SEL_P4/K8#	PIN#40,41,43,44
0	K8 3.3V swing
1	P4 0.8V swing

MODE	PIN#35/36
0	PCIE-8 T/C
1	PCI STOP#/CPU_STOP#

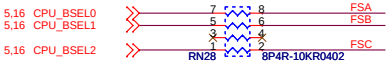
SEL24_48#	Pin#10
0	48Mhz
1	24Mhz

Clock Generator Power Good Block





CPU Frequency Selection

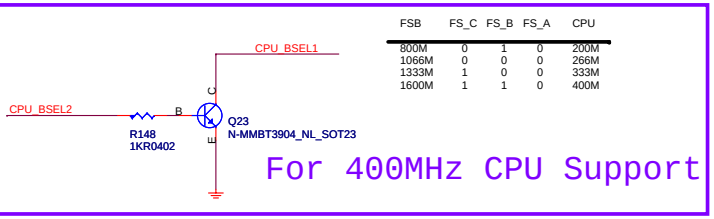


FS_C	FS_B	FS_A	CPU
0	0	0	266M
0	0	1	133M
0	1	0	200M
0	1	1	166M
1	0	0	333M
1	0	1	100M
1	1	0	400M
1	1	1	200M

CPU Frequency Selection

FS_C	FS_B	FS_A	CPU
0	0	1	133M
0	1	0	200M
0	0	0	266M
1	0	0	333M
1	1	0	400M

Only the selection in the table is valid



FSB	FS_C	FS_B	FS_A	CPU
800M	0	1	0	200M
1066M	0	0	0	266M
1333M	1	0	0	333M
1600M	1	1	0	400M

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Size: Custom | Document Description: CLK-RTM 876-665 | Rev: 1.1

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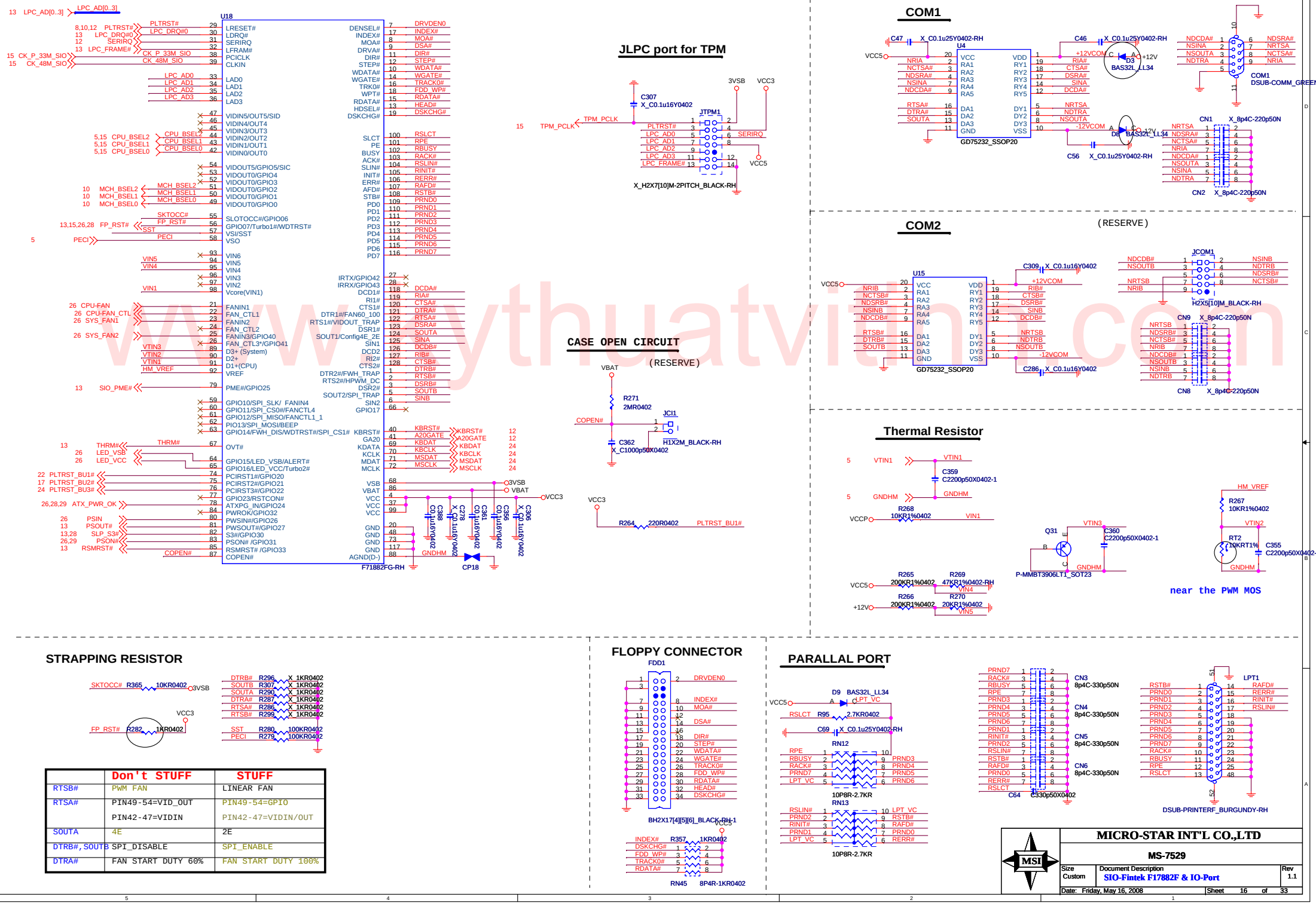

	Don't STUFF	STUFF
RTSB#	PWM FAN	LINEAR FAN
RTSA#	PIN49-54=VID_OUT PIN42-47=VIDIN	PIN49-54=GPIO PIN42-47=VIDIN/OUT
SOUTA	4E	2E
DTRB#,SOUTB	SPI_DISABLE	SPI_ENABLE
DTRA#	FAN START DUTY 60%	FAN START DUTY 100%

MICRO-STAR INT'L CO.,LTD		
MS-7529		
Size: Custom	Document Description: SIO-Fintek F17882F & IO-Port	Rev: 1.1
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R257=2K(R11-0202T12-R01) for 8101E;
R257=2.49k(R11-2491T12-R01) for 8111B/C

For 8111C only

R187
For 8111C only

For 8101E only

R224
For 8111C only

For 8101E only

For 8101E only

For 8101E only

For 8101E only

For 8101E only

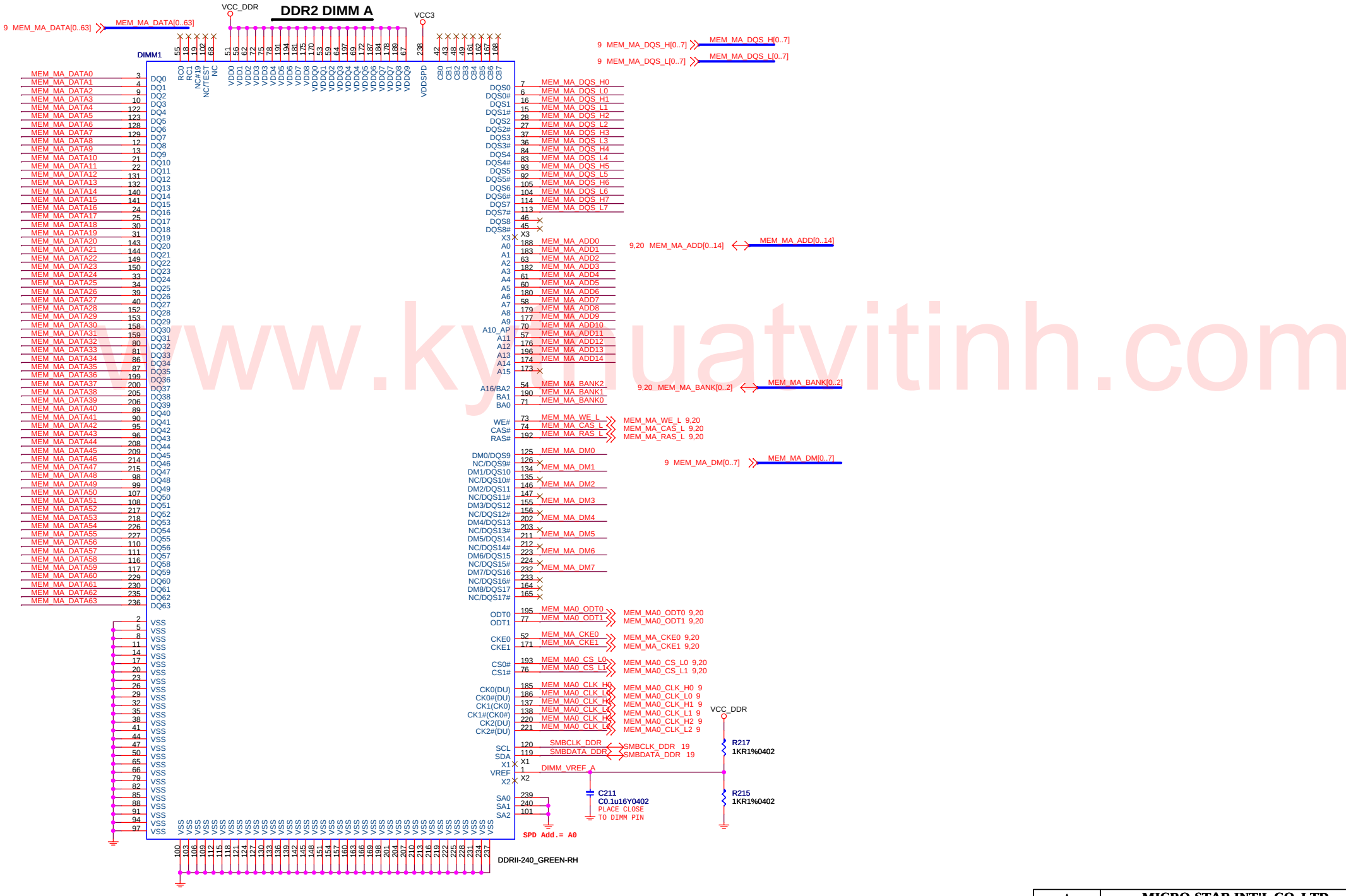
CHOKE
For 8111C only

For 8101E only

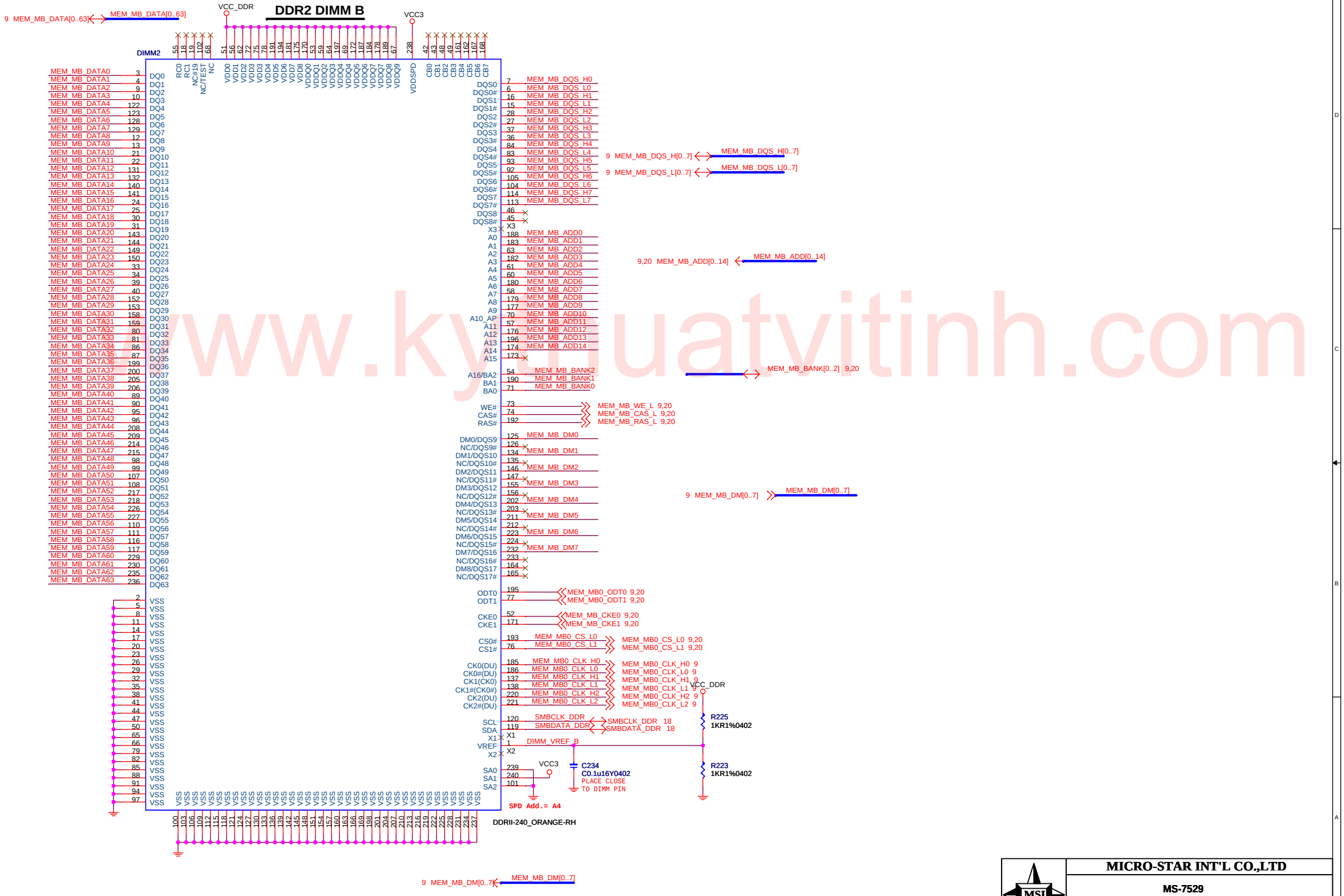
For 8111C only

Giga-Lan	10/100-Lan
N58-22F0181-S42	N58-22F0201-S42
Link Yellow Active Blinking 1000 Orange 100 Green 10 None	Link Yellow Active Blinking 100 Green 10 None
19 20 Yellow 21 Orange 22 Green	19 20 Yellow 21 22 Green

Micro Star Restricted Secret	
Title: RTL8101E/8111C	Rev: 1.1
Document Number: MS-7529	
MICRO-STAR INT'L CO.,LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw	Last Revision Date: Thursday, May 29, 2008 Sheet 17 of 33



MICRO-STAR INT'L CO.,LTD	
MS-7529	
Size: Custom	Document Description: DDR II DIMM A & B
Rev: 1.1	
Date: Thursday, May 29, 2008	Sheet 18 of 33



MICRO-STAR INT'L CO.,LTD	
MS-7529	
Size: Custom	Document Description: DDR II DIMM A & B
Rev: 1.1	
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CHANNEL A V_SM_VTT DECOULPING CAPS

VTT_DDR
C120 X_C4.7u6.3X5

VTT_DDR
C104 C0.1u16Y0402
C99 X_C0.1u16Y0402
C127 X_C0.1u16Y0402

CHANNEL B V_SM_VTT DECOULPING CAPS

VTT_DDR
C103 X_C4.7u6.3X5
C106 C4.7u6.3X5

VTT_DDR
C117 X_C0.1u16Y0402
C96 X_C0.1u16Y0402
C128 X_C0.1u16Y0402
C101 C0.1u16Y0402

VCC_DDR
C89 C1U10Y0402-RH
C108 C1U10Y0402-RH
C279 C0.1u16Y0402
C86 C0.1u16Y0402
C87 C0.1u16Y0402
C100 C2200p50X0402-1
C98 C0.1u16Y0402

VCC_DDR
C132 C1U10Y0402-RH
C95 X_C1U10Y0402-RH
C147 C2200p50X0402-1
C109 C2200p50X0402-1
C121 X_C500p50X0402
C184 C2200p50X0402-1

EMI

VCC_DDR
C113 X_C0.1u16Y0402
VTT_DDR

VTT_DDR

RN20 8P4R-33R0402
MEM_MA_ADD4
MEM_MA_ADD3
MEM_MA_ADD1
MEM_MA_ADD2

RN22 8P4R-33R0402
MEM_MA_ADD7
MEM_MA_ADD8
MEM_MA_ADD5
MEM_MA_ADD6

RN24 8P4R-33R0402
MEM_MA_BANK2
MEM_MA_ADD12
MEM_MA_ADD11
MEM_MA_ADD9

RN17 8P4R-33R0402
9,18 MEM_MA_RAS_L
9,18 MEM_MA_WE_L
9,18 MEM_MA_CAS_L
MEM_MA_RAS_L
MEM_MA_WE_L
MEM_MA_CAS_L
MEM_MA_ADD13

MEM_MA_ADD14 R135 33R0402

RN19 8P4R-33R0402
MEM_MA_ADD0
MEM_MA_BANK1
MEM_MA_ADD10
MEM_MA_BANK0

RN15 8P4R-43R0402
MEM_MA0_ODT1
MEM_MA0_ODT0
MEM_MA0_CS_L1
MEM_MA0_CS_L0

MEM_MA_CKE0 R136 43R0402
MEM_MA_CKE1 R138 43R0402

9,18 MEM_MA_ADD[0..14]
9,18 MEM_MA_BANK[0..2]
9,18 MEM_MA0_CS_L[0..1]
9,18 MEM_MA_CKE[0..1]
9,18 MEM_MA0_ODT[0..1]

VTT_DDR

RN21 8P4R-33R0402
MEM_MB_ADD4
MEM_MB_ADD3
MEM_MB_ADD1
MEM_MB_ADD2

RN25 8P4R-33R0402
MEM_MB_BANK2
MEM_MB_ADD12
MEM_MB_ADD11
MEM_MB_ADD7

RN23 8P4R-33R0402
MEM_MB_ADD9
MEM_MB_ADD8
MEM_MB_ADD6
MEM_MB_ADD5

RN16 8P4R-33R0402
9,19 MEM_MB_RAS_L
9,19 MEM_MB_WE_L
9,19 MEM_MB_CAS_L
MEM_MB_RAS_L
MEM_MB_WE_L
MEM_MB_CAS_L
MEM_MB_ADD13

MEM_MB_ADD14 R137 33R0402

RN18 8P4R-33R0402
MEM_MB_ADD0
MEM_MB_ADD10
MEM_MB_BANK1
MEM_MB_BANK0

RN14 8P4R-43R0402
change RN
MEM_MB0_ODT1
MEM_MB0_CS_L1
MEM_MB0_ODT0
MEM_MB0_CS_L0

MEM_MB_CKE0 R141 43R0402
MEM_MB_CKE1 R139 43R0402

9,19 MEM_MB_ADD[0..14]
9,19 MEM_MB_BANK[0..2]
9,19 MEM_MB0_CS_L[0..1]
9,19 MEM_MB_CKE[0..1]
9,19 MEM_MB0_ODT[0..1]

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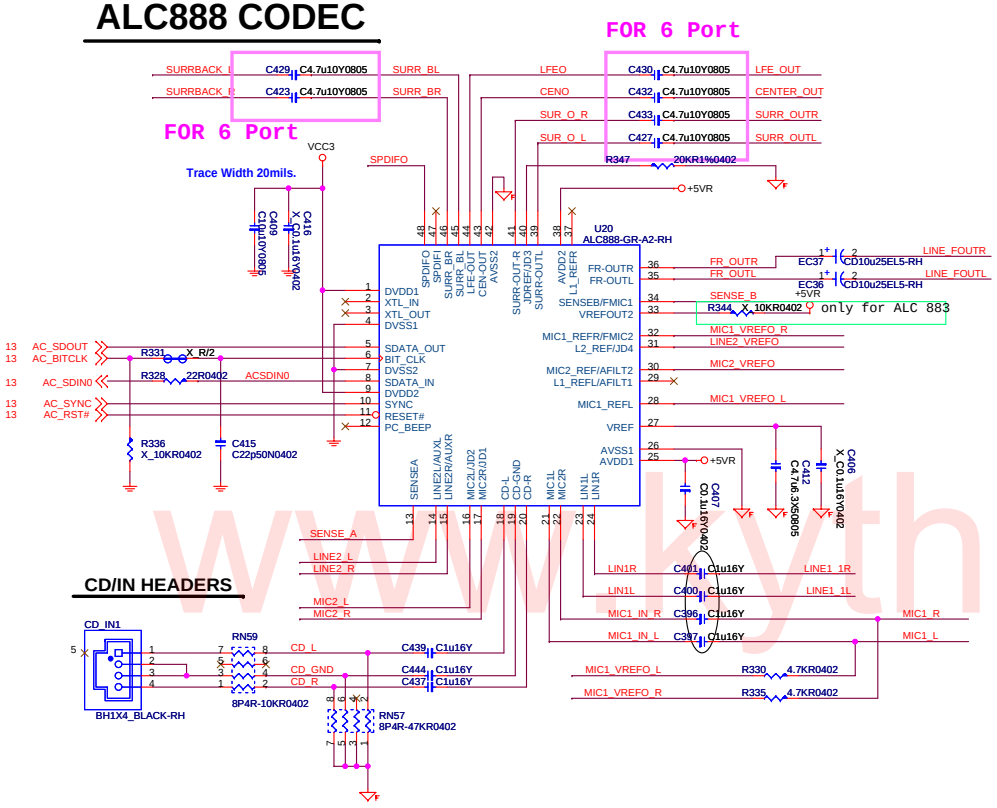
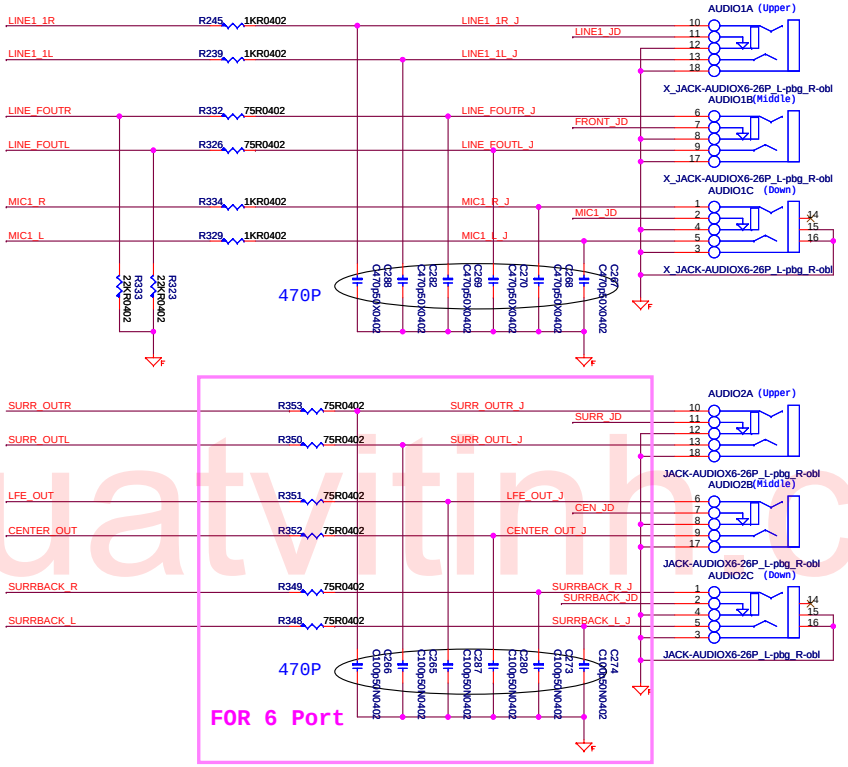
ALC888 CODEC

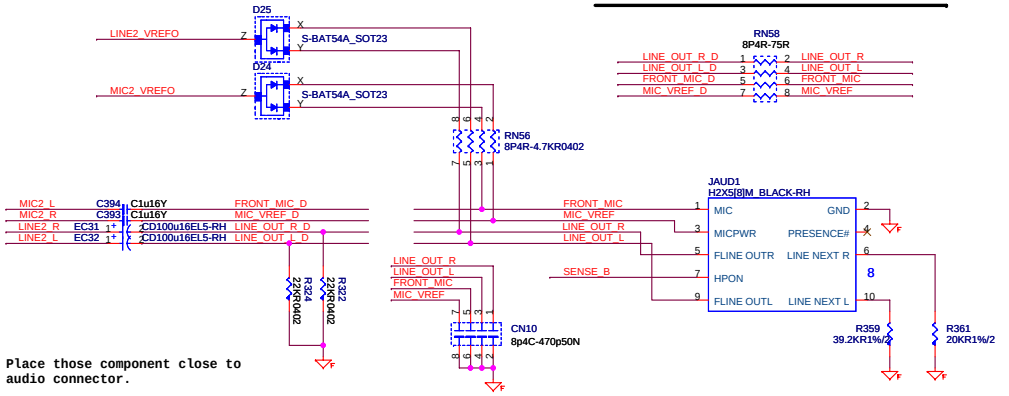


CD/IN HEADERS

ALC888 JACK

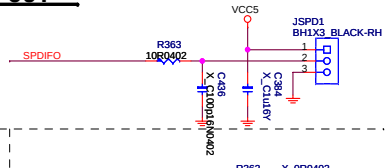


Azalia Front Audio Connector

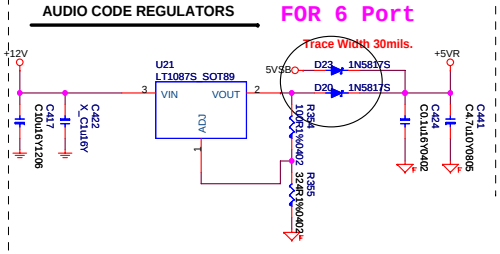


ALC883 JACK DETECT

SPDIF OUT



AUDIO CODE REGULATORS



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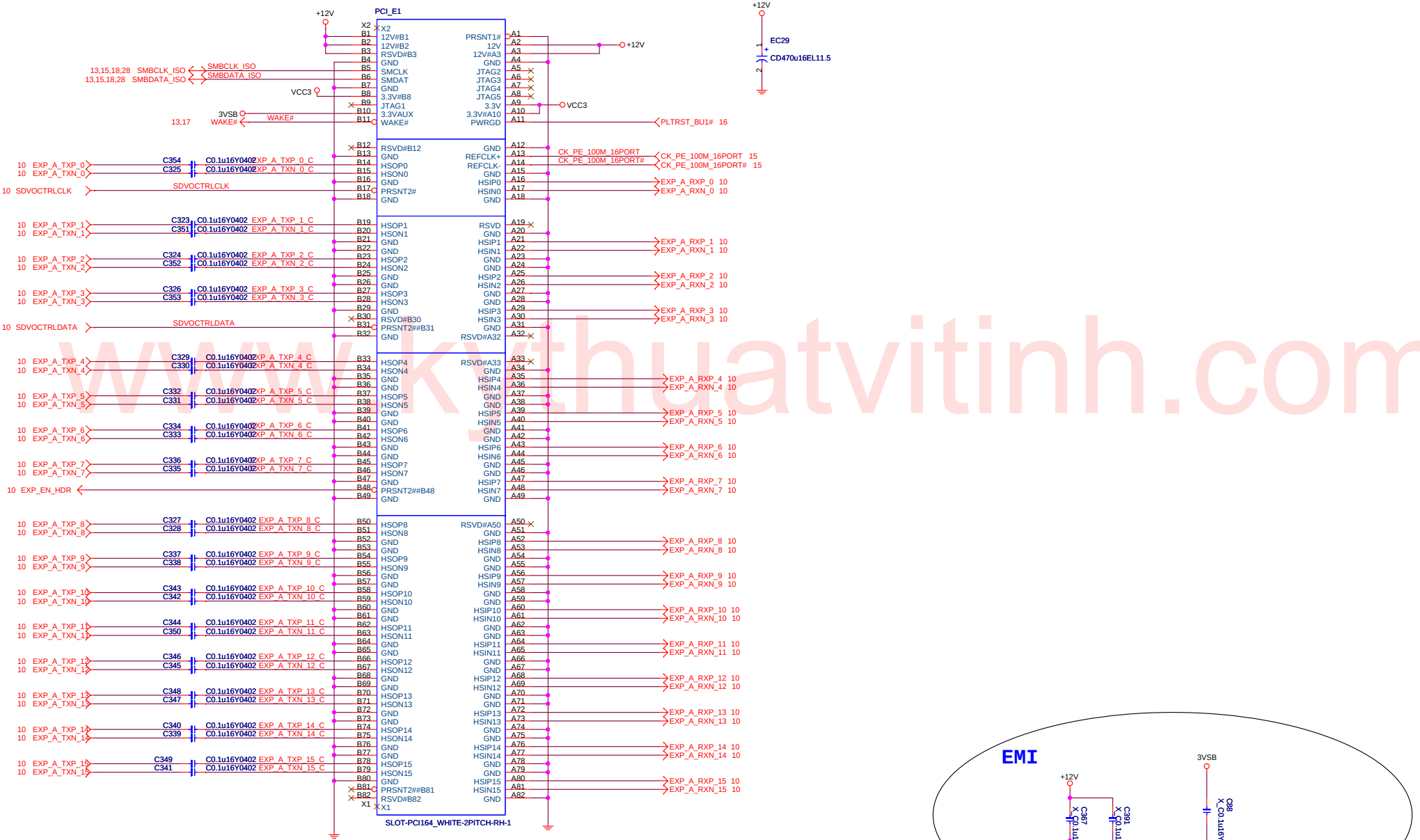
PCIE X16 PORT



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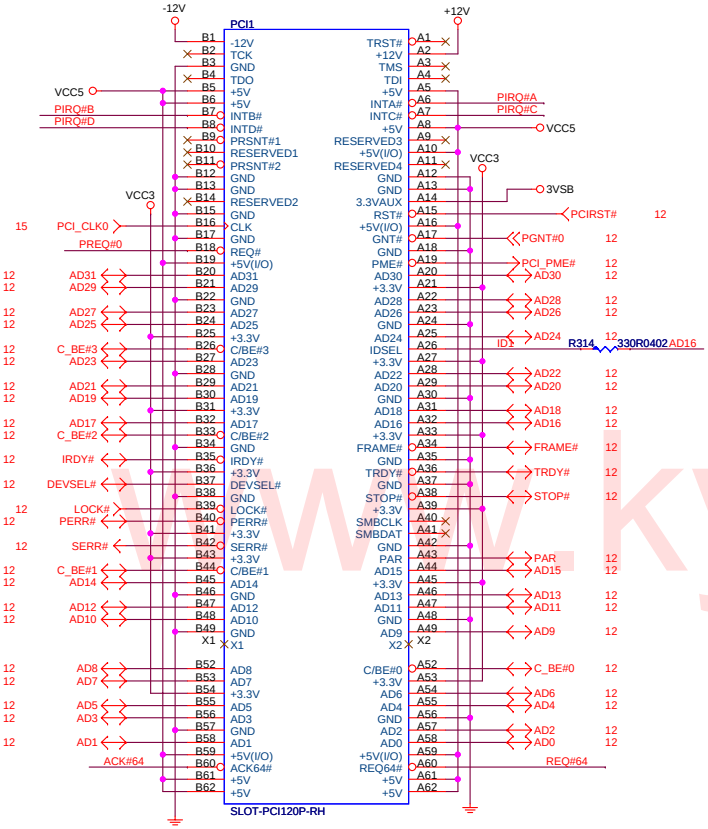
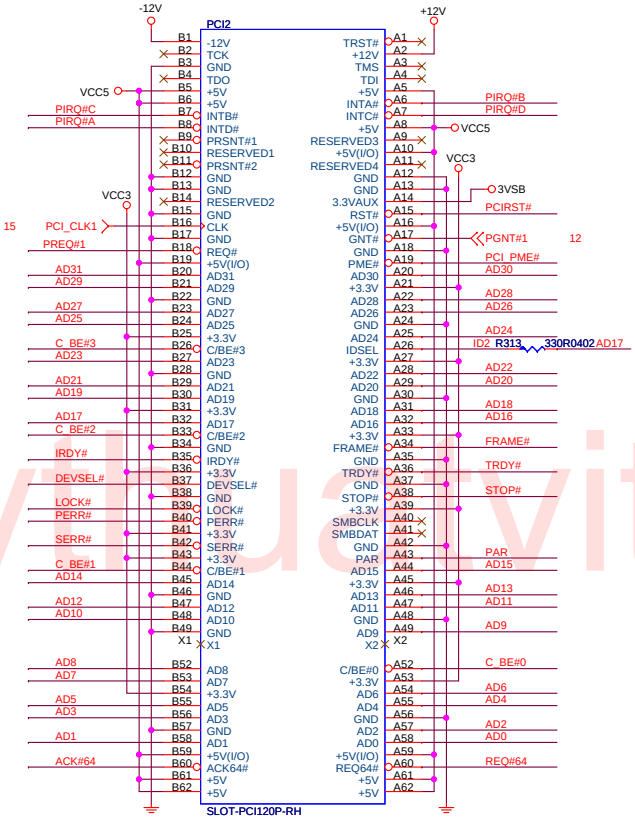
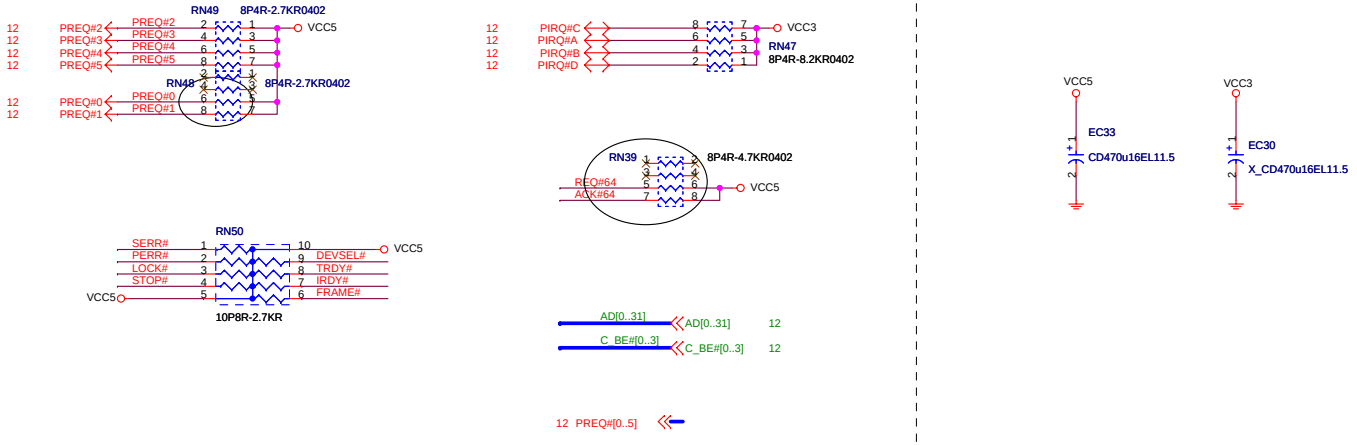
PCI SLOT 1 (PCI VER: 2.2 COMPLY)



PCI SLOT 2 (PCI VER: 2.2 COMPLY)



PCI PULL-UP / DOWN RESISTORS



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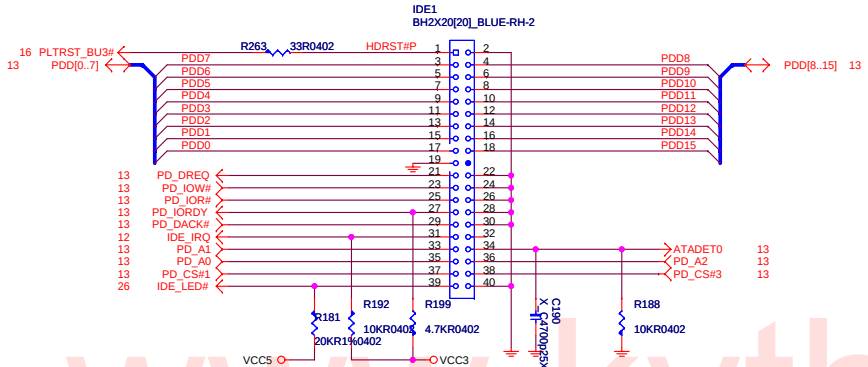
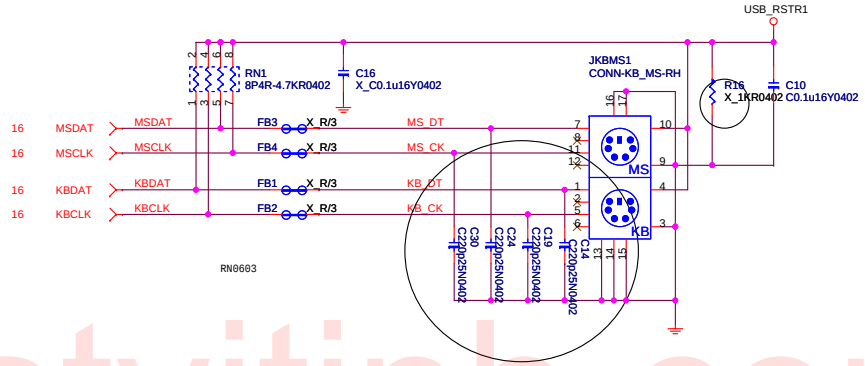
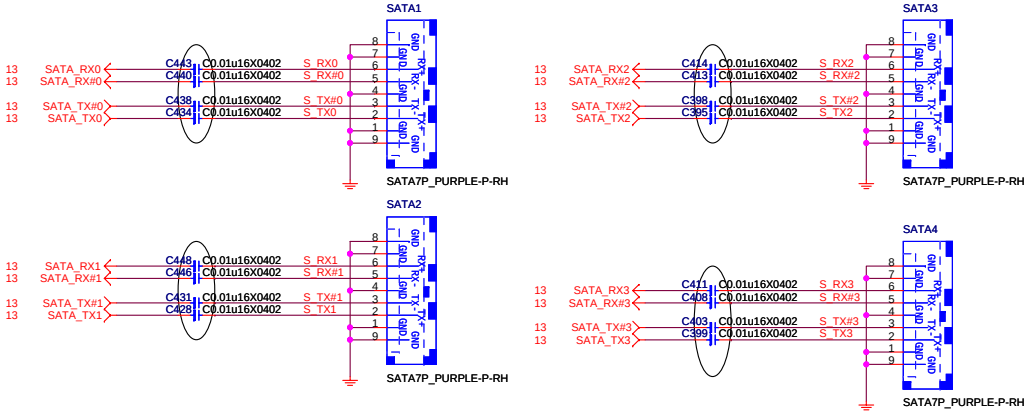
ATA 33/66/100 IDE Connectors



PS2 KEYBOARD & MOUSE CONNECTOR



SERIAL ATA CONNECTOR BLOCK



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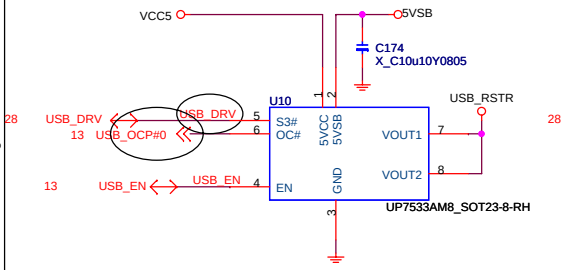
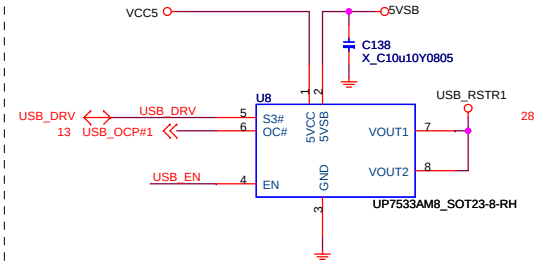
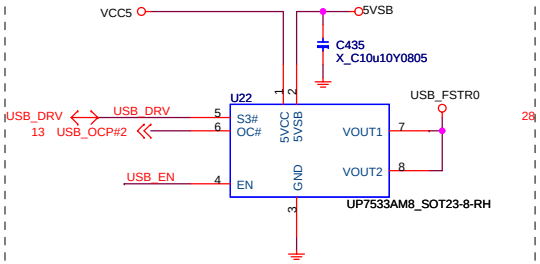
POWER CIRCUIT FOR USB PORT 0,1



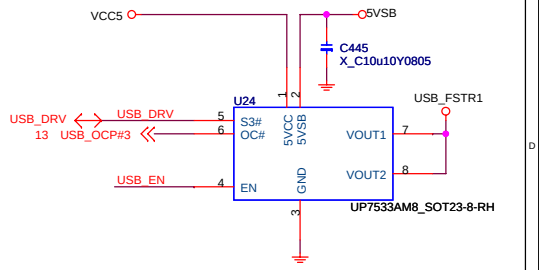
POWER CIRCUIT FOR USB PORT 2,3



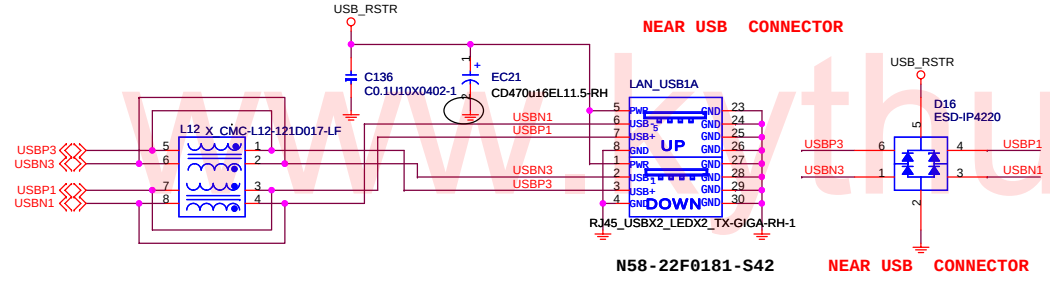
POWER CIRCUIT FOR USB PORT 4,5



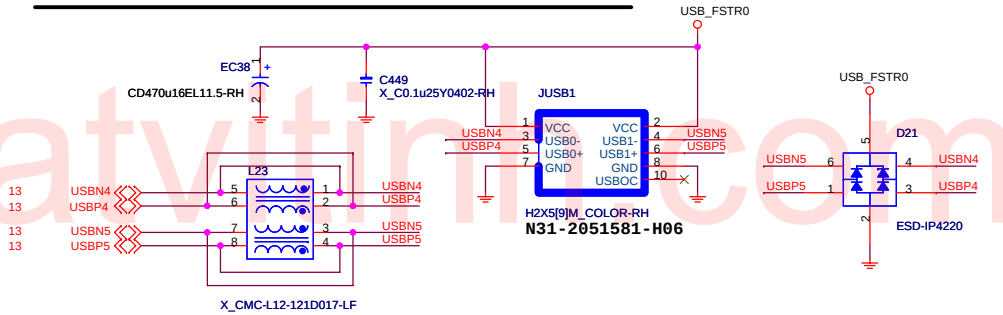
POWER CIRCUIT FOR USB PORT 6,7



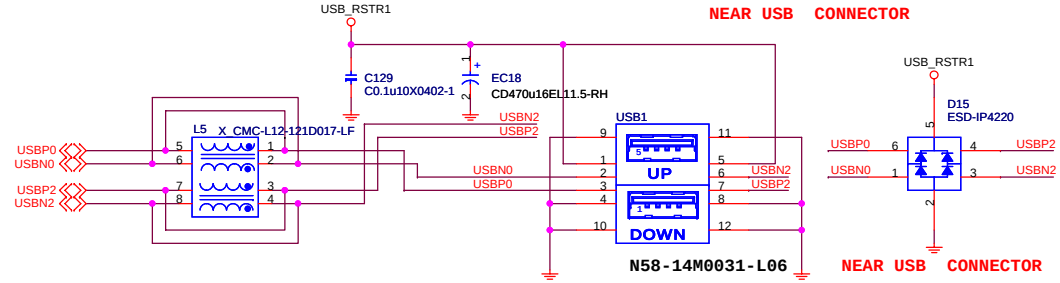
REAR PANEL USB CONNECTOR FOR USB PORT 0,1



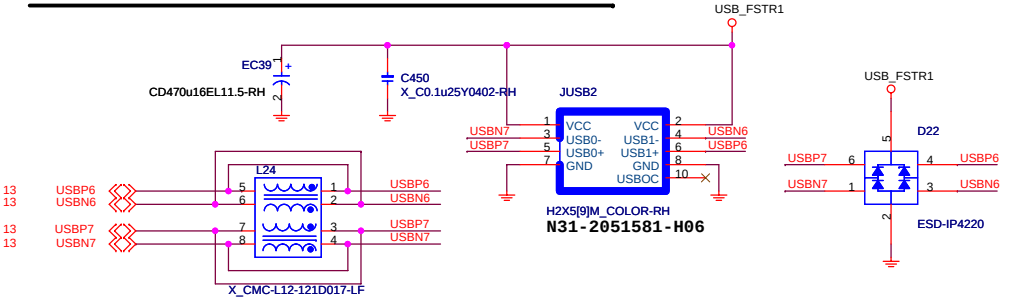
FRONT PANEL USB CONNECTOR FOR USB PORT 4,5



REAR PANEL USB CONNECTOR FOR USB PORT 2,3



FRONT PANEL USB CONNECTOR FOR USB PORT 6,7



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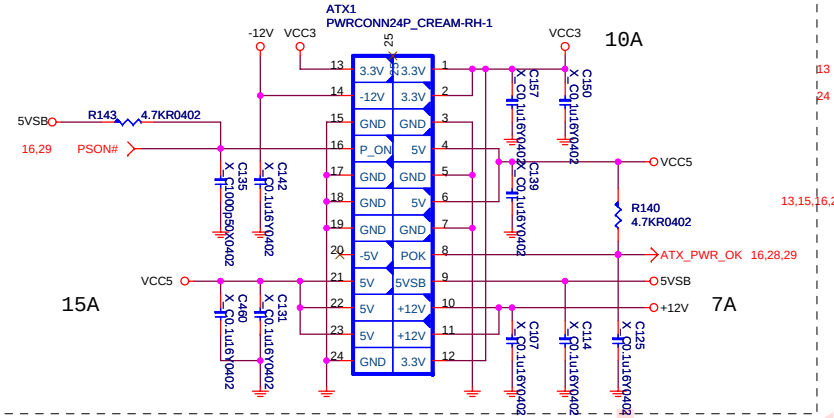
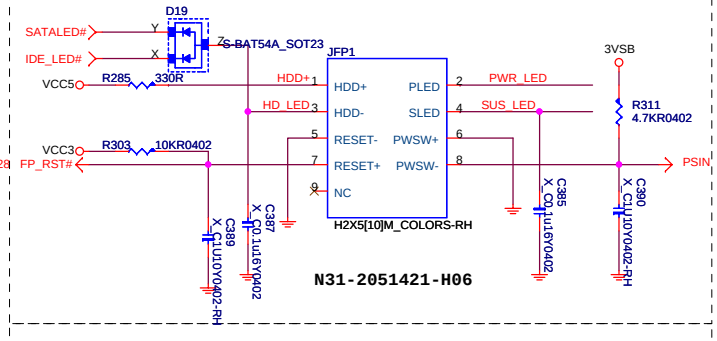
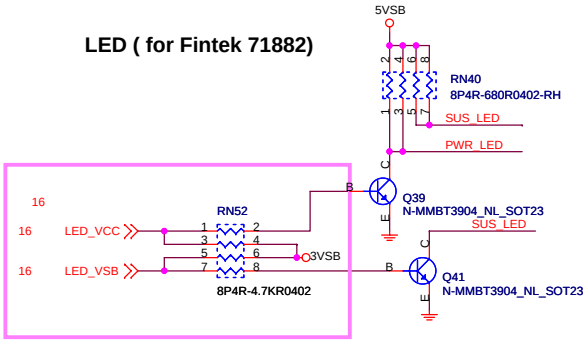
ATX Connector



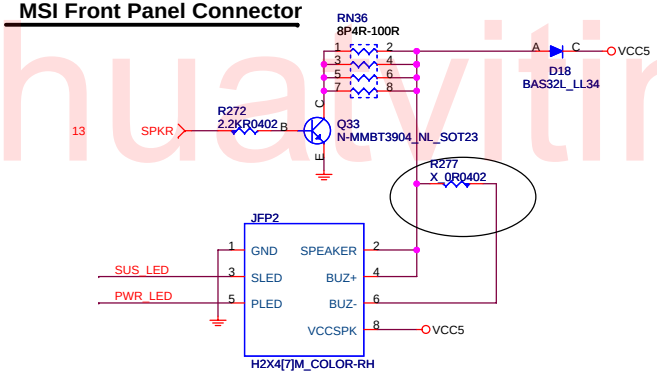
INTEL/PB Front Panel Connector



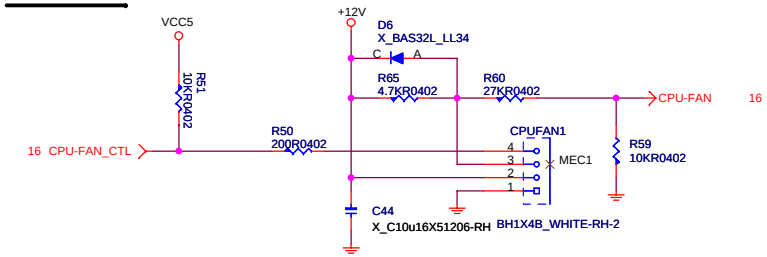
LED (for Fintek 71882)



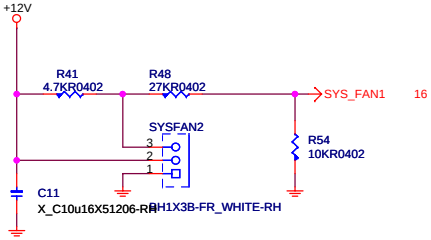
MSI Front Panel Connector



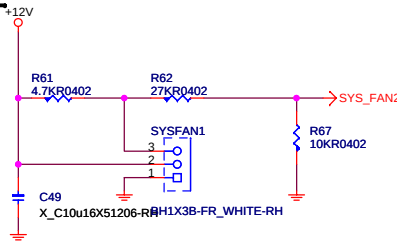
CPU FAN



SYSTEM FAN



PWR FAN



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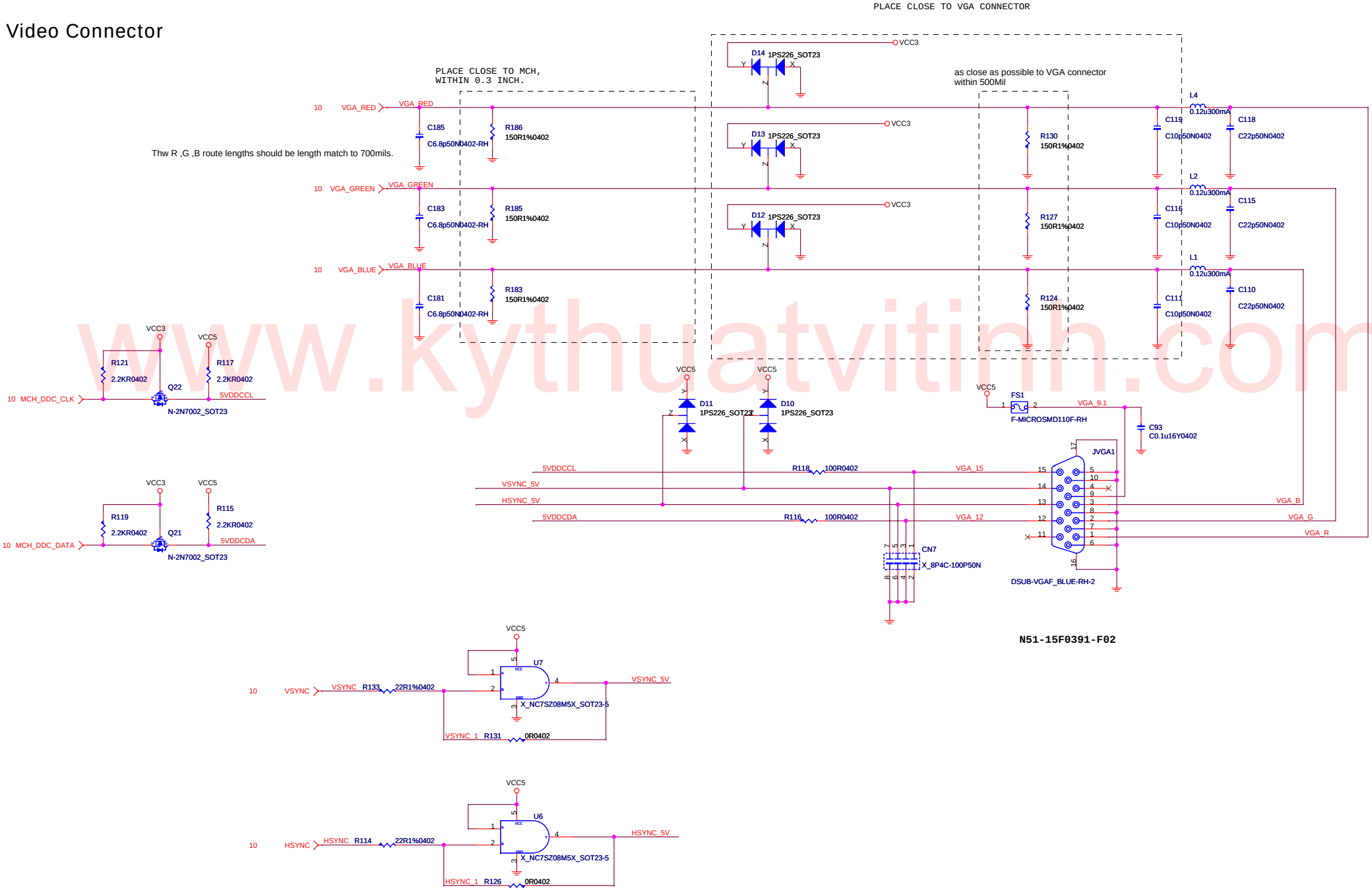
Video Connector



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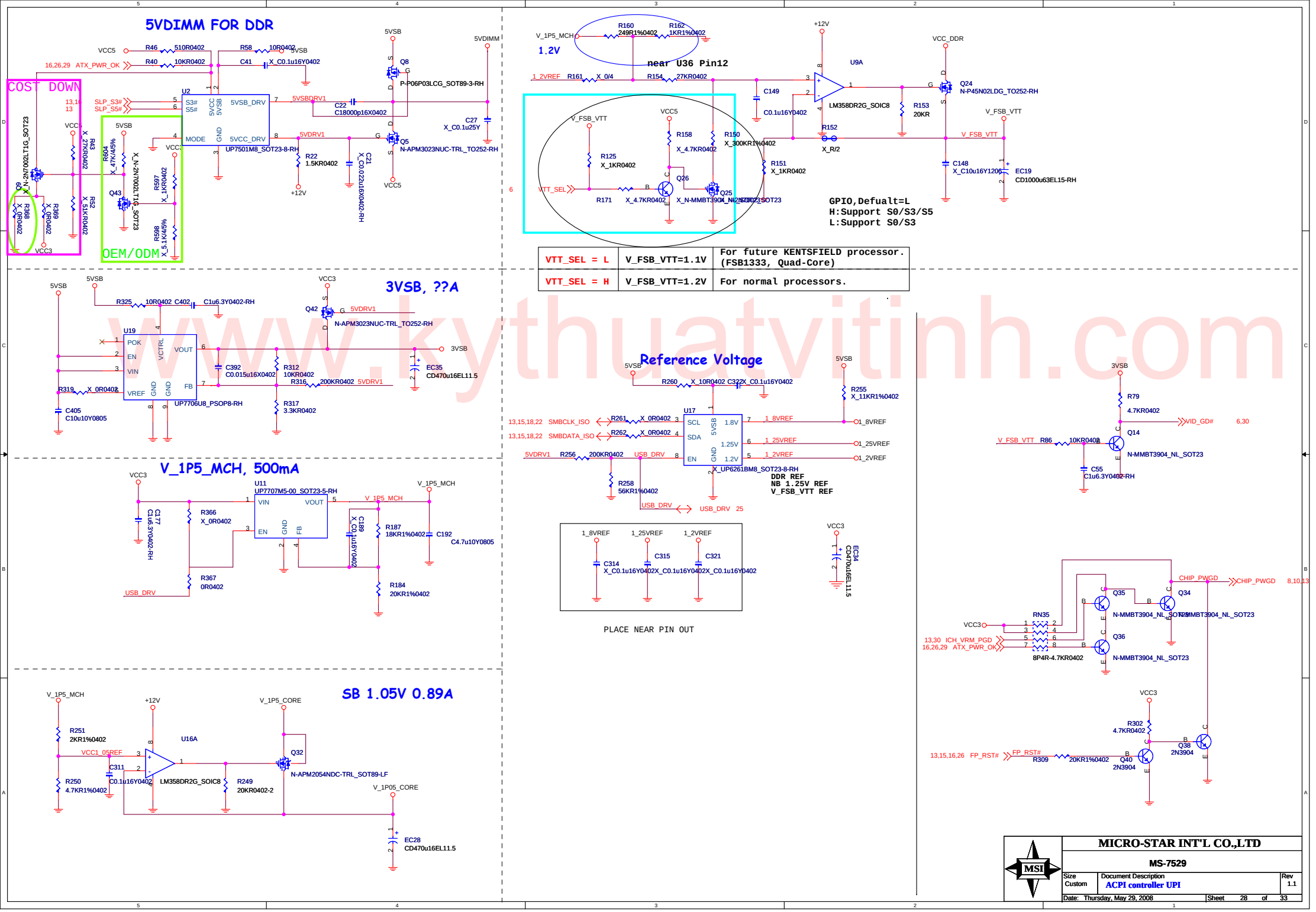
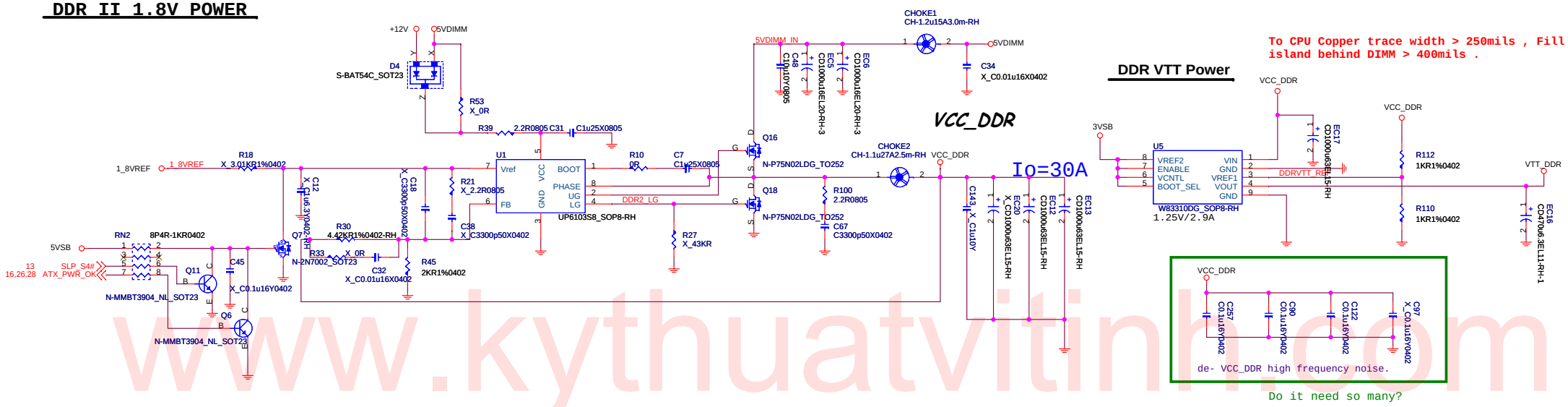
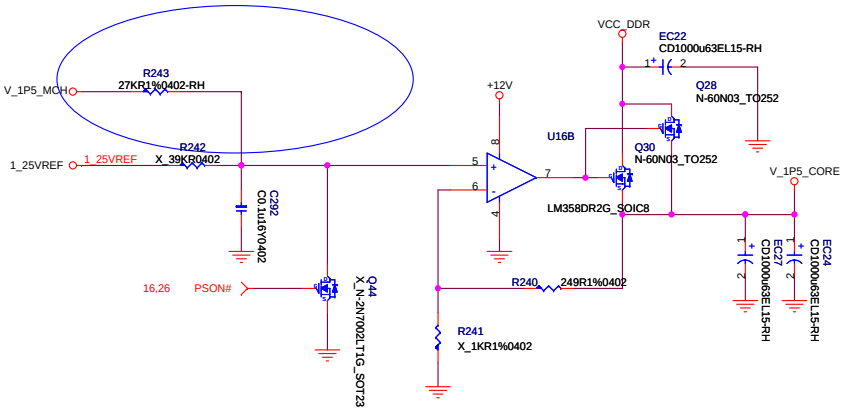


DDR II 1.8V POWER

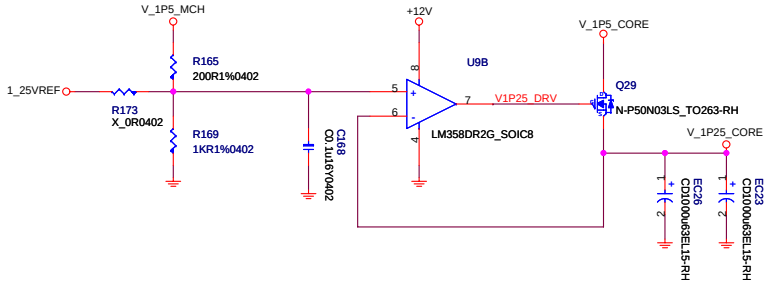


1.5V Core

For cost down



V_1P25_CORE 18.1A+2.47A+2.94A



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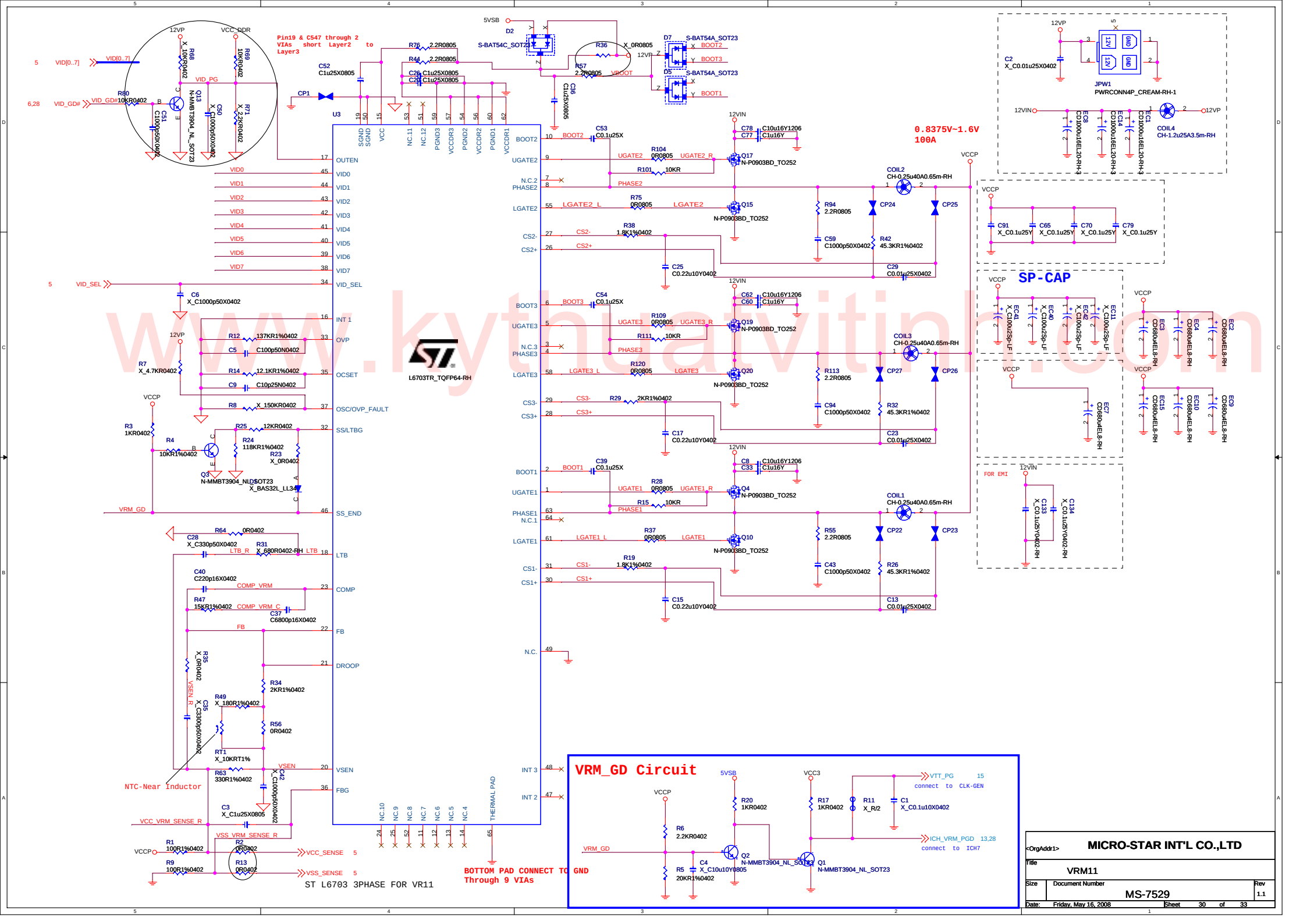
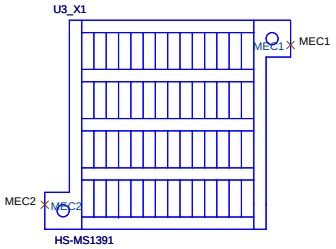
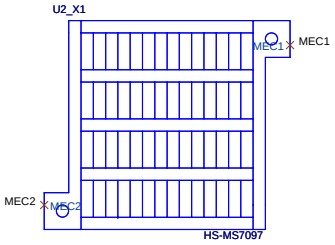

Pin19 & C547 through 2 VIAs short Layer2 to Layer3
L6703TR_TQFP64-RH
0.8375V~1.6V 100A
SP-CAP
VRM_GD Circuit
NTC-Near Inductor
ST L6703 3PHASE FOR VR11
BOTTOM PAD CONNECT TO GND Through 9 VIAs
MICRO-STAR INT'L CO.,LTD
VRM11
MS-7529
Friday, May 16, 2008

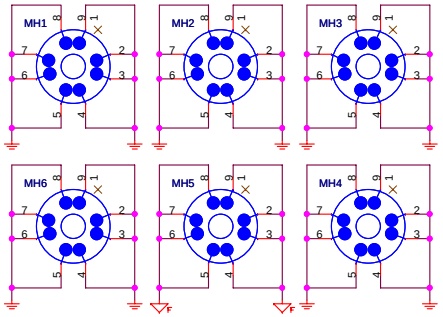
ICH7 HEATSINK



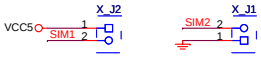
MCH HEATSINK



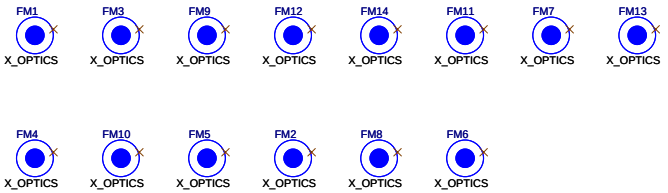
Mounting Holes



Simulation



Optics Orientation Holes



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ICH7

GPIO	Alt Func	PIN	I/O/NC	POWER	PU	SMI	TOL	DEFAULT	SIGNAL NAME
GPIO0	Unmultiplexed	AB18	I/O	CORE	N	Y	3.3V	GPI	GPI0(pull high)
GPIO1	REQ5#	C8	I/O	CORE	N	Y	5V	GPI	PREQ#5
GPIO2	PIRQE#	G8	I/OD	CORE	N	Y	5V	GPI	GPIO2(pull high)
GPIO3	PIRQF#	F7	I/OD	CORE	N	Y	5V	GPI	GPIO3(pull high)
GPIO4	PIRQG#	F8	I/OD	CORE	N	Y	5V	GPI	GPIO4(pull high)
GPIO5	PIRQH#	G7	I/OD	CORE	N	Y	5V	GPI	GPIO5(pull high)
GPIO6	Unmultiplexed	AC21	I/O	CORE	N	Y	3.3V	GPI	ATADET0
GPIO7	Unmultiplexed	AC18	I/O	CORE	N	Y	3.3V	GPI	STRAPPED HI
GPIO8	Unmultiplexed	E21	I/O	Resume	N	Y	3.3V	GPI	STRAPPED HI
GPIO9	Unmultiplexed	E20	I/O	Resume	N	Y	3.3V	GPI	STRAPPED HI
GPIO10	Unmultiplexed	A20	I/O	Resume	N	Y	3.3V	GPI	STRAPPED HI
GPIO11	SMBALERT#	B23	I/O	Resume	N	Y	3.3V	Native	STRAPPED HI
GPIO12	Unmultiplexed	F19	I/O	Resume	N	Y	3.3V	GPI	SIO_PME#
GPIO13	Unmultiplexed	E19	I/O	Resume	N	Y	3.3V	GPI	STRAPPED HI
GPIO14	Unmultiplexed	R4	I/O	Resume	N	Y	3.3V	GPI	STRAPPED HI
GPIO15	Unmultiplexed	E22	I/O	Resume	N	Y	3.3V	GPI	STRAPPED HI
GPIO16	Unmultiplexed	AC22	I/O	CORE	N	N	3.3V	GPO	NC
GPIO17	GNT5#	D8	I/O	CORE	N	N	3.3V	GPO	STRAPPED L
GPIO18	Unmultiplexed	AC20	I/O	CORE	N	N	3.3V	GPO	NC
GPIO19	SATA_1GP	AH18	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO20	Unmultiplexed	AF21	I/O	CORE	N	N	3.3V	GPO	NC
GPIO21	SATA_0GP	AF19	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO22	REQ4#	A13	I/O	CORE	N	N	3.3V	Native	STRAPPED HI
GPIO23	LDRQ_1#	AA5	I/O	CORE	N	N	3.3V	Native	STRAPPED HI
GPIO24	Unmultiplexed	R3	I/O	Resume	N	N	3.3V	GPO	NC
GPIO25	Unmultiplexed	D20	I/O	Resume	Y	N	3.3V	GPO	GPIO25(high 7507,low 7398)
GPIO26	Unmultiplexed	A21	I/O	Resume	N	N	3.3V	GPO	USB_EN
GPIO27	Unmultiplexed	B21	I/O	Resume	N	N	3.3V	GPO	NC
GPIO28	Unmultiplexed	E23	I/O	Resume	N	N	3.3V	GPO	NC
GPIO29	OC5#	C3	I/O	Resume	N	N	3.3V	GPI	USB_OCP#2
GPIO30	OC6#	A2	I/O	Resume	N	N	3.3V	GPI	USB_OCP#3
GPIO31	OC7#	B3	I/O	Resume	N	N	3.3V	GPI	USB_OCP#3
GPIO32	Unmultiplexed	AG18	I/O	CORE	N	N	3.3V	GPO	BIOS_WP#(fill with 1)
GPIO33	Unmultiplexed	AC19	I/O	CORE	N	N	3.3V	GPO	NC
GPIO34	Unmultiplexed	U2	I/O	CORE	N	N	3.3V	GPO	NC
GPIO35	SATACLKREQ#	AD21	I/O	CORE	N	N	3.3V	GPO	NC
GPIO36	SATA2GP	AH19	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO37	SATA3GP	AE19	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO38	Unmultiplexed	AD20	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO39	Unmultiplexed	AE20	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO48	GNT4#	A14	I/O	CORE	N	N	3.3V	Native	STRAPPED HI
GPIO49	CPUPWRGD	AG24	I/O	V_CPU_IO	N	N	V_CPU_IO	Native	H_PWRGD

Following are the GPIOs that need to be terminated properly if not used:
GPIO[39:36,23:21,19,7:0]: default as inputs and should be pulled up to Vcc3_3 if unused.
GPIO[31:29,15:8]: default as inputs and should be pulled up to VccSus3_3 if unused.

SIO Fintek71882FG(CONTINUE)

GPIO	Alt Func	PIN	Usage	Input/Output	NOTES
GPIO0	VIDOUT0	49	MCH_BSEL0	O12	
GPIO1	VIDOUT1	50	MCH_BSEL1	O12	
GPIO2	VIDOUT2	51	MCH_BSEL2	O12	
GPIO3	VIDOUT3	52	NC	O12	
GPIO4	VIDOUT4	53	NC	O12	
GPIO5	VIDOUT5/SIC	54	NC	I/OOD12t	
GPIO6	SLOTOCC#	55	GPO	I/OOD12t	
GPIO7	Turbo1#/WDTRST#	56	WDTRST#	OD12-5v	
GPIO15	LED_VSB/ALERT#	64	LED_VSB	OD12	
GPIO16	LED_VCC/Turbo2#	65	LED_VCC	OD12	
GPIO20	PCIRST1#	74	PCIRST1#	OD12	
GPIO21	PCIRST2#	75	PCIRST2#	O12	
GPIO22	PCIRST3#	76	PCIRST3#	O12	
GPIO23	RSTCON#	77	RSTCON#	OD12	
GPIO24	ATXPG_IN	78	ATXPG_IN	AIN	
GPIO32	PWROK	84	PWROK	OD12	
GPIO26	PWSIN#	80	PWSIN#	INts5v	
GPIO27	PWSOUT#	80	PWSOUT#	OD12	
GPIO30	S3#	82	S3#	INts5v	
GPIO31	PSON#	83	PSON#	OD12-5v	
GPIO33	RSMRST#	85	RSMRST#	OD12	
GPIO40	FANIN3	25	FANIN3	INts5v	
GPIO41	FAN_CTL3	26	FAN_CTL3(NC)	OD12-5v	
GPIO25	PME#	79	PME#	OD12-5v	
GPIO10	SPI_SLK/FANIN4	59	GPIO10(NC)	I/OOD12t	
GPIO11	SPI_CS0#/FANCTL4	60	GPIO11(NC)	I/OOD12t	
GPIO12	SPI_MISO/FANCTL1_1	61	GPIO12(NC)	I/OOD12t	
GPIO13	SPI_MOSI/BEEP	62	BEEP(NC)	OD24	
GPIO14	FWH_DIS/WDTRST#/SPI_CS1#	63	GPIO14	I/OOD12t	
GPIO42	IRTX	27	IRTX	O12	
GPIO43	IRRX	28	IRRX	INts	
GPIO17		66	NC	I/OOD12t	

PCI Config.

DEVICE	MCP1 INT PIN	REQ#/GNT#	IDSEL	CLOCK
PCI1	PIRQ#A PIRQ#B PIRQ#C PIRQ#D	PREQ#0 PGNT#0	AD16	PCI_CLK0
PCI2	PIRQ#B PIRQ#C PIRQ#D PIRQ#A	PREQ#1 PGNT#1	AD17	PCI_CLK1

DDRII DIMM Config.

DEVICE	ADRRESS	CLOCK
DIMM A	A0H	P_DDR0_A/N_DDR0_A P_DDR1_A/N_DDR1_A P_DDR2_A/N_DDR2_A
DIMM B	A4H	P_DDR0_B/N_DDR0_B P_DDR1_B/N_DDR1_B P_DDR2_B/N_DDR2_B

JCI1	*Chassis Intrusion*
Open	Normal
(1-2)	Chassis Open

JUMPER SETTING		
JBAT1	(1-2)NORMAL	(2-3)CLEAR

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0A Change list:

1. Add DMI Audio net name
2. Change LED Power pull high to 680 Change r20 to 1.5K
3. Change D10 D11 Power pull VCC5, Q20 Pull up VCC3
4. Delet R252 R254 C132 R22 C60,change U5 to I95-7523212-T07
5. Modify footprint : C_P3_5_D8_H9 NC_0402_6 NC_0603_10 C0805MSB C0603MS_BOT
6. Swap RN65 RN61 RN23 RN64 RN63 RN24 RN28 RN25 RN66 ; Delet EC20,
7. Add 5VCC TO 3VCC sequence
8. change TESTPIN30 to TPC20B
9. RENAME ,Swap RN37, X_J1 Change to GND , Change C300 C301 to 0.22UF
10. Modify V_1P25_CORE to G31

1.0 Change list:

1. U11 EN(pin3)change to USB_DRV
2. Add SIO pin55 SKTOCC# pull up to 3vsb
3. Swap RN26
4. add Control UP7501 power seqence

Title: History		
Size: Custom	Document Number: MS-7529	Rev: 1.1
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