LED Driver IC

IK2102

Description

The IK2102 are cathode-grid LED display drives with output size - 4 digits x13 segments or 7 digits x 10 segments and addition key scan function.
Serial interface provide connection with microprocessor.

Features

- Wide operation Voltage : 3.0V ~ 5.5V
- Display Size : PKG option
- 8-Step Dimming Circuitry
- Process Rate : 500kHz with
- OSC: built in (with external resistor)
- Pulse Segment Current: 10mA type (8mA – 12mA) @ V_{DD}= 3.3V – 5.5V
- Pulse Segment Current: 20mA type (16mA – 24mA) @ V_{DD}= 5.0V
- Key scanning: 10x2 matrix
- Serial Interface
- Operation Temperature : -40 ~ 85°C
- PKG option
  IK2102 (28Pins) : 4 digits x13 segments
  to 7 digits x 10 segments with key scan function

IK2102DW
SOP-28

IK2102TSD
TSSOP-28

Ta=-40 ~ 85℃
For all package

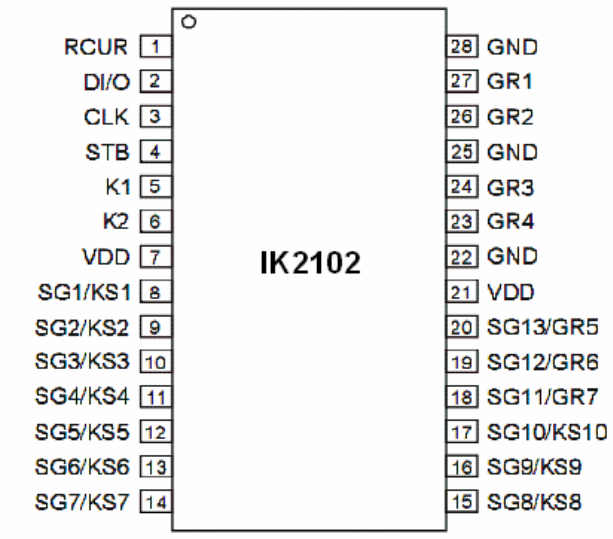
Application

- Micro-computer Peripheral Device
- VCR set
- DVD Combo set
- DMB Player

ORDERING INFORMATION

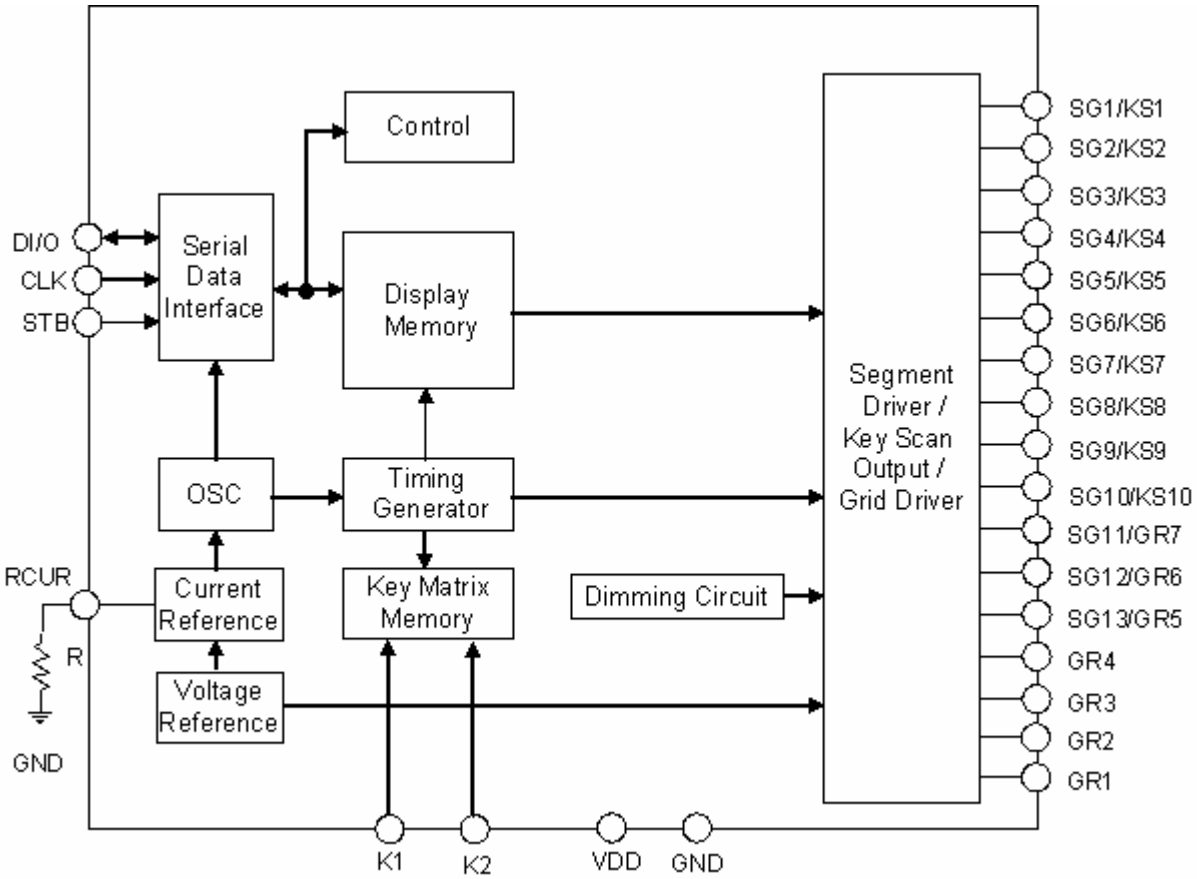
Device	Operating Temperature Range	Package	Shipping
IK2102DW	T_A = -40° to 85° C	SOP 28	tube
IK2102TSD		TSSOP 28	tube

Pin Description IK2102 (28Pins)



Pin Name	I/O	Description	Pin No.
RCUR	I	A resistor is connected to this pin to determine the output currents and oscillation frequency.	1
DI/O	I/O	Data Input - Output Pin This pin inputs serial data at the rising edge of the shift clock (starting from the bit) Data Output Pin - N-Channel, Open-Drain This pin outputs serial data at the falling edge of the shift clock	2
CLK	I	Clock Input Pin This pin reads serial data at the rising edge and output data at the falling edge.	3
STB	I	Serial Interface Strobe Pin The data input after the STB has fallen is processed as a command. When this pin is HIGH, CLK is ignored.	4
K1 to K2	I	Key Data Input Pins The data sent to these pins are latched at the end of the display cycle. (Internal Pull-Low Resistor)	5, 6
VDD	-	Power Supply	7, 21
SG1/KS1 to SG10/KS10	O	Segment Output Pins (P-Channel, Open Drain) Also acts as the Key Source	8 ~ 17
SG11/GR7 to SG13/GR5	O	Segment / Grid Output Pins	18 ~ 20
GND	-	Ground Pins	22, 25, 28
GR4 to GR1	O	Grid Output Pins	23, 24, 26, 27

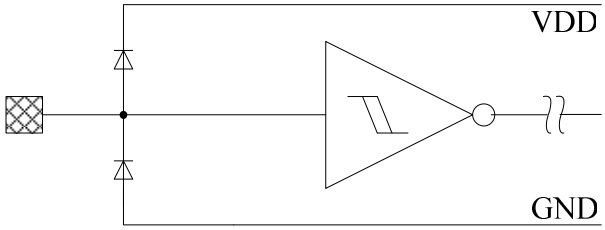
BLOCK DIAGRAM



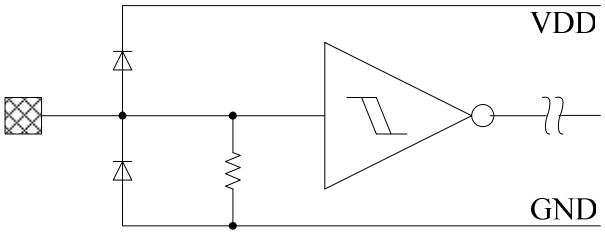
INPUT / OUTPUT CONFIGURATIONS

The schematic diagrams of the input and output circuits of the logic section are shown below.

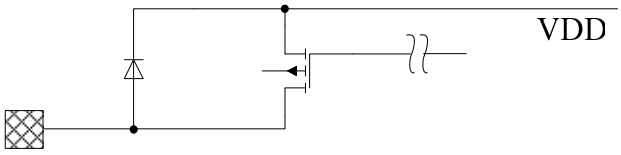
Input Pins: CLK, STB & DIN



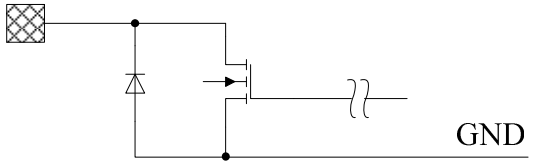
Input Pins: K1, K2



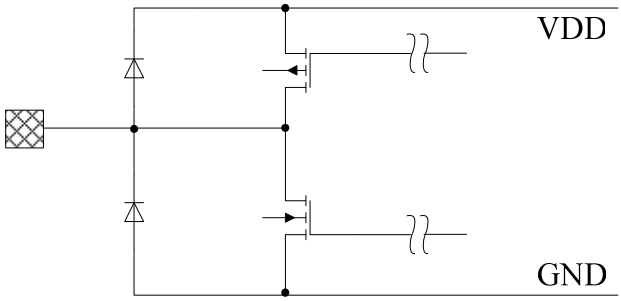
Input Pins: RCUR, SG1 to SG11



Output Pins: DOUT, GR1 to GR4



Output Pins: SG12_GR7, SG13_GR6 & SG12_GR5



FUNCTIONAL DESCRIPTION

Commands

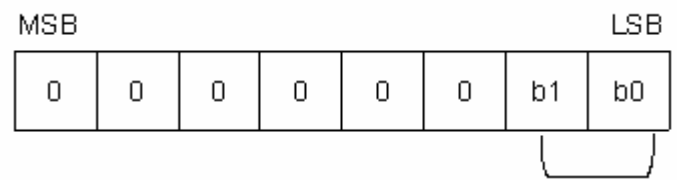
A command is the first byte (b0 to b7) inputted to IK2102 via DIN, DI/O Pin after STB Pin has changed From ”HIGH” to “LOW” state. If for some reason the STB Pin is set “HIGH” while data or commands Are being transmitted, the serial communication is initialized, and the data/ commands being transmitted are considered invalid.

COMMAND 1 : DISPLAY MODE SETTING COMMANDS

IK2102 provides 4 display mode setting as shown in the diagram below: As stated earlier a command is the first one byte(b0 to b7) transmitted to IK2102 via the DIN, DI/O Pin when STB is “LOW”. However, for these commands, Bit 3 & Bit 8 (b2 to b7) are given a value of “0”.

The Display Mode Setting Commands determine the number of segments and grids be used (14 to 9 segments, 4 to 7 grids). A display command “ON” must be executed in order to resume display. If the same mode setting is selected, no command execution is take place, therefore, nothing happens.

When Power is turned “ON”, the mode 11 is selected.

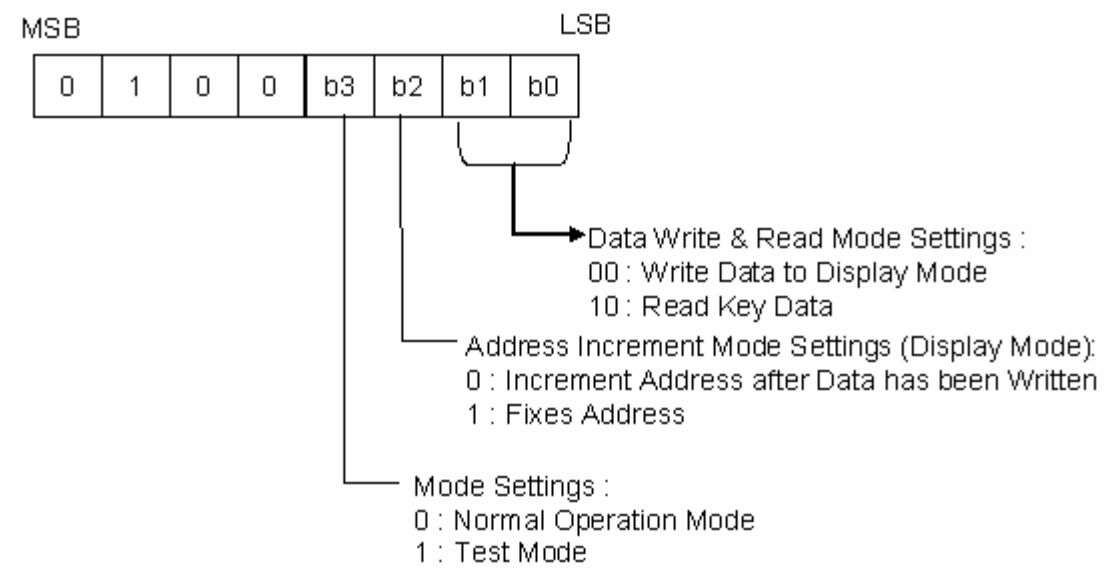


Display Mode Settings :
00 : 4 Grids, (13 Segments-28pin)
01 : 5 Grids, (12 Segments-28pin)
10 : 6 Grids, (11 Segments-28pin)
11 : 7 Grids, (10 Segments-28pin)

COMMAND 2 : DATA SETTING COMMANDS

The Data Setting Commands executes the Data Write Mode for IK2102. The Data Setting Command, the bits5 and 6 (b4, b5) are given the value of “0”. , bit7 (b6) is given the value of “1” while bit8 (b7) is given the value of “0”. Please refer to the diagram below.

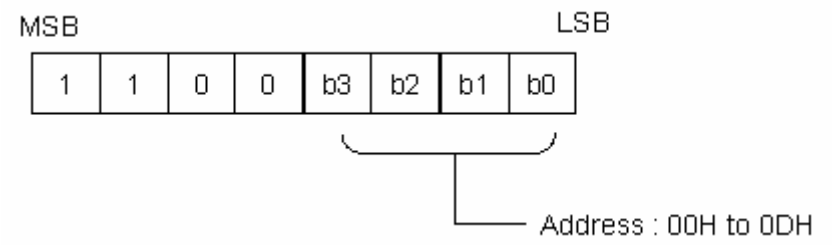
When power is turned ON, bit 4 to bit 1 (b3 to b0) are given the value of “0”.



COMMAND 3 : ADDRESS SETTING COMMANDS

Address Setting Commands are used to set the address of the display memory. The address is considered valid if it has a value of “00H” to 0DH”. If the address is set to 0EH or higher, the data is ignored until a valid address is set. When power is turned ON, the address is set at “00H”.

Please refer to the diagram below.



Display Mode and RAM Address

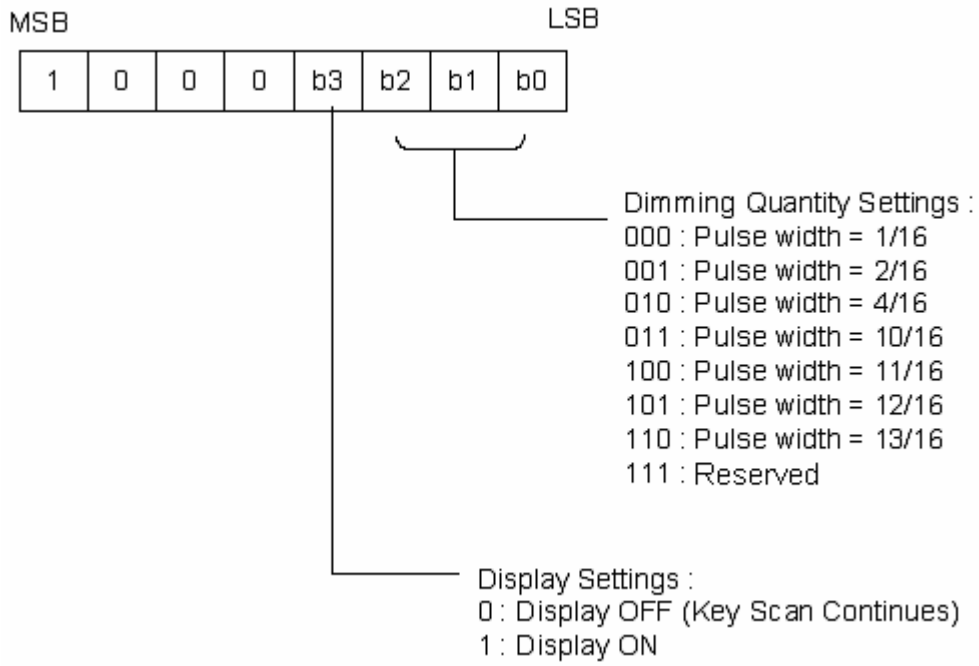
Data transmitted from an external device to IK2102 via the serial interface are stored in the Display RAM and are assigned addresses. The RAM Addresses of IK2102 are given below in 8 bit unit.

SG1	SG4 SG5	SG8 SG9	SG12 SG13	
00HL	00HU	01HL	01HU	DIG1
02HL	02HU	03HL	03HU	DIG2
04HL	04HU	05HL	05HU	DIG3
06HL	06HU	07HL	07HU	DIG4
08HL	07HU	09HL	09HU	DIG5
0AHL	0AHU	0BHL	0BHU	DIG6
0CHL	0CHU	0DHL	0DHU	DIG7

b0 b3	b4 b7
xxHL	xxHU
Lower 4 bits	Higher 4 bits

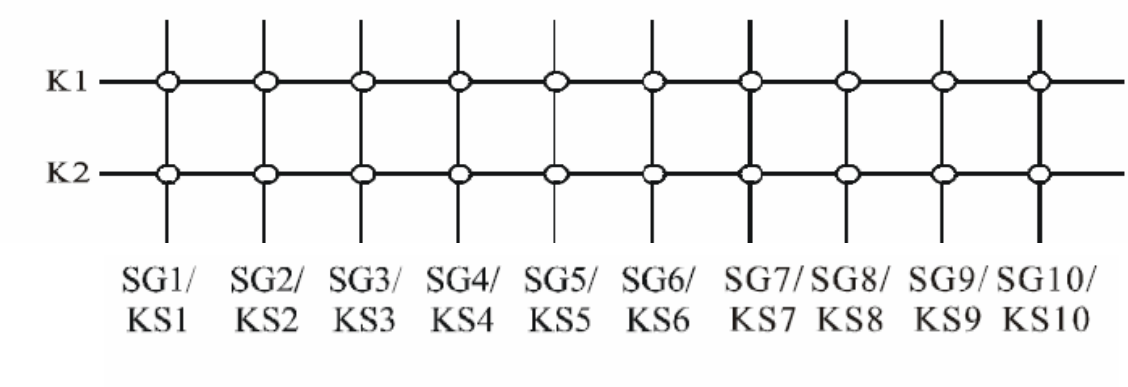
COMMAND 4 : DISPLAY CONTROL COMMANDS

The Display Control Commands are used to turn ON or OFF a display. It also used to set the pulse width. Please refer to the diagram below. When the power is turned ON, a 1/16 pulse width is selected and the displayed is turned OFF.

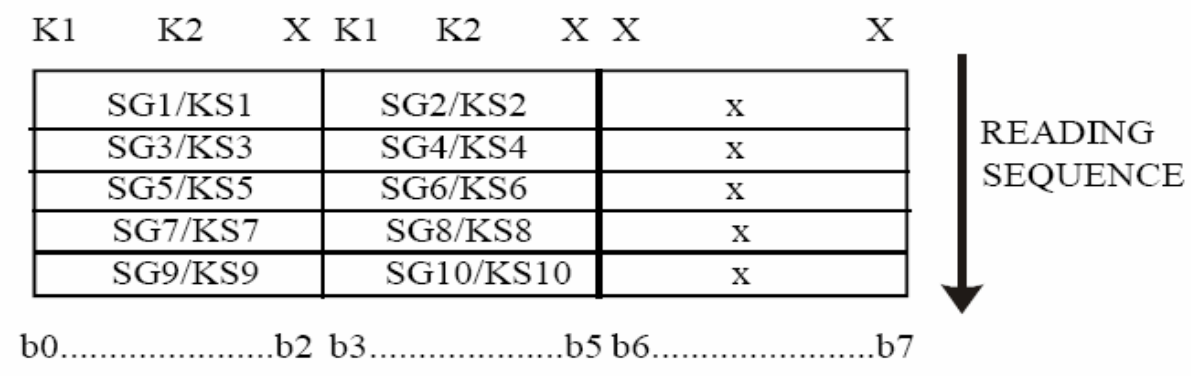


KEY MATRIX & KEY INPUT DATA STOREGE RAM

Key Matrix consists of 10 x 2 array as shown below:

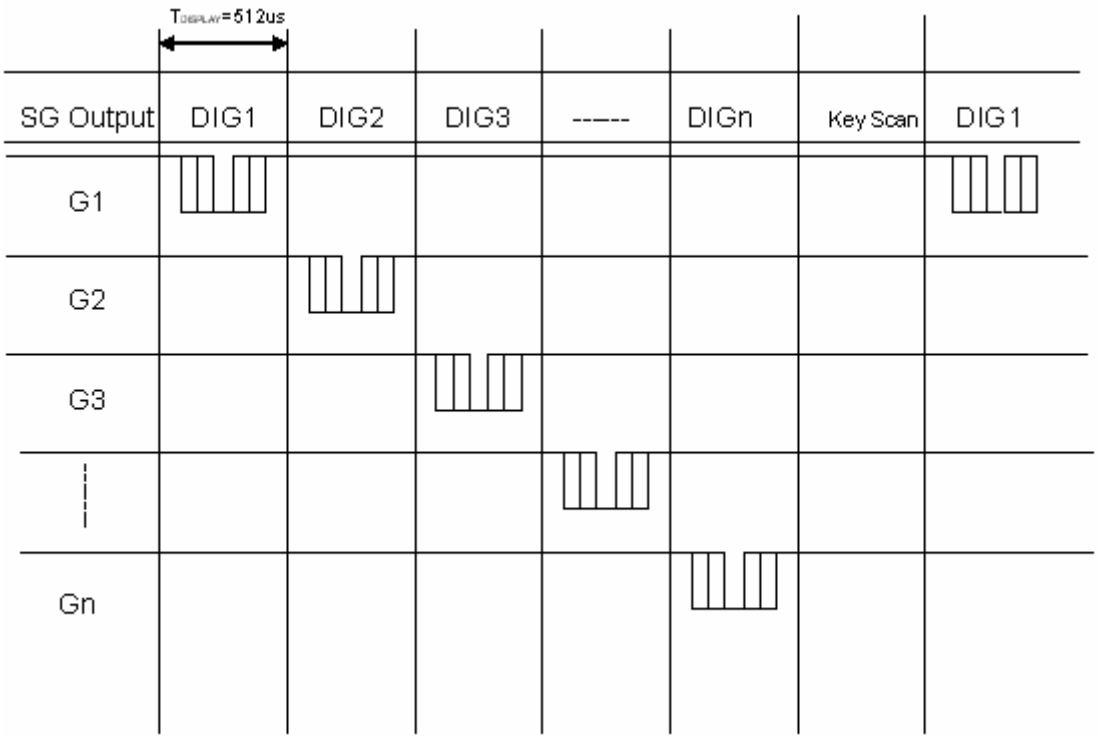


Each data entered by each key (or any combination of keys) is stored as follows and read by a READ Command, starting from the last significant bit. When the most significant bit of the data (b0) has been read, the least significant bit of the next data (b7) is read.



Note: b2, b5, b6 and b7 do not care.

SCANNING AND DISPLAY TIMING

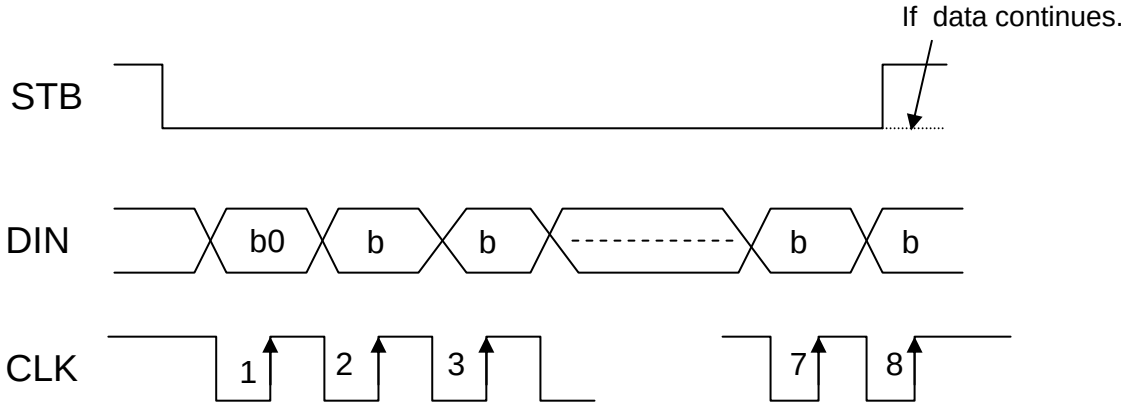


1 Frame = Tdisplay x (n+1)

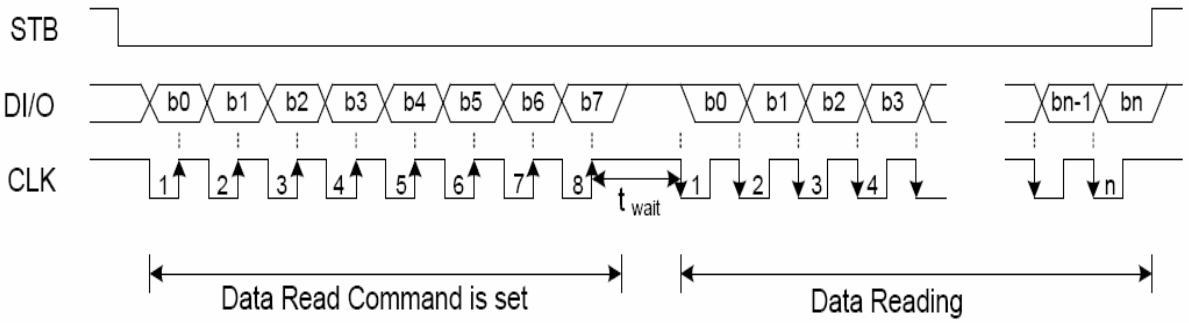
SERIAL COMMUMICATION FORMAT

The following diagram shows the serial communication format.

Reception (Data/Command Write)



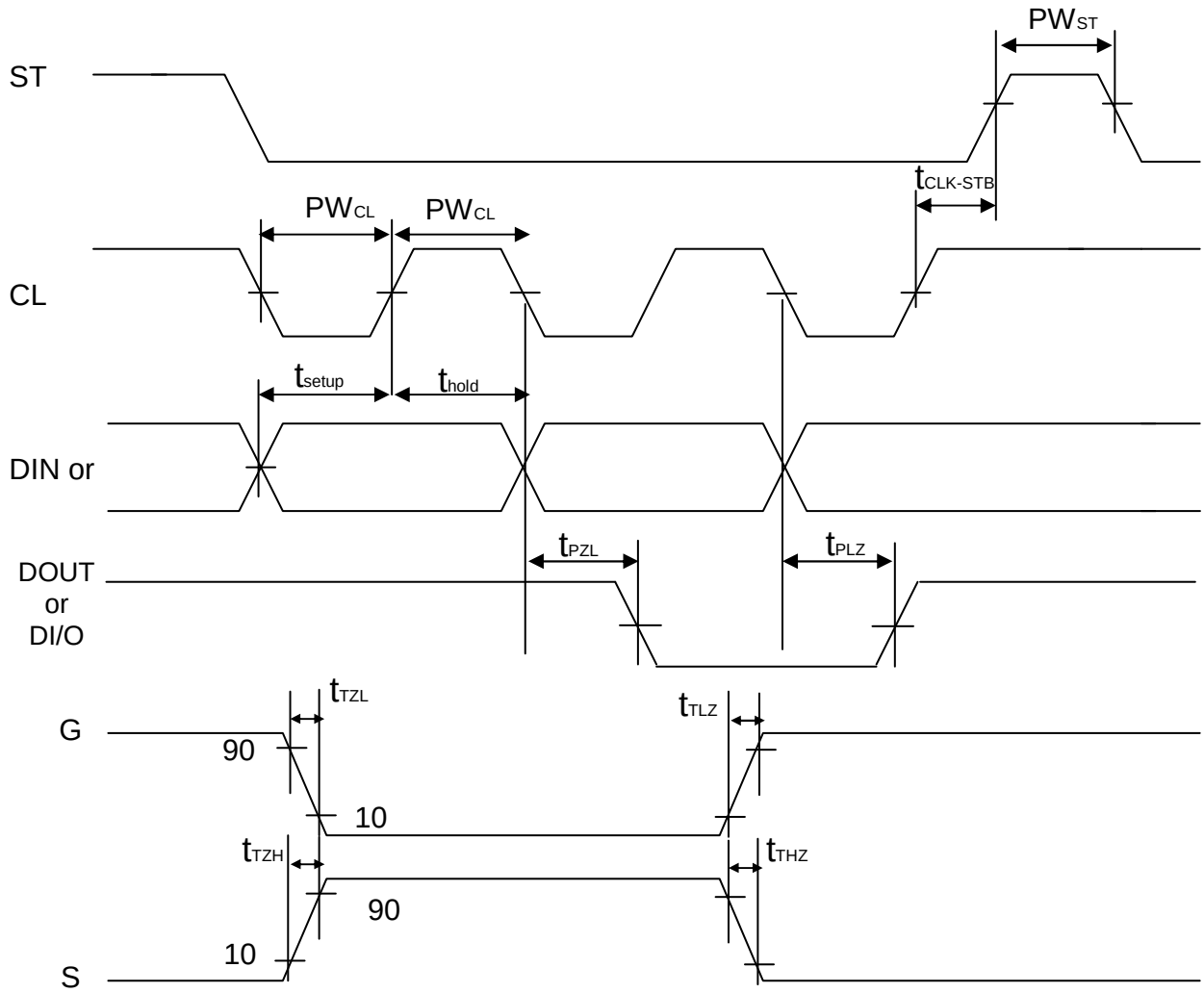
Transmission (Data Read)



Where: t_{wait} (waiting time) ≥ 1μs

SWITCHING CHARACTERISTIC WAVEFORM

Switching Characteristics Waveform is given below.

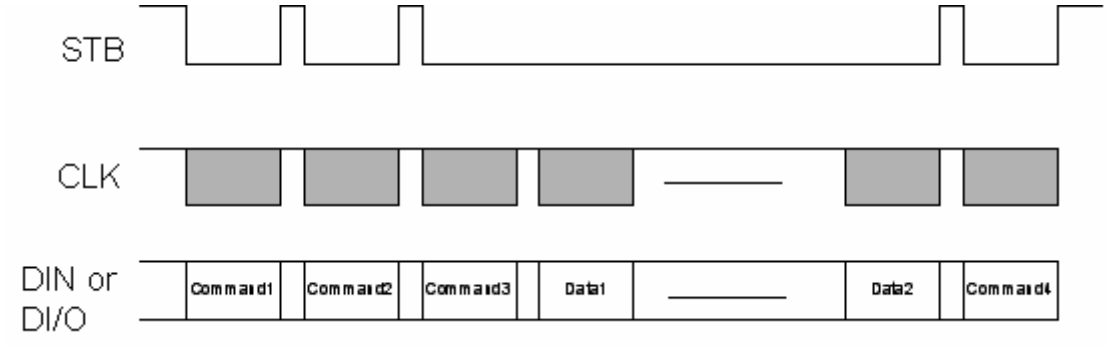


PW $_{CLK}$ (Clock Pulse Width) ≥ 400ns
t setup (Data Setup Time) ≥ 100ns
t $_{CLK-STB}$ (Clock - Strobe Time) ≥ 1㎲
t $_{TZH}$ (Rise Time) ≤ 1㎲
t $_{TZL}$ <1㎲

PW$_{STB}$ (Strobe Pulse Width) ≥ 1㎲
thold (Data Hold Time) ≥ 100ns
t $_{THZ}$ (Fall Time) ≤ 10㎲
fosc = Oscillation Frequency
t $_{TIZ}$ <10㎲

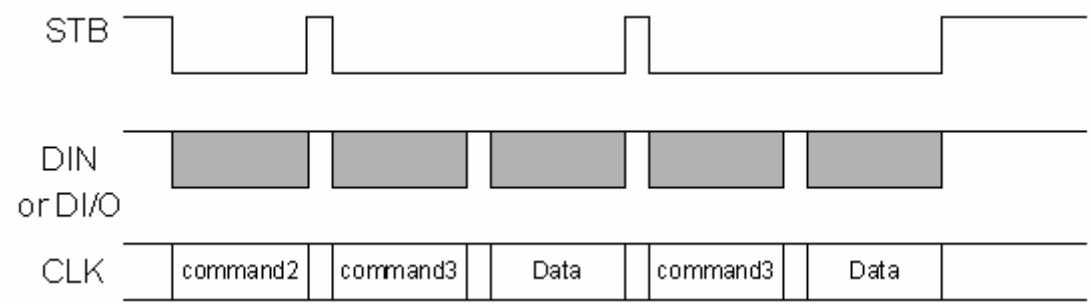
APLICATIONS

Display memory is updated by incrementing addresses. Please refer to the following diagram.



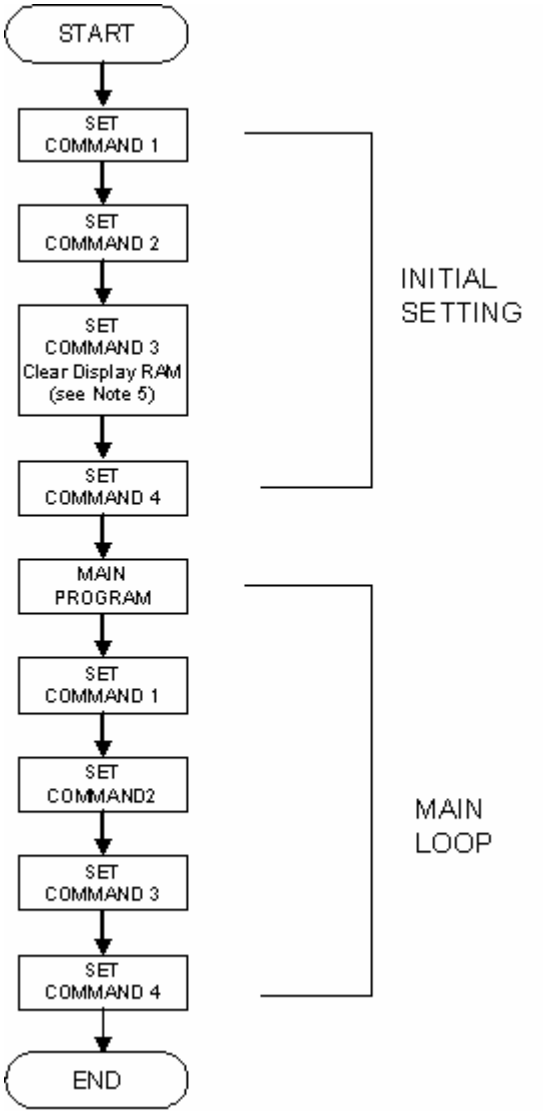
Where : Command 1 : Display Mode Setting
Command 2 : Data Setting Command
Command 3 : Address Setting Command
Data 1 to n : Transfer Display Data (14 Bytes max.)
Command 4 : Display Control Command

The following diagram shows the waveforms when updating specific addresses.



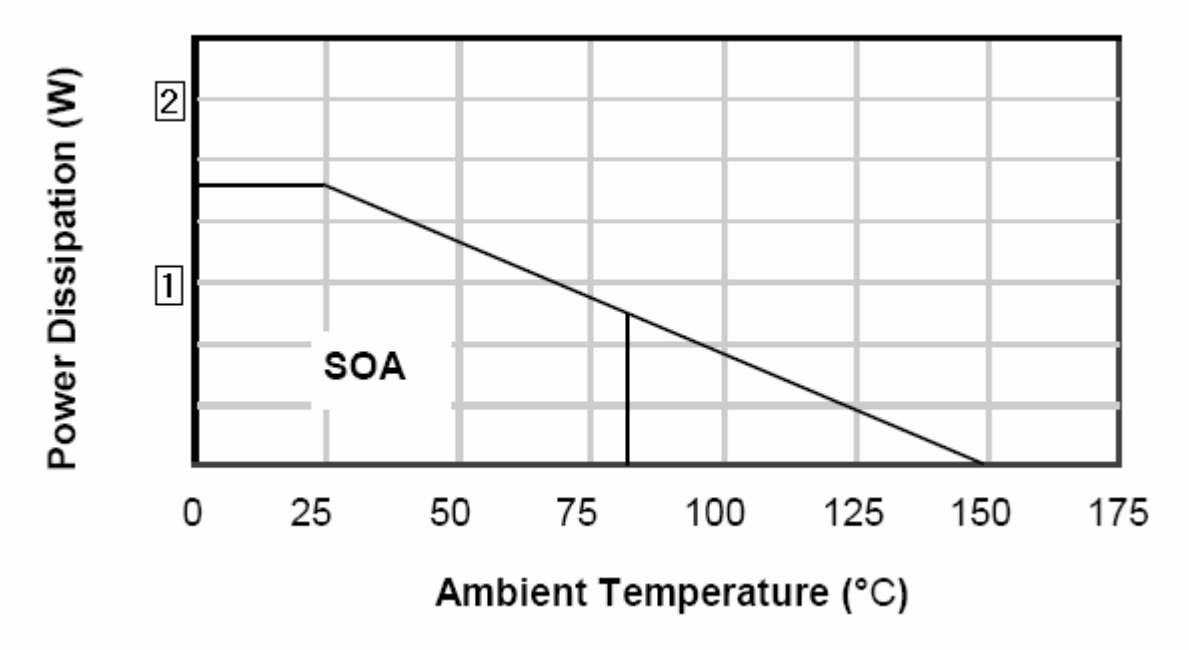
Where : Command 2 -- Data Setting Command
Command 3 -- Address Setting Command
Data -- Display Data

RECOMMENDED SOFTWARE PROGRAMMING FLOWCHART



Note : 1. Command 1 : Display Mode Setting
2. Command 2 : Data Setting Commands
3. Command 3 : Address Setting Commands
4. Command 4 : Display Control Commands
5. When IC power is applied for the first time, the contents of the Display RAM are not defined : thus, it is strongly suggested that the contents of the Display RAM must be cleared during the initial setting.

POWER DISSIPATION CURVE



ABSOLUTE MAXIMUM RATINGS

(Unless otherwise stated, Ta=25℃, GND=0V)

Parameter	Symbol	Rating	Units
Supply Voltage	V_{DD}	-0.5 to +6.0	V
Logic Input Voltage	V_I	-0.5 to V_{DD}+0.5	V
Driver Output Current/Pin	I_{OLGR}	300	mA
	I_{OHSG}	-24	mA
Maximum Driver Output Current/Total	I_{TOTAL}	300	mA
Operation Temperature	Topr	-40 ~ +85	℃
Storage Temperature	Tstg	-65 ~ 150	℃

RECOMMENDED OPERATING RANGE

(Unless otherwise stated, Ta= -40 to +85℃, GND=0V)

Parameter	Symbol	Min	Typ	Max	Unit
Logic Supply Voltage	V_{DD}	3.0	3.3	5.5	V
Dynamic Current (see Note)	I_{DDdyn}	.	.	1	mA
High-Level Input Voltage	V_{IH}	0.7V_{DD}	.	V_{DD}	V
Low-Level Input Voltage	V_{IL}	0	.	0.3 V_{DD}	V

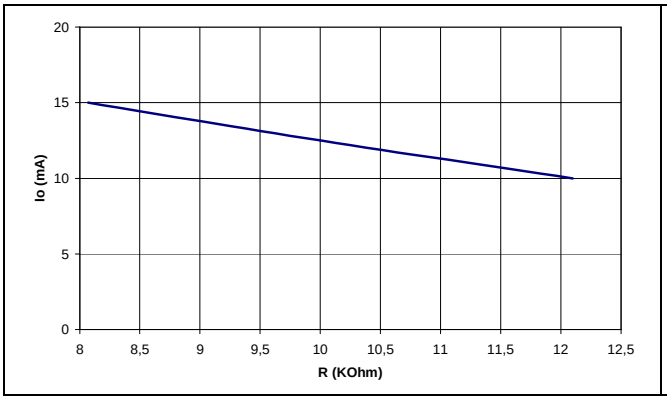
Note : Test Condition : Set Display Control Commands = 80H (Display Turn OFF State)

ELECTRICAL CHARACTERISTICS

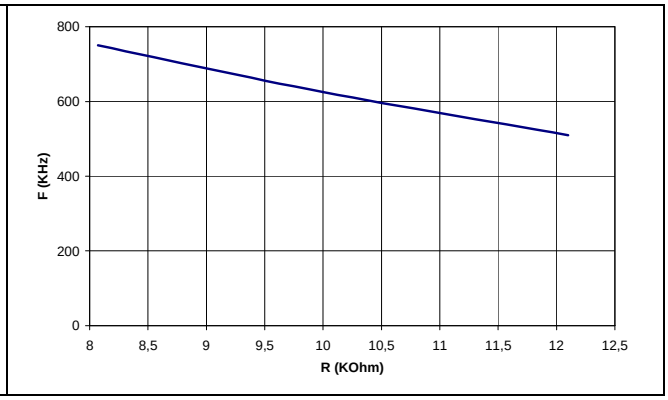
(Unless otherwise stated, V_{DD}=3.3~5.5V, GND=0V, Ta=-40 ~ 85℃)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High-Level Output Current	I_{OHSG1}	(V_{DD} = 3.3 ~5.5V) V_{LED} =2.3V R = 12.1KOhm SG1 to SG11 SG12/GR7 to SG14/GR5	8	10	12	mA
	I_{OHSG2}	(V_{DD} = 5V) V_{LED} =2.3V R = 8.07KOhm SG1 to SG11 SG12/GR7 to SG14/GR5	12	15	18	mA
Digital Input Current	I_{DG}	-	-0.2	-	+0.2	uA
Low-Level Digital Output Current	I_{OLDG}	V_O = 0.4V	4	-	-	mA
Segment High-Level Output Current Tolerance	I_{TOLSG}	V_O = V_{DD} =2.3V R = 12.1KOhm SG1 TO SG11 SG12/GR7	-	-	±5	%
High-Level Input Voltage	V_{IH}	-	0.7V_{DD}	-	0.3V_{DD}	V
Low-Level Input Voltage	V_{IL}	-	-	-	0.3V_{DD}	V
Oscillation Frequency	f_{OSC1}	(V_{DD}=3.3 ~5.5V) R = 12.1kOhm	400	500	600	kHz
	f_{OSC2}	(V_{DD} = 5V) R = 8.07KOhm	500	750	900	
K1 to K2 Pull Down Resistor	R_{PD}	K1 to K2 V_{DD} =5.0V	40	-	100	KΩ

High-Level Output Current

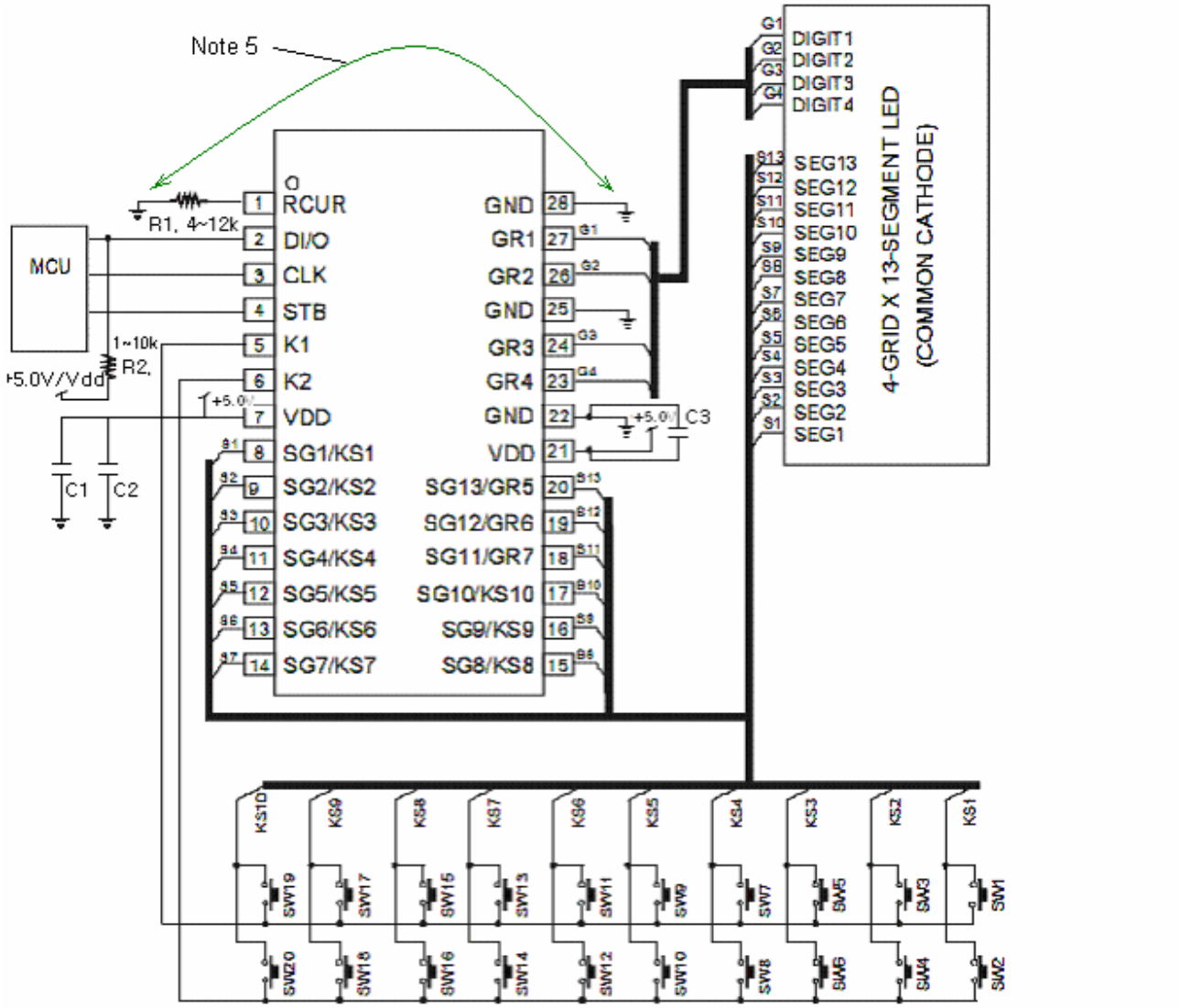


Oscillation Frequency



Remark : graphs are only Vdd=5V

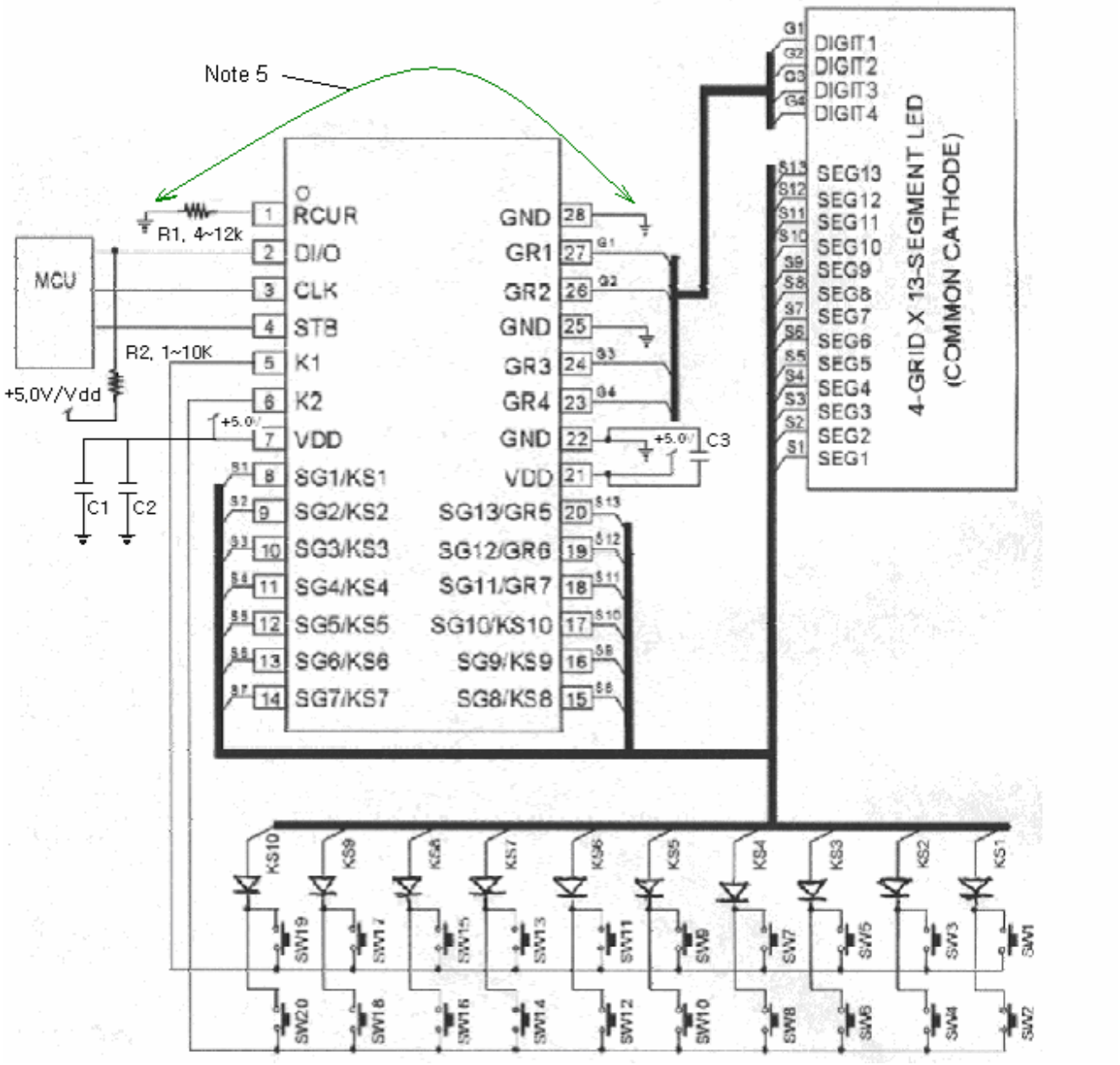
APPLICATION CIRCUIT



Note :
1. Circuit is for V_{DD} =5V
   When V_{DD} =3.3V, Recommend R1 = 12.1kOhm
2. The capacitor (0.1uF) connected between the GND and V_{DD} Pins must be located as near as possible to the IK2102 chip.
3. IK2102 power supply is separate from the application system power supply
4. For increase stability if IC and reduce noise, C1 & C2 should be placed closer to 7 pin and C3 should be placed closer to 21pin.
5. Ground of R1 should be routed directly to pin (28), not though common GND.

Recommend value
C1&C3. 0.1uF-ceramics
C2 470uF ~ 1000uF

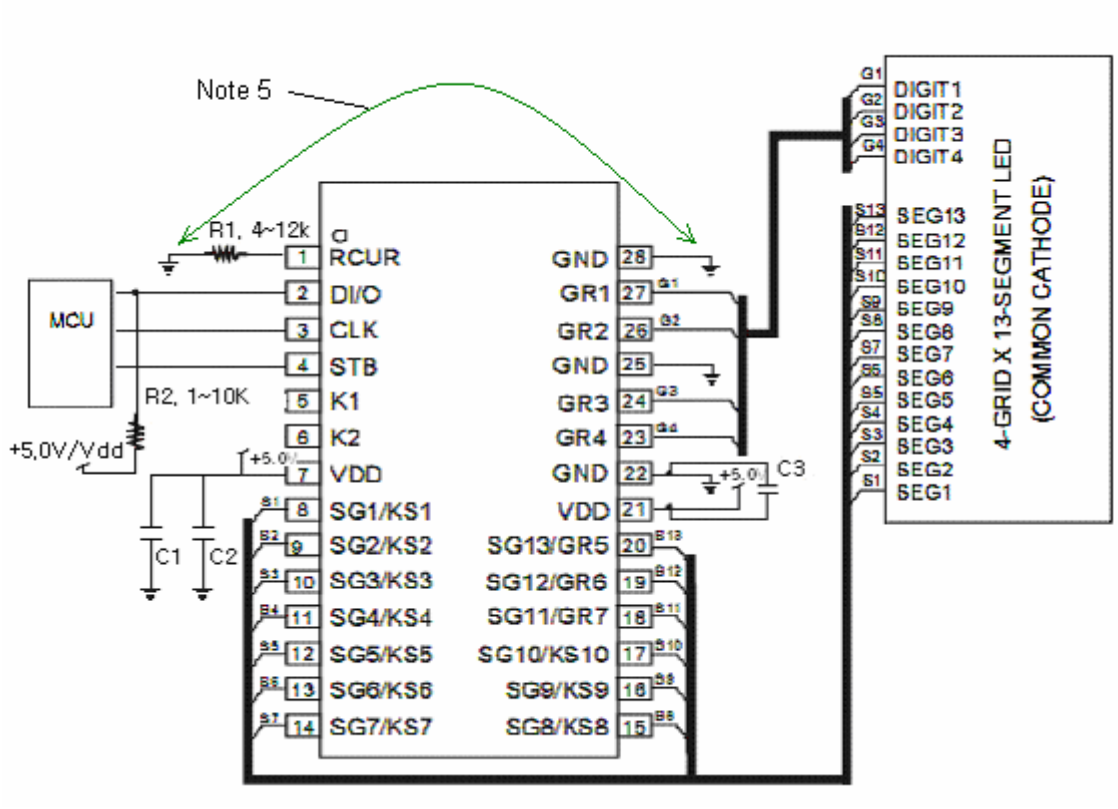
APPLICATION CIRCUIT
(IK2102, key scan with diodes)



Note :
1. Circuit is for V_{DD} =5V
   When V_{DD} =3.3V, Recommend R1 = 12.1kOhm
2. The capacitor (0.1uF) connected between the GND and V_{DD} Pins must be located as near as possible to the IK2102 chip.
3. IK2102 power supply is separate from the application system power supply
4. For increase stability if IC and reduce noise, C1 & C2 should be placed closer to 7 pin and C3 should be placed closer to 21pin.
5. Ground of R1 should be routed directly to pin (28), not though common GND.

Recommend value
C1&C3. 0.1uF - ceramics
C2 470uF ~ 1000uF

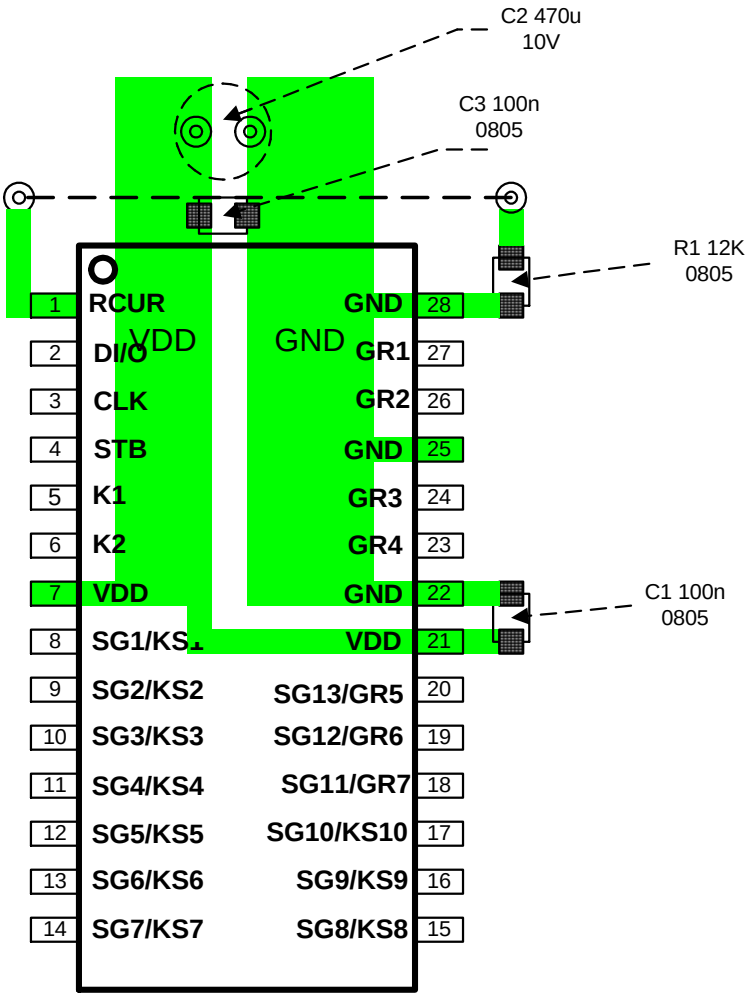
APPLICATION CIRCUIT (IK2102 without key scan)



Note :
1. Circuit is for V_{DD} =5V
   When V_{DD} =3.3V, Recommend R1 = 12.1kOhm
2. The capacitor (0.1uF) connected between the GND and V_{DD} Pins must be located as near as possible to the IK2102 chip.
3. IK2102 power supply is separate from the application system power supply
4. For increase stability if IC and reduce noise, C1 & C2 should be placed closer to 7 pin and C3 should be placed closer to 21pin.
5. Ground of R1 should be routed directly to pin (28), not though common GND.

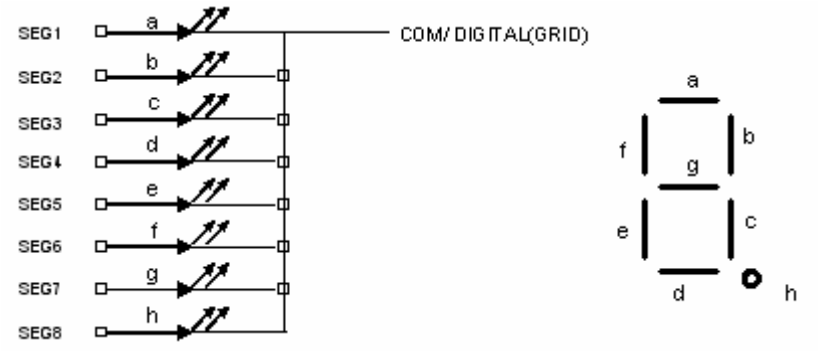
Recommend value
C1&C3. 0.1uF-ceramics
C2 470uF ~ 1000uF

Recommended Layout for GND and Vcc buses



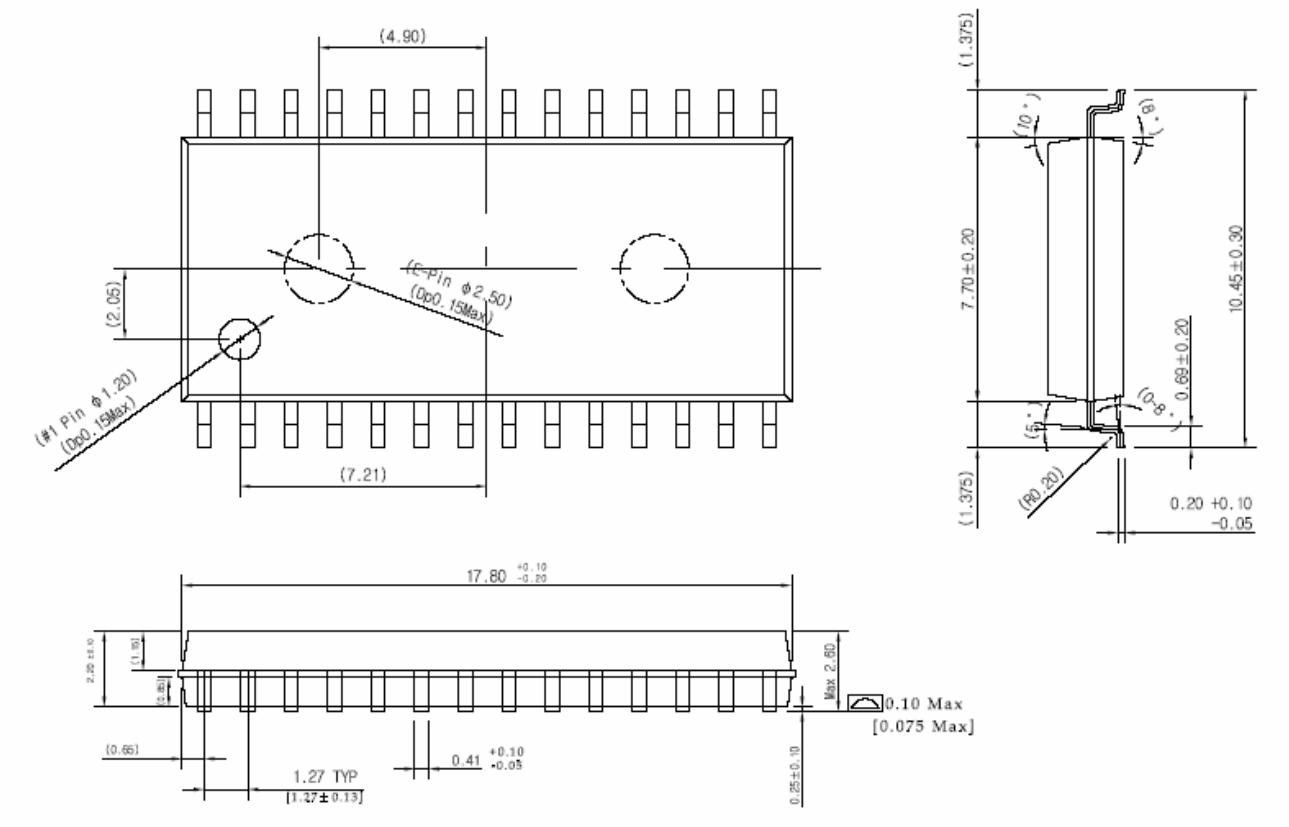
Layout considerations

COMMON CATHODE TYPE LED PANEL



Package Dimensions

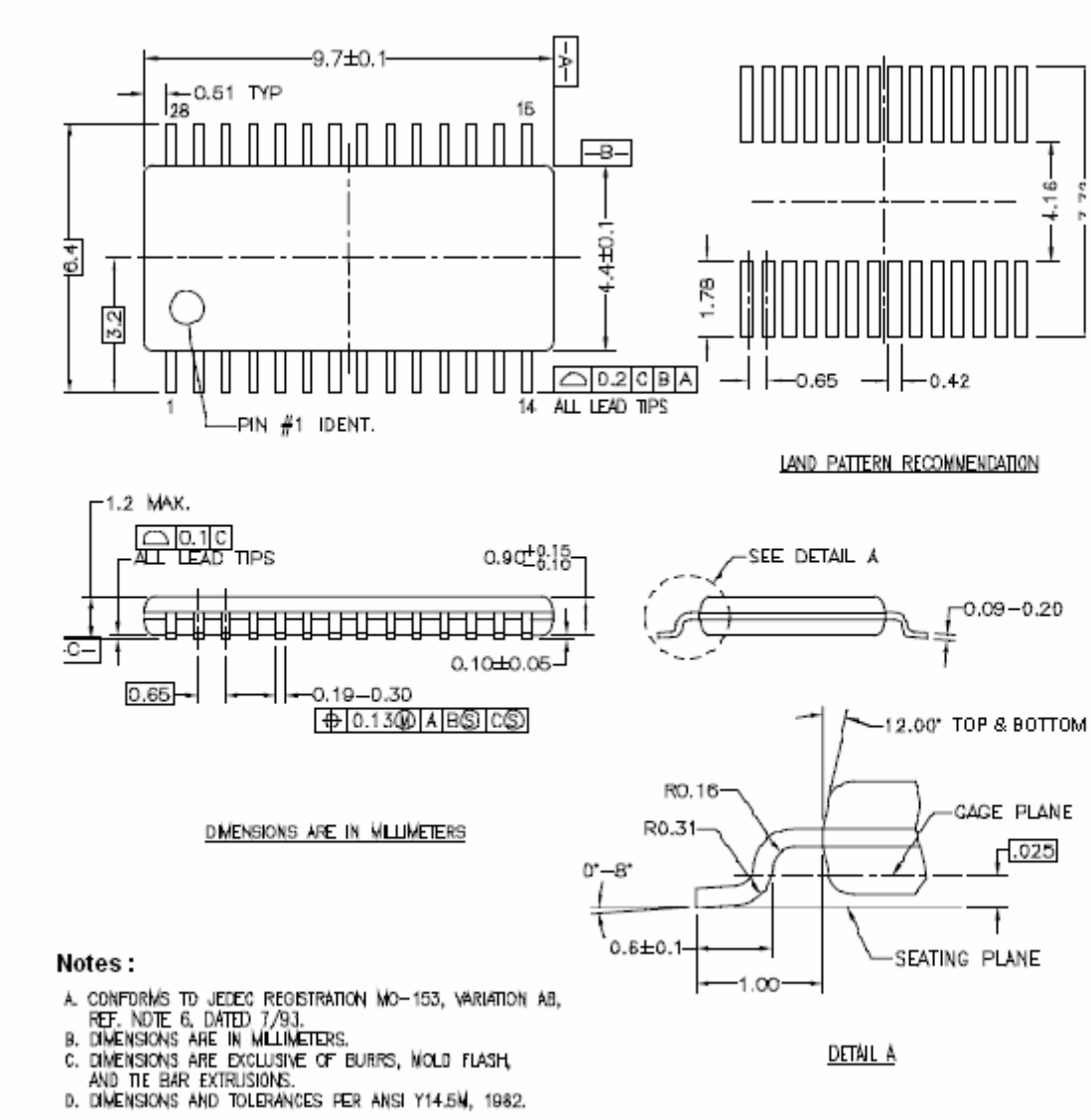
28SOP



Note

1. **These Dimensions Do not include Mold Protrusion.**
2. **“( )” is Reference.**
3. **"[ ]" is Assembly Out Quality.**

28TSSOP



Notes :

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF. NOTE 6, DATED 7/93.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.