MS-6507

Version 1.0
10/01/2001 Update

INTEL (R) Brookdale Chipset
Willamette/Northwood 478pin mPGA-B Processor Schematics

CPU:

Willamette/Northwood mPGA-478B Processor

System Brookdale Chipset:

INTEL MCH (North Bridge) +
INTEL ICH2 (South Bridge)

On Board Chipset:

BIOS -- FWH

LPC Super I/O -- W83627HF

Clock Generation -- CY28324

ON BOARD
SOUND--ADI1885

Expansion Slots:

AGP2.0 SLOT * 1
PCI2.2 SLOT * 3

Micro-Star	Title ***MS-6507***	Rev ***1.0***
Document Number	Cover Sheet	
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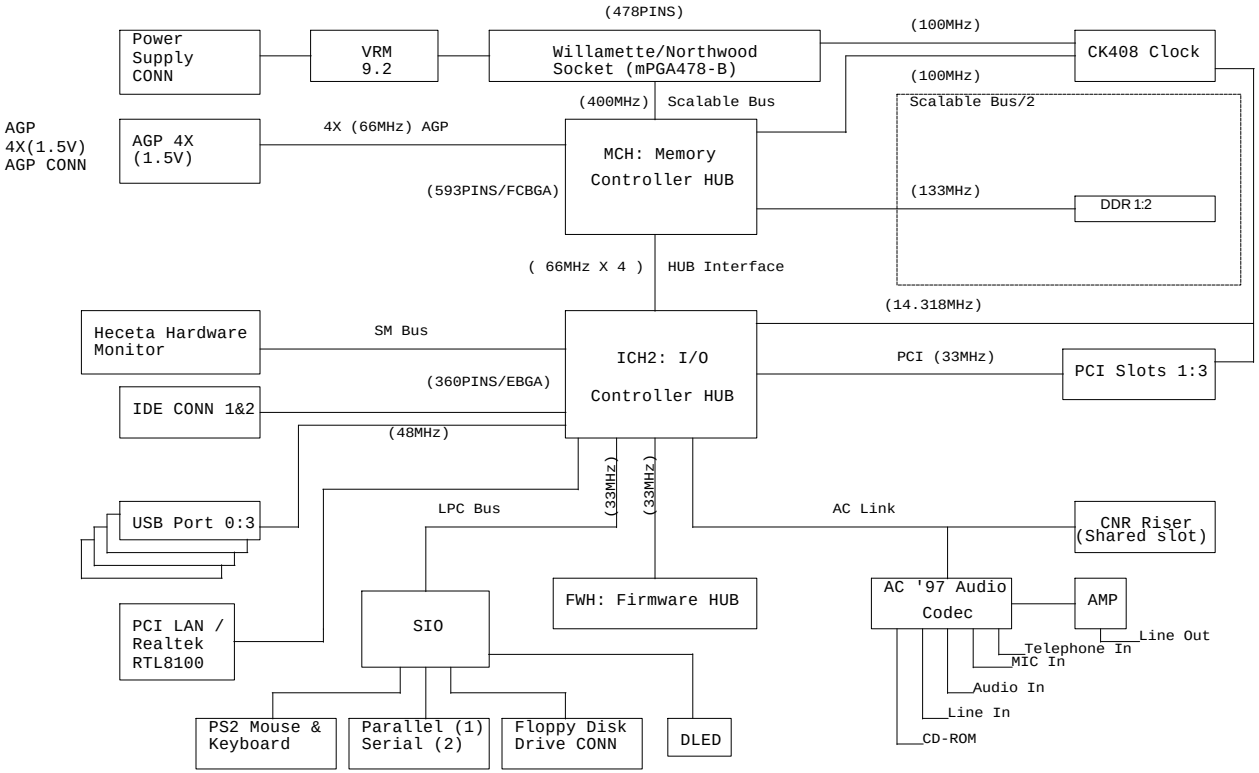

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General Purpose I/O Spec.

ICH2

GPIO Pin	Type	Function
GPIO 0	I	Non Connect
GPIO 1	I	Non Connect
GPIO 2~4	I	Not Implemented
GPIO 5	I	Non Connect
GPIO 6	I	AC97 Enabled/Disabled
GPIO 7	I	None
GPIO 8	I	LAN Wake Up
GPIO 9	I	AC'97 Serial Data In
GPIO 10	I	Non Connect
GPIO 11	I	Non Connect
GPIO 12	I	External SMI
GPIO 13	I	LPC PME
GPIO 14~15	I	Not Implemented
GPIO 16	O	Non Connect
GPIO 17	O	Non Connect
GPIO 18	O	Not Implemented
GPIO 19	O	Not Implemented
GPIO 20	O	Not Implemented
GPIO 21	O	Audio 6 channel control
GPIO 22	O	Non
GPIO 23	OD	BIOS Locked/Unlocked
GPIO 24	O	Non
GPIO 25	O	Non
GPIO 26	O	Non
GPIO 27	I/O	Non
GPIO 28	I/O	non
GPIO 29~31	I/O	Not Implemented

FWH

GPIO Pin	Type	Function
GPI 0	I	ATA IDE 1 Detect
GPI 1	I	ATA IDE 2 Detect
GPI 2	I	Reserved
GPI 3	I	Reserved

DLED-Super I/O

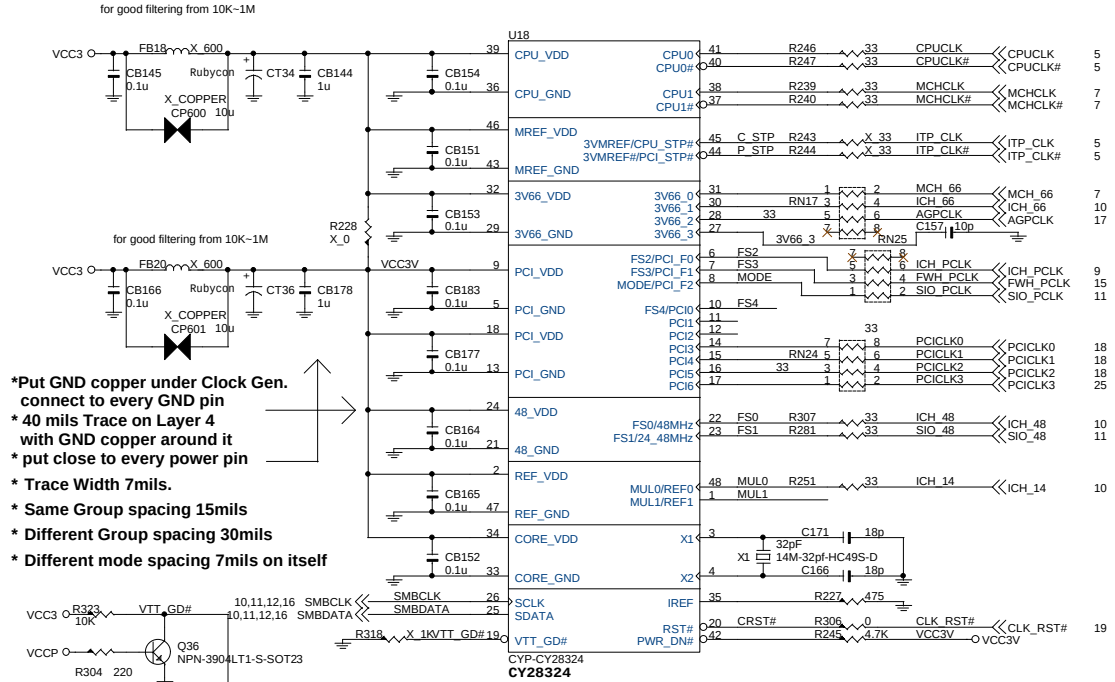
GPIO Pin	Type	Function
GP32	I/OD	DLED1
GP24	I/OD	DLED2
GP34	I/OD	DLED3
GP33	I/OD	DLED4

DEVICE	ICH INT Pin	IDSEL
PCI Slot 1	INTA# INTB# INTC# INTD#	AD16
PCI Slot 2	INTB# INTC# INTD# INTA#	AD17
PCI Slot 3	INTC# INTD# INTA# INTB#	AD18
PCI Audio	INTD#/INTE# INTA# INTB# INTC#	AD23
PCI Lan	INTC#/INTF# INTD# INTA# INTB#	AD22

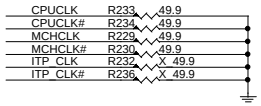
ATA100 IDE CONNECTORS

CLOCK GENERATOR BLOCK

*Trace less 0.5"



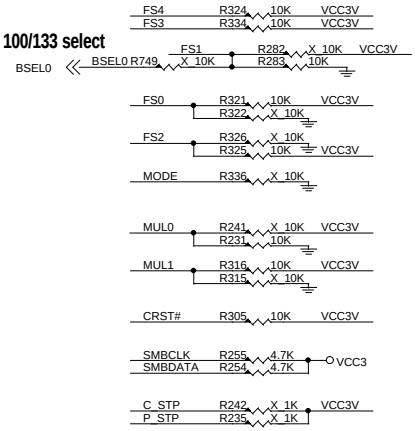
Shut Source Termination Resistors



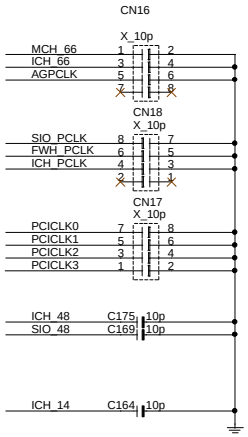
Trace less 0.2"

49.9ohm for 50ohm M/B impedance

CLOCK STRAPPING RESISTORS



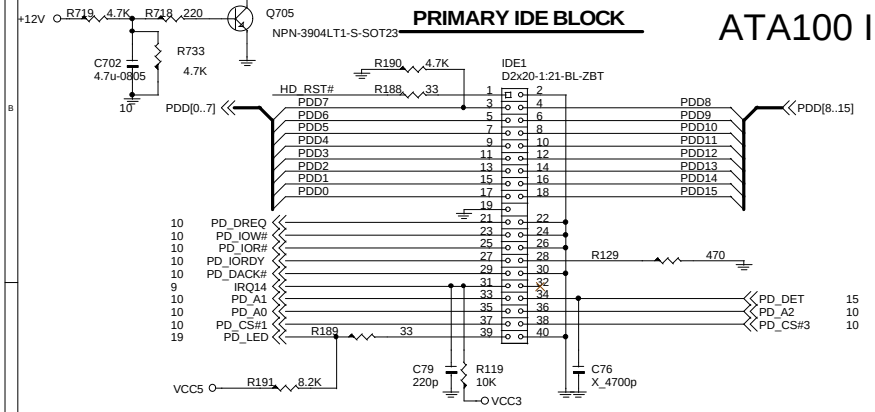
Pull-Down Capacitors



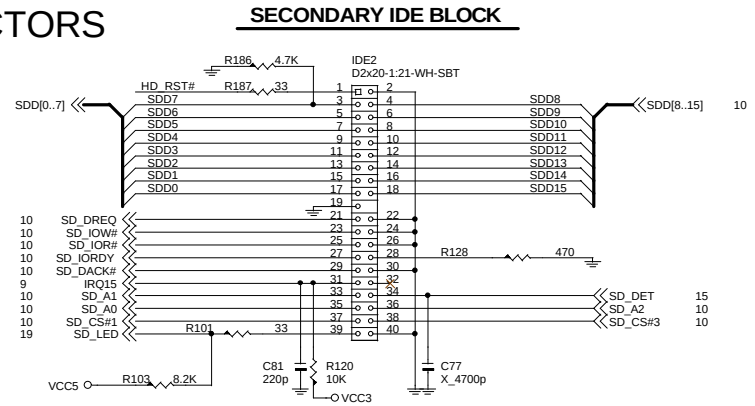
used only for EMI issue

Trace less 0.2"

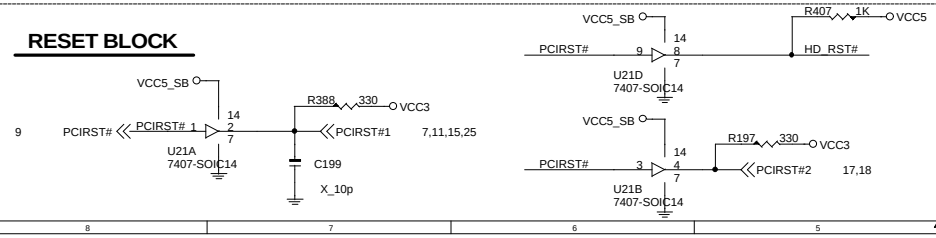
PRIMARY IDE BLOCK



SECONDARY IDE BLOCK



RESET BLOCK



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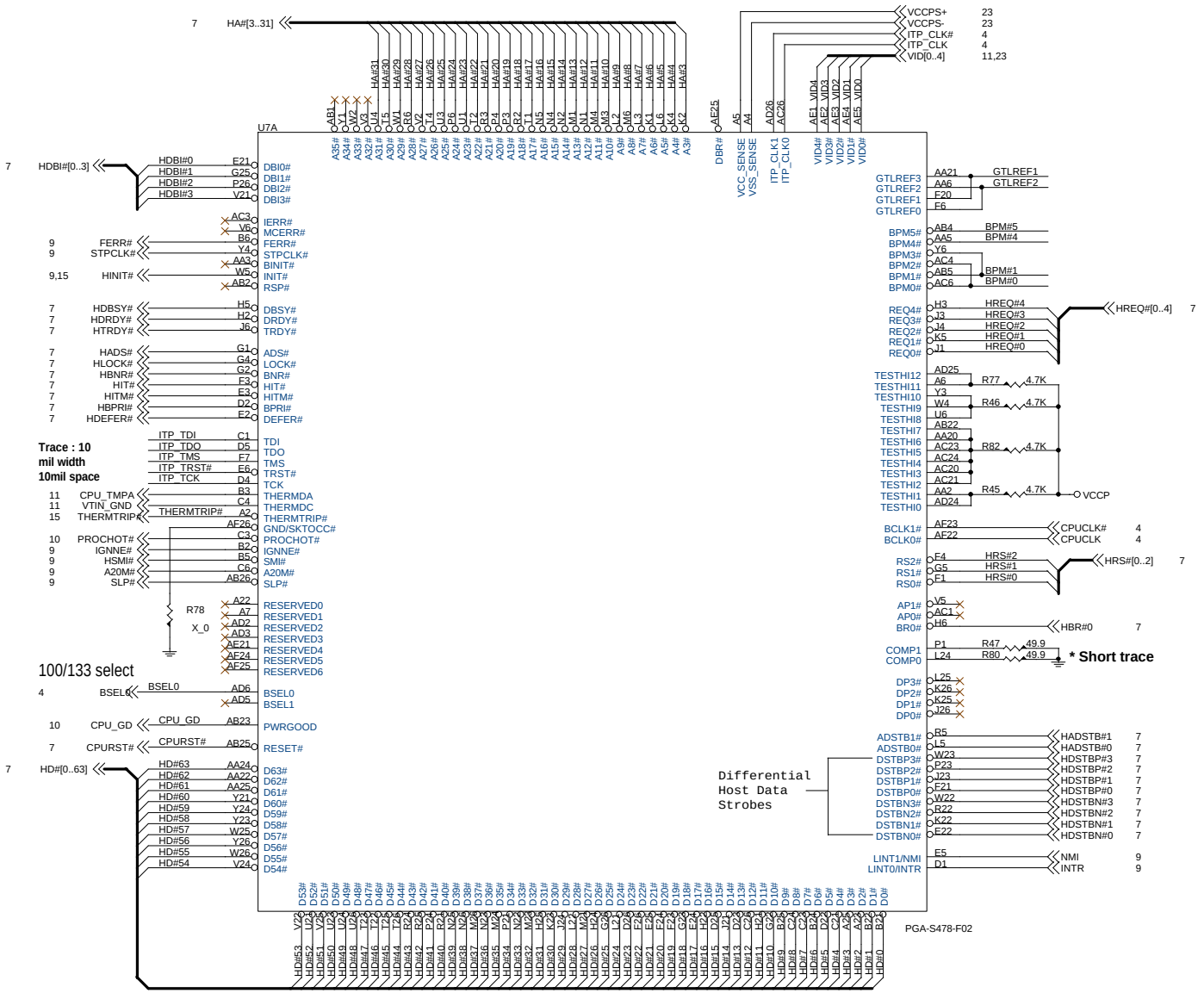
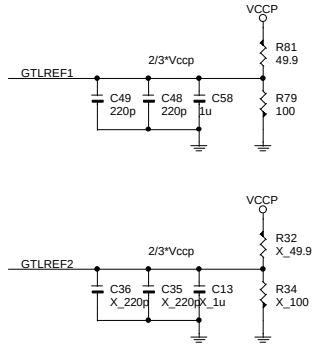
CPU SIGNAL BLOCK

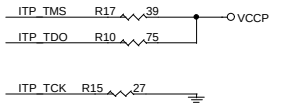


CPU GTL REFERNCE VOLTAGE BLOCK

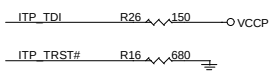


Every pin put one 220pF cap near it.
Trace Width 15mils, Space 15mils.
Keep the voltage dividers within 1.5 inches of the first GTLREF Pin

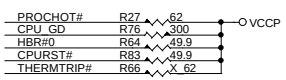
CPU ITP BLOCK



CPU STRAPPING RESISTORS



ALL COMPONENTS CLOSE TO CPU



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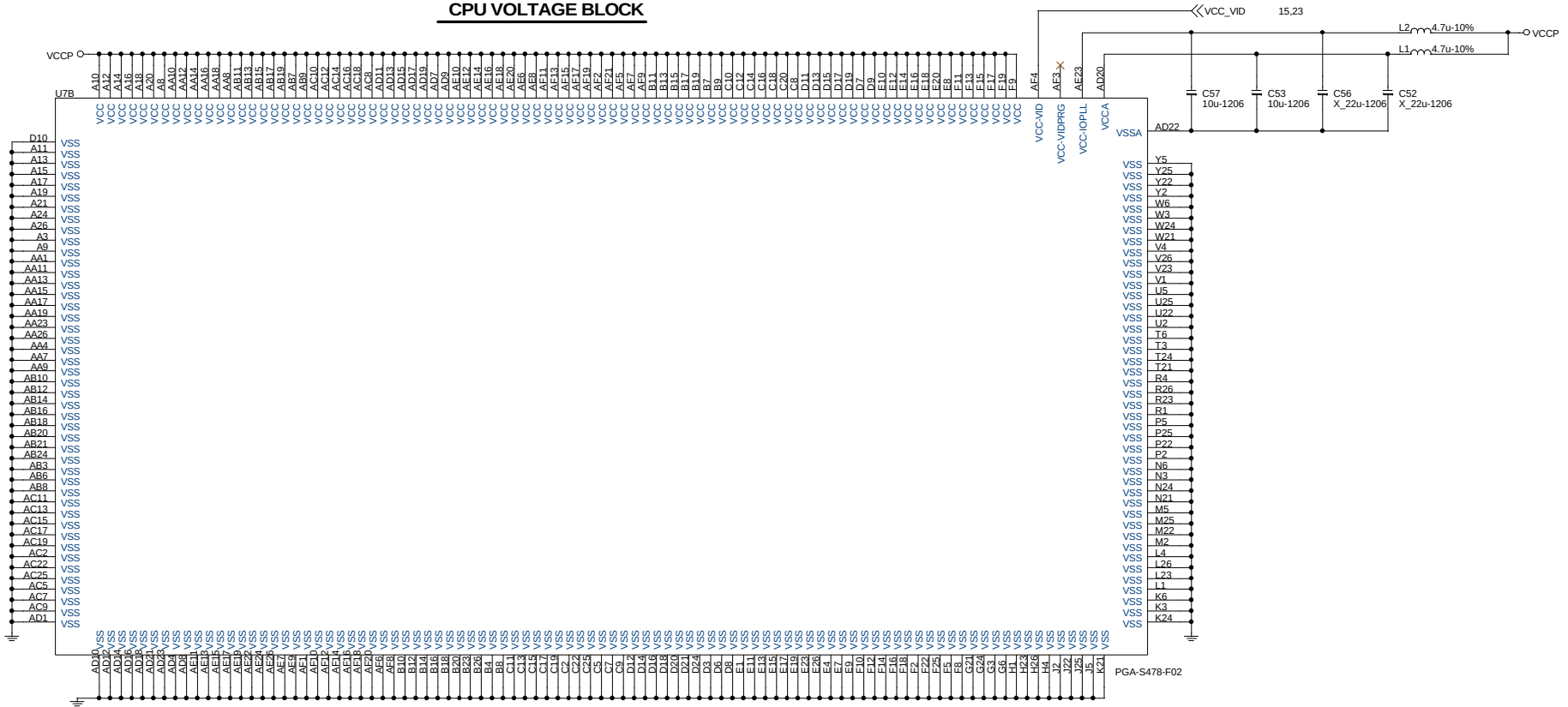
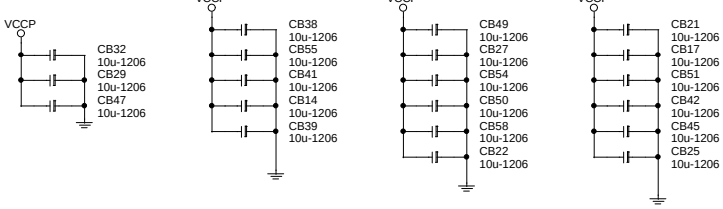
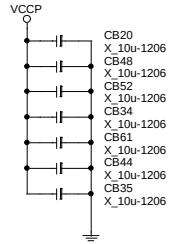
CPU VOLTAGE BLOCK



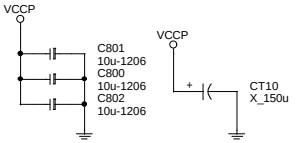
CPU DECOUPLING CAPACITORS



PLACE CAPS WITHIN CPU CAVITY



Reserve if necessary.



PLACE CAPS WITHIN CPU CAVITY SOLDER

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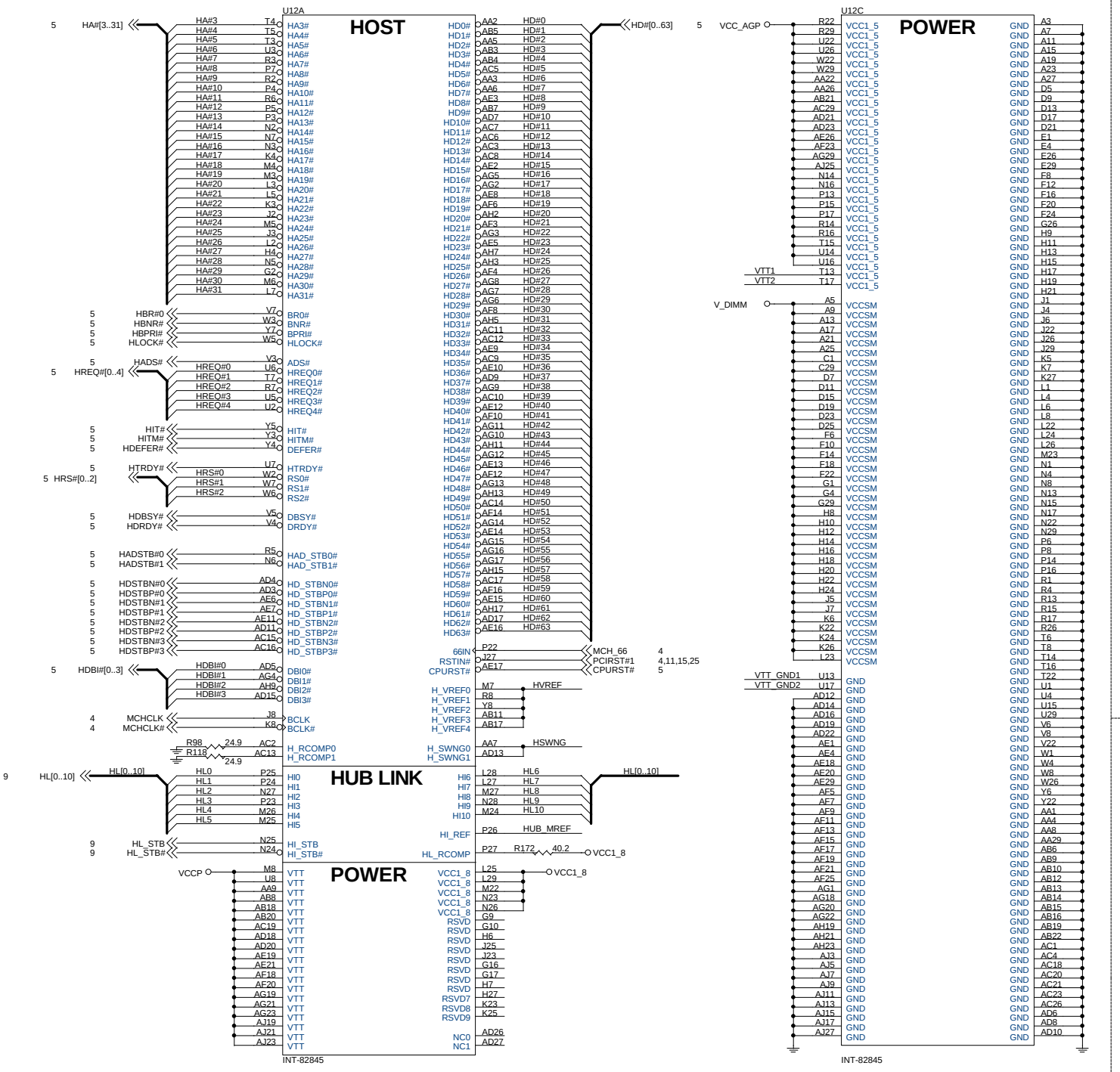
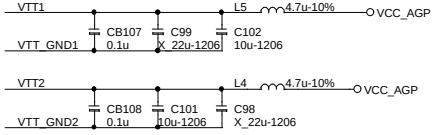
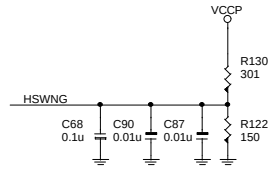
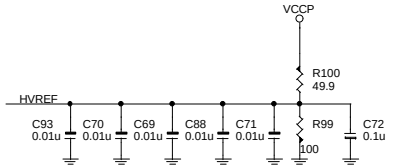


MCH REFERENCE BLOCK

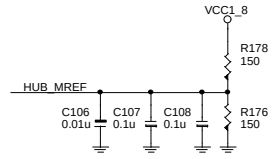




Place 1 Cap. as Close as possible to every pin of MCH
Trace width use 15 mils and 15mils space

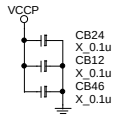


Place 1 Cap. as Close as possible to every pin of MCH
Trace width use 15 mils and 15mils space

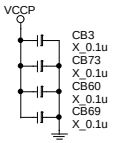


Place 0.01uF Cap. as Close as possible to MCH
Trace width use 15 mils and 15mils space

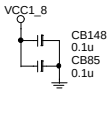
MCH Trace Decoupling Capacitors



ADDRESS



DATA



MCH & ICH2

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1" trace

U12B

DDR

26 MD[0..63]

MD0	G28	SDQ0	
MD1	F27	SDQ1	
MD2	C28	SDQ2	
MD3	E28	SDQ3	
MD4	H25	SDQ4	
MD5	G27	SDQ5	
MD6	F25	SDQ6	
MD7	B28	SDQ7	
MD8	E27	SDQ8	
MD9	C27	SDQ9	
MD10	B25	SDQ10	
MD11	C25	SDQ11	
MD12	B27	SDQ12	
MD13	D27	SDQ13	
MD14	D26	SDQ14	
MD15	E25	SDQ15	
MD16	D24	SDQ16	
MD17	E23	SDQ17	
MD18	C22	SDQ18	
MD19	E21	SDQ19	
MD20	C24	SDQ20	
MD21	B23	SDQ21	
MD22	D22	SDQ22	
MD23	B21	SDQ23	
MD24	C21	SDQ24	
MD25	D20	SDQ25	
MD26	C19	SDQ26	
MD27	D18	SDQ27	
MD28	C20	SDQ28	
MD29	E19	SDQ29	
MD30	C18	SDQ30	
MD31	E17	SDQ31	
MD32	E13	SDQ32	
MD33	C12	SDQ33	
MD34	B11	SDQ34	
MD35	C10	SDQ35	
MD36	B13	SDQ36	
MD37	C13	SDQ37	
MD38	C11	SDQ38	
MD39	D10	SDQ39	
MD40	E10	SDQ40	
MD41	C9	SDQ41	
MD42	D8	SDQ42	
MD43	E8	SDQ43	
MD44	E11	SDQ44	
MD45	B9	SDQ45	
MD46	B7	SDQ46	
MD47	C7	SDQ47	
MD48	C6	SDQ48	
MD49	D6	SDQ49	
MD50	D4	SDQ50	
MD51	B3	SDQ51	
MD52	E6	SDQ52	
MD53	B5	SDQ53	
MD54	C4	SDQ54	
MD55	E5	SDQ55	
MD56	C3	SDQ56	
MD57	D3	SDQ57	
MD58	F4	SDQ58	
MD59	F3	SDQ59	
MD60	B2	SDQ60	
MD61	C2	SDQ61	
MD62	E2	SDQ62	
MD63	G5	SDQ63	

1" Trace

G3	RCVENIN#	
H3	RCVENOUT#	

SMA0	E12	DDRMAA0
SMA1	F17	DDRMAA1
SMA2	E16	DDRMAA2
SMA3	G18	DDRMAA3
SMA4	G19	DDRMAA4
SMA5	E18	DDRMAA5
SMA6	F19	DDRMAA6
SMA7	G21	DDRMAA7
SMA8	G20	DDRMAA8
SMA9	F21	DDRMAA9
SMA10	F13	DDRMAA10
SMA11	E20	DDRMAA11
SMA12	G22	DDRMAA12

DDRMAA[0..12] 16,26,27

SCS#0	E9	DDRCS#0
SCS#1	E7	DDRCS#1
SCS#2	F9	DDRCS#2
SCS#3	E7	DDRCS#3

DDRCS#[0..3] → DDRCS#[0..3] 16,26,27

SCB0	C16	CB0
SCB1	D16	CB1
SCB2	B15	CB2
SCB3	C14	CB3
SCB4	B17	CB4
SCB5	C17	CB5
SCB6	C15	CB6
SCB7	D14	CB7

CB[0..7] → CB[0..7] 26

SDQS0	F26	SDQS0	26
SDQS1	C26	SDQS1	26
SDQS2	C23	SDQS2	26
SDQS3	B19	SDQS3	26
SDQS4	D12	SDQS4	26
SDQS5	C8	SDQS5	26
SDQS6	C5	SDQS6	26
SDQS7	E3	SDQS7	26
SDQS8	E15	SDQS8	26

SCK0	E14	DCLK0
SCK#0	F15	DCLK#0
SCK1	J24	DCLK1
SCK#1	G25	DCLK#1
SCK2	G6	DCLK2
SCK#2	G7	DCLK#2
SCK3	G15	DCLK3
SCK#3	G14	DCLK#3
SCK4	E24	DCLK4
SCK#4	G24	DCLK#4
SCK5	H5	DCLK5
SCK#5	F5	DCLK#5

SCKE0	G23	DDRCKE0
SCKE1	F22	DDRCKE1
SCKE2	H23	DDRCKE2
SCKE3	F23	DDRCKE3

DDRCKE0 16,27
DDRCKE1 16,27
DDRCKE2 16,27
DDRCKE3 16,27

SRAS#	F11	RASA#	26
SCAS#	G8	CASA#	26
SWE#	G11	WEA#	26

SBS0	G12	DDRBS0	16,26,27
SBS1	G13	DDRBS1	16,26,27

SM_RCOMP J28 MRCOMP

SD_REF0 J9 SM_REF
SD_REF1 J21

AGP

17 GAD[0..31]

GAD0	R27	G_AD0
GAD1	R28	G_AD1
GAD2	T25	G_AD2
GAD3	R25	G_AD3
GAD4	T26	G_AD4
GAD5	T27	G_AD5
GAD6	U27	G_AD6
GAD7	U28	G_AD7
GAD8	V26	G_AD8
GAD9	V27	G_AD9
GAD10	T23	G_AD10
GAD11	U23	G_AD11
GAD12	T24	G_AD12
GAD13	U24	G_AD13
GAD14	U25	G_AD14
GAD15	V24	G_AD15
GAD16	Y27	G_AD16
GAD17	Y26	G_AD17
GAD18	AA28	G_AD18
GAD19	AB25	G_AD19
GAD20	AB27	G_AD20
GAD21	AA27	G_AD21
GAD22	AB26	G_AD22
GAD23	Y23	G_AD23
GAD24	AB23	G_AD24
GAD25	AA24	G_AD25
GAD26	AA25	G_AD26
GAD27	AB24	G_AD27
GAD28	AC25	G_AD28
GAD29	AC24	G_AD29
GAD30	AC22	G_AD30
GAD31	AD24	G_AD31

17 GC_BE#[0..3]

GC_BE#0	V25	G_C/BE0#
GC_BE#1	V23	G_C/BE1#
GC_BE#2	Y25	G_C/BE2#
GC_BE#3	AA23	G_C/BE3#

G_FRAME#	Y24	GFRAME#	17
G_IRDY#	W27	GIRDY#	17
G_TRDY#	W24	GTRDY#	17
G_DEVSEL#	W28	GDEVSEL#	17
G_STOP#	W23	GSTOP#	17
G_PAR	W25	GPAR	17

Tri-Stated during RSTIN# assertion

G_REQ#	AG24	GREQ#	17
G_GNT#	AH25	GGNT#	17

SBA0	AH28	SBA0
SBA1	AH27	SBA1
SBA2	AG28	SBA2
SBA3	AG27	SBA3
SBA4	AE28	SBA4
SBA5	AE27	SBA5
SBA6	AE24	SBA6
SBA7	AE25	SBA7

SBA[0..7] 17

SB_STB	AF27	SB_STB	17
SB_STB#	AF26	SB_STB#	17

ST0	AG25	ST0
ST1	AF24	ST1
ST2	AG26	ST2

ST[0..2] 17

AD_STB0	R24	GAD_STB0	17
AD_STB0#	R23	GAD_STB#0	17
AD_STB1	AC27	GAD_STB1	17
AD_STB1#	AC28	GAD_STB#1	17

PIPE#	AF22	PIPE#	17
RBF#	AE22	RBF#	17
WBF#	AF23	WBF#	17

CB224 X_0.1u

AGPREF	AA21	AGPREF	17
G_RCOMP	AD25	R165 40.2	
TESTIN#	H26	R168 X_4.7K	VCC1_8

INT-82845

close MCH
5/23 update

MCH REFERENCE VOLTAGE

DDR_VTT
R500
30
MRCOMP
C500
0.1u

SM_REF
DIMMREF
C95 0.1u
C97 0.1u

MCH MEMORY CLOCK RC CIRCUITS

RN538

DCLK#1	7	8	DCLK#1	DCLK#1	16,26
DCLK1	5	6	DCLK1	DCLK1	16,26
DCLK#4	3	4	DCLK#4	DCLK#4	16,26
DCLK4	1	2	DCLK4	DCLK4	16,26

X_0

RN539

DCLK3	1	2	DCLK3	DCLK3	16,26
DCLK#3	3	4	DCLK#3	DCLK#3	16,26
DCLK0	5	6	DCLK0	DCLK0	16,26
DCLK#0	7	8	DCLK#0	DCLK#0	16,26

X_0

RN540

DCLK2	1	2	DCLK2	DCLK2	16,26
DCLK#2	3	4	DCLK#2	DCLK#2	16,26
DCLK#5	5	6	DCLK#5	DCLK#5	16,26
DCLK5	7	8	DCLK5	DCLK5	16,26

X_0

MCH DECOUPLING CAPACITOR

VCCP: CB93 1u, CB98 0.1u, CB94 0.1u, CB97 0.1u, CB100 0.01u, CB96 10u-1206, CB90 10u-1206

VCC1_8: CB117 1u, CB116 0.1u

VCC_AGP: CB114 0.1u, CB115 0.1u, CB126 0.1u, CB118 0.1u, CB106 0.1u

V_DIMM: CB89 0.1u, CB76 0.1u, CB101 0.1u, CB86 0.1u, CB78 0.1u, CB84 0.1u, CB81 0.1u

EMI
VCC5: C211 0.1u, C208 0.1u, C8 0.1u
V_DIMM: C21 0.1u
VCC5

C105 0.1u, C104 1u — AGPREF

BACK
VCCP: CB219 X_0.1u
V_DIMM: CB225 X_0.1u, CB221 X_0.1u
VCC_AGP: CB222 X_0.1u, CB220 X_0.1u, CB227 X_0.1u, CB223 X_0.1u, CB226 X_0.1u

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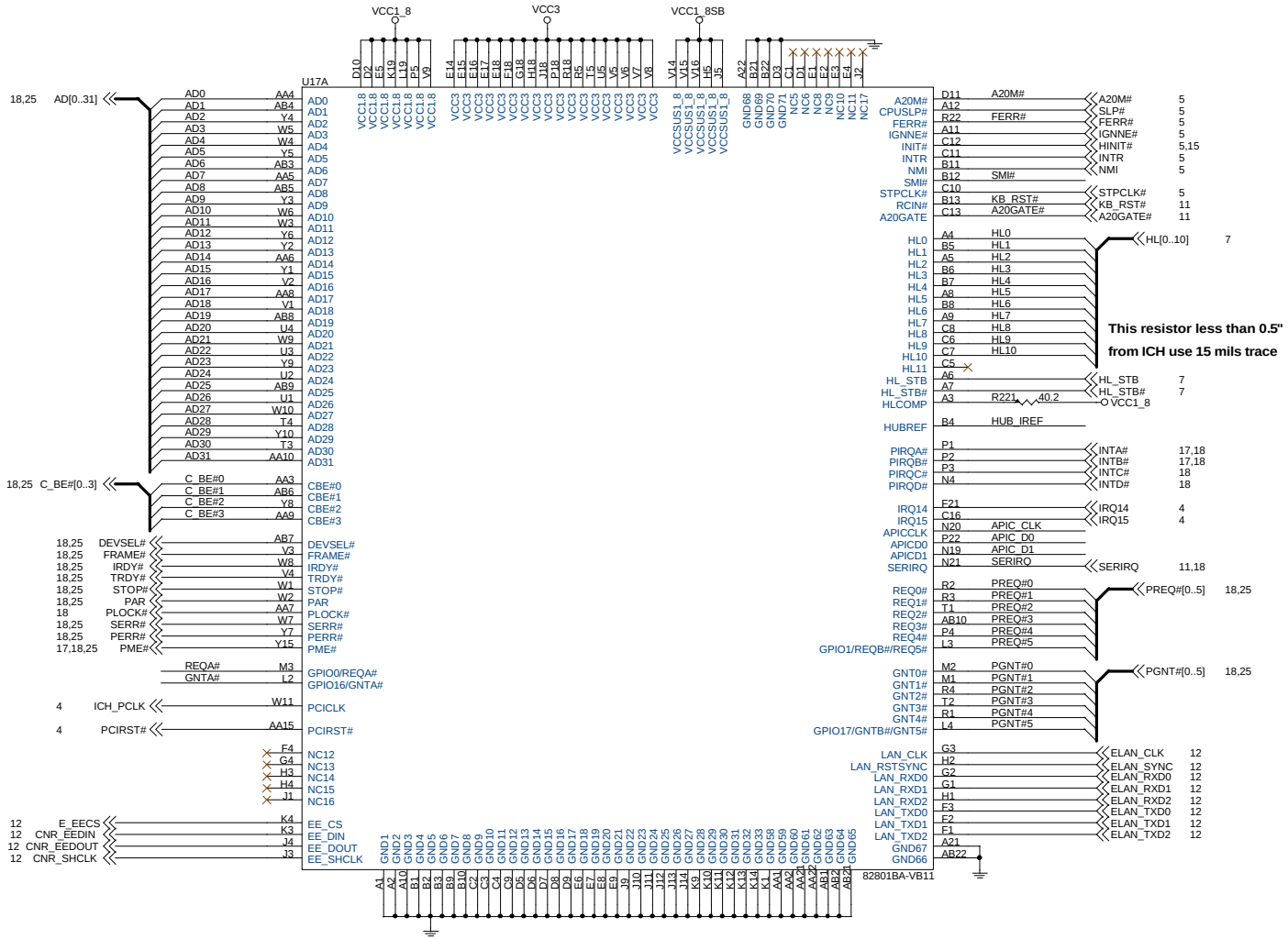
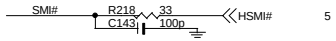
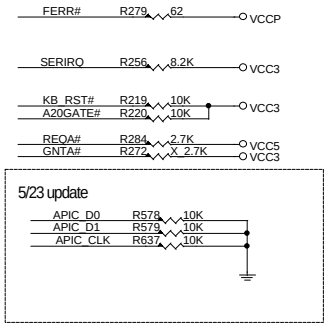
ICH2 PCI / HUB LINK / CPU / LAN / INTERRUPT SIGNALS



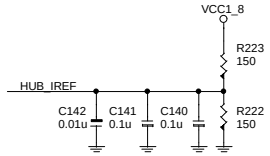
ICH2 SMI# SIGNAL



ICH2 STRAPPING RESISTORS



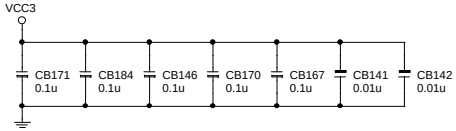
ICH2 REFERENCE VOLTAGE



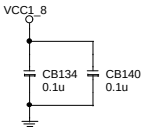
Place Cap. as Close as possible to ICH2

Trace width use 15 mils and 15mils space

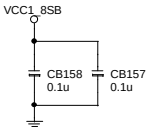
ICH2 DECOUPLING CAPACITORS



Place one 0.1U/0.01U pair in each corner and 2 on opposite sides close to ICH2 if it fit



Distribute near the 1.8V power pin of the ICH2



Distribute near the VCC1_8SB Power pin of the ICH2

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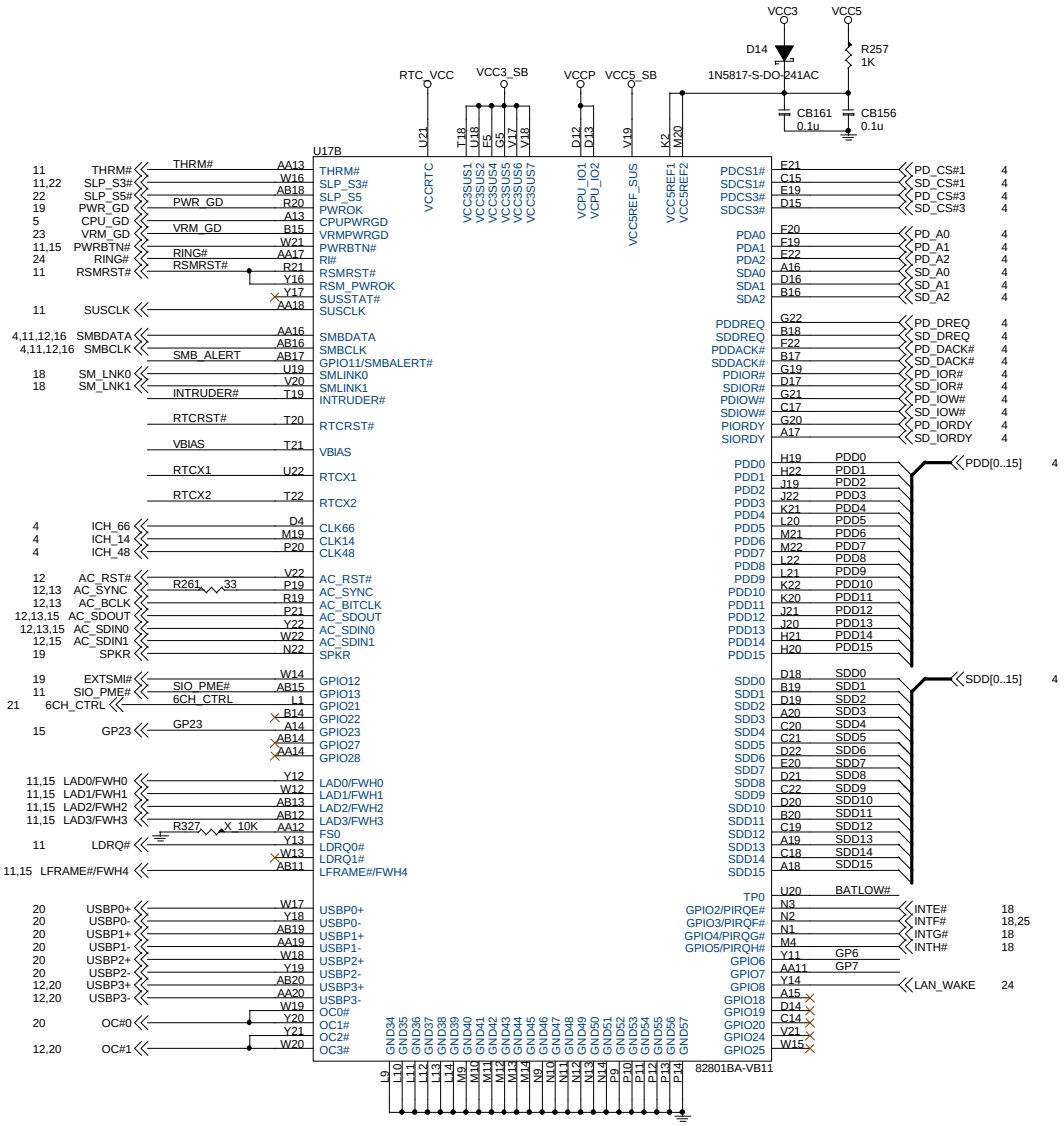
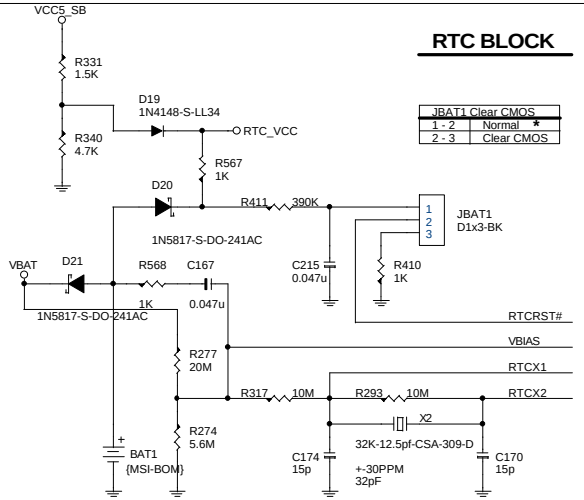
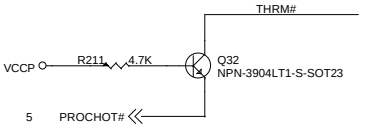
ICH2 ASIC / RTC / AC'97 / GPIO / LPC / USB / IDE SIGNALS



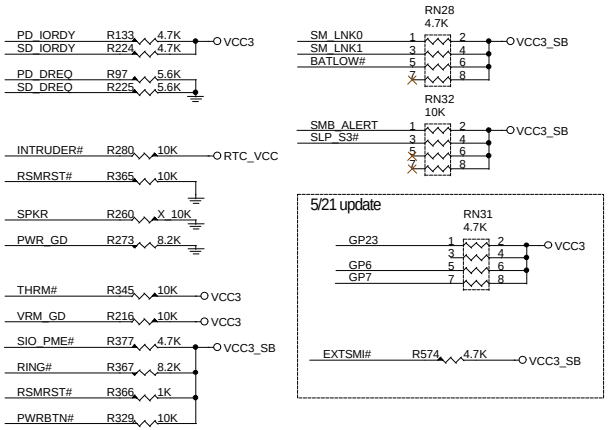
RTC BLOCK



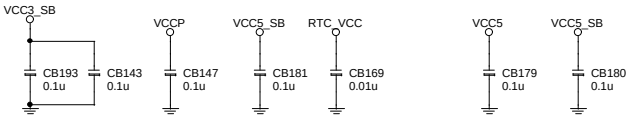
PROCHOT BLOCK



ICH2 STRAPPING RESISTORS



ICH2 DECOUPLING CAPACITOR



Distribute near the VCC3_SB power pin of the ICH

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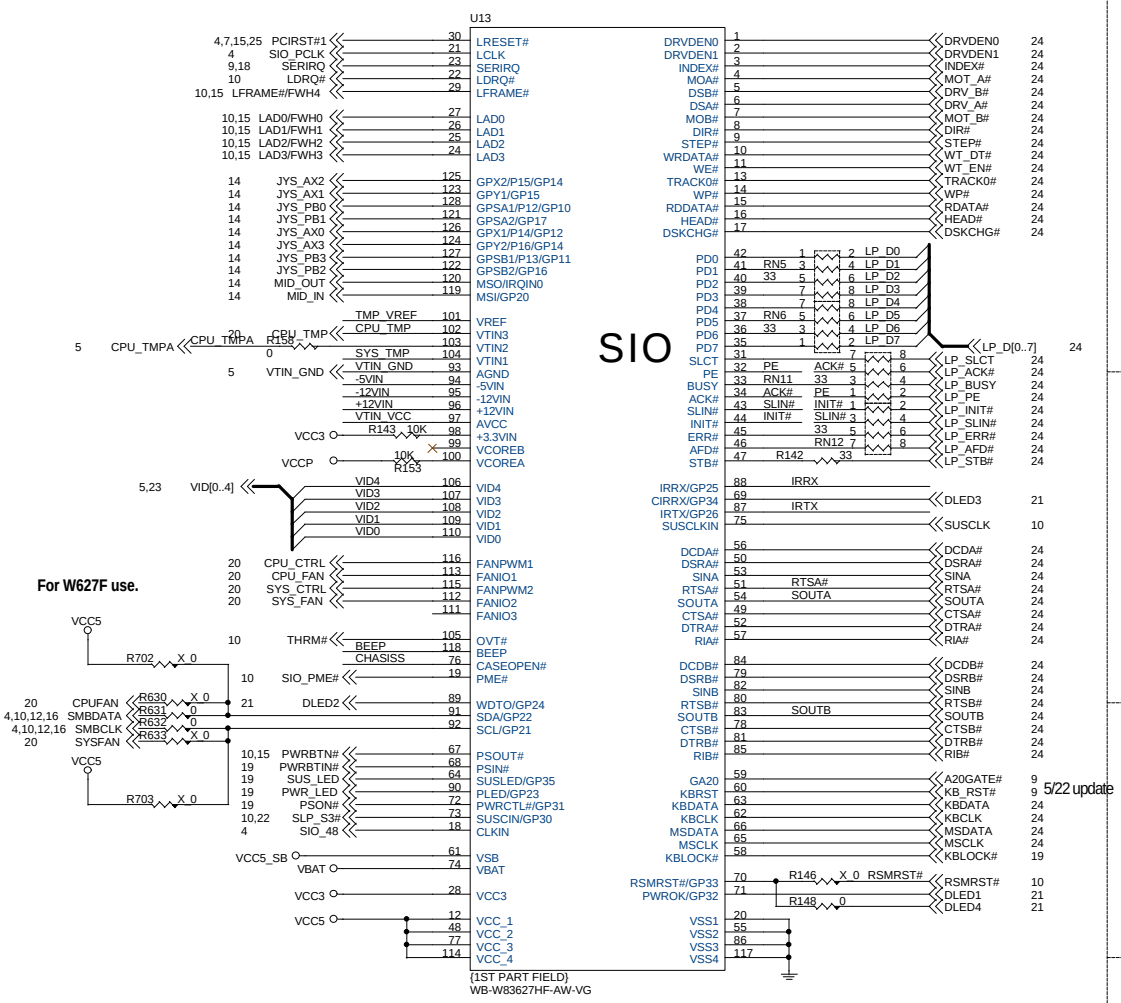
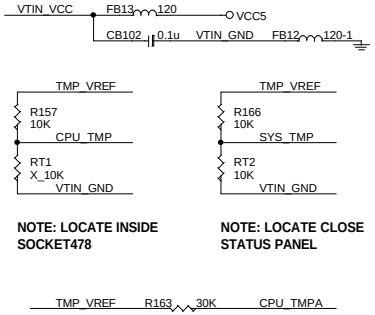
LPC SUPER I/O W83627HF



For W627F use.

5/22 update

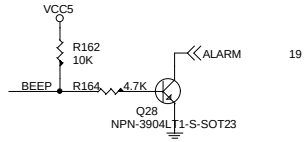
THERMAL RESISTOR BLOCK



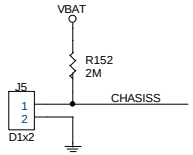
NOTE: LOCATE INSIDE SOCKET478

NOTE: LOCATE CLOSE STATUS PANEL

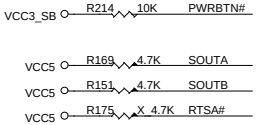
SPEAKER BLOCK



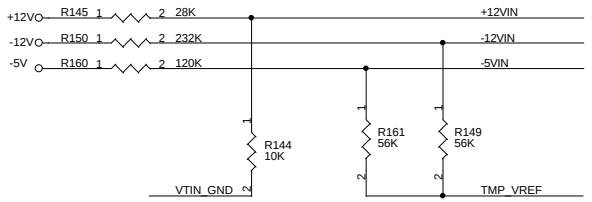
CHASSIS INTRUSION HEADER



SUPER I/O STRAPPING RESISTOR

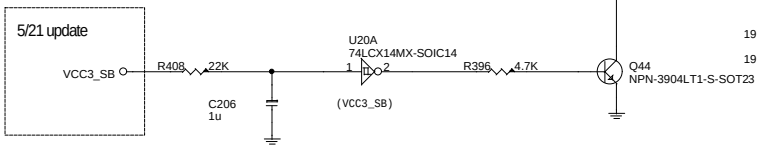


SOUTA	L: Disable KBC	H: Enable KBC
SOUTB	L: 24MHZ	H: 48MHZ
RTSA#	L: CFAD=2E	H: CFAD=4E
DTRA#	L: PNP Default	H: PNP no Default

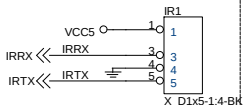


RESUME RESET CIRCUIT BLOCK

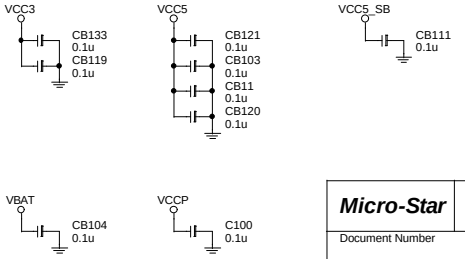
Stuff all for D Version bug



IR HEADER



DECOUPLING CAPACITOR



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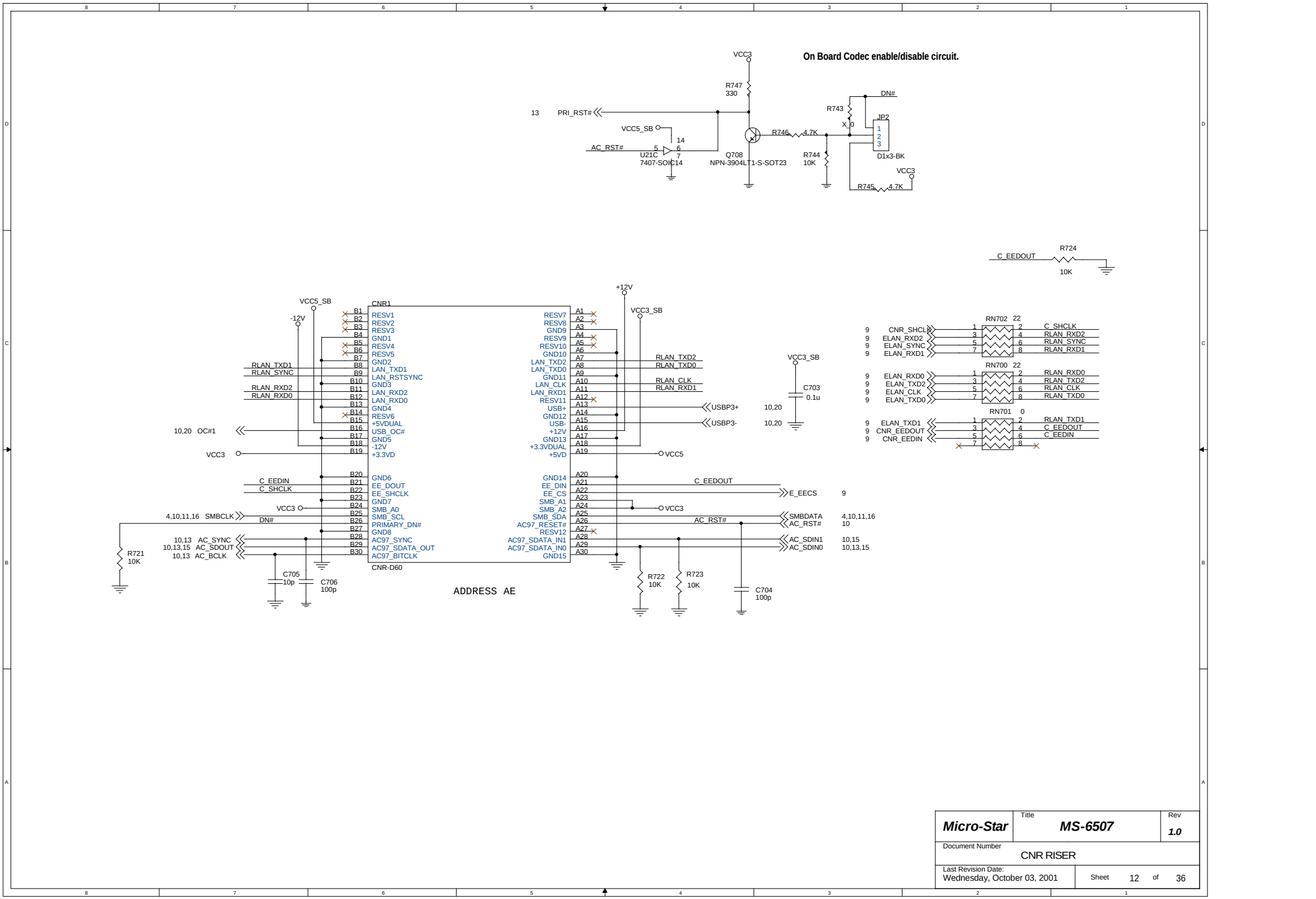

Micro-Star	Title: MS-6507	Rev: 1.0
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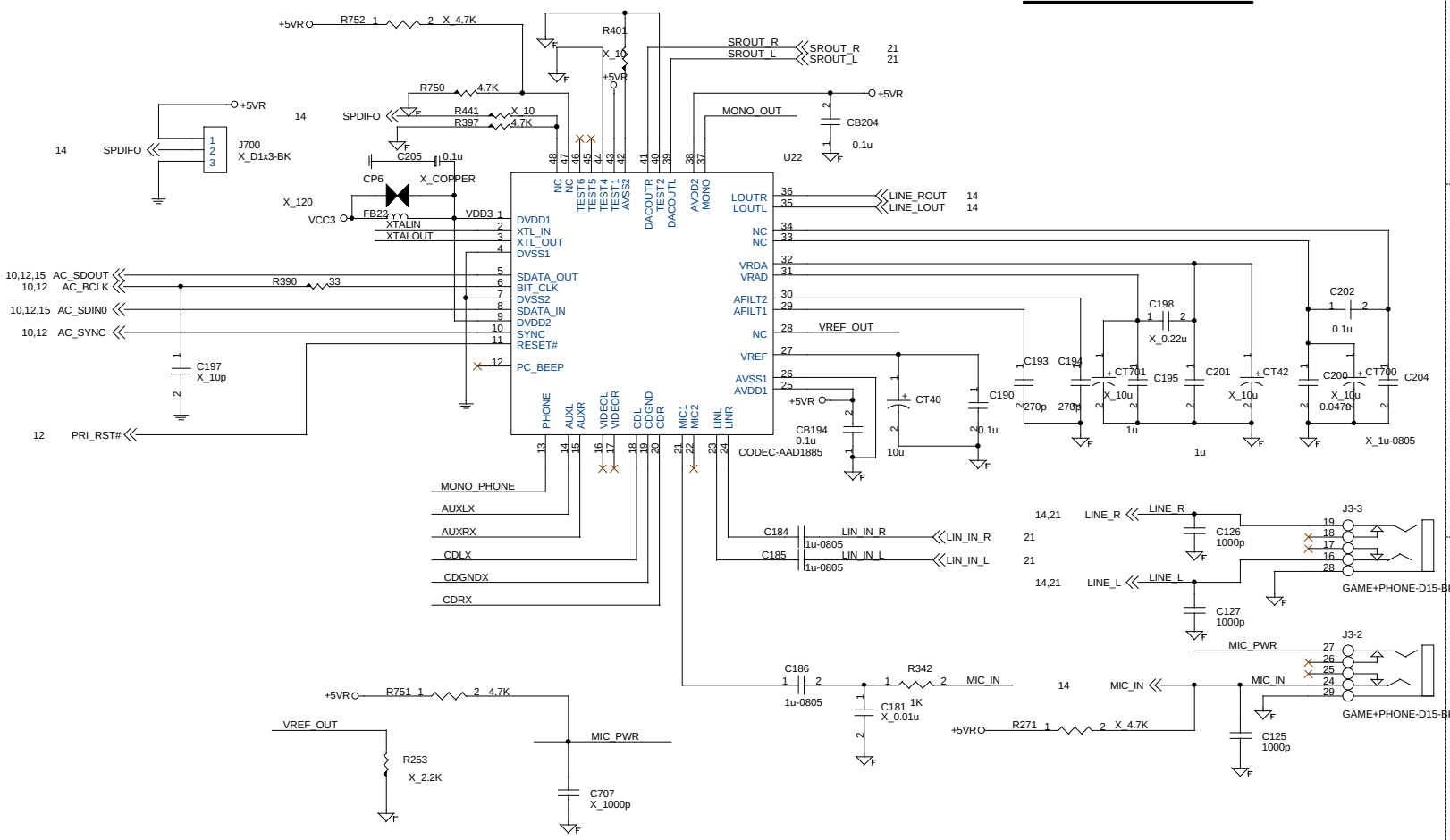
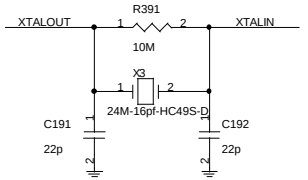
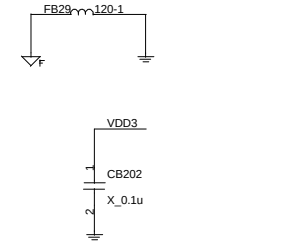
AD1885 AC97 CODEC



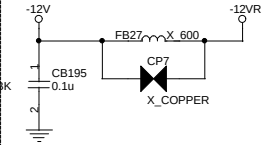
AUDIO CODE CRYSTAL CIRCUIT



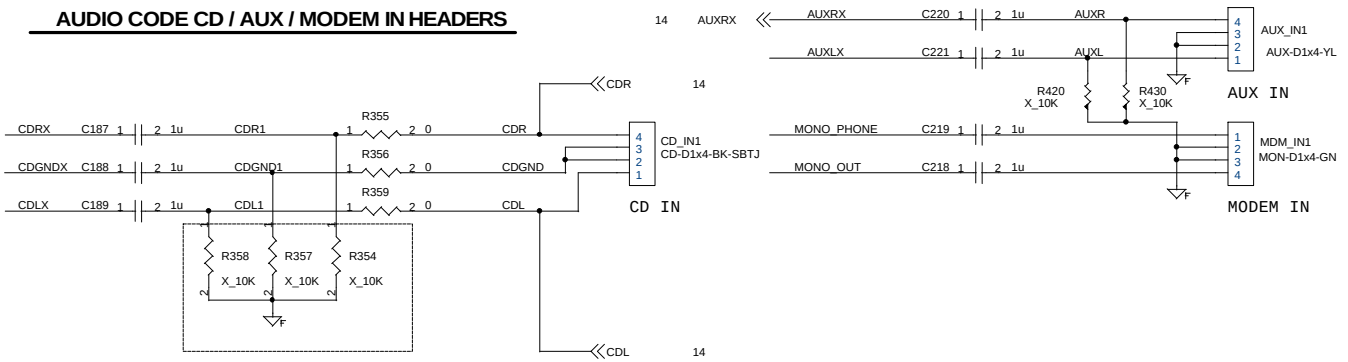
DECOUPLING CAPACITOR

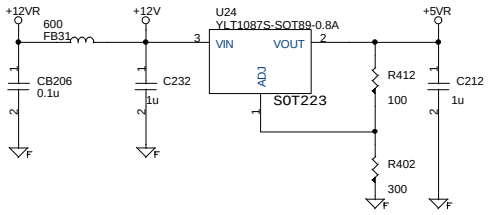


AUDIO CODE REGULATORS



AUDIO CODE CD / AUX / MODEM IN HEADERS





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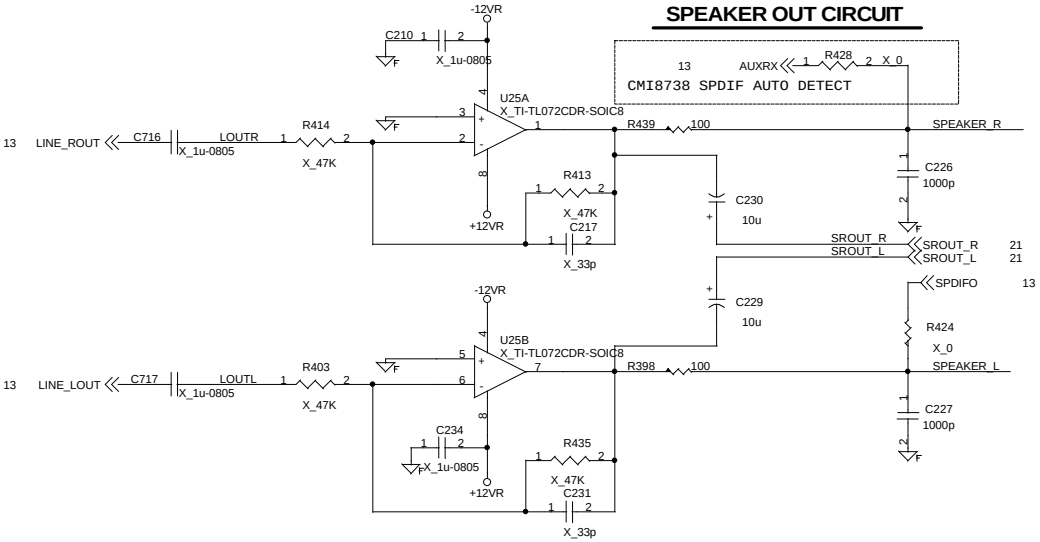
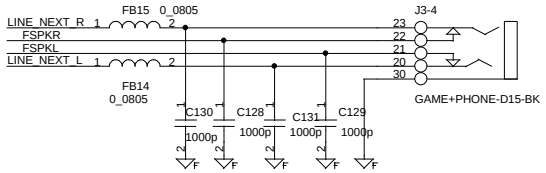
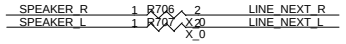
SPEAKER OUT CIRCUIT



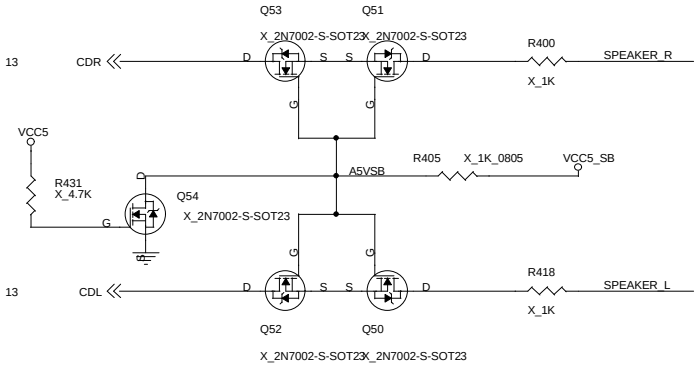
SPEAKER OUT JACK

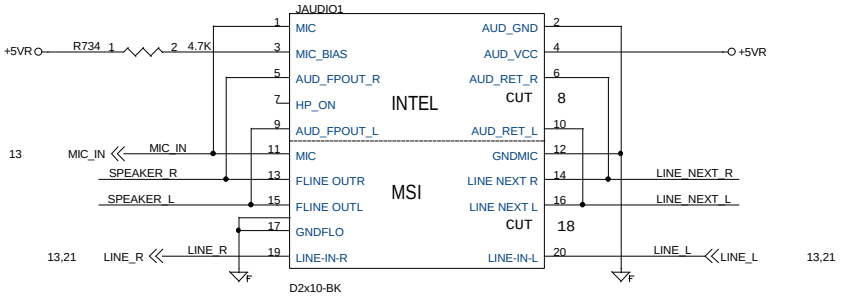


FOR MSI INTERNAL HEADER

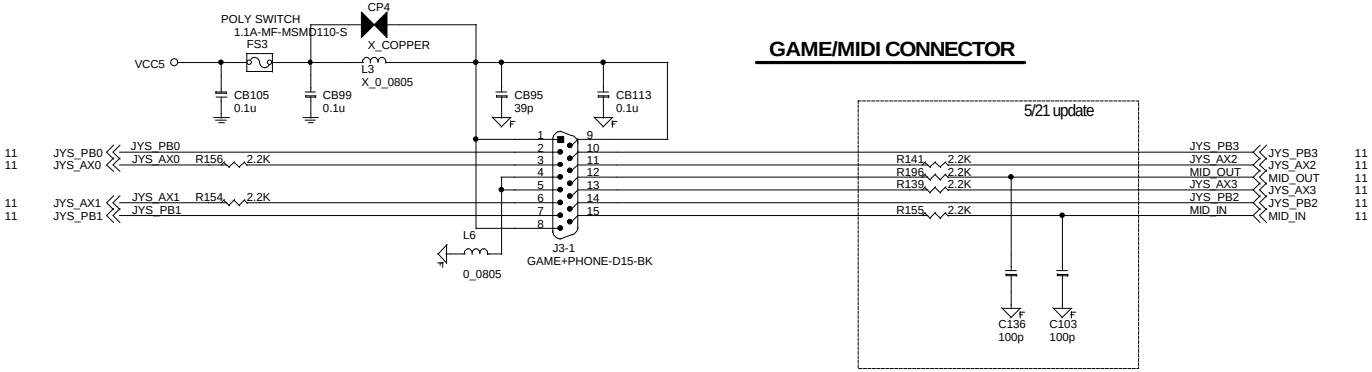


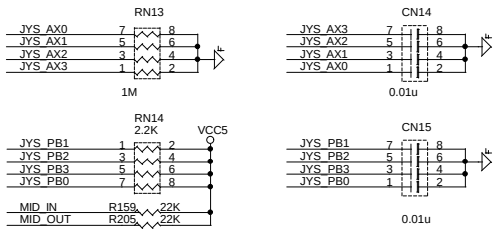
CD PANEL PLAY WITHOUT PC POWER_ON





GAME/MIDI CONNECTOR





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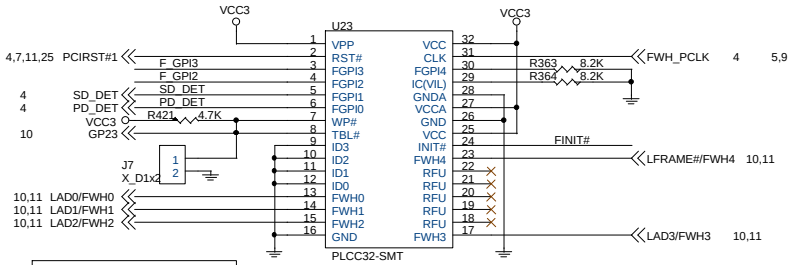
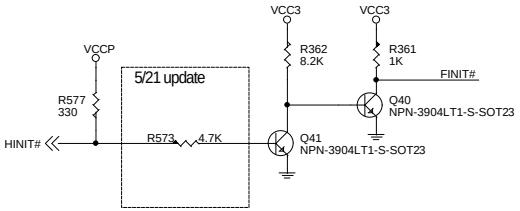
Firware Hub (FWH)

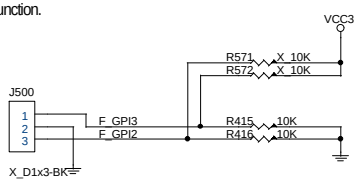


J7 BIOS Update	
SHORT	Locked
OPEN	Unlocked *

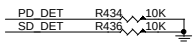
FWH INIT Signal Voltage Translation Block



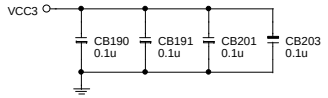
5/16 update
PB function.



FWH RESISTORS

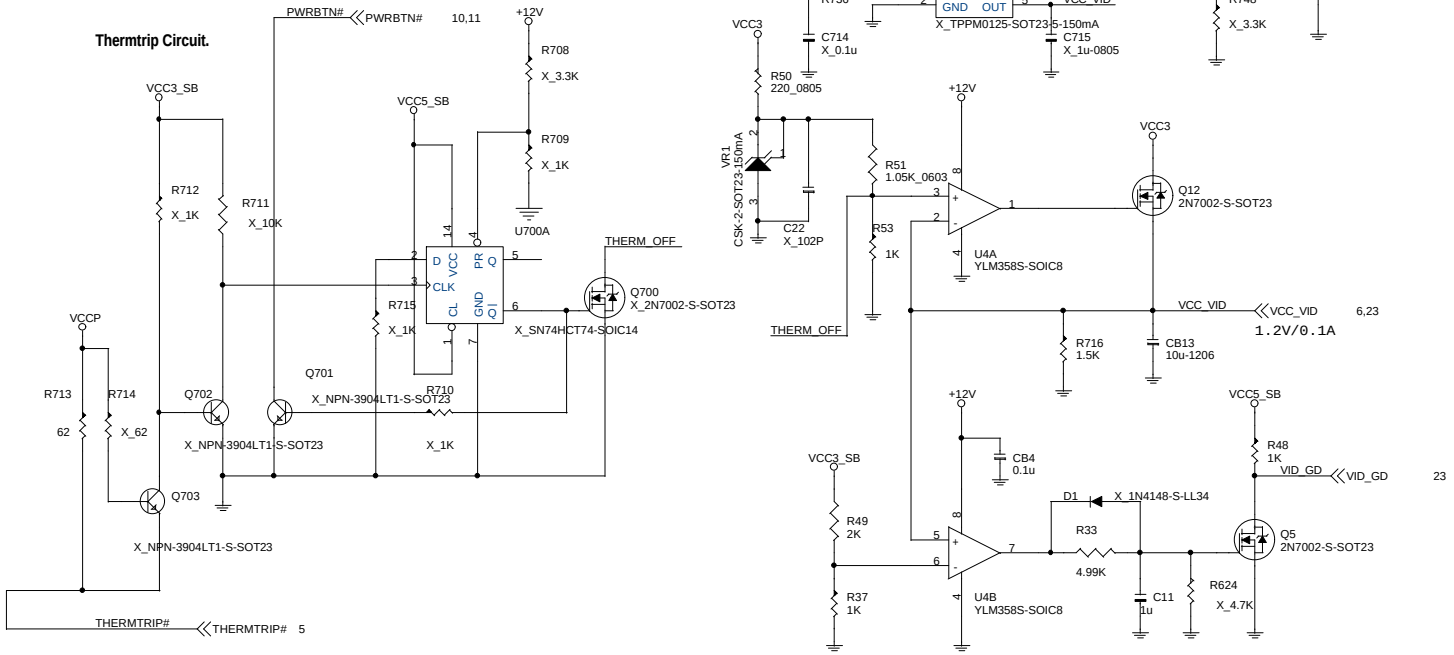


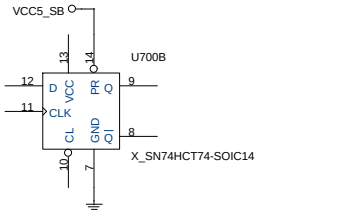
FWH DECOUPLING CAPACITORS



VCC_VID / VID_GOOD

Thermtrip Circuit.





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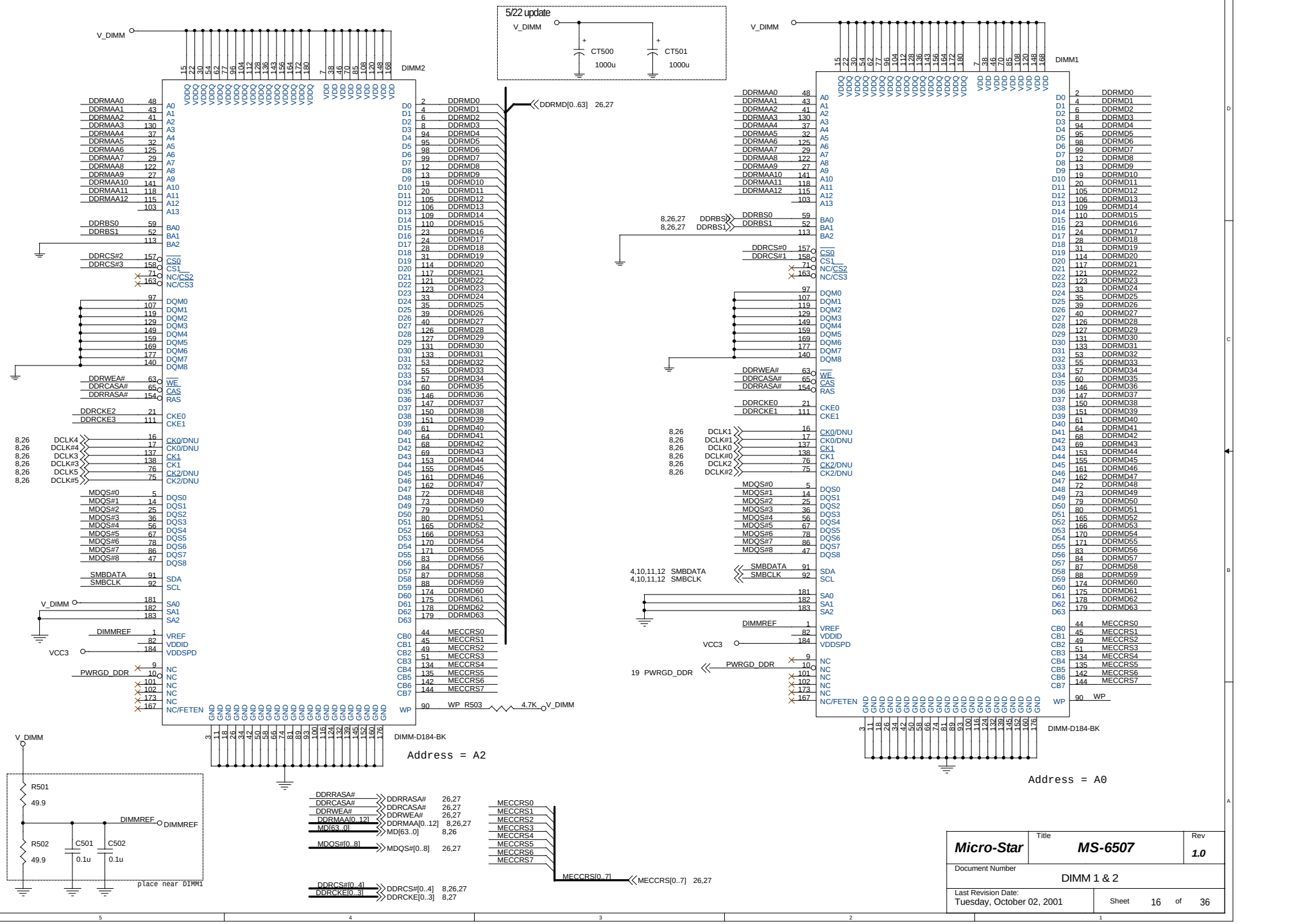
5/22 update
V_DIMM
CT500
1000u
CT501
1000u
DIMM2
DIMM1
DIMM-D184-BK
Address = A2
Address = A0
DDRMD[0..63] 26,27
WP R503 4.7K V_DIMM
R501 49.9
R502 49.9
C501 0.1u
C502 0.1u
DIMMREF
place near DIMM1
DDRRASA# 26,27
DDRCASA# 26,27
DDRWEA# 26,27
DDRMAA[0..12] 8,26,27
MD[63..0] 8,26
MDQS#[0..8] 26,27
DDRCS#[0..4] 8,26,27
DDRCKE[0..3] 8,27
MECCRS[0..7] 26,27
Micro-Star
MS-6507
1.0
DIMM 1 & 2
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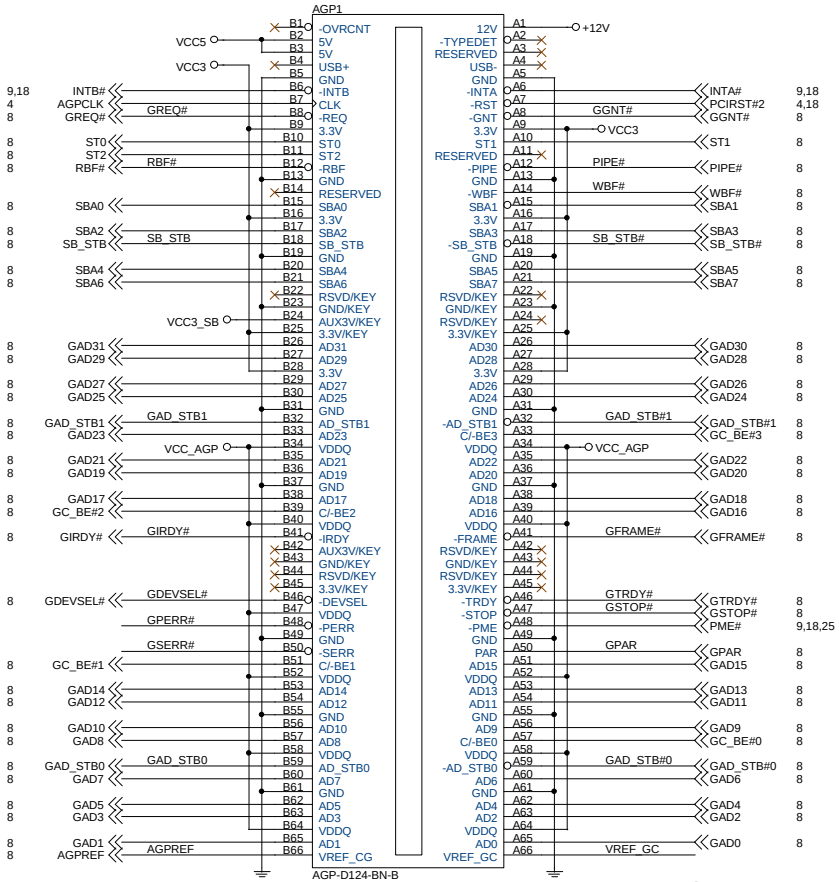
AGP UNIVERSAL 2X/4X SLOT(AGP VER:2.0 COMPLY)

VCC5 = 60mils trace / 15 mils space



VREF_GC:form the chipset to the graphics controller

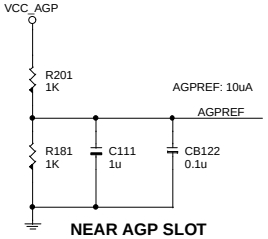
VREF_GC:form the graphics controller to the chipset

AGP Slot Imax

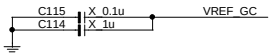
VCC_AGP 8.0A
VCC3 6.0A
VCC12 1.0A
VCC5 2.0A

INTA#
INTB#

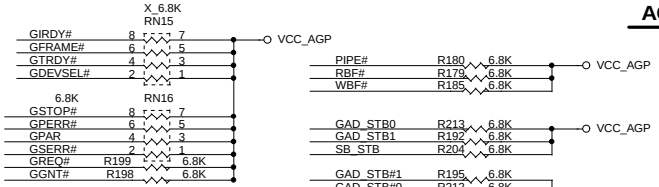
AGP SIGNAL REFERENCE CIRCUIT

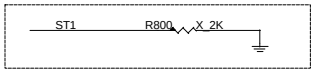


NEAR AGP SLOT



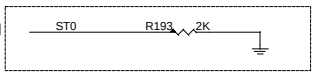
AGP TERMINATION RESISTORS





5/23 update

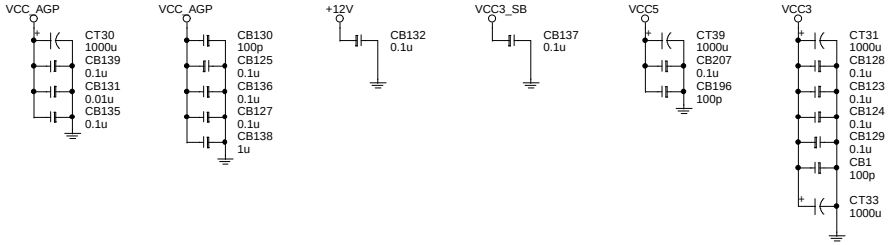
HI: SDRAM
LO:DDR



LESS 10MILS STUB TRACE LENGTH MUST BE FOLLOWING.

Place these resistors between PCI and AGP slot

AGP SLOT DECOUPLING CAPACITORS



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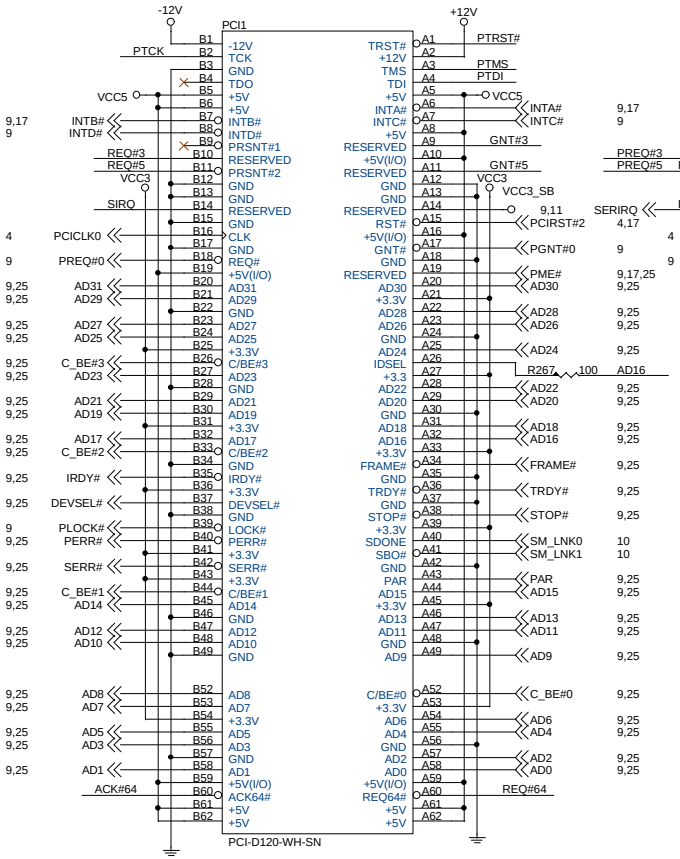
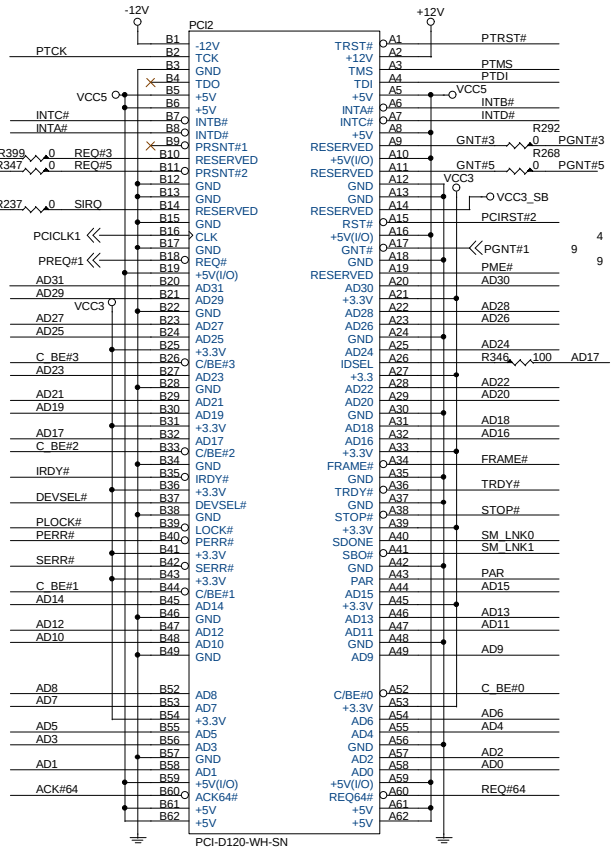
PCI SLOT 1 (PCI VER: 2.2 COMPLY)



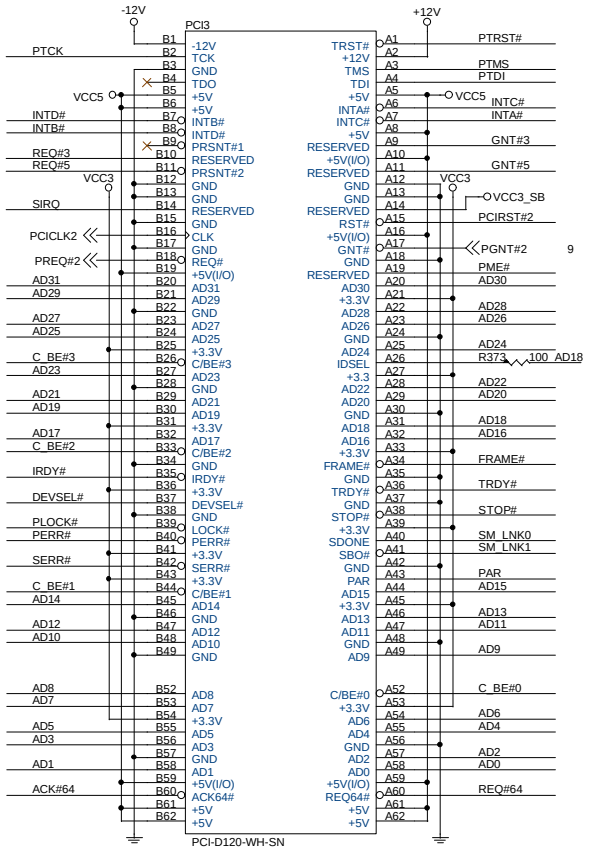
IDSEL = AD16
MASTER = PREQ0
INTA#

PCI SLOT 2 (PCI VER: 2.2 COMPLY)



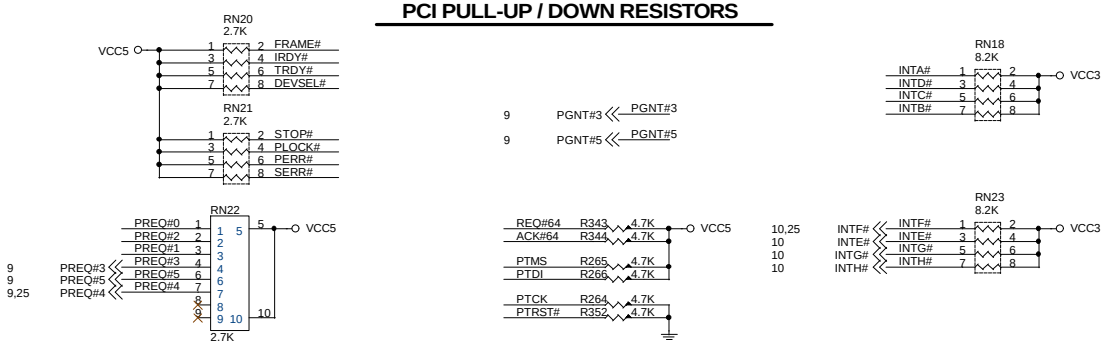
IDSEL = AD17
MASTER = PREQ1
INTB#

PCI SLOT 3 (PCI VER: 2.2 COMPLY)

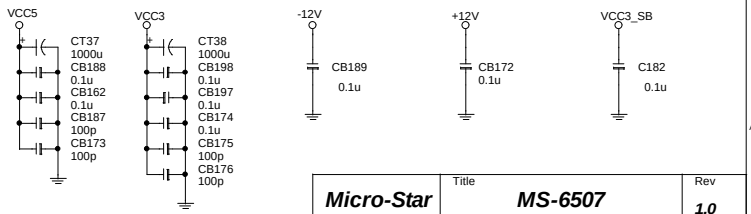


IDSEL = AD18
MASTER = PREQ2
INTC#

PCI PULL-UP / DOWN RESISTORS



PCI SLOT DECOUPLING CAPACITORS



Micro-Star	Title: MS-6507		Rev: 1.0
Document Number: PCI Slot 1 & 2 & 3			
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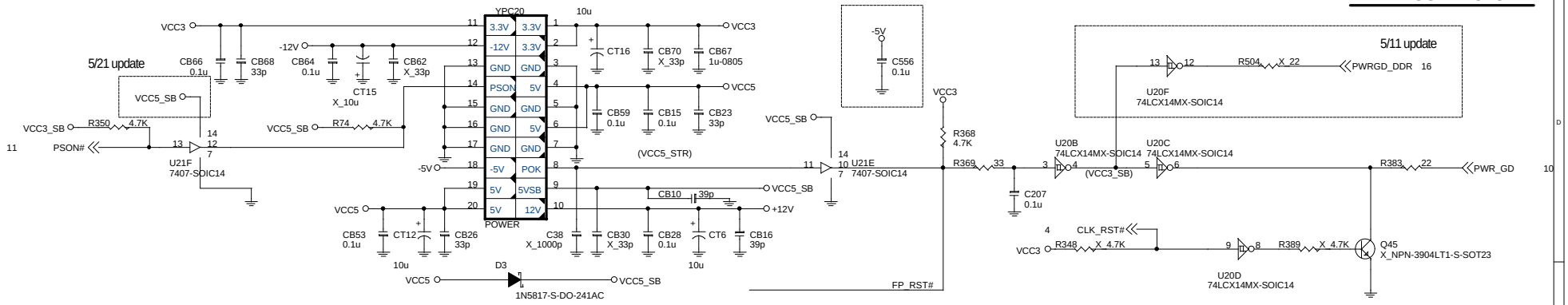
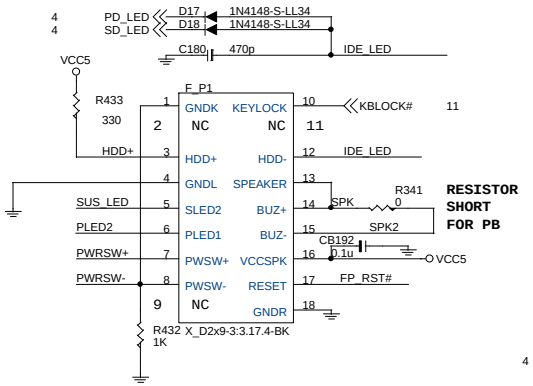
ATX CONNECTOR

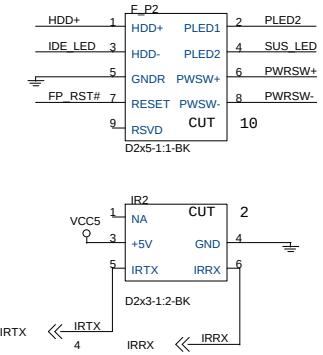
5/22 update for EMI use, close ATX connector



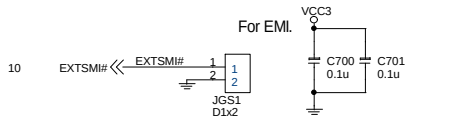
Brookdale FRONT PANEL-M

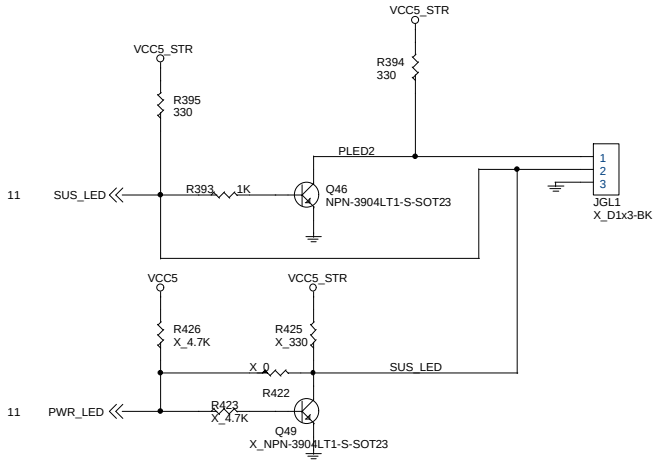


INTEL FRONT PANNEL PIN HEADER.

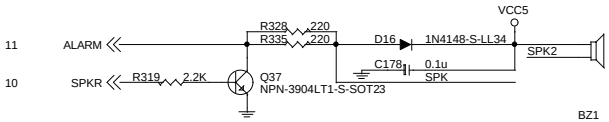


For EMI.

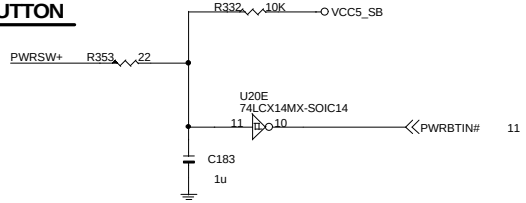




SPEAKER

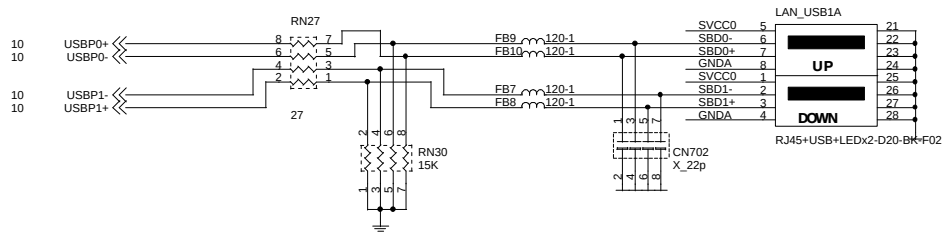


POWER BUTTON

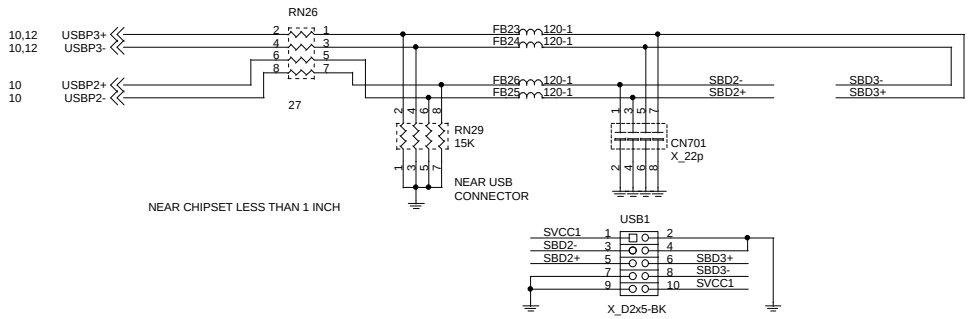


Micro-Star	Title: MS-6507	Rev: 1.0
	Document Number: Front Panel & Connector	
	Last Revision Date: Wednesday, October 03, 2001	Sheet 19 of 36

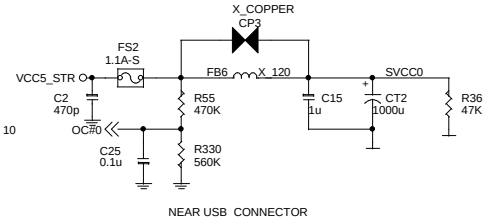
BACK PANEL USB CONNECTOR FOR USB PORT 0,1



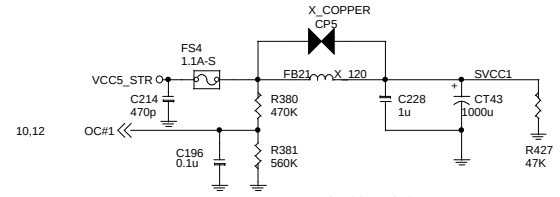
FRONT PANEL USB CONNECTOR FOR USB PORT 2,3



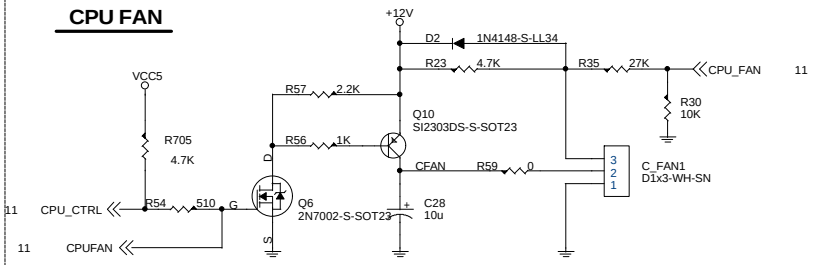
POWER CIRCUIT FOR USB PORT 0,1



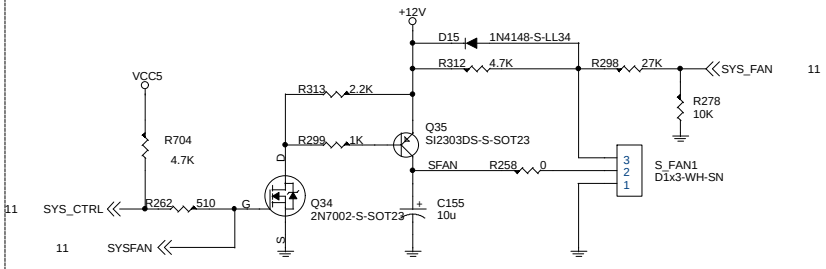
POWER CIRCUIT FOR USB PORT 2, 3



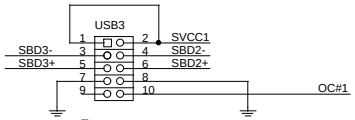
CPU FAN



SYSTEM FAN



INTEL USB FRONT PANNEL PIN HEADER



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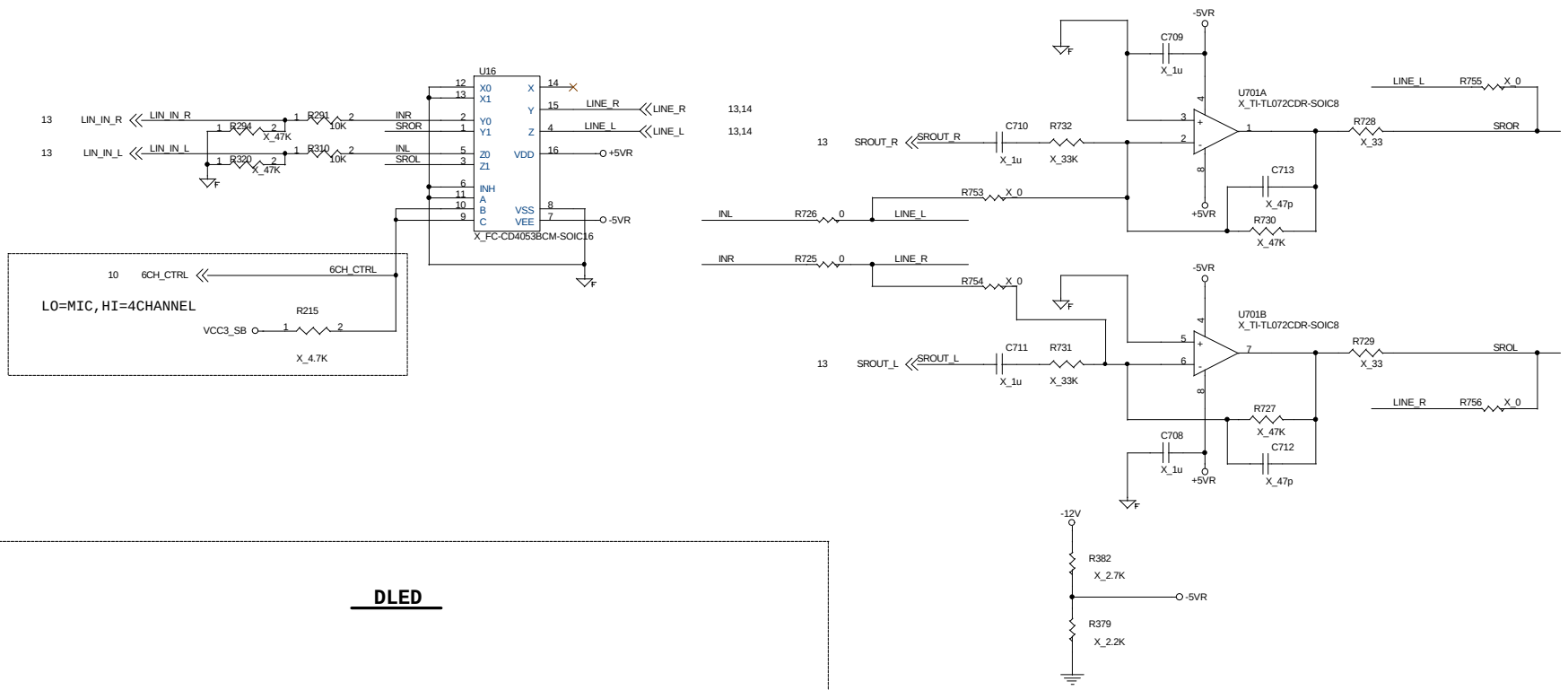
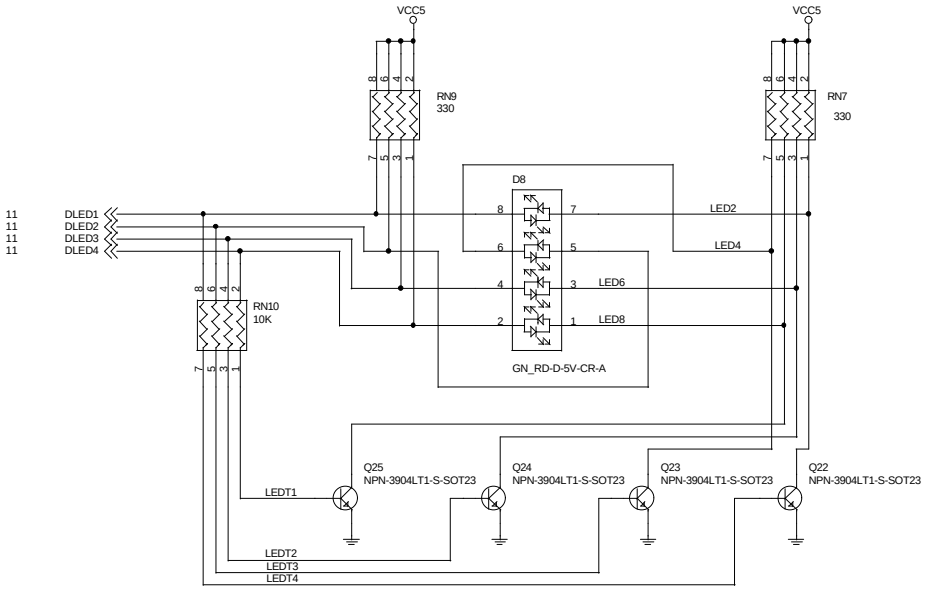
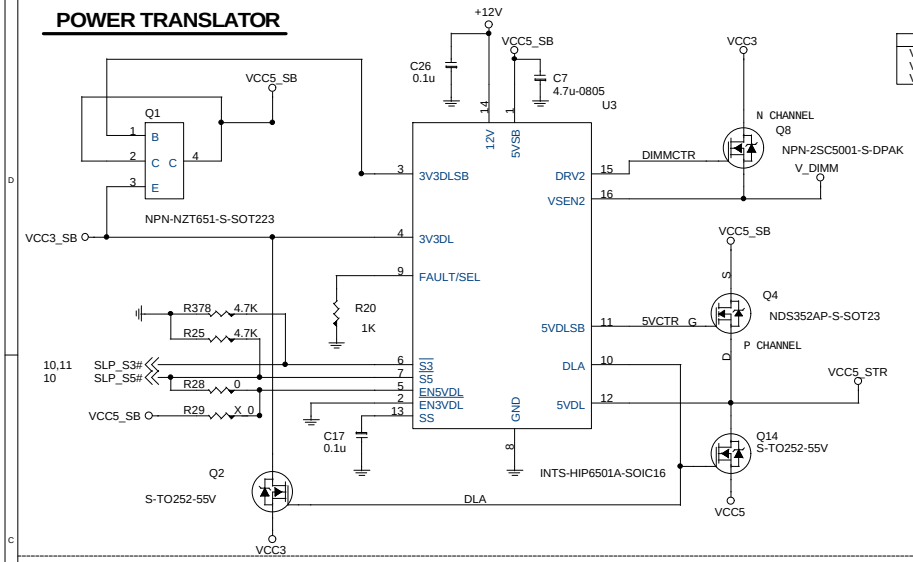


DLED



Micro-Star	Title: MS-6507	Rev: 1.0
Document Number: D-LED & 4 CHANNEL CONTROL		
Last Revision Date: Tuesday, October 02, 2001	Sheet 21 of 36	

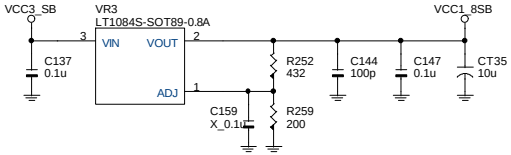
POWER TRANSLATOR



Power	S0	S3	S5
VCC3_SB	Main	Standby	Standby
VCC5_STR	Main	Standby	0V
VCC_DIMM	Main	Standby	0V

1.8V STANDBY POWER TRANSLATOR

(40mils trace / 20 mils space)



POWER CONSUMPTION

	VCCP	VCC_AGP	VCC1_8	VCC3_DIMM	VCC3	VCC5	VCC5_SB	+12V	-12V
CPU	69.0A	0	0	0	0	0	0	NOTE4	0
PMCH	2.4A	NOTE1	0.2A	2.0A	0	0	0	0	0
ICH2	0	0	NOTE3	0	NOTE3	0	NOTE3	0	0
CY28324	0	0	0	0	0	0	0	0	0
AD1885	0	0	0	0	0		0	0	0
FWH -SST	0	0	0	0			0		
W83627HF	0	0	0	0	0		0	0	0
HIP6301		0	0	0	0		0	0	0
HIP6602A		0	0	0			0	0	0
HIP6601A	0	0	0	0	0	0	0	0	0
SC1547	0	0	0	0	0	0			0
DIMM	0	0	0	NOTE2	0		NOTE2	0	0
AGP	0	8.0A	0	0	6.0A	2.0A	?	1.0A	0
PCI	0	0	0	0		0	0	0	0
USB	0		0	0		0			0
USB HUB	0	0	0	0	0	0	0	0	0
FAN	0	0	0	0	0	0	0	0	0
TTL	0	0	0	0	0	0	0	0	0
AMPLIFIER	0	0	0	0			0	0	0
OTHER	0	0	0	0	0		0		

NOTE1 --- MCH
VCC_AGP = VCC1_5 (1.5A) + VCC_AGP (0.37A)

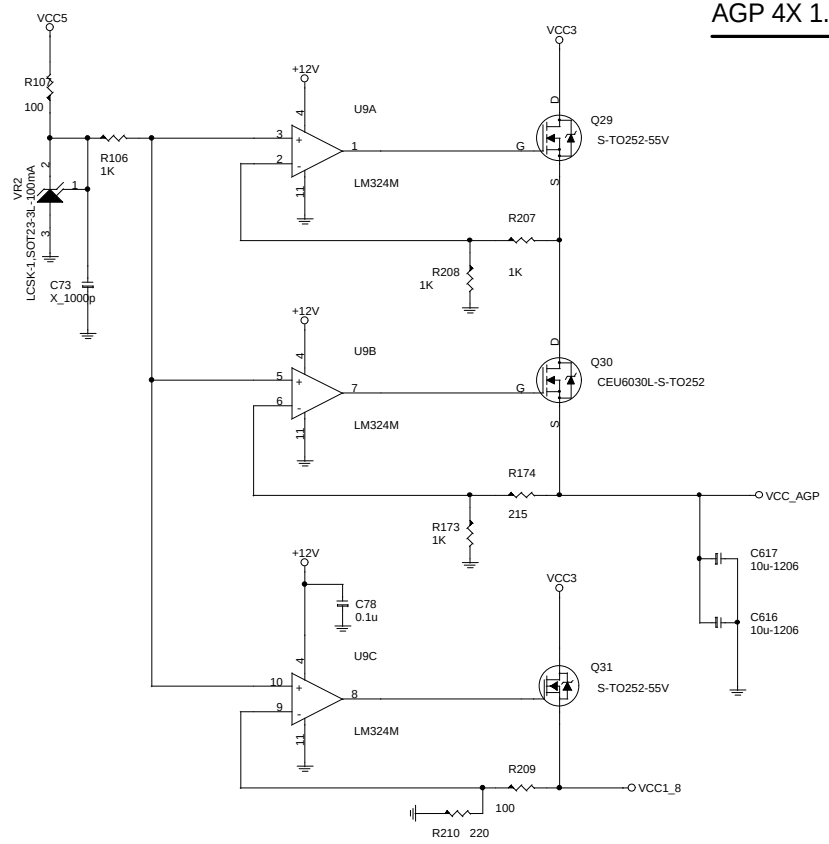
NOTE2 --- DIMM
S0 STATE --- 2.0A * 3 = 6.0A ---> VCC3
S1/S3 STATE --- 200mA * 3 = 600mA ---> VCC3_SB
VCC3_SB --> 600mA*3.3V/5V=396mA --> VCC5_SB

NOTE3 --- ICH2

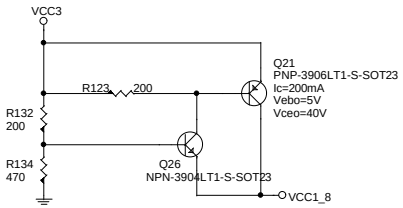
Power	S0	S1	S3/S4/S5
1.8V	300mA	100mA	N/A
1.8V_LAN	36mA	28mA	N/A
VCC1_8SB	45mA	30mA	7mA
VCC3	410mA	5mA	N/A
VCC3+562ET	230mA	210mA	N/A
VCC3_SB	25mA	0.6mA	N/A

VCC3_SB =
VCC1_8SB =
VCC5_SB = VCC3_SB + VCC1_8SB

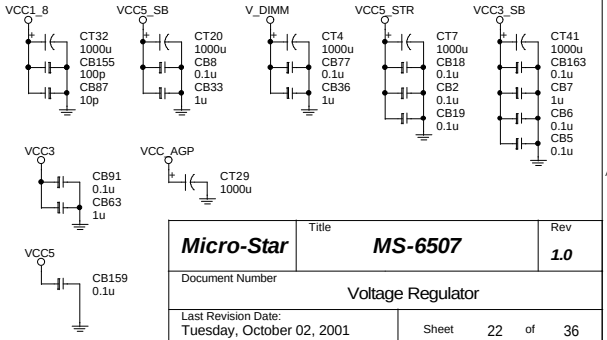
AGP 4X 1.5V POWER TRANSLATOR



1.8V/3.3V SEQUENCE CIRCUIT



REGULATORS OUTPUT DECOUPLING CAPACITORS



Micro-Star	Title: MS-6507	Rev: 1.0
	Document Number: Voltage Regulator	
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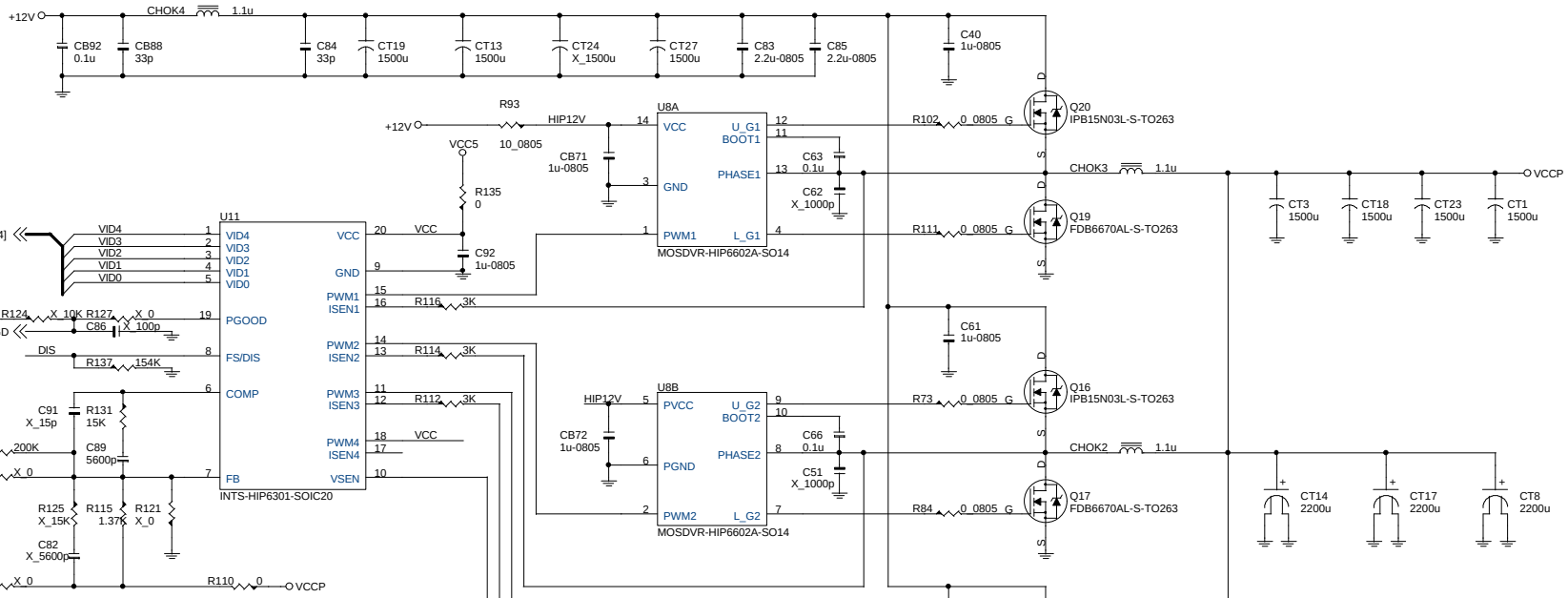
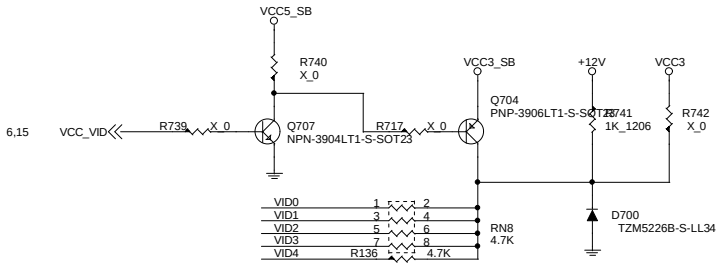


VID4	VID3	VID2	VID1	VID0	VDC(V)
1	1	1	1	0	1.100
1	1	1	0	1	1.125
1	1	1	0	0	1.150
1	1	0	1	1	1.175
1	1	0	1	0	1.200
1	1	0	0	1	1.225
1	1	0	0	0	1.250
1	0	1	1	1	1.275
1	0	1	1	0	1.300
1	0	1	0	1	1.325
1	0	1	0	0	1.350
1	0	0	1	1	1.375
1	0	0	1	0	1.400
1	0	0	0	1	1.425
1	0	0	0	0	1.450
0	1	1	1	1	1.475

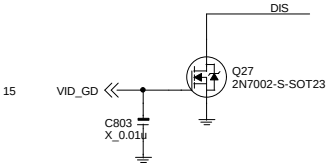
VID4	VID3	VID2	VID1	VID0	VDC(V)
0	1	1	1	0	1.500
0	1	1	0	1	1.525
0	1	1	0	0	1.550
0	1	0	1	1	1.575
0	1	0	1	0	1.600
0	1	0	0	1	1.625
0	1	0	0	0	1.650
0	0	1	1	1	1.675
0	0	1	1	0	1.700
0	0	1	0	1	1.725
0	0	1	0	0	1.750
0	0	0	1	1	1.775
0	0	0	1	0	1.800
0	0	0	0	1	1.825
0	0	0	0	0	1.850
1	1	1	1	1	OFF

HIP6301V DON'T NEED PULL HIGH
HIP6301 NEED PULL HIGH

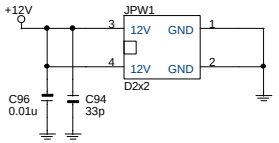
VID PULL-UP RESISTORS



PWM GOOD



ATX12V POWER CONNECTOR



Micro-Star	Title: MS-6507	Rev: 1.0
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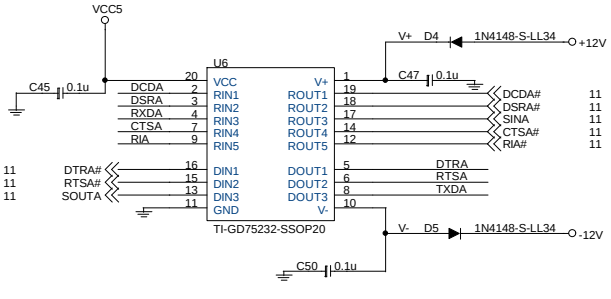
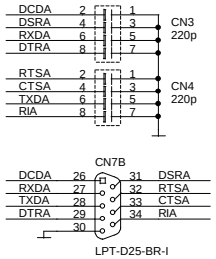
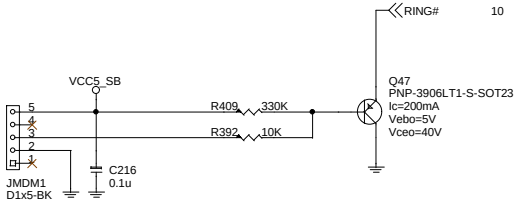
5/22 update

SERIAL PORT 1

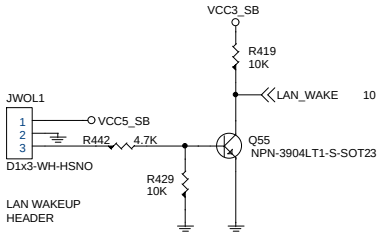




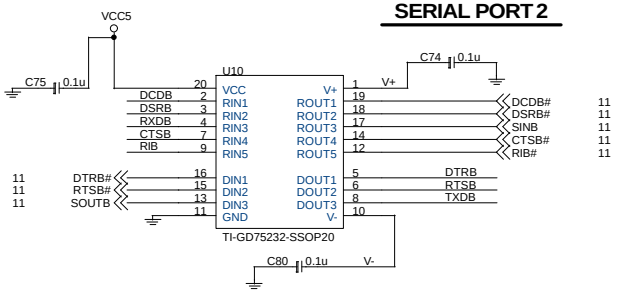
MODEM RING BLOCK

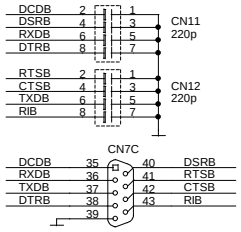


LAN WAKEUP BLOCK

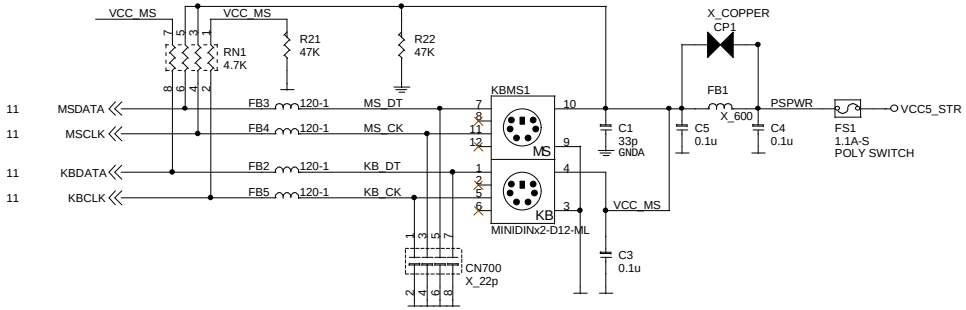


SERIAL PORT 2

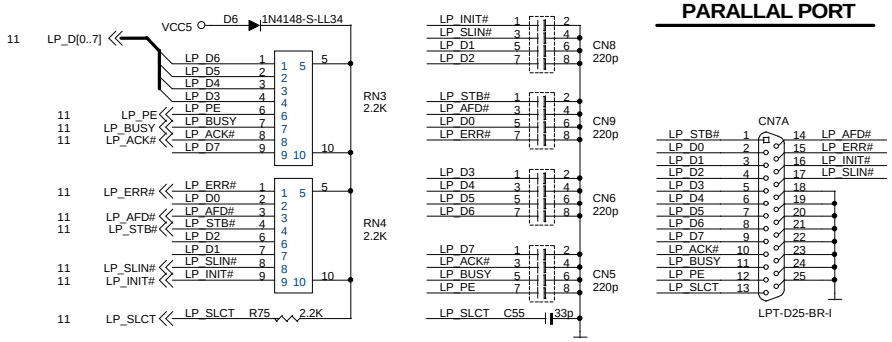




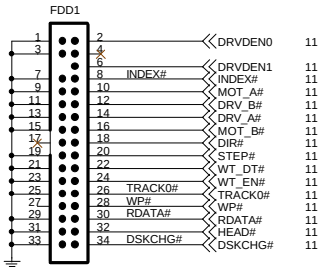
PS2 KEYBOARD & MOUSE CONNECTOR



PARALLAL PORT



FLOPPY CONNECTOR



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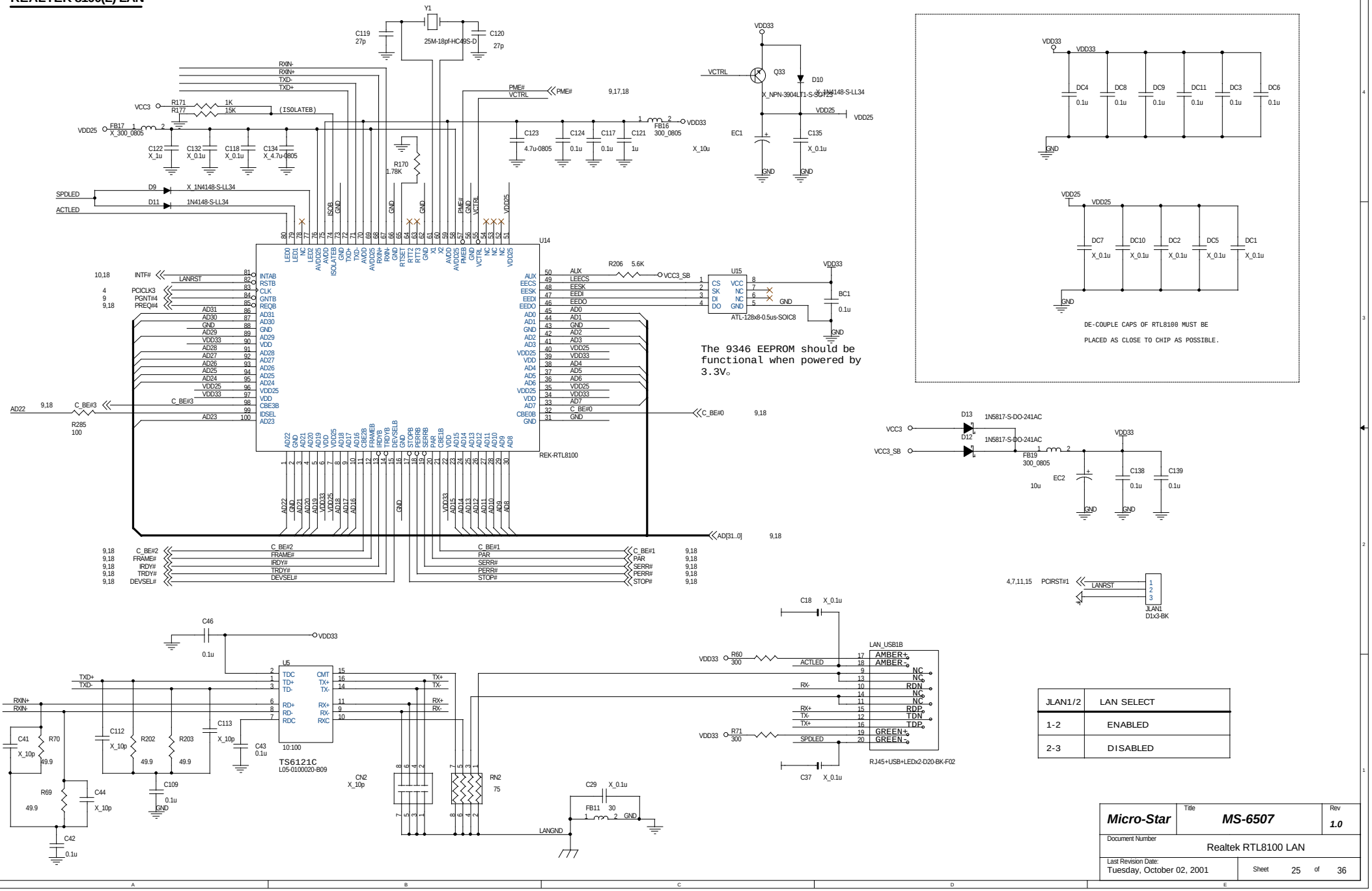
REALTEK 8100(L) LAN



JLAN1/2	LAN SELECT
1-2	ENABLED
2-3	DISABLED

Micro-Star	Title: MS-6507	Rev: 1.0
Document Number: Realtek RTL8100 LAN		
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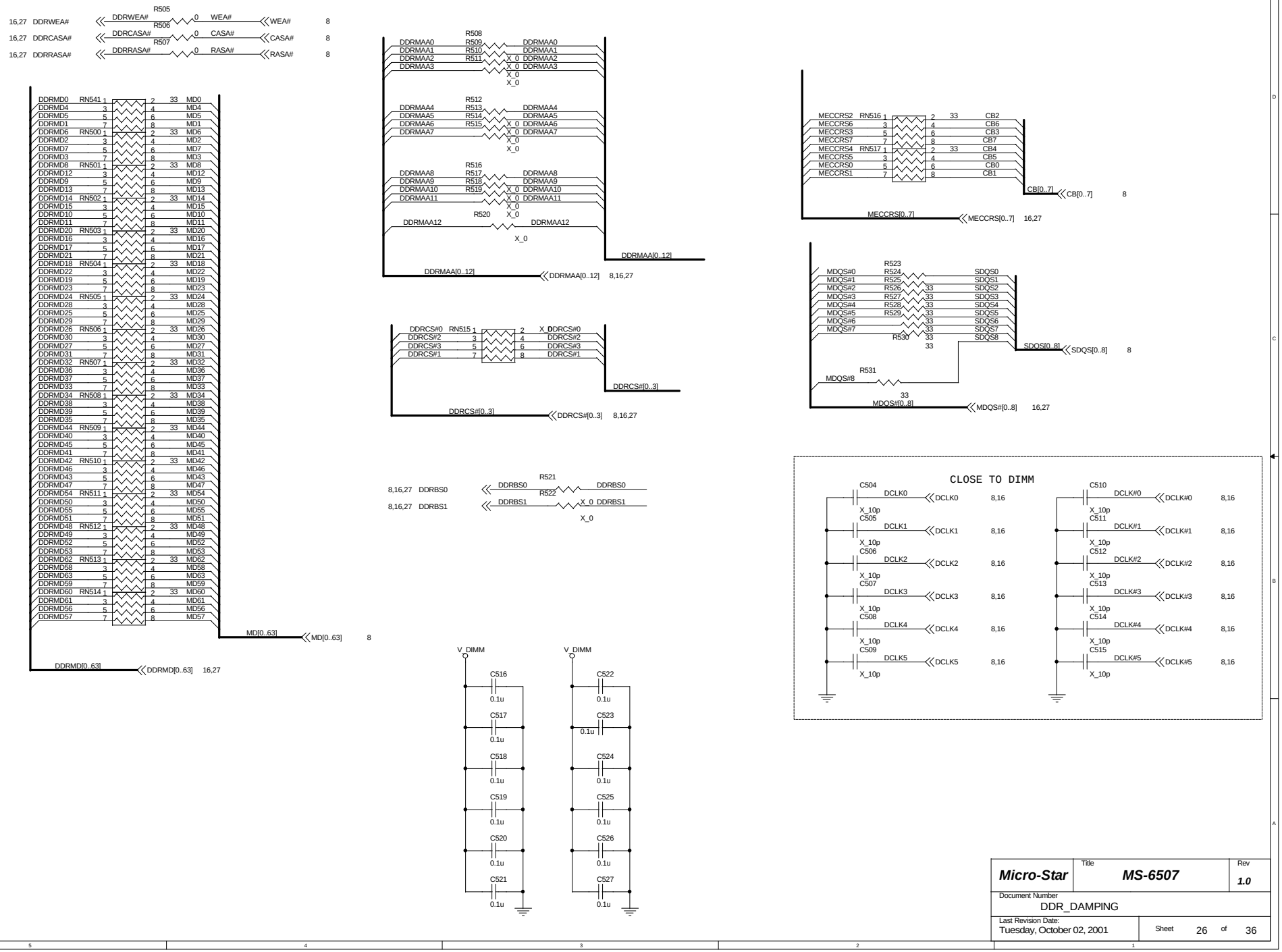
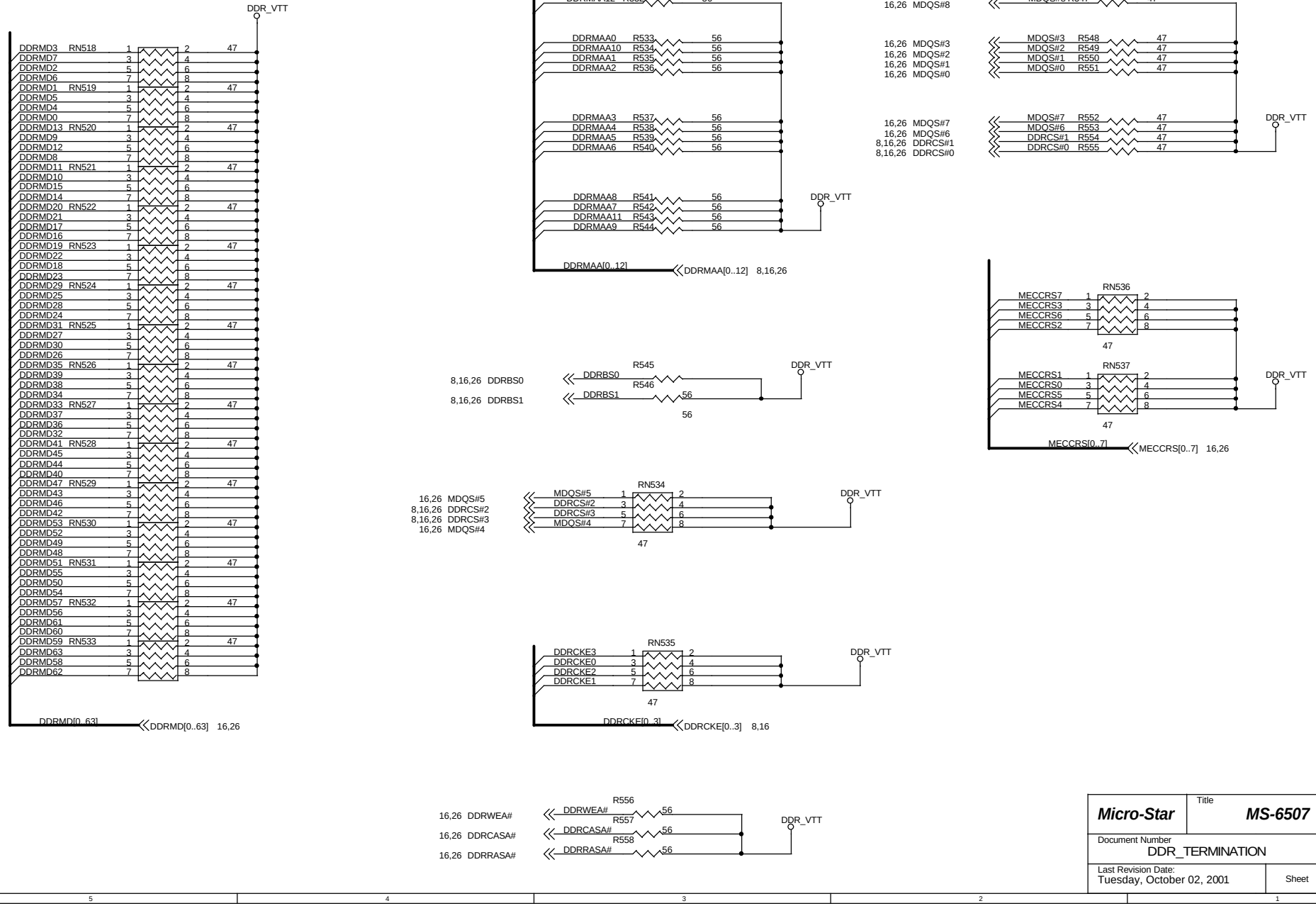
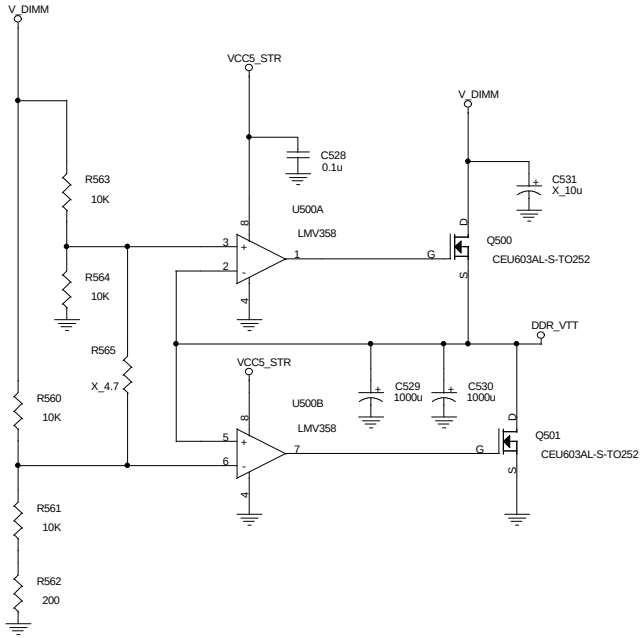
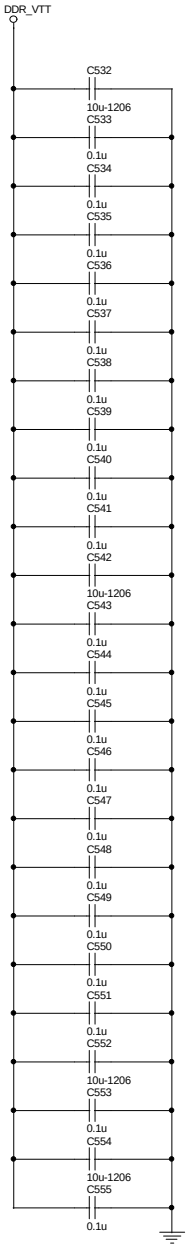


Micro-Star	Title: MS-6507	Rev: 1.0
Document Number: DDR_DAMPING		
Last Revision Date: Tuesday, October 02, 2001	Sheet 26 of 36	



Micro-Star	Title: MS-6507	Rev: 1.0
Document Number: DDR_TERMINATION		
Last Revision Date: Tuesday, October 02, 2001	Sheet 27 of 36	





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Document Number: DDR_T_POWER		
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Jumper Setting & Connector Setting

Jumper	Description	
J1	INTERUDER HEADER	
J2	CHASISS INTRUSION HEADER	
J3	AUDIO REAR PHONE JACK (LINE_IN, LINE_OUT, MIC_IN)	
J4	AUDIO AUX HEADER	
J5	AUDIO FRONT PANEL HEADPHONE JACK HEADER	
J6	AUDIO INTERNAL SPEAKER HEADER (ATAPI)	
J7	BIOS function	
1-2	Normal	(Default)
2-3	Configuration Mode	
REMOVED	Recovery	
JBAT1	CLEAR CMOS	
1-2	NORMAL	(Default)
2-3	CLEAR CMOS	
IR1	IR HEADER	
CD_IN1	CDROM HEADER (ATAPI)	
MDM_IN1	TELEPHONY HEADER (ATAPI)	
JP1	CNR RISER CODEC SELECT HEADER	
1-2	AUTO MODE	(Default)
2-3	PRIMARY AUDIO CODEC ONBOARD	

Connector	Description
U3	INTEL mPGA478-B CPU
IDE1	Primary
IDE2	Secondary
DIM1	SDRAM DIMM1
DIM2	SDRAM DIMM2
AGP1	AGP Slot
PCI1	PCI Slot1
PCI2	PCI Slot2
PCI3	PCI Slot3
COM1	Serial Port
COM2	Serial Port
LPT	Parallel Port
FDD1	Floopy
JMDM1	MODEM RING HEADER
JWOL1	LAN WAKEUP HEADER
KBMS1	PS/2 Keyboard and PS/2 mouse
C_FAN1	CPU FAN HEADER
S_FAN	System FAN HEADER
USB1	USB REAR CONNECTOR
USB2	USB INTERNAL HEADER
POWER	ATX Power
JSMB1	SMBUS HEADER
F_P1	Front Panel
Pin1	Power of Hard LED
Pin2	Power LED
Pin3	Hard LED
Pin4	Suspend LED
Pin5,8,12,13	GND
Pin6	Power Button
Pin7	Reset Button
Pin9	VCC
P_FAN1	ATX FAN HEADER
JPW1	ATX12V Power

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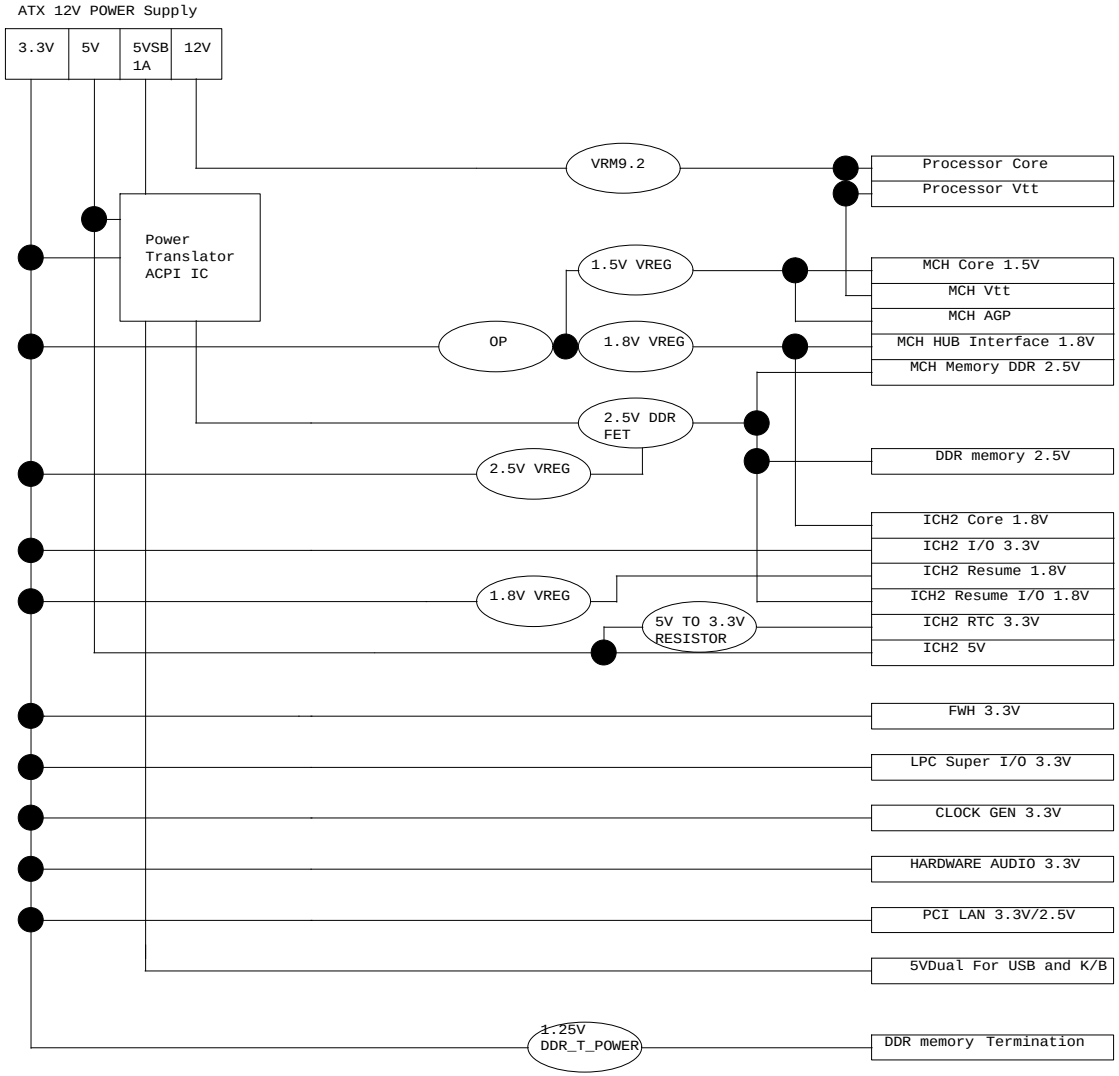
Power Delivery Map



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Pentium 4 Processor /Northwood mPGA 478

Source Synchronous Signal Group and the Associated Strobes

Signals	Associated Strobe
REQ[4:0],A[16:3]#	ADSTB0#
A[31:17]#	ADSTB1#
D[15:0]#,DBI0#	DSTBP0#,DSTBN0#
D[31:16]#,DBI1#	DSTBP1#,DSTBN1#
D[47:32]#,DBI2#	DSTBP2#,DSTBN2#
D[63:48]#,DBI3#	DSTBP3#,DSTBN3#

ADSTB0#
ADSTB1# should be +- 25mils

Signals	Length	Inaccuracy
Data	**2.0" to 10.0"**	+/- 100 mil
Address	**2.0" to 10.0"**	+/- 200 mil
Strobe	**2.0" to 10.0"**	+/- 25 mil
Clock	**2.0" to 10.0"**	Don't need

***** Delta=(CPU_pkglen.net-CPUpkglen.strobe)+(CS_pkglen.net-CS_pkglen.strobe)
Trace : 7 mil width 13mil space

Miscellaneous Signals

HL_STB/HL_STB#

Taces 5mils

20mils — HL[0:10]
HL_STB
15mils — HL_STB#
20mils — HL[0:10]

* Max Length : 8"
* STB and STB# Length must be equal

HL[10..0]

20mils — Others
15mils — HL[0:10]
15mils — HL[0:10]
20mils — Others

* Max Length : 8"
* Length must be matched within +/- 0." of the Strobe Signals

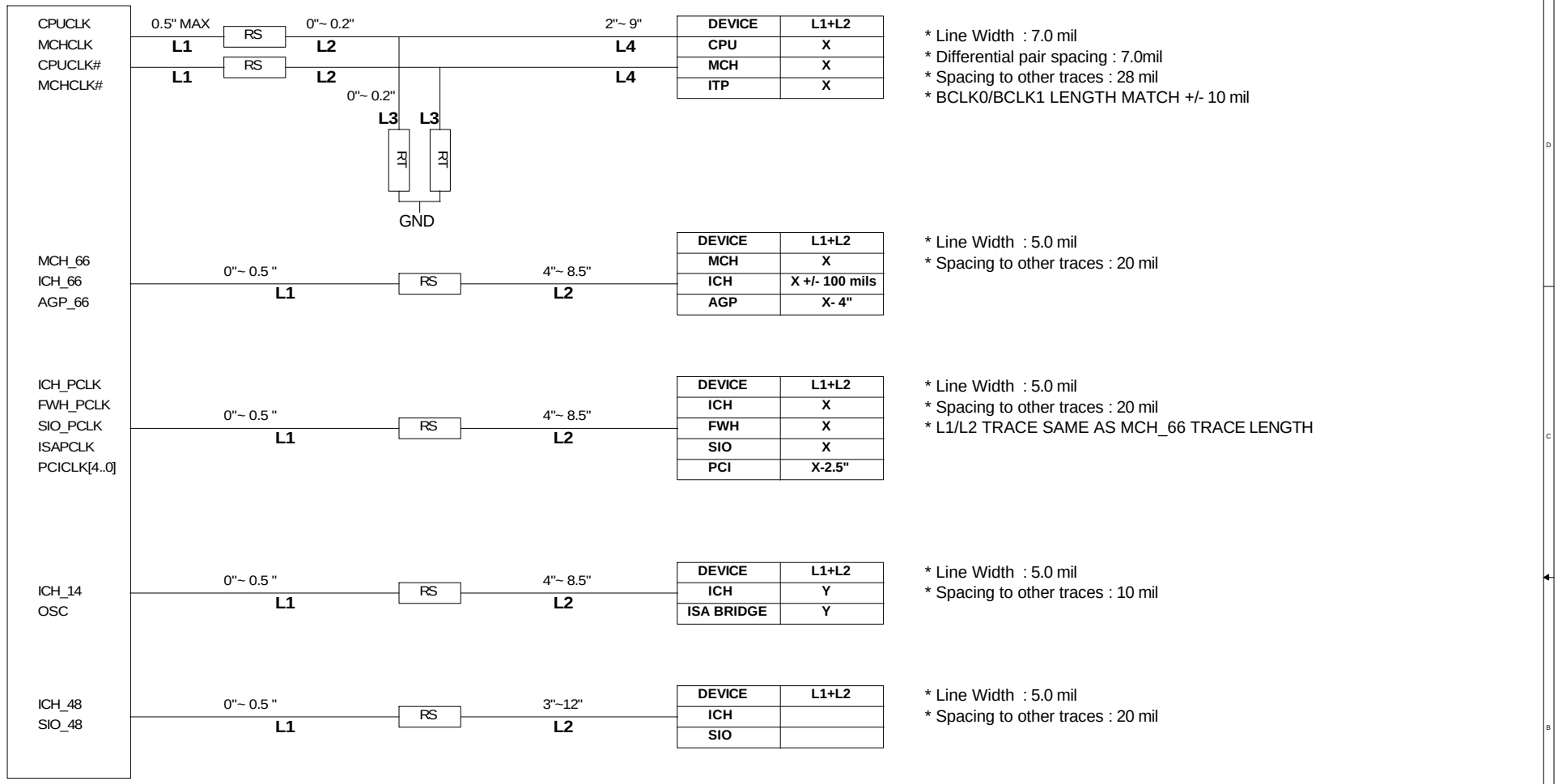
USB

*** USB Trace width : 9 mils**
*** USB Trace Spacing : 25 mils**
*** Differential USB Signlas Trace Spacing : 18 mils**
*** USB Power Trace must be 40mils width**

AGP

1X Timing group	2X/4X Timing group
AGPCLK PIPE# RBF# WBF# ST[2..0] GFRAME# GIRDY# GTRDY# GSTOP# GDEVSEL# GREQ# GGNT# GPAR	SET#1 GAD[15..0] GC_BE#[1..0] GAD_STB0 GAD_STB0# SET#2 GAD[31..16] GC_BE#[3..2] GAD_STB1 GAD_STB1# SET#3 SBA[7..0] SB_STB SB_STB#

SIGNALS	Maximum Length	Width	Space	Dismatch Length	Relative to
1X Timing group	7.5"	5 mil	5 mil	X	X
2X/4X Timing group SET#1	7.25"	5 mil	20 mil	+/- 0.125"	GAD_STB0 GAD_STB0#
2X/4X Timing group SET#2	7.25"	5 mil	20 mil	+/- 0.125"	GAD_STB1 GAD_STB1#
2X/4X Timing group SET#3	7.25"	5 mil	20 mil	+/- 0.125"	SB_STB SB_STB#
2X/4X Timing group SET#1	6"	5 mil	15 mil	+/- 0.25"	GAD_STB0 GAD_STB0#
2X/4X Timing group SET#2	6"	5 mil	15 mil	+/- 0.25"	GAD_STB1 GAD_STB1#
2X/4X Timing group SET#3	6"	5 mil	15 mil	+/- 0.25"	SB_STB SB_STB#



DEVICE	L1+L2
CPU	X
MCH	X
ITP	X

* Line Width : 7.0 mil
* Differential pair spacing : 7.0mil
* Spacing to other traces : 28 mil
* BCLK0/BCLK1 LENGTH MATCH +/- 10 mil

DEVICE	L1+L2
MCH	X
ICH	X +/- 100 mils
AGP	X- 4"

* Line Width : 5.0 mil
* Spacing to other traces : 20 mil

DEVICE	L1+L2
ICH	X
FWH	X
SIO	X
PCI	X-2.5"

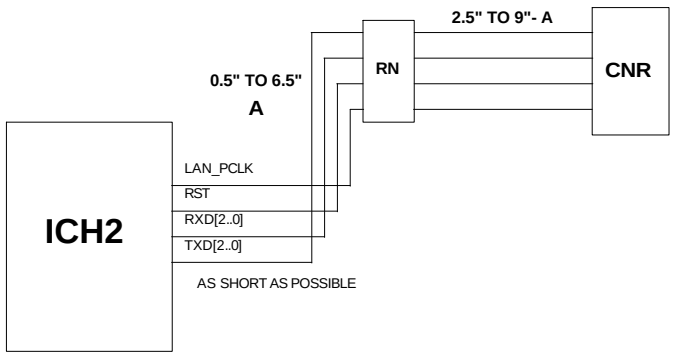
* Line Width : 5.0 mil
* Spacing to other traces : 20 mil
* L1/L2 TRACE SAME AS MCH_66 TRACE LENGTH

DEVICE	L1+L2
ICH	Y
ISA BRIDGE	Y

* Line Width : 5.0 mil
* Spacing to other traces : 10 mil

DEVICE	L1+L2
ICH	
SIO	

* Line Width : 5.0 mil
* Spacing to other traces : 20 mil



* Line Width : 7.0 mil
* Differential signls space : 14mils
* Differential signls length mismatch +/- 7mil

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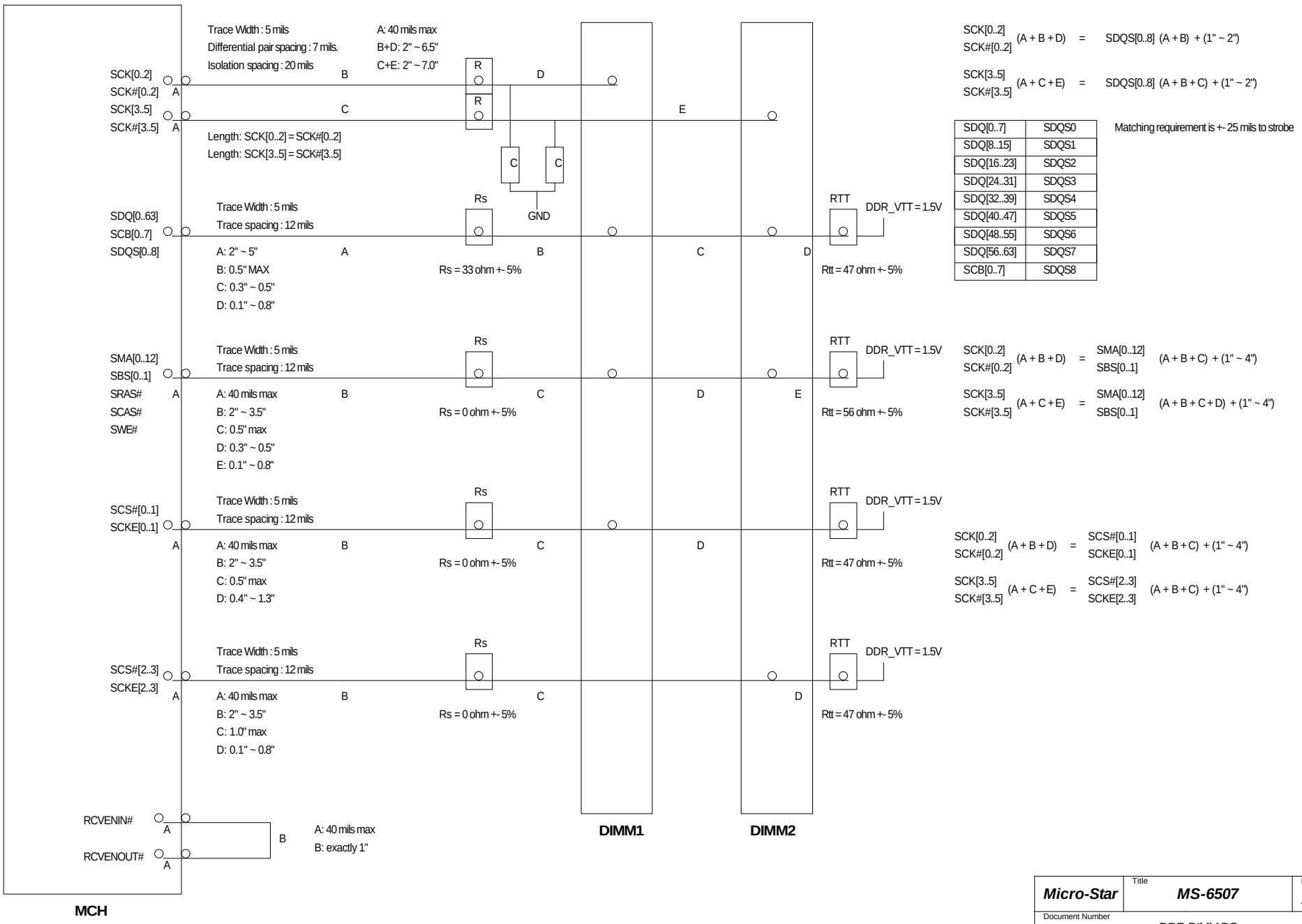

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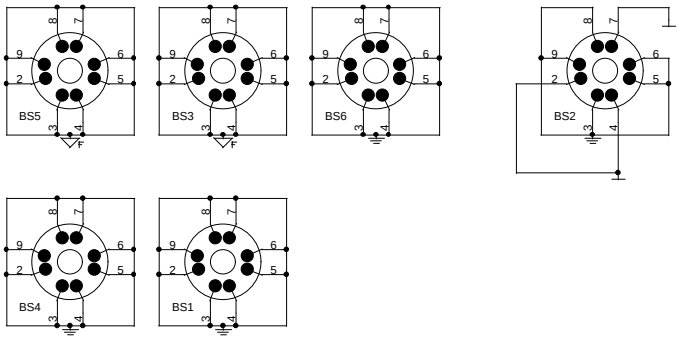
PCB OTHER COMPONENT



U3_X1 U4_X1

BS1_X1 BS2_X1 BS3_X1 BS4_X1

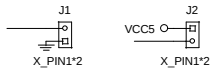
BS6_X1 BS7_X1 BS8_X1 BS9_X1

BS1_X1 BS2_X1 BS3_X1 BS4_X1 BS6_X1 BS7_X1 BS8_X1 BS9_X1

FM1 FM2 FM3 FM4 FM5 FM6 FM7 FM8

X_FM

SIMULATION TRACE



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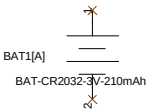
JBAT1 Clear CMOS	
1 - 2	Normal *
2 - 3	Clear CMOS

JBAT1(1-2)
JC-D2-GN

BAT SOCKET

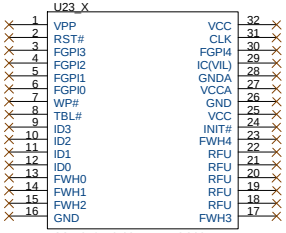


J7 BIOS Update	
SHORT	Locked
OPEN	Unlocked *

J7(1)
X_JC-D2-GN

BIOS

U23_X



SST-256K*8-33MHz-PLCC32

FRONT PANNEL BUZZER

F_P114-15
X_JC-D2-GN

JP2	On board codec
1-2	ENABLED
2-3	DISABLED

JP2(1-2)
JC-D2-GN

JLAN1	LAN SELECT
1-2	ENABLED
2-3	DISABLED

JLAN1(1-2)
JC-D2-GN

Audio Choice

JA1(13-16)
JC-D2x2-GN

MS6507 PCB

PCB

Heat sink

U12_X

Hooker

U12_X1 D1x3-1:2-BK
U12_X2 D1x3-1:2-BK
U12_X3 D1x3-1:2-BK
U12_X4 D1x3-1:2-BK

CN7(A) COM-D9-GN
CN7(B) COM-D9-GN

Micro-Star	Title: MS-6507	Rev: 1.0
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HISTORY

From 0A to 0B

1.Remove H/W Audio.
2.Add CNR Slot.
3.Reduce 1cm in width.
4.Add thermtrip circuit.
5.Fix no cpu can not shutdown issue.
6.Change super I/O to 627F compatible.
7.Fix power sequency issue.
8.Fix Glitch on DDR signal.
9.Modified Vcore power plane placement.
10.Add Intel front pannel pin header.

From 0B to 1.0

1.Modified D-LED circuit.
2.Modified core power placement.
3.Move C_FAN signal away from cpu.

Micro-Star	Title ***MS-6507***	Rev ***1.0***
Document Number	HISTORY	
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