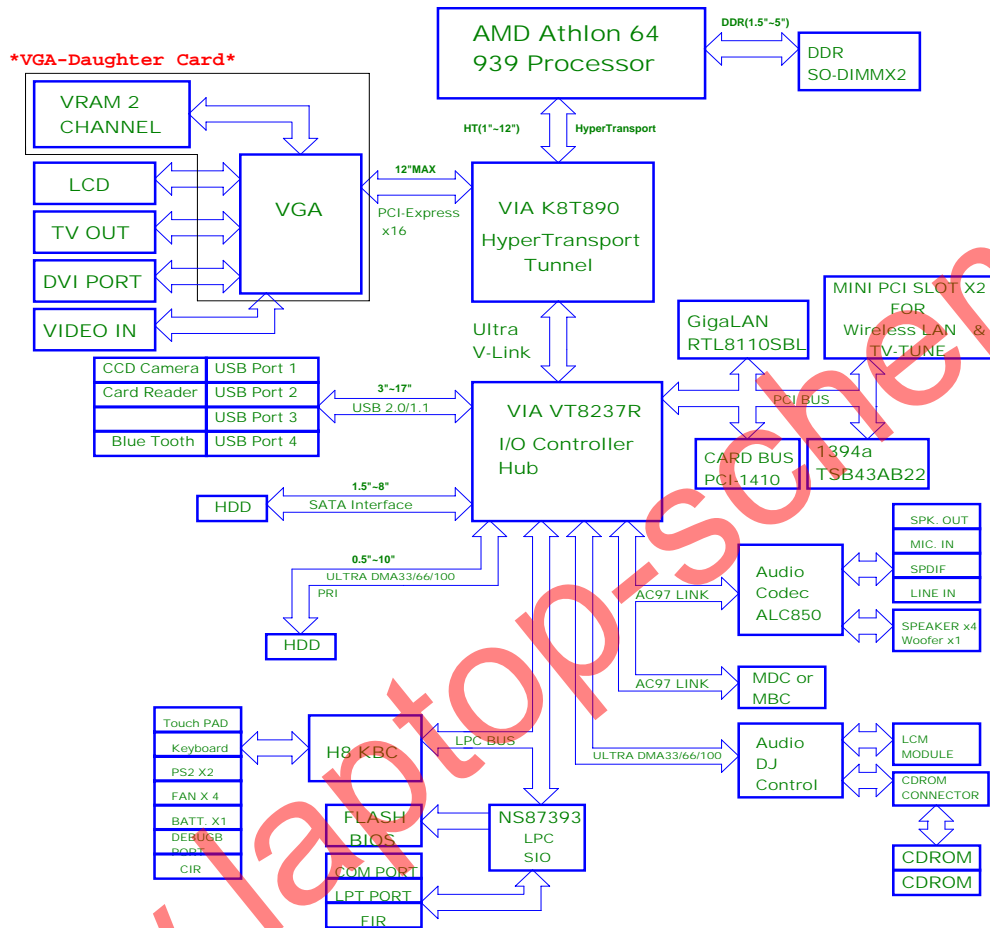
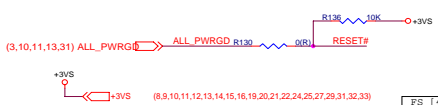
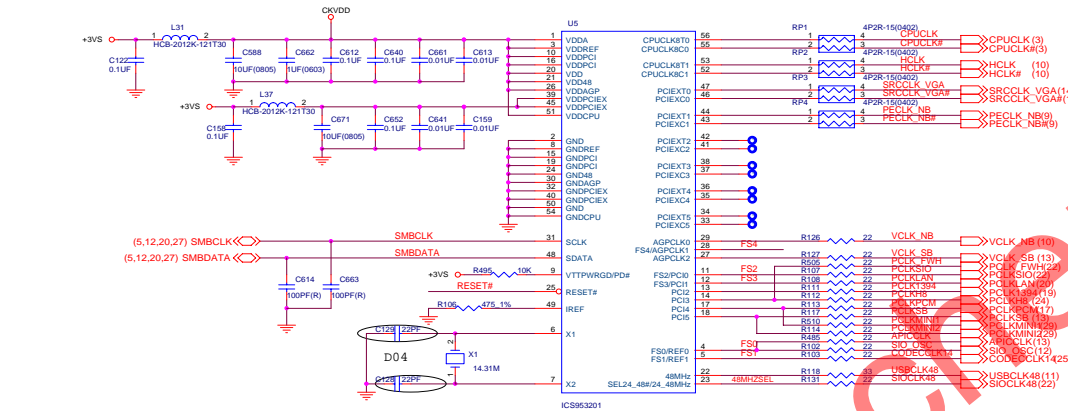


## BLOCK DIAGRAM



DEVICE	INT#	REQ#/GNT#	IDSEL
PCMCIA	INT#C	FREQ#0 PGNT#0	AD16
1394	INT#E	FREQ#1 PGNT#1	AD17
LAN	INT#F	FREQ#2 PGNT#2	AD19
MINI PCI-1	INT#B	FREQ#4 PGNT#4	AD21
MINI PCI-2	INT#G	FREQ#3 PGNT#3	AD20
K8T890	INT#H		

# CLOCK GENERATOR

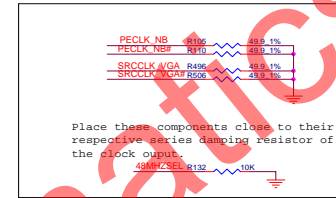


(3,10,11,13,31) ALL\_PWRGD → ALL\_PWRGD R130 0(R) RESET#

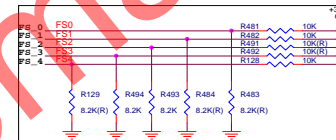
(8,9,10,11,12,13,14,15,16,19,20,21,22,24,25,27,29,31,32,33)

FS_[4:0]	CPU	PCIEEX	AGP	PCI	FS_[4:0]	CPU	PCIEEX	AGP	PCI
00000	100.90	100.90	67.27	33.63	10000	100.00	100.00	66.67	33.33
00001	133.90	100.43	66.95	33.48	10001	133.00	100.00	66.67	33.33
00010	168.00	100.80	67.20	33.60	10010	166.66	104.16	69.44	34.72
00011	202.00	101.00	67.33	33.67	10011	200.00	100.00	66.67	33.33
00100	100.20	100.20	66.80	33.40	10100	103.00	103.00	68.67	34.33
00101	133.50	100.13	66.75	33.38	10101	137.33	103.00	68.66	34.33
00110	166.70	100.04	66.68	33.34	10110	171.66	103.00	68.66	34.33
00111	200.40	100.20	66.80	33.40	10111	206.00	103.00	68.67	34.33
01000	160.00	100.00	66.67	33.33	11000	208.00	104.00	69.33	34.67
01001	202.00	101.00	67.33	33.67	11001	210.00	105.00	70.00	35.00
01010	230.00	105.00	70.00	35.00	11010	215.00	107.50	71.67	35.83
01011	212.00	106.00	70.67	35.33	11011	220.00	110.00	73.33	36.67
01100	270.00	107.25	67.50	33.75	11100	226.00	113.00	75.33	37.67
01101	225.00	112.50	75.00	37.50	11101	230.00	115.00	76.67	38.33
01110	266.67	100.00	66.67	33.33	11110	240.00	120.00	80.00	40.00
01111	300.00	112.50	75.00	37.50	11111	250.00	125.00	83.33	41.67

## Clock Synthesizer

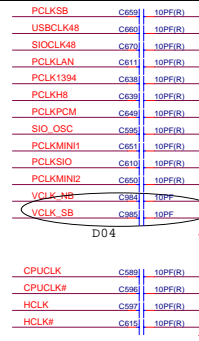


Place these components close to their respective series damping resistor of the clock output.



Place these components close to their respective series damping resistor of the clock output.

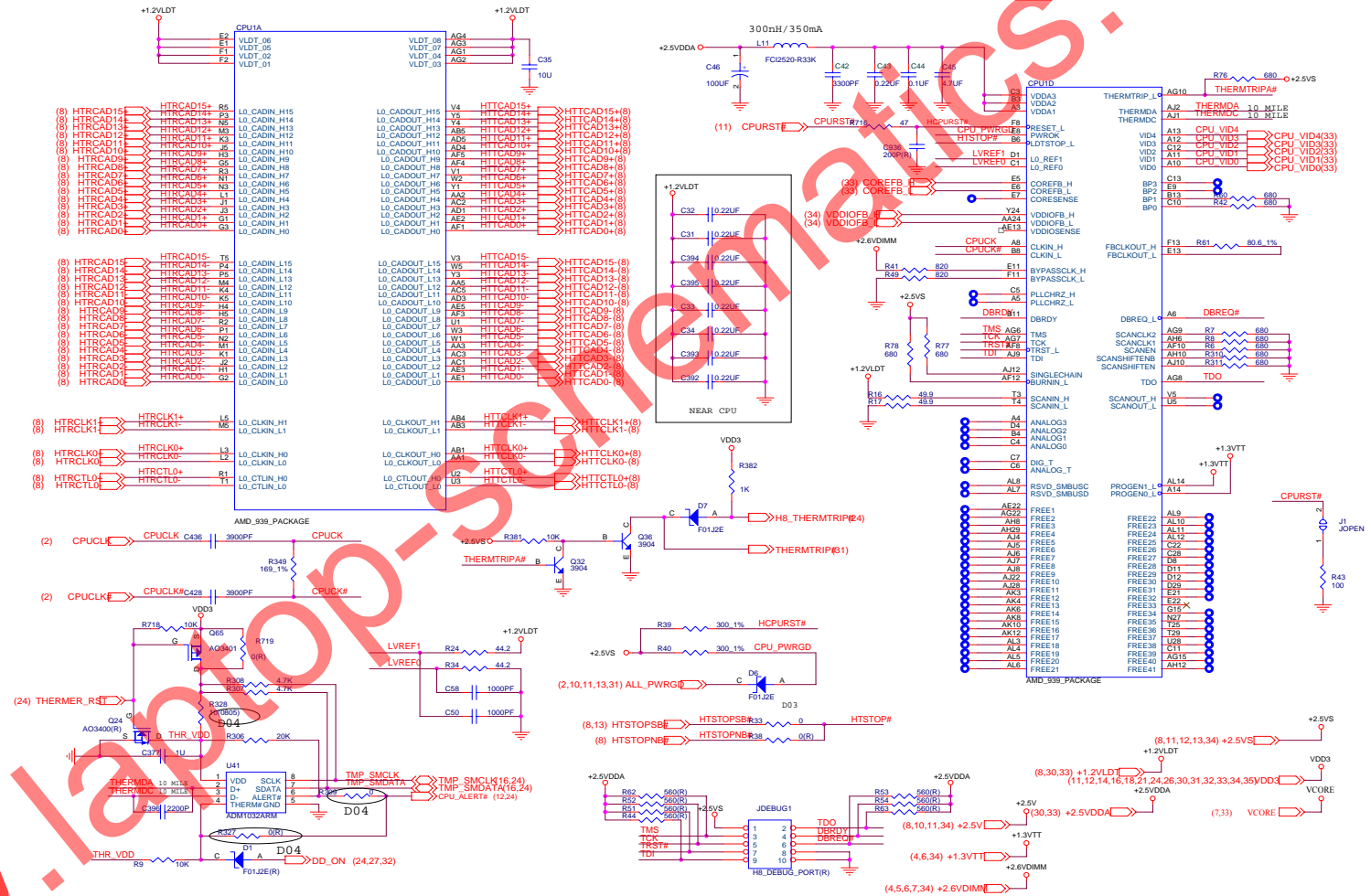
Set FS\_[4:0] value at 10011 for default frequencies as below:  
 CPU PCIEEX AGP PCI  
 200.00 100.00 66.67 33.33



Sheet 2 of 40  
**CLOCK  
 GENERATOR**

# CPU-1 CONTROL/ HYPERTRANSPORT

Sheet 3 of 40  
CPU-1 CONTROL/  
HYPERTRANSPORT



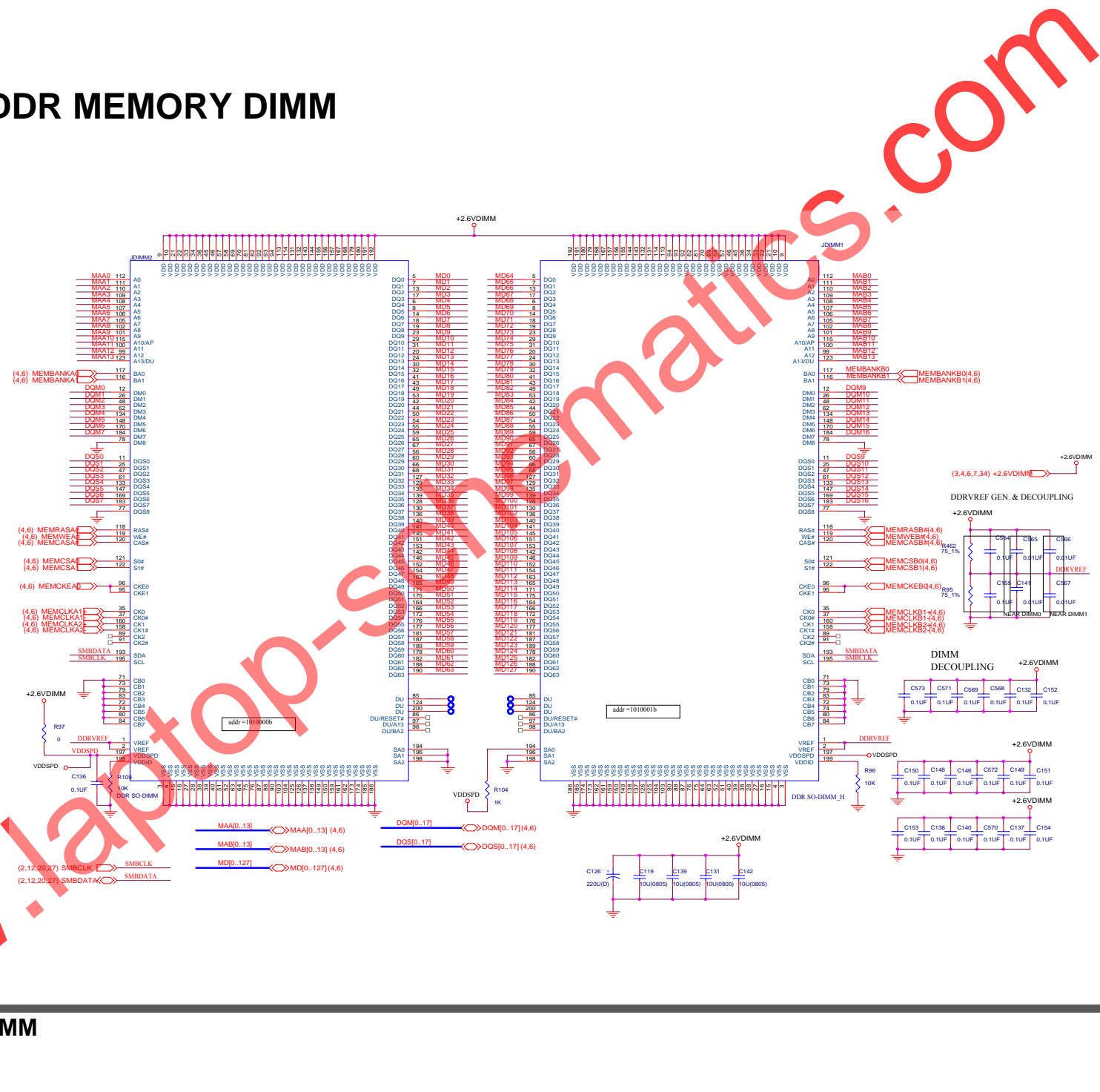
# CPU-2 MEMORY INTERFACE



Sheet 4 of 40  
CPU-2 MEMORY  
INTERFACE

# DDR MEMORY DIMM

Sheet 5 of 40  
DDR MEMORY  
DIMM

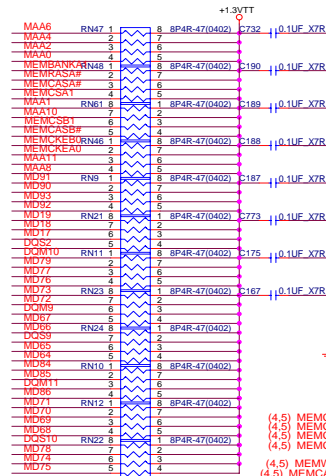
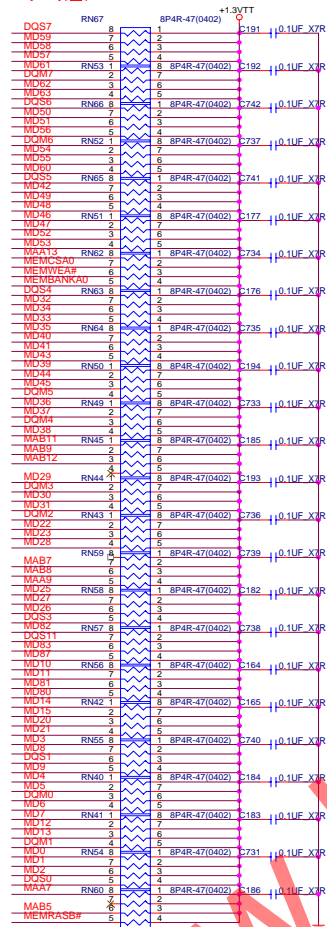


# DDR TERMINATION

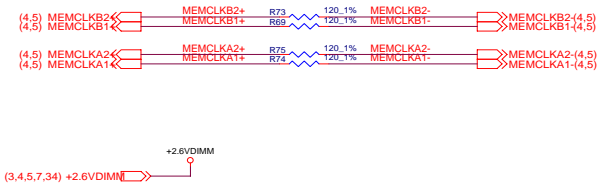
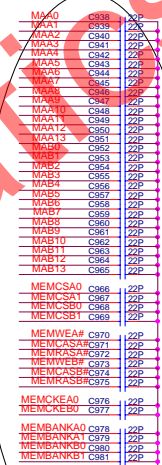
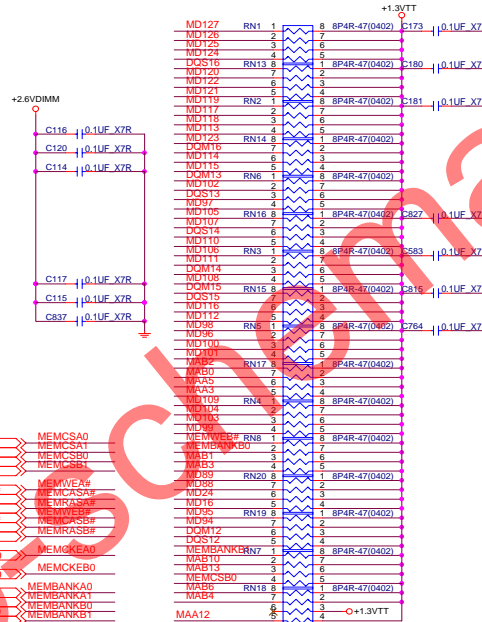
- (4,5) MD[0..127] <<> MD[0..127]
- (4,5) DQM[0..17] <<> DQM[0..17]
- (4,5) DQS[0..17] <<> DQS[0..17]
- (4,5) MAA[0..13] <<> MAA[0..13]

- (4,5) MAB[0..13] <<> MAB[0..13]
- +1.3VTT
- (3,4,34) +1.3VTT <<>

## DDR Termination



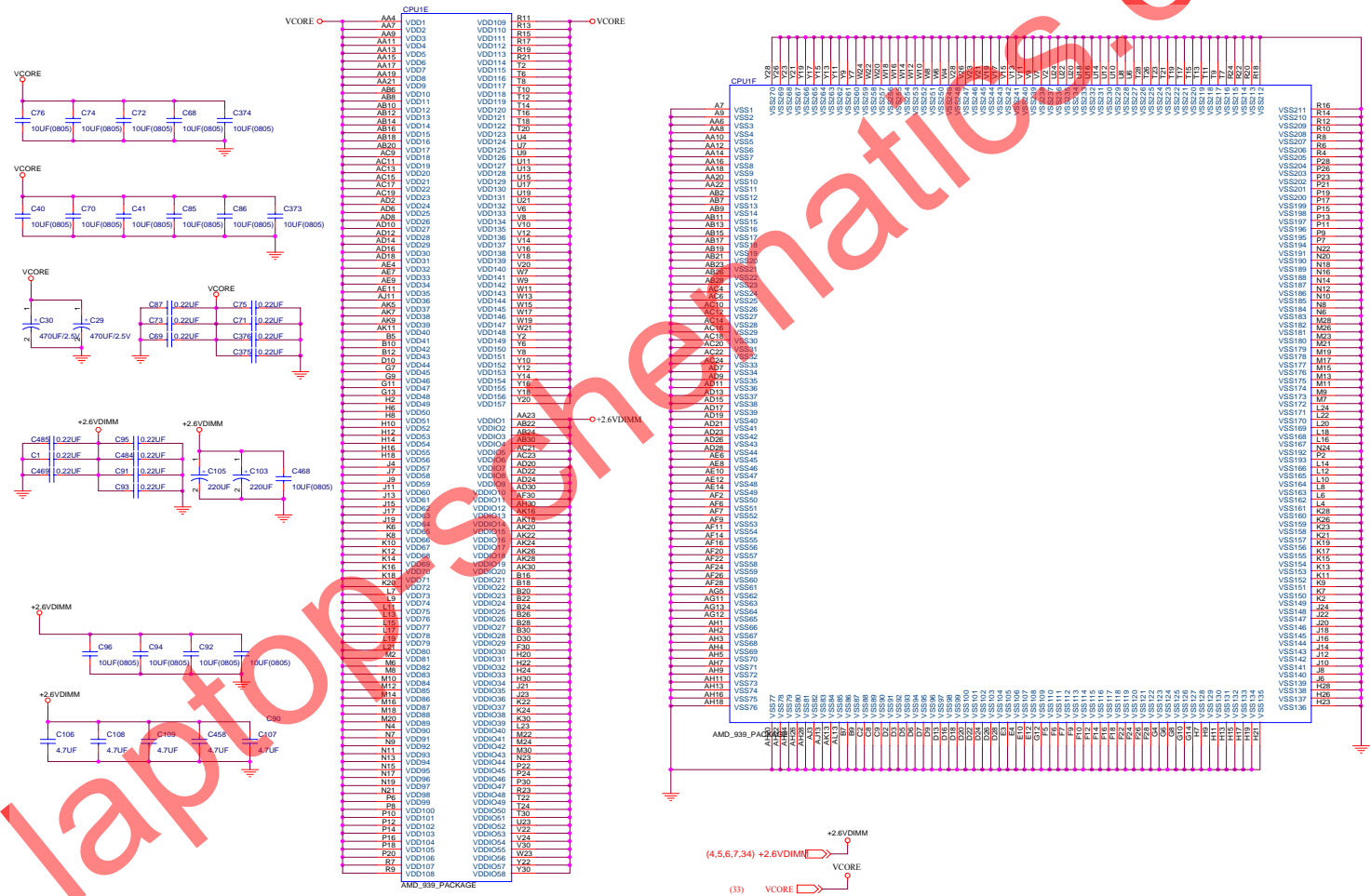
LAYOUT: Place a cap every 1 inch on VTT trace between Clawhammer and DDR.



Sheet 6 of 40  
DDR  
TERMINATION

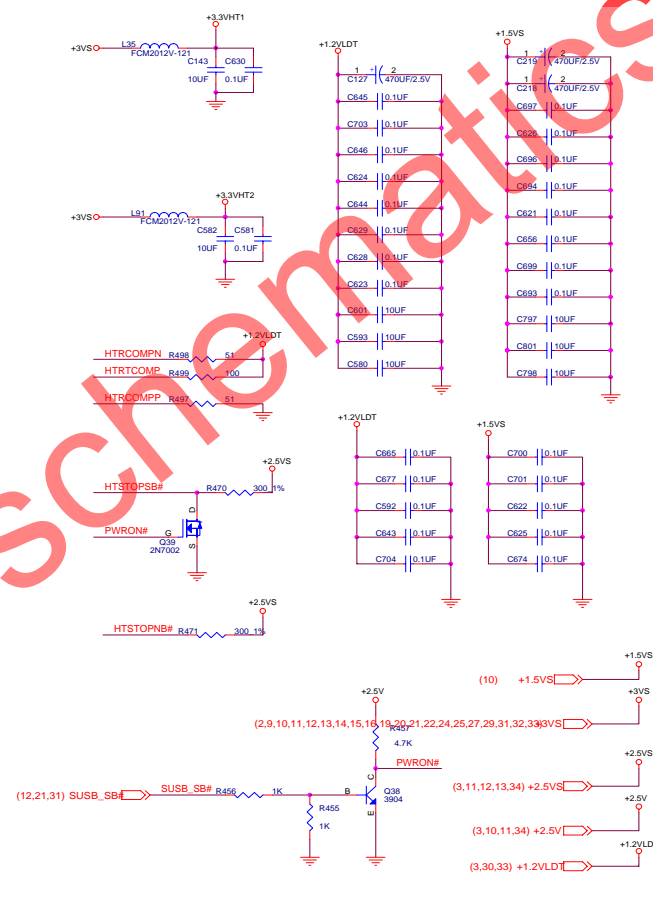
# CPU-3 POWER/ GND

Sheet 7 of 40  
CPU-3 POWER/  
GND





NB K8T890-1 HT INTERFACE



Sheet 8 of 40 NB K8T890-1 HT INTERFACE

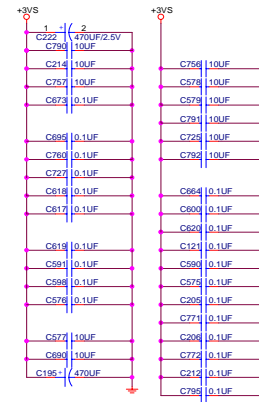
www.laptime.com



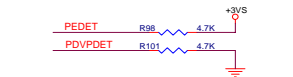
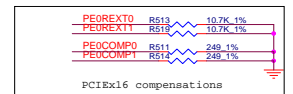
# NB K8T890-2 PCI-E INTERFACE

Sheet 9 of 40  
NB K8T890-2 PCI-E  
INTERFACE

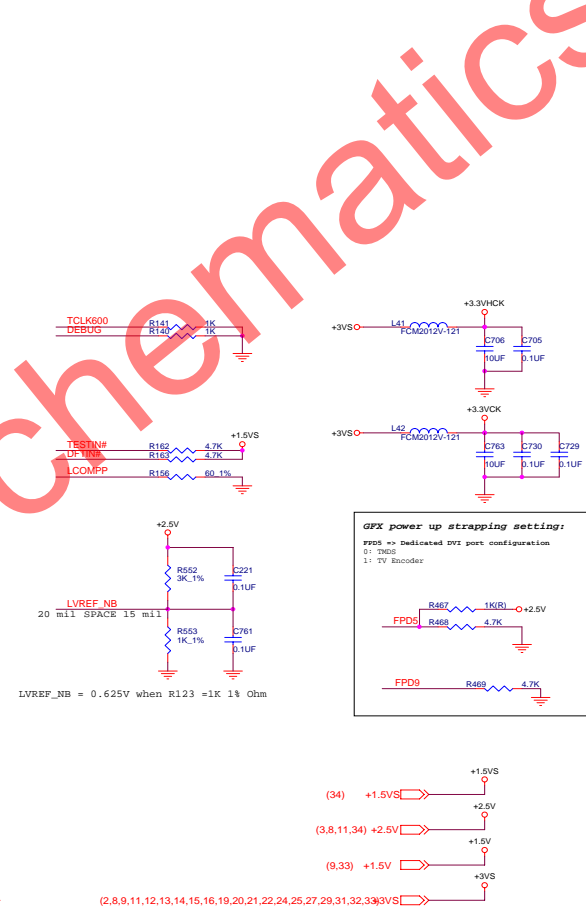
(14) PCIE\_RXP[0..15] <-- PCIE\_RXP[0..15]  
(14) PCIE\_RXN[0..15] <-- PCIE\_RXN[0..15]  
PCIE\_TXP[0..15] <-- PCIE\_TXP[0..15](14)  
PCIE\_TXN[0..15] <-- PCIE\_TXN[0..15](14)



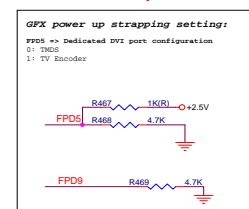
**Note:**  
K8T890 support 4 Xi Lane or 1 X4 Lane PCI Express.



# NB K8T890-3 VLINK & VGA

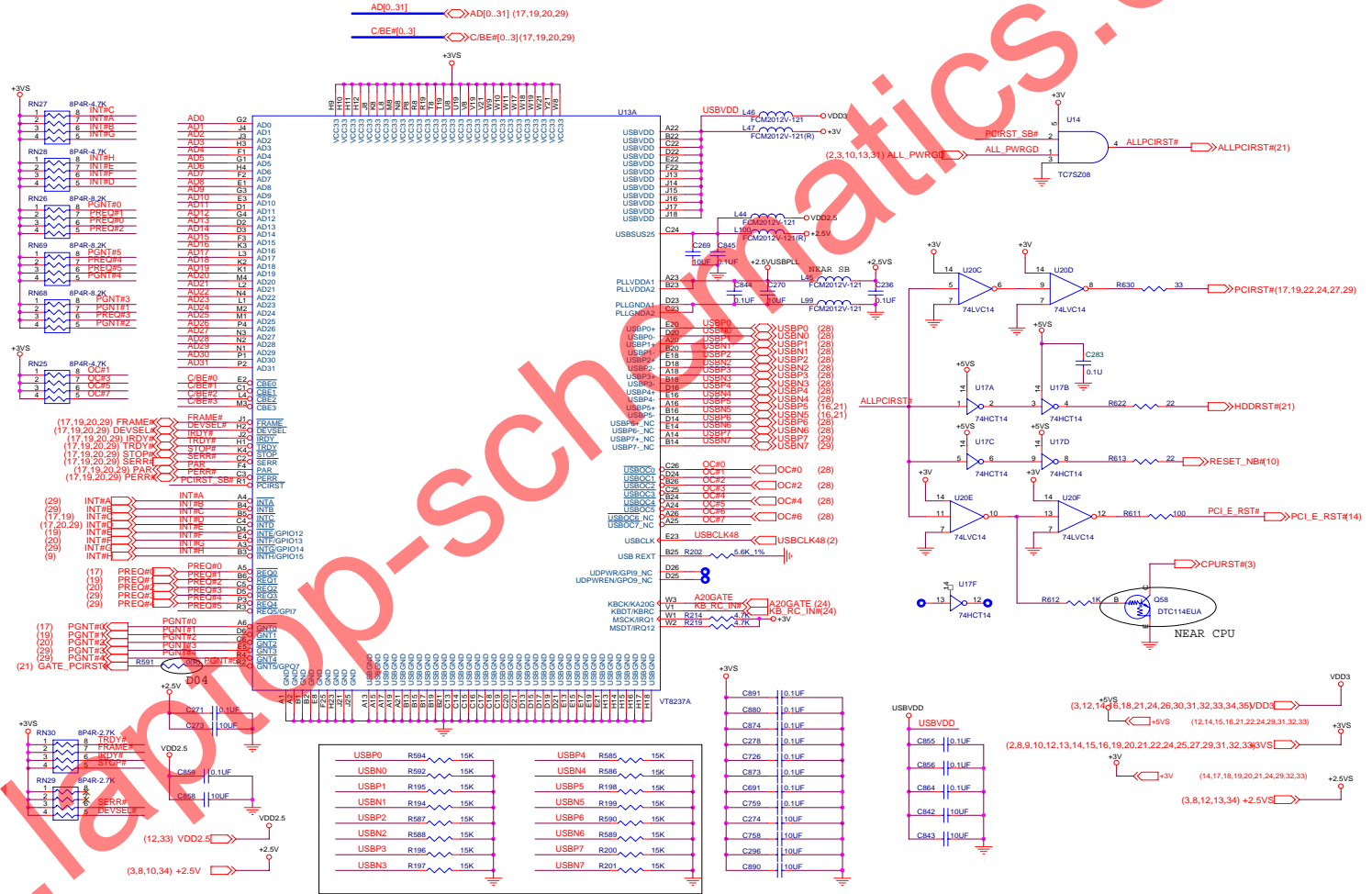


Sheet 10 of 40  
NB K8T890-3  
VLINK & VGA

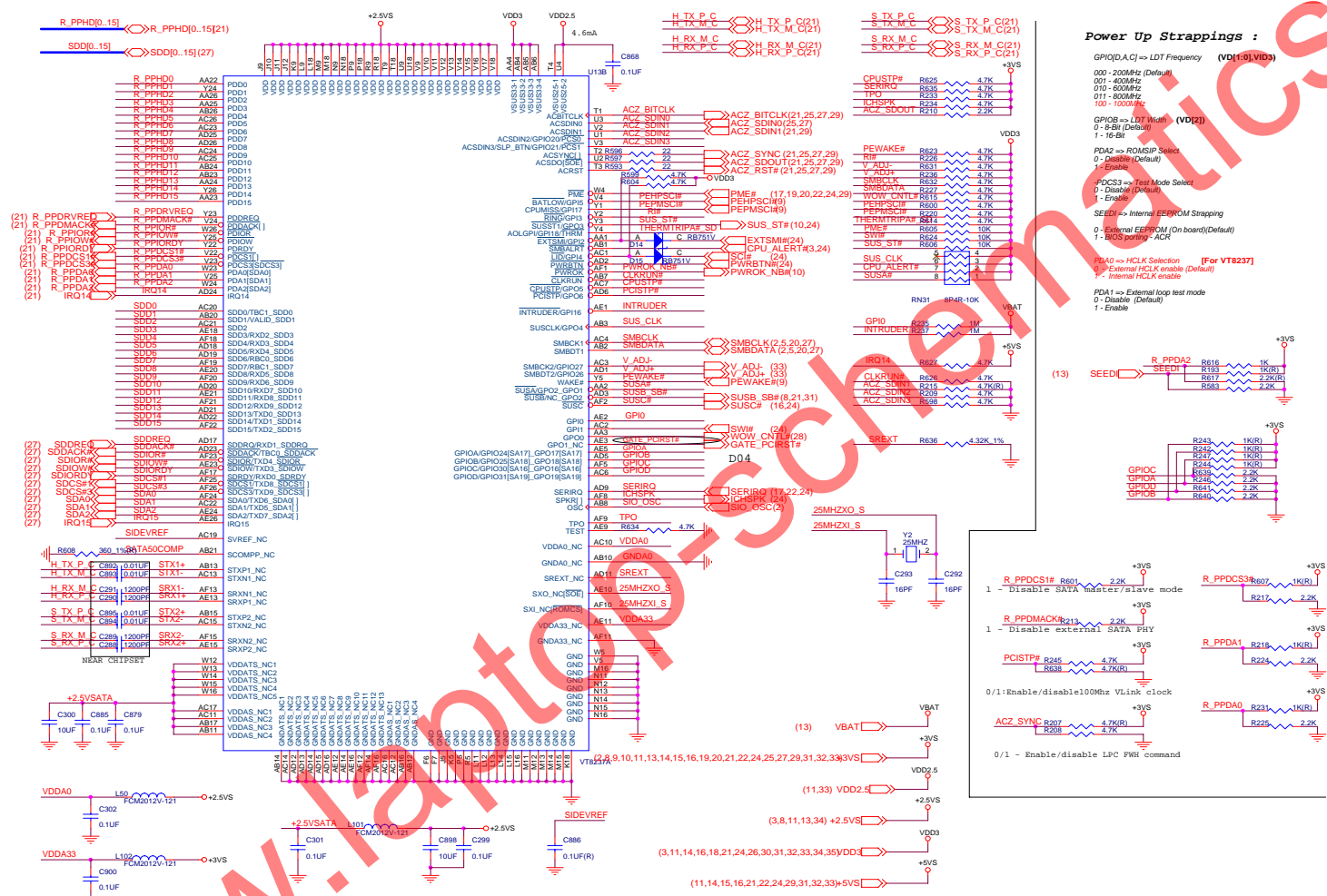


# SB VT8237A-1PCI/ USB

Sheet 11 of 40  
SB VT8237A-1PCI/  
USB



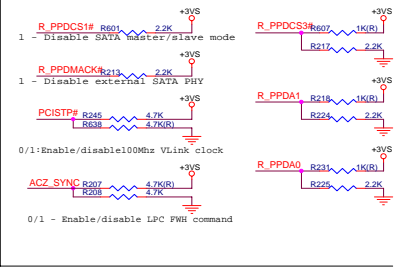
# SB VT8237A-2 IDE, ISA & SATA



**Power Up Strappings :**

- GPIO[A,C] => LDT Frequency (VD1[0],VD3)
  - 001 - 200MHz (Default)
  - 001 - 400MHz
  - 010 - 600MHz
  - 011 - 800MHz
  - 100 - 1000MHz
- GPIOB => LDT Width (VD2)
  - 0 - 5-Bit (Default)
  - 1 - 16-Bit
- PD42 => ROAISIP Select
  - 0 - Disable (Default)
  - 1 - Enable
- PDCS3 => Test Mode Select
  - 0 - Disable (Default)
  - 1 - Enable
- SEEDI => Internal EEPROM Strapping
  - 0 - External EEPROM (On board, Default)
  - 1 - BIOS parsing - ACR
- PD40 => HCLK Selection [For VT8237]
  - 0 - External HCLK enable (Default)
  - 1 - Internal HCLK enable
- PD41 => External loop test mode
  - 0 - Disable (Default)
  - 1 - Enable

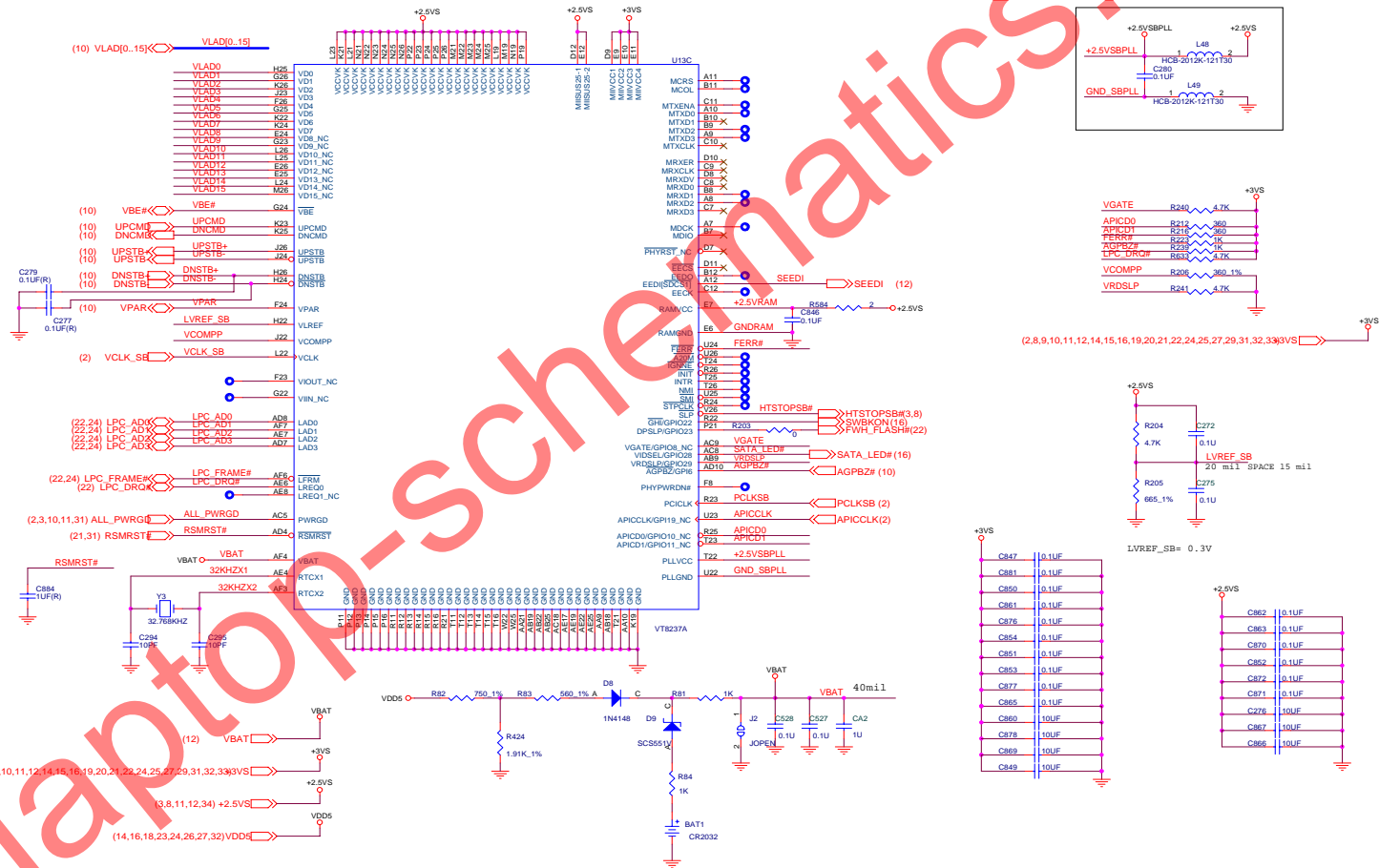
Sheet 12 of 40  
SB VT8237A-2 IDE,  
ISA & SATA



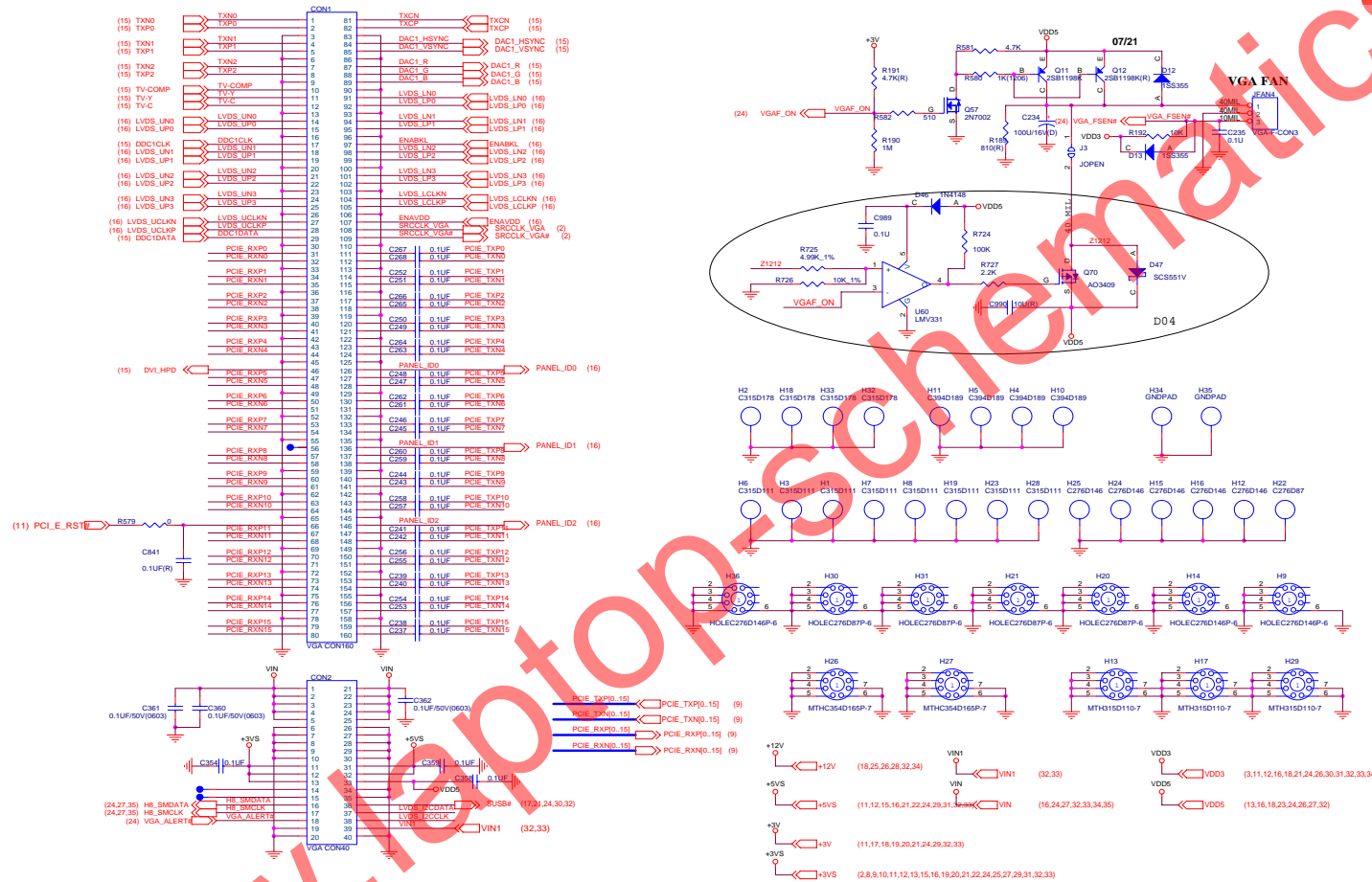
- R\_PPDCS3#R607 2.2K
- 1 - Disable SATA master/slave mode
- R\_PPDMACK#R213 2.2K
- 1 - Disable external SATA PHY
- PCISTP# R245 4.7K
- GND R638 4.7K
- 0/1: Enable/disable 100MHz VLink clock
- ACZ\_SYNC#R208 4.7K
- GND R225 4.7K
- 0/1 - Enable/disable LPC FW command

# SB VT8237A-3 LPC, LAN, VLINK

Sheet 13 of 40  
SB VT8237A-3 LPC,  
LAN, VLINK



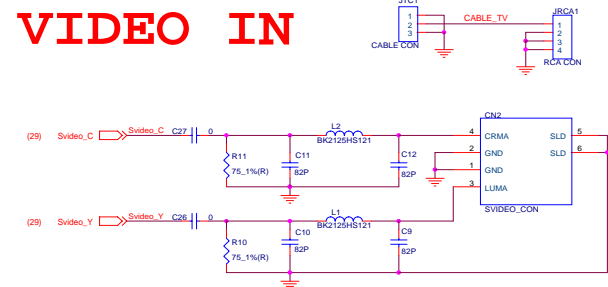
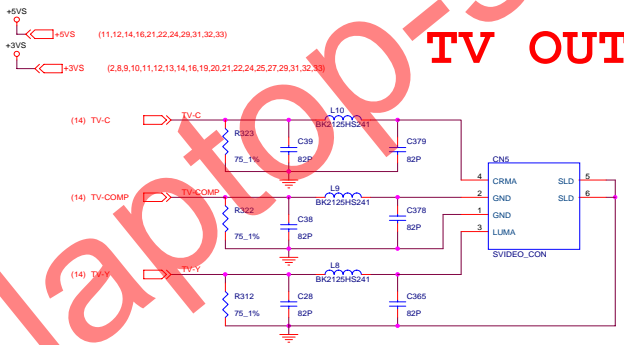
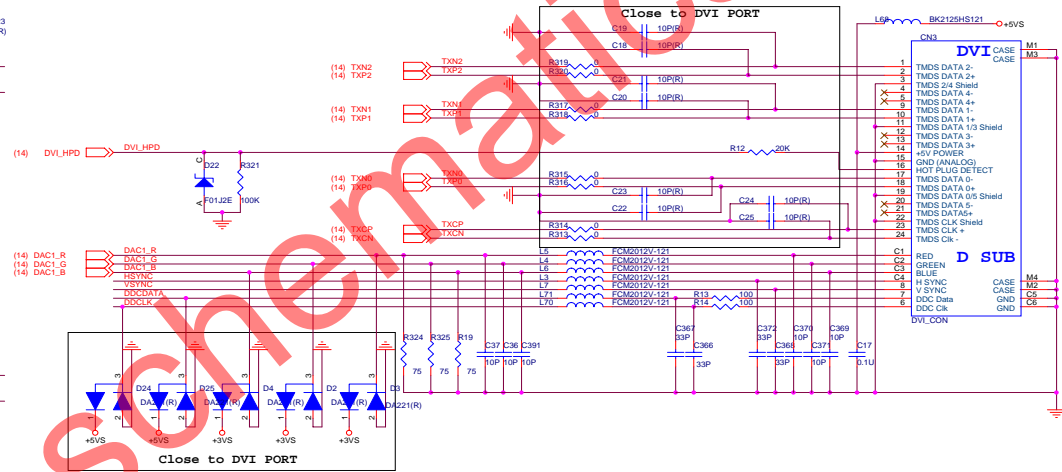
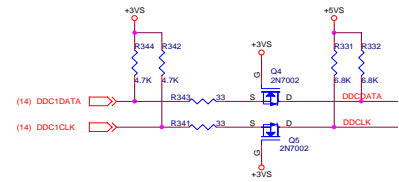
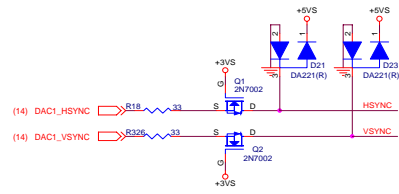
# VGA DAUGHTER CONNECTOR



Sheet 14 of 40  
VGA DAUGHTER  
CONNECTOR

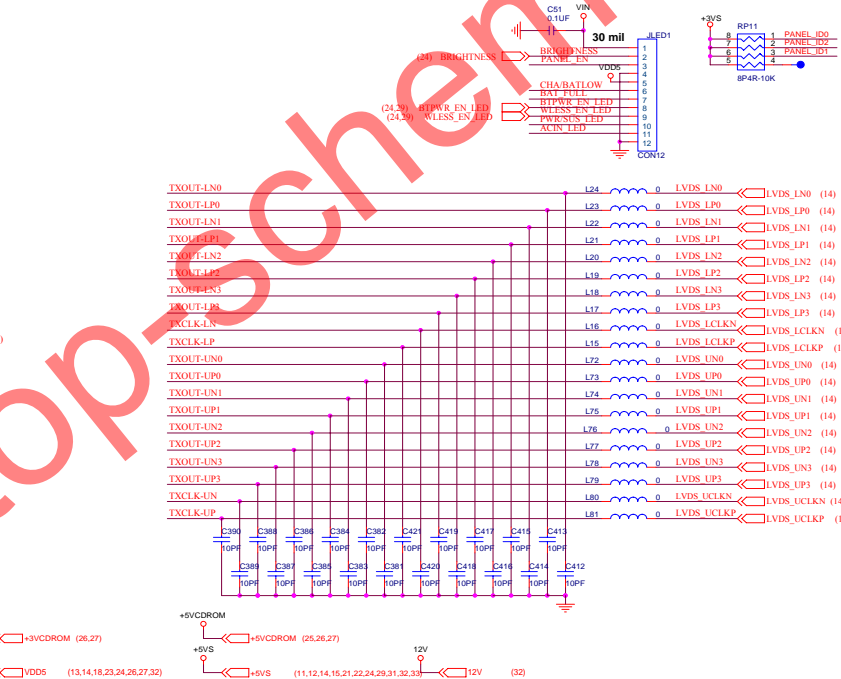
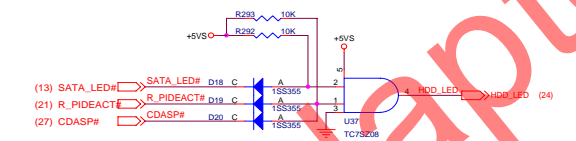
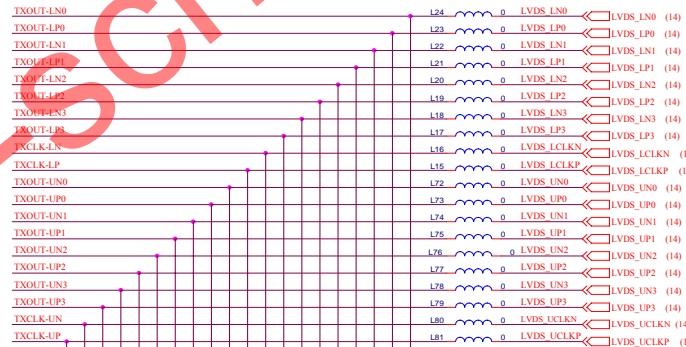
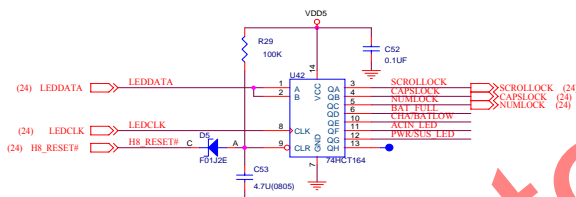
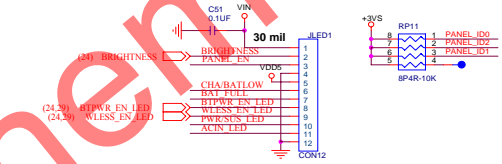
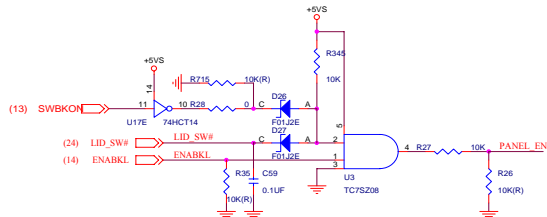
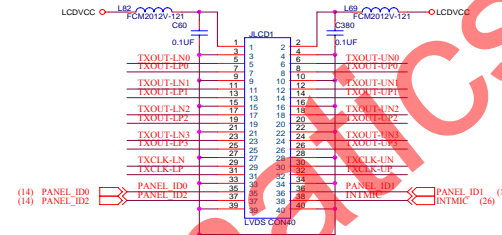
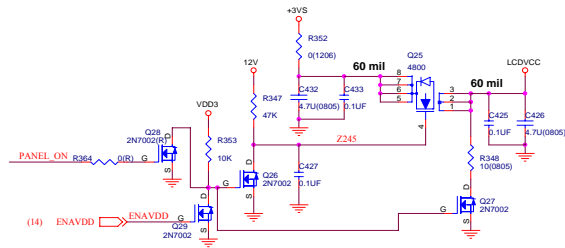
# DVI/ TV OUT/ VIDEO IN CON

Sheet 15 of 40  
DVI/ TV OUT/  
VIDEO IN CON





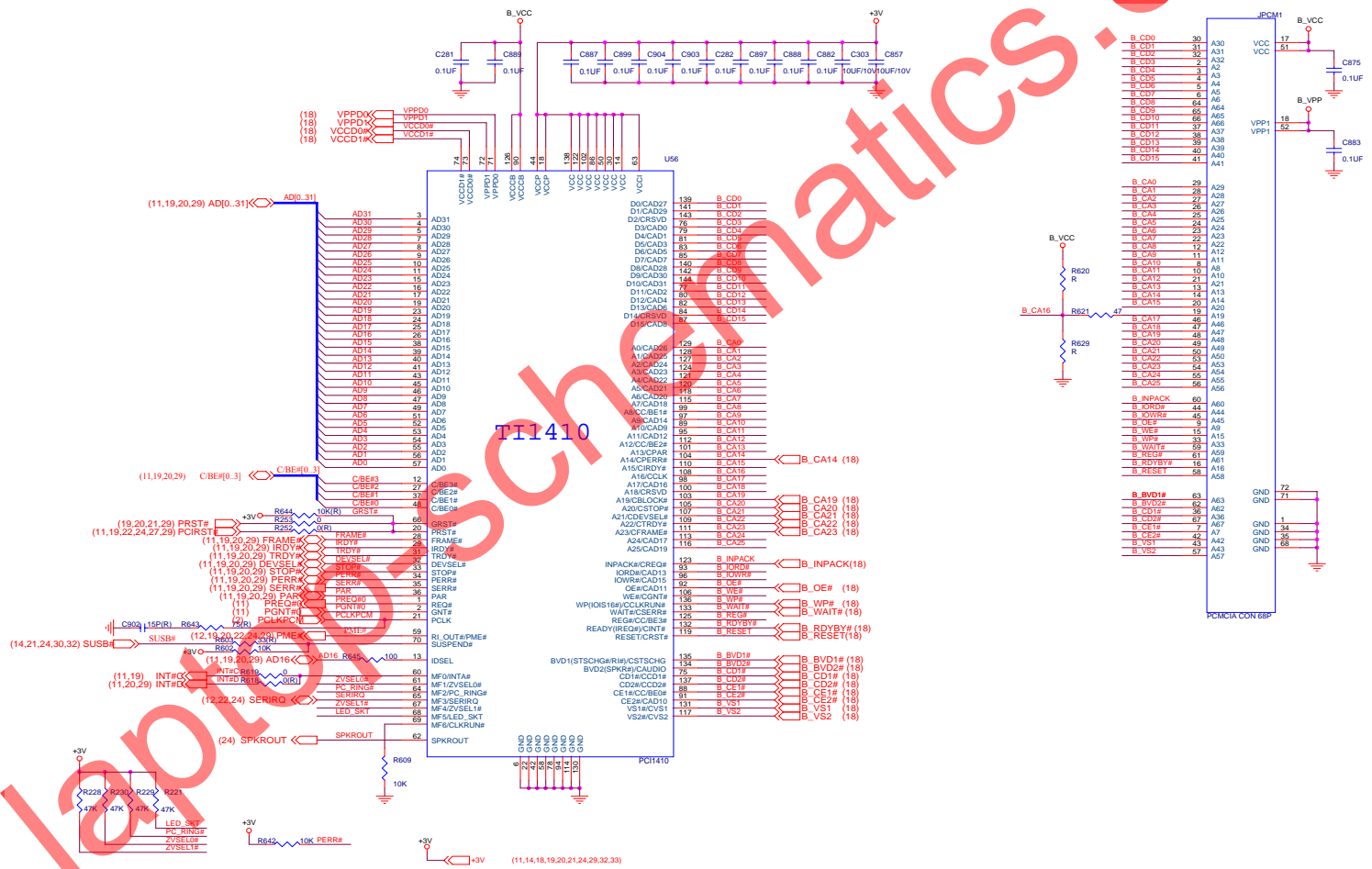
# PANEL CON/ LED INDICATOR



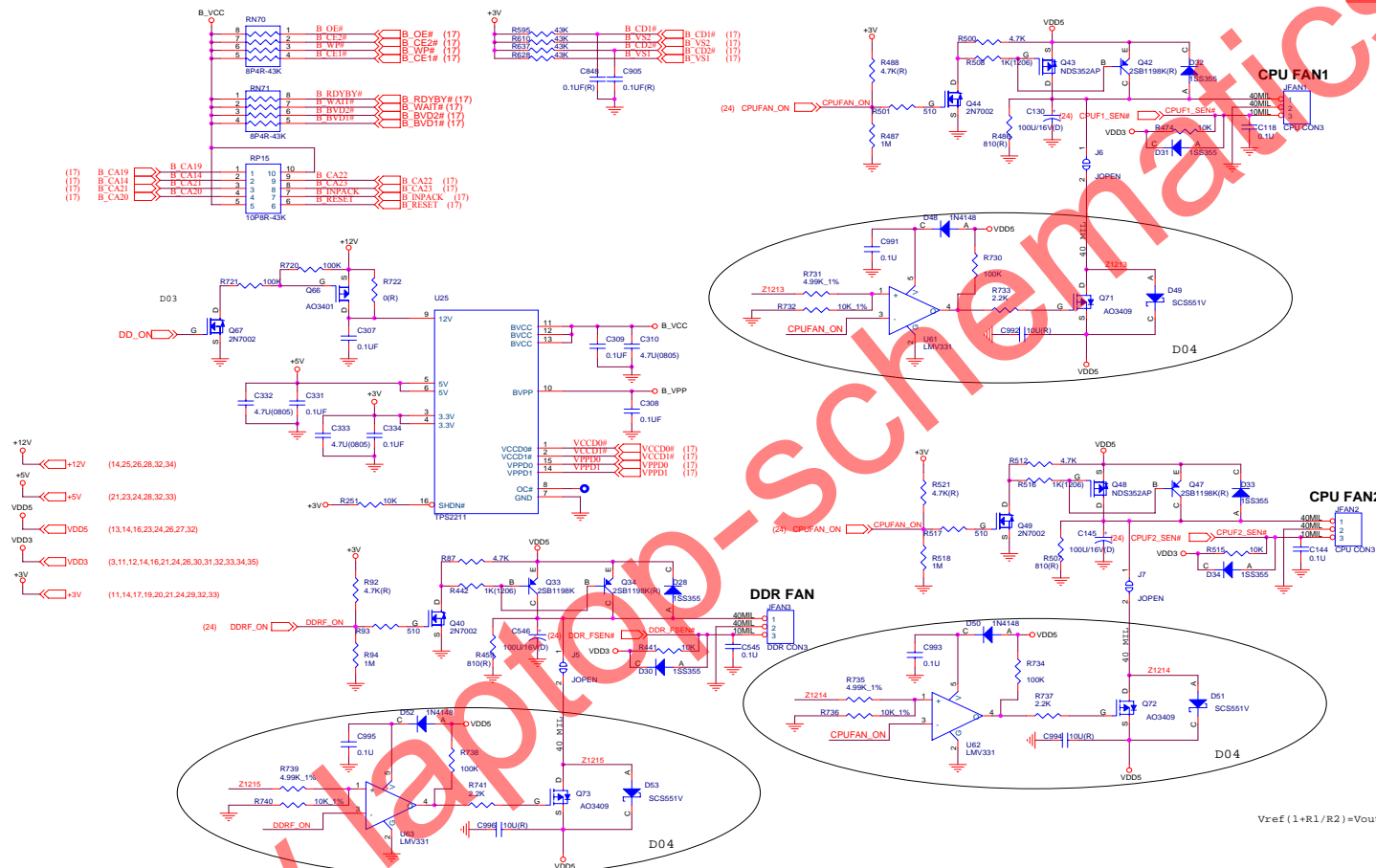
Sheet 16 of 40  
PANEL CON/ LED  
INDICATOR

# PCMCIA T11410

Sheet 17 of 40  
PCMCIA T11410



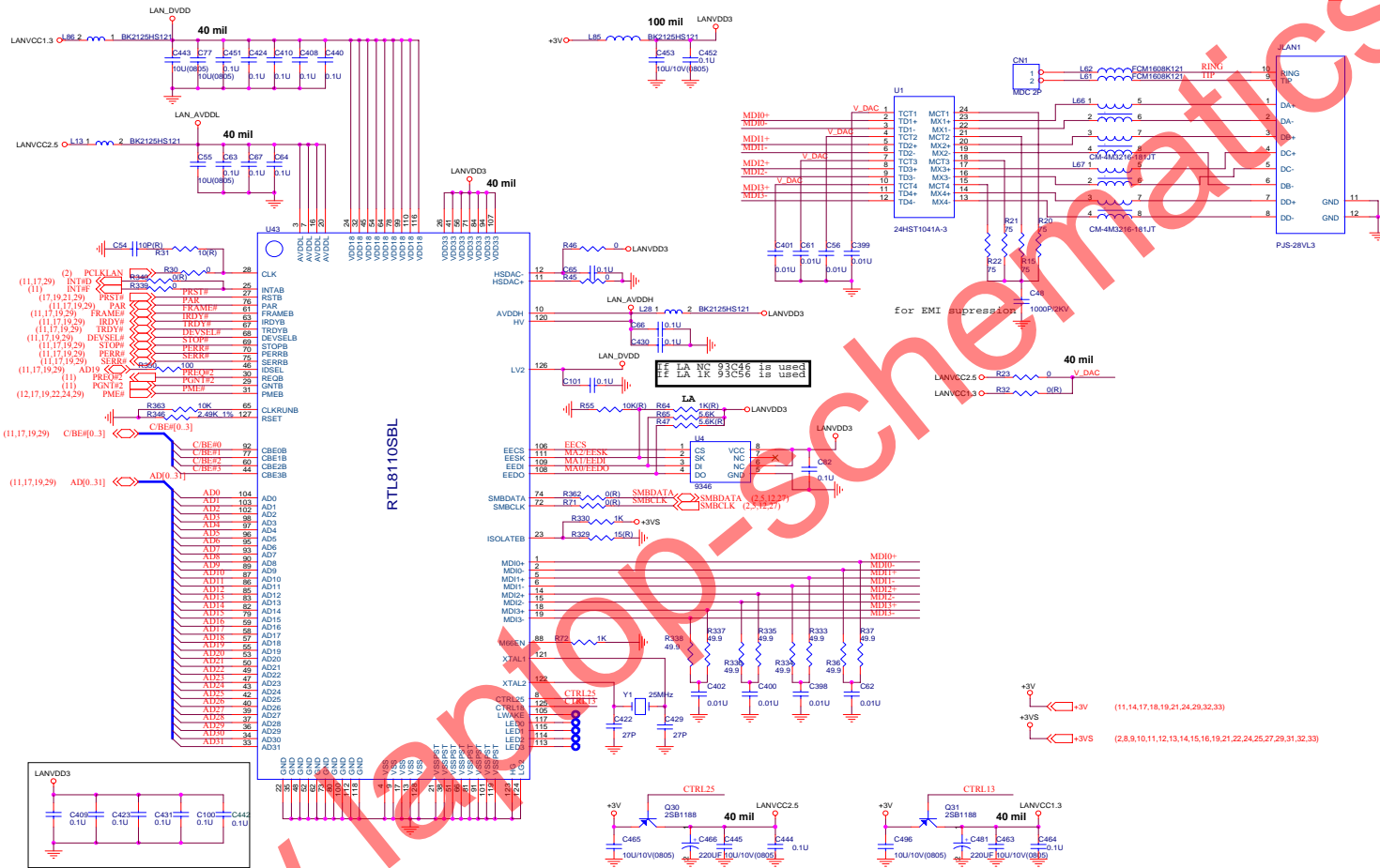
# PCMCIA POWER/ FAN CON



Sheet 18 of 40  
PCMCIA POWER/  
FAN CON



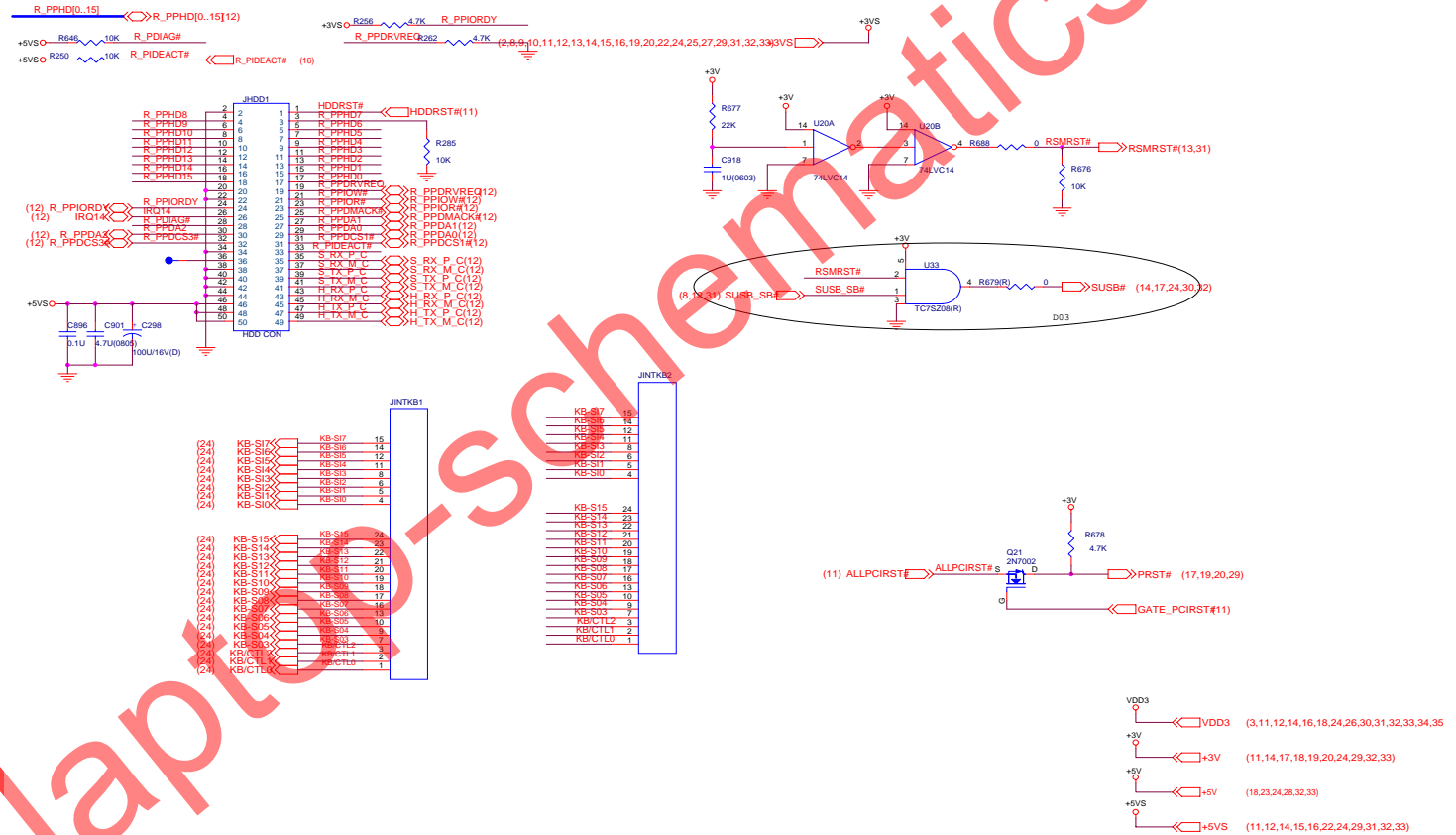
# GLAN RTL8110SBL



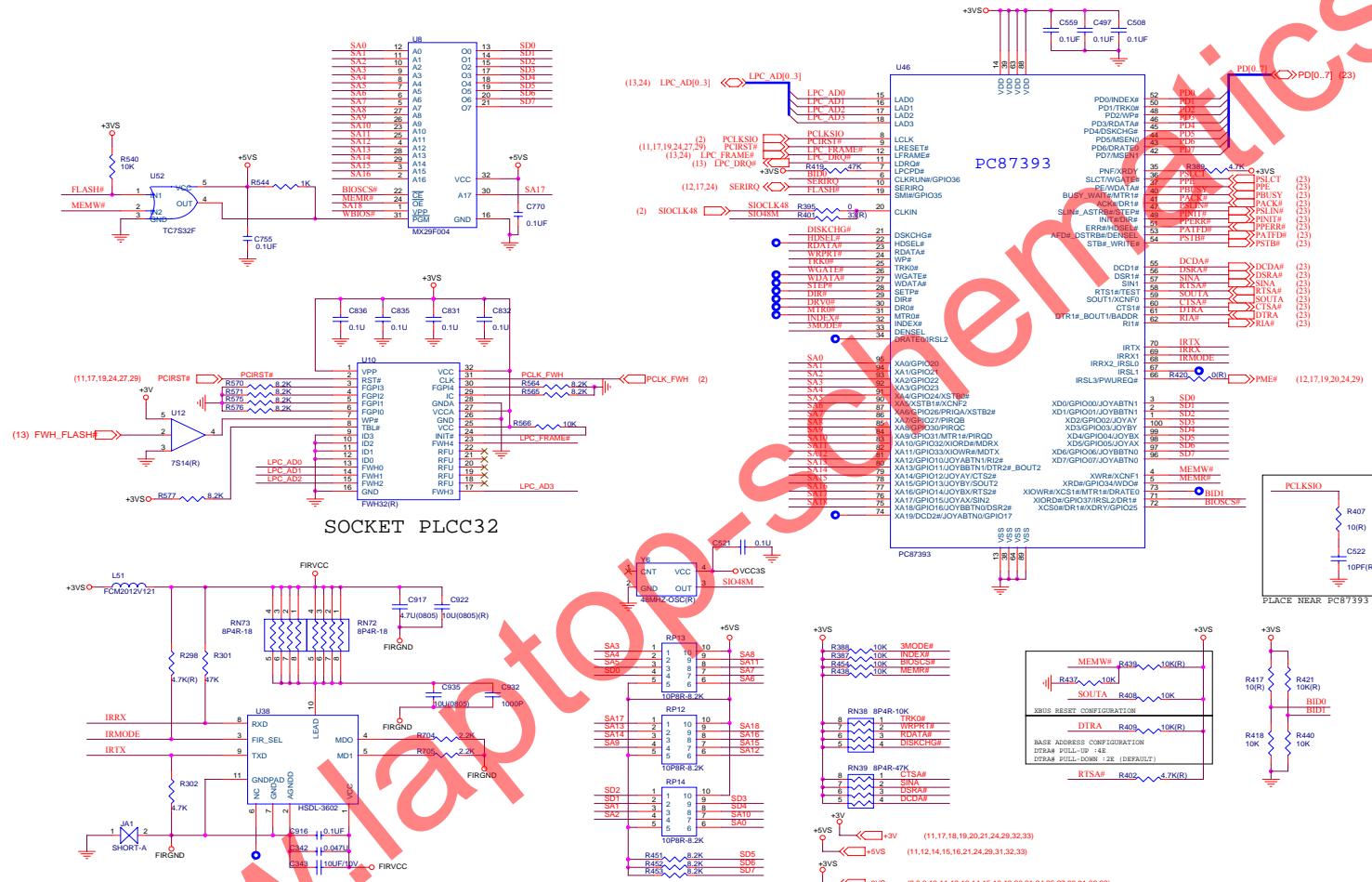
Sheet 20 of 40  
GLAN RTL8110SBL

# HDD CON

Sheet 21 of 40  
HDD CON



# LPC SUPER I/ O NS87393

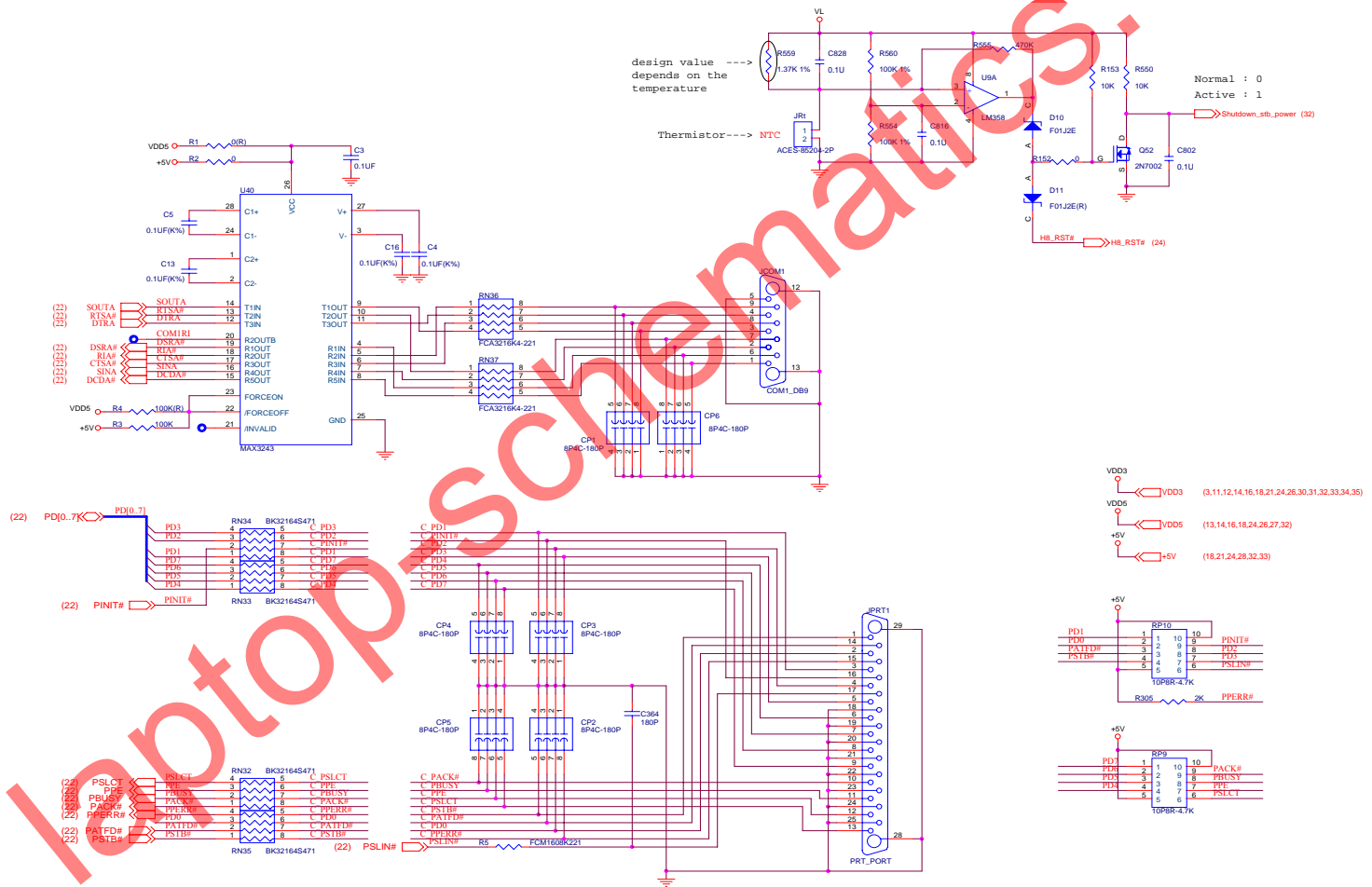


Sheet 22 of 40  
LPC SUPER I/O  
NS87393

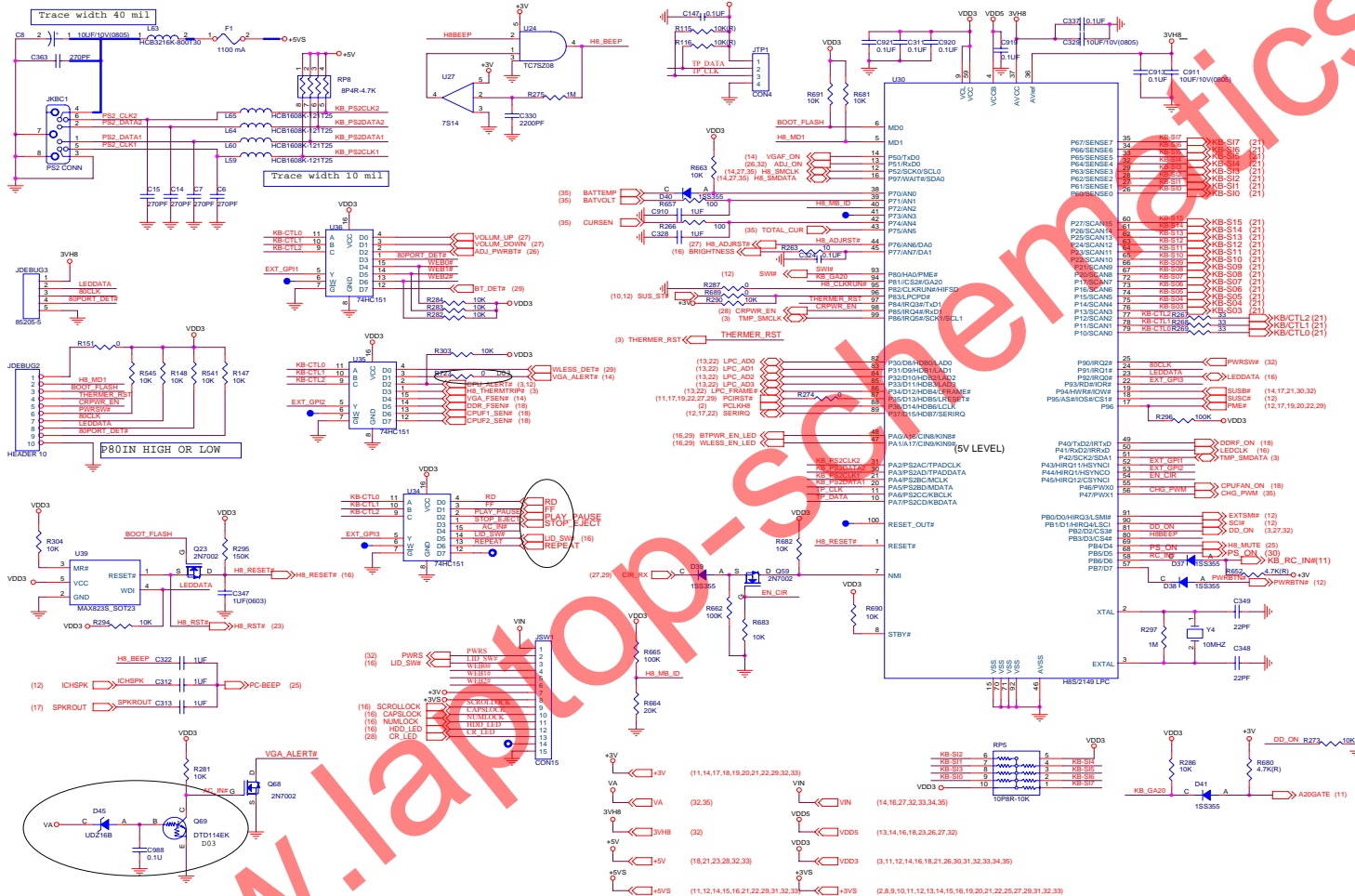


# LPT/ COM PORT CON/ Thermistor

Sheet 23 of 40  
LPT/ COM PORT  
CON/ Thermistor



# LPC H8

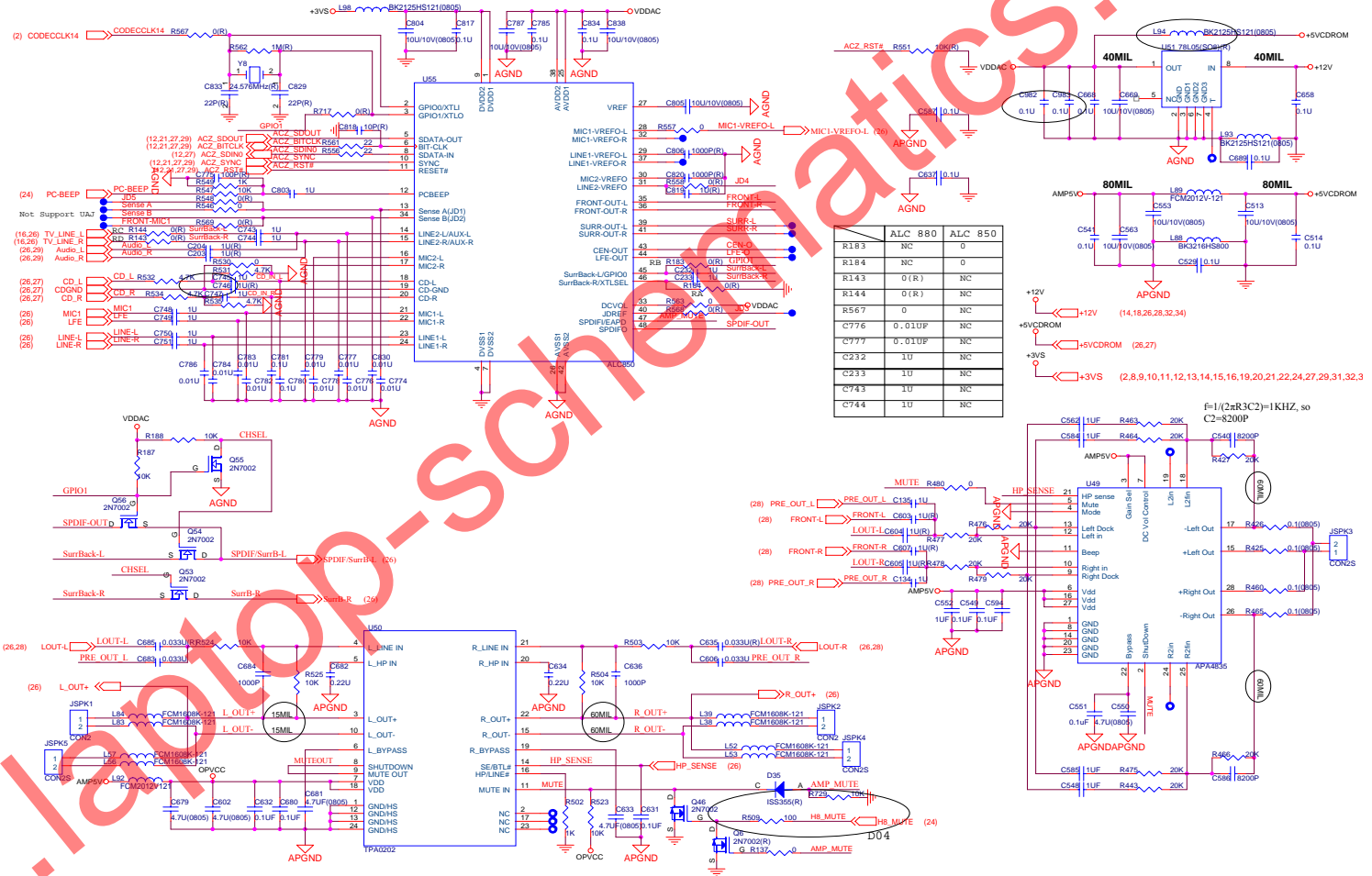


Sheet 24 of 40  
LPC H8

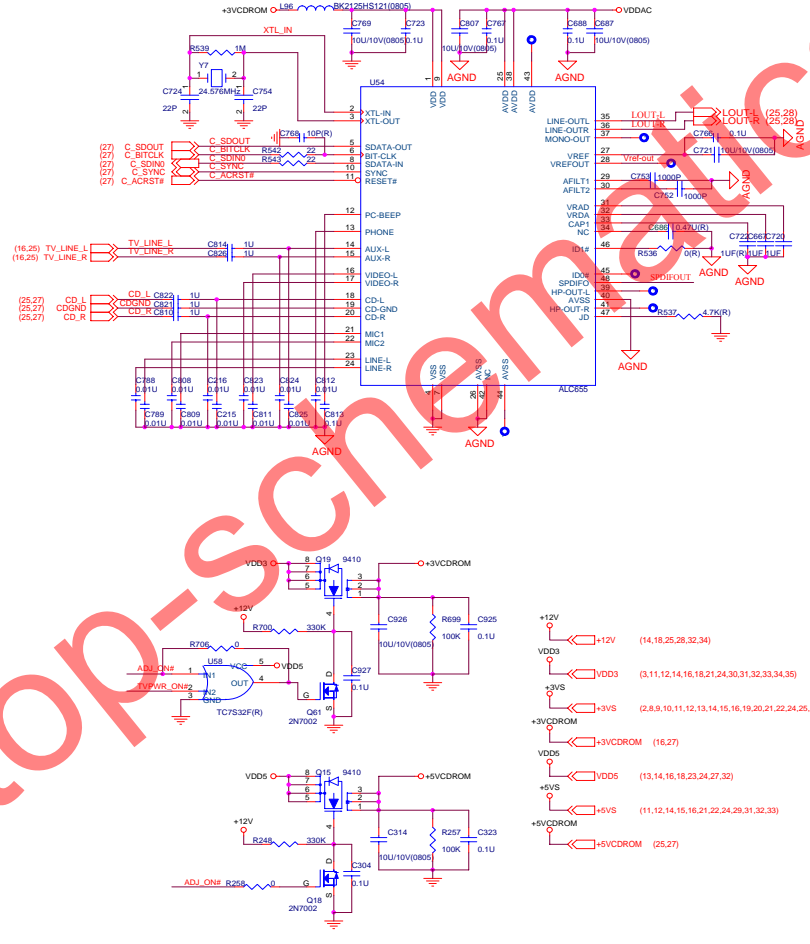
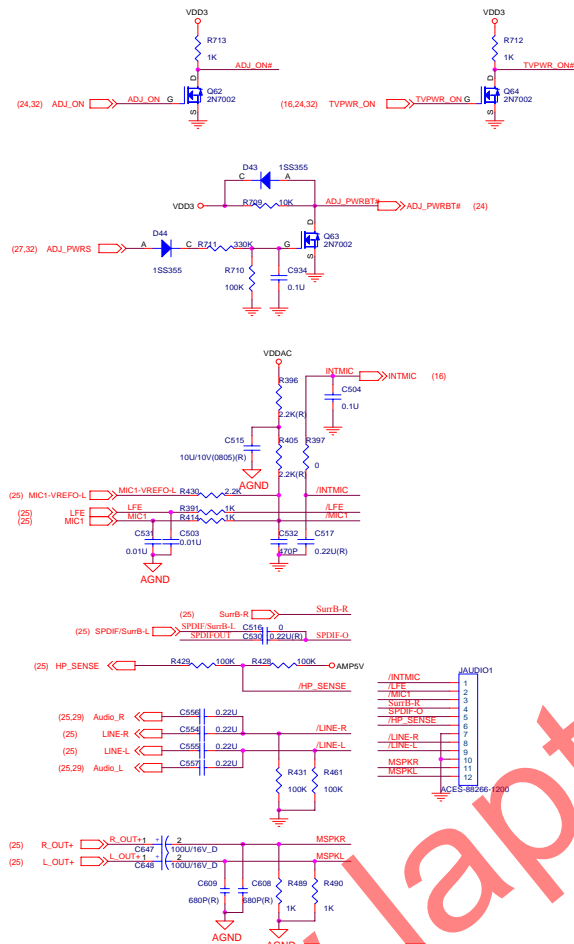
www.laptop-schematics.com

# CODEC ALC850

Sheet 25 of 40  
CODEC ALC850



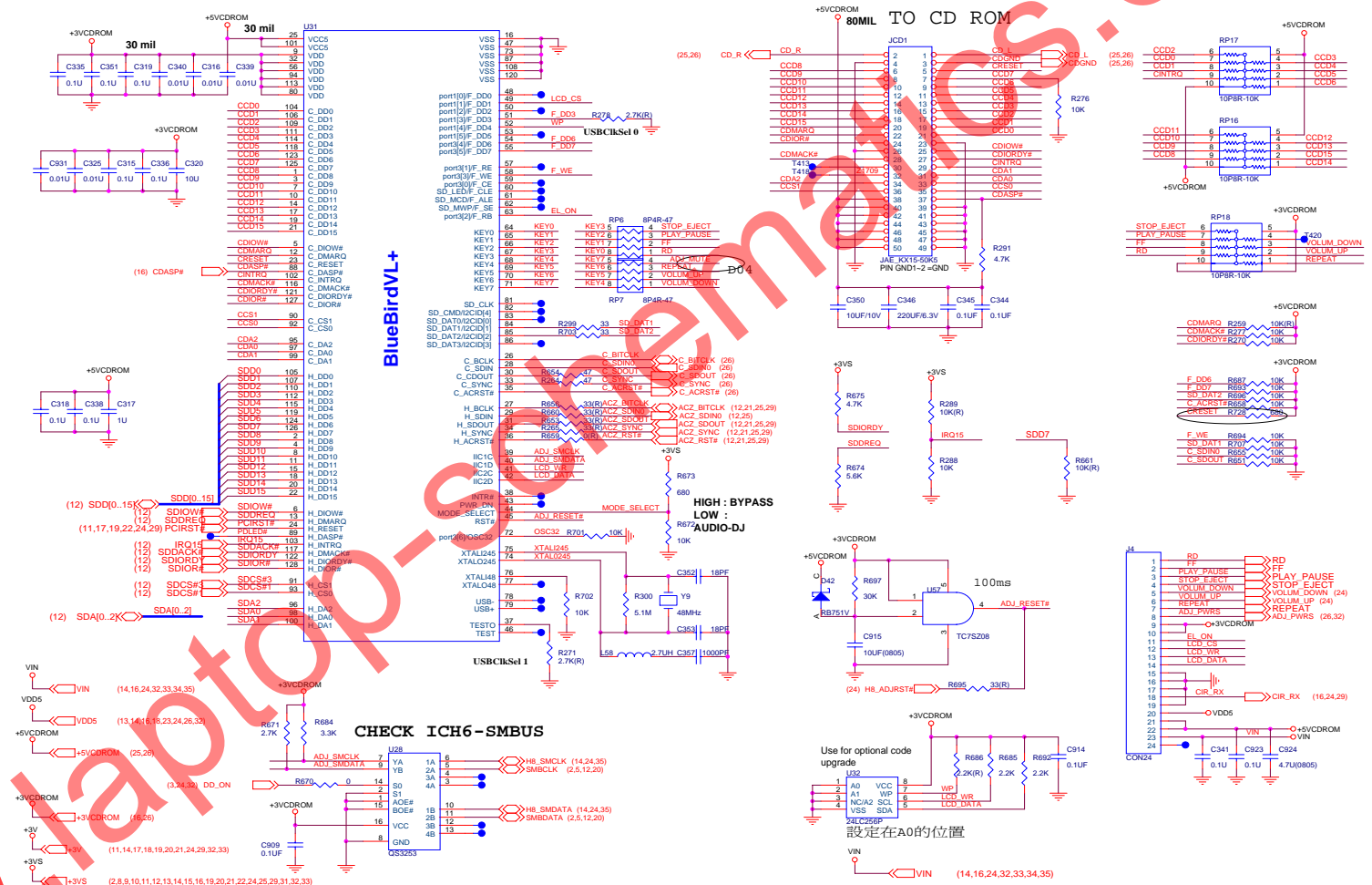
# AUDIO JACK & ADJ POWER



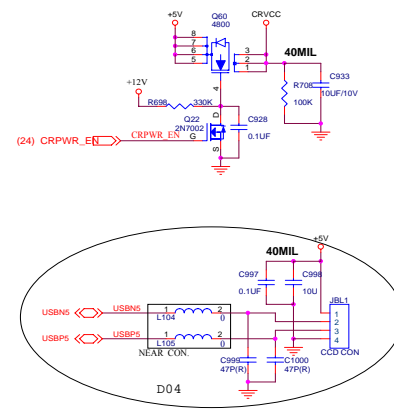
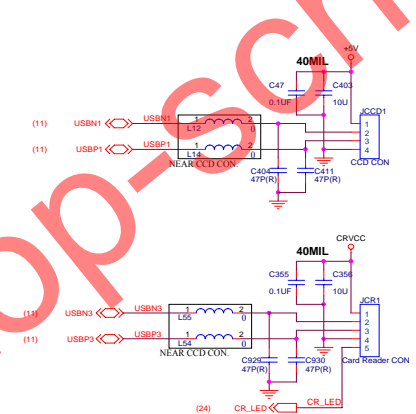
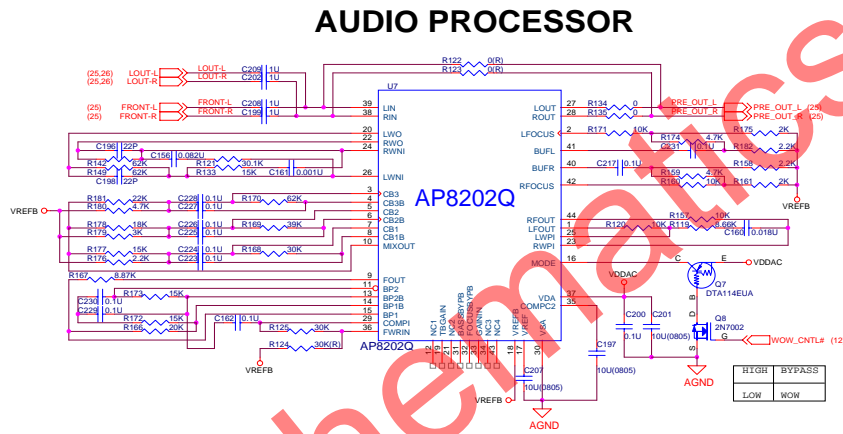
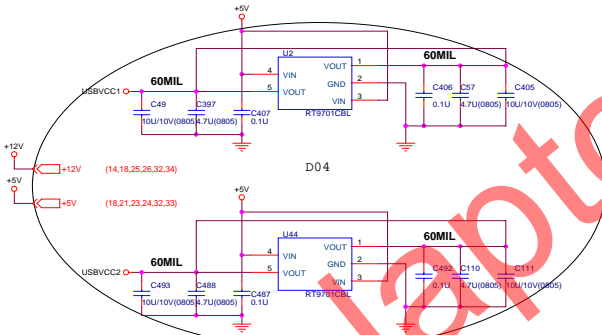
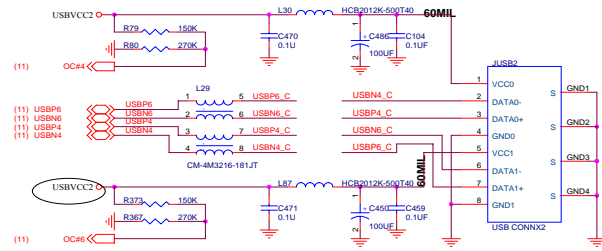
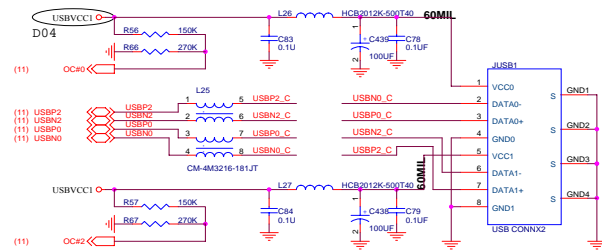
Sheet 26 of 40  
AUDIO JACK &  
ADJ POWER

# AUDIO DJ BBVL + CONTROL

Sheet 27 of 40  
AUDIO DJ BBVL +  
CONTROL



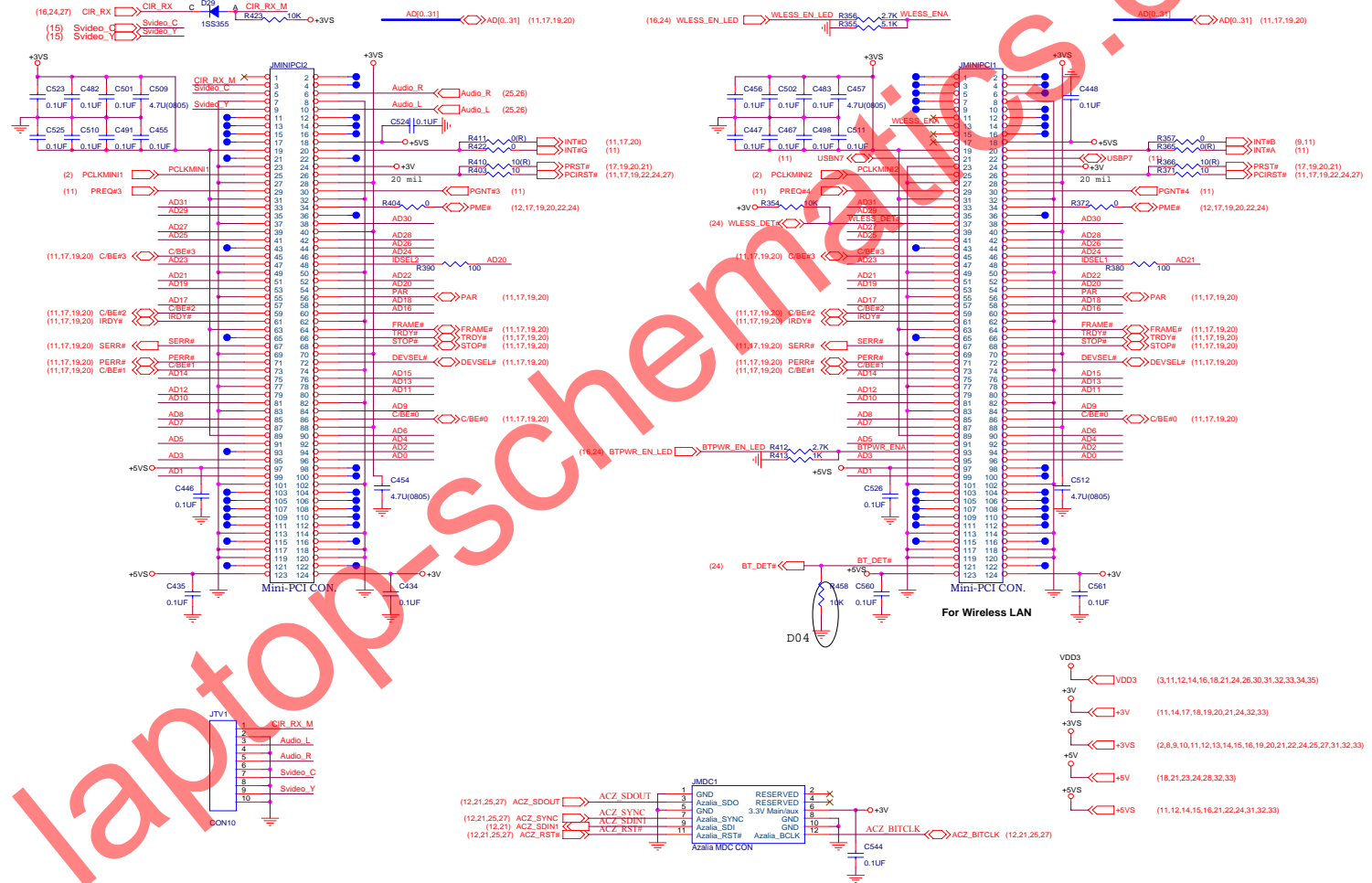
# USB/ CR/ CCD CON/ SRS



Sheet 28 of 40  
USB/ CR/ CCD  
CON/ SRS

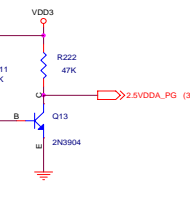
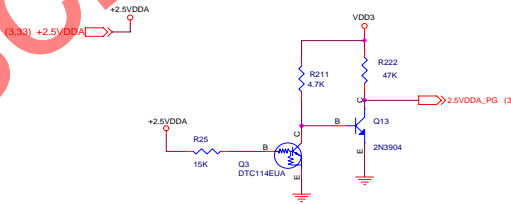
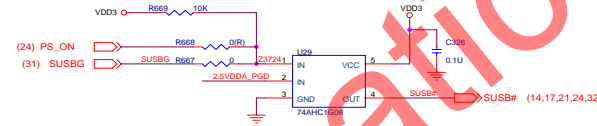
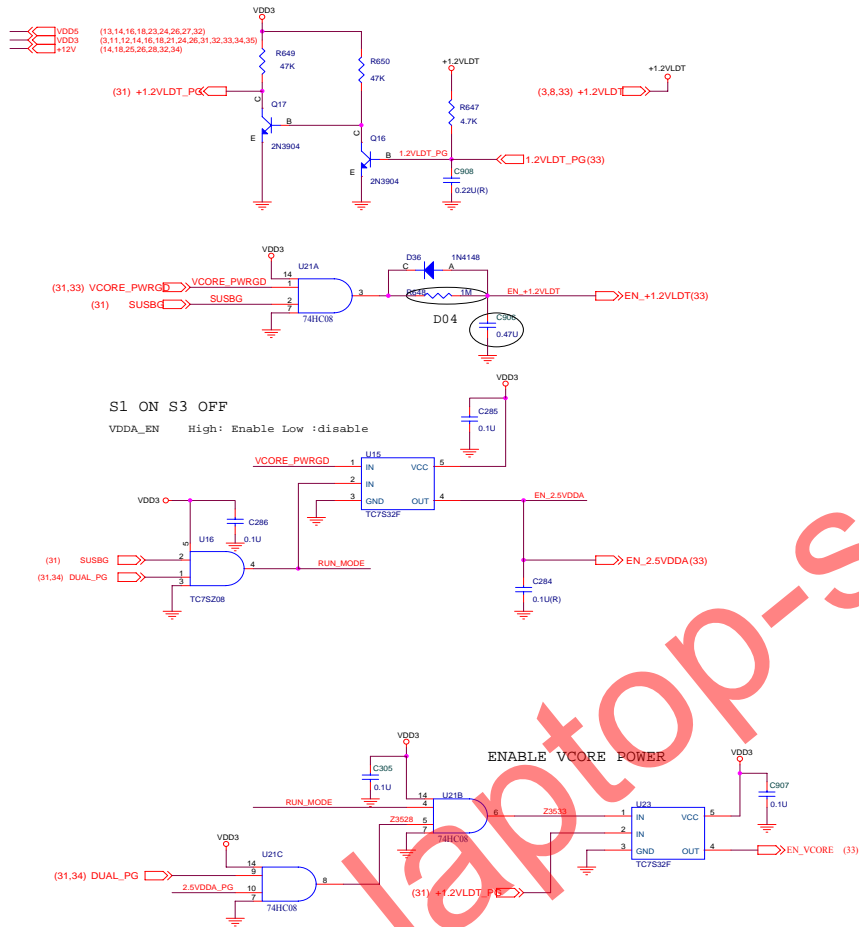
# MINI PCI/ NC/ MDC/ BT CON

Sheet 29 of 40  
MINI PCI/ NC/ MDC/  
BT CON





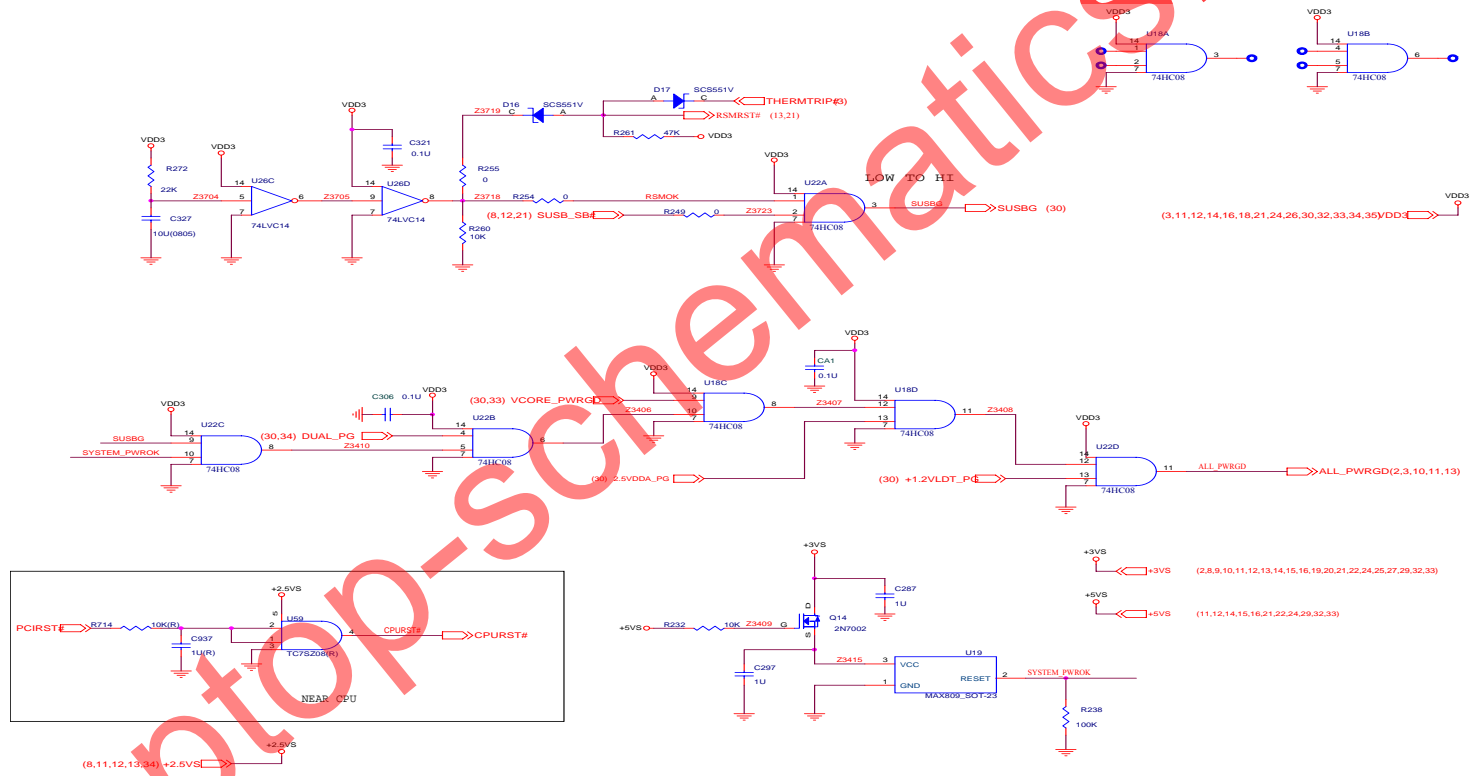
# POWER CONTROLLER 1



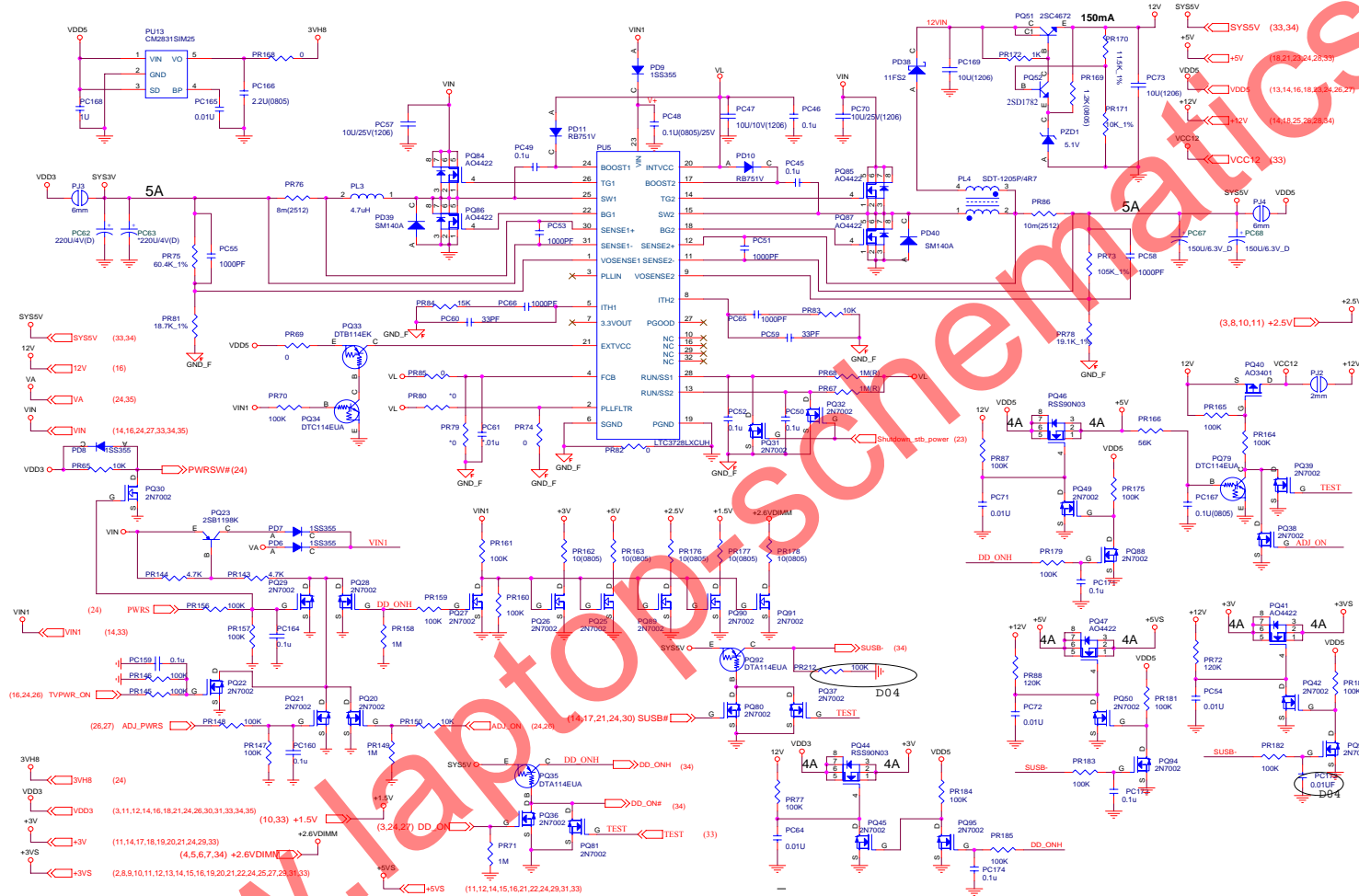
Sheet 30 of 40  
POWER  
CONTROLLER 1

# POWER CONTROLLER 2

Sheet 31 of 40  
POWER  
CONTROLLER 2



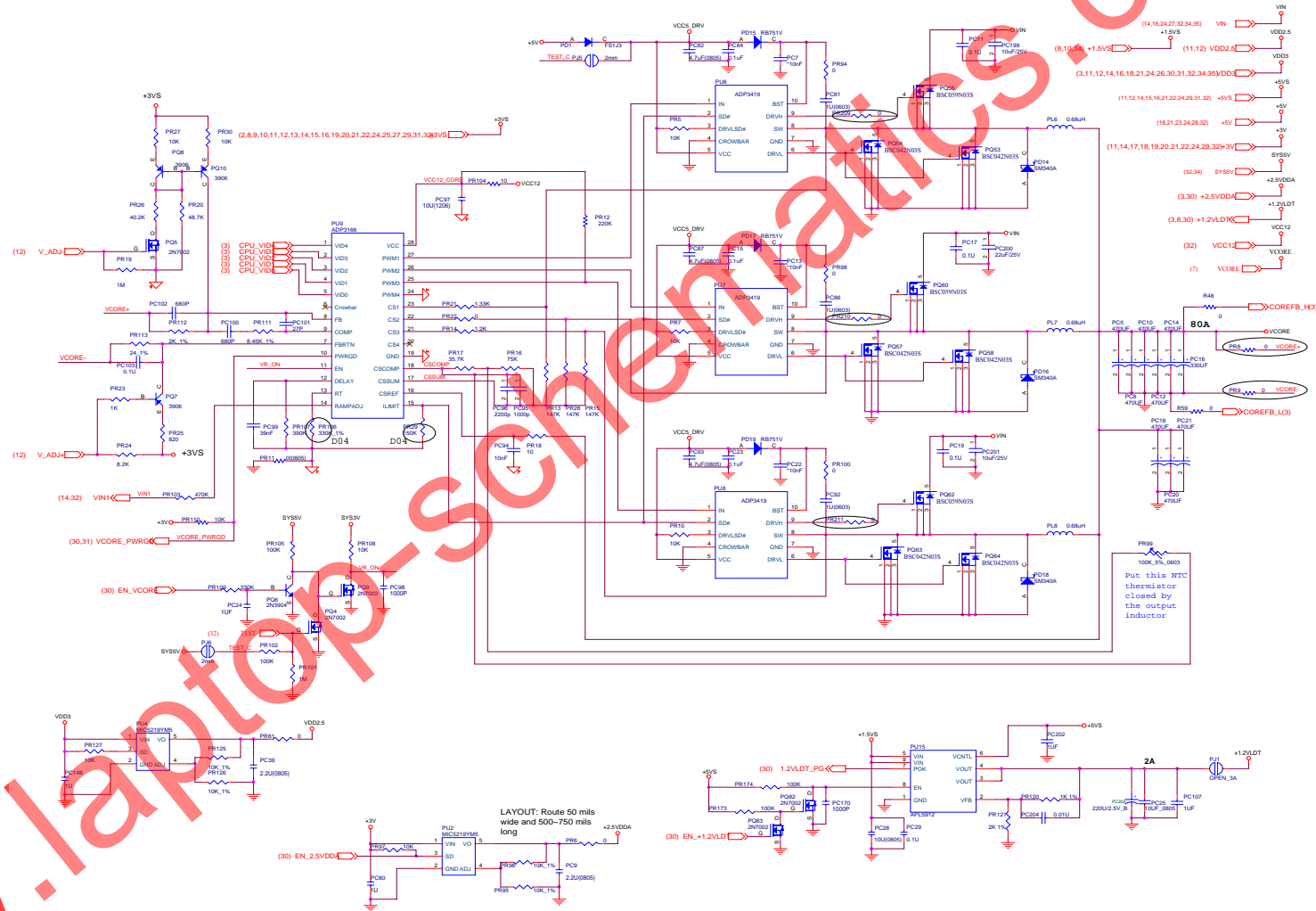
# SYSTEM POWER



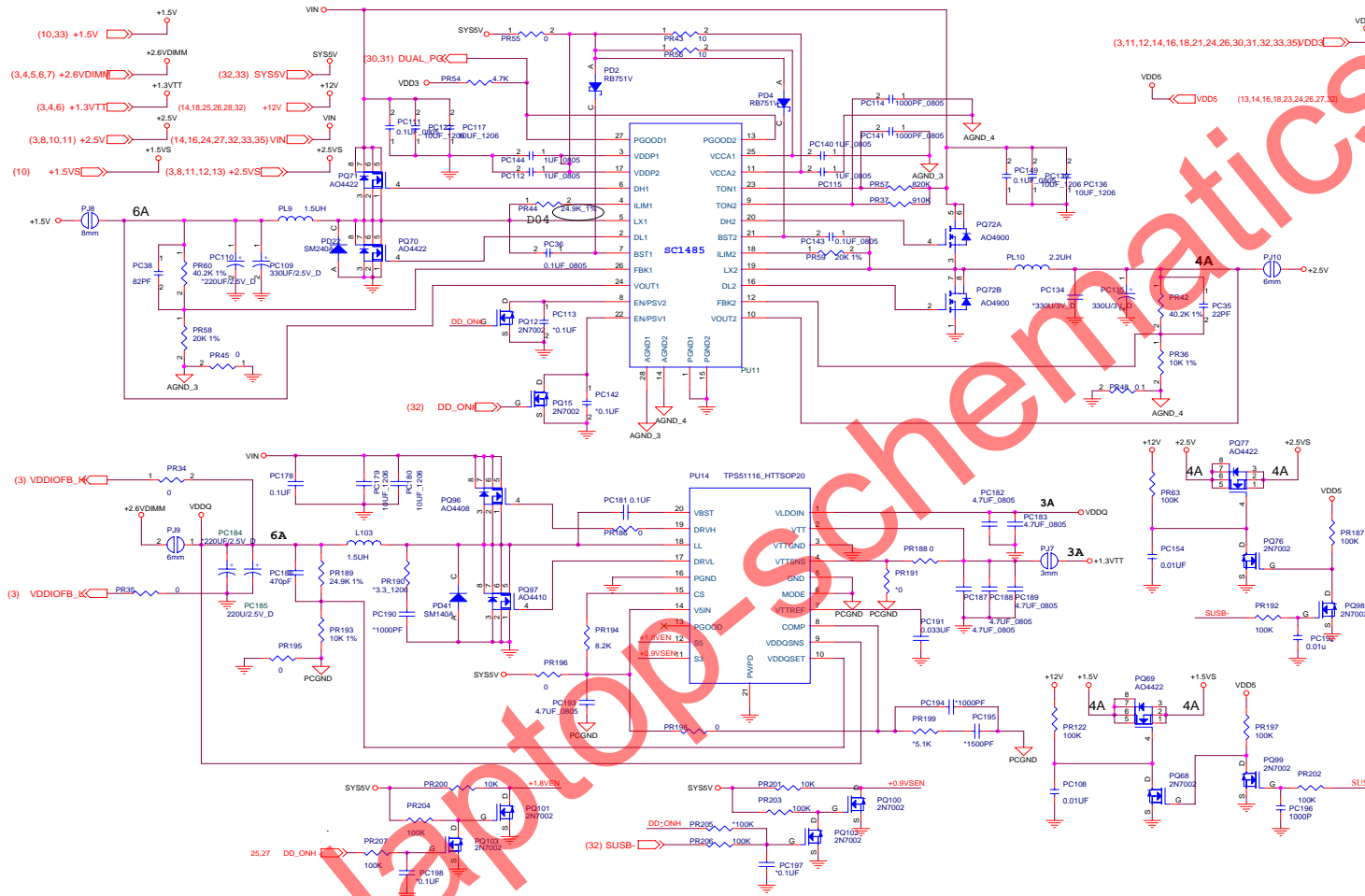
Sheet 32 of 40  
SYSTEM POWER

# VCORE

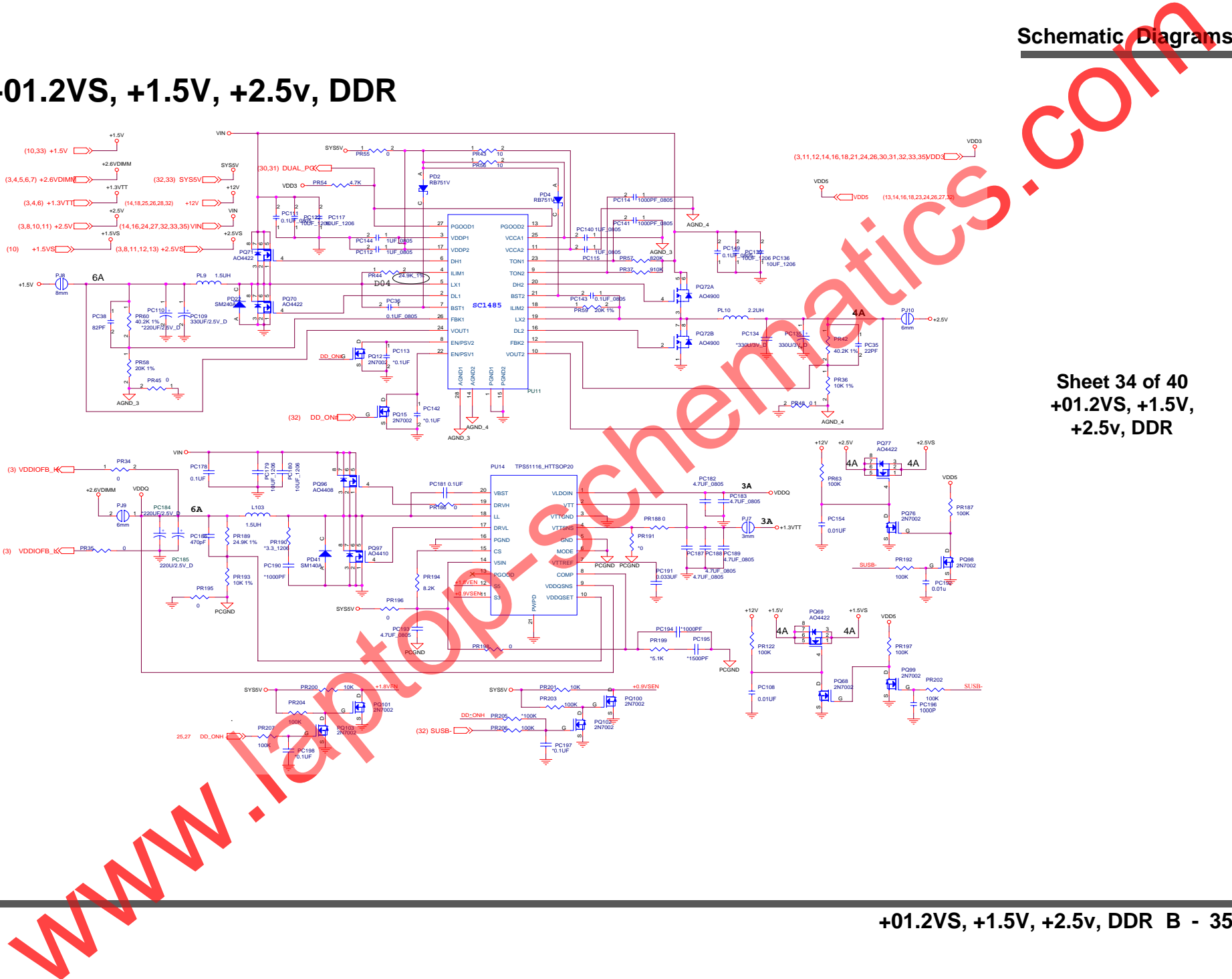
Sheet 33 of 40  
VCORE



+01.2VS, +1.5V, +2.5v, DDR

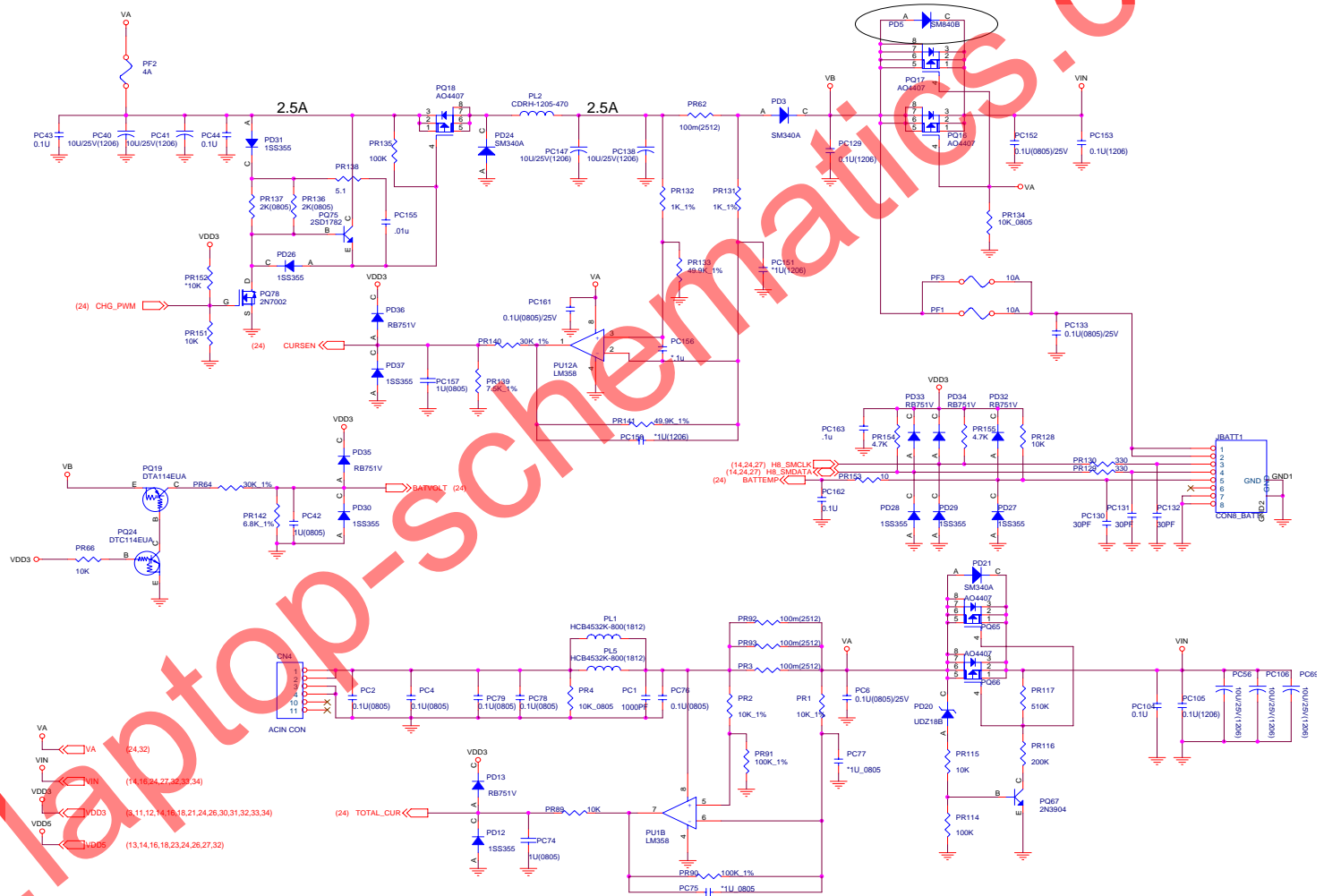


Sheet 34 of 40  
+01.2VS, +1.5V,  
+2.5v, DDR



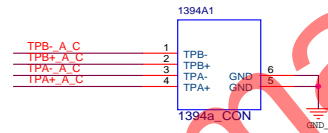
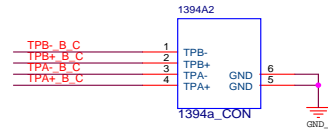
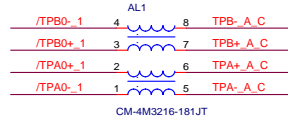
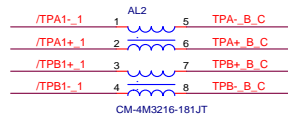
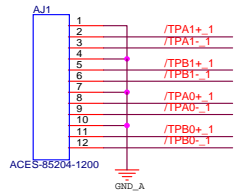
# CHARGER

Sheet 35 of 40  
CHARGER

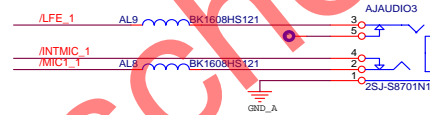
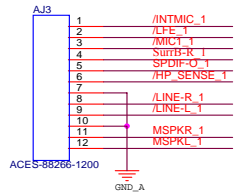


# AUDIO BOARD

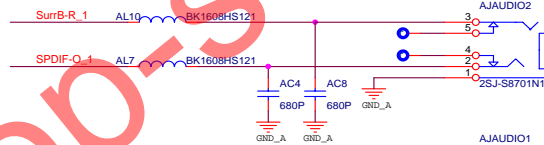
IEEE1394a



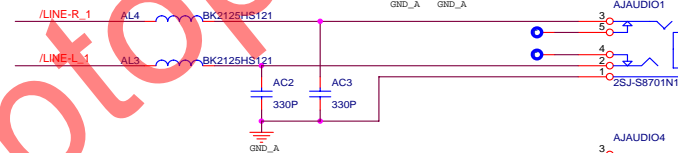
Sheet 36 of 40  
AUDIO BOARD



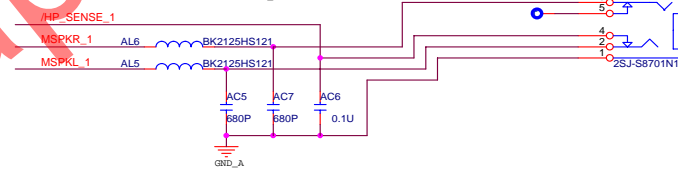
MIC IN  
(CENTER)



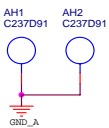
SPDIF OUT  
(SURRB)



LINE IN  
(SURR)

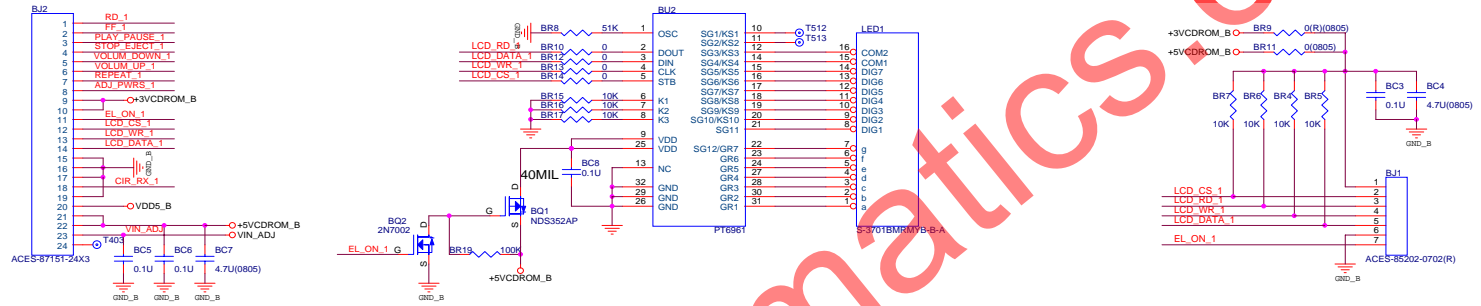


SPEAKER OUT  
(FRONT)

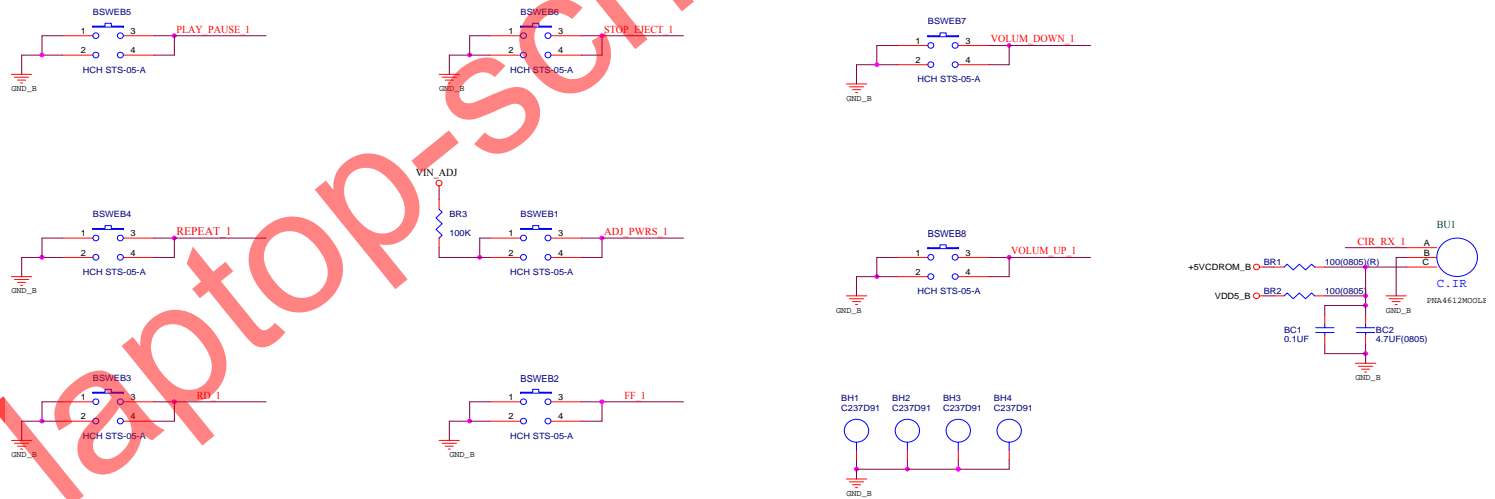




# AUDIO DJ BOARD

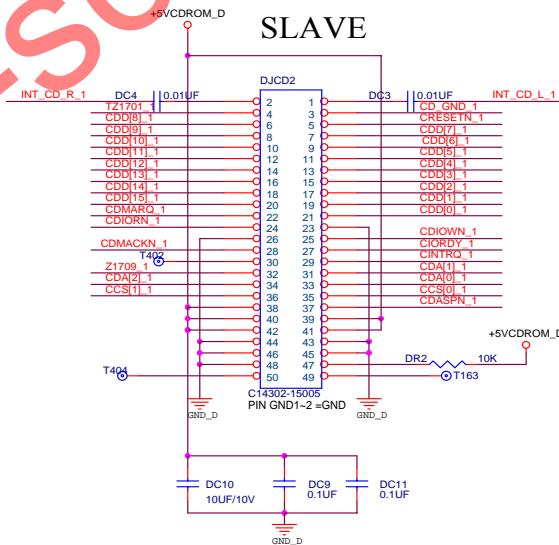
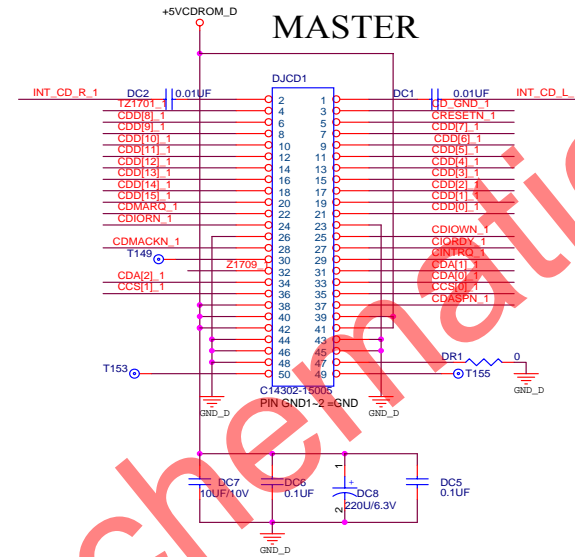
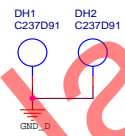
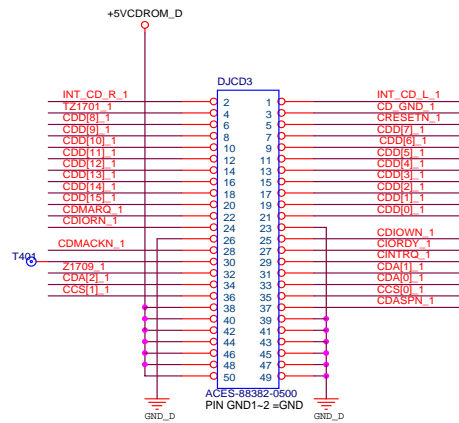


Sheet 37 of 40  
AUDIO DJ BOARD

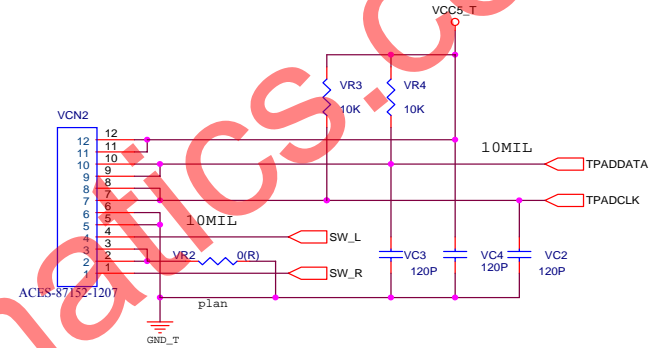
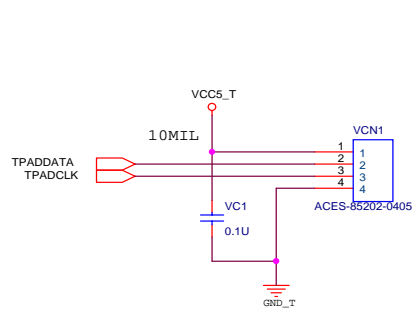


# CD-ROM BOARD

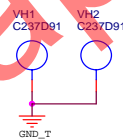
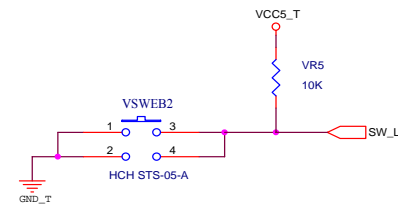
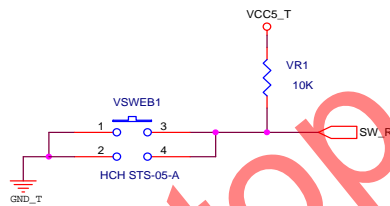
Sheet 38 of 40  
CD-ROM BOARD



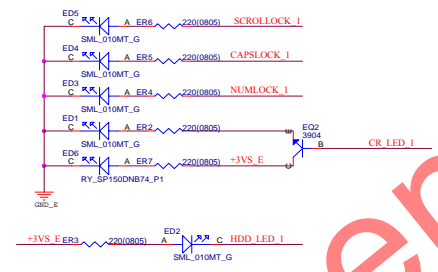
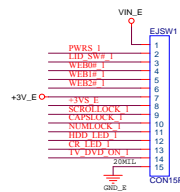
# CLICK BOARD



Sheet 39 of 40  
CLICK BOARD



# SWITCH BOARD



Sheet 40 of 40  
SWITCH BOARD

