

P60, GeFORCE2 MX 200, 4MX16 SDR, 32MB, RGB, TV, AGP4X

PCI DEVICE ID 0X0=0X111 FOR NV11.

STRAPS: AGP4X, SIDEBAND DIS, FAST WRITE DIS, AGP BIOS, NORMAL PCIAD, 14.318MHZ

TV out will be stuffed on both PCB sides!

Stuffing Options Meaning

- 1 BT stuff Brooktree BT868/869 TV encoder
- 2 CX stuff Conexant CX25870/871 TV encoder
- 3 CH stuff Crontel CH7007 TV encoder
- 4 NO_TV no TV, just a bracket without TV cutout
- 5 NV_BOTTOM stuff caps on bottom side under GPU
- 6 RGB_PROT RGB protection diodes


HISTORY:

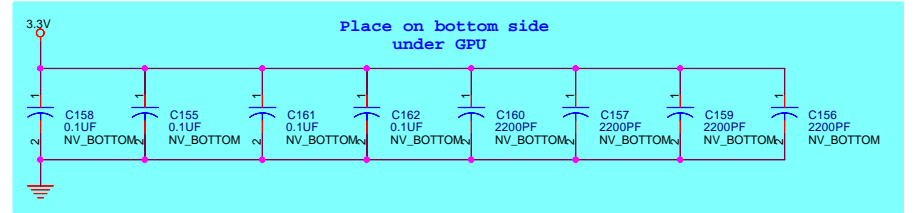
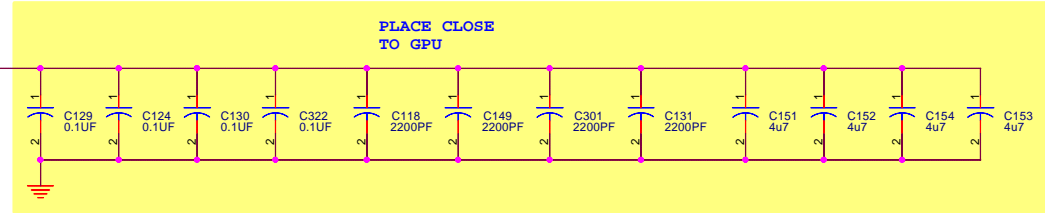
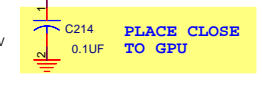
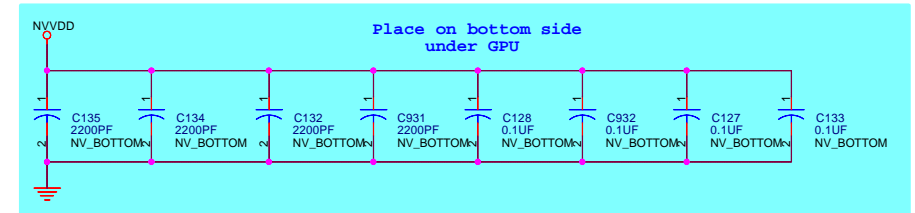
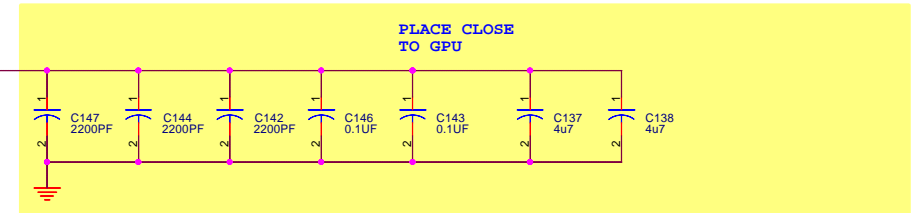
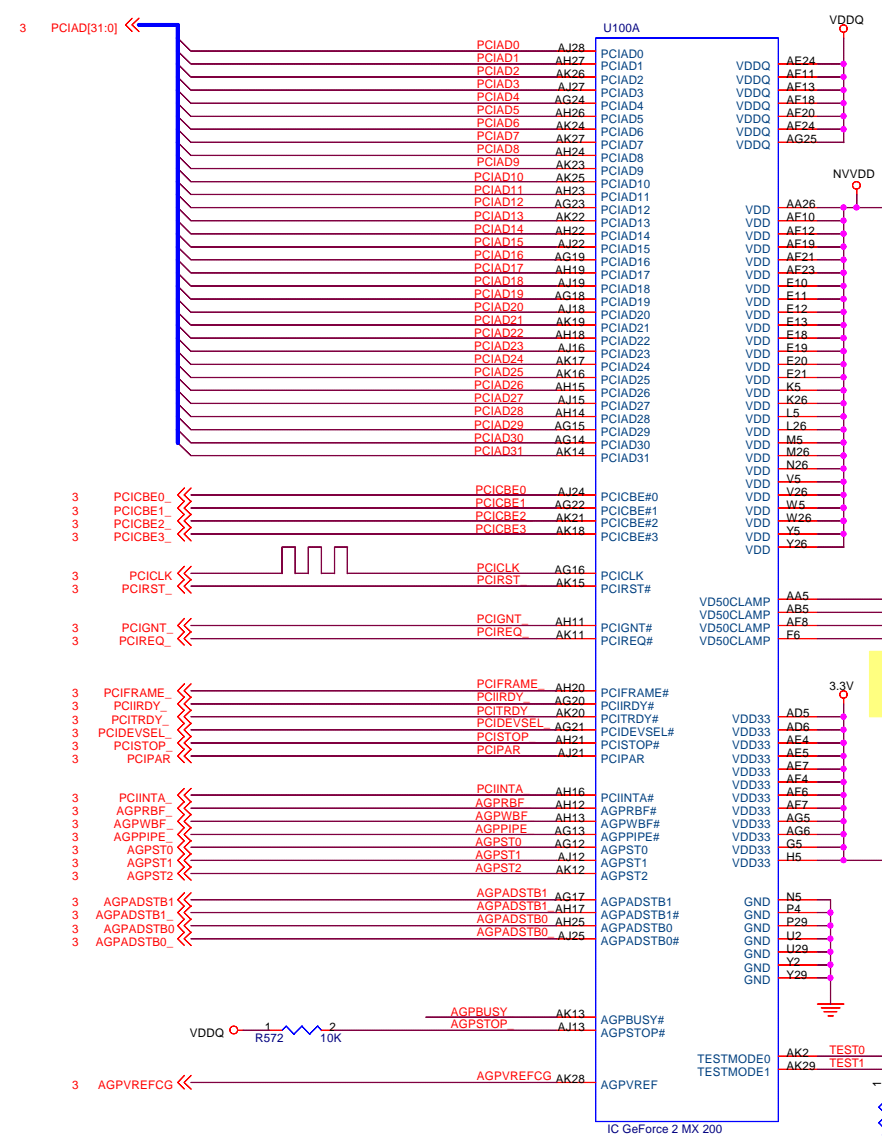
- X00 Based on P43-A01 Initial
- X01 Changed CLK and DQS termination options
- X02 Added alternative caps for power supply
Changed cap packages (cost reduction)
Connected U700.67 to VAA3.3V (CX-fix)
- X03 Moved some strapping to the bottom side
Updated some PCB symbols
- X04 Deleted extra components of the AGP bus
- X05 Added note for DQS feedback.
- X06 C818 changed from 3.3V to 5V decoupling in RGB section (see page 5).
- X07 Updated pin-/function swaps
- X08 added cap for TVCLK from CH to NV11
- X09 deleted unplaceable decoupling caps C140, C141, C150
- A00 no chages, just release ...

PAGE OVERVIEW

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- 6 NVXX FBA/FBB
- 7 FBA DDR 4Mx32
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- 9 TV encoder
- 10 power supply

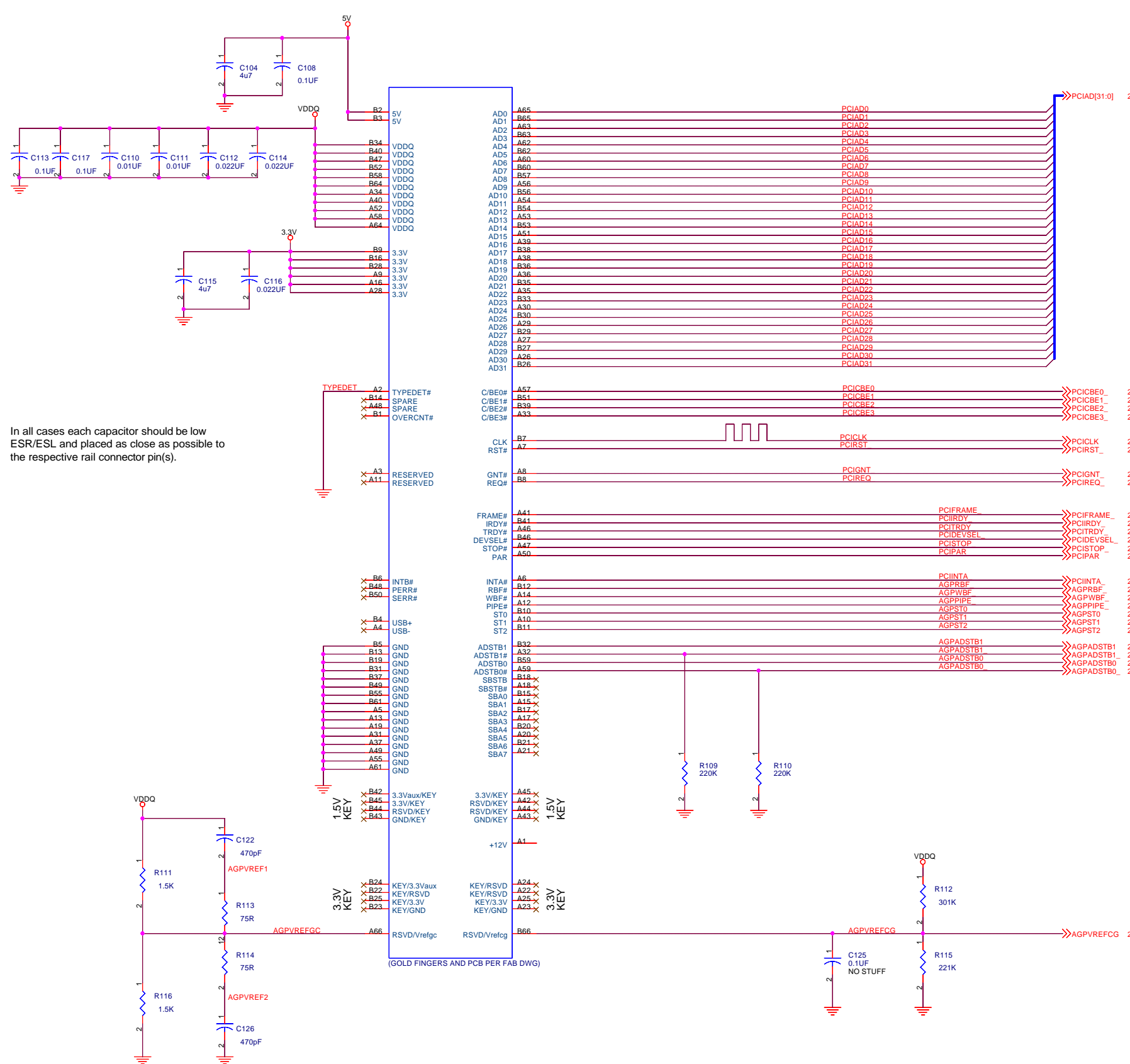
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 NVIDIA	NVIDIA Corporation 3535 Monroe St Santa Clara, CA 95051, USA		
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Size B	CAGE Code	DWG NO	Rev
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1a. NVXX HOST

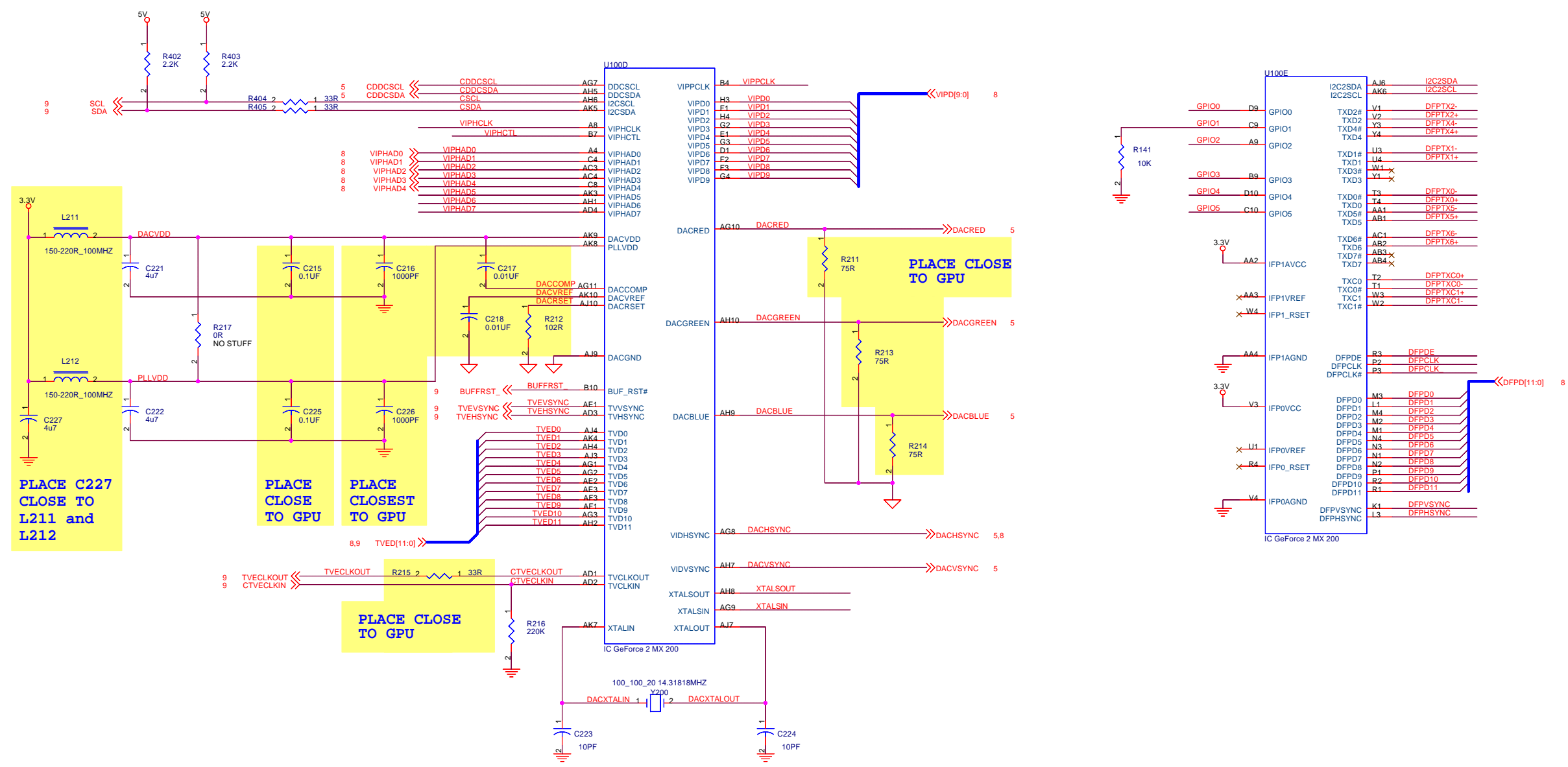
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In all cases each capacitor should be low ESR/ESL and placed as close as possible to the respective rail connector pin(s).

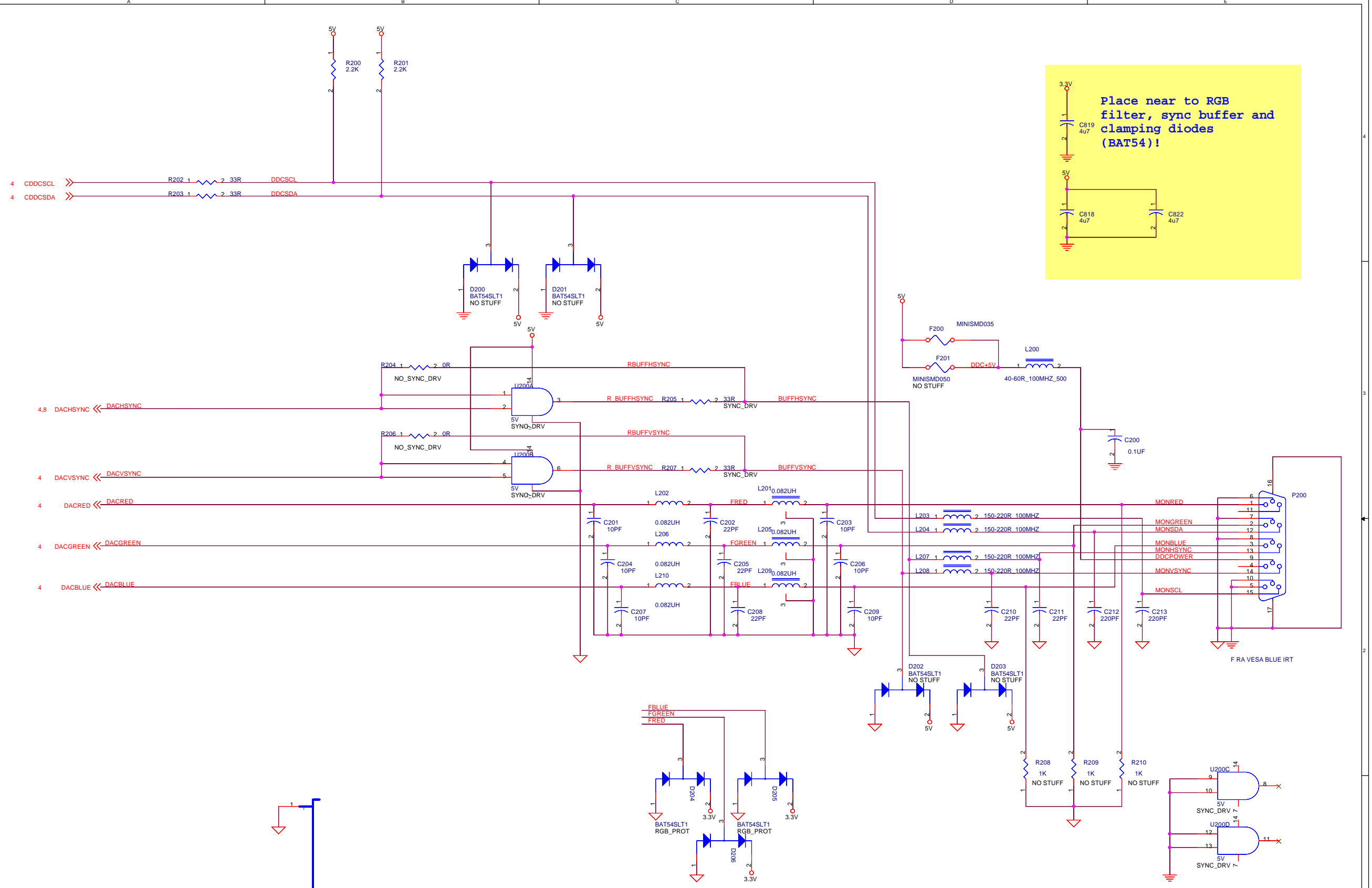
1b1. AGP I/O

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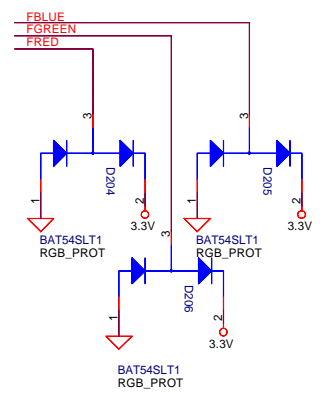
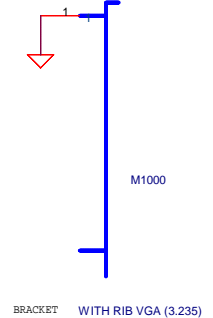


2b. NVXX DAC

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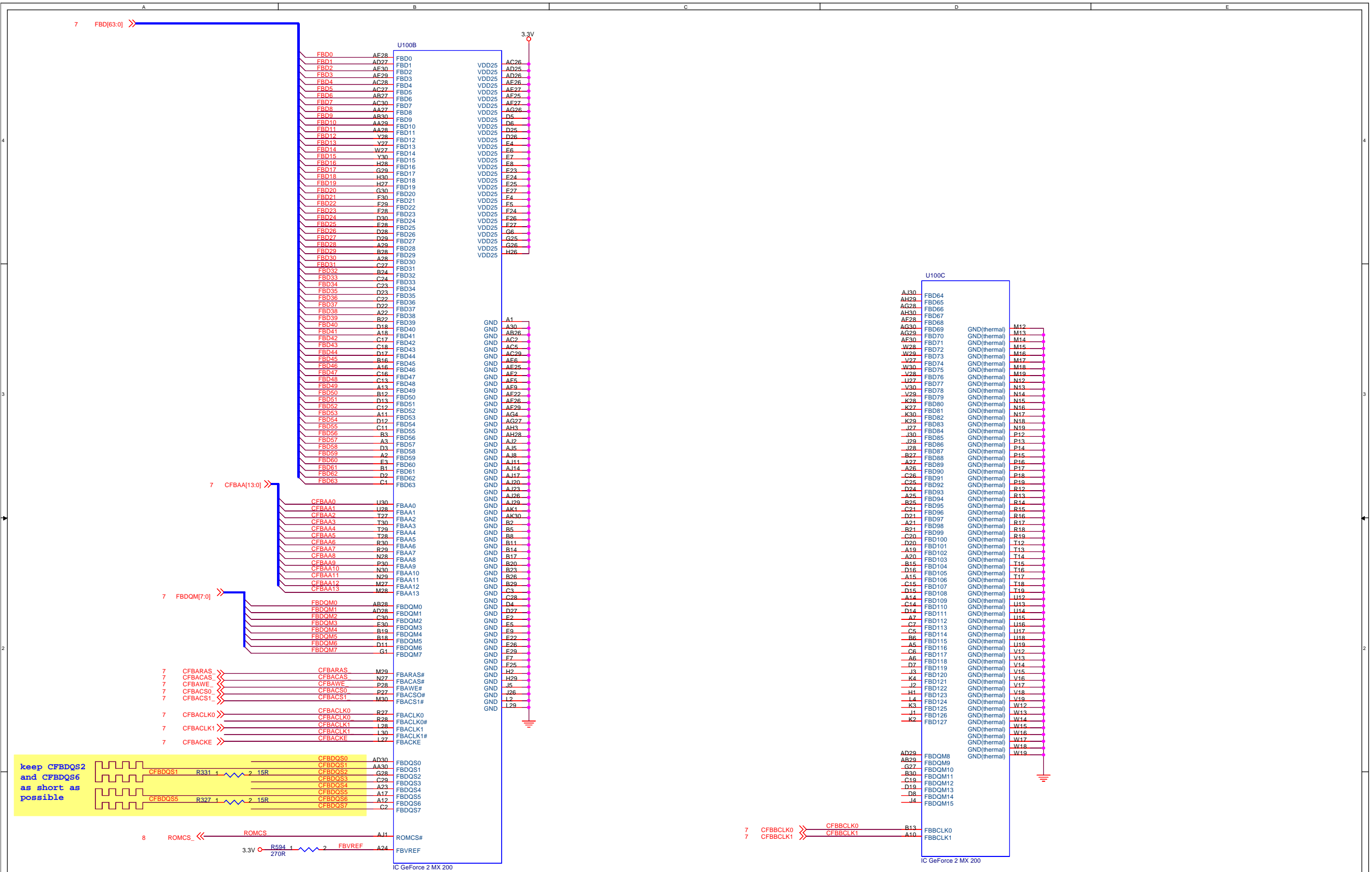


Place near to RGB filter, sync buffer and clamping diodes (BAT54)!



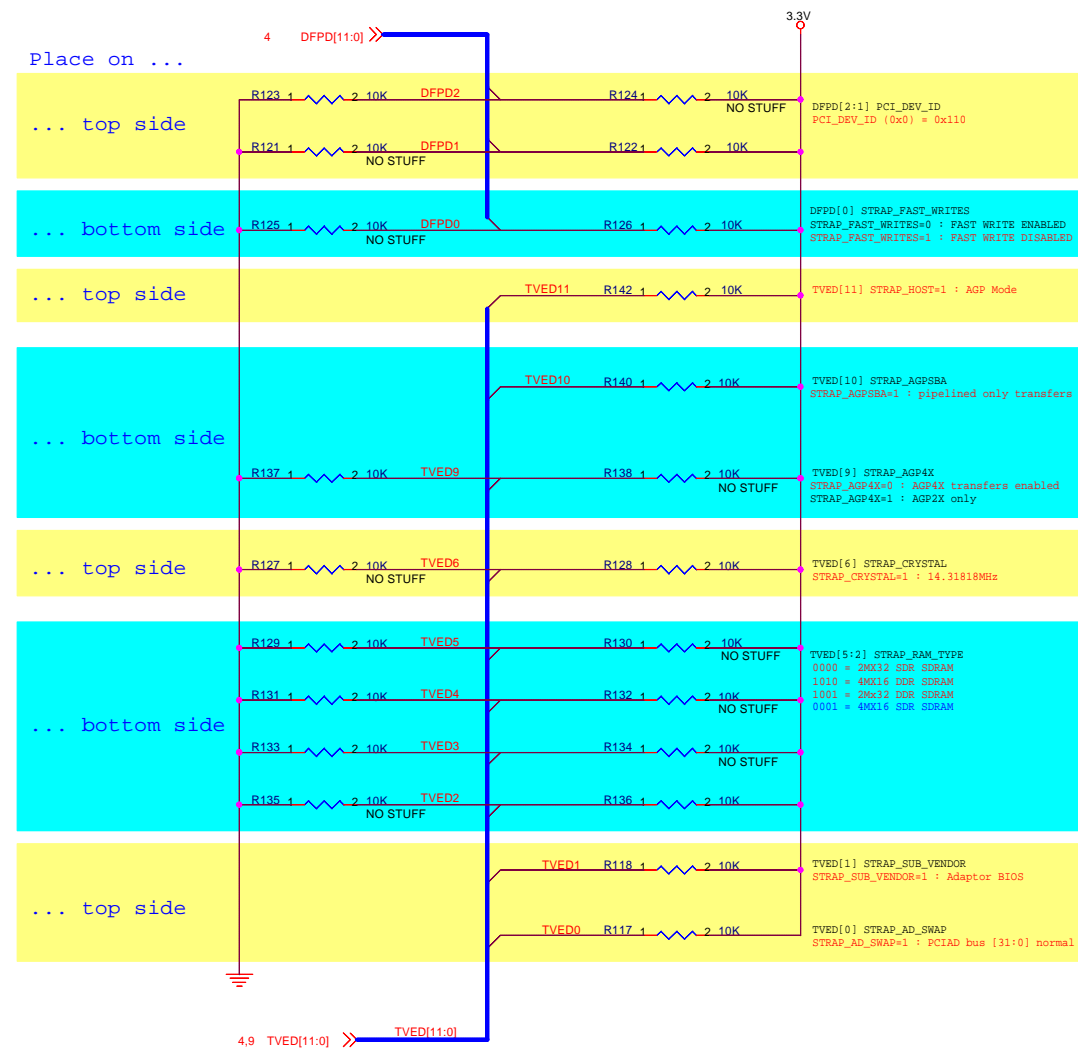
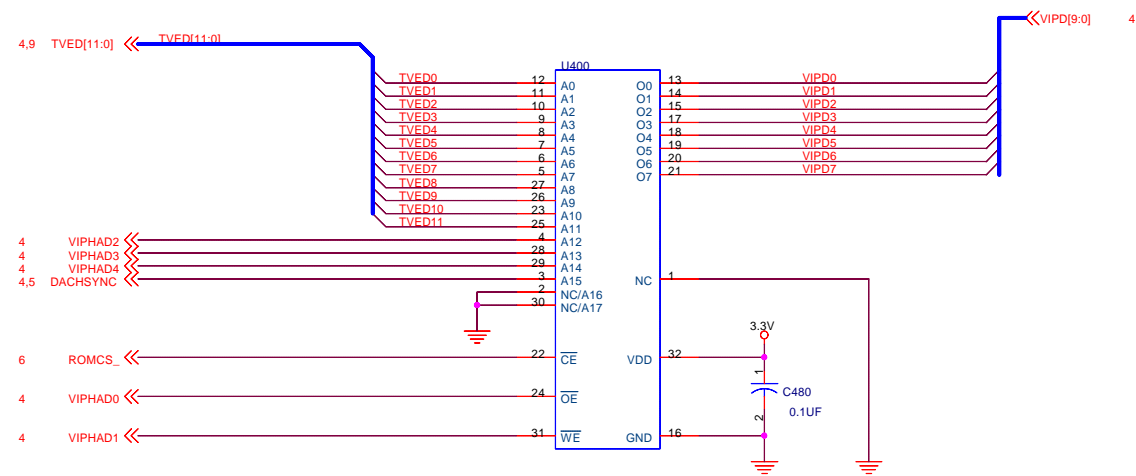
2a. DAC I/O

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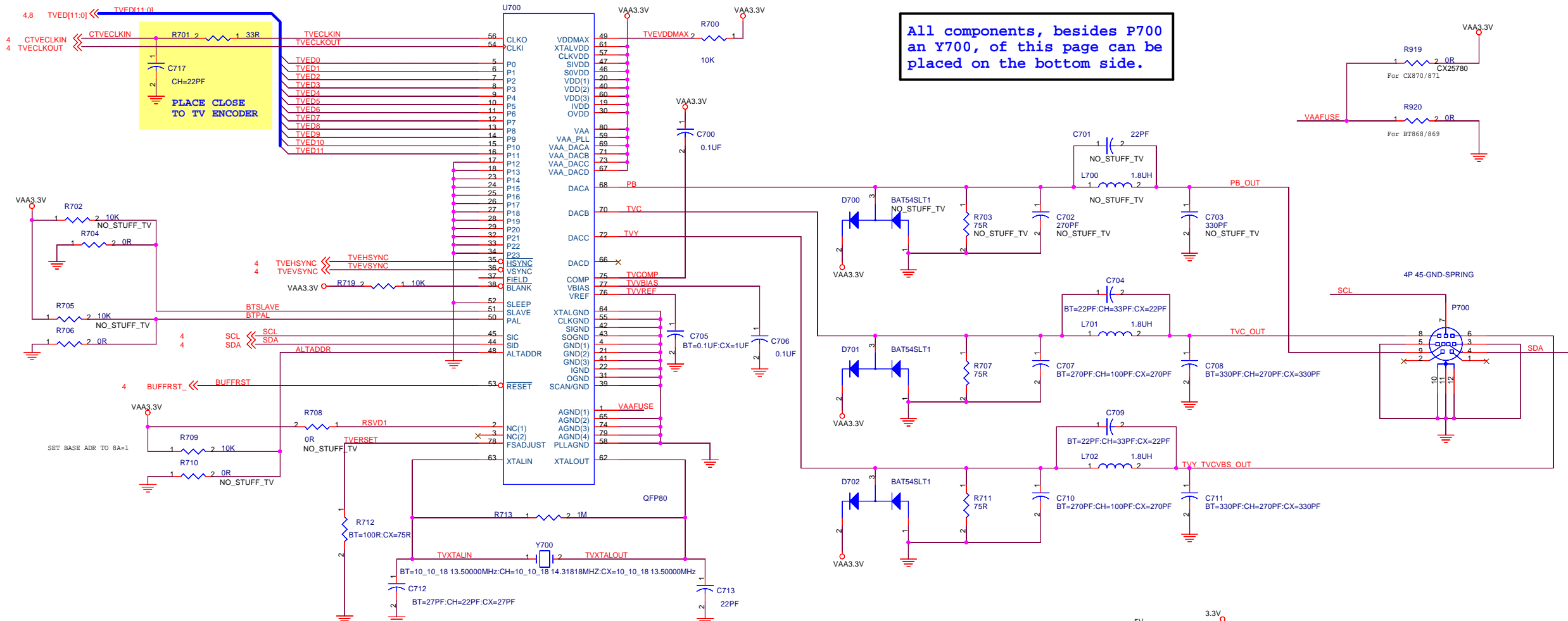
3a. NVXX FBA/FBB

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4a. ROM & STRAPS


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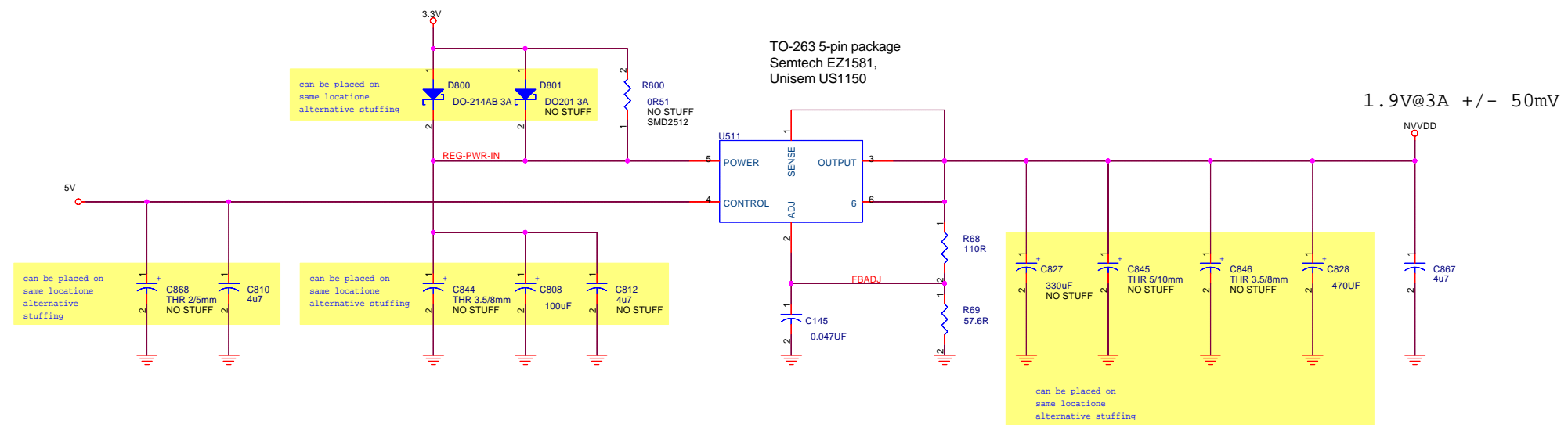


All components, besides P700 an Y700, of this page can be placed on the bottom side.


Parts for Chronitel CH7008/8A only

5a1. TV ENCODERS

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3b. power supply

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