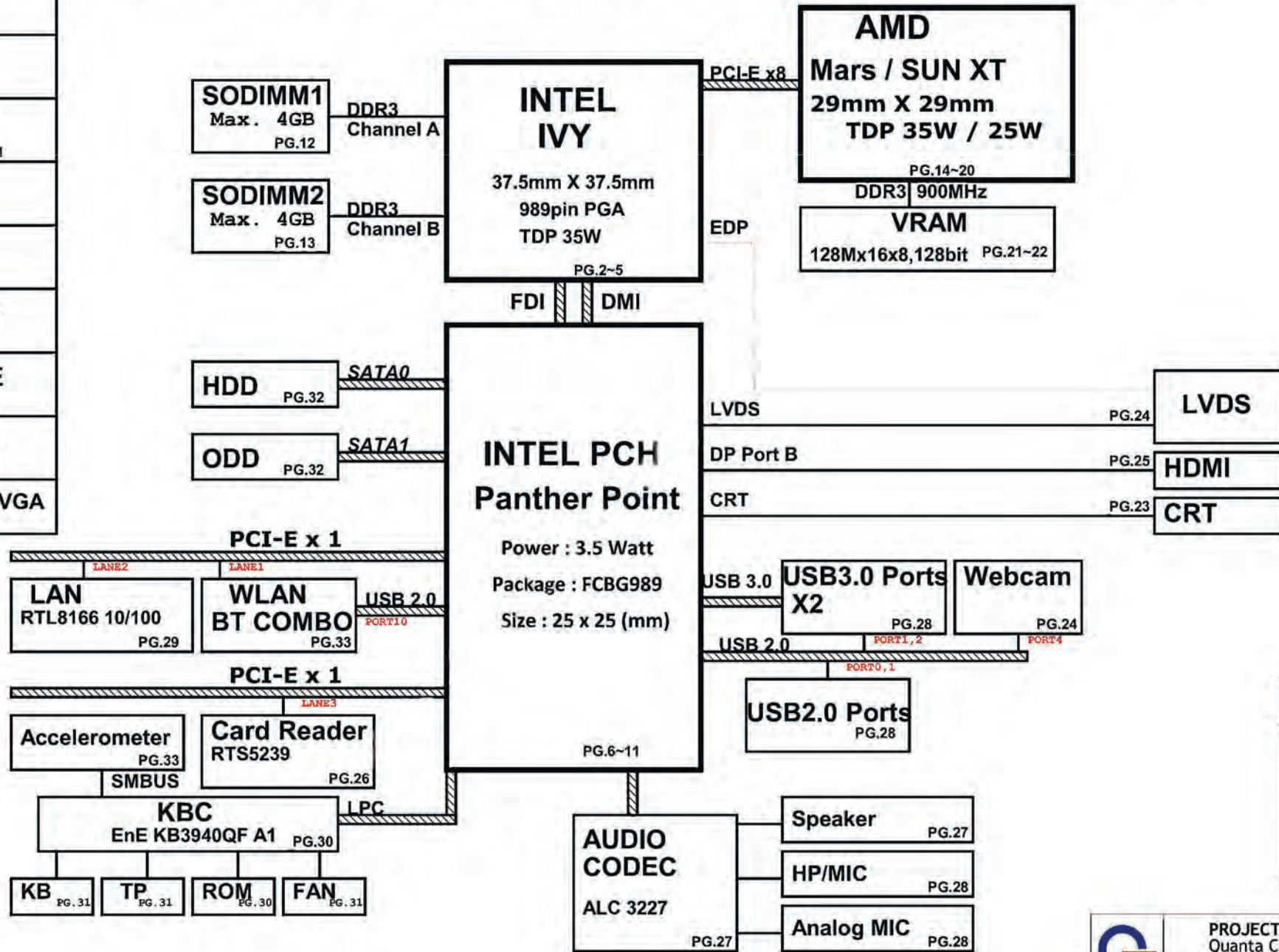


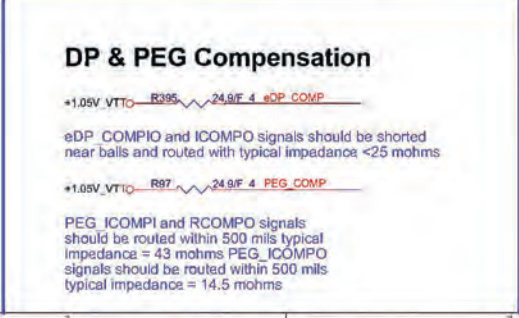
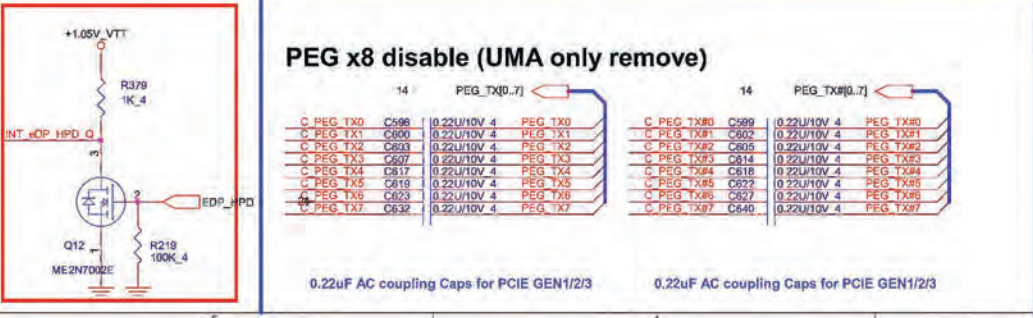
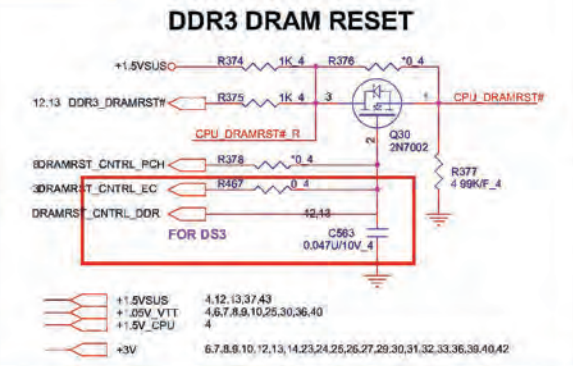
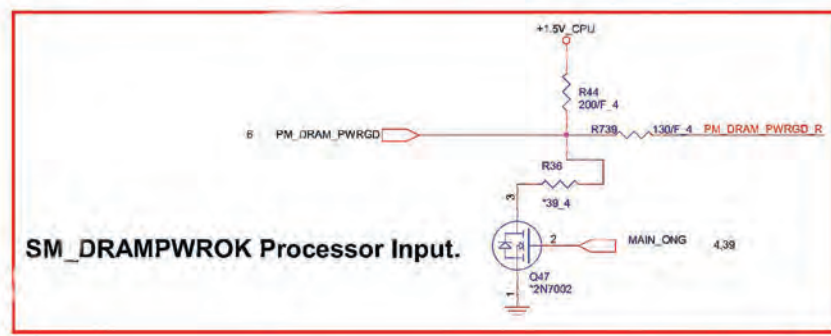
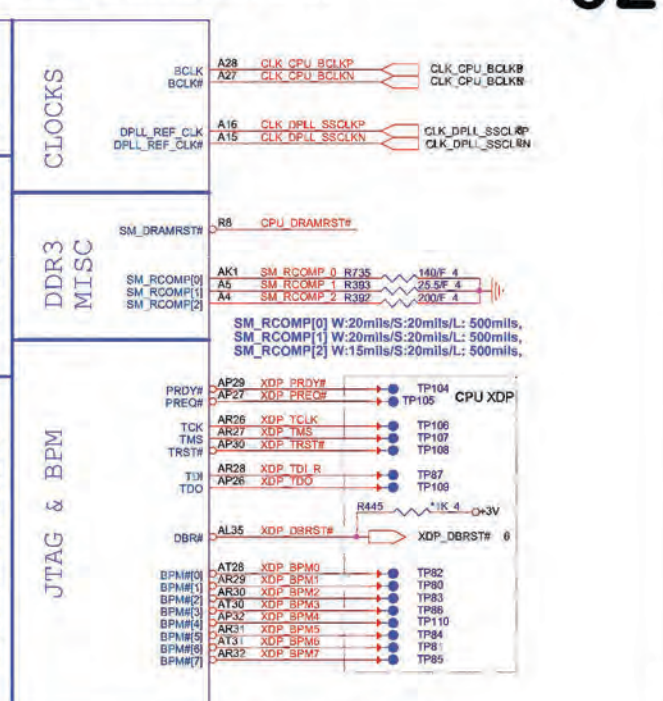
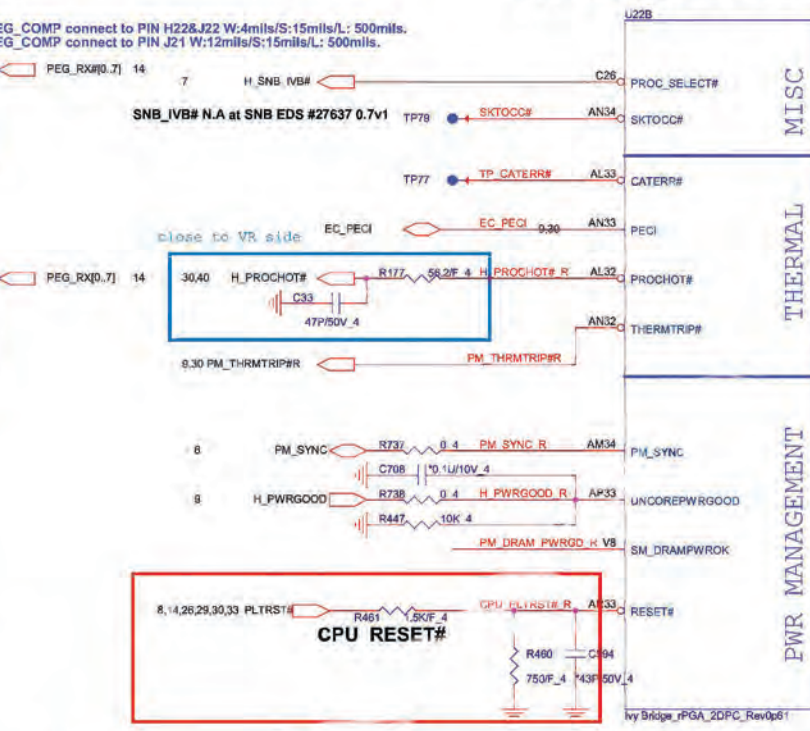
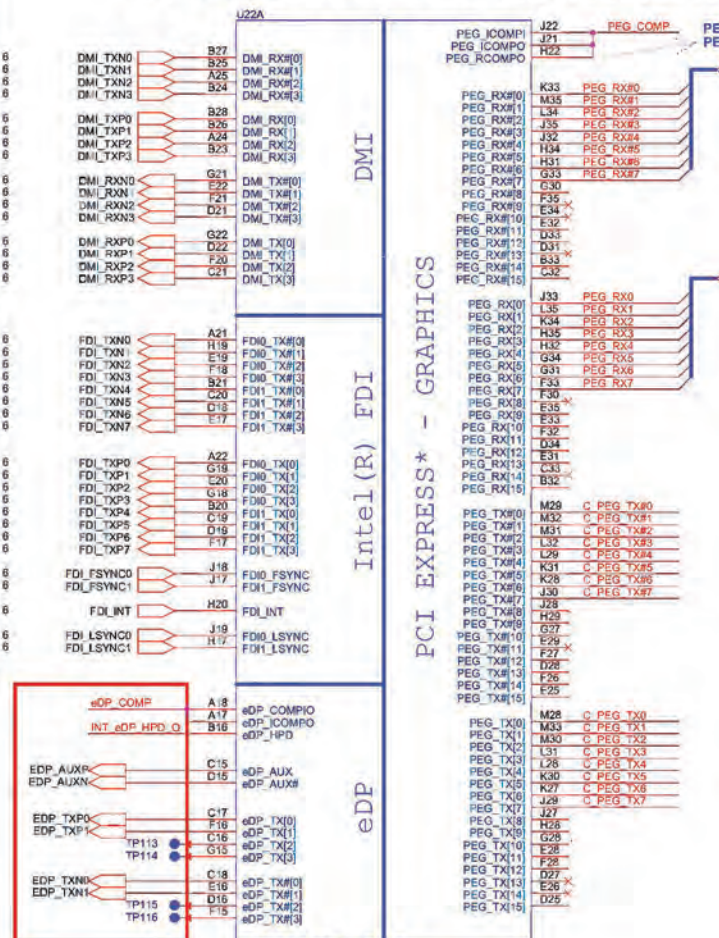
R62 INTEL CHIEF RIVER SYSTEM DIAGRAM

+3V/+5V S5
PG.35
+1.05V
PG.36
CPU Core
PG.40~41
DDR3
PG.37
Charge
PG.34
Dis-Charge
PG.39
+VGACORE
PG.42
+VCCSA
PG.38
+1.0V/+1.8/ +3 VGA
PG.43



Stackup
TOP
GND
IN1
IN2
VCC
BOT

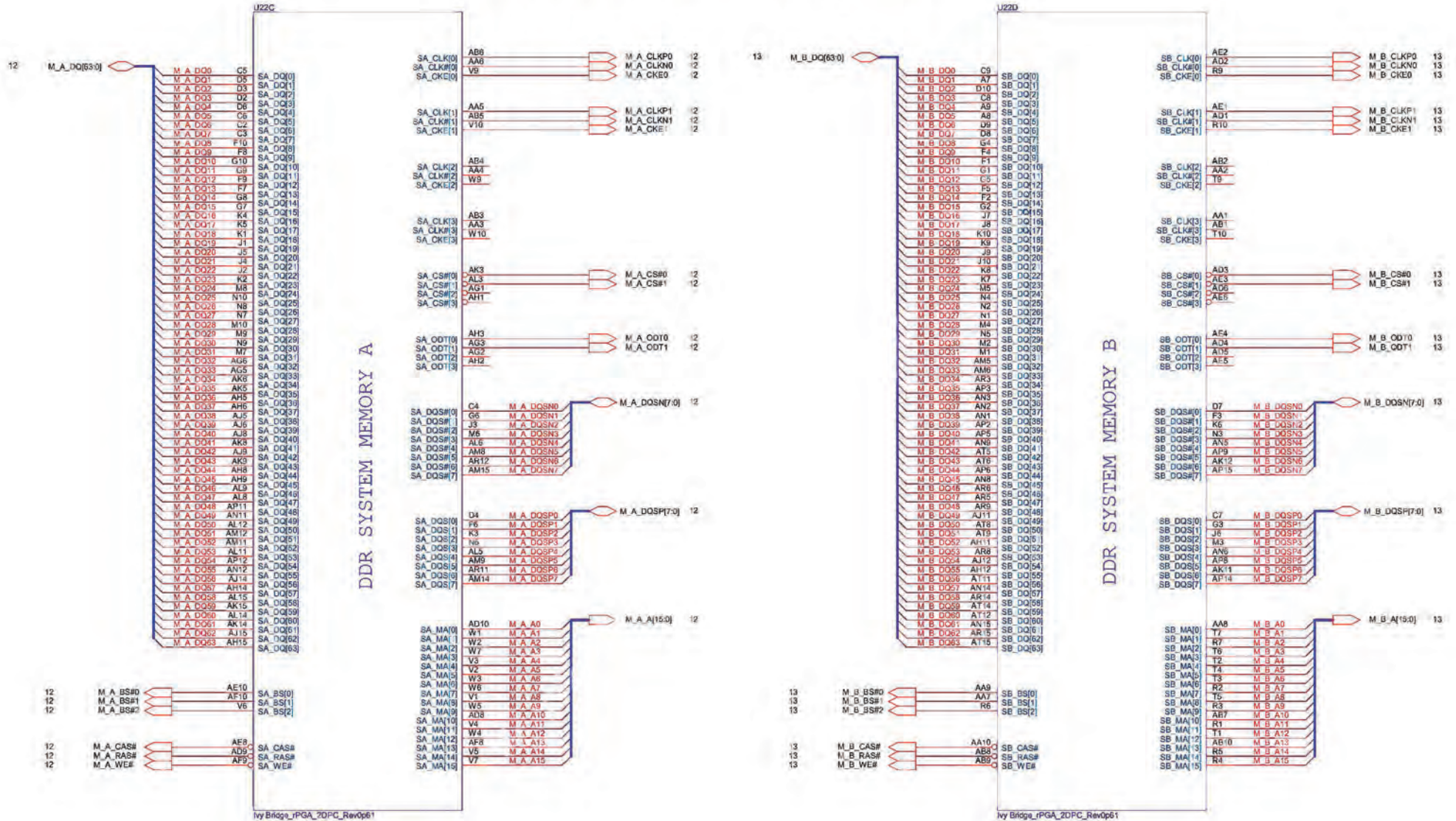
	PROJECT : R62		Rev 1A
	Quanta Computer Inc.		
	Size Custom	Document Number	
BLOCK DIAGRAM		Date: Monday, October 22, 2012	Sheet 1 of 43



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Quanta Computer Inc.

Size: Custom
 Document Number: SNB 1/4 (PCIE&DMI&FDI)
 Date: Monday, October 22, 2012
 Sheet: 2 of 43
 Rev: 1A

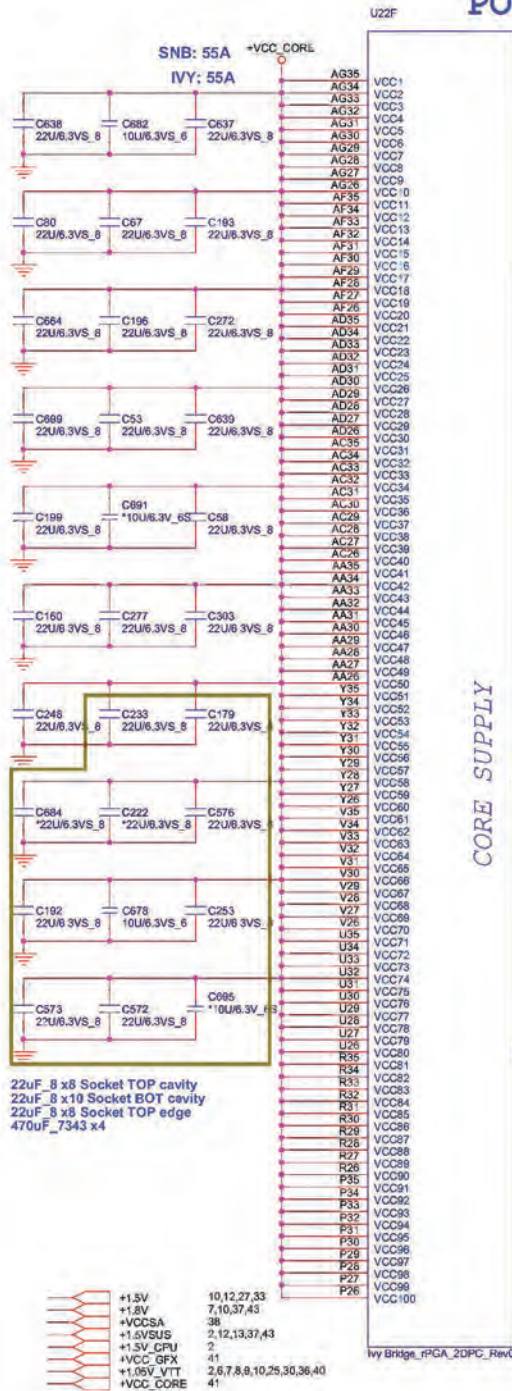
Ivy Bridge Processor (DDR3)



	PROJECT : R62		Rev 1A
	Quanta Computer Inc.		
	Size: Custom Document Number: SNB 2/4 (DDR3 I/F)		
Date: Monday, October 22, 2012		Sheet: 3 of 43	

Ivy Bridge Processor (POWER)

POWER

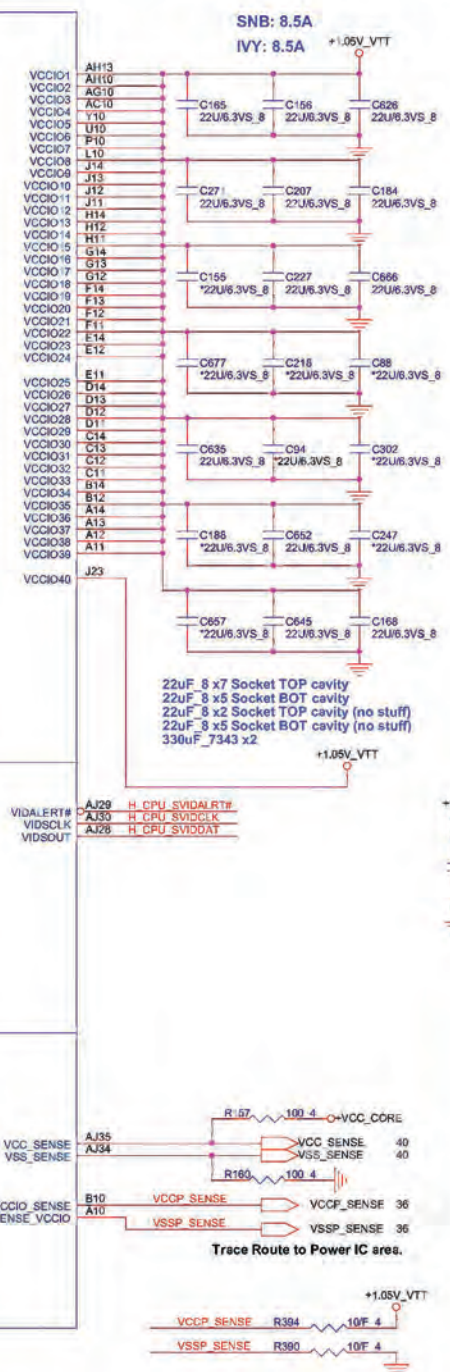


PEG AND DDR

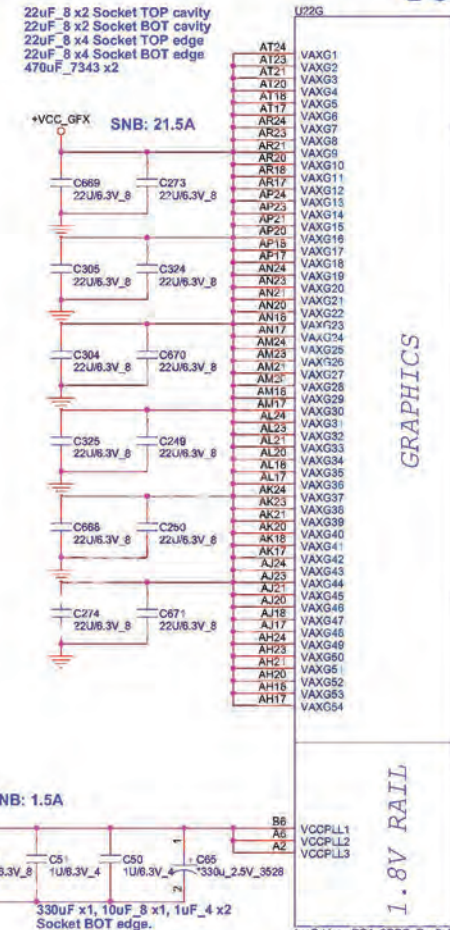
CORE SUPPLY

SVID

SENSE LINES

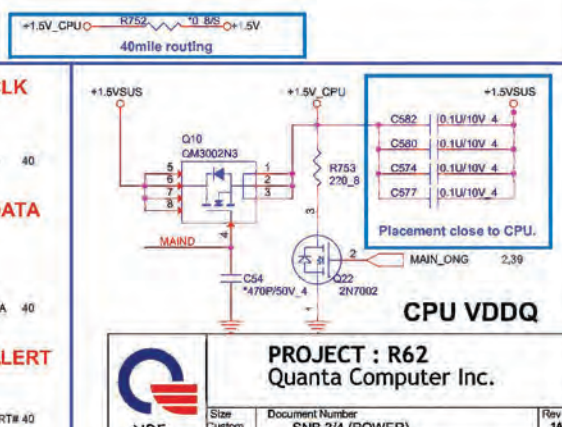
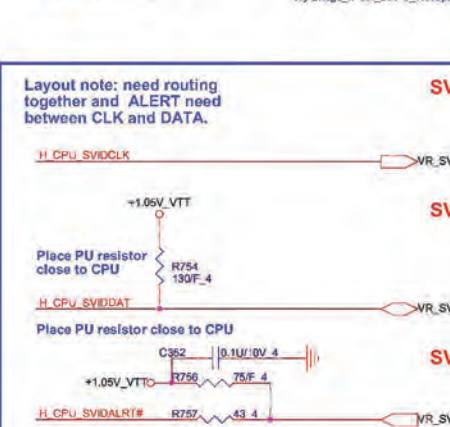
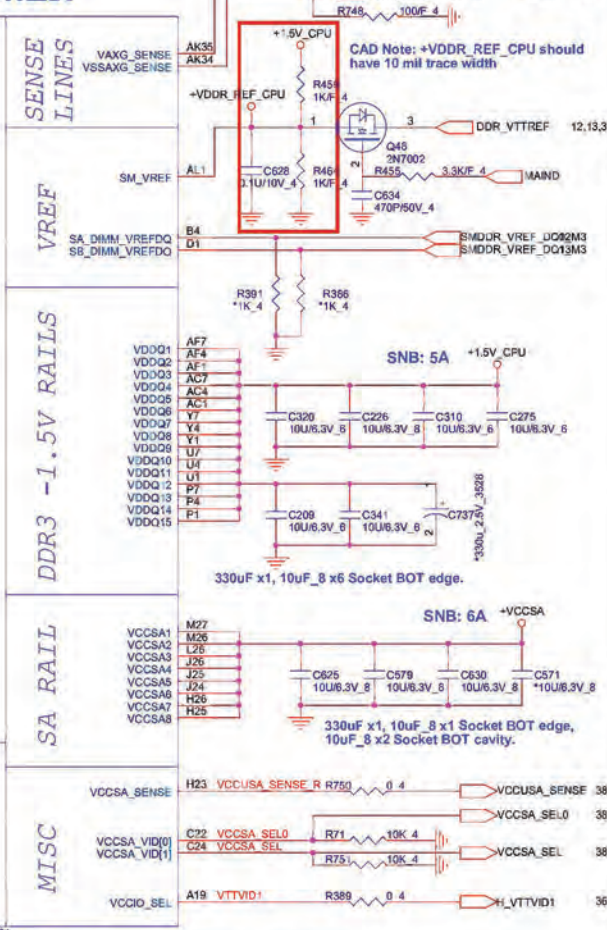


POWER

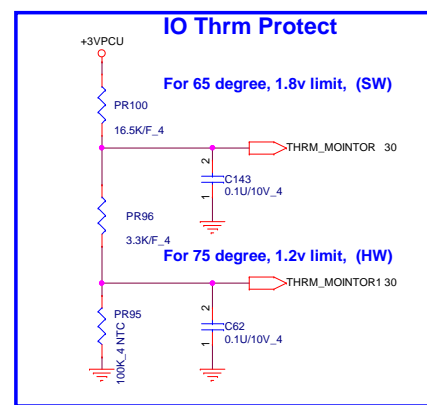
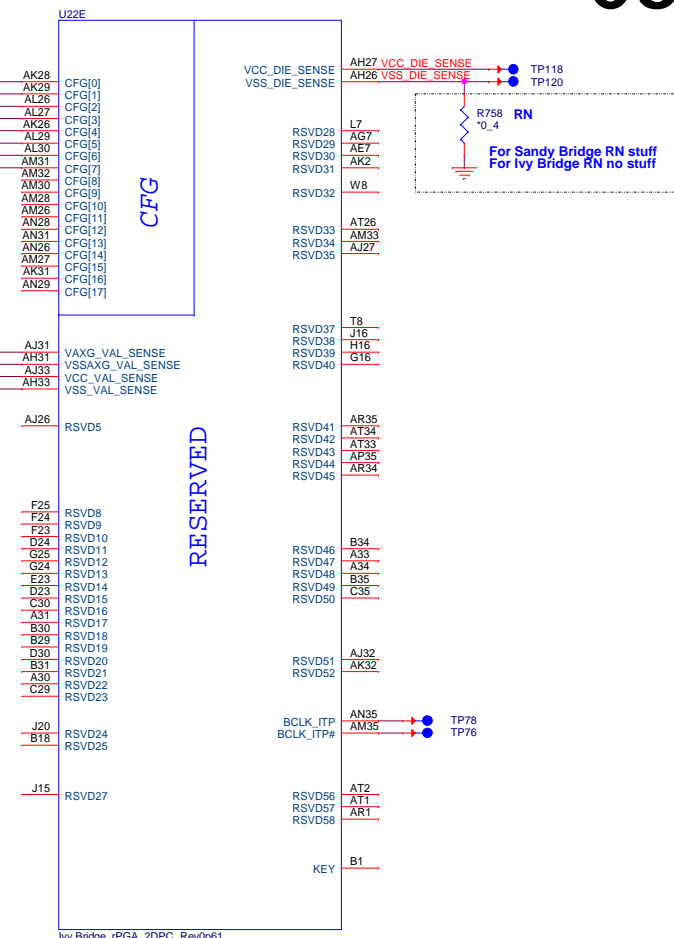
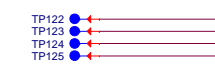
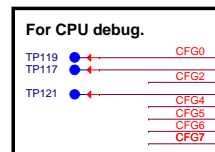
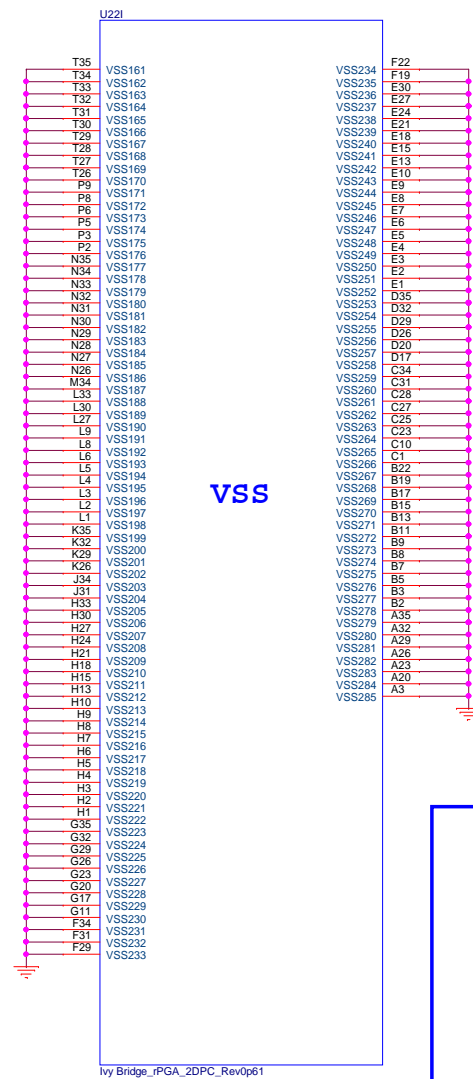
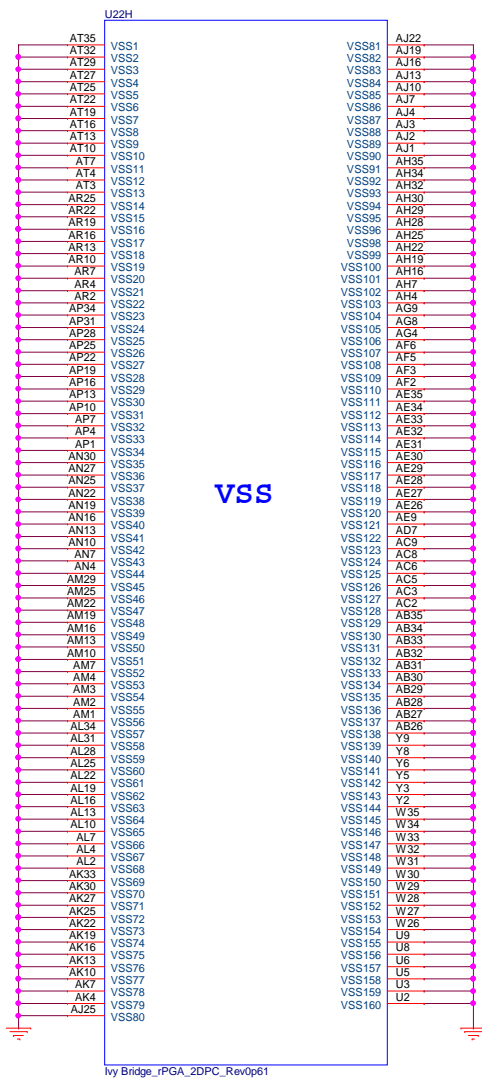


GRAPHICS

1.8V RAIL



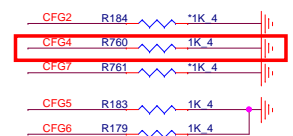
+1.5V	10,12,27,33
+1.8V	7,10,37,43
+VCCSA	38
+1.5VSSUS	2,12,13,37,43
+1.5V_CPU	2
+VCC_GFX	41
+1.05V_VTT	2,6,7,8,9,10,25,30,36,40
+VCC_CORE	41



Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversa)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training

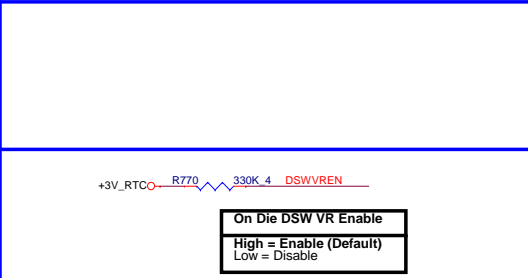
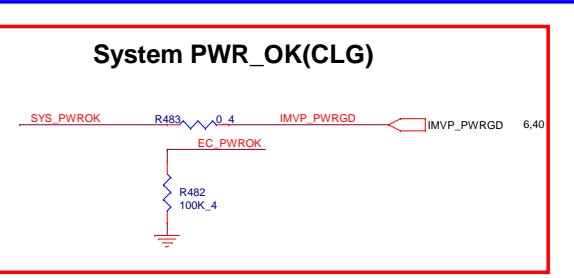
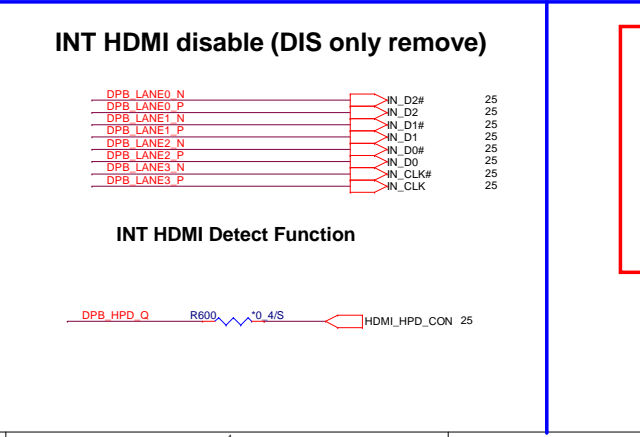
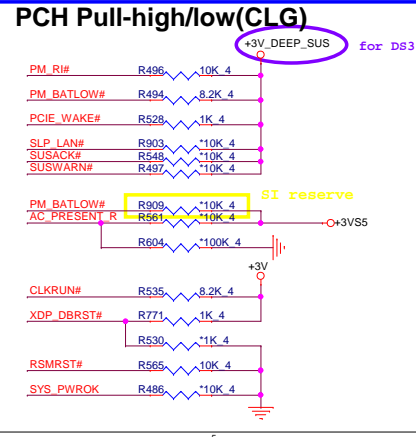
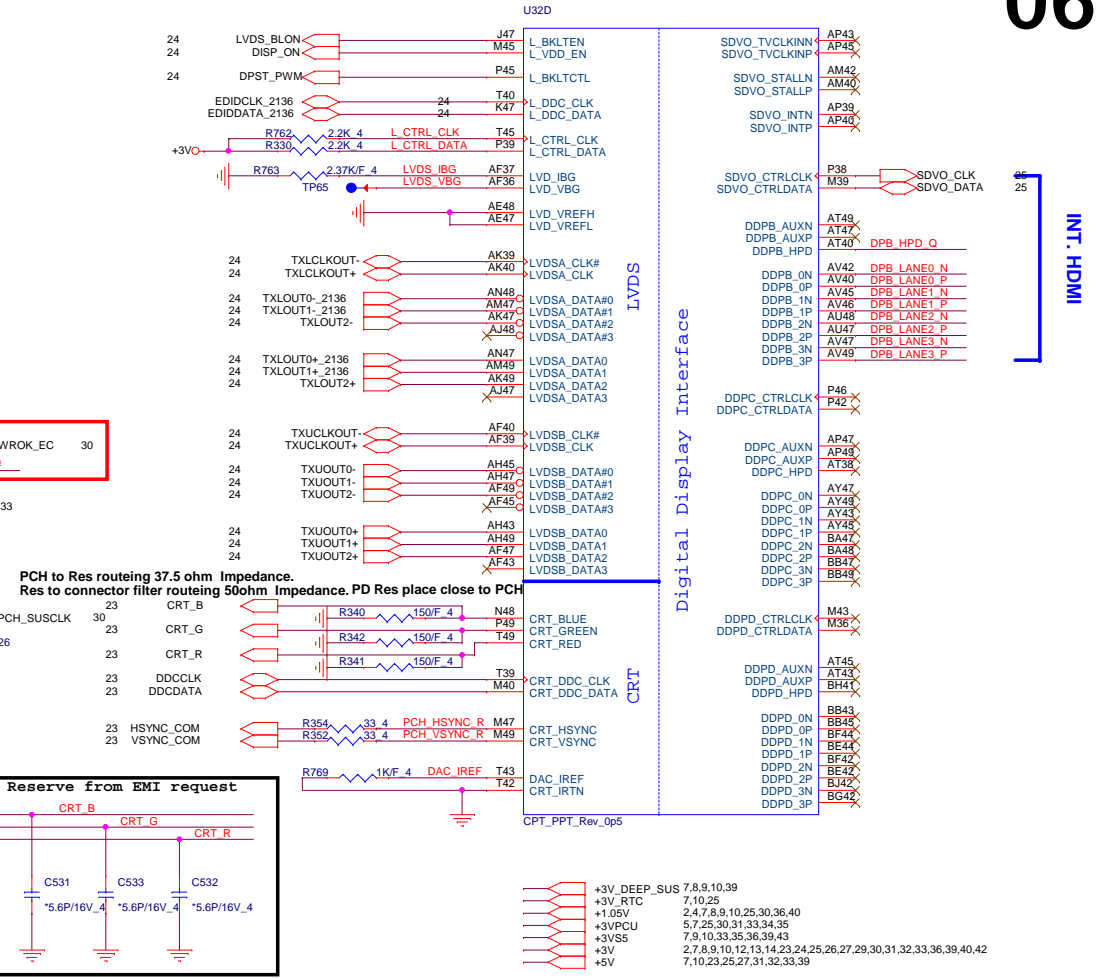
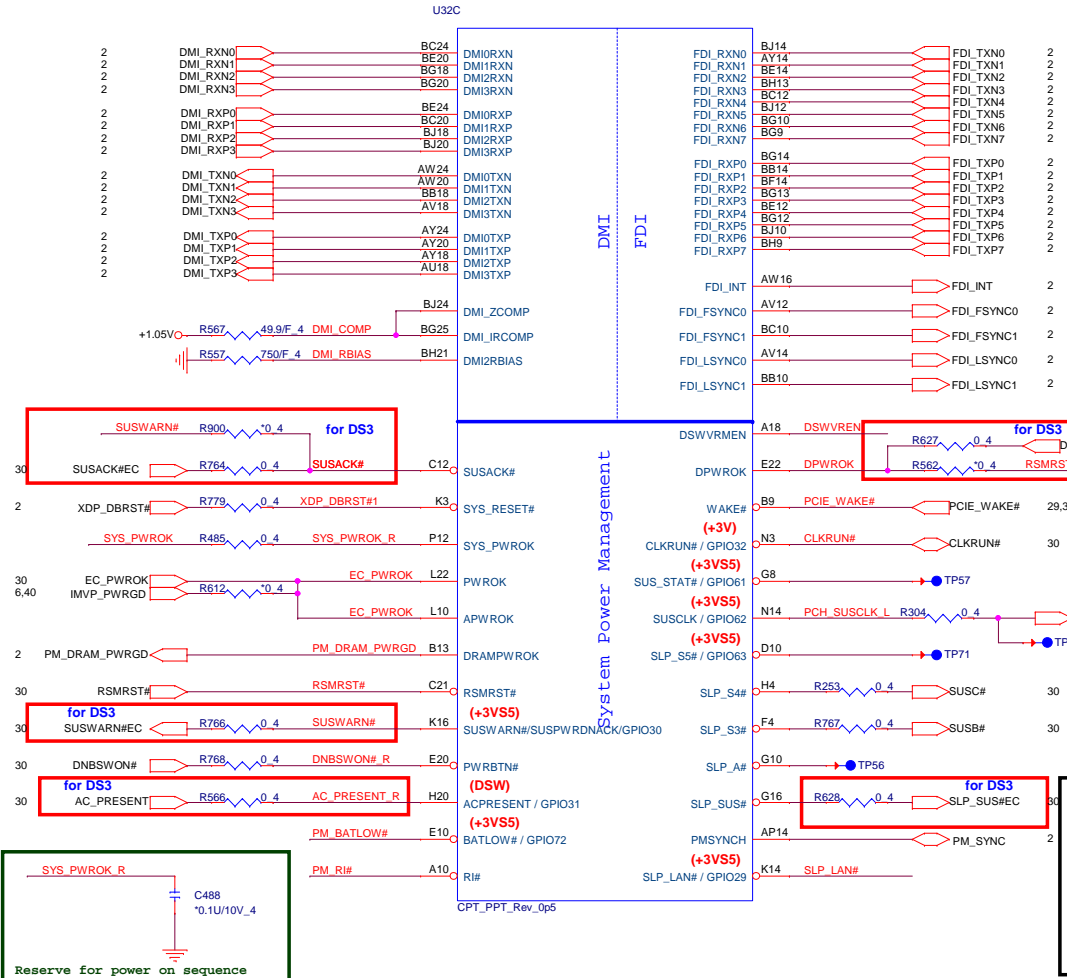


CFG[6:5] (PCIe Port Bifurcation Straps)
 11: (Default) x16 - Device 1 functions 1 and 2 disabled
 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

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Quanta Computer Inc.

NBS

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PCH Pull-high/low (CLG)

Reserve for power on sequence

INT HDMI disable (DIS only remove)

INT HDMI Detect Function

System PWR_OK (CLG)

On Die DSW VR Enable

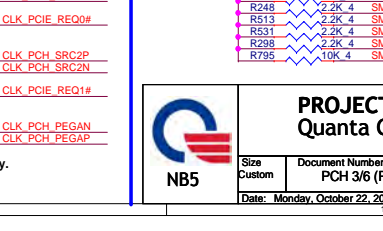
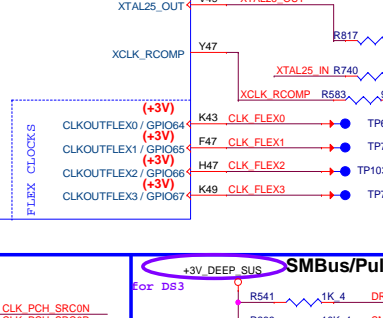
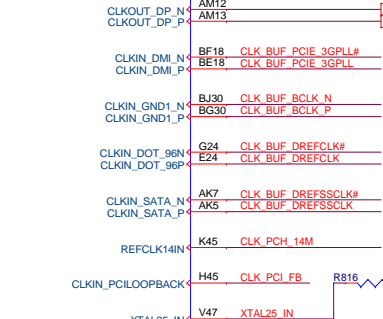
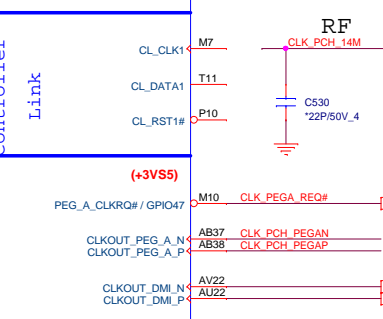
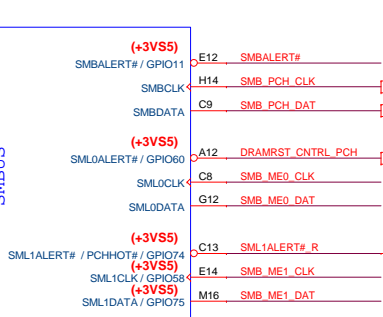
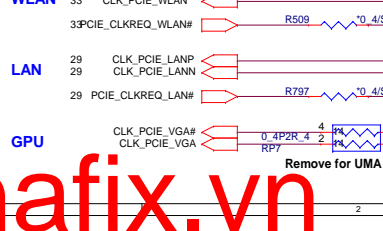
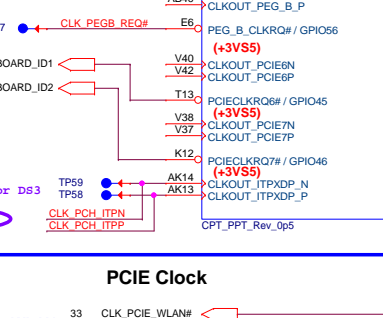
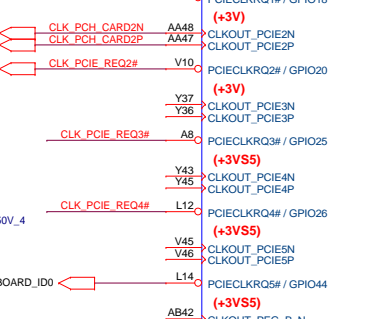
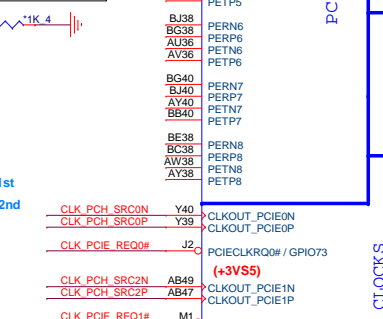
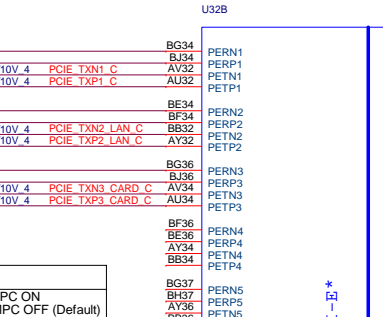
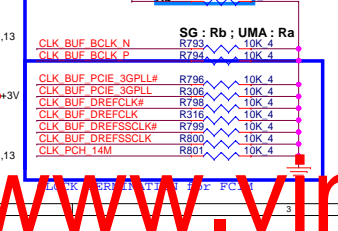
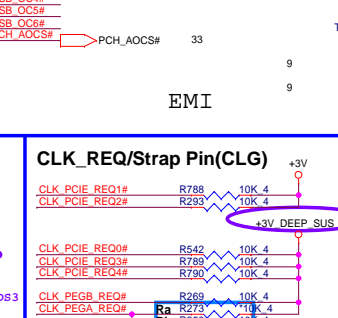
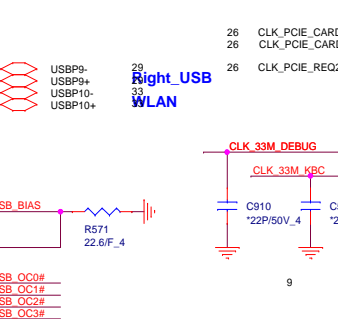
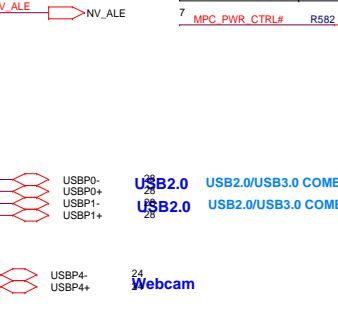
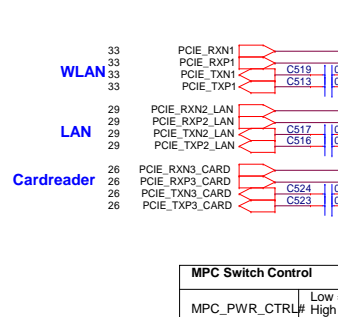
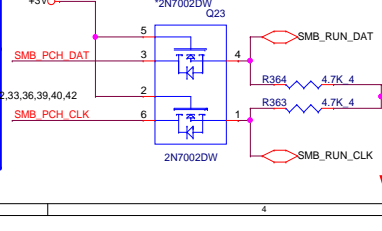
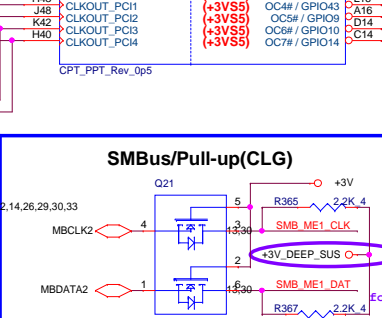
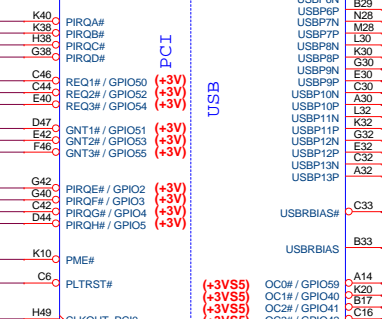
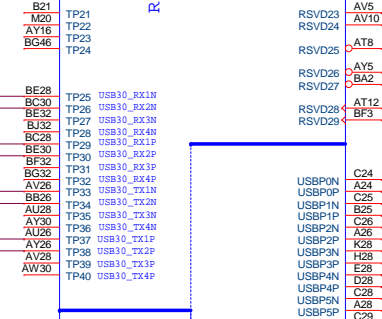
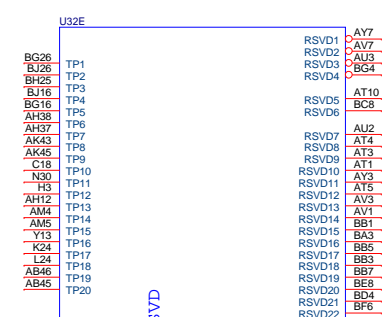
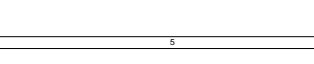
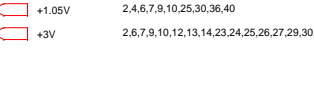
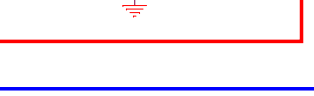
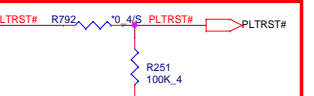
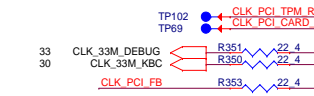
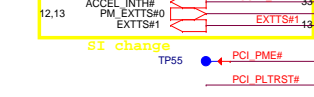
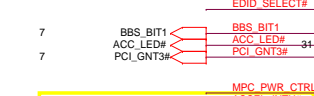
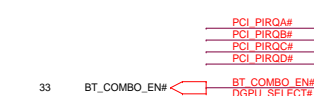
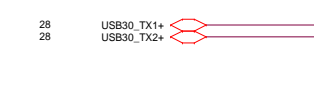
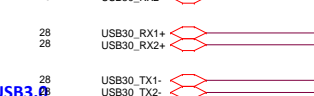
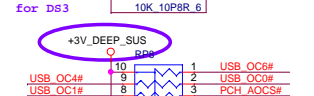
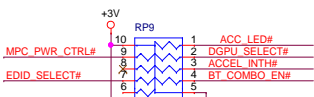
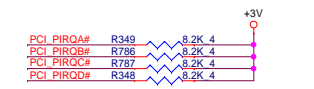
High = Enable (Default)
Low = Disable

PROJECT : R62
Quanta Computer Inc.

Size: Custom
Document Number: PCH 1/6 (DMI/FDI/VIDEO)
Rev: 1A

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PCI/USBOC# Pull-up(CLG)



MPC Switch Control
MPC_PWR_CTRL# Low = MPC ON
High = MPC OFF (Default)

MPC_PWR_CTRL# R582 1K 4

CLK_33M_DEBUG CLK_33M_KBC

CLK_33M_KBC C910 C534

CLK_PCIE_REQ0# CLK_PCIE_REQ1#

CLK_PCIE_REQ2# CLK_PCIE_REQ3#

CLK_PCIE_REQ4#

CLK_PCIE_REQ5#

CLK_PCIE_REQ6#

CLK_PCIE_REQ7#

CLK_PCIE_REQ8#

CLK_PCIE_REQ9#

CLK_PCIE_REQ10#

CLK_PCIE_REQ11#

CLK_PCIE_REQ12#

CLK_PCIE_REQ13#

CLK_PCIE_REQ14#

CLK_PCIE_REQ15#

CLK_PCIE_REQ16#

CLK_PCIE_REQ17#

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CLK_PCIE_REQ19#

CLK_PCIE_REQ20#

CLK_PCIE_REQ21#

CLK_PCIE_REQ22#

CLK_PCIE_REQ23#

CLK_PCIE_REQ24#

CLK_PCIE_REQ25#

CLK_PCIE_REQ26#

CLK_PCIE_REQ27#

CLK_PCIE_REQ28#

CLK_PCIE_REQ29#

CLK_PCIE_REQ30#

CLK_PCIE_REQ31#

CLK_PCIE_REQ32#

CLK_PCIE_REQ33#

CLK_PCIE_REQ34#

CLK_PCIE_REQ35#

CLK_PCIE_REQ36#

CLK_PCH_14M

CLK_PCH_14M C530

CLK_PCH_14M *22P/50V_4

CLK_PCH_14M

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CLK_PCH_14M

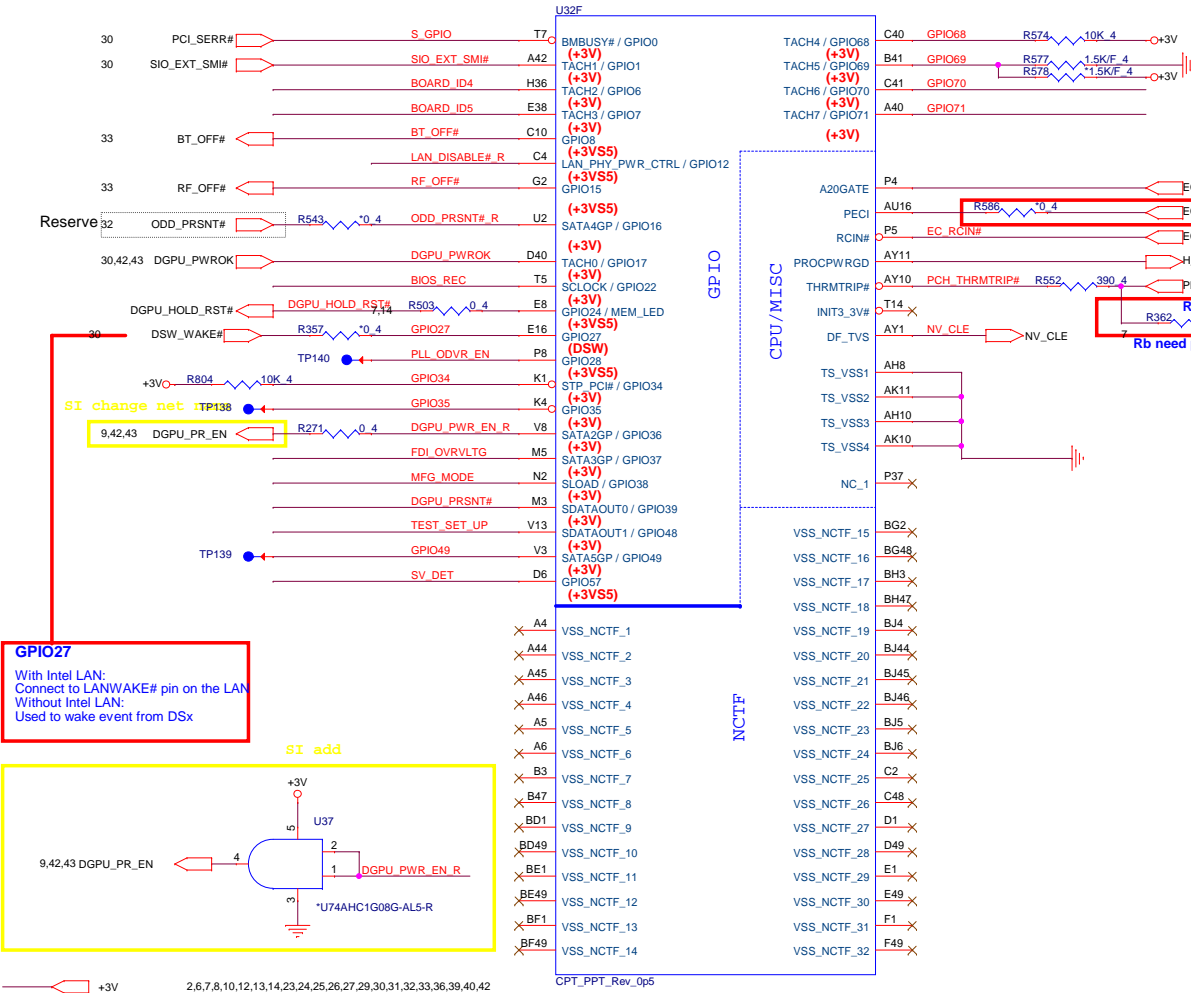
CLK_PCH_14M

PROJECT : R62
Quanta Computer Inc.

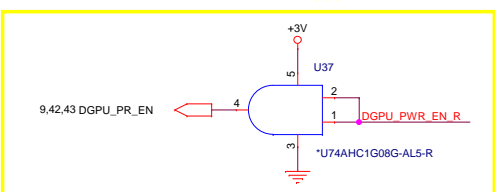
Size Custom Document Number PCH 3/6 (PCI-E/USB/CLK) Rev 1A

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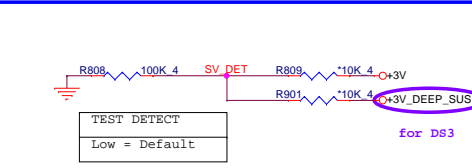
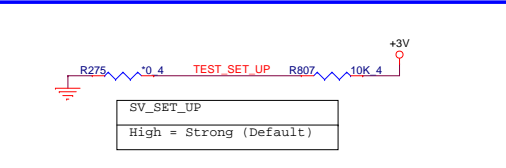
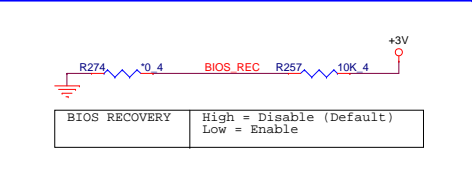
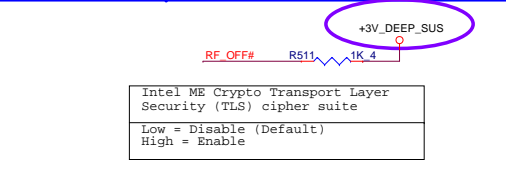
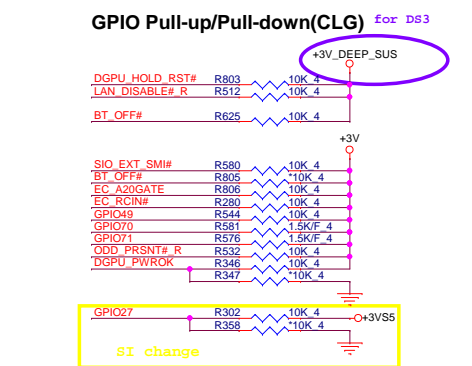
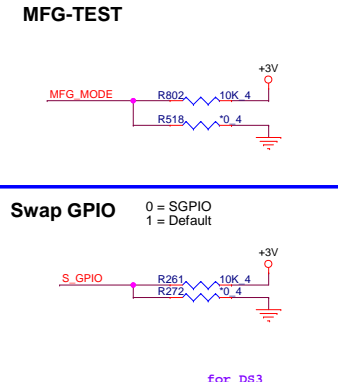
Cougar Point/Panther Point (GPIO,VSS_NCTF,RSVD)



GPIO27
 With Intel LAN:
 Connect to LANWAKE# pin on the LAN
 Without Intel LAN:
 Used to wake event from DSx

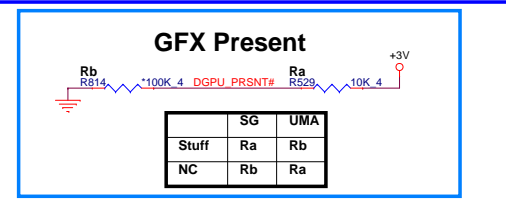
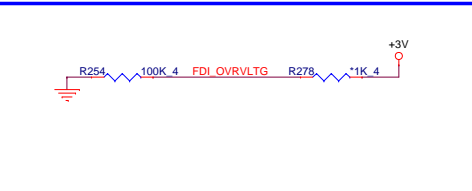
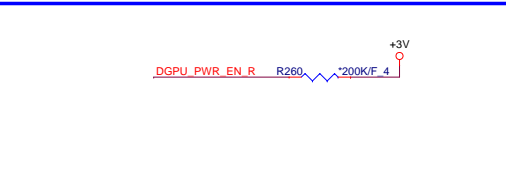
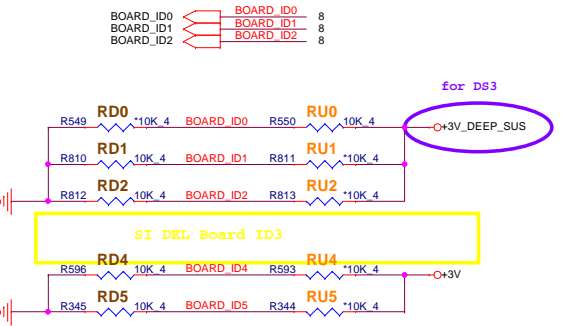


SI add



BOARD ID SETTING

Model	BOARD_ID5	BOARD_ID4	BOARD_ID3	BOARD_ID2	BOARD_ID1	BOARD_ID0
DB R62 UMA				0	0	0
DB R62 DIS				0	0	1
			0	1	1	1
		1	1	1	1	1
		0	0	0	0	0



PROJECT : R62
 Quanta Computer Inc.

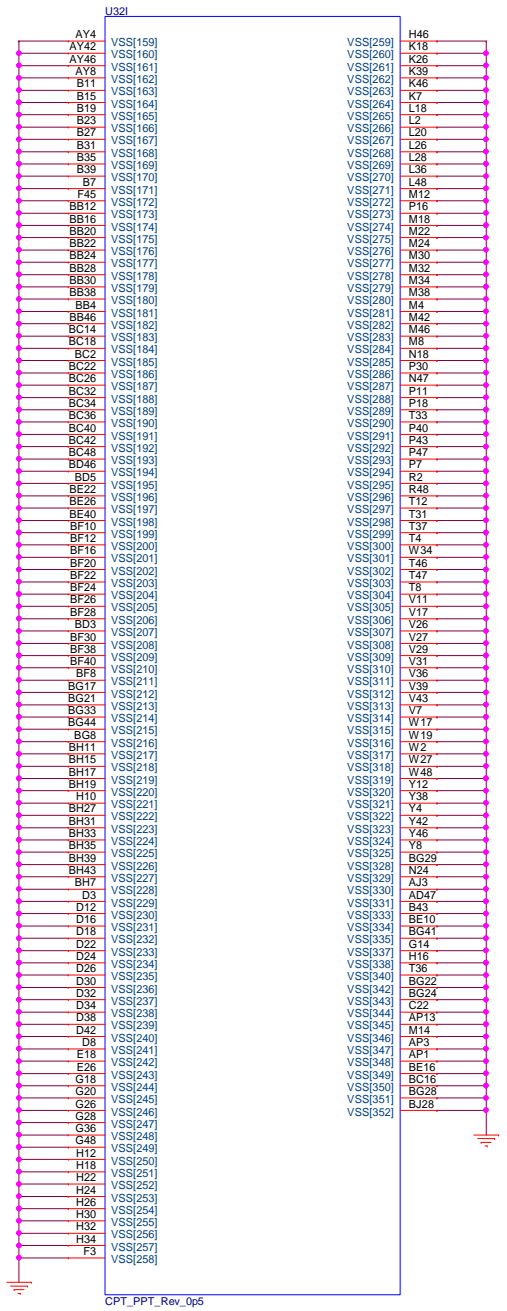
NB5

Size	Document Number	Rev
Custom	PCH 4/6 (GPIO/MISC)	1A

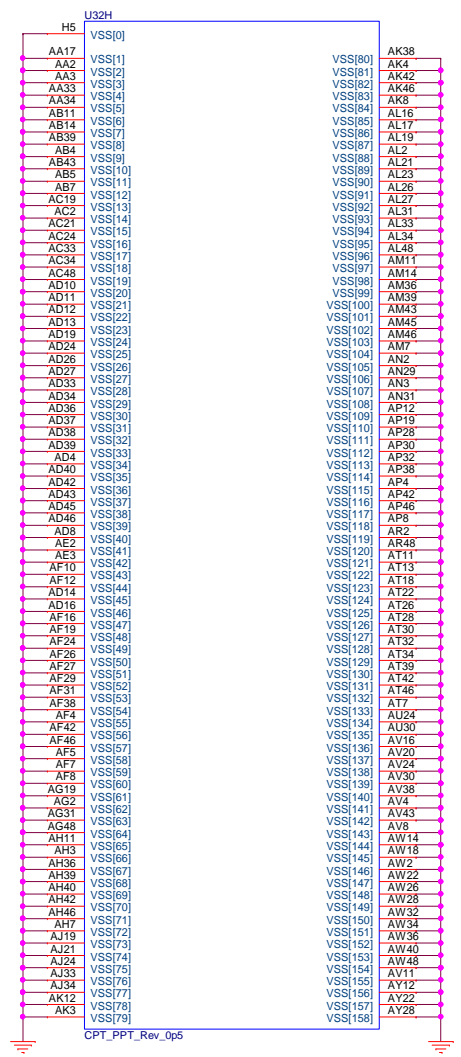
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Cougar Point/Panther Point (GND)


Cougar Point/Panther Point (GND)

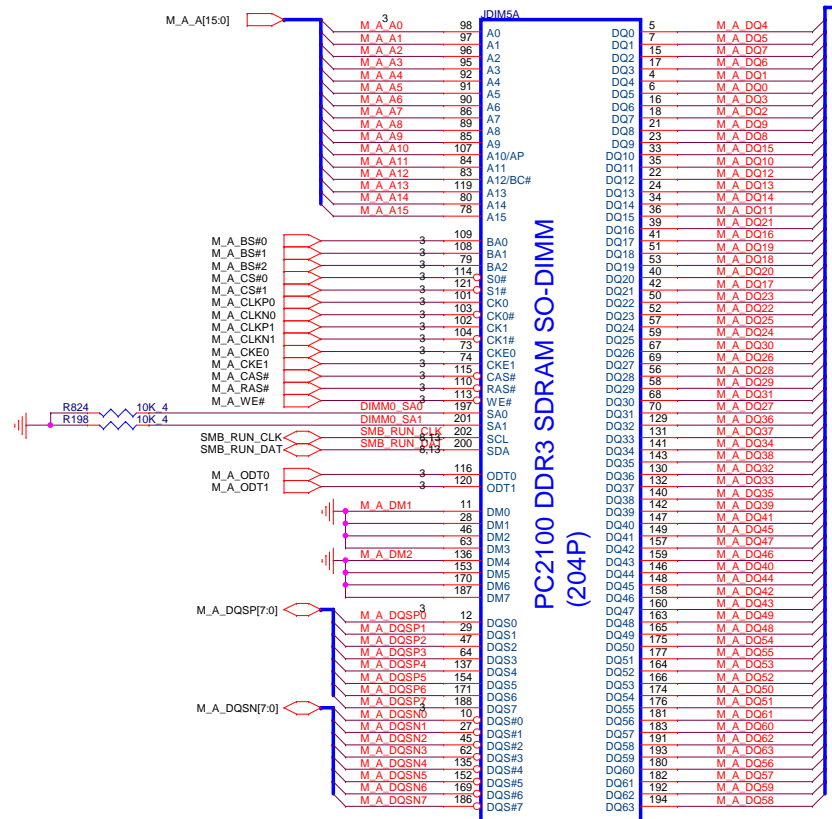


CPT_PPT_Rev_0p5



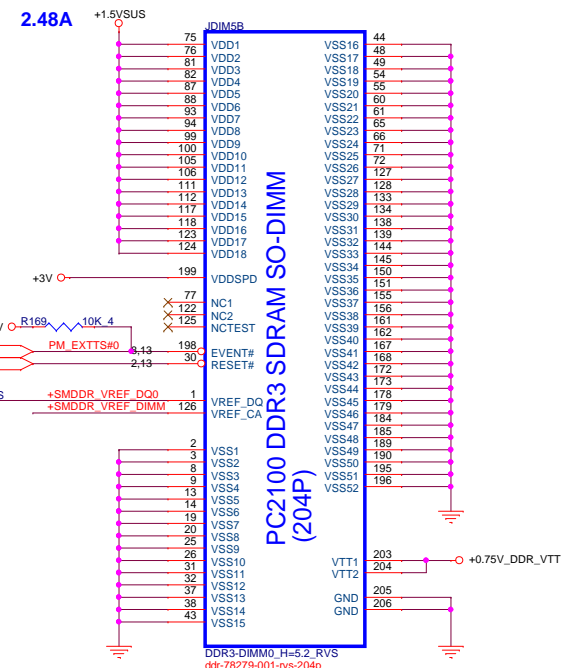
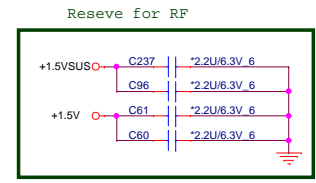
CPT_PPT_Rev_0p5

	PROJECT : R62 Quanta Computer Inc.		
	Size Custom	Document Number PCH 6/6 (GND)	Rev 1A
	Date: Monday, October 22, 2012		Sheet 11 of 43



PC2100 DDR3 SDRAM SO-DIMM (204P)

DDR3-DIMM0_H=5.2_RVS
 ddr-78279-001-rvs-204p
 DGMK4000278
 SOCKET DDR3 SODIMM(204P,H5.2,RVS)QBCON

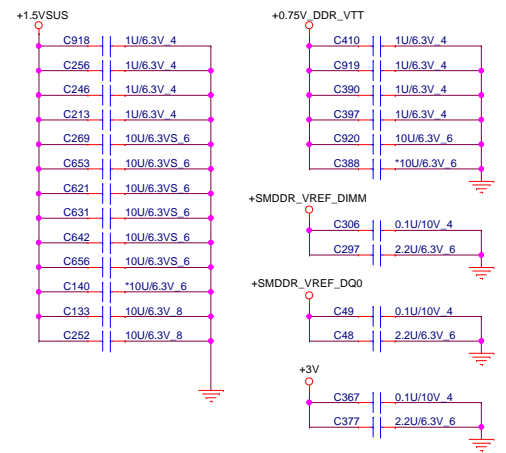


PC2100 DDR3 SDRAM SO-DIMM (204P)

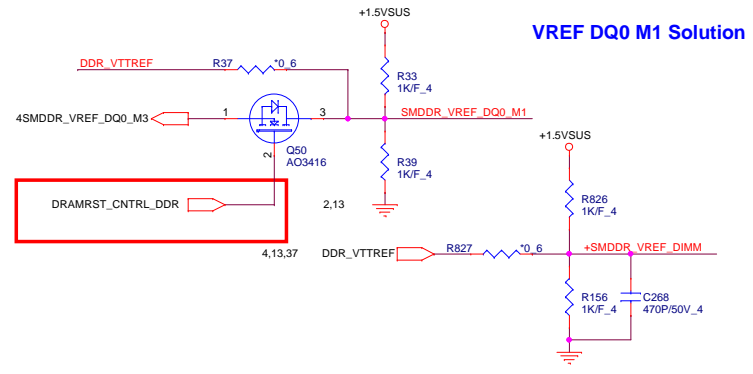
DDR3-DIMM0_H=5.2_RVS
 ddr-78279-001-rvs-204p
 DGMK4000278
 SOCKET DDR3 SODIMM(204P,H5.2,RVS)QBCON

- +1.5V 4,10,27,33
- +0.75V_DDR_VTT 3,37,39
- +1.5VSUS 2,4,13,37,43
- +3VPCU 5,7,25,30,31,33,34,35
- +3V 2,6,7,8,9,10,13,14,23,24,25,26,27,29,30,31,32,33,36,39,40,42

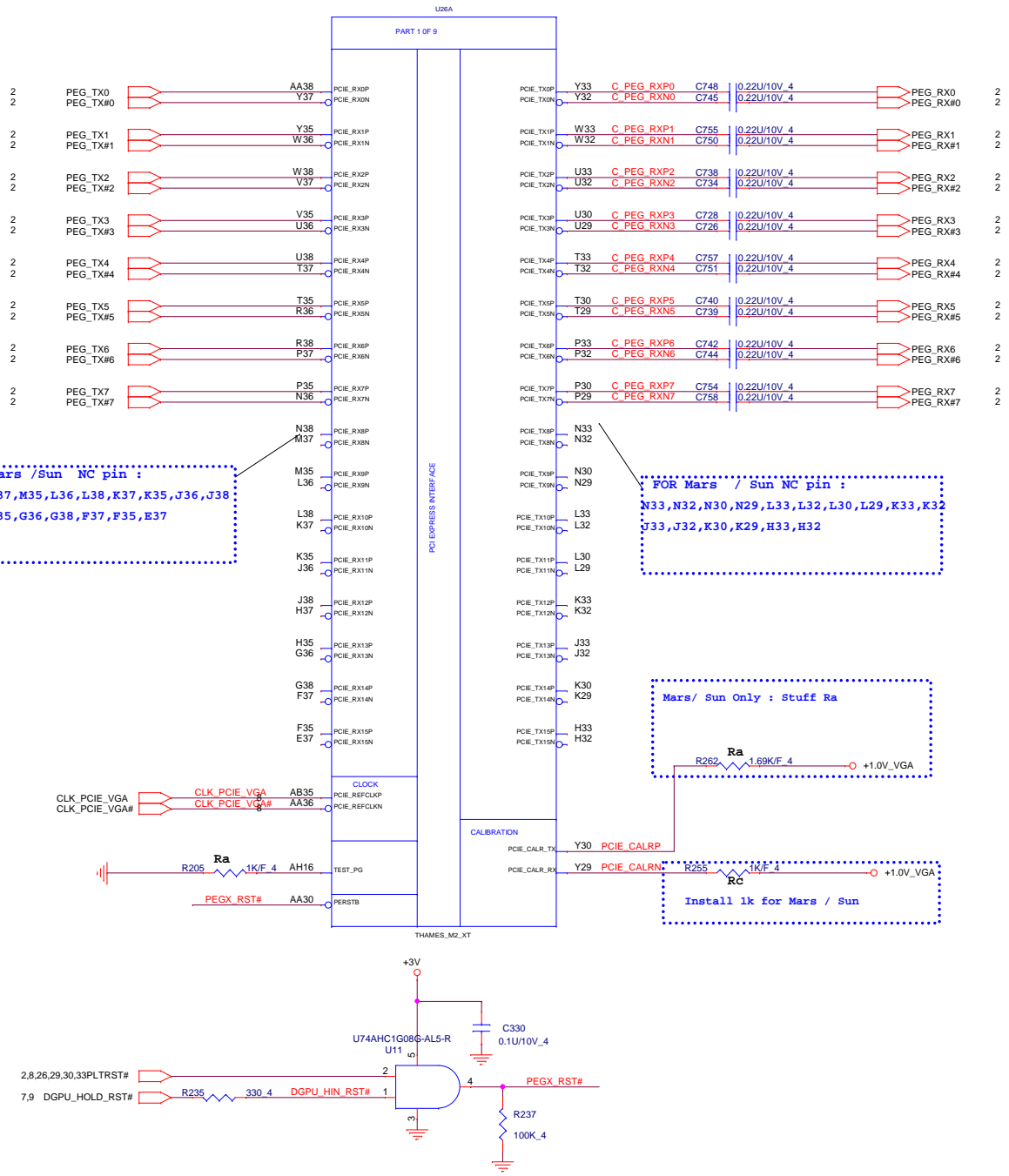
Place these Caps near So-Dimm0.



VREF DQ0 M1 Solution



	PROJECT : R62		Rev 1A
	Quanta Computer Inc.		
	Document Number	DDR3 DIMM0-RVS (5.2H)	
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For Mars /Sun NC pin :
 N38, M37, M35, L36, L38, K37, K35, J36, J38
 H37, H35, G36, G38, F37, F35, E37

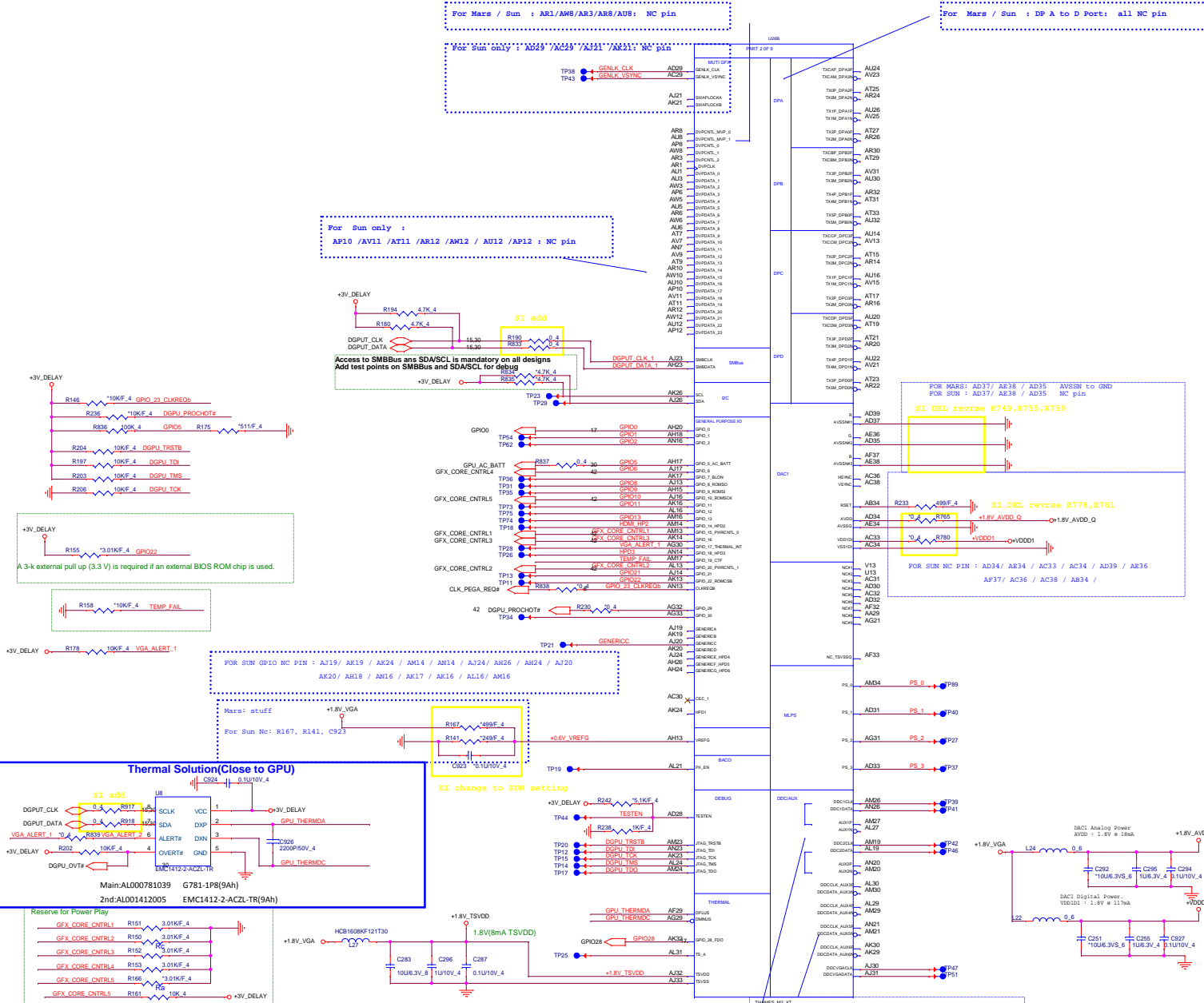
FOR Mars / Sun NC pin :
 N33, N32, N30, N29, L33, L32, L30, L29, K33, K32
 J33, J32, K30, K29, H33, H32

Mars/ Sun Only : Stuff Ra
 R262 1.69K/F 4 +1.0V_VGA

Install 1k for Mars / Sun
 R255 1K/F 4 +1.0V_VGA

2,6,7,8,9,10,14,21,23,24,25,26,27,29,30,31,32,33,36,39-40,42
 16,18,19,43 +1.0V_VGA

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	Quanta Computer Inc.		
	Size Custom	Document Number THAMES_PCIE_Interface	
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MLPS Implementation

- Connect GPIO_28 to 10K pulldown to enable MLPS
- If any of PS_0/1/2/3 is not used, leave "no connect"
- R_pu, R_pd and C must be properly populated per tables below
- Place MLPS circuit components as close to the ASIC as possible
- Total DC resistance of trace between PS pin and C should be less than 2 ohms
- Total DC resistance of trace between PS pin and C and ground should be less than 2 ohms
- Trace capacitance should be less than 100pF. Resistors should be of +/-1% tolerance

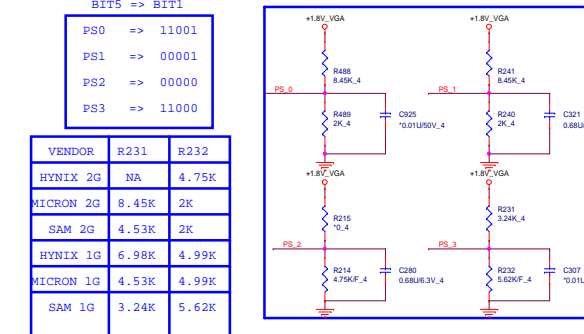
Capacitor Lookup Table

C (nF)	Bits(5,4)
680	00
82	01
10	10
NC	11

Resistor Divider Lookup Table

R_pu (Ohm)	R_pd (Ohm)	Bits(3,2,1)
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

Pin/Bit	Name	Description	Default	Legacy
PS_0[3:1]	romidg[2:0]	Memory aperture size or ROM type select: If bios_rom_en = 0, romidg[2:0] define memory aperture size. If bios_rom_en = 1, romidg[2:0] define ROM type	xxx	gpio_13, gpio_12, gpio_11
PS_0[4]	n/a	Reserved		1
PS_1[1]	bif_gen3_en_a	PCIe Gen3 capability: 1=Gen3 supported, 0=Gen3 not supported	x	gpio_2
PS_1[2]	bif_clk_pm_en	PCIe CLK PM capability: 1 = CLKREQ supported	x	gpio_8
PS_1[3]	n/a	Reserved		gpio_10
PS_1[4]	tx_pwr_enb	PCIe Tx power savings: 0=50% swing, 1=full swing	x	gpio_0
PS_1[5]	tx_deemph_en	PCIe Tx de-emphasis: 1=1x de-emphasis enabled	x	gpio_1
PS_2[1]	n/a	Reserved		n/a
PS_2[2]	n/a	Reserved		n/a
PS_2[3]	bios_rom_en	Enable external BIOS ROM: 1=External ROM connected	x	gpio_22
PS_2[5]	vga_ds	VGA disable: 1=Disable this GPU as the system's VGA controller	0	gpio_9
PS_2[6]	n/a	Reserved		n/a
PS_3[1]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[2]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[3]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[5]	aud_port_ep[2]	3-bit field indicating number of audio-capable display outputs	xxx	n/a
PS_3[6]	aud_port_ep[1]			
PS_3[5]	aud_port_ep[0]			



VENDOR	R231	R232
HYNIX 2G	NA	4.75K
MICRON 2G	8.45K	2K
SAM 2G	4.53K	2K
HYNIX 1G	6.98K	4.99K
MICRON 1G	4.53K	4.99K
SAM 1G	3.24K	5.62K

PS3 BIT3=>BIT1	ID	Memory Type	Configuration	PN	Channel Size
000	0	Hynix	H5TC4G63AFR-11C	256Mx16 *4 pcs	AKD5PW0TW08 IC SDRAM@6P/H5TC4G63AFR-11C
001	1	Micron	MT41J256M10HA-093GE	256Mx16 *4 pcs	AKD5PZ3T101 IC SDRAM@6P/MT41J256M10HA-093GE
010	2	Samsung	K4W4G1646B-HC1A	256Mx16 *4 pcs	AKD5PZD1501 IC SDRAM@6P/K4W4G1646B-HC1A
011	3	Hynix	H5TC2G63FR-11C	128Mx16 *4 pcs	AKD5MZD1W03 IC SDRAM@6P/H5TC2G63FR-11C
100	4	Micron	MT41J128M16JT-093CE	128Mx16 *4 pcs	AKD5MGT535 IC SDRAM@6P/K4W4G1646B-HC1A
101	5	Samsung	K4W2G1646E-BC1A	128Mx16 *4 pcs	AKD5MGT535 IC SDRAM@6P/K4W2G1646E-BC1A



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Quanta Computer Inc.

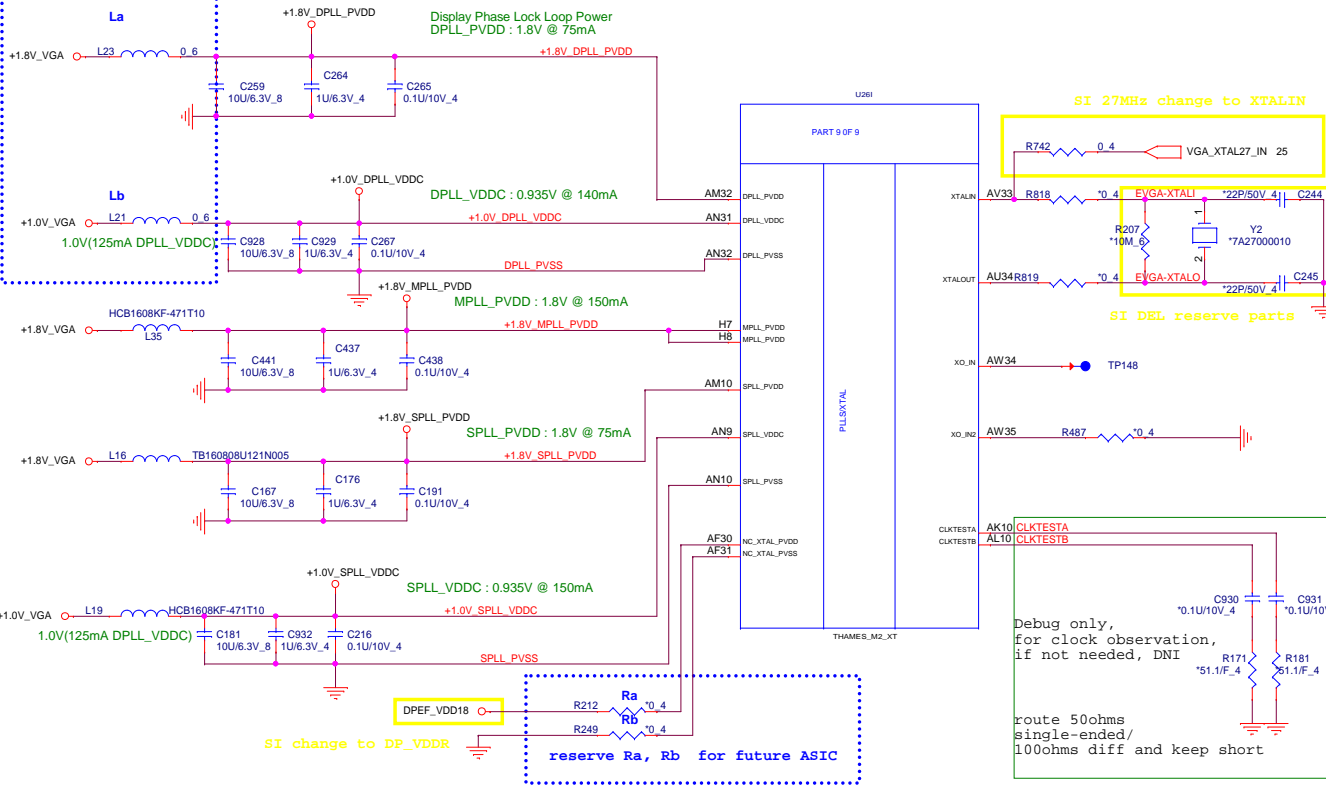
14.16.19.49: av_VGA
 16.18.19.25.49: av_VGA
 17.18 : +3V_DELAY

14.16.19.49: +1.8V_VGA
 16.18.19.25.49: +1.8V_VGA
 17.18 : +3V_DELAY

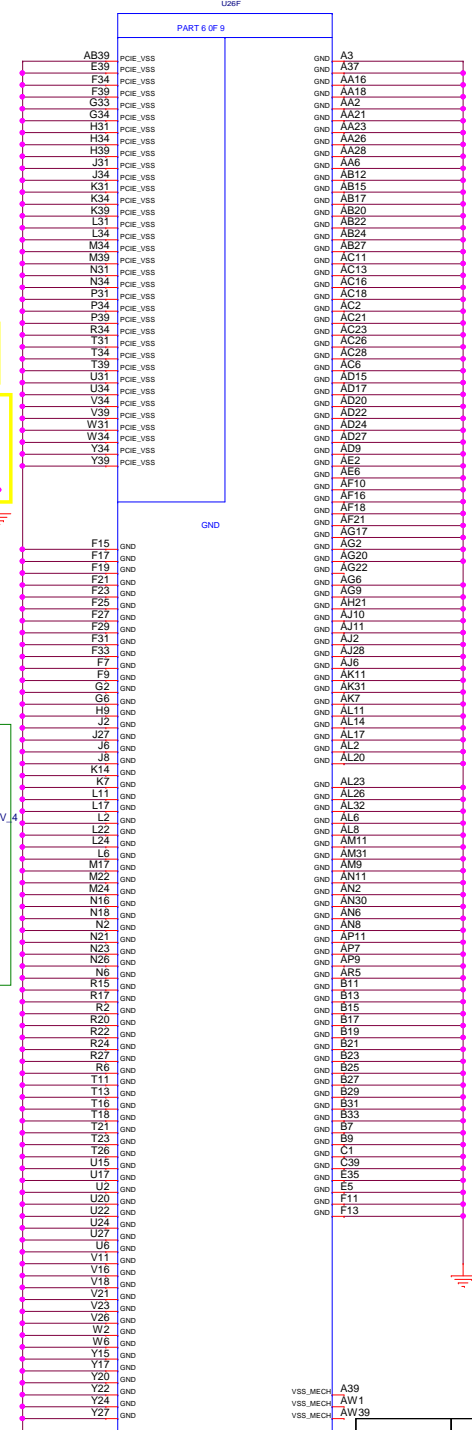
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Memory Type	
DDR3	27-MHz (± 30 ppm) crystal connected to XTALIN/XTALOUT, or 27-MHz (1.8 V) oscillator connected to XTALIN.
GDDR5	27-MHz (3.3 V) oscillator connected to XO_IN, and 100-MHz (3.3 V) oscillator connected to XO_IN2. (By default, this clock should not be spread since internal spreading is used.)

Fo Mars/ Sun
Change La, Lb
Bead to 0 ohm



14,18,19,43 +1.0V_VGA → +1.0V_VGA
15,18,19,25,42 +1.8V_VGA → +1.8V_VGA



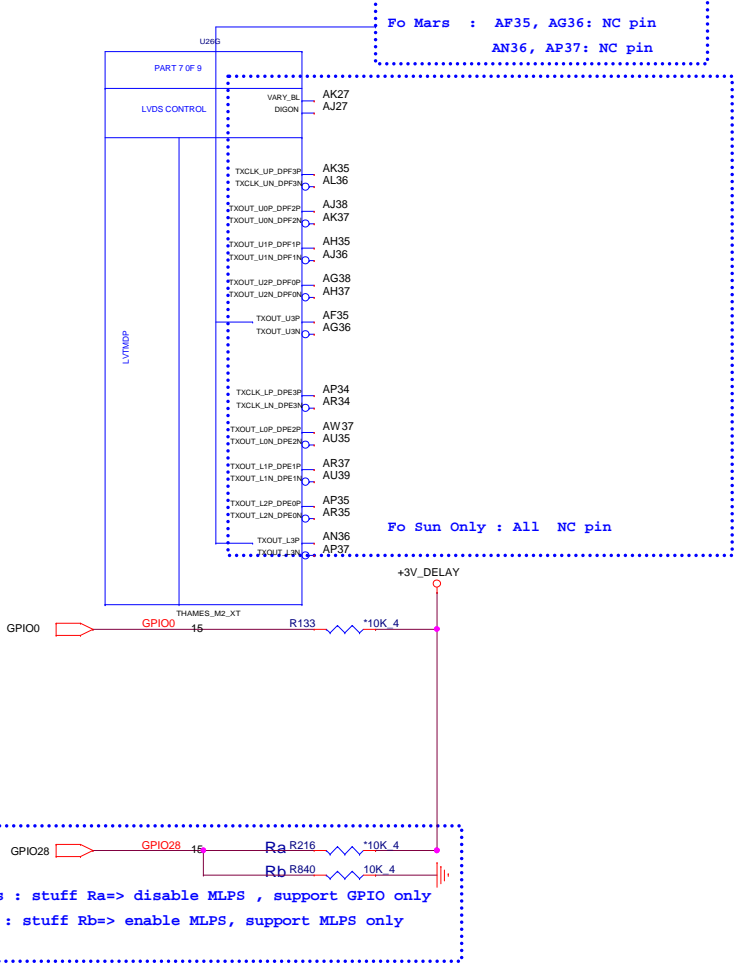
Debug only,
for clock observation,
if not needed, DNI

route 50ohms
single-ended/
100ohms diff and keep short



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Quanta Computer Inc.

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CONFIGURATION STRAPS -- SEE EACH DATABOOK FOR STRAP DETAILS
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

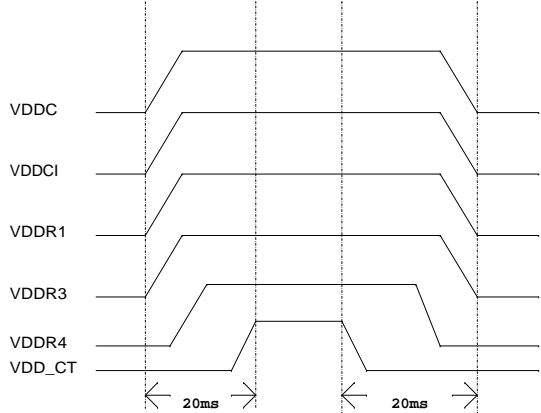
STRAPS	MLPS	GPIO PIN	DESCRIPTION OF DEFAULT SETTINGS	Default Setting
MLPS_DISABLE	NA	GPIO_28_FDO	Enable MLPS, NA for Thames/Whistler/Seymour 0: Enable MLPS, disable GPIO PINSTRAP 1: Disable MLPS, enable GPIO PINSTRAP	X
TX_PWRS_ENB	PS_1[4]	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	X
TX_DEEMPH_EN	PS_1[5]	GPIO1	PCIe Transmitter De-emphasis Enable 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled	X
BIF_GEN3_EN_A	PS_1[1]	GPIO2	PCIe Gen3 Enable (NOTE: RESERVED for Thames/Whistler/Seymour) 0: GEN3 not supported at power-on 1: GEN3 supported at power-on	1
BIF_VGA DIS	PS_2[4]	GPIO9	VGA Control 0: VGA controller capacity enabled 1: VGA controller capacity disabled (for multi-GPU)	0
ROMIDCFG[2:0]	PS_0[3..1]	GPIO[13:11]	Serial ROM type or Memory Aperture Size Select If GPIO22 = 0, defines memory aperture size If GPIO22 = 1, defines ROM type 100 - 512Kbit M25P05A (ST) 101 - 1Mbit M25P05A (ST) 101 - 2Mbit M25P20 (ST) 101 - 4Mbit M25P40 (ST) 101 - 8Mbit M25P80 (ST) 100 - 512Kbit Pm25LV512 (Chingis) 101 - 1Mbit Pm25LV010 (Chingis)	XXX
BIOS_ROM_EN	PS_2[3]	GPIO22	Enable external BIOS ROM device 0: Disabled 1: Enabled	X
AUD[1] AUD[0]	NA NA	HSYNC VSYNC	00 - No audio function 01 - Audio for DP only 10 - Audio for DP and HDMI if dongle is detected 11 - Audio for both DP and HDMI HDMI must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature.	XX
CEC_DIS	PS_0[4]	GENLK_VSYNC	Enable CEC function. Reserved for Thames/Whistler/Seymour 0: Disabled 1: Enabled	X
RESERVED RESERVED RESERVED RESERVED	PS_1[3] PS_1[2] NA NA	GENLK_CLK GPIO8 GPIO21 GENERICC	NOTE: ALLOW FOR PULLUP PADS FOR THE RESERVED STRAPS BUT DO NOT INSTALL RESISTOR IF THESE GPIOs ARE USED, THEY MUST KEEP LOW AND NOT CONFLICT DURING RESET Reserved Reserved Reserved Reserved (for Thames/Whistler/Seymour)	0 0 0 0
AUD_PORT_CONN_PINSTRAP[2] AUD_PORT_CONN_PINSTRAP[1] AUD_PORT_CONN_PINSTRAP[0]	PS_3[5] PS_3[4] PS_0[5]	NA NA NA	STRAPS TO INDICATE THE NUMBER OF AUDIO CAPABLE DISPLAY OUTPUTS 111 = 0 usable endpoints 110 = 1 usable endpoints 101 = 2 usable endpoints 100 = 3 usable endpoints 011 = 4 usable endpoints 010 = 5 usable endpoints 001 = 6 usable endpoints 000 = all endpoints are usable	XXX

Memory Aperture size

GPIO9	BIOSROM	GPIO13	ROMIDCFG2	GPIO12	ROMIDCFG1	GPIO11	ROMIDCFG0
0	128M	0	0	0	0	0	0
0	256M	0	0	1	0	1	0
0	64M	0	0	1	1	0	1
0	32M	0	0	1	1	1	1
0	512M	1	1	0	0	0	0
0	1G	1	1	0	0	1	1
0	2G	1	1	1	1	0	0
0	4G	1	1	1	1	1	1

It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.

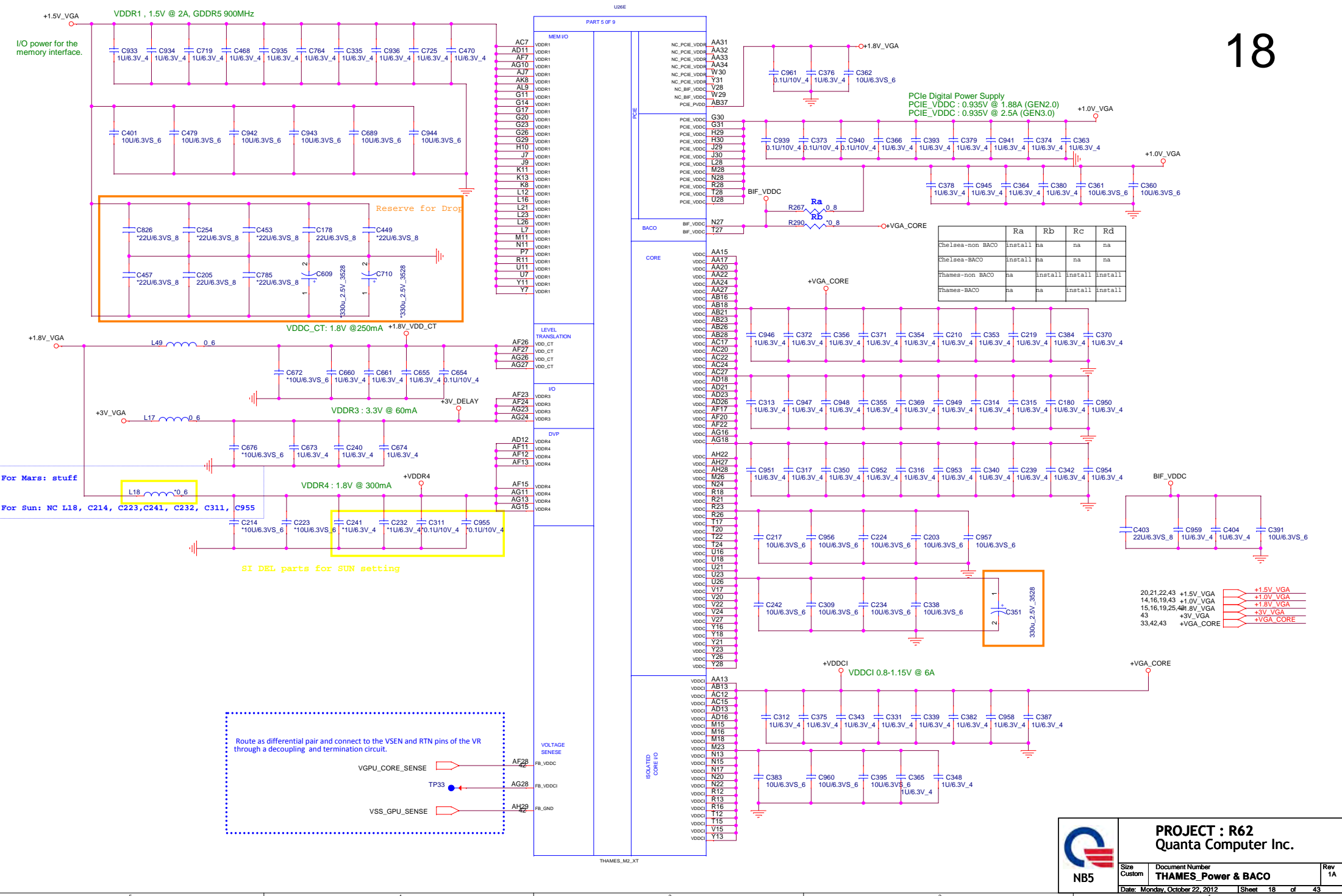
Power Up/Down Sequence



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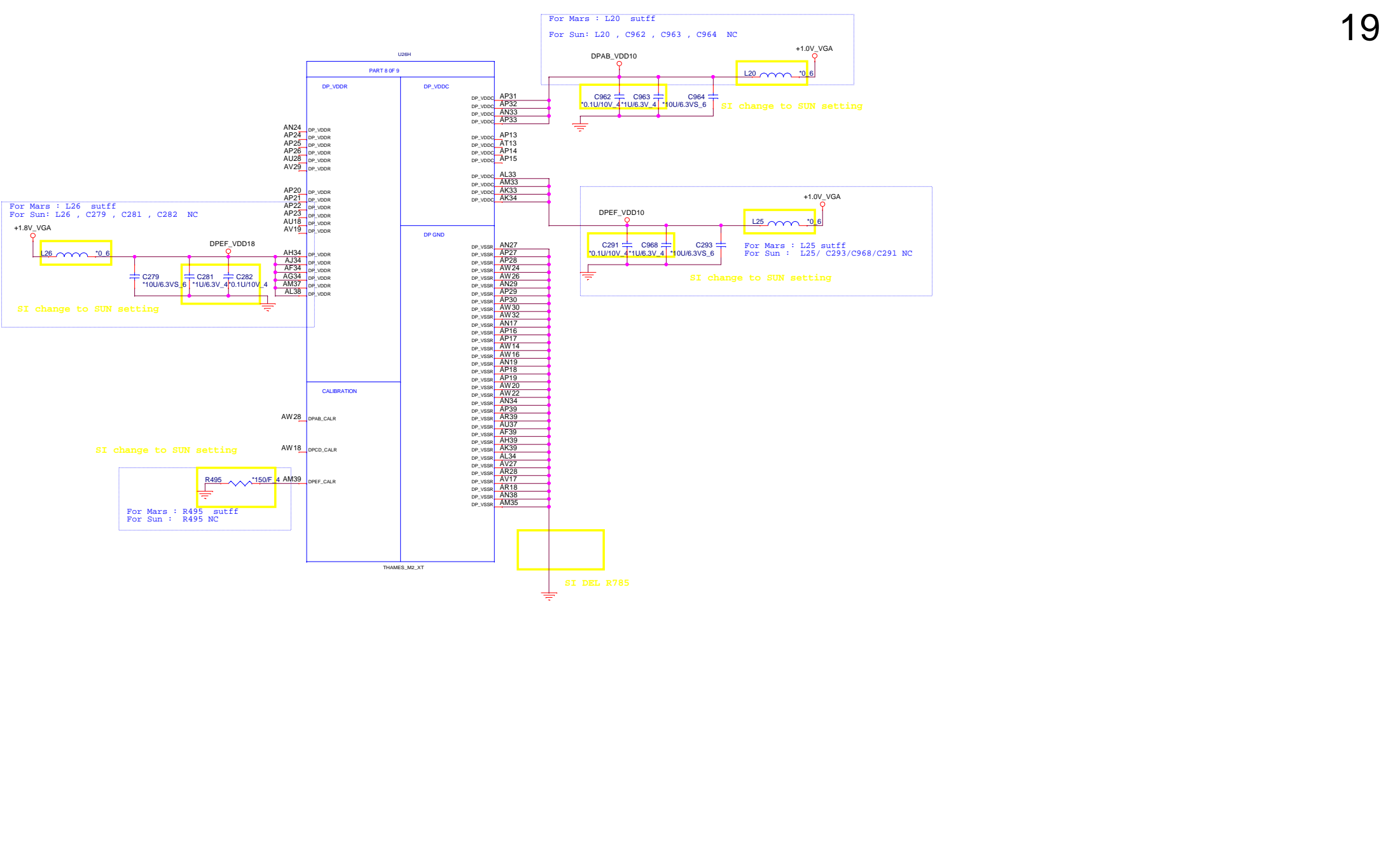
NBS

Size Custom Document Number THAMES_LVDS / STRAP Rev 1A
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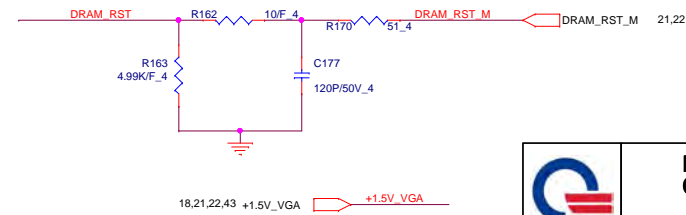
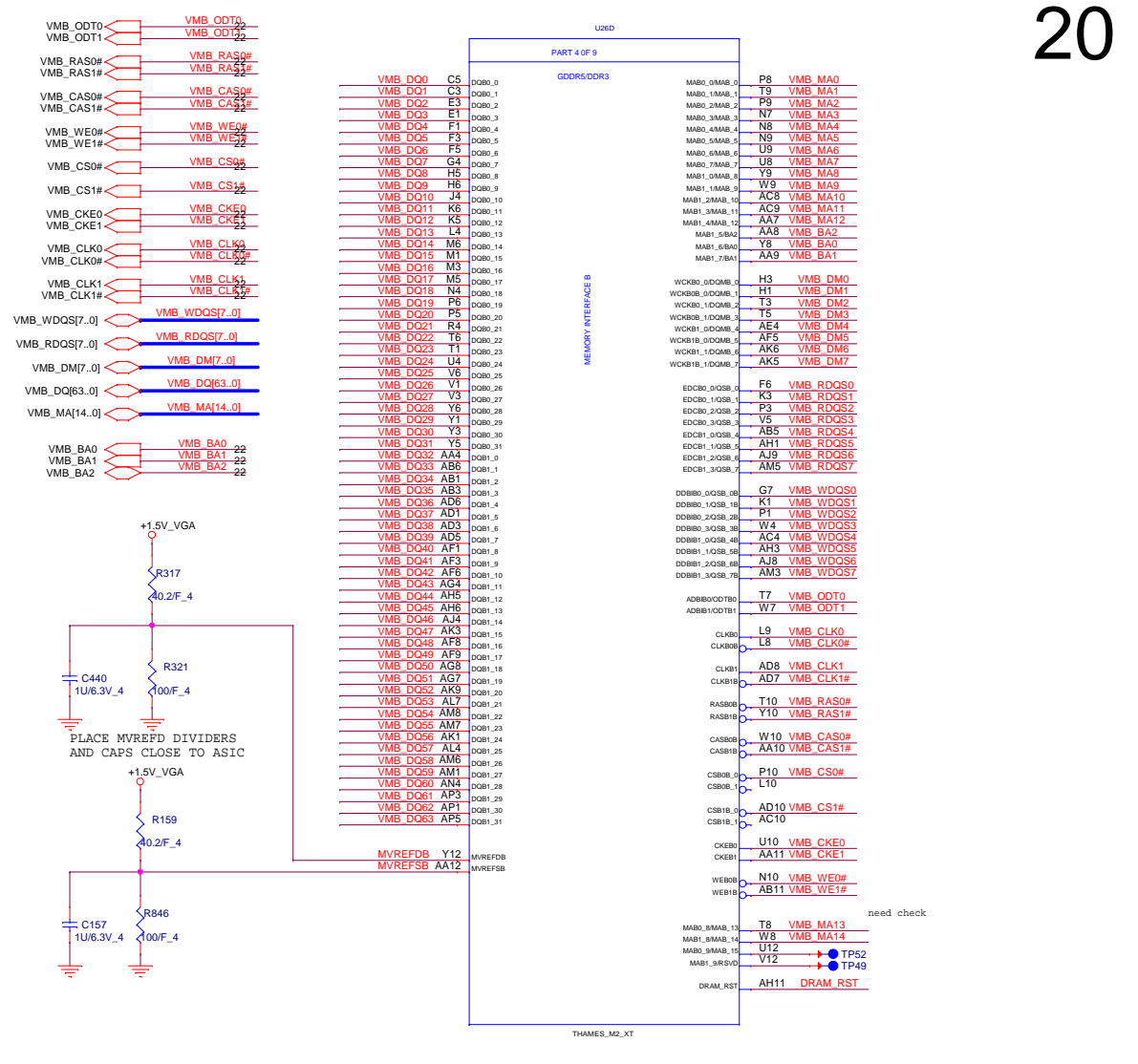
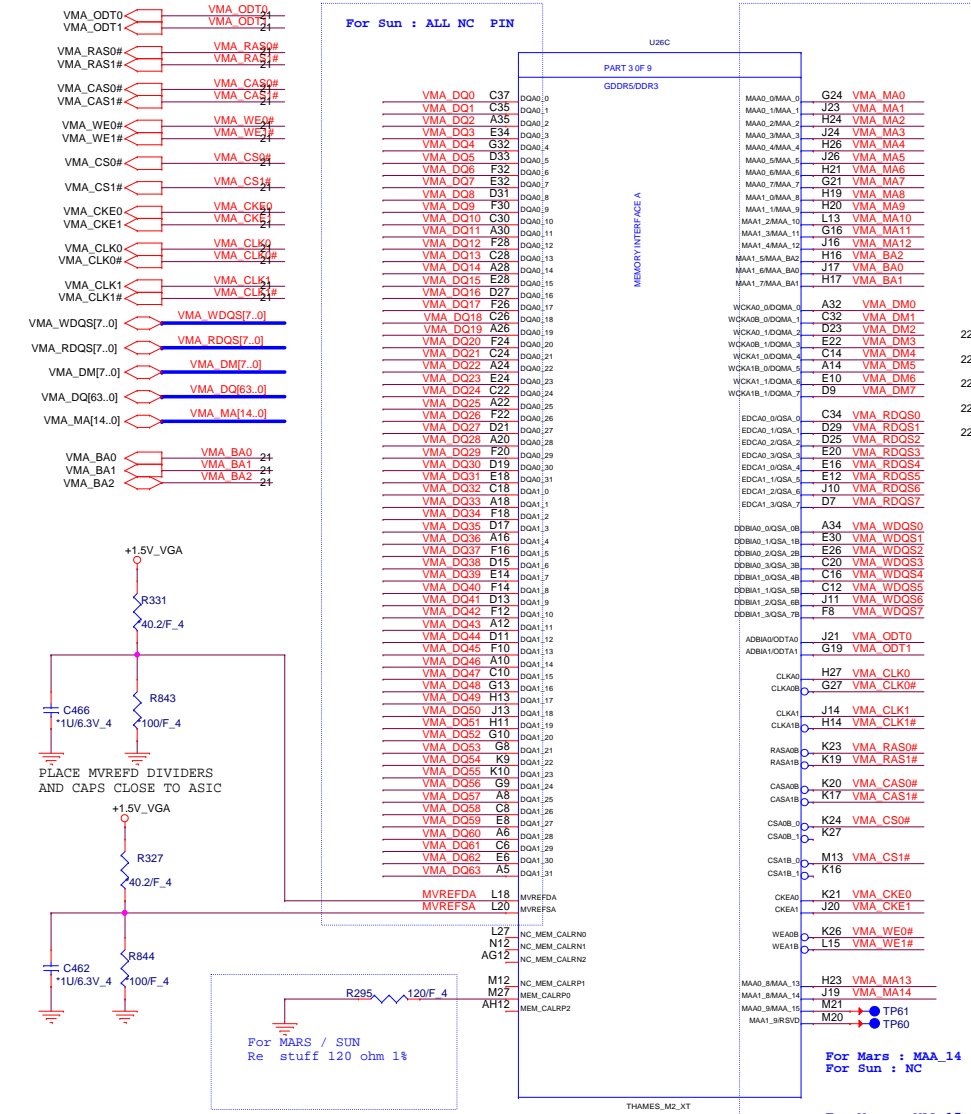
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Quanta Computer Inc.

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14,16,18,43 +1.0V_VGA
 15,16,18,25,40+1.8V_VGA

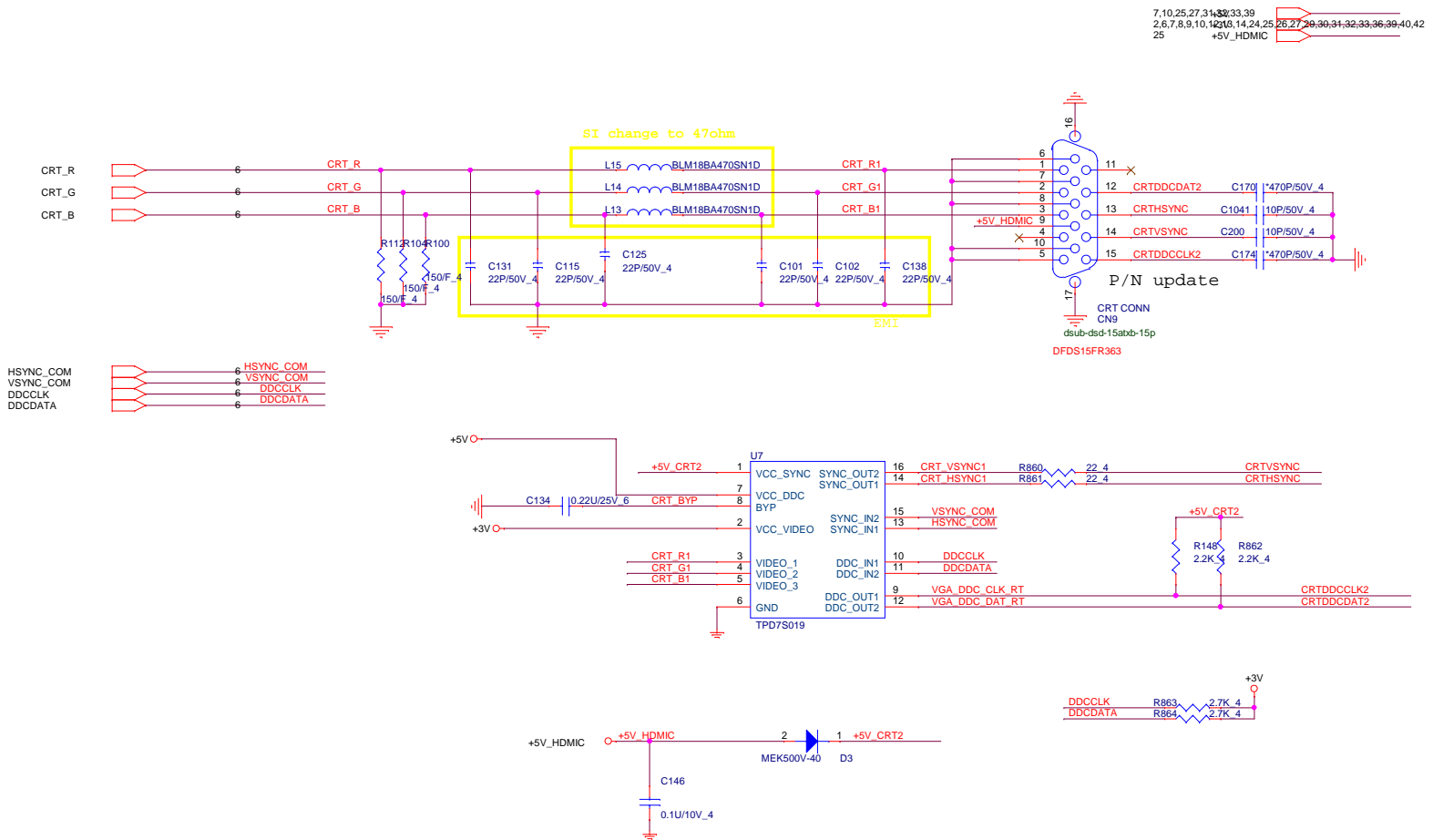
	PROJECT : R62		Rev 1A
	Quanta Computer Inc.		
	Size Custom	Document Number THAMES_DP Powers	
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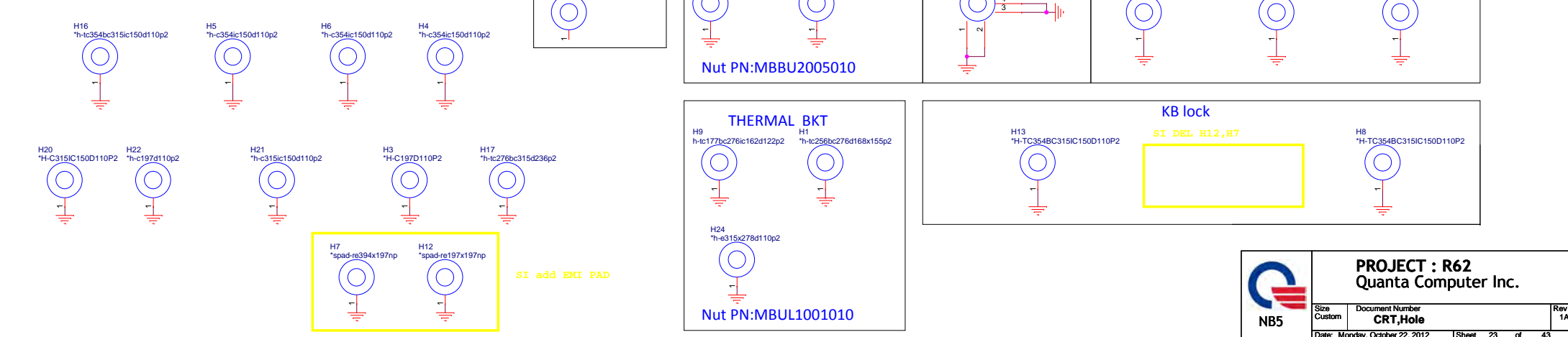
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Quanta Computer Inc.

NBS

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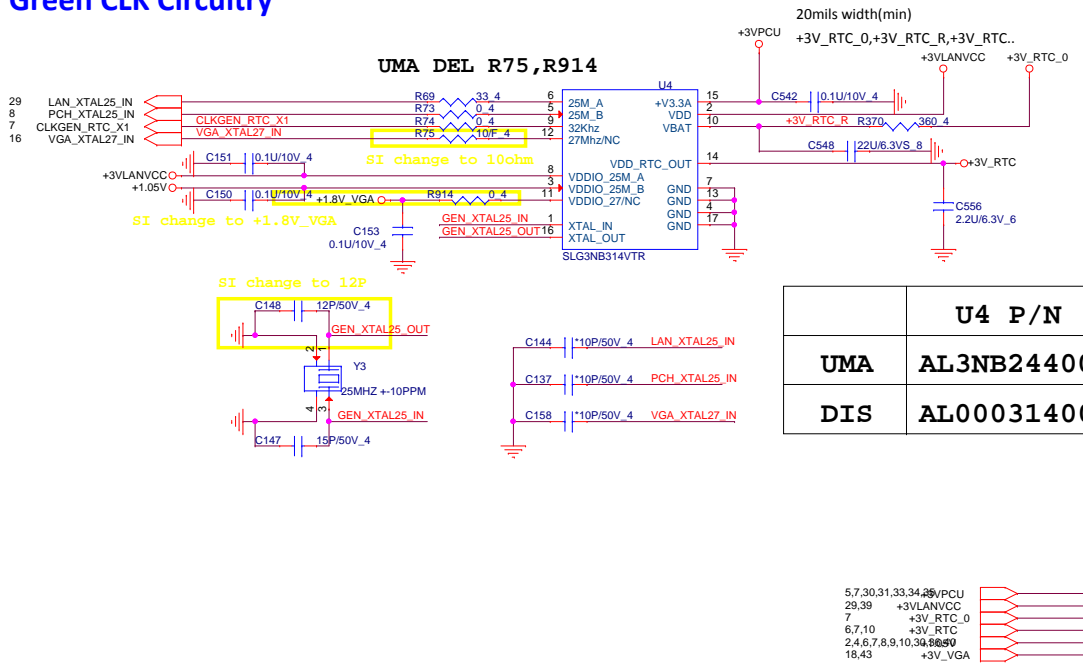


HOLE

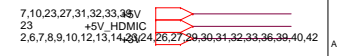
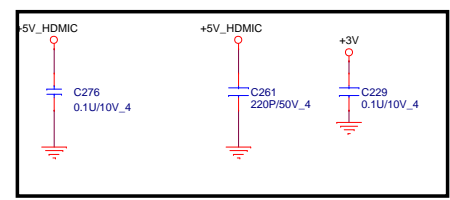


	PROJECT : R62 Quanta Computer Inc.		
	Size Custom	Document Number CRT,Hole	Rev 1A
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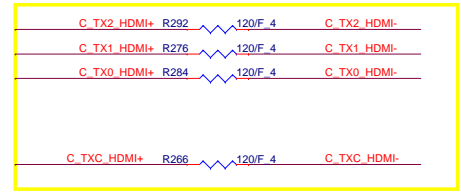
Green CLK Circuitry



EMI request

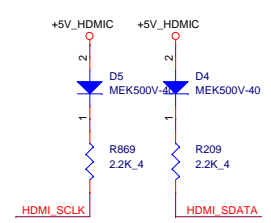
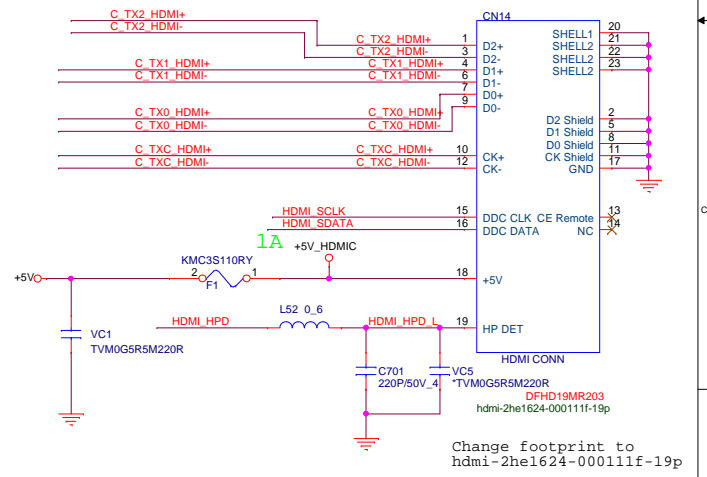
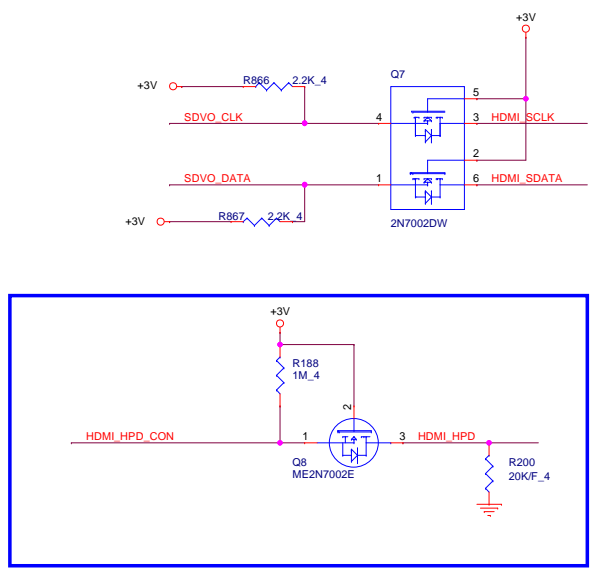
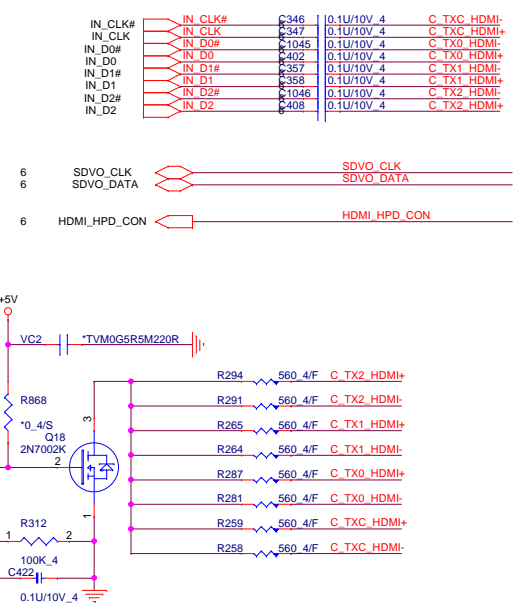


EMI request



close to HDMI conn

Close to HDMI Connector



	PROJECT : R62		Rev 1A
	Quanta Computer Inc.		
	Size Custom	Document Number HDMI CONN	
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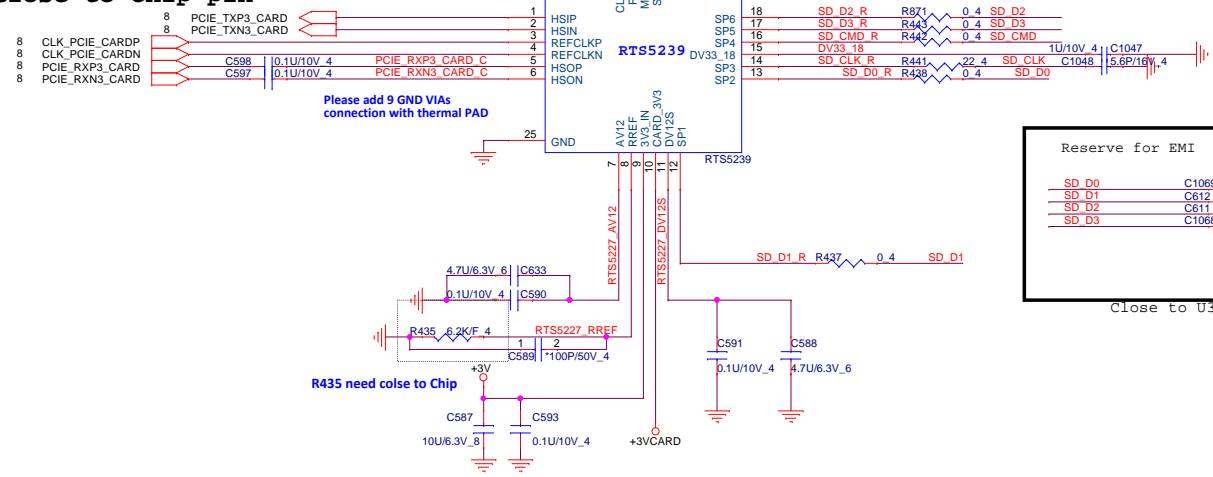
8 CLK_PCIE_REQ2# CLK_PCIE_REQ2# R446 0.4S CLK_PCIE_REQ2#_R

SP1	SD D1	
SP2	SD D0	MS D1
SP3	SD CLK	MS D0
SP4	SD CMD	MS D2
SP5	SD D3	MS D3
SP6	SD D2	MS CLK
SP7	SD_WP	MS_BS

Share Pin

Close to chip pin

Close to chip pin



Please add 9 GND VIAs connection with thermal PAD

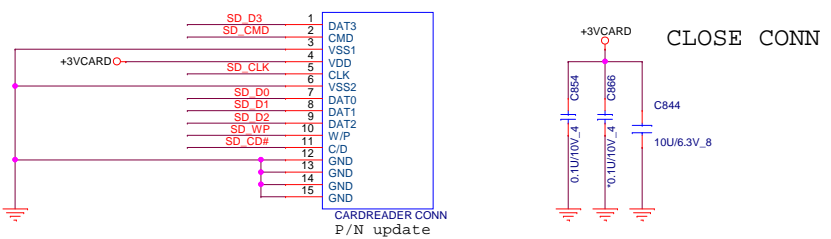
R435 need close to Chip

Reserve for EMI

SD D0	C1069	5.6P/16V_4
SD D1	C612	5.6P/16V_4
SD D2	C611	5.6P/16V_4
SD D3	C1068	5.6P/16V_4

Close to U38

SD / MMC
CARD READER



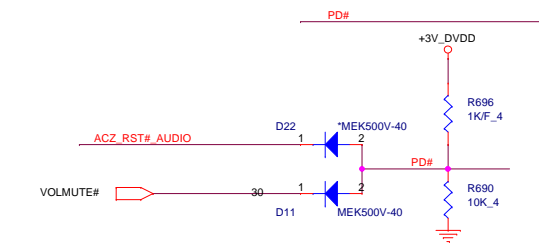
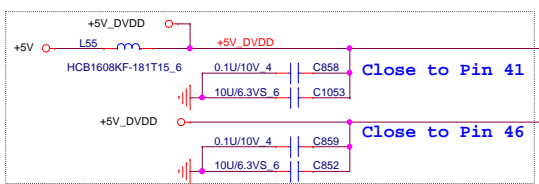
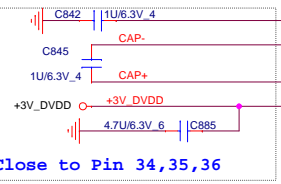
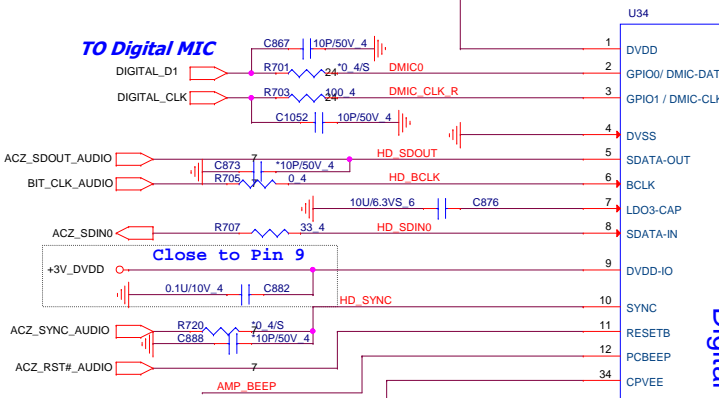
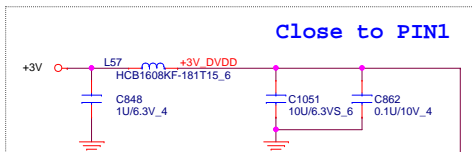
Reserve for EMI

SD D0	C1049	5.6P/16V_4
SD D1	C886	5.6P/16V_4
SD D2	C610	5.6P/16V_4
SD D3	C1050	5.6P/16V_4
SD CLK	C1100	5.6P/16V_4

Close to CN8

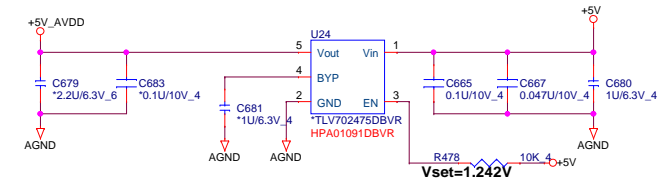
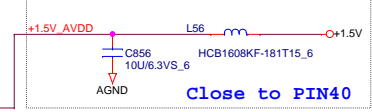
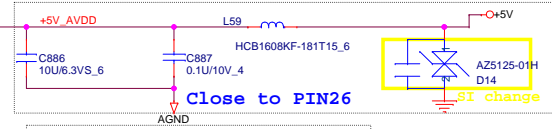
2,6,7,8,9,10,12,13,14,23,24,25,27,29,30,31,32,33,36,39,40,42

	PROJECT : R62 Quanta Computer Inc.		Rev 1A	
	Size Custom	Document Number RTS5229 & CR SOCKET		Date: Monday, October 22, 2012 Sheet 26 of 43



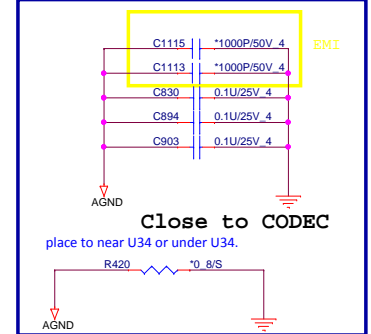
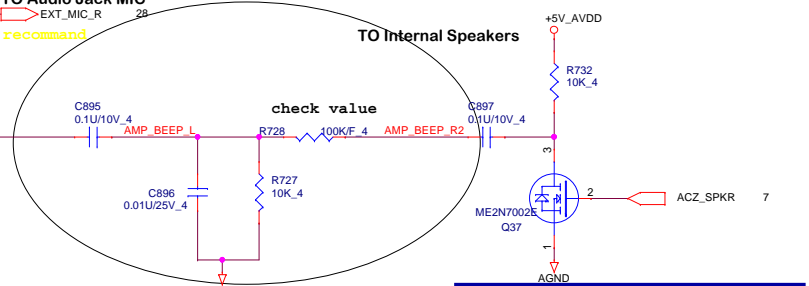
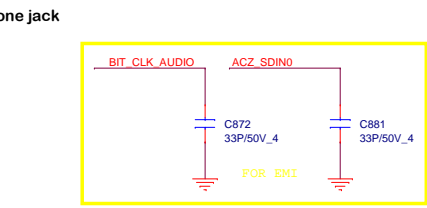
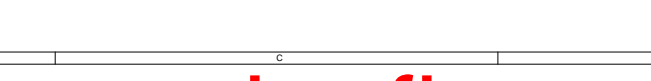
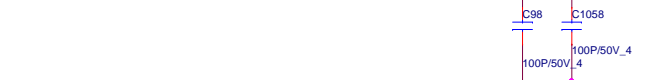
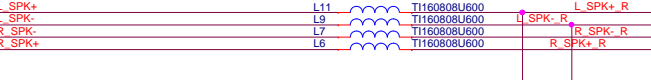
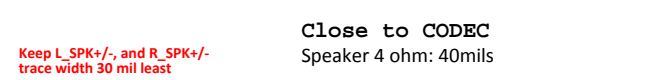
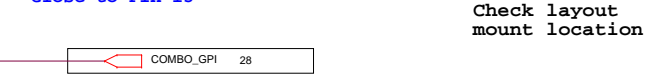
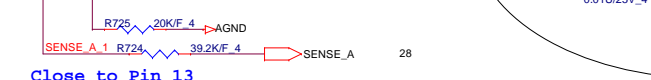
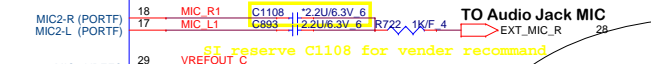
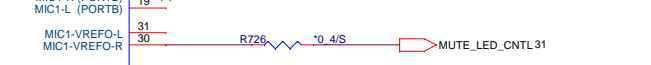
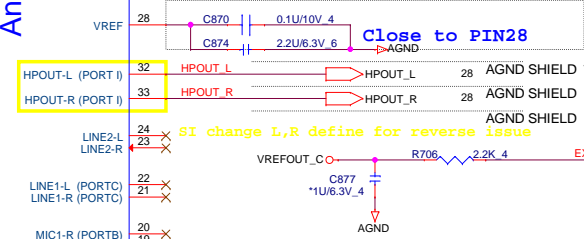
7,10,23,25,31,32,33,39 +5V
2,6,7,8,9,10,12,13,14,23,24,25,29,30,31,32,33,36,39,40,42
4,10,12,33 +1.5V

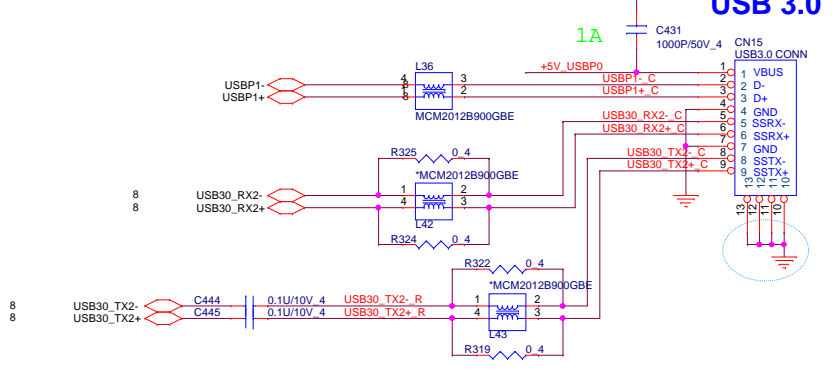
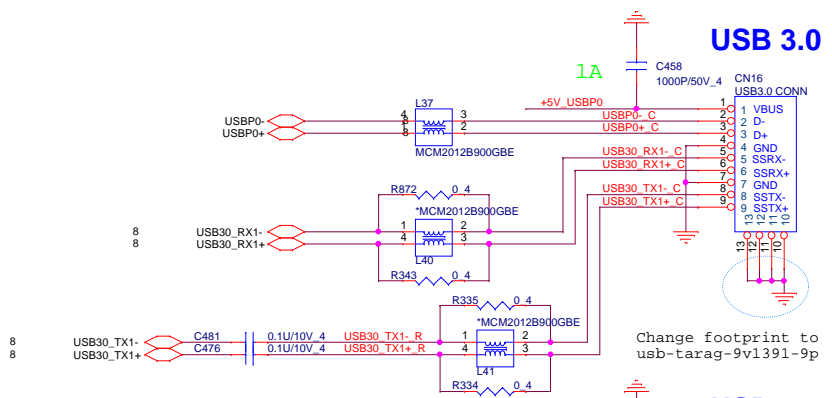
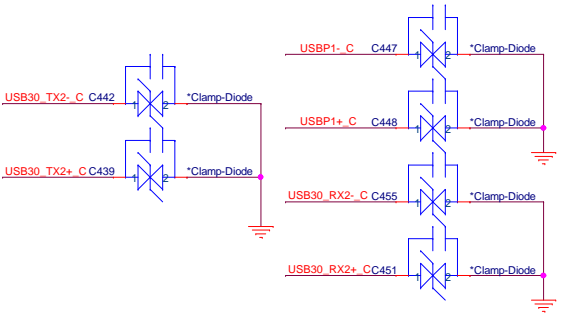
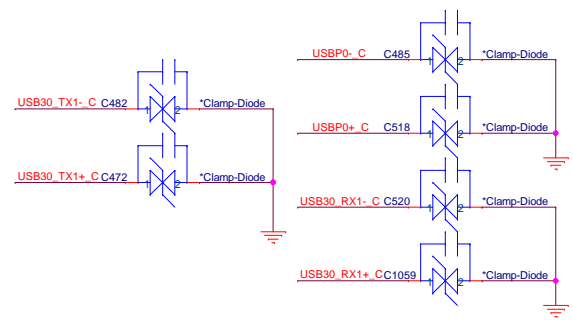
>40mils trace



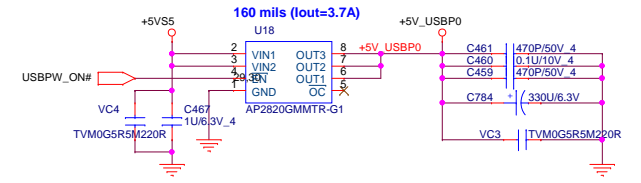
Analog

Digital

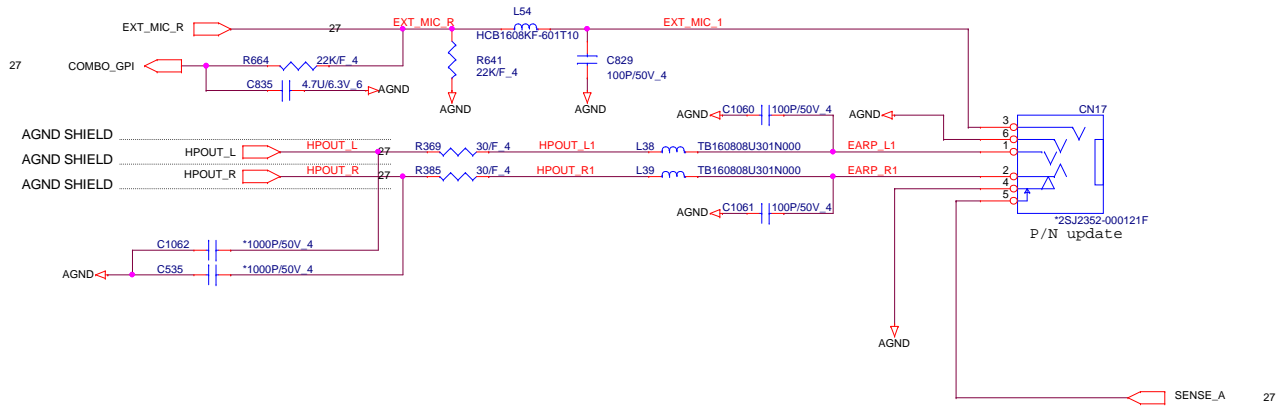




USB3.0 X 2/USB2.0 COMBO

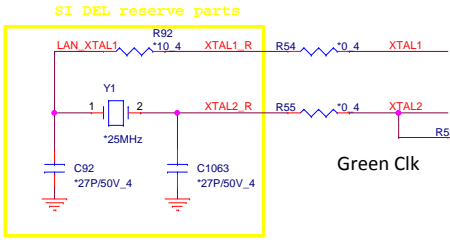


COMBO JACK



10,29,33,35,36,37,38,39,40,41,42,39
 2,6,7,8,9,10,12,13,14,23,24,25,26,27,29,30,31,32,33,36,39,40,42
 25,29,39 +3VLANVCC

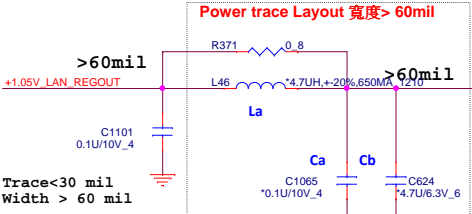
	PROJECT : R62		Rev 1A
	Quanta Computer Inc.		
	Size Custom Document Number USB/BT/Audio Jack	Date: Monday, October 22, 2012 Sheet 28 of 43	



Green Clk

For GbE
* Place Cc,Cd,Ce,Cf close to each VDD10 pin-- 3, 22, 8, 30

For 10/100 NA Ce,Cf
* Place Ce, Cf close to each VDD10 pin-- 8, 30 only,



For GbE
Stuff La, Ca, Cb

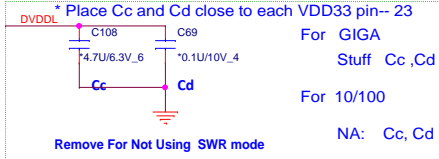
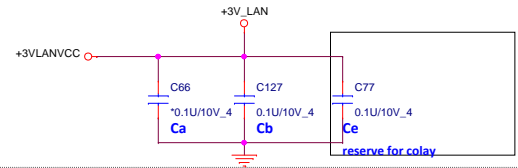
For 10/100
NA: La, Ca, Cb

For GbE
* Place Cf close to each VDD10 pin-- 22 (reserve)

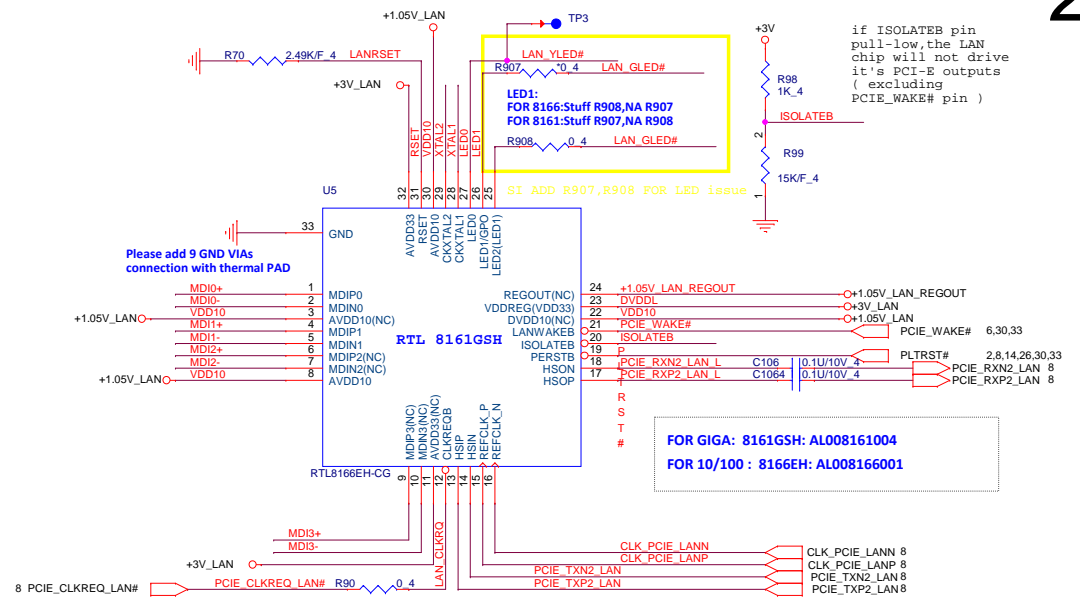
For 10/100
* Place Cg close to each VDD10 pin-- 30 (reserve)

For 10/100
* Stuff Ca and Ce only, close to each VDD33 pin-- 23, 32

For GIGA
* Stuff Ca and Cb only, close to each VDD33 pin-- 11, 32

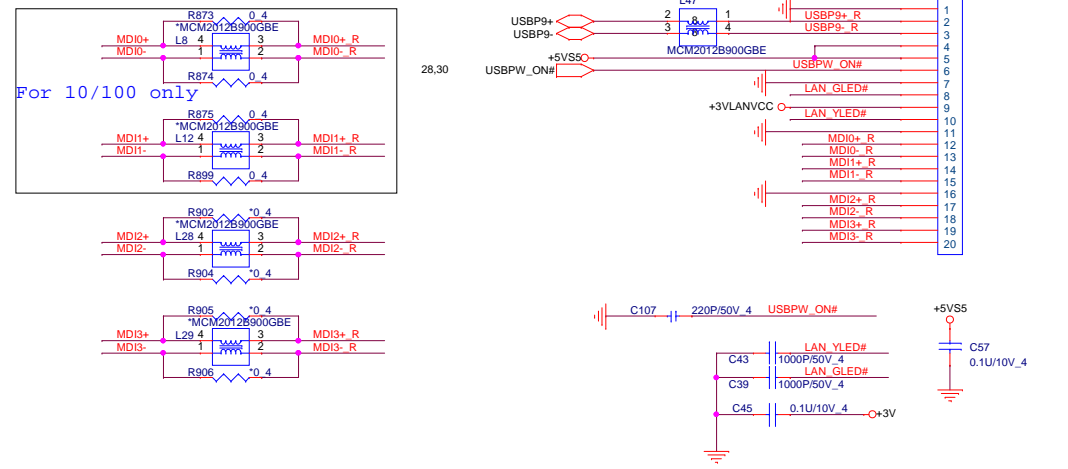


2,6,7,8,9,10,12,13,14,23,24,25,26,27,30,31,32,33,36,39,40,42,25,39 +3VLANVCC



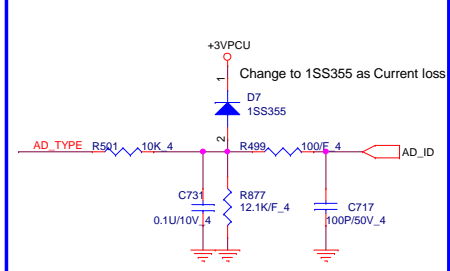
if ISOLATEB pin pull-low, the LAN chip will not drive it's PCI-E outputs (excluding PCIE_WAKE# pin)

Right SIDE USBX1 and LAN CONN

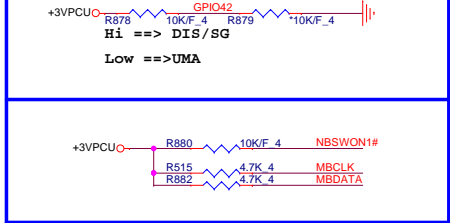


	PROJECT : R62 Quanta Computer Inc.		
	Size Custom	Document Number RTL 8105E/RJ45	Rev 1A
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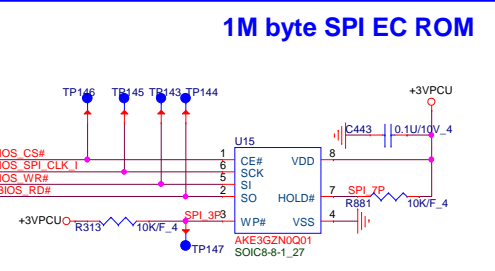
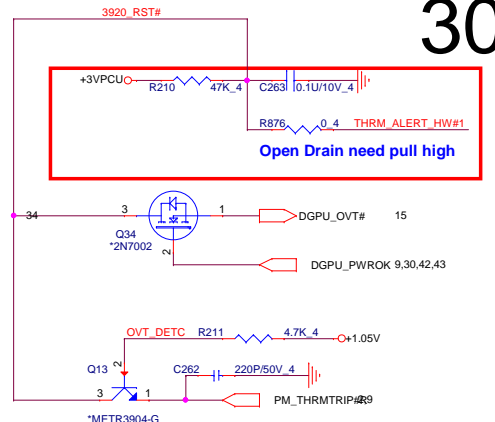
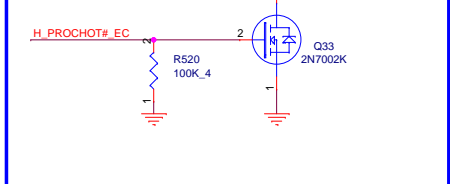
adapter Type check



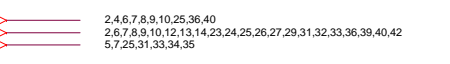
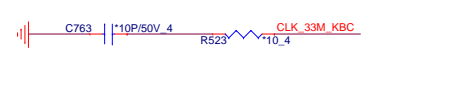
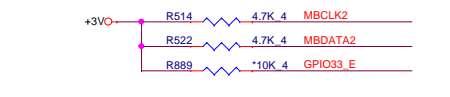
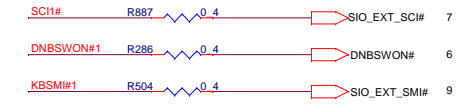
adapter select for EC



PROCHOT control

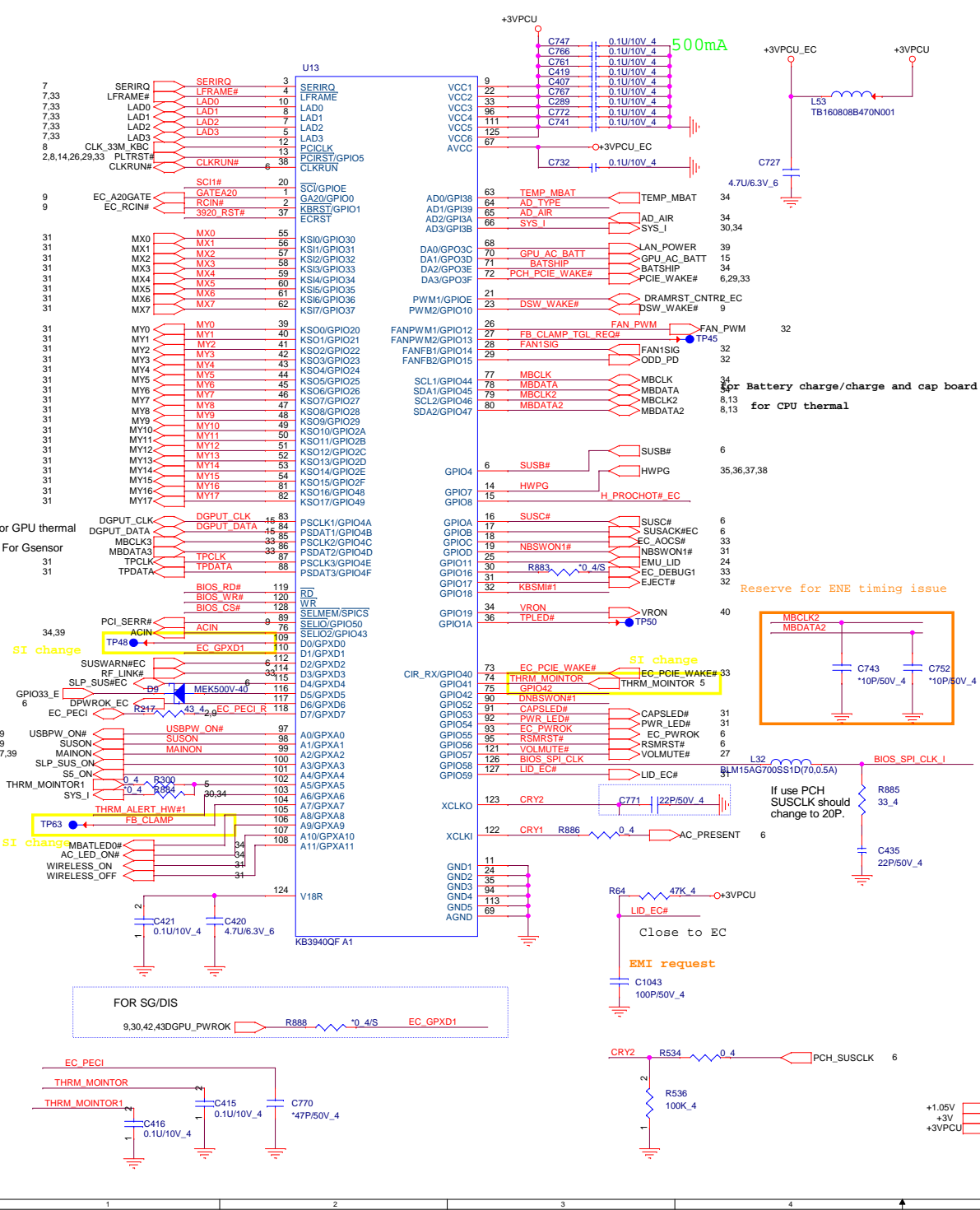


Vender	Size	P/N
EON	1MB	AKE3GN0Q01 (EN25Q80A-100HIP)
GigaDevice	1MB	AKE3GGN0Q00 (GD25Q80BSIGR)
AMIC	1MB	AKE3GZP0801 (A25L080M-F)
Socket		DFHS08FS023

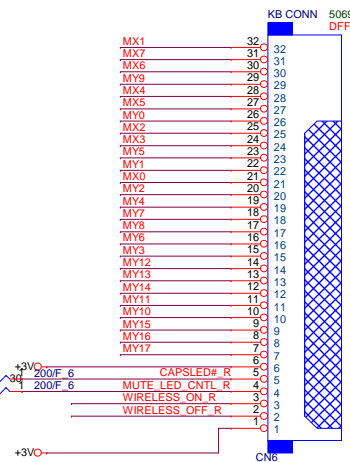
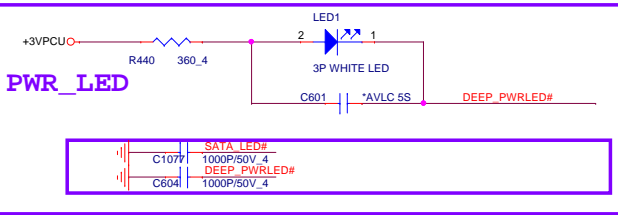
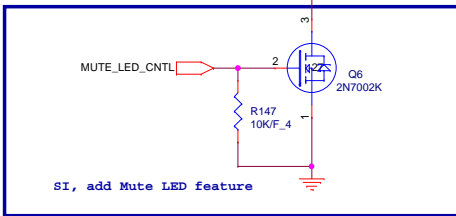
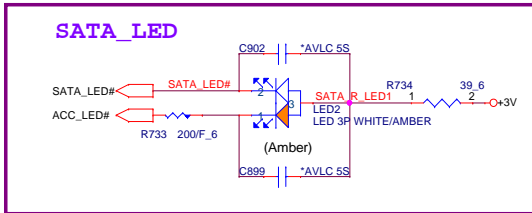
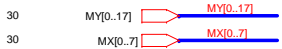


PROJECT : R62
Quanta Computer Inc.

Size Custom	Document Number EC (KB3940 A1)ROM	Rev 1A
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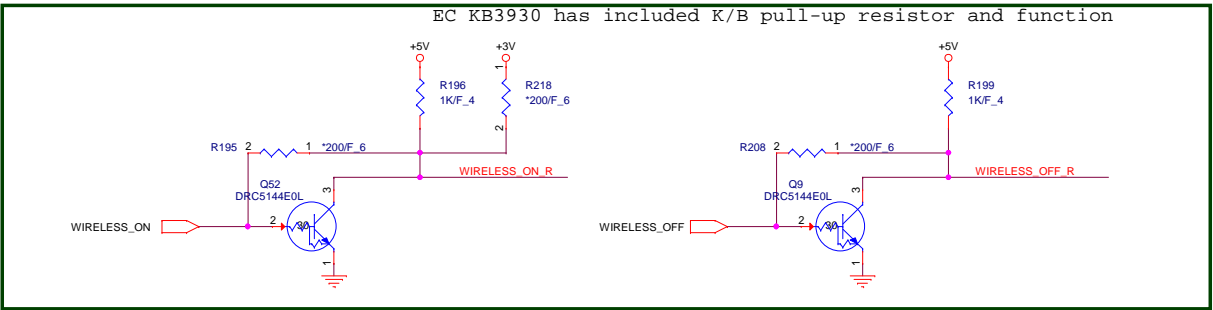
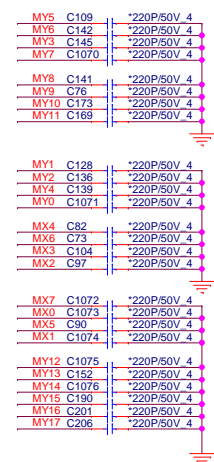
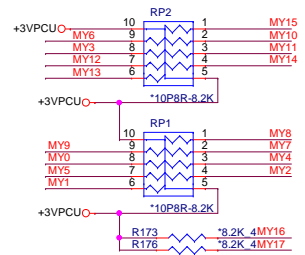


KEYBOARD Con.

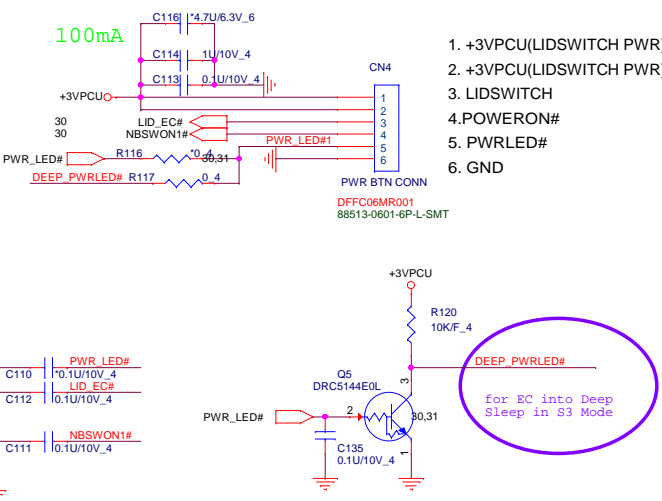


P/N update

KEYBOARD PULL-UP



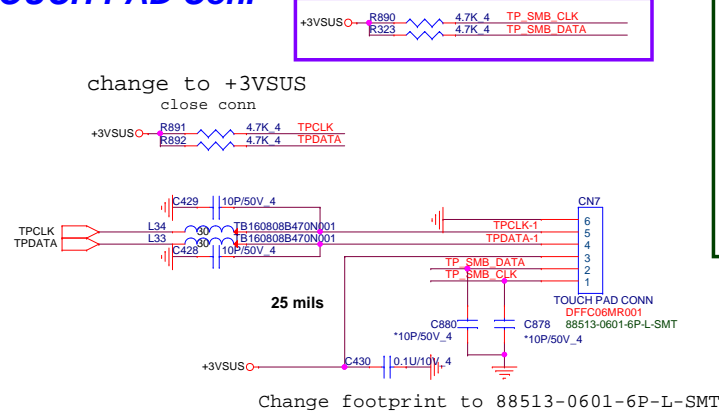
POWER BOTTON CONNECT



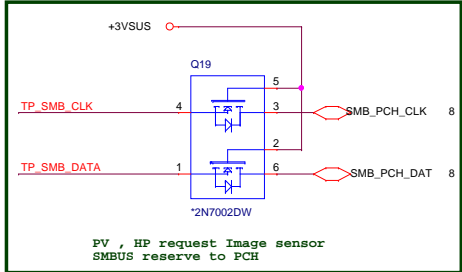
1. +3VPCU(LIDSWITCH PWR)
2. +3VPCU(LIDSWITCH PWR)
3. LIDSWITCH
4. POWERON#
5. PWRLED#
6. GND

for EC into Deep Sleep in S3 Mode

TOUCH PAD Con.



Change footprint to 88513-0601-6P-L-SMT

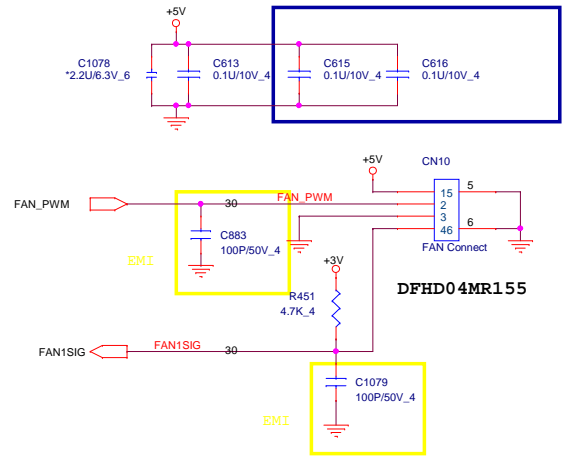


PV , HP request Image sensor SMBUS reserve to PCH

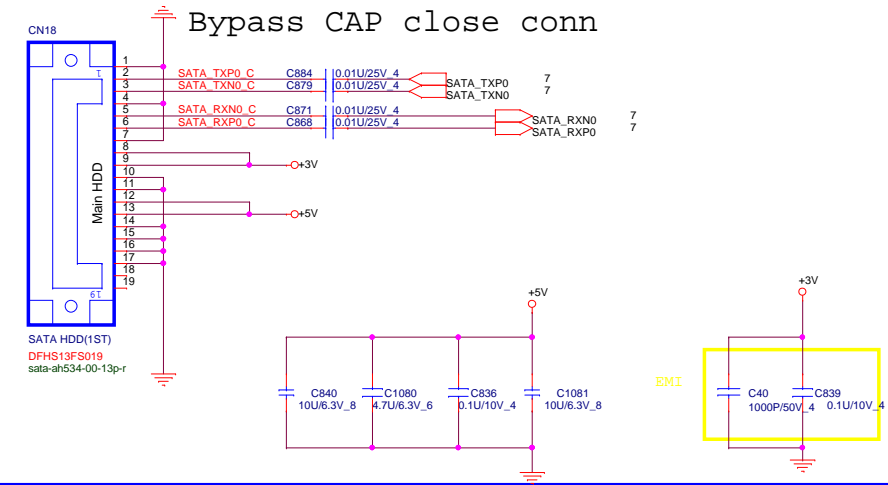


PROJECT : R62		
Quanta Computer Inc.		
Size Custom	Document Number	Rev 1A
LED/KB/SW/TP		
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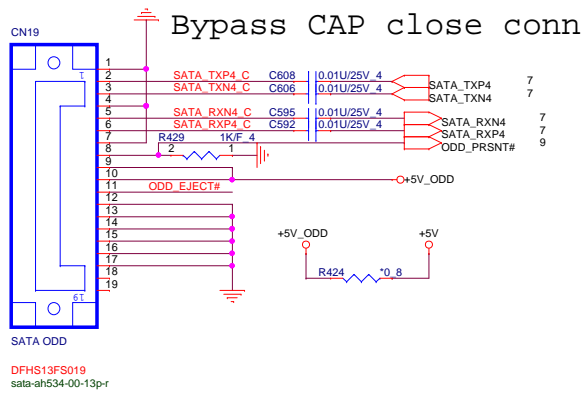
CPU FAN



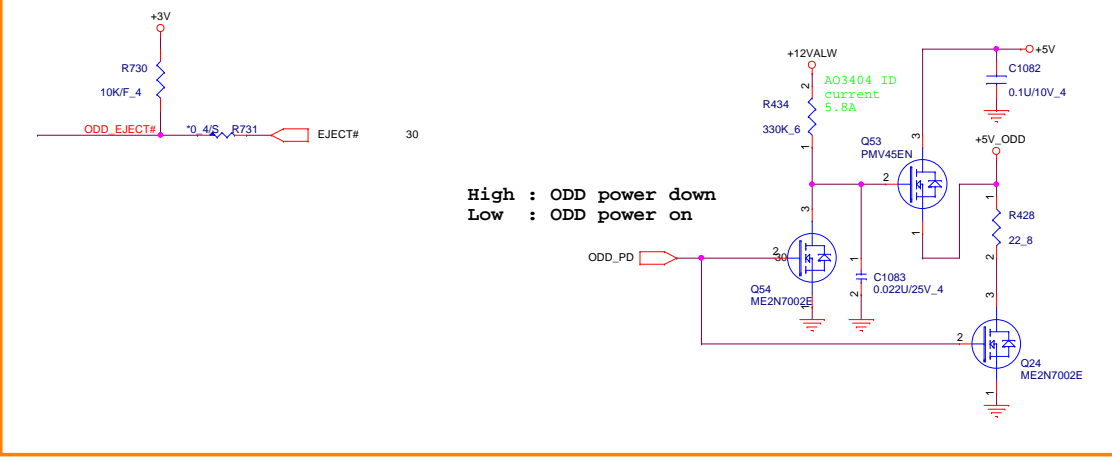
SATA HDD CONNECTOR



SATA ODD CONNECTOR



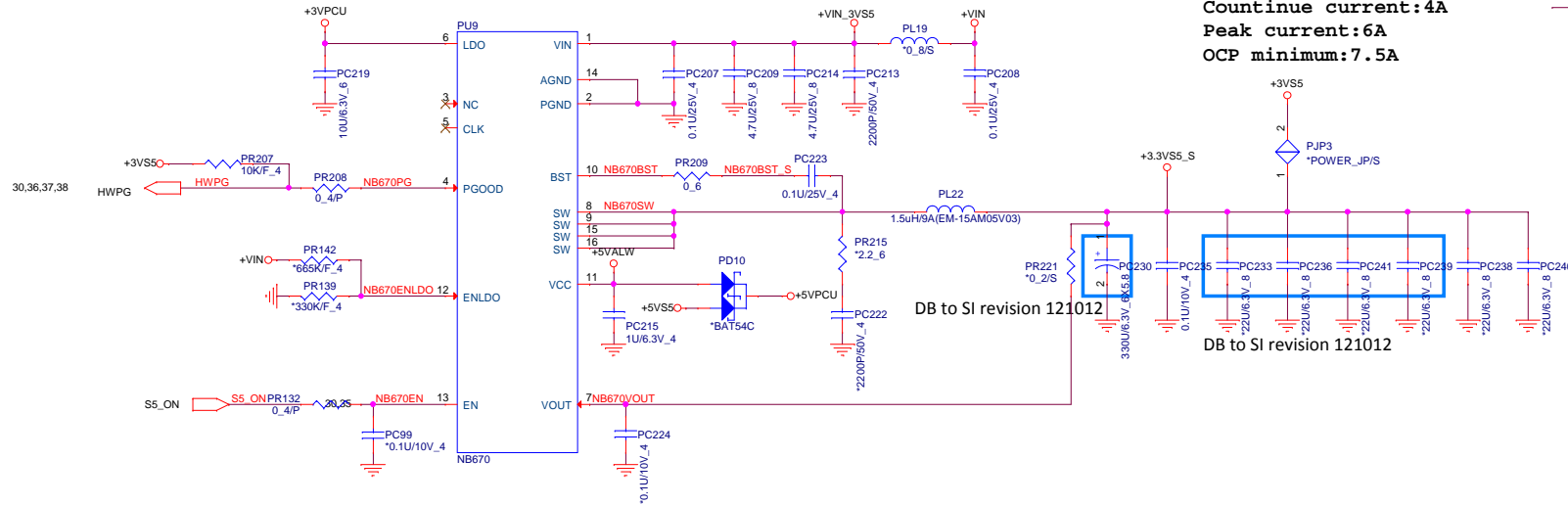
follow INTEL DG change eject PU to +3V.



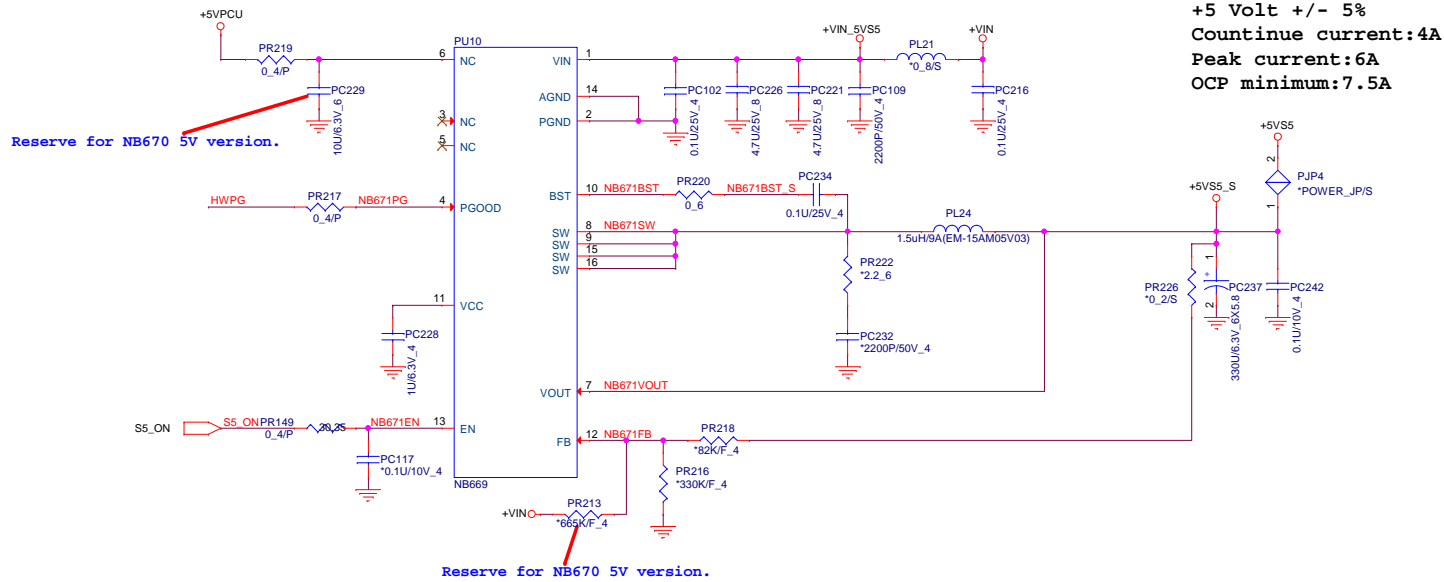
- +3V 2,6,7,8,9,10,12,13,14,23,24,25,26,27,29,30,31,33,36,39,40,42
- +3VPCU 5,7,25,30,31,33,34,35
- +5V 7,10,23,25,27,31,33,39
- +12VALW 34,39,43

PROJECT : R62
Quanta Computer Inc.

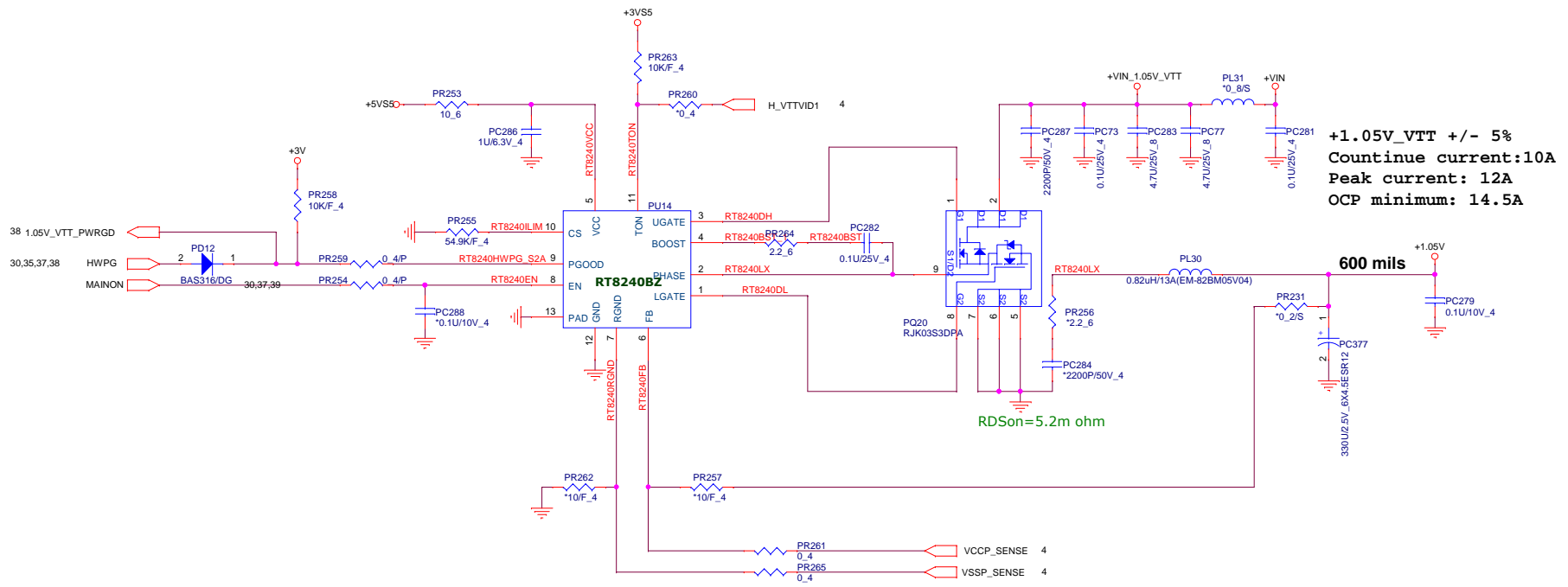
Size Custom	Document Number HDD/ODD/FAN	Rev 1A
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+3VS5
+5VS5
6,7,9,10,33,36,39,43
10,28,29,33,36,37,38,39,40,41,42,43



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	Quanta Computer Inc.		
	Size Custom	Document Number 3/5VPCU(RT8243A)	Rev 1A
Date: Monday, October 22, 2012		Sheet	35 of 43




+1.05V_VTT +/- 5%
Countinue current:10A
Peak current: 12A
OCP minimum: 14.5A

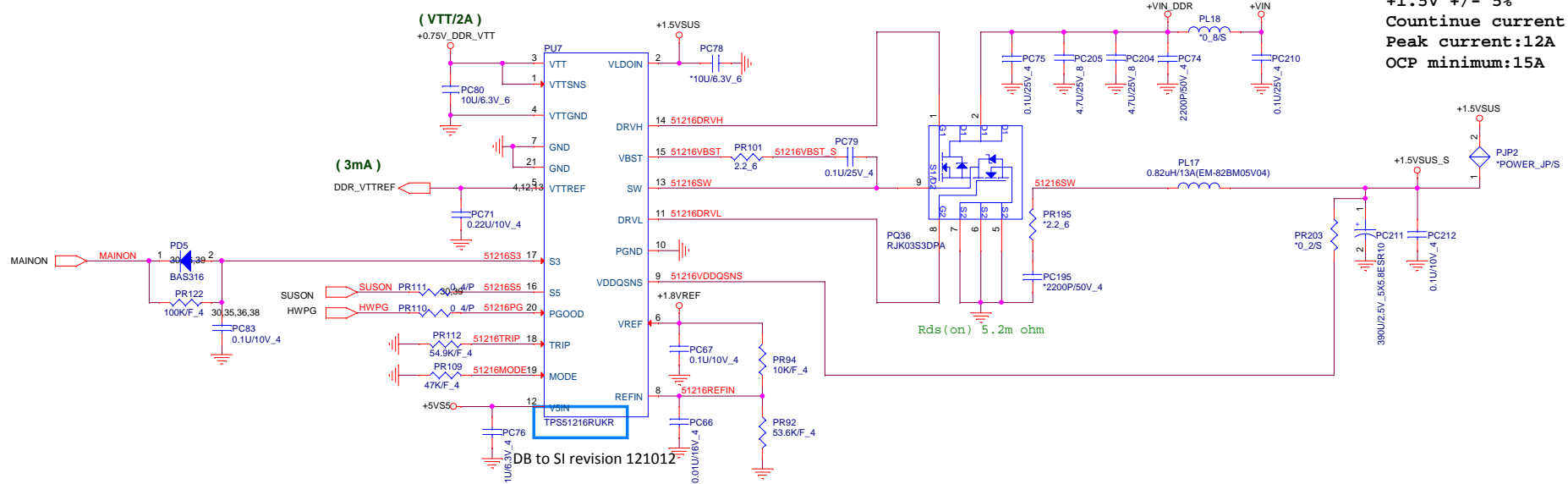
600 mils

RDSon=5.2m ohm

+1.05V 2,4,6,7,8,9,10,25,30,40

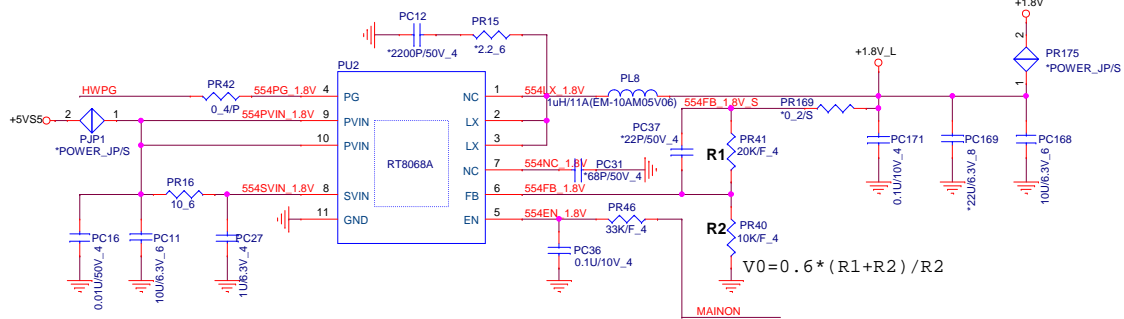
	PROJECT : R62		Rev 1A
	Quanta Computer Inc.		
	Size Custom	Document Number 1.05V(RT8228BZ)	
Date: Monday, October 22, 2012		Sheet 36 of 43	

+1.5V +/- 5%
Countinue current:10A
Peak current:12A
OCp minimum:15A



DB to SI revision 121012

1.8V +/- 3%
Countinue current:2A
Peak current:3A
OCp minimum:4A

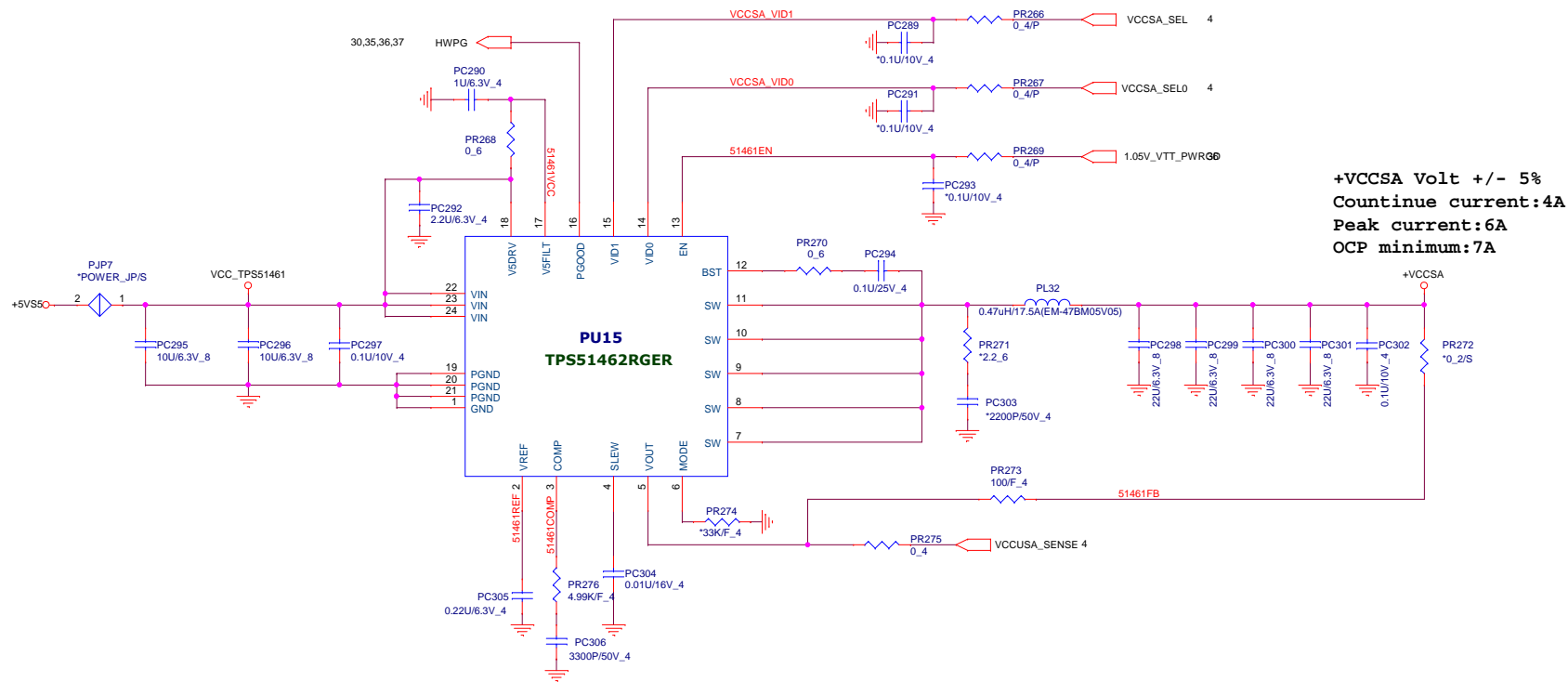


	PROJECT : R62		
	Quanta Computer Inc.		
	Size Custom	Document Number DDR3L(APW8819)	Rev 1A
Date	Monday, October 22, 2012	Sheet	37 of 43


TPSS1462RGER/AL051462000

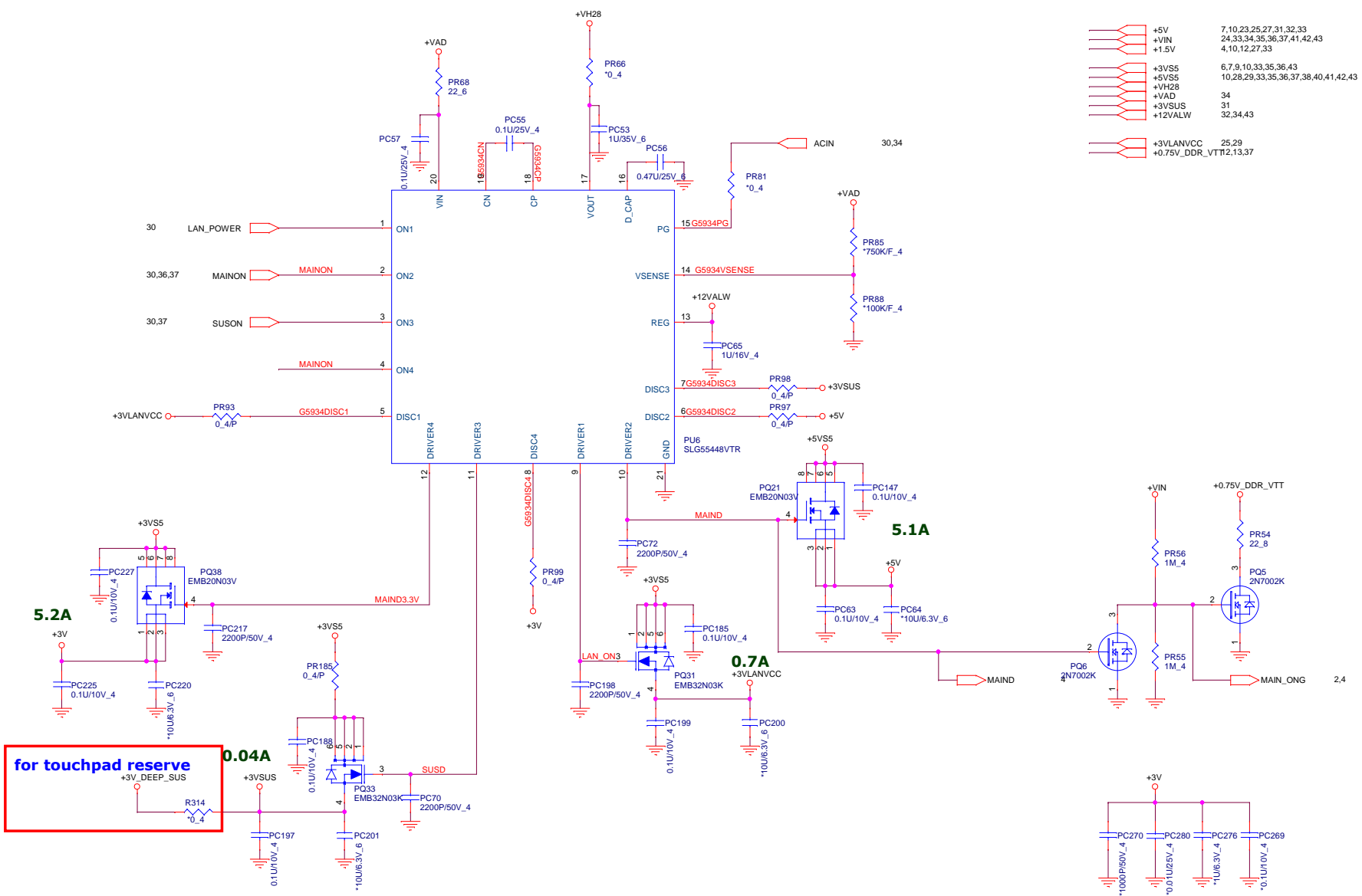
For CPU SV system agent
voltage slew rate of 0.5 -10 mV/μs

SEL0	SEL1	+VCCSA
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V



+VCCSA Volt +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7A

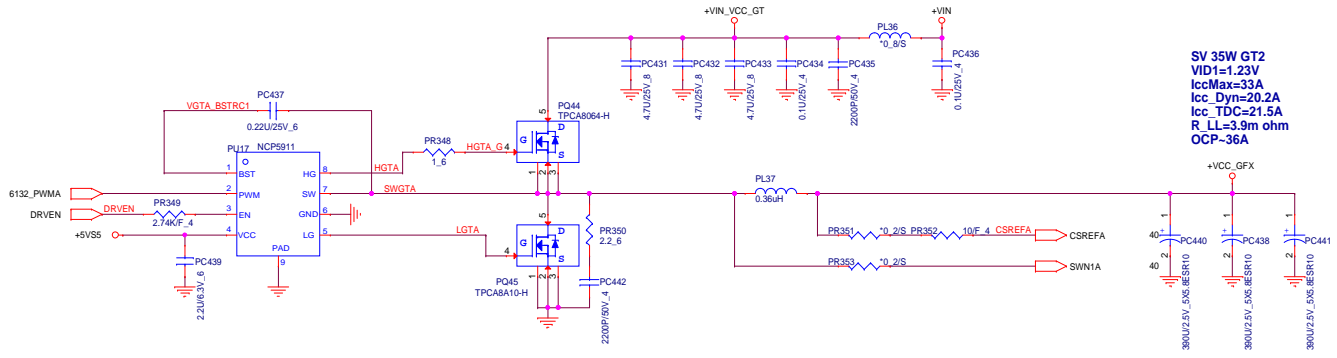
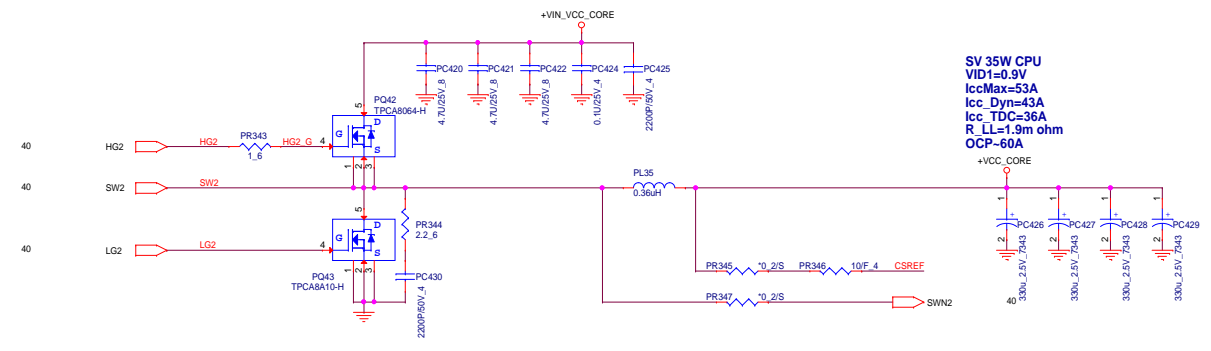
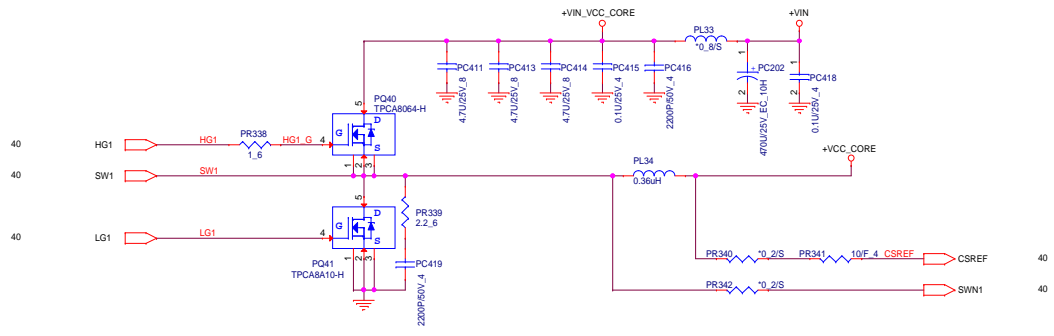
	PROJECT : R62		Rev 1A
	Quanta Computer Inc.		
	Size Custom	Document Number DDR3L(APW8819)	
Date: Monday, October 22, 2012		Sheet 38 of 43	



+5V	7,10,23,25,27,31,32,33
+VIN	24,33,34,35,36,37,41,42,43
+1.5V	4,10,12,27,33
+3VS5	6,7,9,10,33,35,36,43
+5VS5	10,28,29,33,35,36,37,38,40,41,42,43
+VH28	
+VAD	34
+3VSUS	31
+12VALW	32,34,43
+3VLAVCC	25,29
+0.75V_DDR_VTT2	13,37

for touchpad reserve

	PROJECT : R62 Quanta Computer Inc.	
	Size Custom Document Number Dis-charge IC (G5934) Date: Monday, October 22, 2012	Rev 1A Sheet 39 of 43



VGA Core

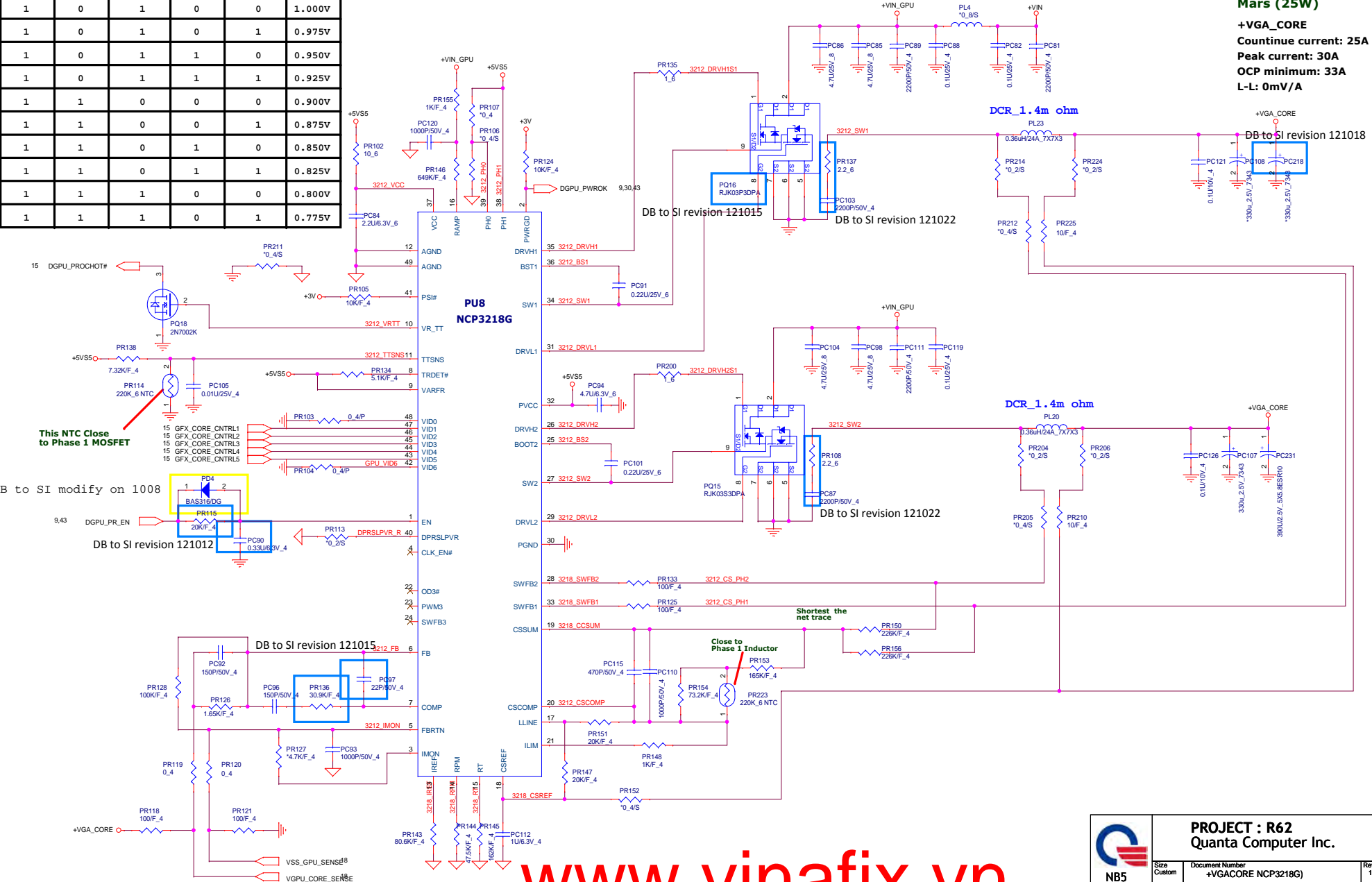
GPIO10 GPIO12 GPIO16 GPIO20 GPIO15 Mars XT

PWRCNTL5	PWRCNTL4	PWRCNTL3	PWRCNTL2	PWRCNTL1	V-CORE
0	1	1	1	1	1.125V
1	0	0	0	0	1.100V
1	0	0	0	1	1.075V
1	0	0	1	0	1.050V
1	0	0	1	1	1.025V
1	0	1	0	0	1.000V
1	0	1	0	1	0.975V
1	0	1	1	0	0.950V
1	0	1	1	1	0.925V
1	1	0	0	0	0.900V
1	1	0	0	1	0.875V
1	1	0	1	0	0.850V
1	1	0	1	1	0.825V
1	1	1	0	0	0.800V
1	1	1	0	1	0.775V

Default

Mars (25W)

+VGA_CORE
 Continune current: 25A
 Peak current: 30A
 OCP minimum: 33A
 L-L: 0mV/A



This NTC Close to Phase 1 MOSFET

DB to SI modify on 1008

DB to SI revision 121012

DB to SI revision 121015

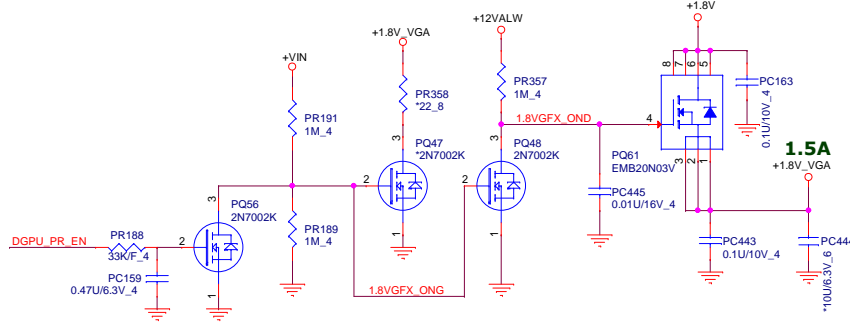
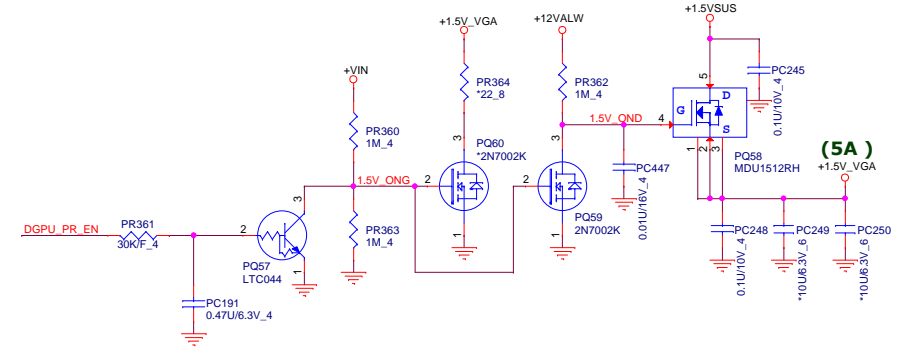
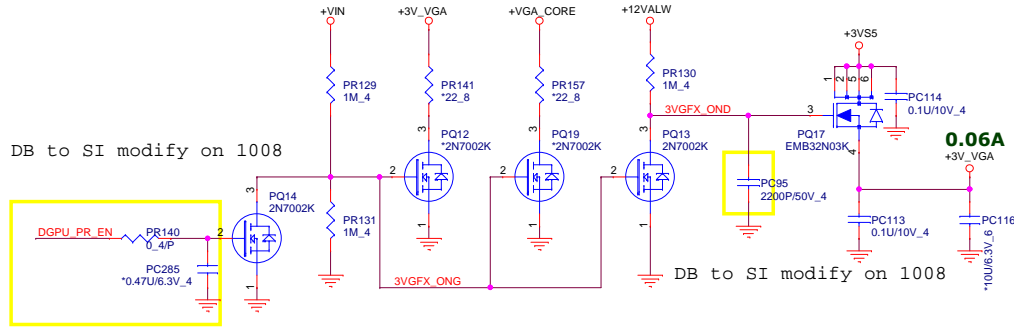
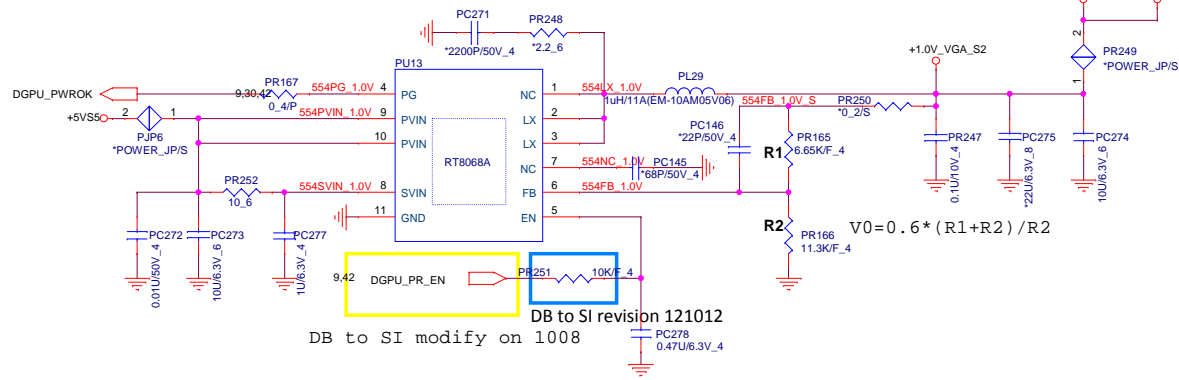
Close to Phase 1 Inductor

Shortest the net trace

NB5	PROJECT : R62		Rev 1A
	Quanta Computer Inc.		
	Size Custom	Document Number +VGA_CORE NCP3218G	
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R2 Value	P/N	1.0V_VGA
10K	CS31002FB26	1.0V
11.3K	CS31132FB07	0.95V

+0.95V +/- 3%
 Countinue current:2A
 Peak current:3A
 OCP minimum:4A



- +1.8V_VGA 15,16,18,19,25
- +1.0V_VGA 14,16,18,19
- +3V_VGA 18

	PROJECT : R62 Quanta Computer Inc.	
	Size Custom Document Number +VGA CORE (RT8208/1.8V) Date: Monday, October 22, 2012	Rev 1A Sheet 43 of 43