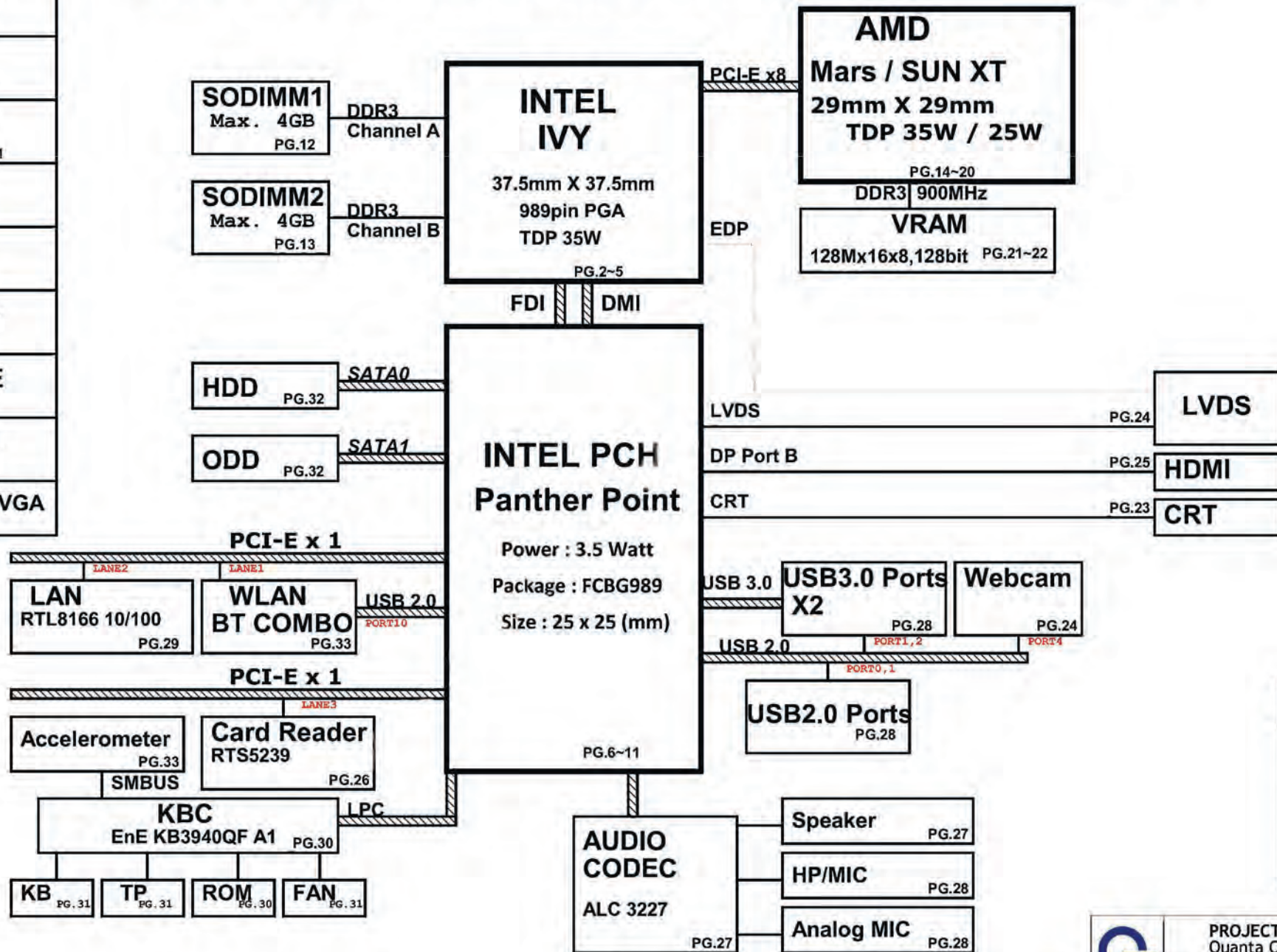


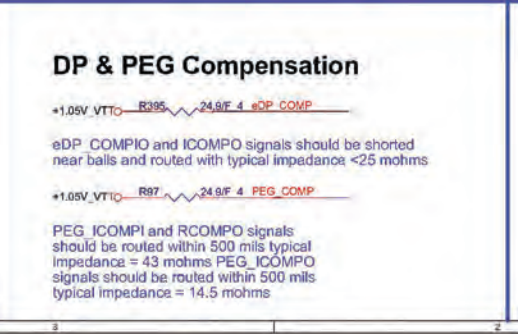
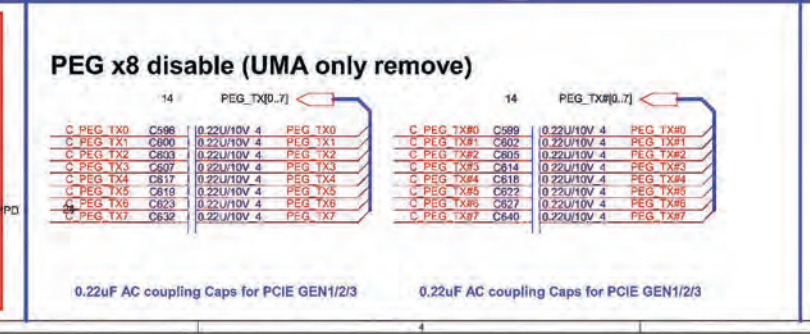
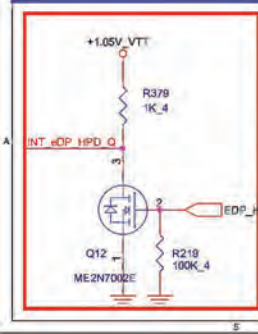
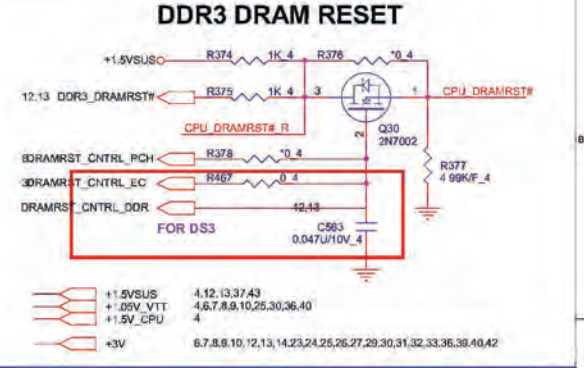
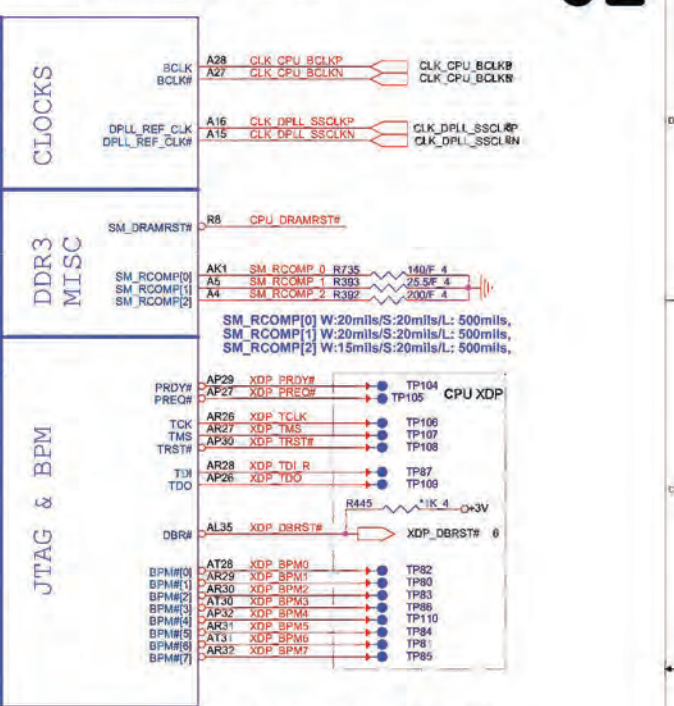
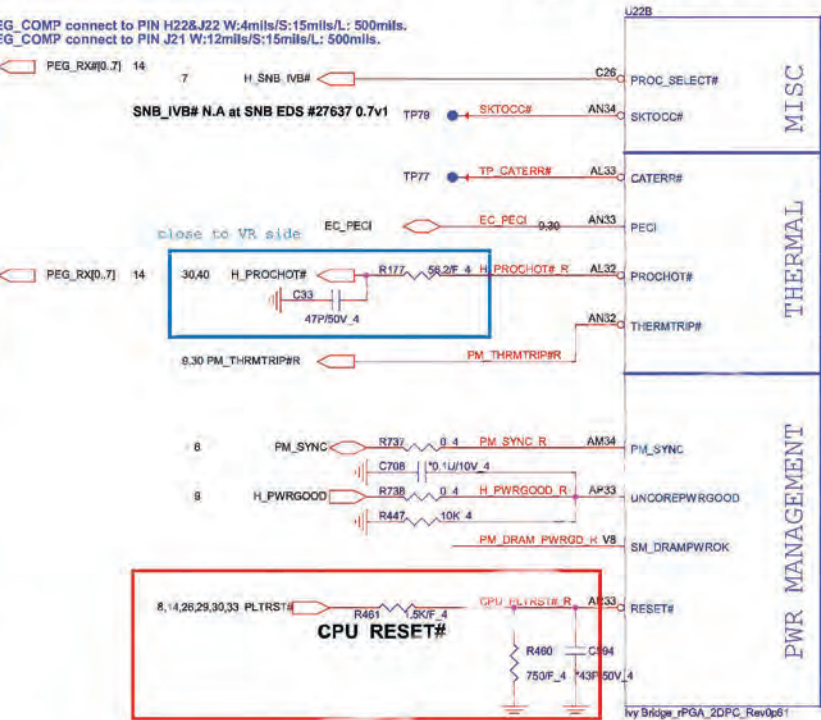
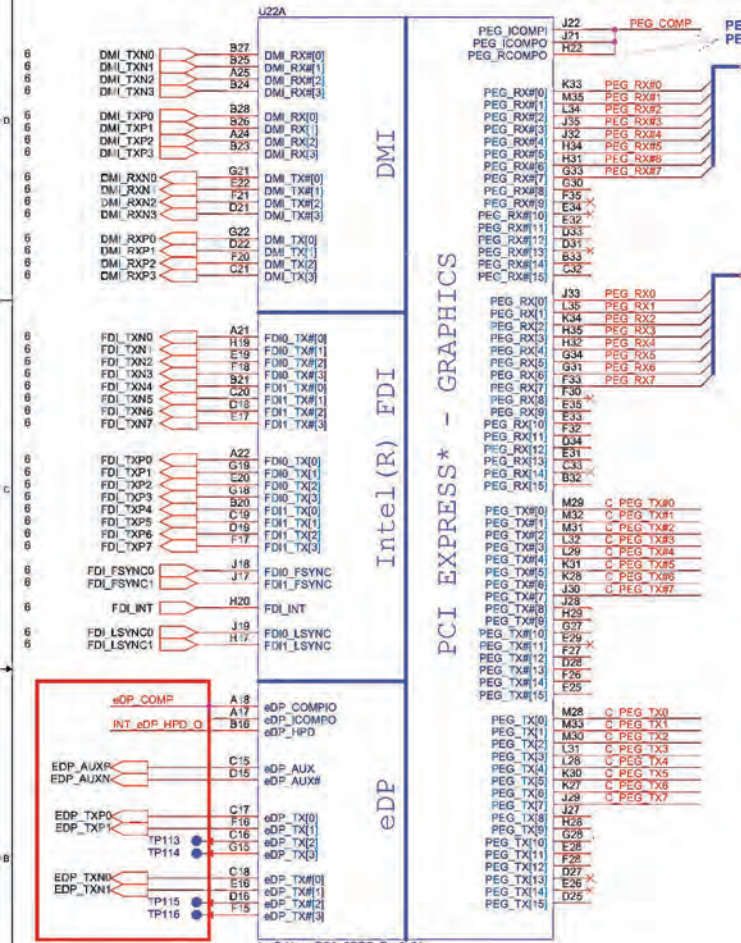
R62 INTEL CHIEF RIVER SYSTEM DIAGRAM

01

+3V/+5V S5
PG.35
+1.05V
PG.36
CPU Core
PG.40~41
DDR3
PG.37
Charge
PG.34
Dis-Charge
PG.39
+VGACORE
PG.42
+VCCSA
PG.38
+1.0V/+1.8/ +3 VGA
PG.43



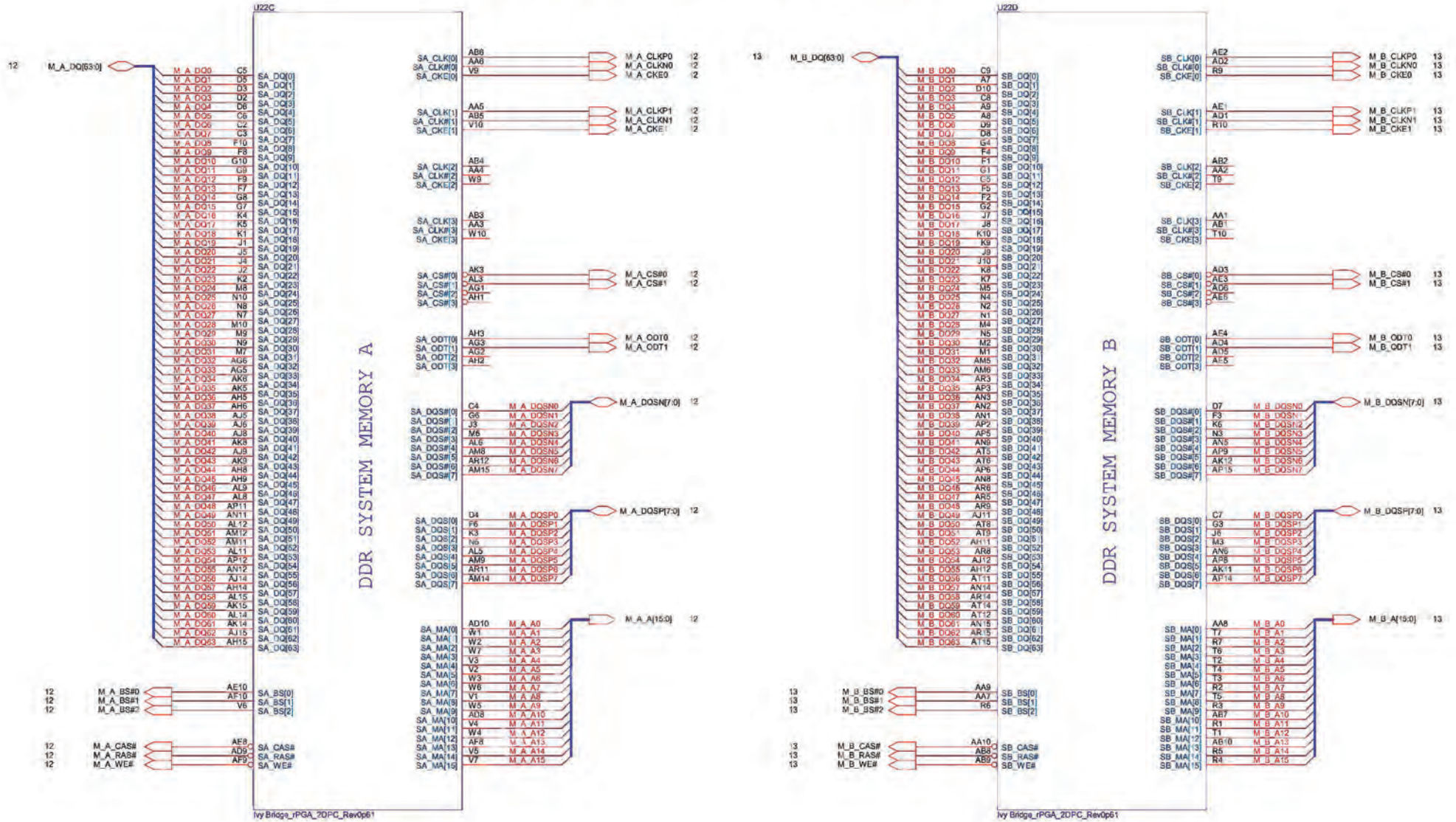
Stackup
TOP
GND
IN1
IN2
VCC
BOT



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Quanta Computer Inc.

Size: Custom
Document Number: SNB 1/4 (PCIE&DMI&FDI)
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Sheet: 2 of 43
Rev: 1A

Ivy Bridge Processor (DDR3)



PROJECT : R62
Quanta Computer Inc.

Size: Custom
 Document Number: SNB 2/4 (DDR3 I/F)
 Date: Monday, October 22, 2012 | Sheet: 3 of 43

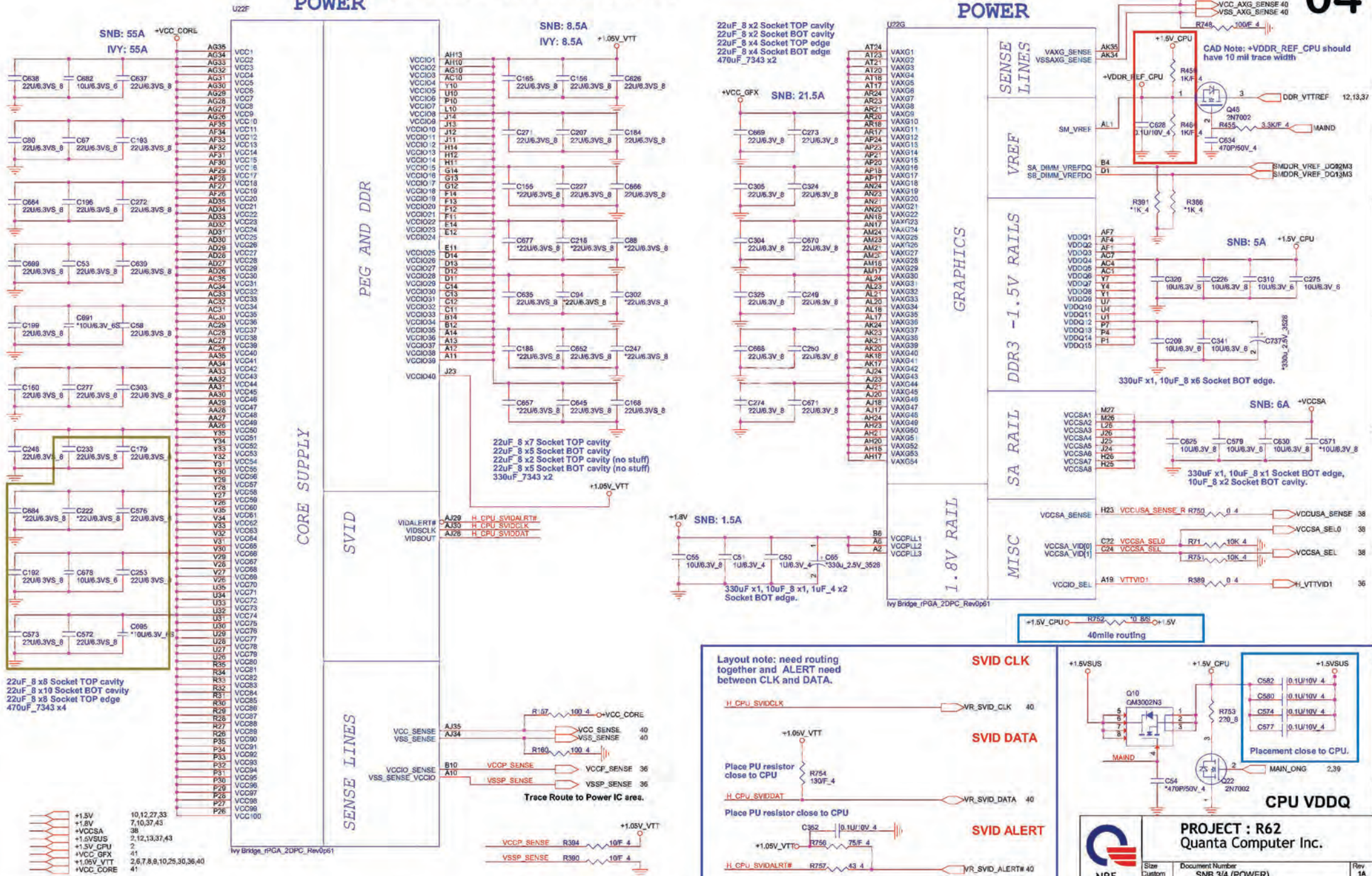
NBS

Ivy Bridge Processor (POWER)

04

POWER

POWER



+1.5V	10,12,27,33
+1.8V	7,10,37,43
+VCCSA	38
+1.5VSUS	2,12,13,37,43
+1.5V_CPU	2
+VCC_GFX	41
+1.05V_VTT	2,6,7,8,9,10,25,30,36,40
+VCC_CORE	41

Ivy Bridge_rPGA_2DPC_Rev0p61

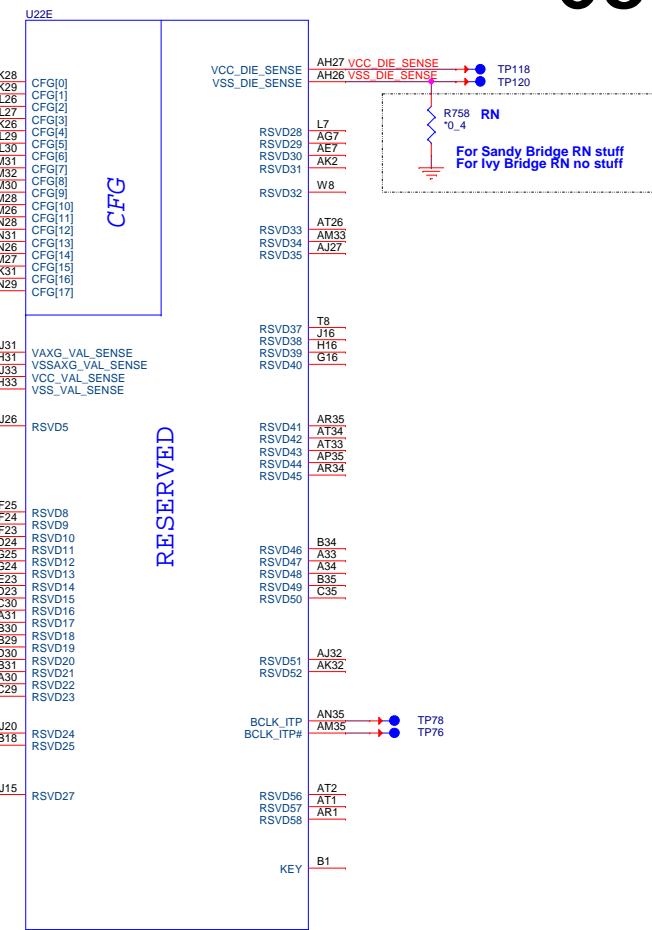
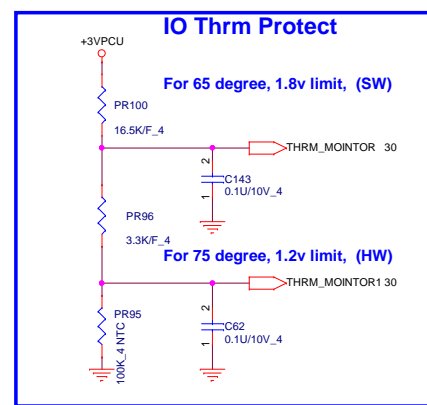
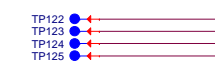
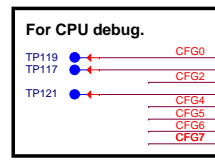
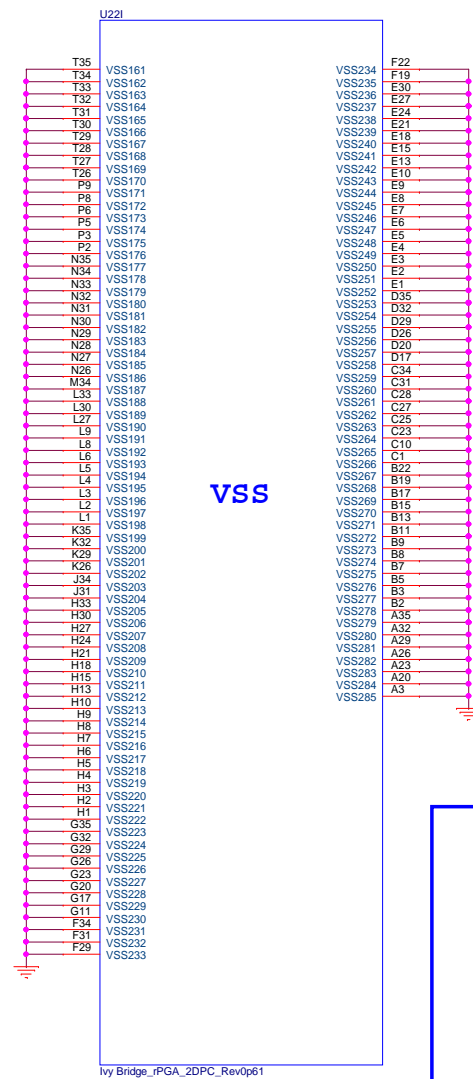
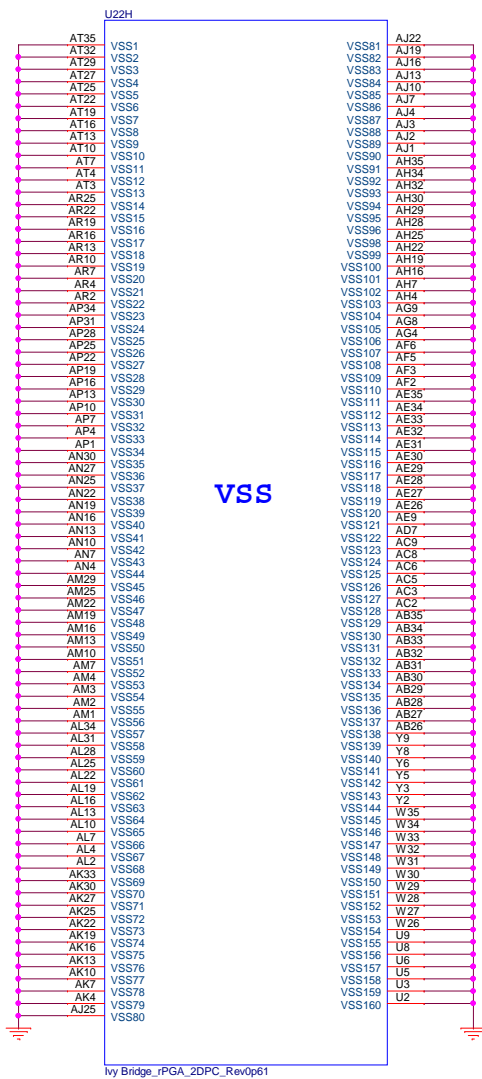
Ivy Bridge_rPGA_2DPC_Rev0p61

+1.5V_CPU - R752 10 85 40 +1.5V
 40mile routing



Ivy Bridge Processor (GND)

Ivy Bridge Processor (RESERVED, CFG)

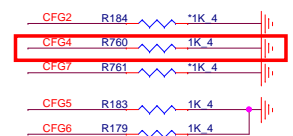


For rPGA socket, RSVD59 pin should be left NC.

Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

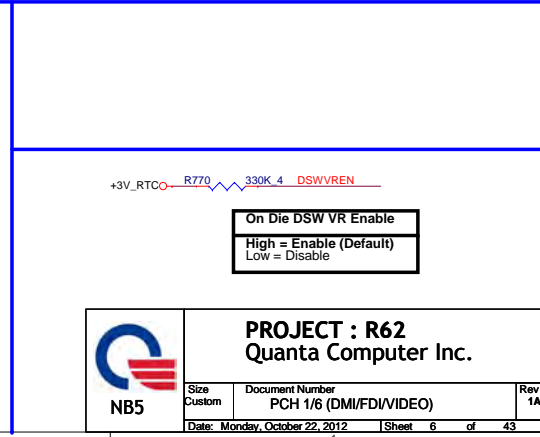
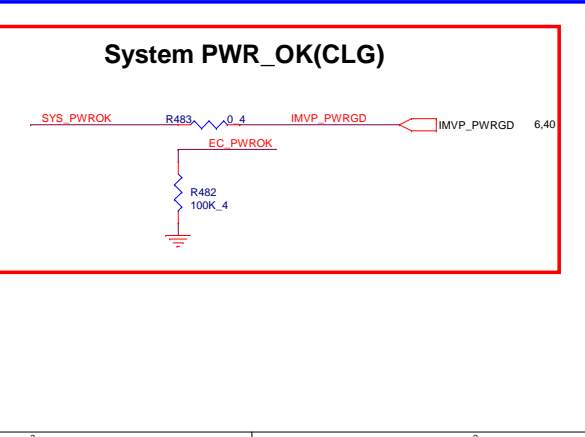
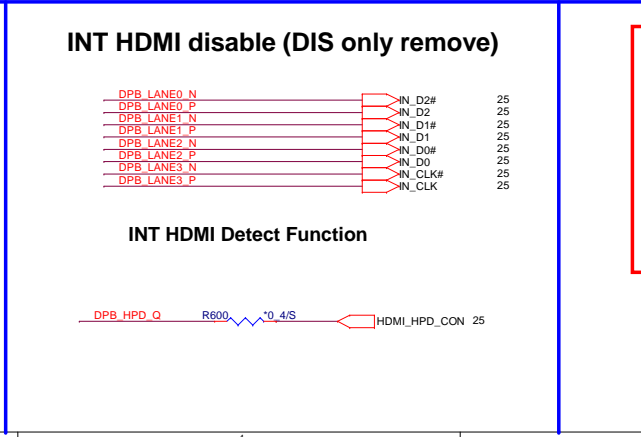
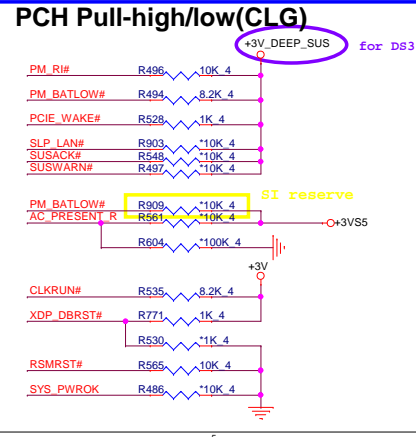
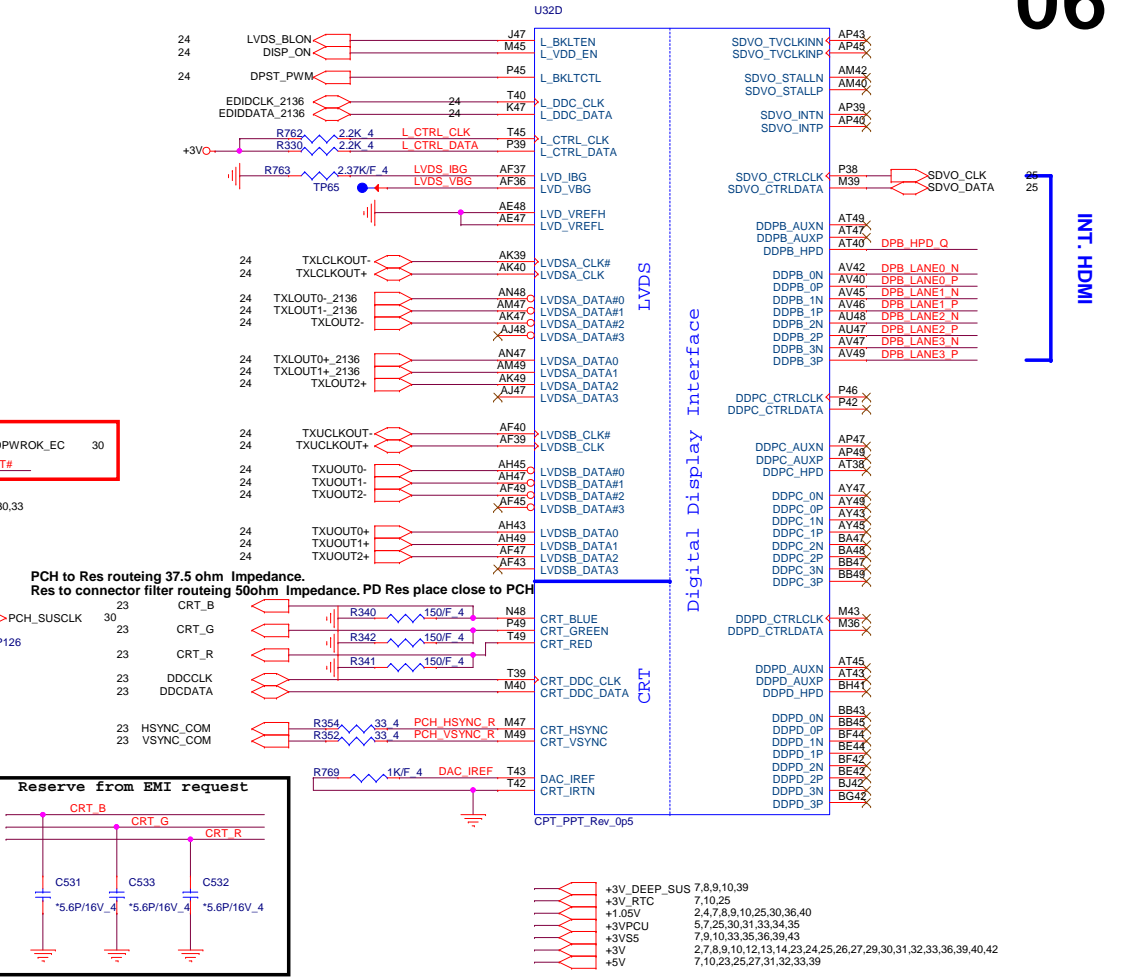
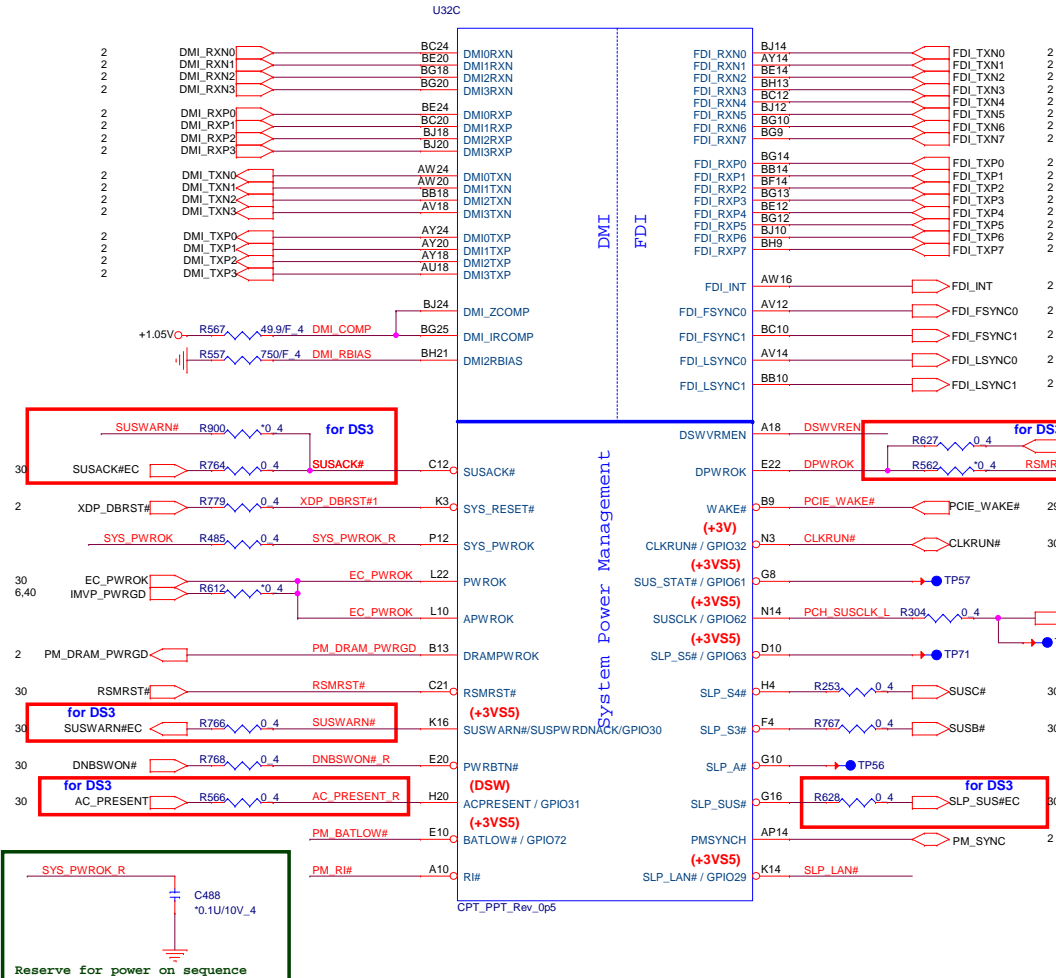
	1	0
CFG2 (PEG Static Lane Reversa)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training



CFG[6:5] (PCIe Port Bifurcation Straps)
 11: (Default) x16 - Device 1 functions 1 and 2 disabled
 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

PROJECT : R62
Quanta Computer Inc.

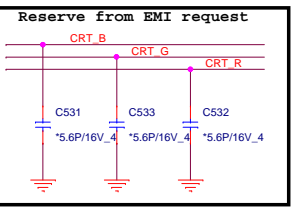
Size Custom	Document Number SNB 4/4 (GND)	Rev 1A
Date: Monday, October 22, 2012	Sheet 5 of 43	



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Quanta Computer Inc.

Size: Custom
 Document Number: PCH 1/6 (DMI/FDI/VIDEO)
 Date: Monday, October 22, 2012 | Sheet 6 of 43

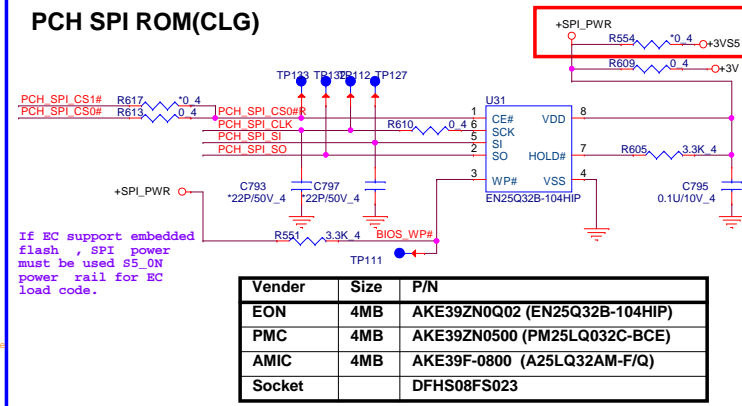
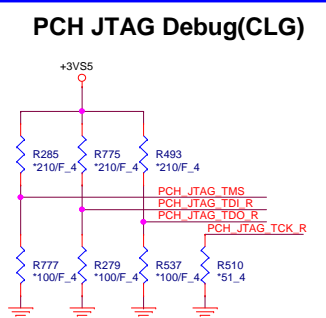
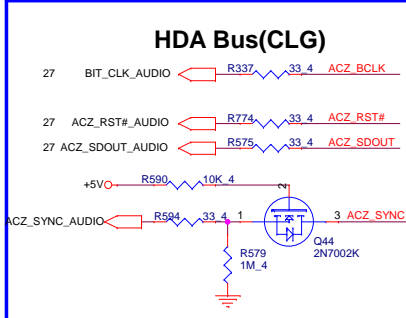
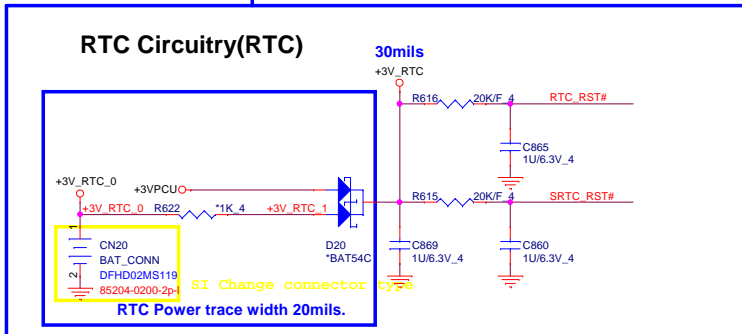
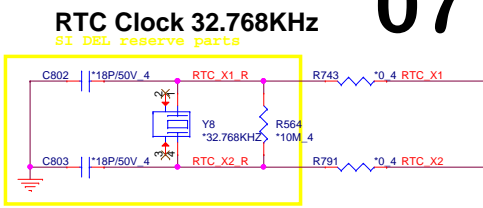
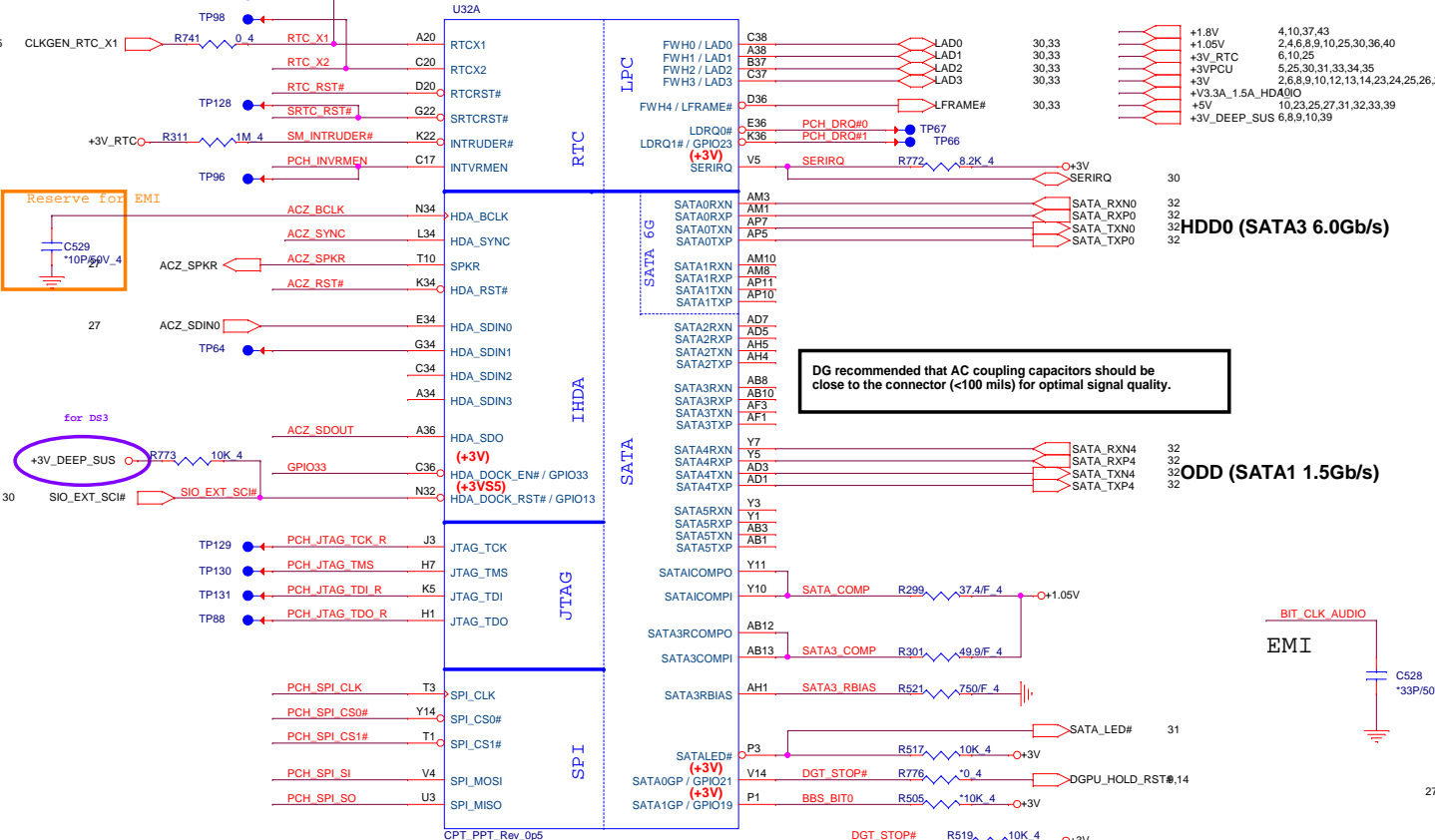
PCH to Res routing 37.5 ohm Impedance.
 Res to connector filter routing 50ohm Impedance. PD Res place close to PCH



On Die DSW VR Enable
 High = Enable (Default)
 Low = Disable

Cougar Point/Panther Point (HDA,JTAG,SATA)

07



Vender	Size	P/N
EON	4MB	AKE392N0Q02 (EN25Q32B-104HIP)
PMC	4MB	AKE392N0500 (PM25LQ032C-BCE)
AMIC	4MB	AKE39F-0800 (A25LQ32AM-F/Q)
Socket		DFHS08FS023

DG recommended that AC coupling capacitors should be close to the connector (<100 mils) for optimal signal quality.

ODD (SATA1 1.5Gb/s)

PCH Strap Table

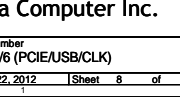
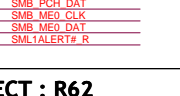
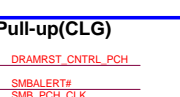
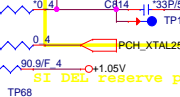
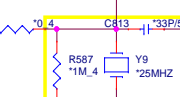
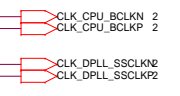
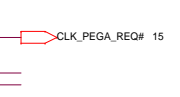
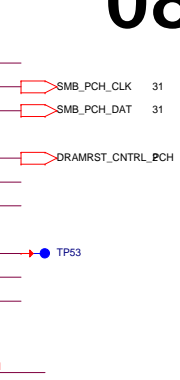
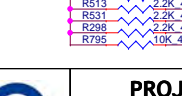
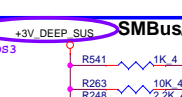
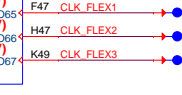
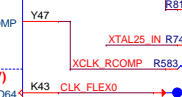
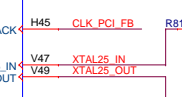
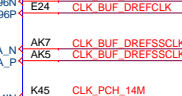
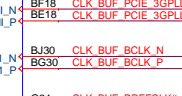
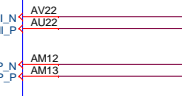
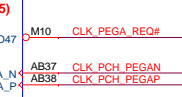
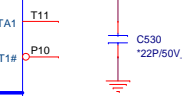
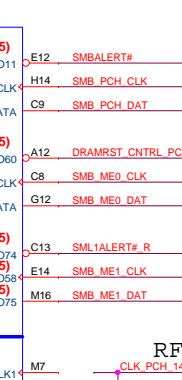
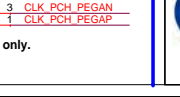
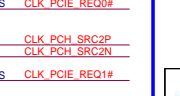
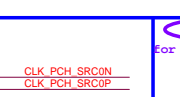
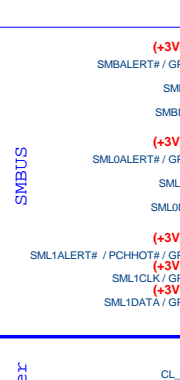
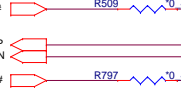
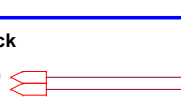
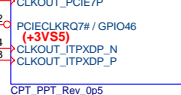
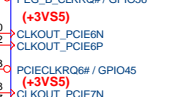
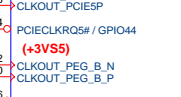
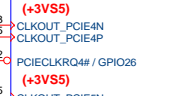
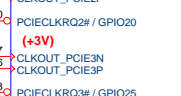
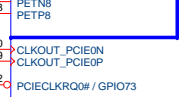
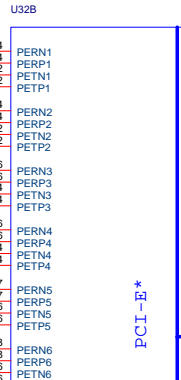
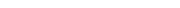
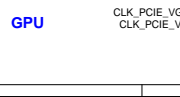
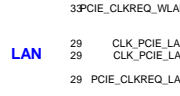
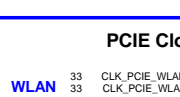
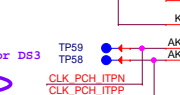
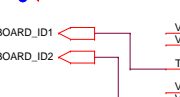
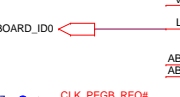
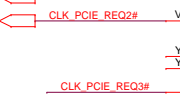
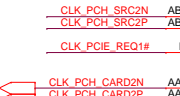
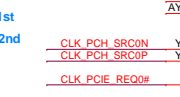
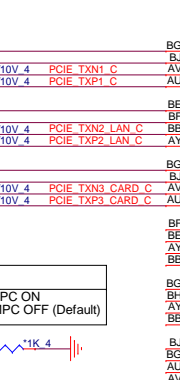
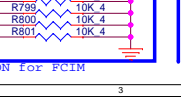
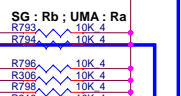
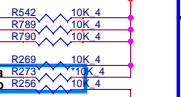
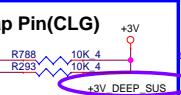
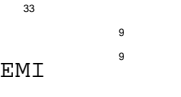
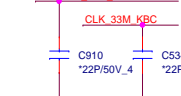
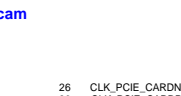
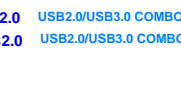
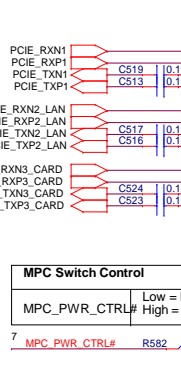
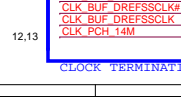
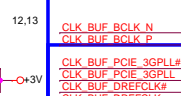
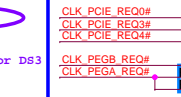
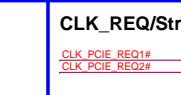
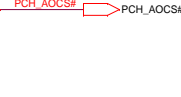
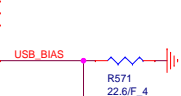
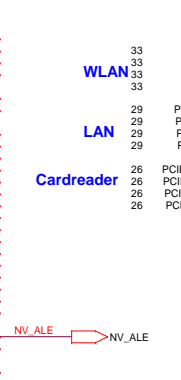
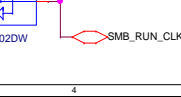
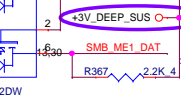
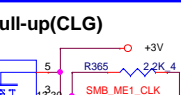
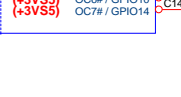
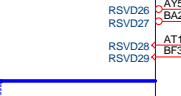
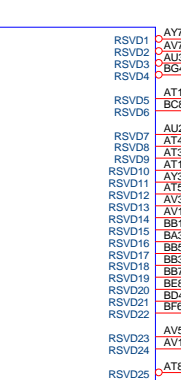
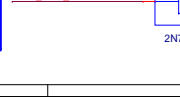
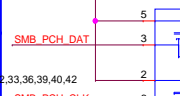
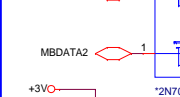
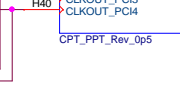
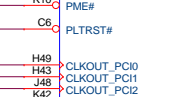
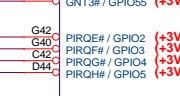
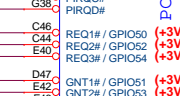
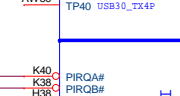
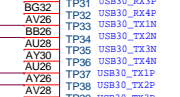
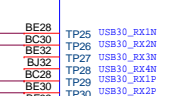
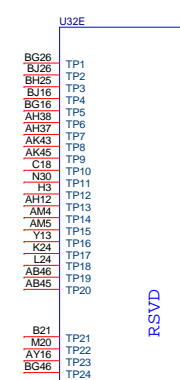
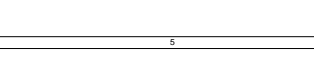
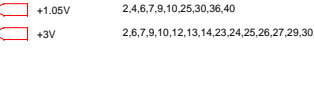
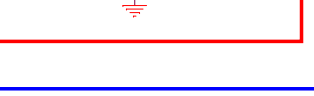
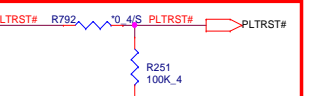
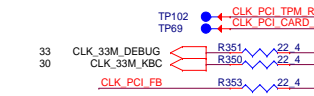
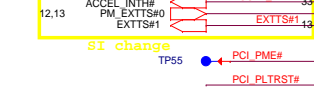
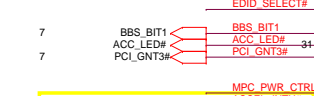
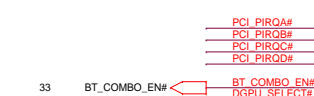
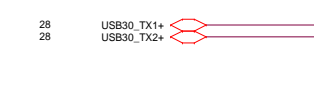
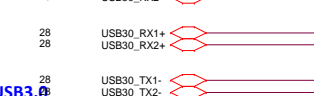
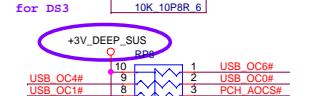
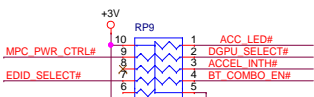
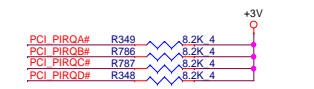
Pin Name	Strap description	Sampled	Configuration	Circuit
SPKR	Different from Calpella No reboot mode setting	PWR0K	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	
GNT3# / GPIO55	Top-Block Swap Override	PWR0K	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	+3V ₀ R595 10K 4 PCI_GNT3# 8
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	PCH_INVRMEN R563 330K 4 +3V_RTC
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security Only for Interposer	PWR0K	0 = Override 1 = Default (weak pull-up 20K)	GPIO33 R572 0.4 2 BIOS_WP#
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWR0K	[Need external pull-down for LPC BIOS] Default weak pull-up on GNT0/1#	R782 1K 4 BBS_BIT0 R595 1K 4 BBS_BIT1 8
GPIO19	Different from Calpella Boot BIOS Selection 0 [bit-0]	PWR0K		
GNT2# / GPIO53	ESI strap (Server only)	PWR0K	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN
NV_ALE	Intel Anti-Theft HDD protection Only for Interposer	PWR0K	0 = Disable (Internal pull-down 20kohm)	+1.8V ₀ R783 1K 4 NV_ALE 8
NV_CLE	DMI Termination voltage	PWR0K	weak pull-down 20kohm	+1.8V ₀ R526 2.2K 4 R546 1K 4 NV_CLE H_SNB_IVB# 9 bandy/ivy_brd16
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	+V3.3A_1.5A_HDA_IO R784 1K 4 ACZ_SYNC
HDA_SDO	Flash Descriptor Security	PWR0K	0 = Default (weak pull-down 20K) 1 = Overriden	GPIO33_E ACZ_SDOUT R573 1K 4 +V3.3A_1.5A_HDA_IO
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)	
GPIO28	Different from Calpella On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	
SPI_MOSI	ITPM function Disable	APWR0K	0 = Default (weak pull-down 20K) 1 = Enable	

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PCI/USBOC# Pull-up(CLG)



MPC Switch Control
MPC_PWR_CTRL# Low = MPC ON
MPC_PWR_CTRL# High = MPC OFF (Default)

USB B2.0 USB2.0/USB3.0 COMBO 1st
USB B2.0 USB2.0/USB3.0 COMBO 2nd

Webcam
USB P0-USB P4

High USB WLAN
USB P9-USB P10

EMMI
CLK_PCIE_REQ1#-4
CLK_PCIE_REQ0#-3
CLK_PCIE_REQ3#-2
CLK_PCIE_REQ4#-1

EMMI
CLK_PCIE_REQ1#-4
CLK_PCIE_REQ0#-3
CLK_PCIE_REQ3#-2
CLK_PCIE_REQ4#-1

EMMI
CLK_PCIE_REQ1#-4
CLK_PCIE_REQ0#-3
CLK_PCIE_REQ3#-2
CLK_PCIE_REQ4#-1

EMMI
CLK_PCIE_REQ1#-4
CLK_PCIE_REQ0#-3
CLK_PCIE_REQ3#-2
CLK_PCIE_REQ4#-1

EMMI
CLK_PCIE_REQ1#-4
CLK_PCIE_REQ0#-3
CLK_PCIE_REQ3#-2
CLK_PCIE_REQ4#-1

EMMI
CLK_PCIE_REQ1#-4
CLK_PCIE_REQ0#-3
CLK_PCIE_REQ3#-2
CLK_PCIE_REQ4#-1

EMMI
CLK_PCIE_REQ1#-4
CLK_PCIE_REQ0#-3
CLK_PCIE_REQ3#-2
CLK_PCIE_REQ4#-1

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CLK_PCIE_REQ1#-4
CLK_PCIE_REQ0#-3
CLK_PCIE_REQ3#-2
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EMMI
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CLK_PCIE_REQ0#-3
CLK_PCIE_REQ3#-2
CLK_PCIE_REQ4#-1

EMMI
CLK_PCIE_REQ1#-4
CLK_PCIE_REQ0#-3
CLK_PCIE_REQ3#-2
CLK_PCIE_REQ4#-1

Controller Link
CL_CLK1#
CL_DATA1#
CL_RST1#

Controller Link
CL_CLK1#
CL_DATA1#
CL_RST1#

Controller Link
CL_CLK1#
CL_DATA1#
CL_RST1#

Controller Link
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CL_RST1#

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CL_RST1#

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CL_RST1#

Controller Link
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CL_DATA1#
CL_RST1#

Controller Link
CL_CLK1#
CL_DATA1#
CL_RST1#

RF
CLK_PCH_14M
CLK_PCH_PEGAN
CLK_PCH_PEGAP

RF
CLK_PCH_14M
CLK_PCH_PEGAN
CLK_PCH_PEGAP

RF
CLK_PCH_14M
CLK_PCH_PEGAN
CLK_PCH_PEGAP

RF
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CLK_PCH_PEGAP

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CLK_PCH_PEGAN
CLK_PCH_PEGAP

RF
CLK_PCH_14M
CLK_PCH_PEGAN
CLK_PCH_PEGAP

RF
CLK_PCH_14M
CLK_PCH_PEGAN
CLK_PCH_PEGAP

RF
CLK_PCH_14M
CLK_PCH_PEGAN
CLK_PCH_PEGAP

PCIE Clock
CLK_PCIE_WLAN#
CLK_PCIE_LAN#
CLK_PCIE_VGA#

PCIE Clock
CLK_PCIE_WLAN#
CLK_PCIE_LAN#
CLK_PCIE_VGA#

PCIE Clock
CLK_PCIE_WLAN#
CLK_PCIE_LAN#
CLK_PCIE_VGA#

PCIE Clock
CLK_PCIE_WLAN#
CLK_PCIE_LAN#
CLK_PCIE_VGA#

PCIE Clock
CLK_PCIE_WLAN#
CLK_PCIE_LAN#
CLK_PCIE_VGA#

SMBus/Pull-up(CLG)
SMBALERT#
SMB_PCH_CLK
SMB_PCH_DAT

SMBus/Pull-up(CLG)
SMBALERT#
SMB_PCH_CLK
SMB_PCH_DAT

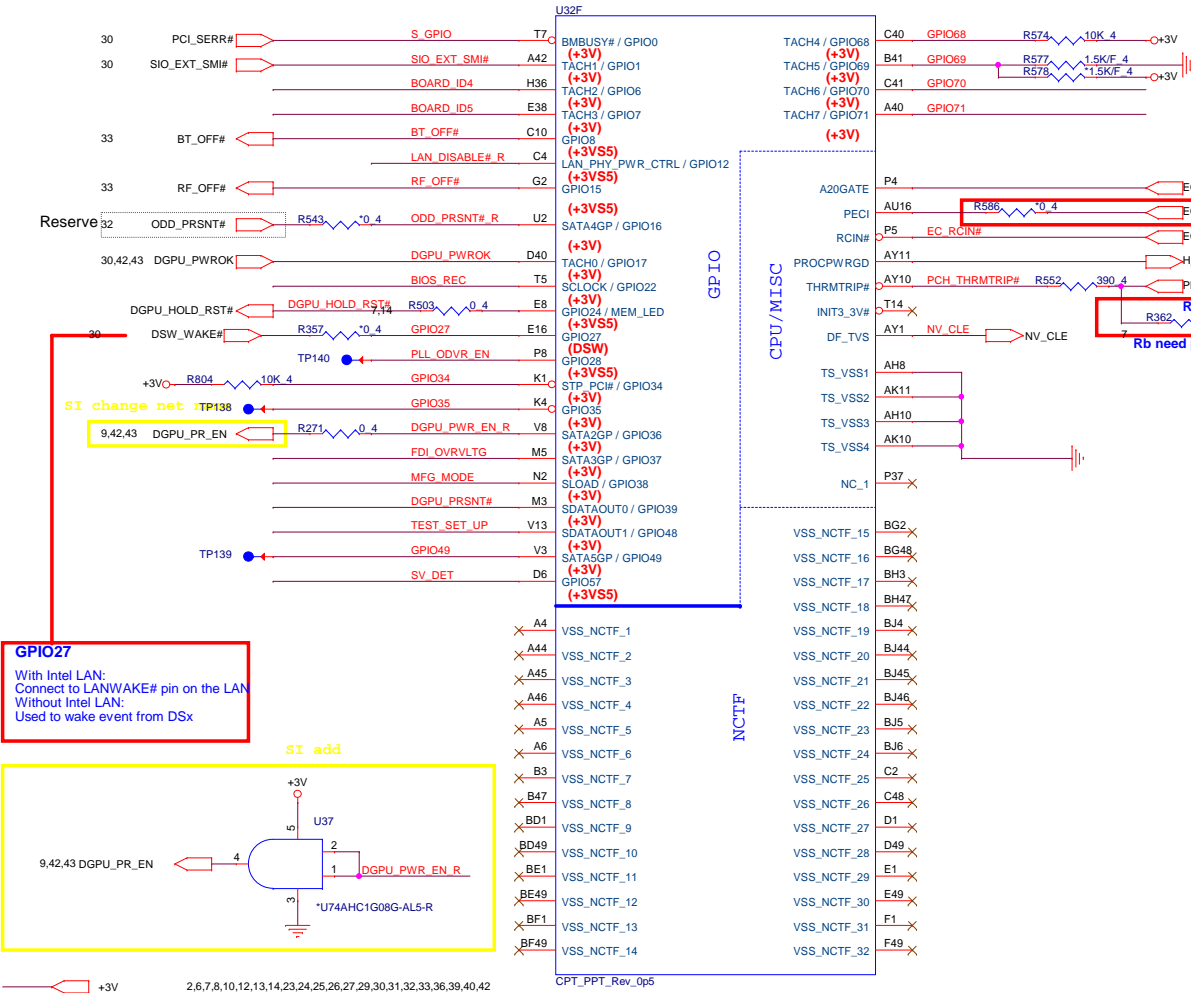
SMBus/Pull-up(CLG)
SMBALERT#
SMB_PCH_CLK
SMB_PCH_DAT

SMBus/Pull-up(CLG)
SMBALERT#
SMB_PCH_CLK
SMB_PCH_DAT

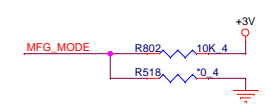
SMBus/Pull-up(CLG)
SMBALERT#
SMB_PCH_CLK
SMB_PCH_DAT

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Quanta Computer Inc.
NB5
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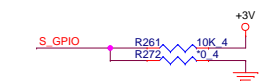
Cougar Point/Panther Point (GPIO,VSS_NCTF,RSVD)



MFG-TEST



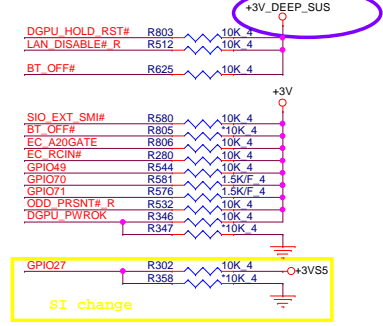
Swap GPIO



0 = SGPIO
1 = Default

for DS3

GPIO Pull-up/Pull-down(CLG) for DS3



Intel ME Crypto Transport Layer Security (TLS) cipher suite
Low = Disable (Default)
High = Enable

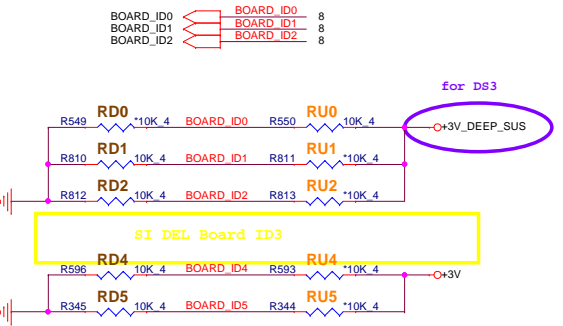
BIOS RECOVERY High = Disable (Default)
Low = Enable

SV_SET_UP High = Strong (Default)

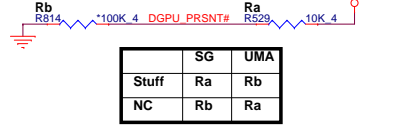
TEST DETECT Low = Default

BOARD ID SETTING

Model	BOARD_ID5	BOARD_ID4	BOARD_ID3	BOARD_ID2	BOARD_ID1	BOARD_ID0
DB R62 UMA				0	0	0
DB R62 DIS				0	0	1
			0	1	1	1
		1	1	1	1	1
		0	0	0	0	0



GFX Present



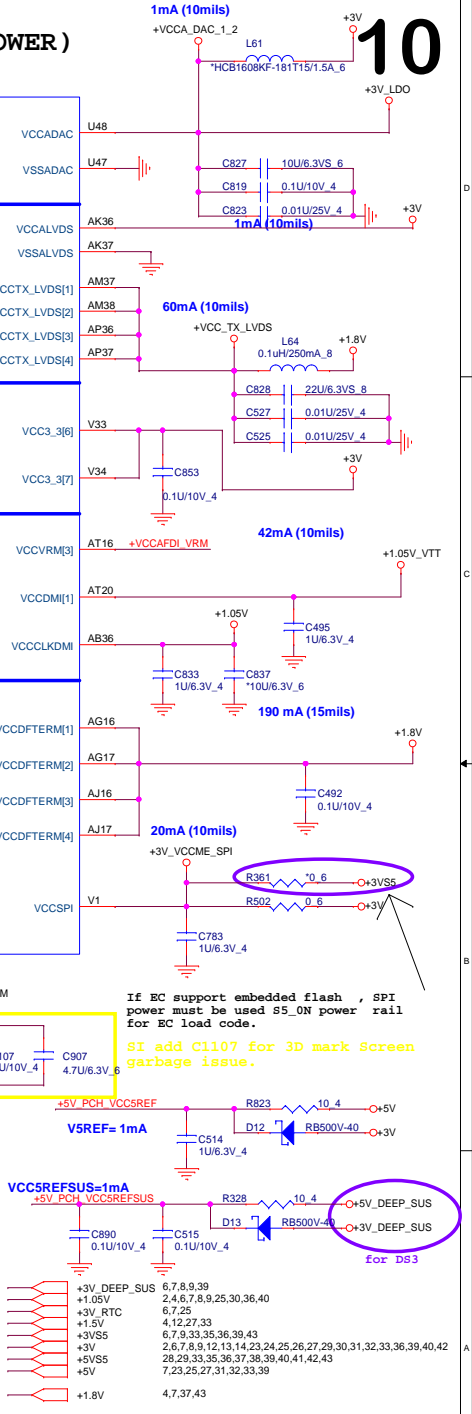
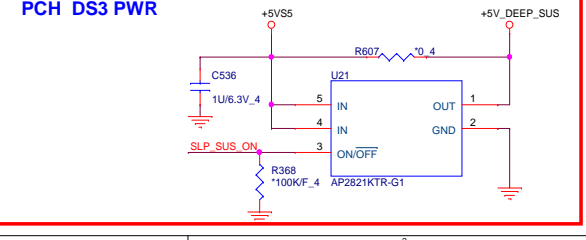
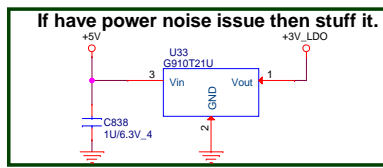
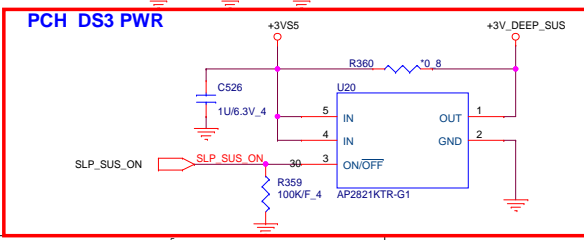
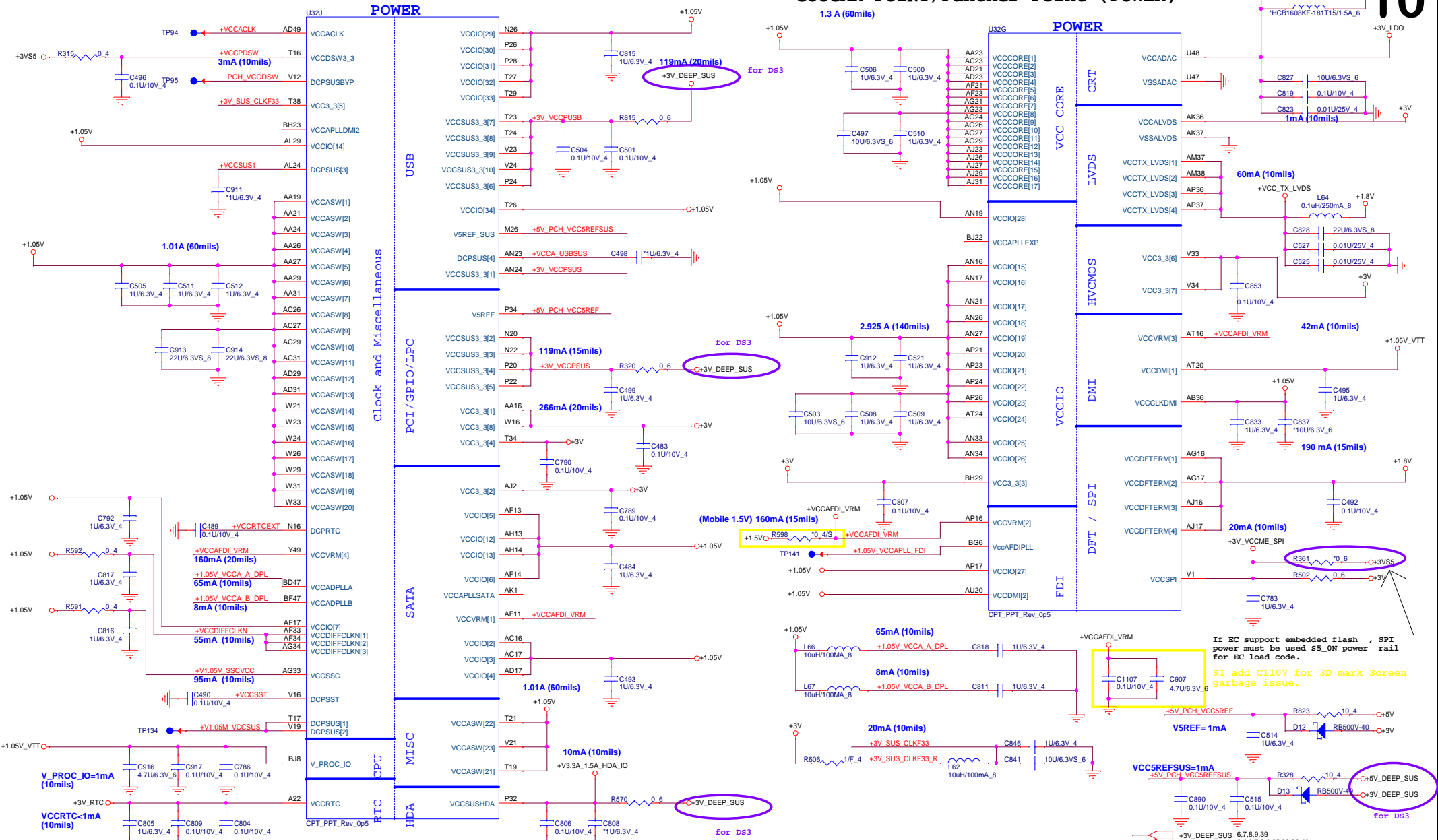
SG	UMA
Stuff	Ra Rb
NC	Rb Ra




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Cougar Point/Panther Point (POWER)

COUGAR POINT/Panther Point (POWER)





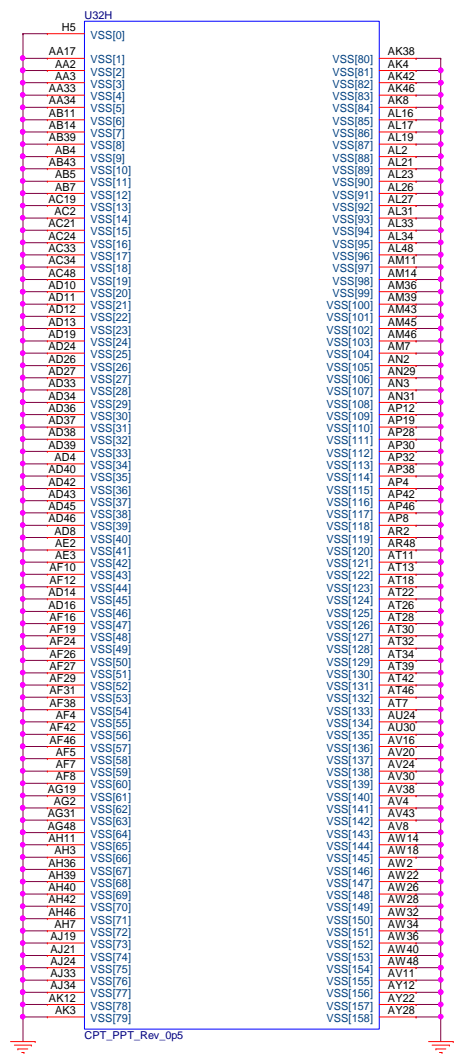
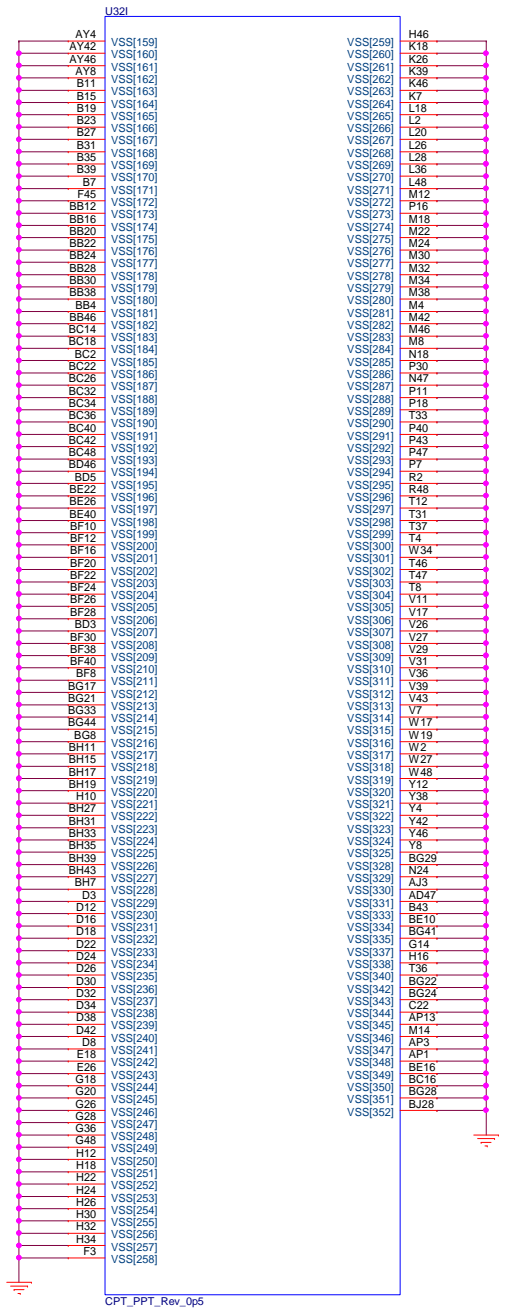
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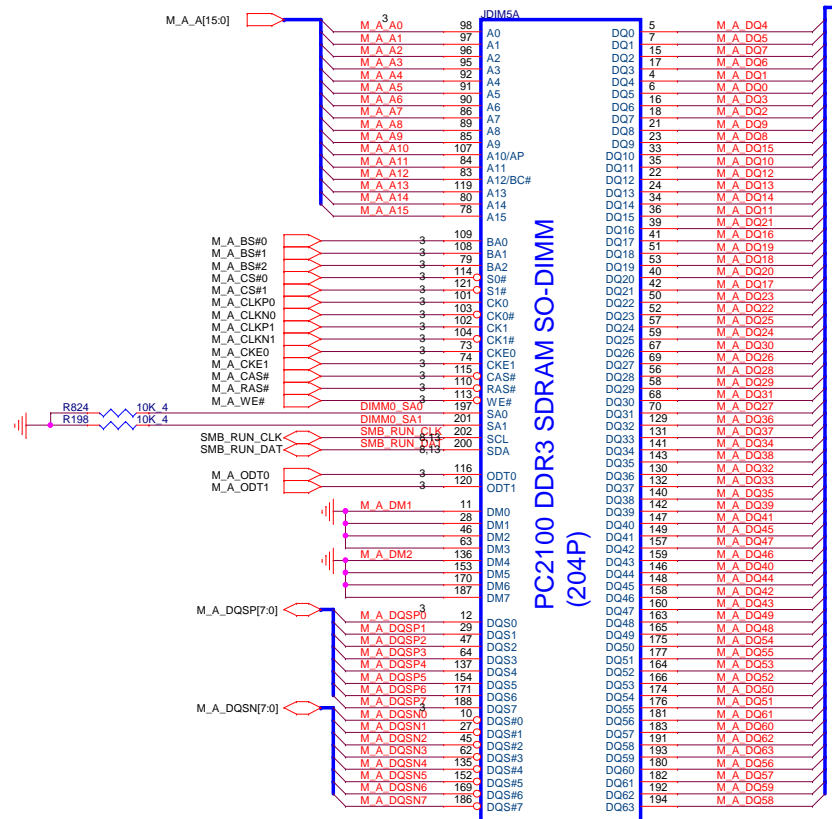
Size	Document Number	Rev
Custom	PCH 5/6 (POWER)	1A
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Cougar Point/Panther Point (GND)

Cougar Point/Panther Point (GND)

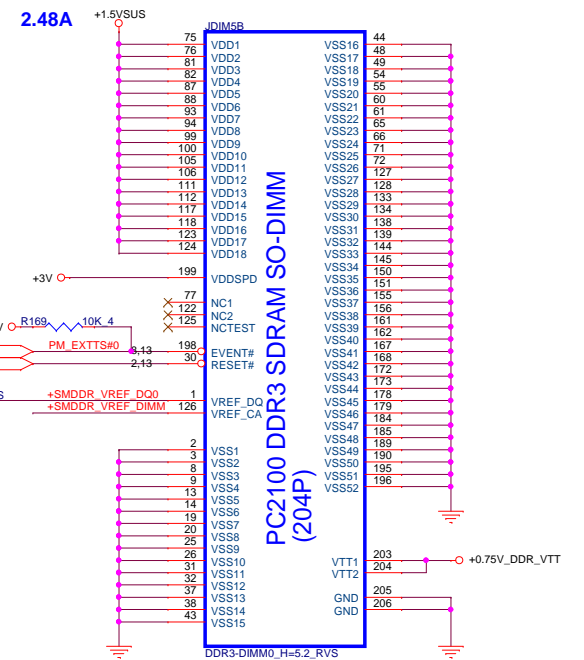
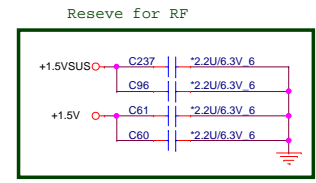


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	Quanta Computer Inc.		
	Size Custom	Document Number PCH 6/6 (GND)	
Date: Monday, October 22, 2012		Sheet 11 of 43	



PC2100 DDR3 SDRAM SO-DIMM (204P)

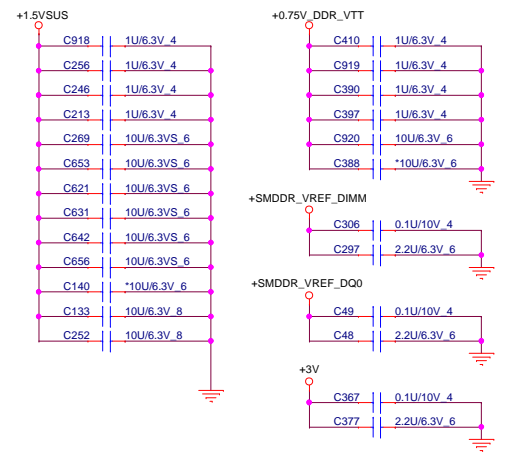
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 ddr-78279-001-rvs-204p
 DGMK4000278
 SOCKET DDR3 SODIMM(204P,H5.2,RVS)QBCON



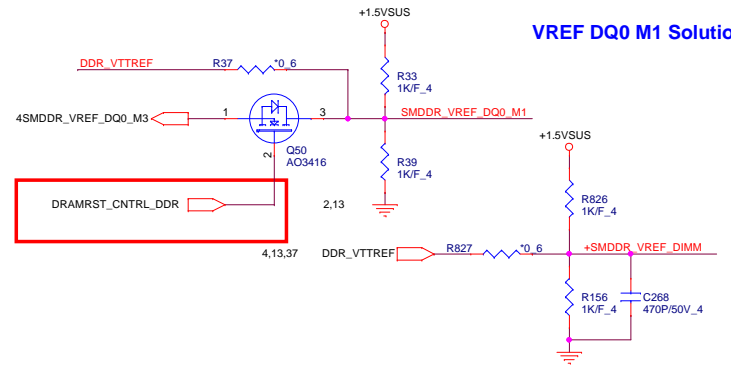
DDR3-DIMM0_H=5.2.RVS
 ddr-78279-001-rvs-204p
 DGMK4000278
 SOCKET DDR3 SODIMM(204P,H5.2,RVS)QBCON

- +1.5V → 4,10,27,33
- +0.75V_VTT → 3,37,39
- +1.5VSUS → 2,4,13,37,43
- +3VPCU → 5,7,25,30,31,33,34,35
- +3V → 2,6,7,8,9,10,13,14,23,24,25,26,27,29,30,31,32,33,36,39,40,42

Place these Caps near So-Dimm0.



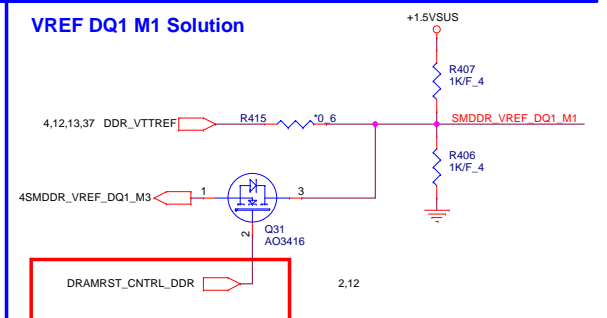
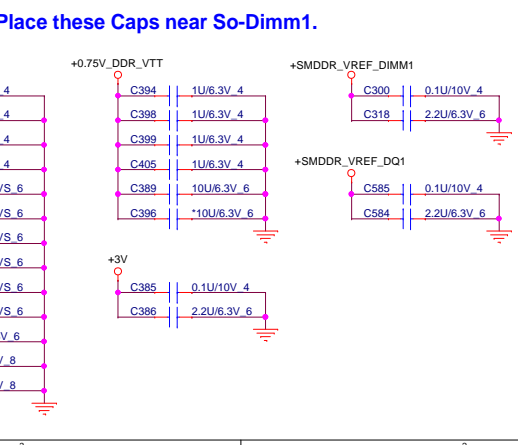
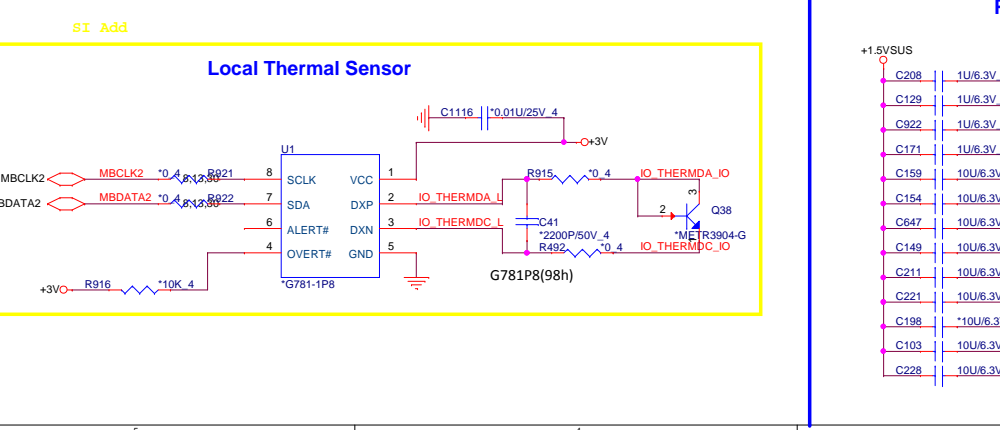
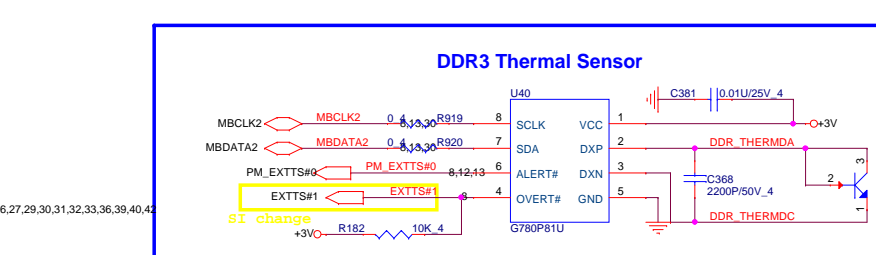
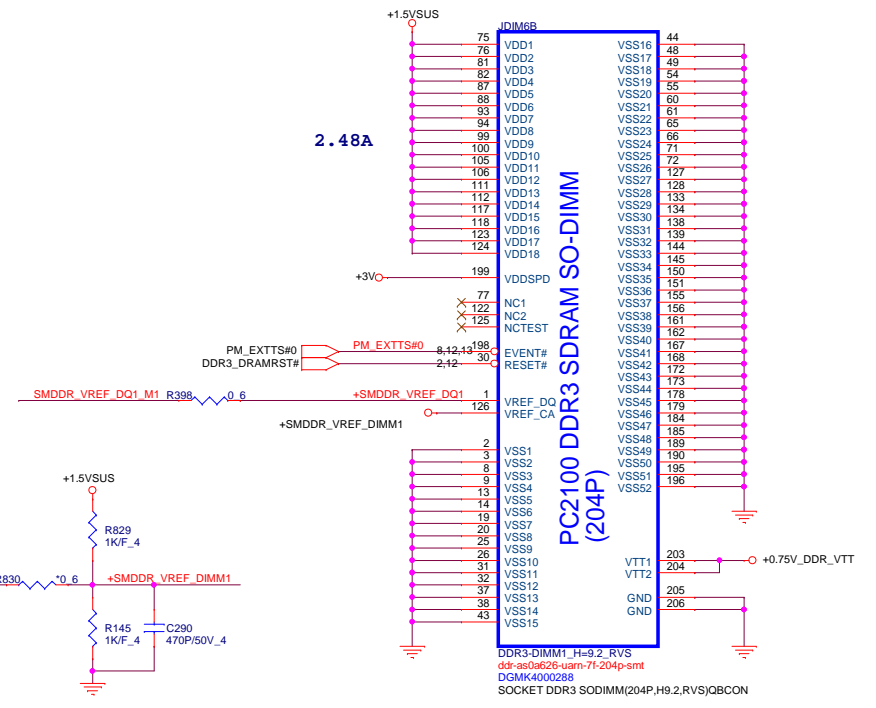
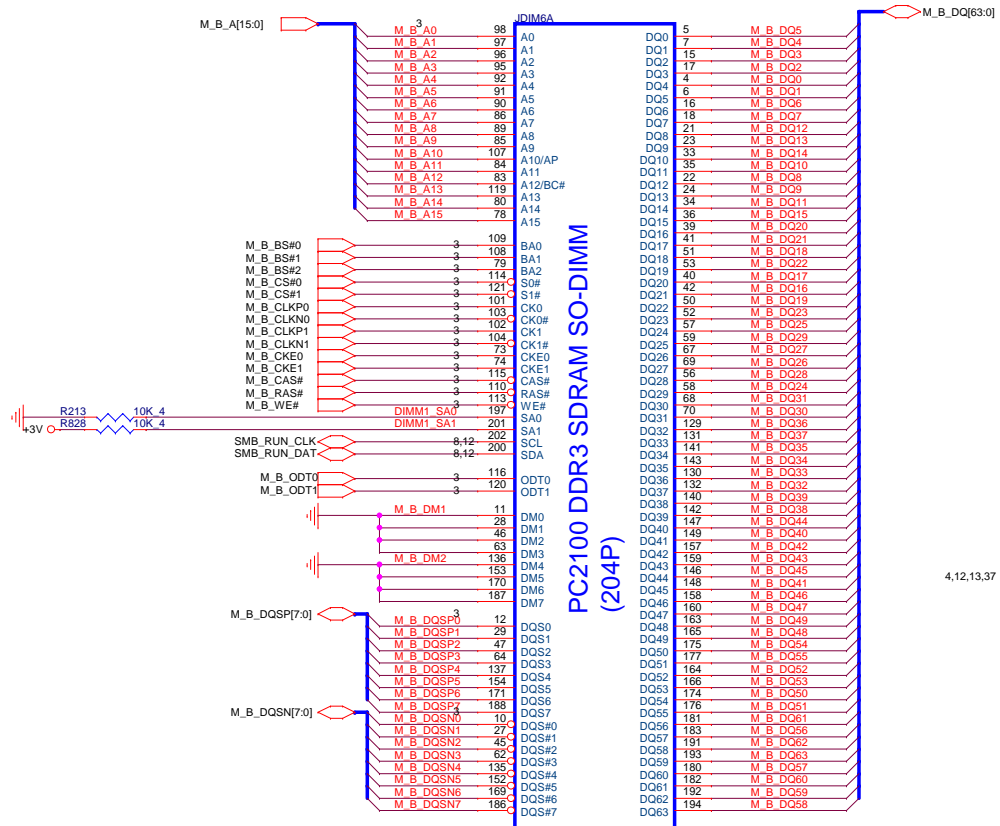
VREF DQ0 M1 Solution



PROJECT : R62
Quanta Computer Inc.

NBS

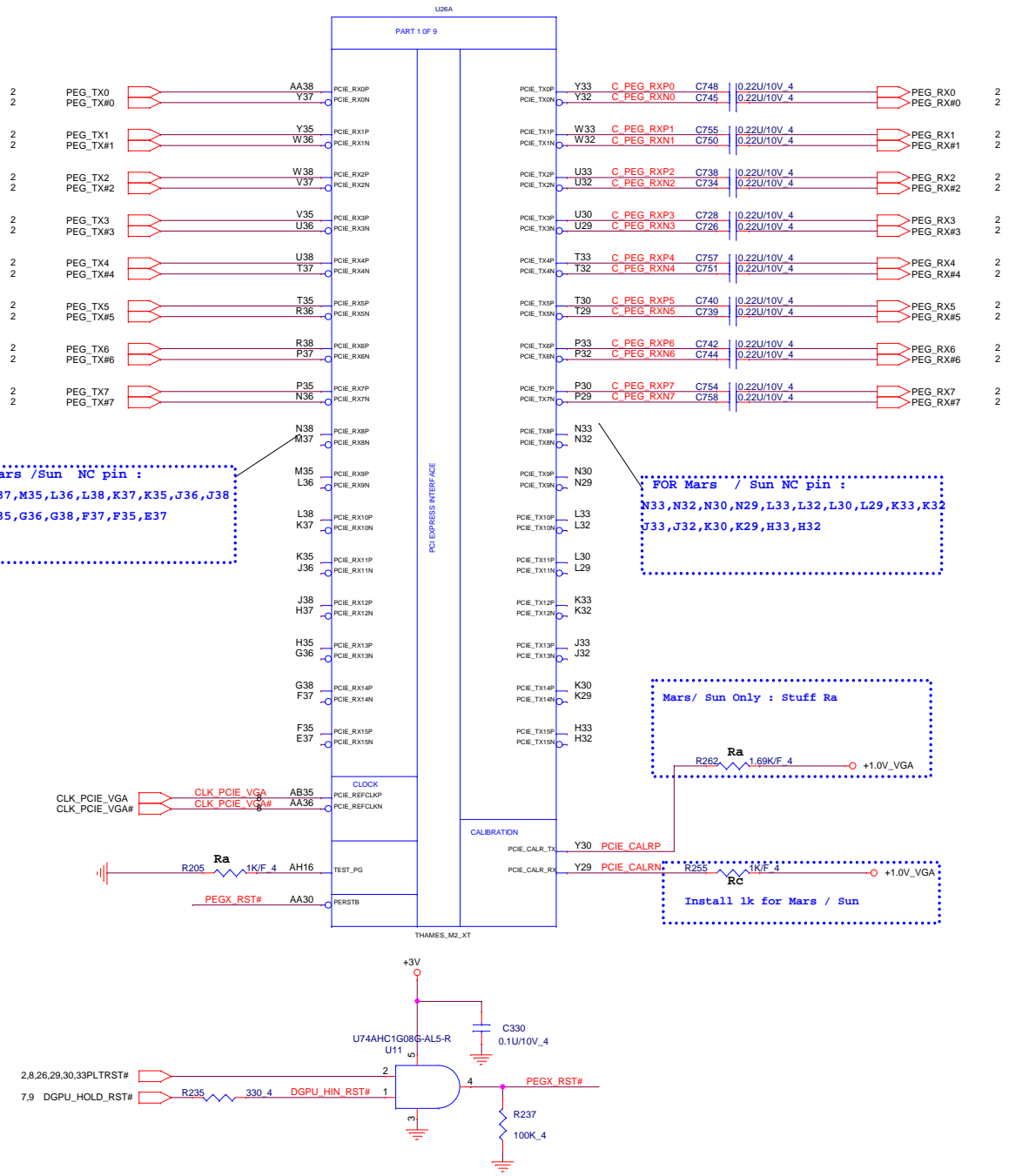
Size Custom	Document Number DDR3 DIMM0-RVS (5.2H)	Rev 1A
Date: Monday, October 22, 2012		Sheet 12 of 43



PROJECT : R62
Quanta Computer Inc.

NB5

Size Custom	Document Number DDR3 DIMM1-RVS (9.2H)	Rev 1A
Date: Monday, October 22, 2012		Sheet 13 of 43



For Mars /Sun NC pin :
 N38, M37, M35, L36, L38, K37, K35, J36, J38
 H37, H35, G36, G38, F37, F35, E37

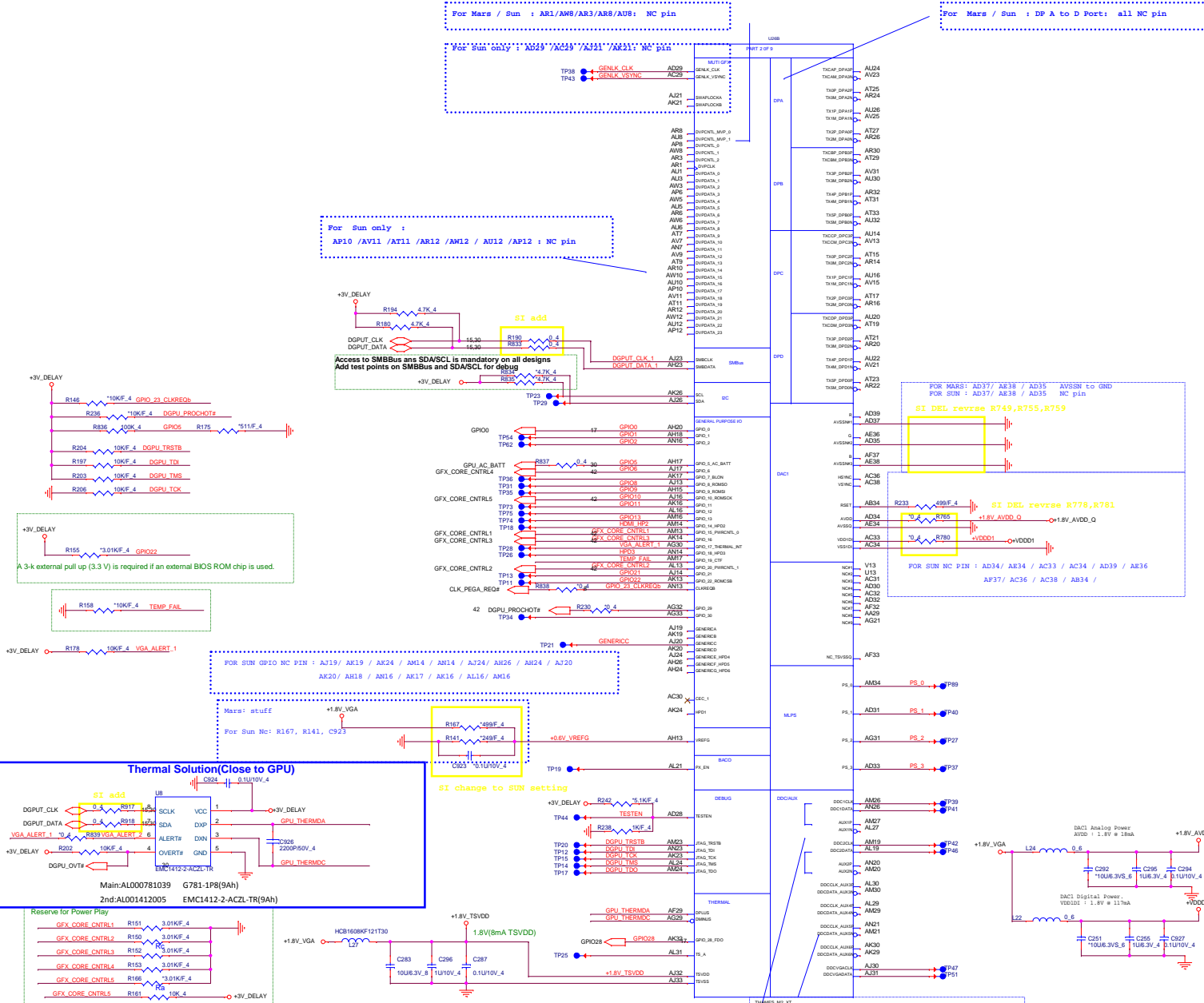
FOR Mars / Sun NC pin :
 N33, N32, N30, N29, L33, L32, L30, L29, K33, K32
 J33, J32, K30, K29, H33, H32

Mars/ Sun Only : Stuff Ra

Install 1k for Mars / Sun

2,6,7,8,9,10,14,21,23,24,25,26,27,29,30,31,32,33,36,39,40,42
 16,18,19,43 +1.0V_VGA

	PROJECT : R62 Quanta Computer Inc.		Rev 1A
	Size Custom	Document Number THAMES_PCIE_Interface	
	Date: Monday, October 22, 2012		Sheet 14 of 43



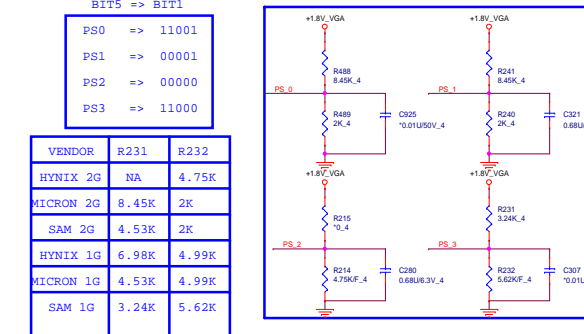
MLPS Implementation

- Connect GPIO_28 to 10K pulldown to enable MLPS
- If any of PS_0/1/2/3 is not used, leave "no connect"
- R_pu, R_pd and C must be properly populated per tables below
- Place MLPS circuit components as close to the ASIC as possible
- Total DC resistance of trace between PS pin and C should be less than 2 ohms
- Total DC resistance of trace between PS pin and C and ground should be less than 2 ohms
- Trace capacitance should be less than 100pF. Resistors should be of +/-1% tolerance

C (nF)	Bits(5,4)
680	00
82	01
10	10
NC	11

R_pu (Ohm)	R_pd (Ohm)	Bits(3,2,1)
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

Pin/Bit	Name	Description	Default	Legacy
PS_0[3:1]	romidg[2:0]	Memory aperture size or ROM type select: If bios_rom_en = 0, romidg[2:0] define memory aperture size. If bios_rom_en = 1, romidg[2:0] define ROM type	xxx	gpio_13, gpio_12, gpio_11
PS_0[4]	n/a	Reserved		1
PS_1[1]	bif_gen3_en_a	PCIe Gen3 capability: 1=Gen3 supported, 0=Gen3 not supported	x	gpio_2
PS_1[2]	bif_clk_pm_en	PCIe CLK PM capability: 1 = CLKREQ supported	x	gpio_8
PS_1[3]	n/a	Reserved		gpio_10
PS_1[4]	tx_pwr_enb	PCIe Tx power savings: 0=50% swing, 1=full swing	x	gpio_0
PS_1[5]	tx_deemph_en	PCIe Tx de-emphasis: 1=1x de-emphasis enabled	x	gpio_1
PS_2[1]	n/a	Reserved		n/a
PS_2[2]	n/a	Reserved		n/a
PS_2[3]	bios_rom_en	Enable external BIOS ROM: 1=External ROM connected	x	gpio_22
PS_2[5]	vga_ds	VGA disable: 1=Disable this GPU as the system's VGA controller	0	gpio_9
PS_2[5]	n/a	Reserved		n/a
PS_3[1]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[2]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[3]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[5]	aud_port_ep[2:0]	3-bit field indicating number of audio-capable display outputs	xxx	n/a



For Mars: Stuff Ra, Rc=> VDDC 1.1V

For Mars / Sun:nc pin
AL30, AM30, AL29, AM29, AN21, AM21, AK30, AK29

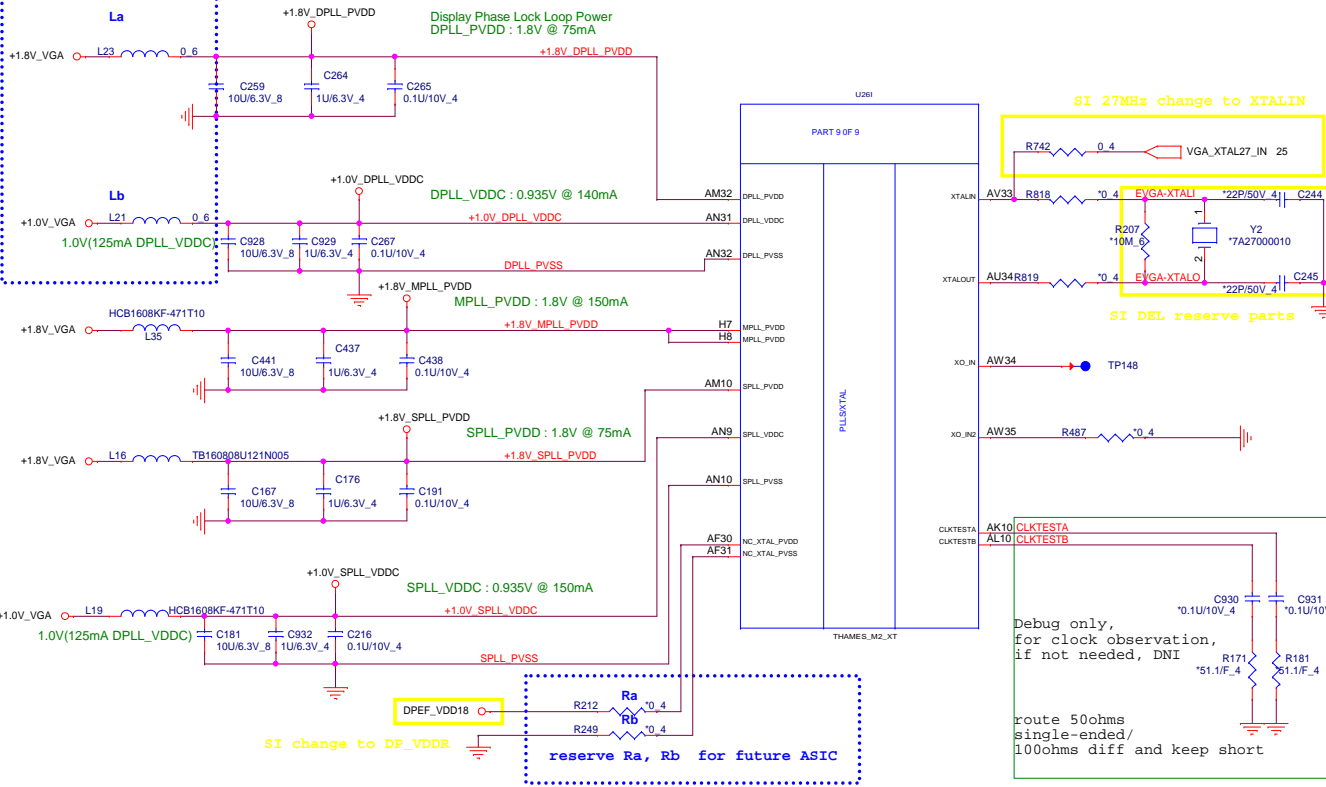
For Sun Only :nc pin
AL27, AM27, AM20, AN20, AM26, AM26, AL19, AM19, AJ30, AJ31

PS3 BIT3==>BIT1	ID	Memory Type	Configuration	PN	Channel Size	
000	0	Hynix	H5TC4G63AFR-11C	256Mx16 *4 pcses	AKD5PGWTW08 IC SDRAM/96PH5TC4G63AFR-11C	2G
001	1	Micron	MT41J256M10HA-093GE	256Mx16 *4 pcses	AKD5PZ3TL01 IC SDRAM/96PMT41J256M10HA-093GE	2G
010	2	Samsung	K4W4G1646B-HC1A	256Mx16 *4 pcses	AKD5PZDT501 IC SDRAM/96PK4W4G1646B-HC1A	2G
011	3	Hynix	H5TC2G63FR-11C	128Mx16 *4 pcses	AKD5MZTW03 IC SDRAM/96PH5TC2G63FR-11C	1G
100	4	Micron	MT41L128M16JT-093CE	128Mx16 *4 pcses	AKD5MGTW08 IC SDRAM/96PK41L128M16JT-093CE	1G
101	5	Samsung	K4W2G1646E-BC1A	128Mx16 *4 pcses	AKD5MGT535 IC SDRAM/96PK4W2G1646E-BC1A	1G



Memory Type	
DDR3	27-MHz (± 30 ppm) crystal connected to XTALIN/XTALOUT, or 27-MHz (1.8 V) oscillator connected to XTALIN.
GDDR5	27-MHz (3.3 V) oscillator connected to XO_IN, and 100-MHz (3.3 V) oscillator connected to XO_IN2. (By default, this clock should not be spread since internal spreading is used.)

Fo Mars/ Sun
Change La, Lb
Bead to 0 ohm



SI 27MHz change to XTALIN

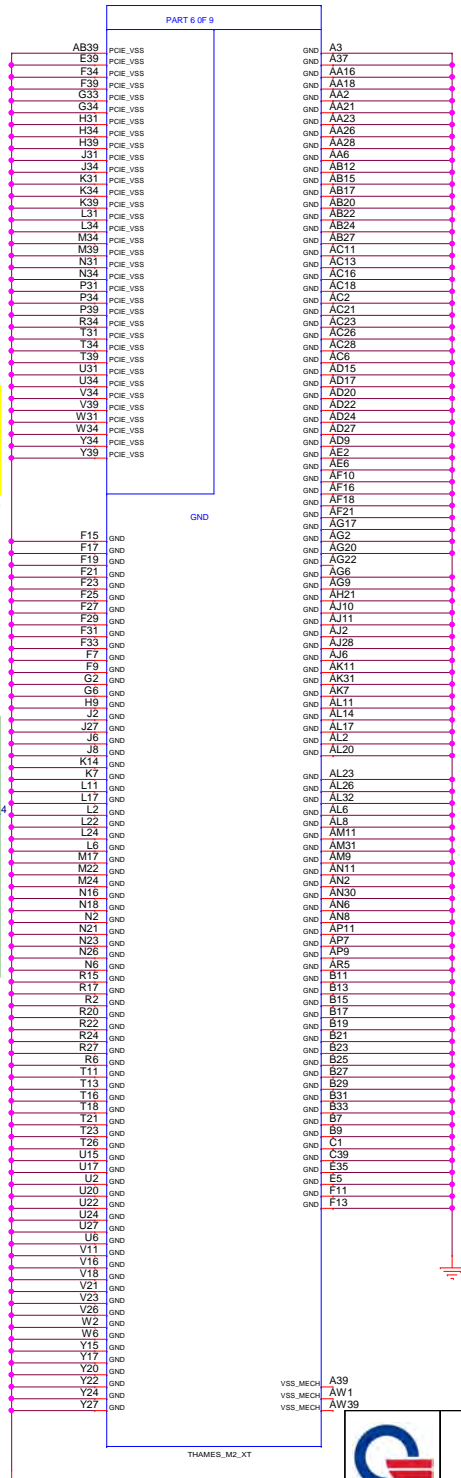
SI DEL reserve parts

Debug only,
for clock observation,
if not needed, DNI

route 50ohms
single-ended/
100ohms diff and keep short

DPEF_VDD18

reserve Ra, Rb for future ASIC



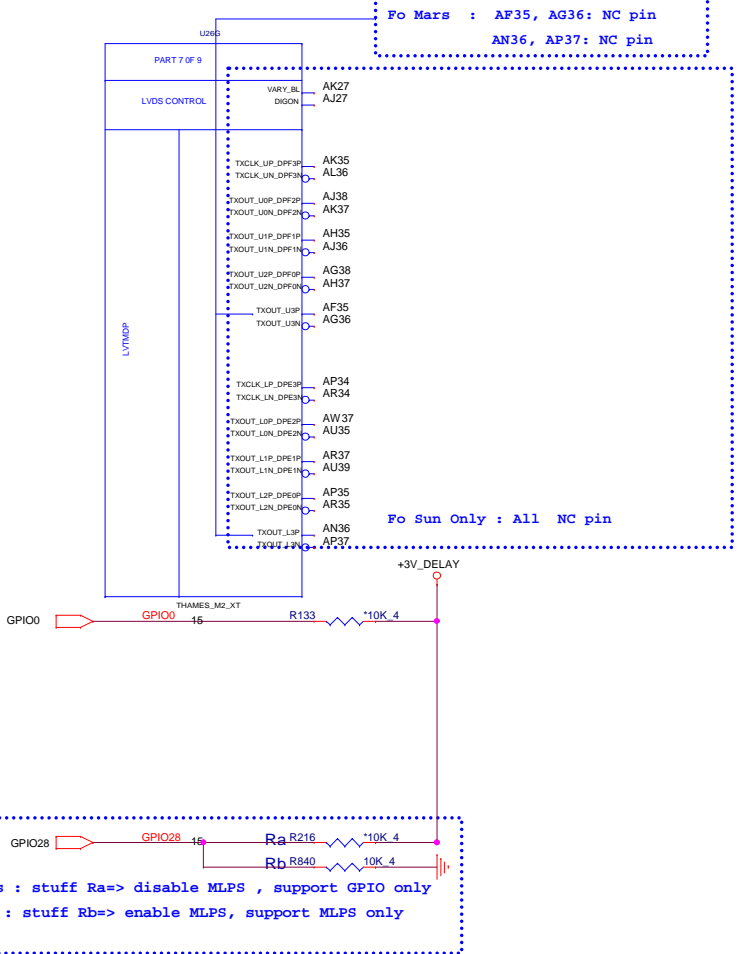
AG22 is nc pin

14,18,19,43 +1.0V_VGA

15,18,19,25,42 +1.8V_VGA



PROJECT : R62
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CONFIGURATION STRAPS -- SEE EACH DATABOOK FOR STRAP DETAILS
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

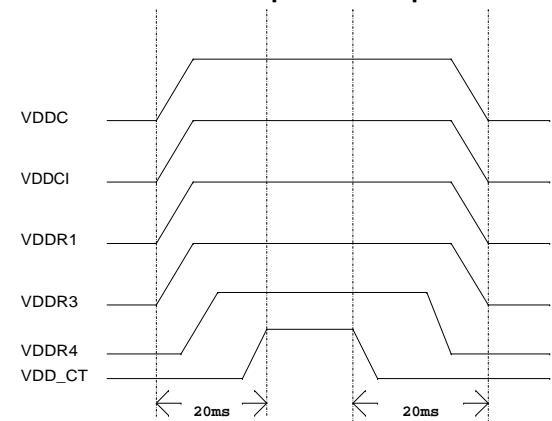
STRAPS	MLPS	GPIO PIN	DESCRIPTION OF DEFAULT SETTINGS	Default Setting
MLPS_DISABLE	NA	GPIO_28_FDO	Enable MLPS, NA for Thames/Whistler/Seymour 0: Enable MLPS, disable GPIO PINSTRAP 1: Disable MLPS, enable GPIO PINSTRAP	X
TX_PWRS_ENB	PS_1[4]	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	X
TX_DEEMPH_EN	PS_1[5]	GPIO1	PCIe Transmitter De-emphasis Enable 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled	X
BIF_GEN3_EN_A	PS_1[1]	GPIO2	PCIe Gen3 Enable (NOTE: RESERVED for Thames/Whistler/Seymour) 0: GEN3 not supported at power-on 1: GEN3 supported at power-on	1
BIF_VGA DIS	PS_2[4]	GPIO9	VGA Control 0: VGA controller capacity enabled 1: VGA controller capacity disabled (for multi-GPU)	0
ROMIDCFG[2:0]	PS_0[3..1]	GPIO[13:11]	Serial ROM type or Memory Aperture Size Select If GPIO22 = 0, defines memory aperture size If GPIO22 = 1, defines ROM type 100 - 512Kbit M25P05A (ST) 101 - 1Mbit M25P05A (ST) 101 - 2Mbit M25P20 (ST) 101 - 4Mbit M25P40 (ST) 101 - 8Mbit M25P80 (ST) 100 - 512Kbit Pm25LV512 (Chingis) 101 - 1Mbit Pm25LV010 (Chingis)	XXX
BIOS_ROM_EN	PS_2[3]	GPIO22	Enable external BIOS ROM device 0: Disabled 1: Enabled	X
AUD[1] AUD[0]	NA NA	HSYNC VSYNC	00 - No audio function 01 - Audio for DP only 10 - Audio for DP and HDMI if dongle is detected 11 - Audio for both DP and HDMI HDMI must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature.	XX
CEC_DIS	PS_0[4]	GENLK_VSYNC	Enable CEC function. Reserved for Thames/Whistler/Seymour 0: Disabled 1: Enabled	X
RESERVED RESERVED RESERVED RESERVED	PS_1[3] PS_1[2] NA NA	GENLK_CLK GPIO8 GPIO21 GENERICC	Reserved Reserved Reserved Reserved (for Thames/Whistler/Seymour only)	0 0 0 0
AUD_PORT_CONN_PINSTRAP[2] AUD_PORT_CONN_PINSTRAP[1] AUD_PORT_CONN_PINSTRAP[0]	PS_3[5] PS_3[4] PS_0[5]	NA NA NA	STRAPS TO INDICATE THE NUMBER OF AUDIO CAPABLE DISPLAY OUTPUTS 111 = 0 usable endpoints 110 = 1 usable endpoints 101 = 2 usable endpoints 100 = 3 usable endpoints 011 = 4 usable endpoints 010 = 5 usable endpoints 001 = 6 usable endpoints 000 = all endpoints are usable	XXX

Memory Aperture size

GPIO9		GPIO13	GPIO12	GPIO11	
BIOSROM		ROMIDCFG2	ROMIDCFG1	ROMIDCFG0	
0	128M	0	0	0	+VGA_CORE
0	256M	0	0	1	+VGA_CORE
0	64M	0	1	0	+1.5V_VGA
0	32M	0	1	1	+1.5V_VGA
0	512M	1	0	0	+3.3V_Delay
0	1G	1	0	1	+1.8V_VGA
0	2G	1	1	0	+1.8V_VGA
0	4G	1	1	1	+1.8V_VGA

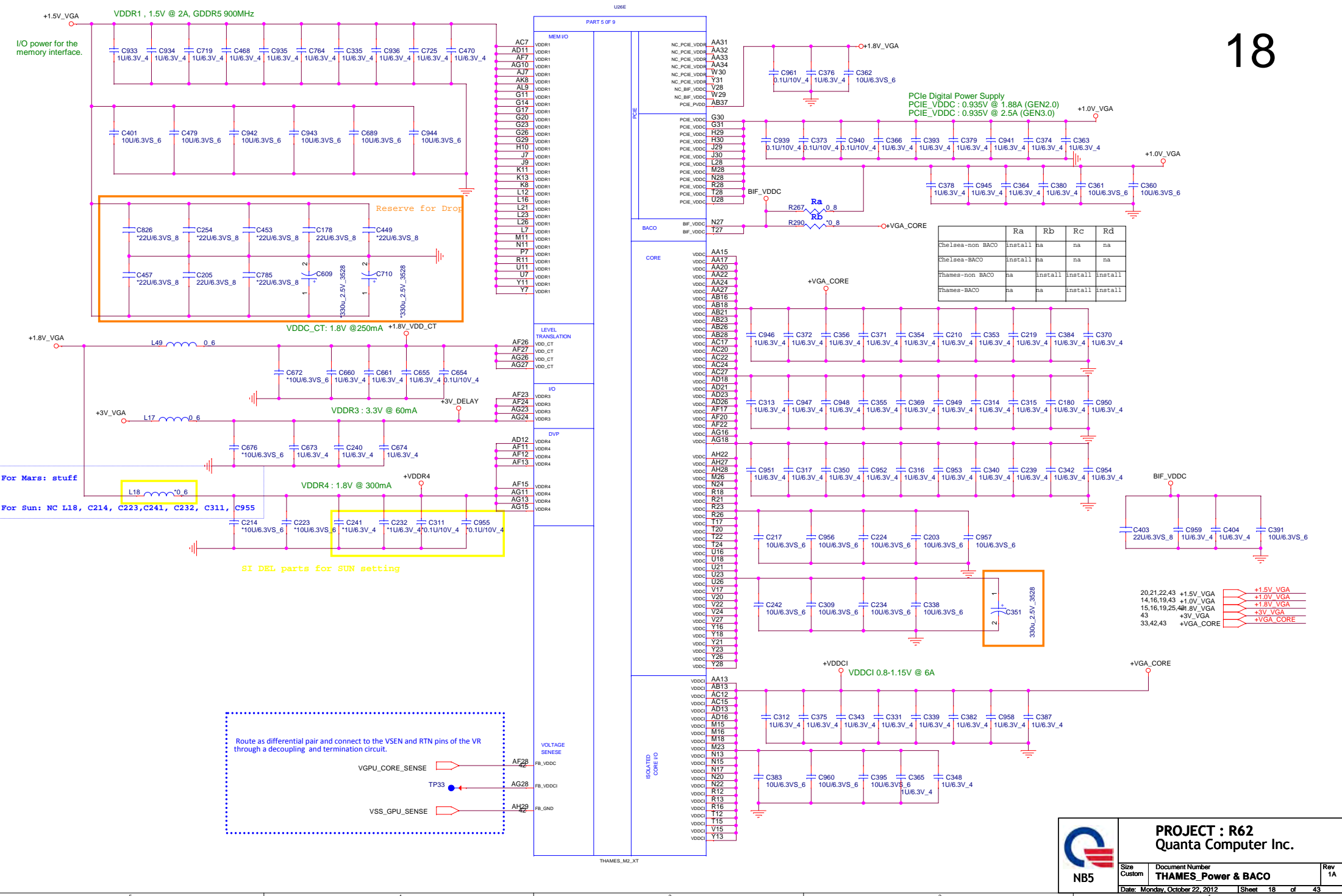
It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.

Power Up/Down Sequence



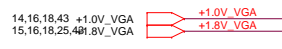
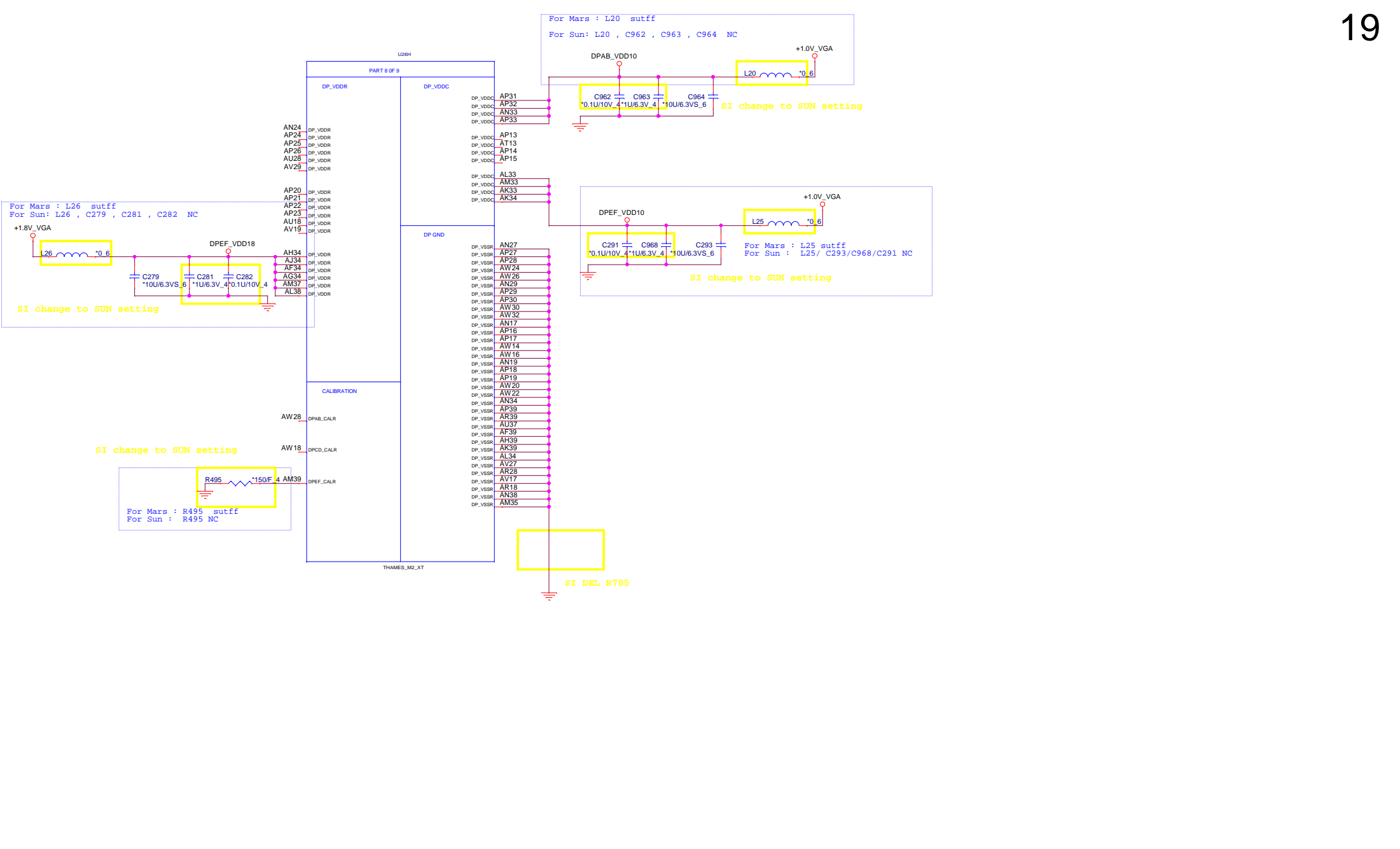
PROJECT : R62
Quanta Computer Inc.


Size Custom	Document Number THAMES_LVDS / STRAP	Rev 1A
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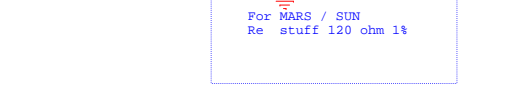
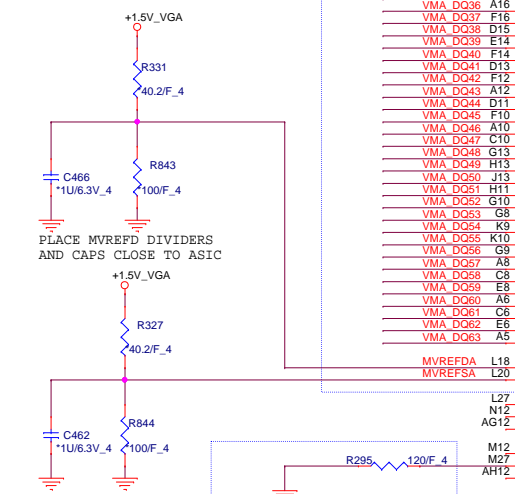
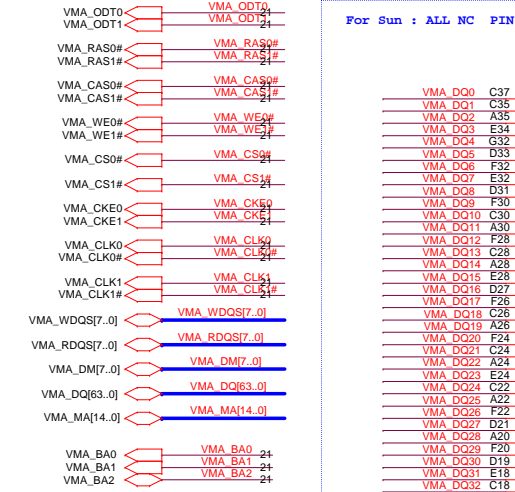


PROJECT : R62
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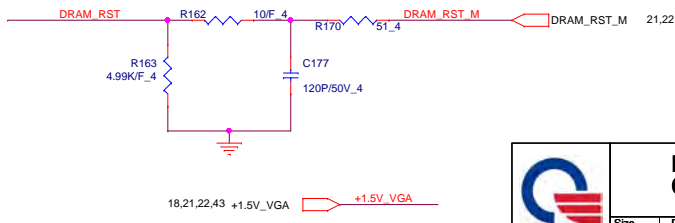
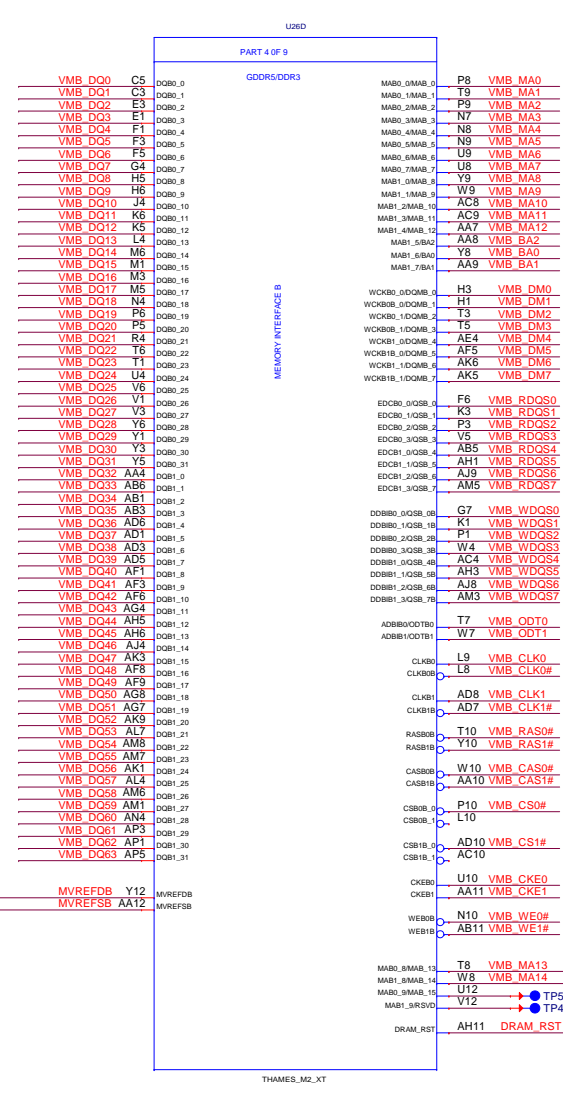
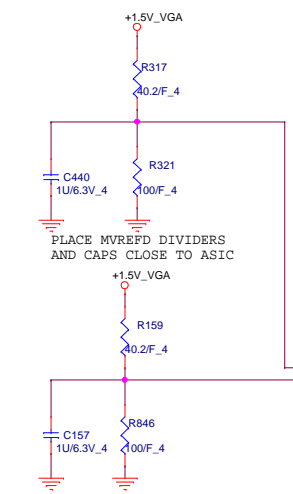
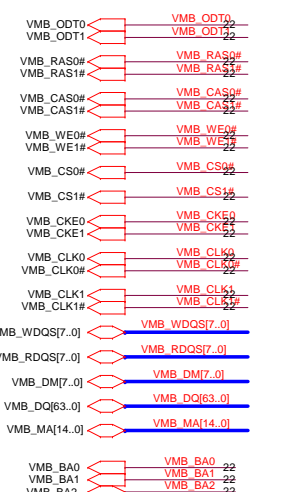
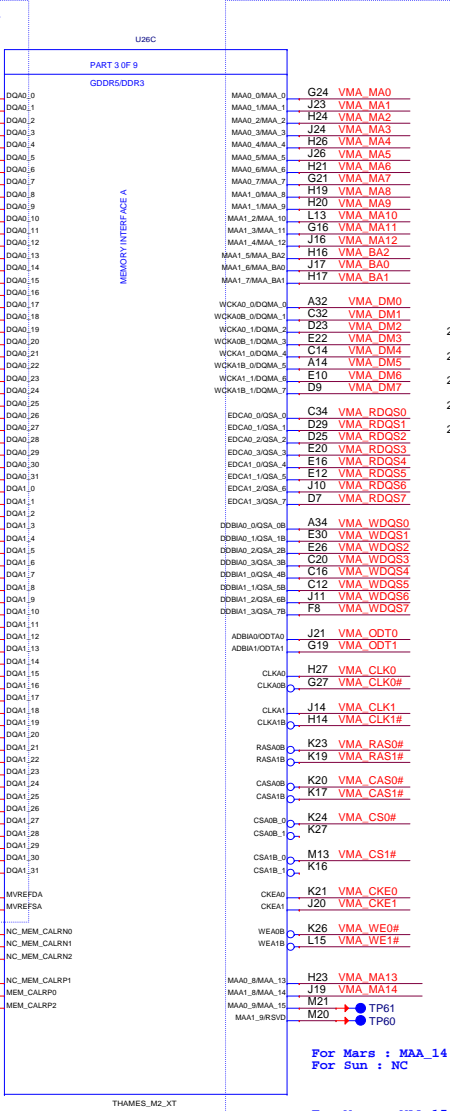
Size Custom	Document Number THAMES_Power & BACO	Rev 1A
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	PROJECT : R62 Quanta Computer Inc.		
	Size Custom	Document Number THAMES_DP Powers	Rev 1A
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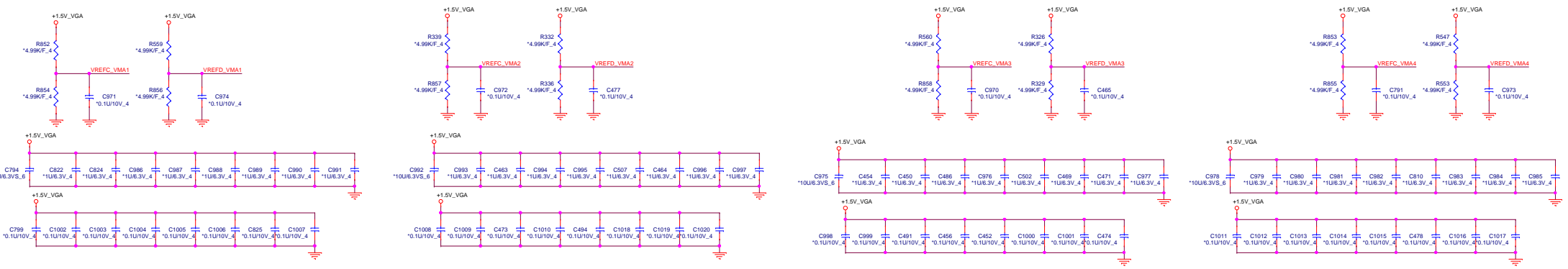
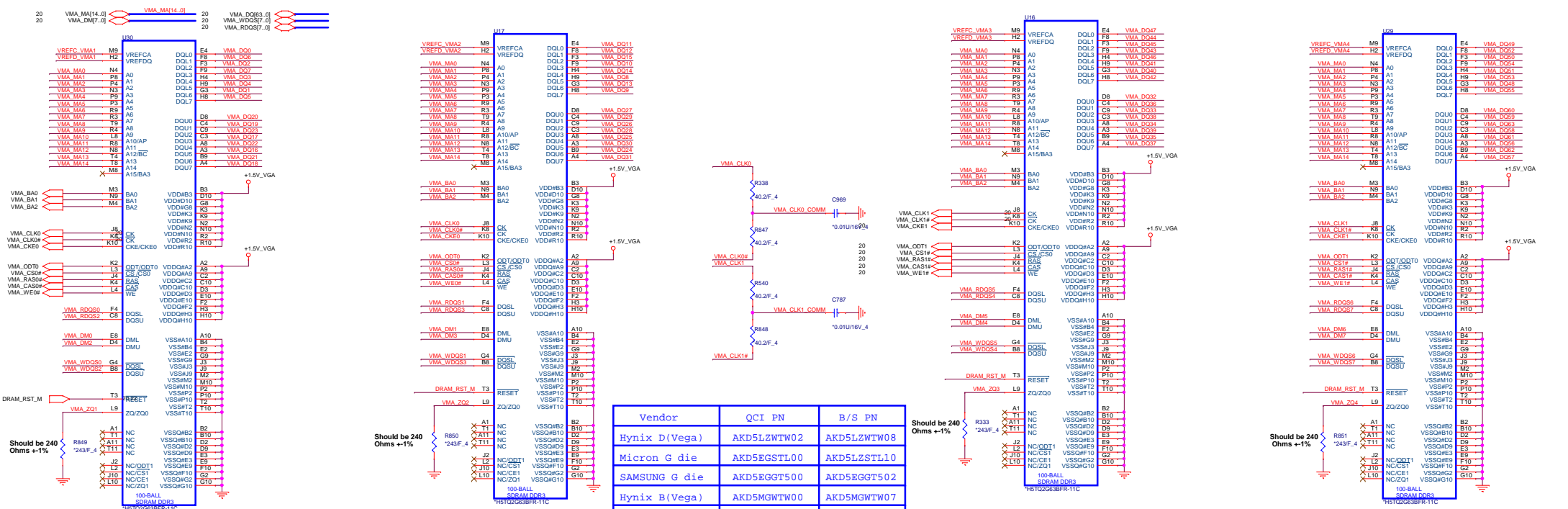
For Sun : ALL NC PIN



PROJECT : R62
Quanta Computer Inc.

Size Custom Document Number THAMES_MEM_Interface Rev 1A
 Date: Monday, October 22, 2012 Sheet 20 of 43

CHANNEL A: 256MB/512MB DDR3

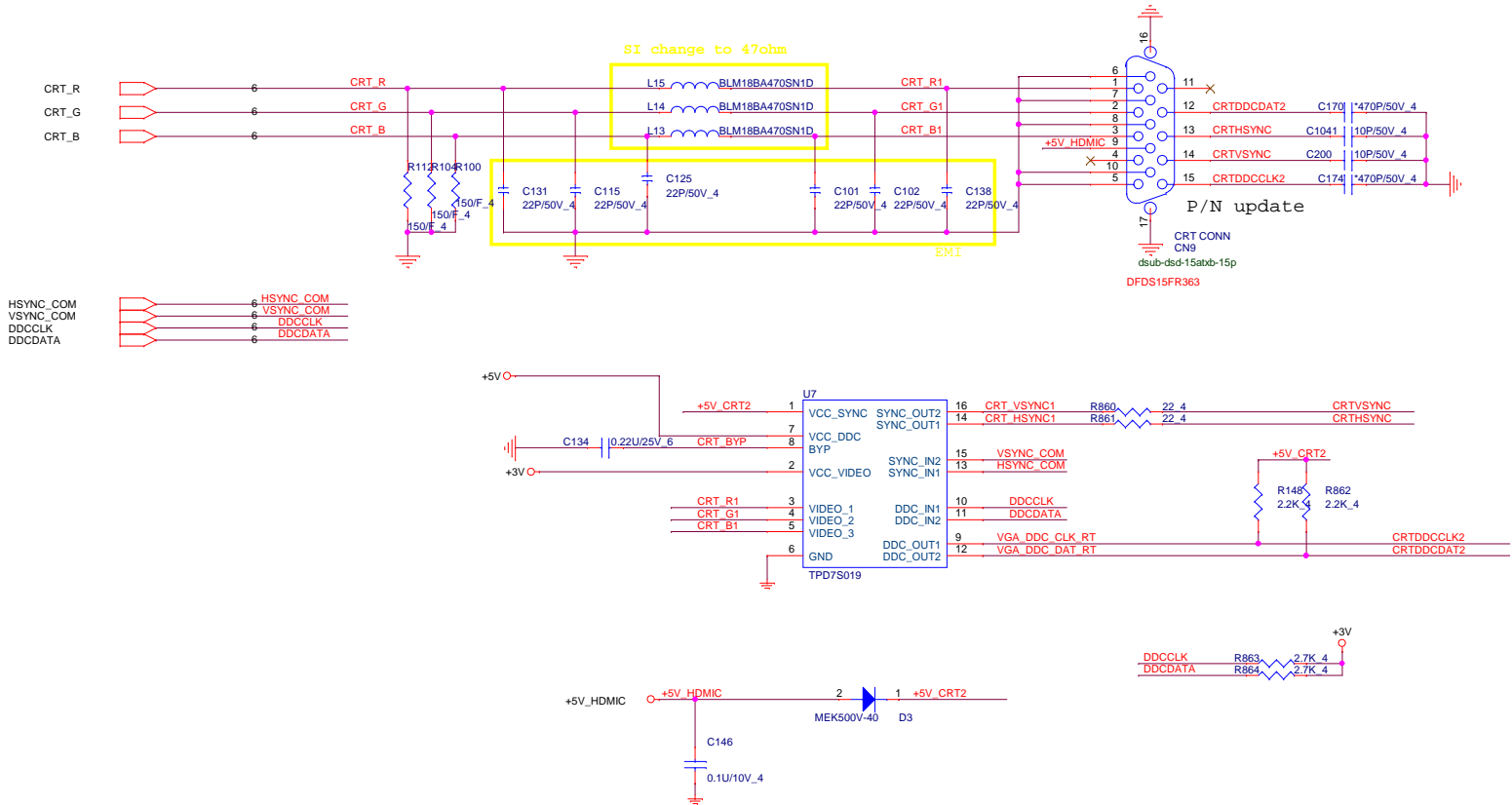


18.20.22.43 +1.5V_VGA

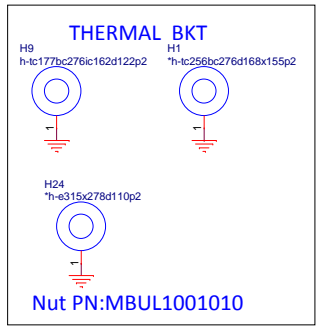
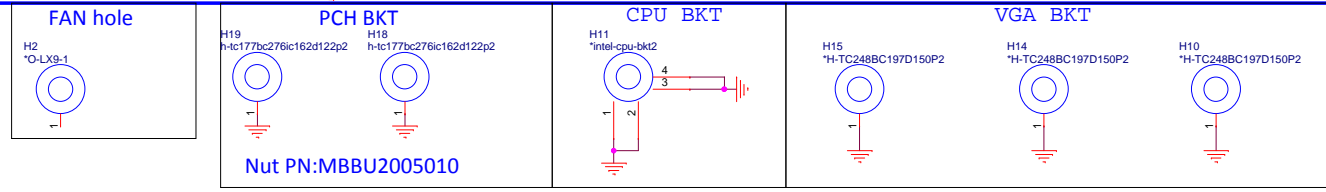
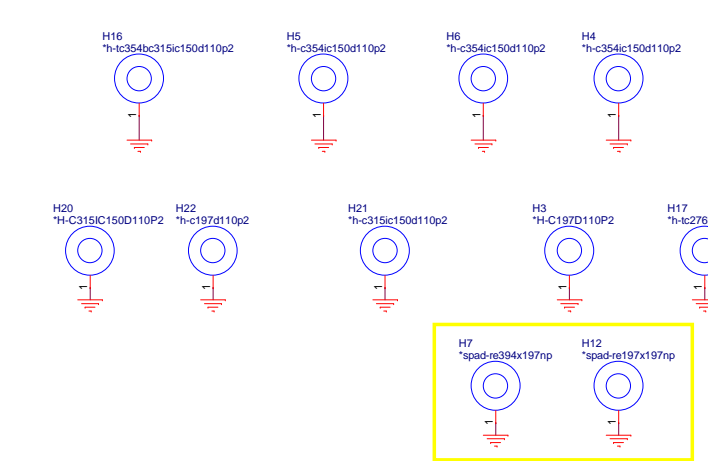
PROJECT : R62
Quanta Computer Inc.

Size: Custom
 Document Number: VRAM-A (DDR3 BGA96)
 Date: Monday, October 22, 2012 | Sheet 21 of 3A

7,10,25,27,31,33,33.39
2,6,7,8,9,10,12,15,14,24,25
25
+5V_HDMIC

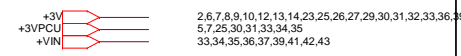
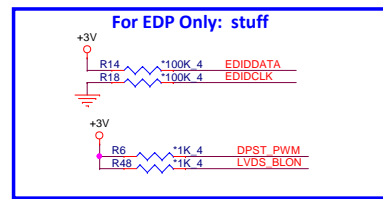
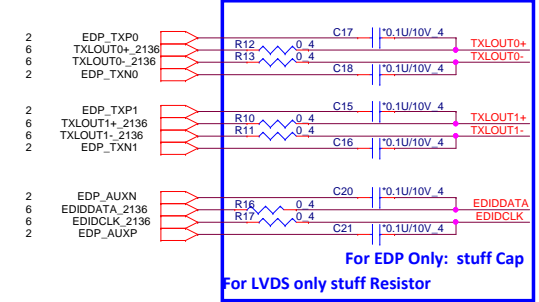
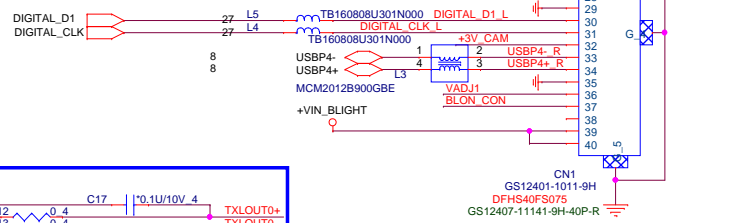
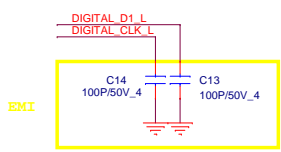
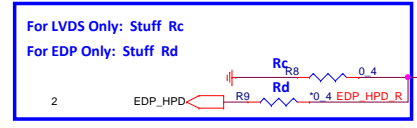
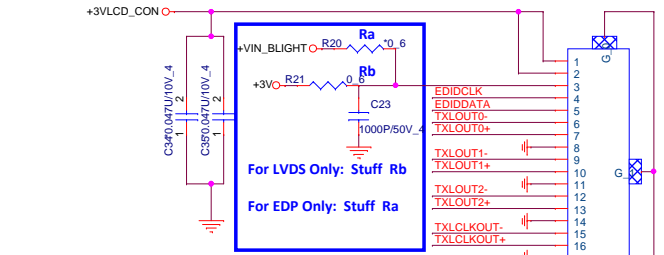
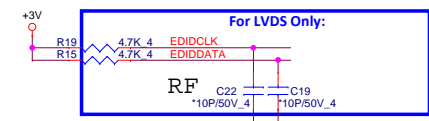
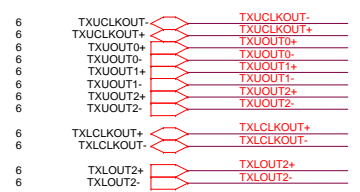
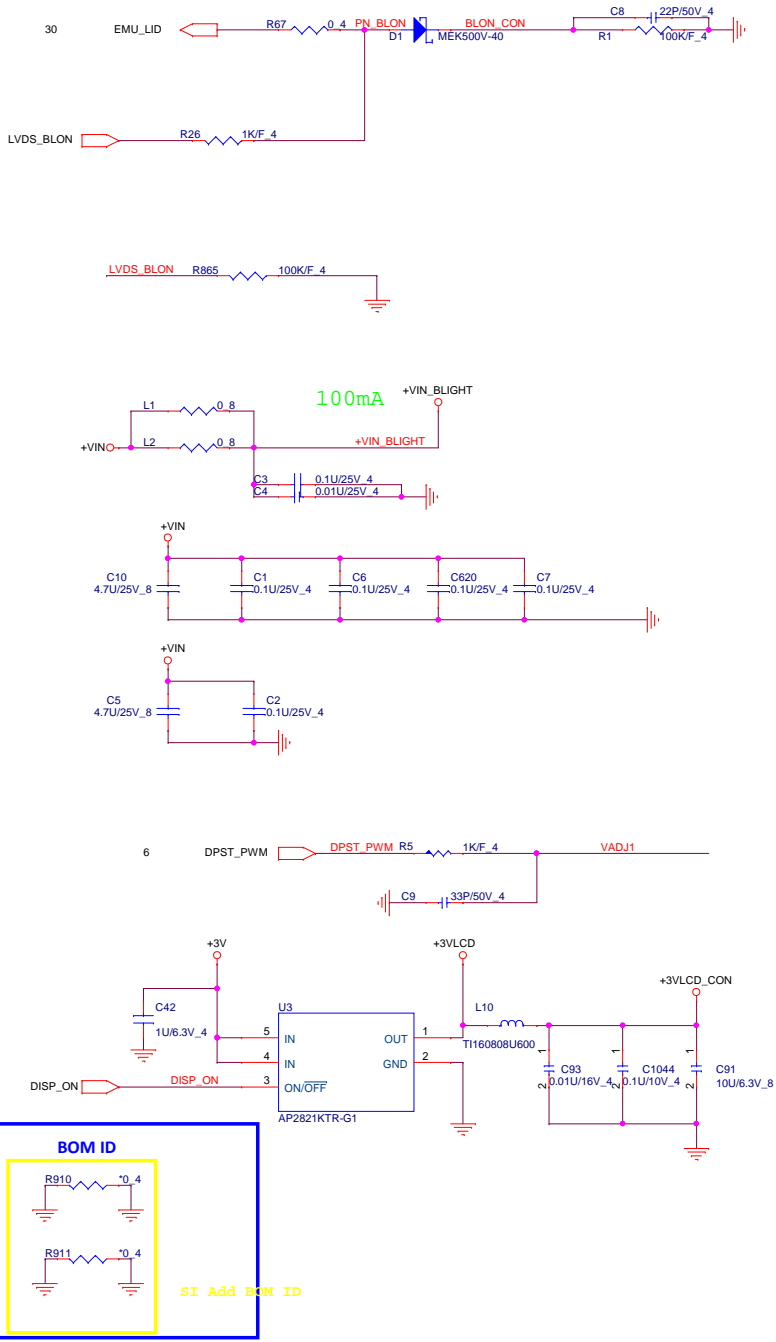


HOLE



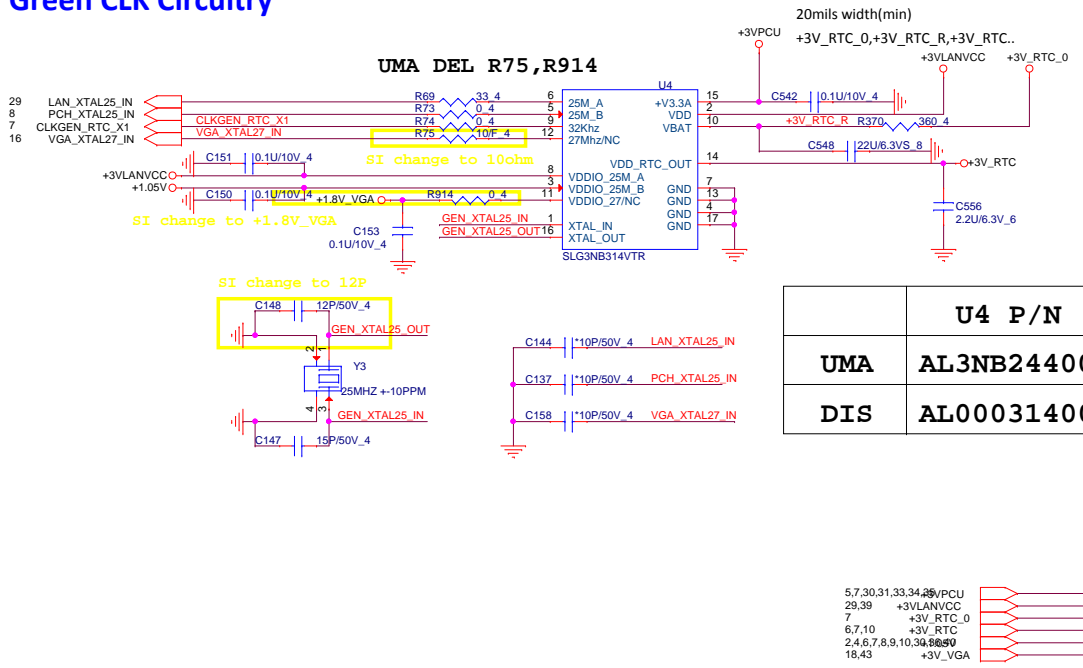
	PROJECT : R62 Quanta Computer Inc.		
	Size Custom	Document Number CRT,Hole	Rev 1A
	Date: Monday, October 22, 2012		Sheet 23 of 43

LID Switch

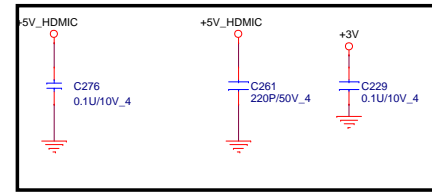


		PROJECT : R62		Rev 1A
		Quanta Computer Inc.		
Size Custom	Document Number LCD CONN/LID/CAM			
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Green CLK Circuitry

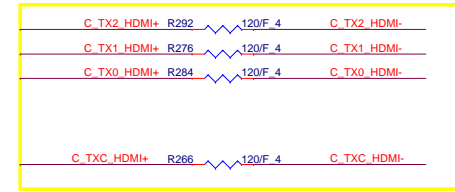


EMI request

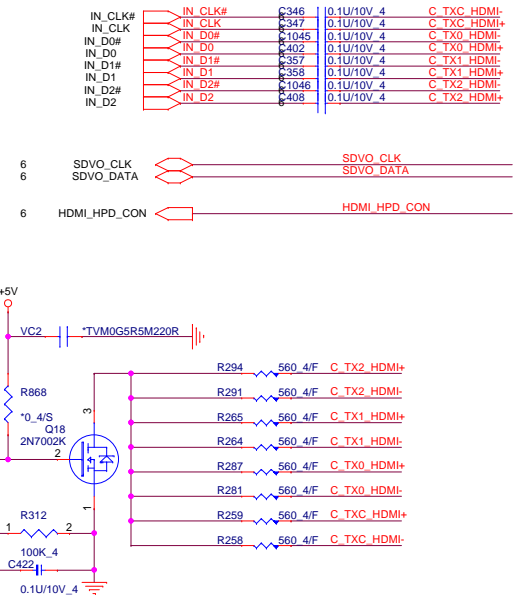


7,10,23,27,31,32,33,34,35,36,37,38,39,40,42
23 +5V_HDMIC
2,6,7,8,9,10,12,13,14,15,16,17,18,19,20,21,22,24,25,26,27,28,29,30,31,32,33,36,39,40,42

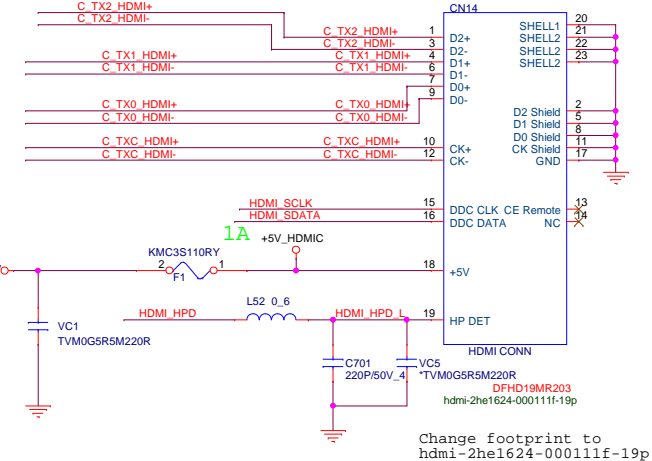
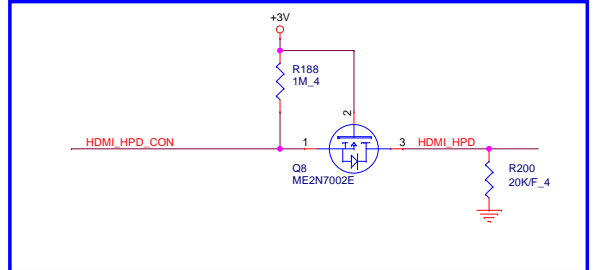
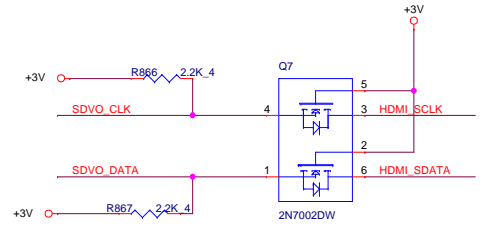
EMI request



close to HDMI conn



Close to HDMI Connector



Change footprint to hdmi-2he1624-000111f-19p

PROJECT : R62
Quanta Computer Inc.

Size Custom	Document Number HDMI CONN	Rev 1A
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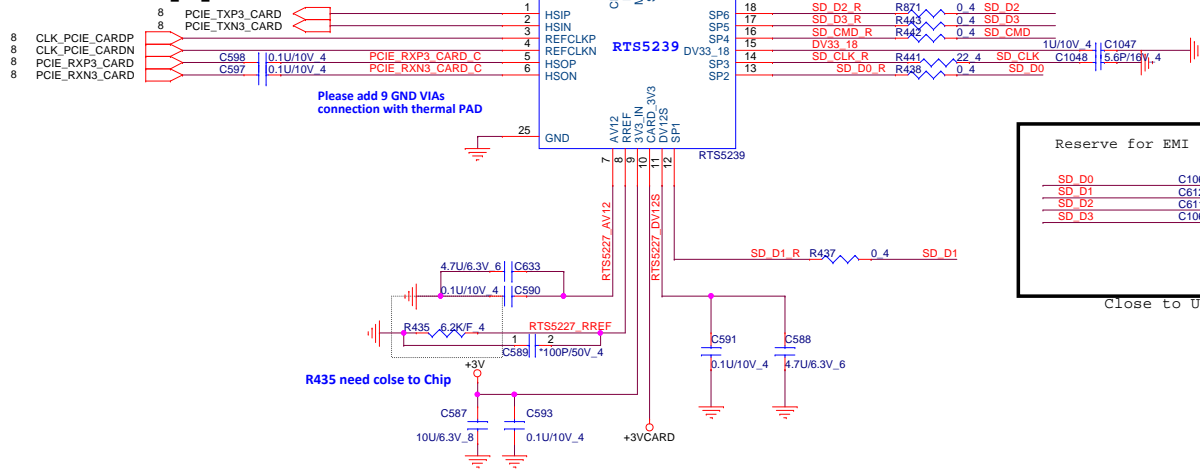
8 CLK_PCIE_REQ2# CLK_PCIE_REQ2# R446 0.4S CLK_PCIE_REQ2#_R

SP1	SD D1	
SP2	SD D0	MS D1
SP3	SD CLK	MS D0
SP4	SD CMD	MS D2
SP5	SD D3	MS D3
SP6	SD D2	MS CLK
SP7	SD_WP	MS_BS

Share Pin

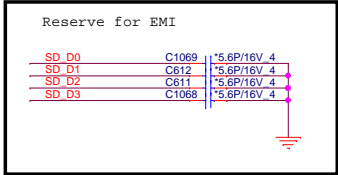
Close to chip pin

Close to chip pin



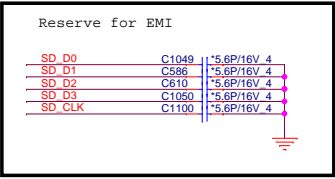
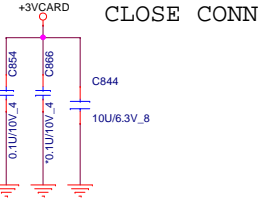
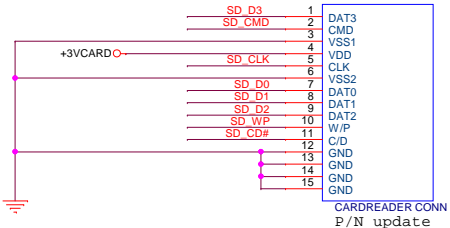
Please add 9 GND VIAs connection with thermal PAD

R435 need close to Chip



Close to U38

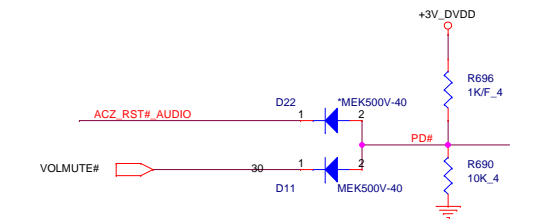
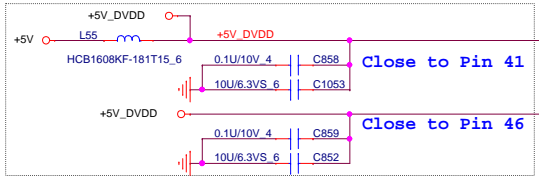
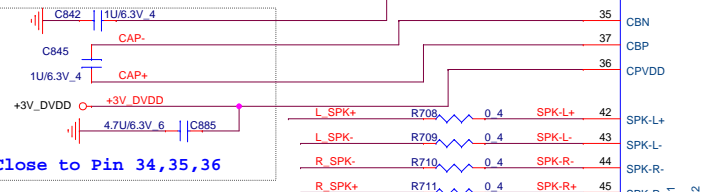
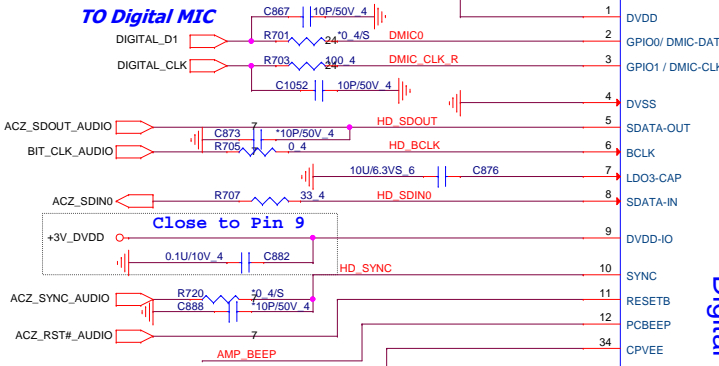
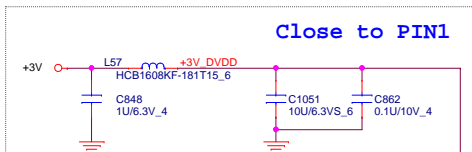
SD / MMC
CARD READER



Close to CN8

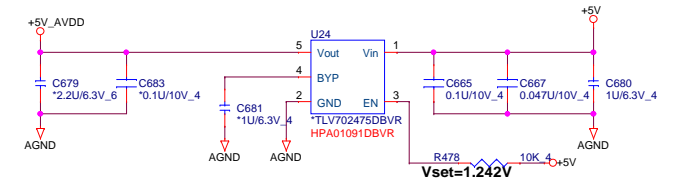
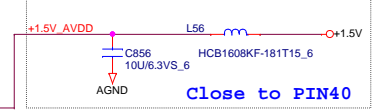
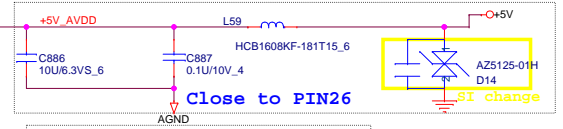
2,6,7,8,9,10,12,13,14,23,24,25,27,29,30,31,32,33,36,39,40,42

	PROJECT : R62 Quanta Computer Inc.		
	Size Custom	Document Number RTS5229 & CR SOCKET	Rev 1A
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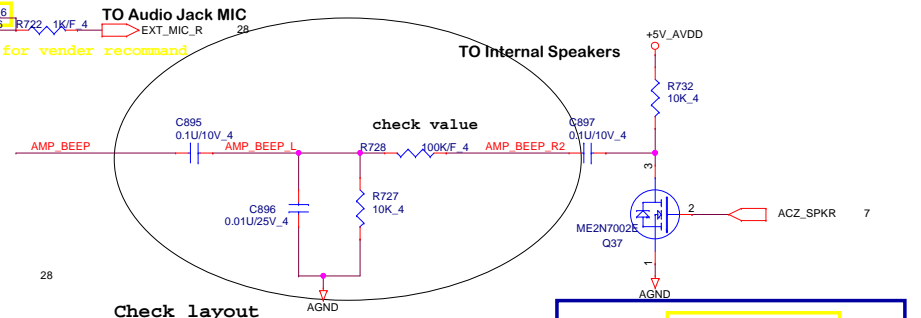
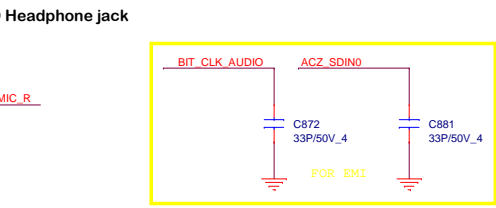
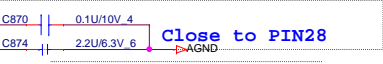
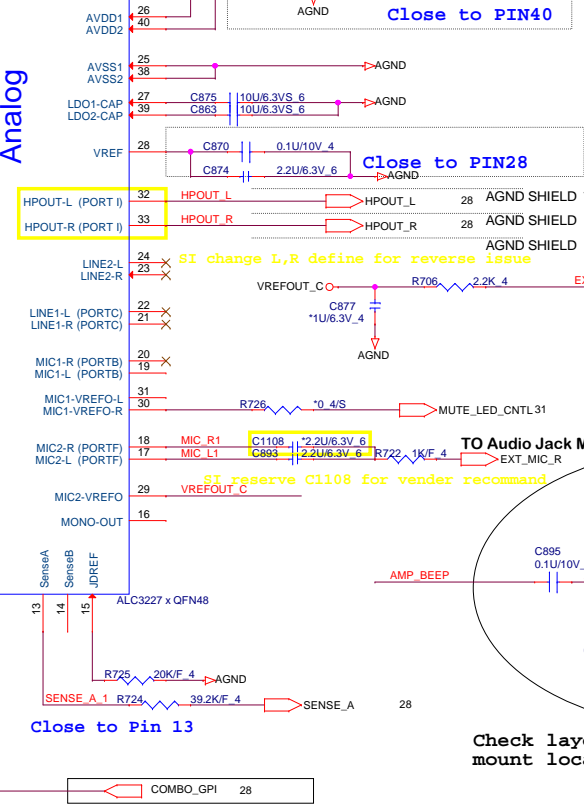
7,10,23,25,31,32,33,39 +5V
2,6,7,8,9,10,12,13,14,23,24,25,29,30,31,32,33,36,39,40,42
4,10,12,33 +1.5V

>40mils trace

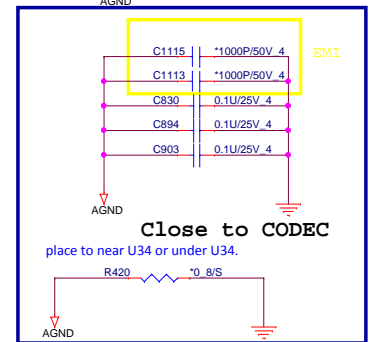
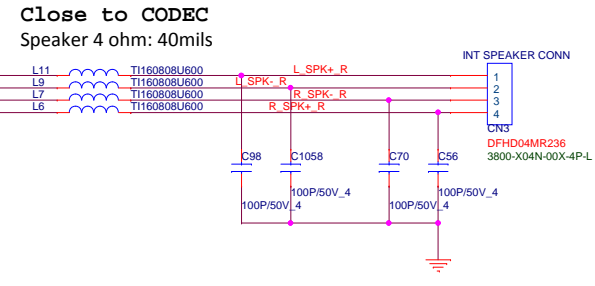


Analog

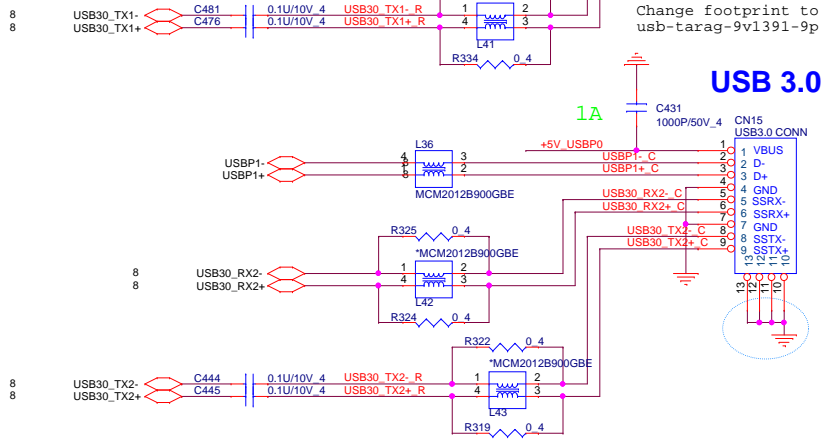
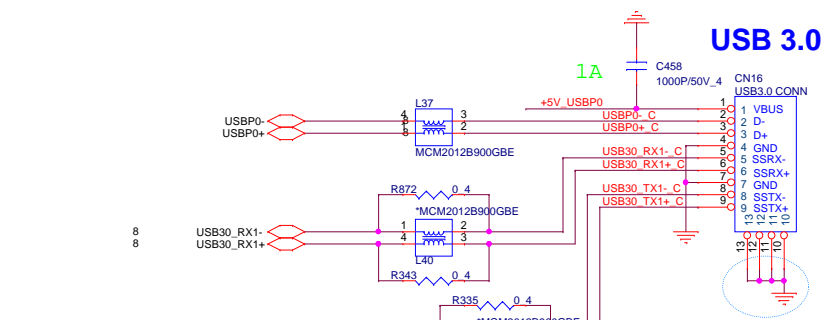
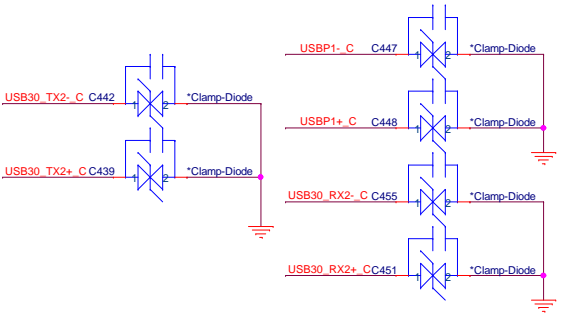
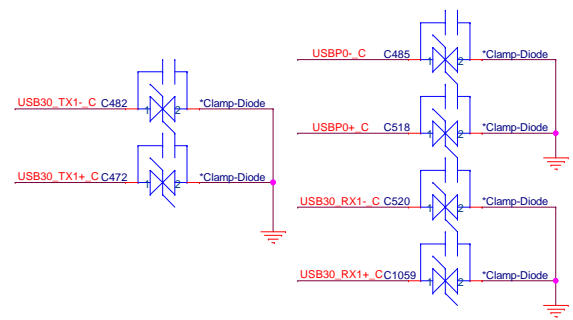
Digital



Keep L_SPK+/- and R_SPK+/- trace width 30 mil least

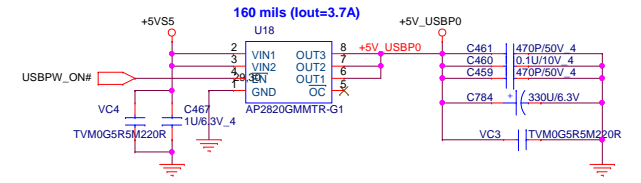


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	Quanta Computer Inc.		
	Size Custom	Document Number Azalia ALC3227	
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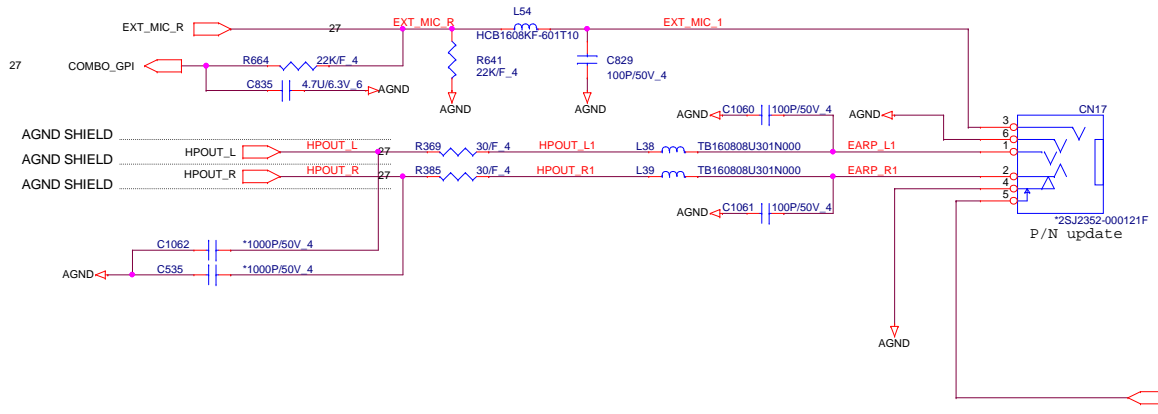


Change footprint to usb-tarag-9v1391-9p

USB3.0 X 2/USB2.0 COMBO

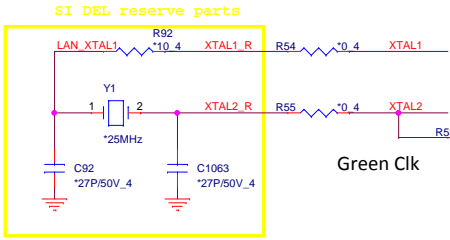


COMBO JACK



10,29,33,35,36,37,38,39,40,41,42,39
 2,6,7,8,9,10,12,13,14,23,24,25,26,27,29,30,31,32,33,36,39,40,42
 25,29,39 +3VLANVCC

	PROJECT : R62		Rev 1A
	Quanta Computer Inc.		
	Size Custom Document Number USB/BT/Audio Jack	Date: Monday, October 22, 2012 Sheet 28 of 43	

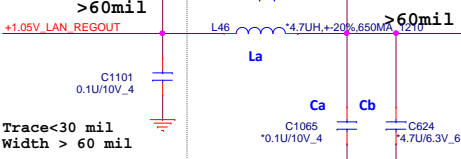


Green Clk

For GbE
* Place Cc,Cd,Ce,Cf close to each VDD10 pin-- 3, 22, 8, 30

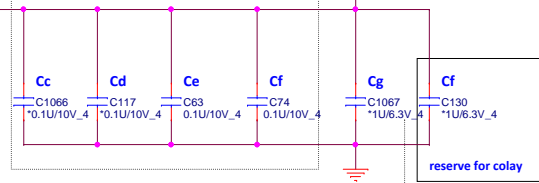
For 10/100 NA Ce,Cf
* Place Ce, Cf close to each VDD10 pin-- 8, 30 only,

Power trace Layout 宽度 > 60mil



For GbE
Stuff La, Ca, Cb

For 10/100
NA: La, Ca, Cb

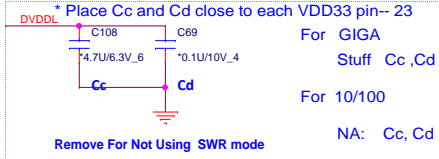
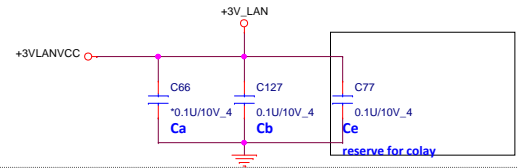


For GbE
* Place Cf close to each VDD10 pin-- 22 (reserve)

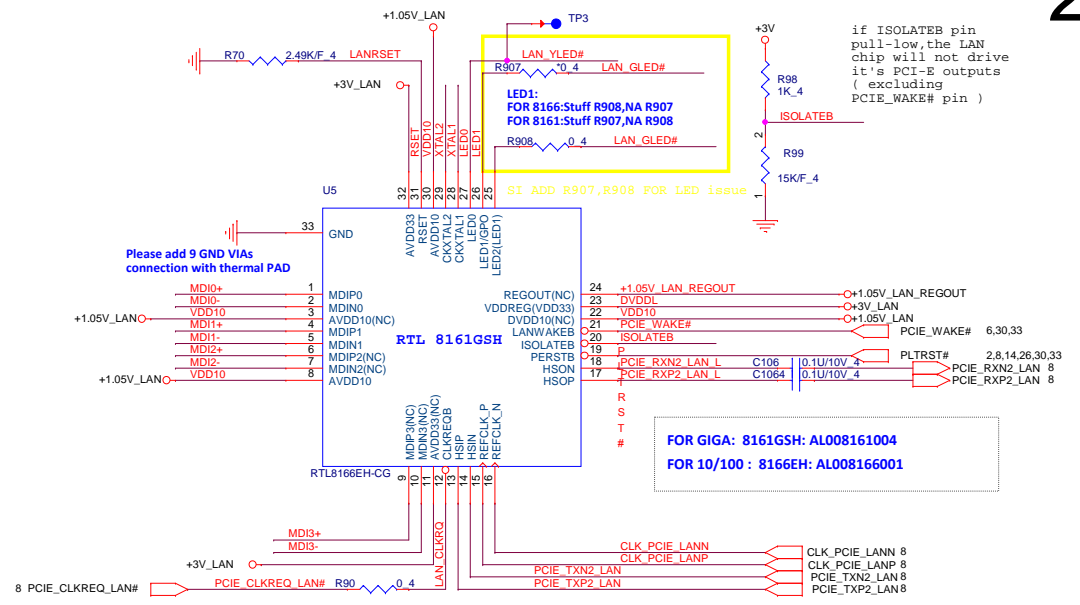
For 10/100
* Place Cg close to each VDD10 pin-- 30 (reserve)

For 10/100
* Stuff Ca and Ce only, close to each VDD33 pin-- 23, 32

For GIGA
* Stuff Ca and Cb only, close to each VDD3 pin-- 11, 32

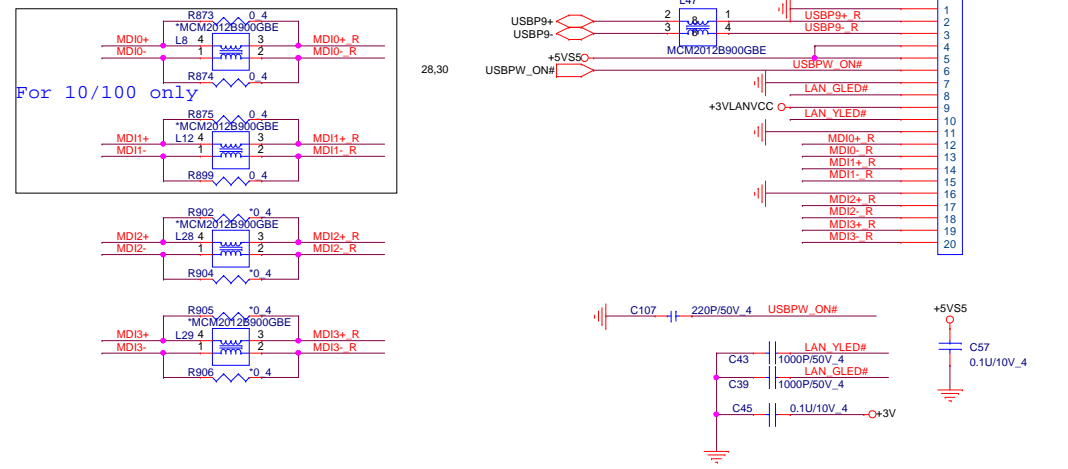


2,6,7,8,9,10,12,13,14,23,24,25,26,27,30,31,32,33,36,39,40,42,25,39 +3VLANVCC

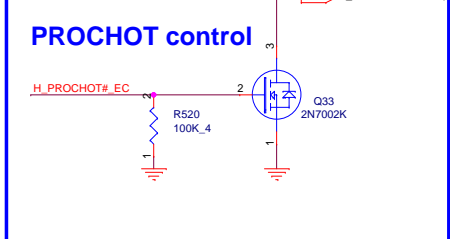
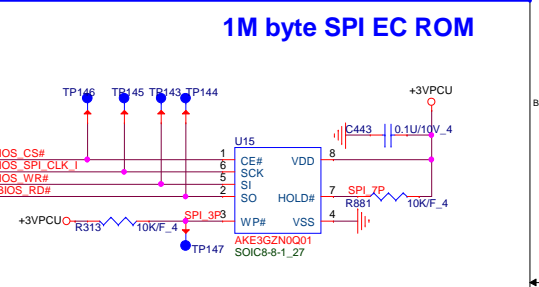
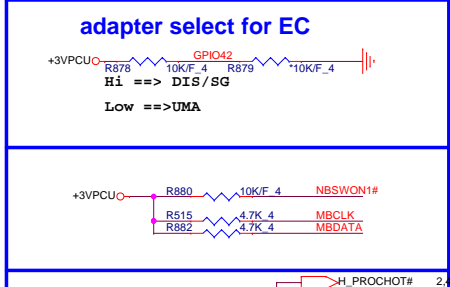
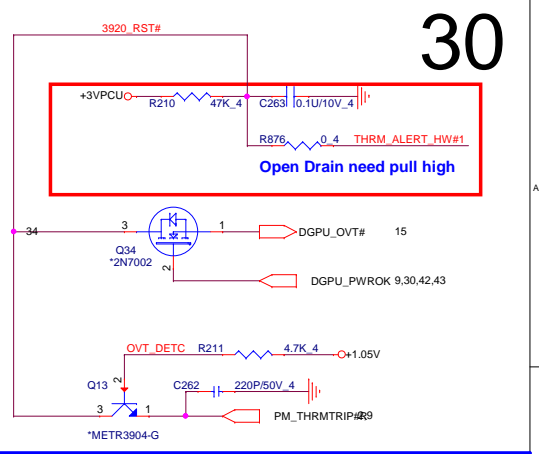
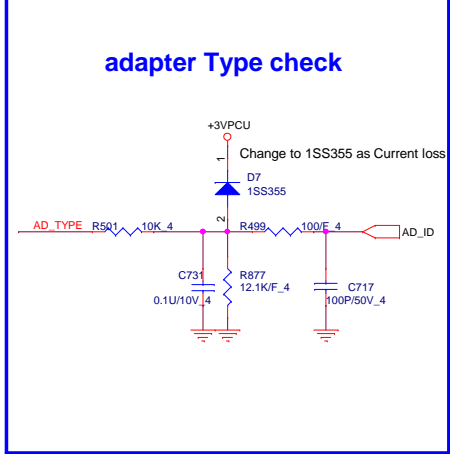
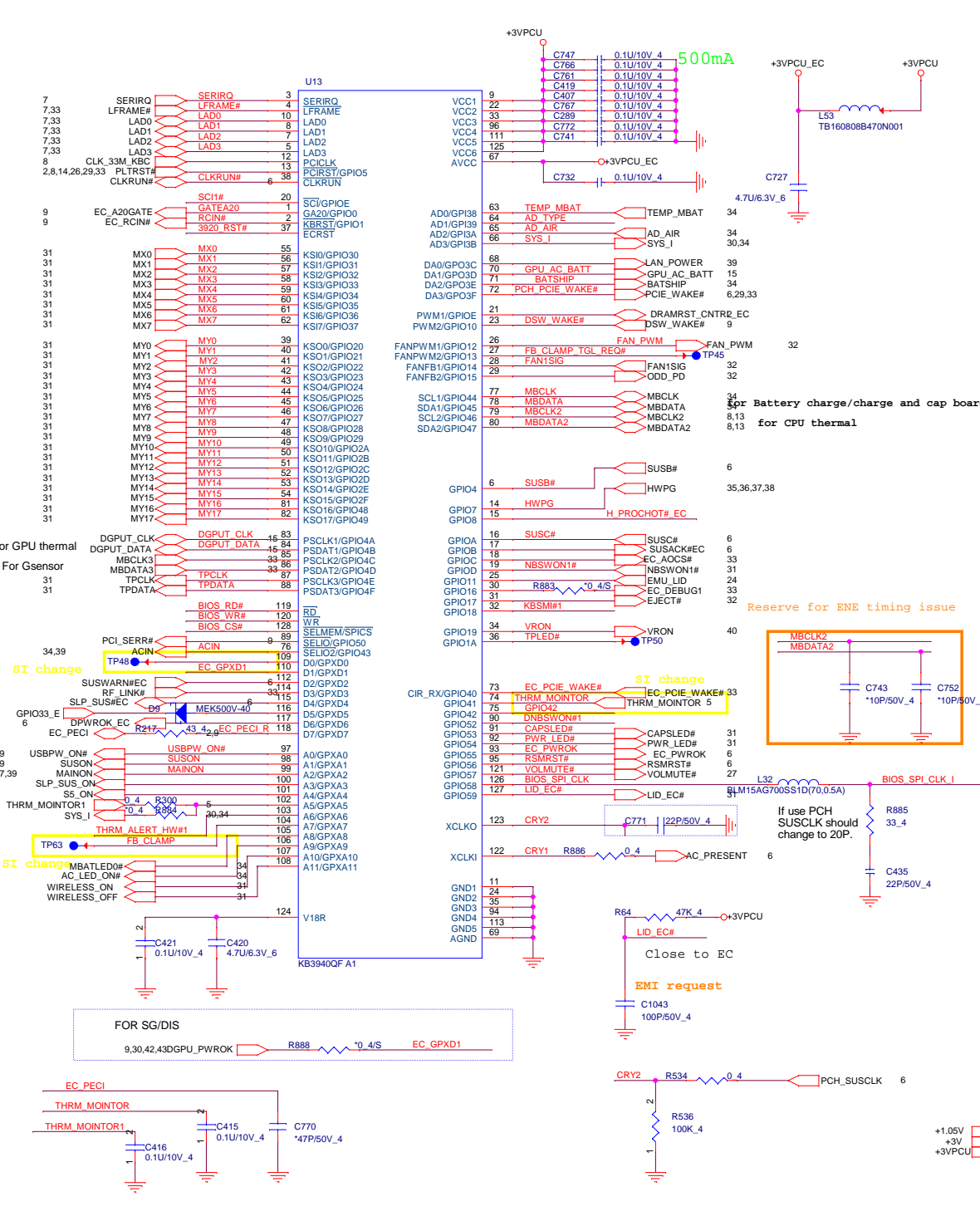


if ISOLATEB pin pull-low, the LAN chip will not drive it's PCI-E outputs (excluding PCIE_WAKE# pin)

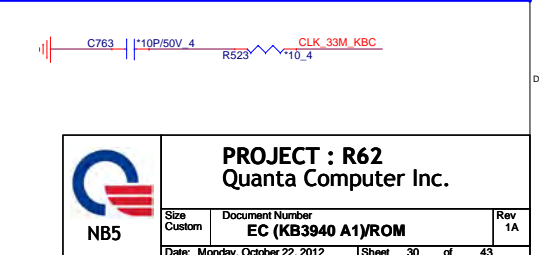
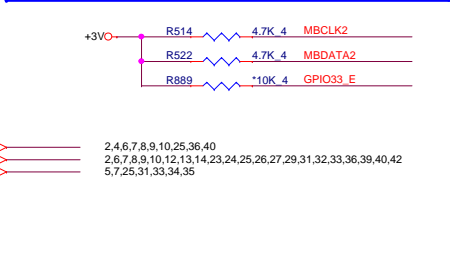
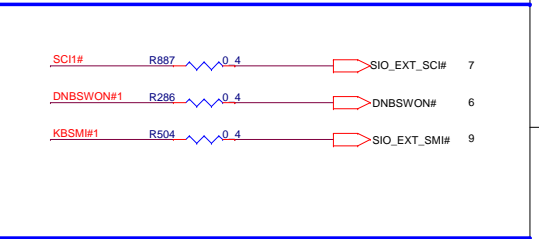
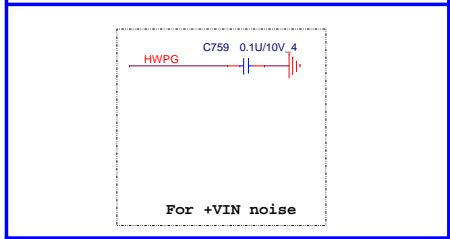
Right SIDE USBX1 and LAN CONN



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Vender	Size	P/N
EON	1MB	AKE3GN0Q01 (EN25Q80A-100HIP)
GigaDevice	1MB	AKE3GGN0Q00 (GD25Q80BSIGR)
AMIC	1MB	AKE3GZP0801 (A25L080M-F)
Socket		DFHS08FS023

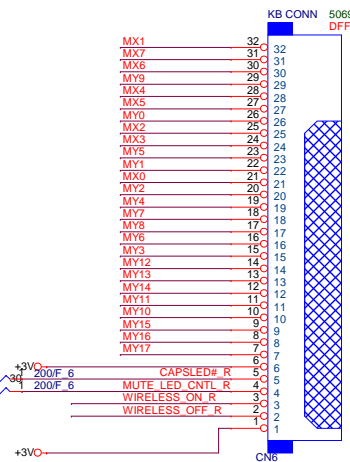
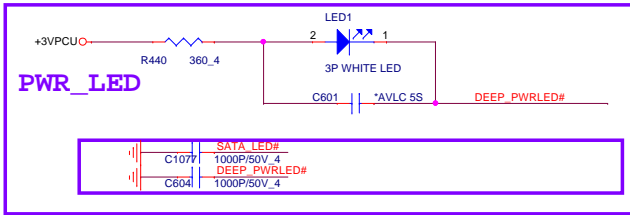
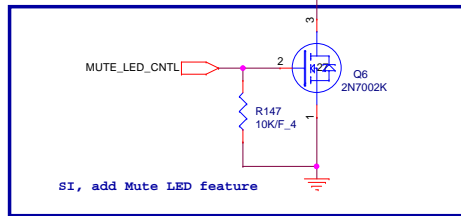
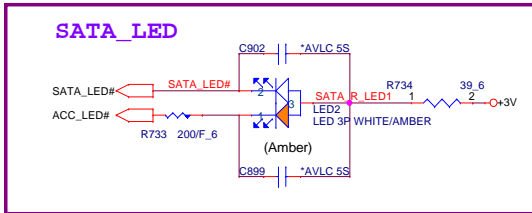
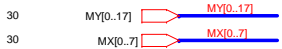


PROJECT : R62

Quanta Computer Inc.

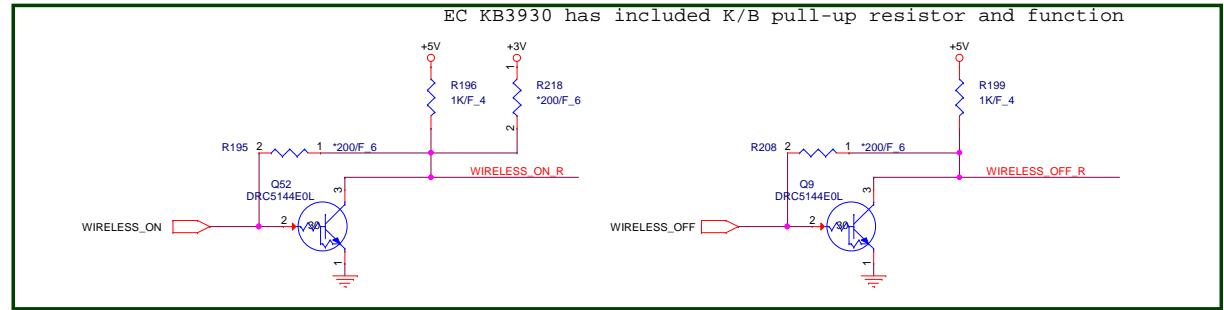
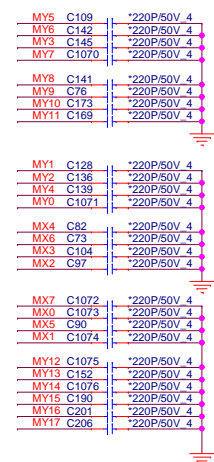
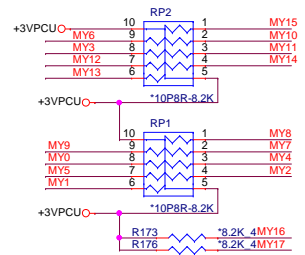
Size Custom	Document Number	Rev 1A
EC (KB3940 A1)ROM		
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KEYBOARD Con.



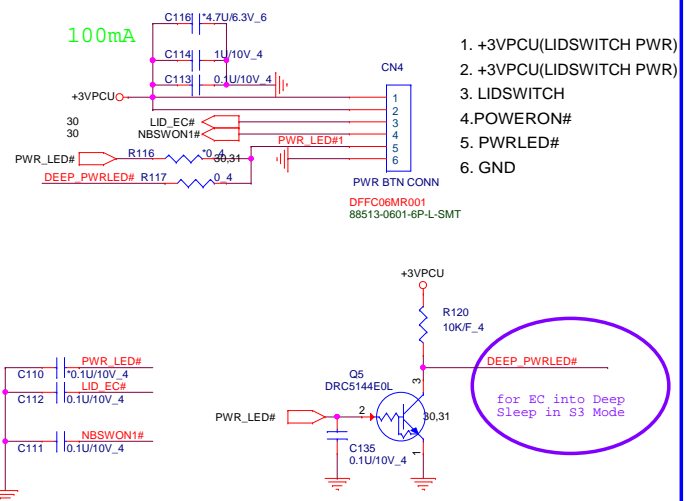
P/N update

KEYBOARD PULL-UP



EC KB3930 has included K/B pull-up resistor and function

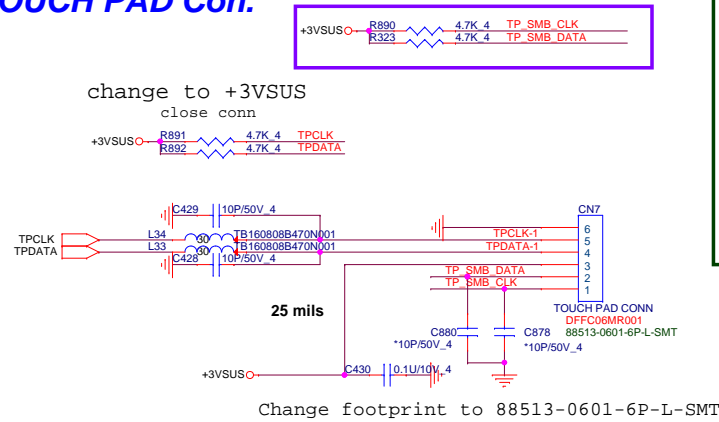
POWER BOTTON CONNECT



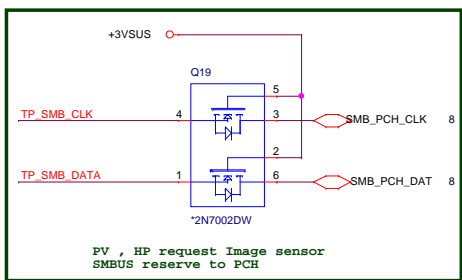
1. +3VPCU(LIDSWITCH PWR)
2. +3VPCU(LIDSWITCH PWR)
3. LIDSWITCH
4. POWERON#
5. PWRLED#
6. GND

for EC into Deep Sleep in S3 Mode

TOUCH PAD Con.



Change footprint to 88513-0601-6P-L-SMT



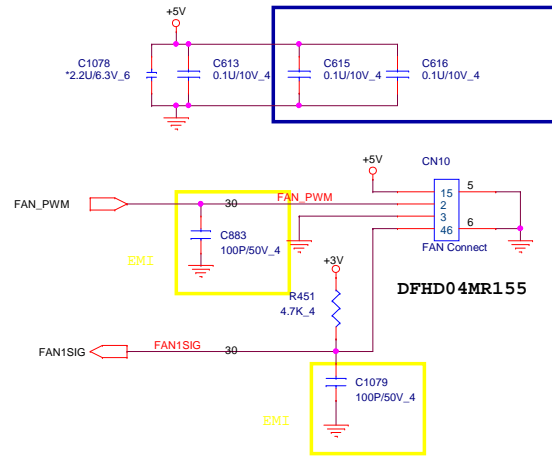
PV , HP request Image sensor SMBUS reserve to PCH



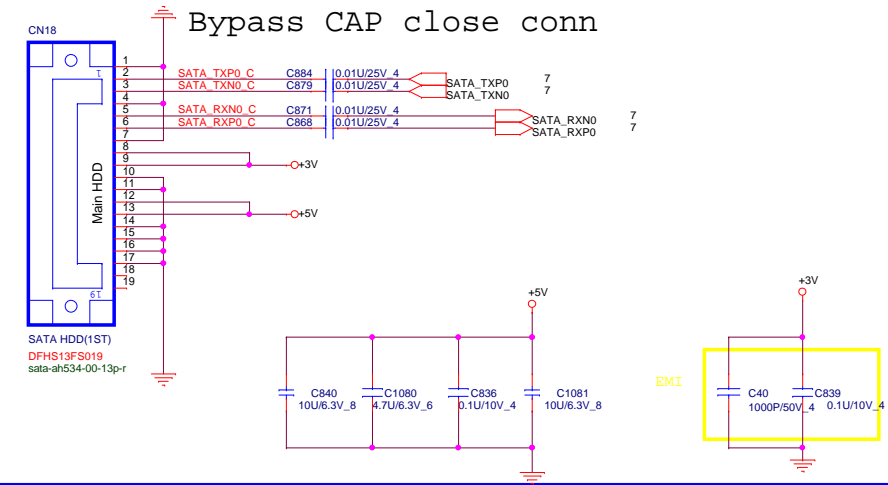
PROJECT : R62
Quanta Computer Inc.

Size Custom	Document Number LED/KB/SW/TP	Rev 1A
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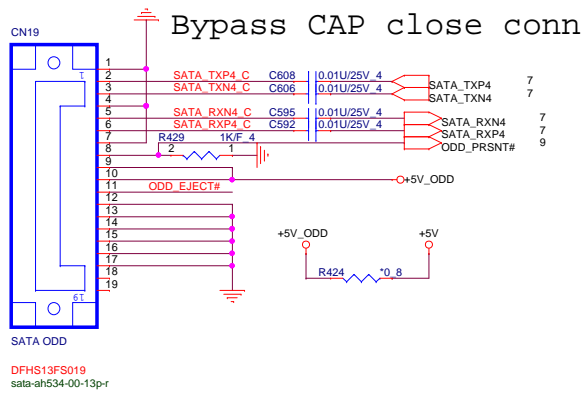
CPU FAN



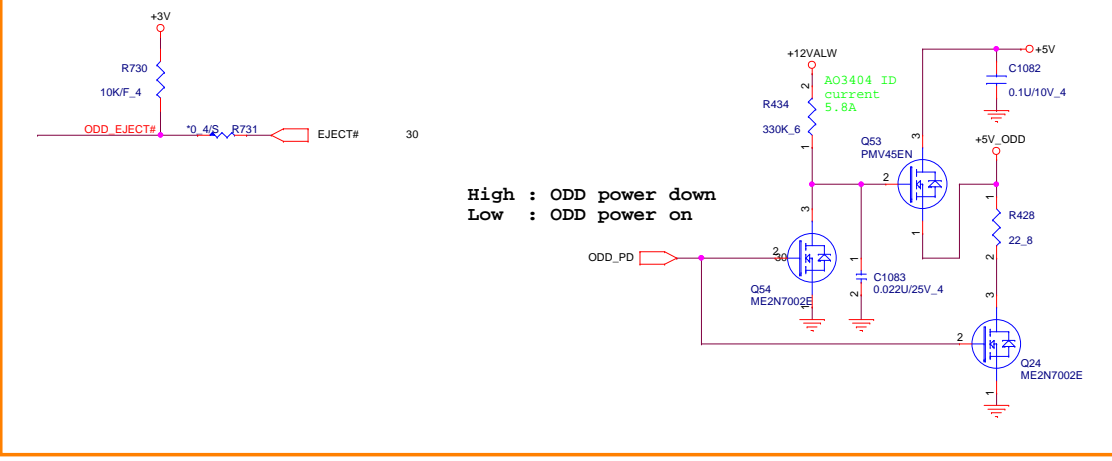
SATA HDD CONNECTOR



SATA ODD CONNECTOR



follow INTEL DG change eject PU to +3V.

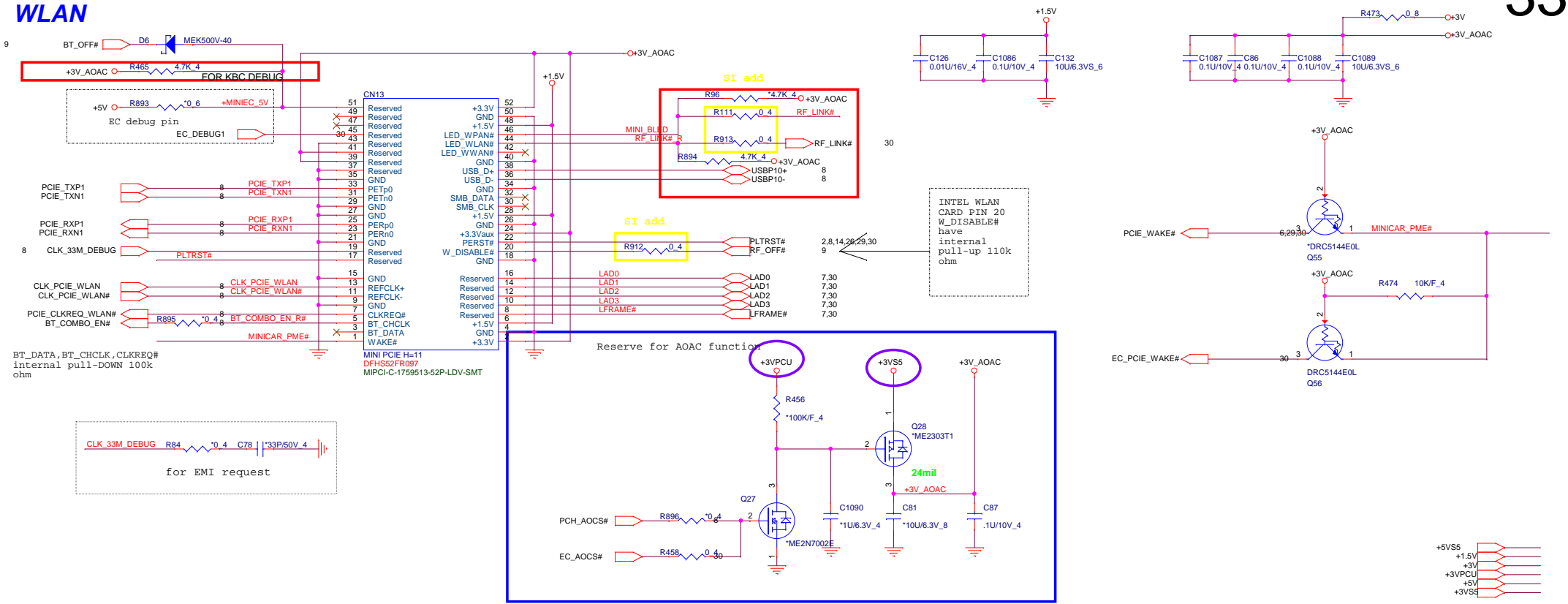


High : ODD power down
Low : ODD power on

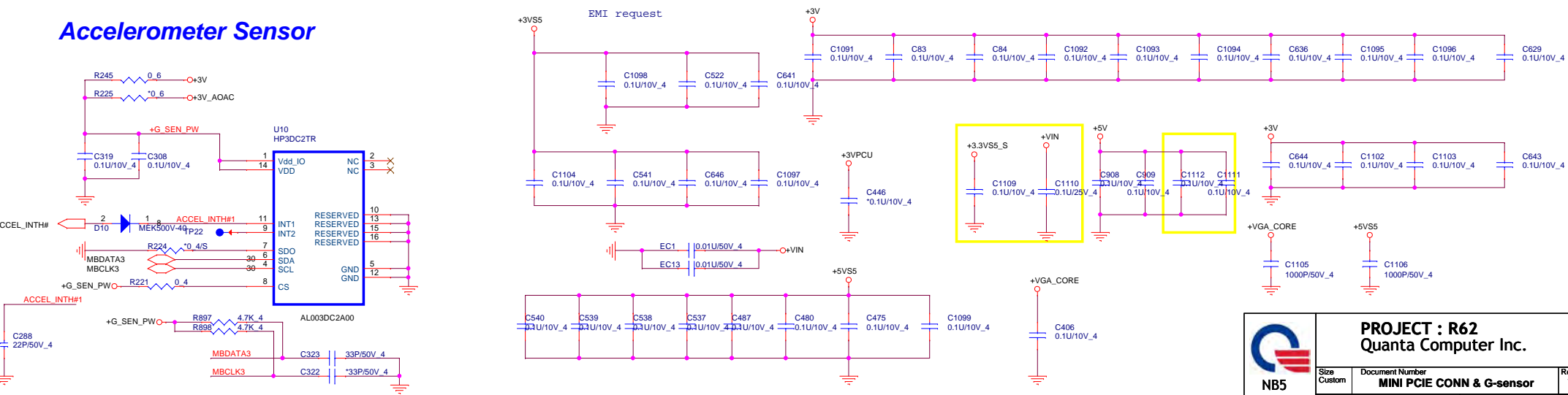
- +3V
 - +3VPCU
 - +5V
 - +12VALW
- 2,6,7,8,9,10,12,13,14,23,24,25,26,27,29,30,31,33,36,39,40,42
5,7,25,30,31,33,34,35
7,10,23,25,27,31,33,39
34,39,43

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	Quanta Computer Inc.		
	Size Custom	Document Number HDD/ODD/FAN	
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Mini PCI-E Card 1 WLAN

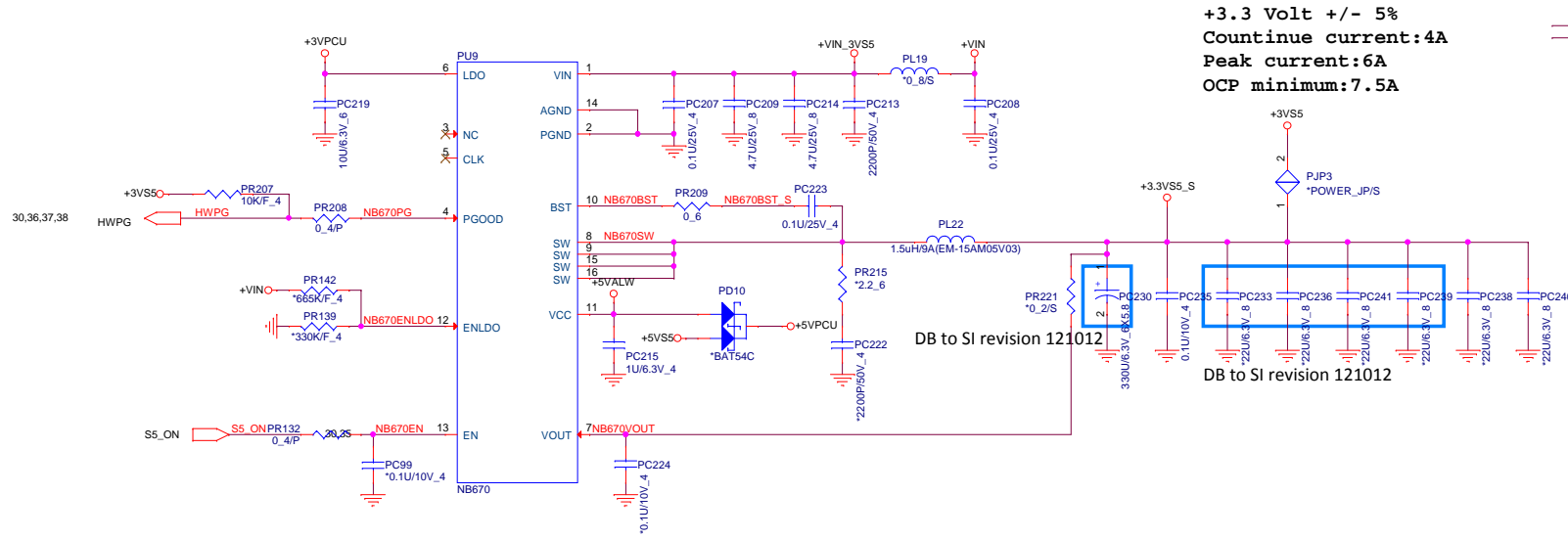



Accelerometer Sensor

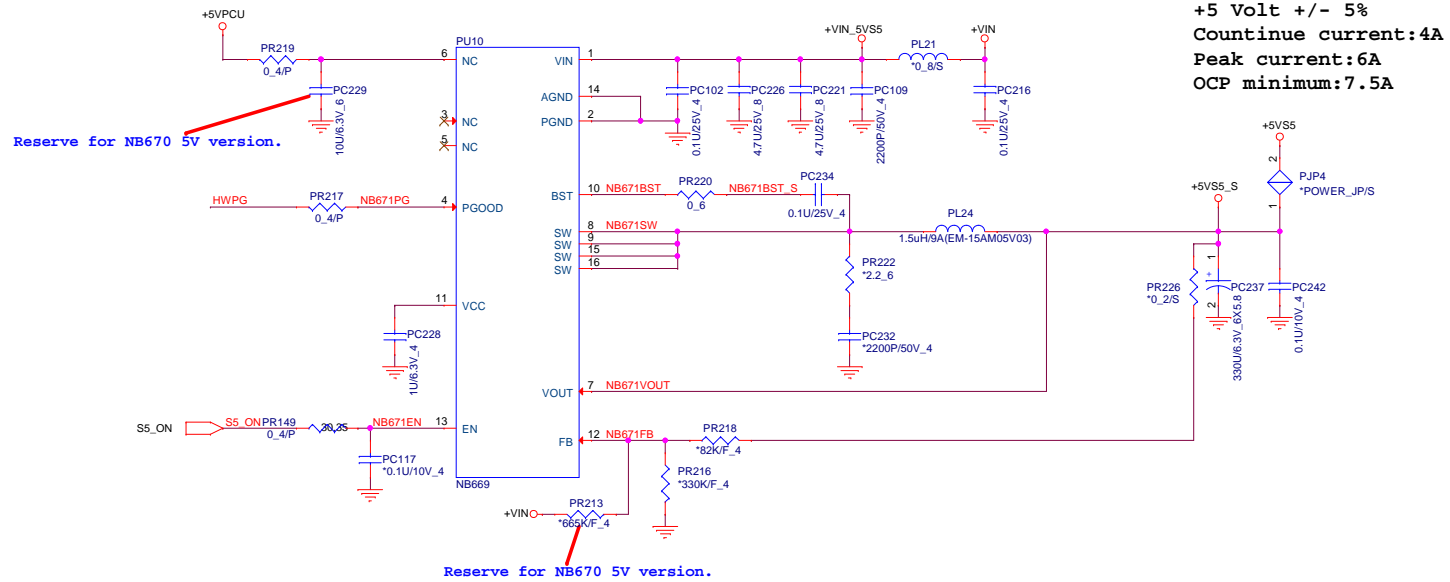



	PROJECT : R62	
	Quanta Computer Inc.	
	Size Custom	Document Number MINI PCI-E CONN & G-sensor
Date: Monday, October 22, 2012		Sheet 33 of 43

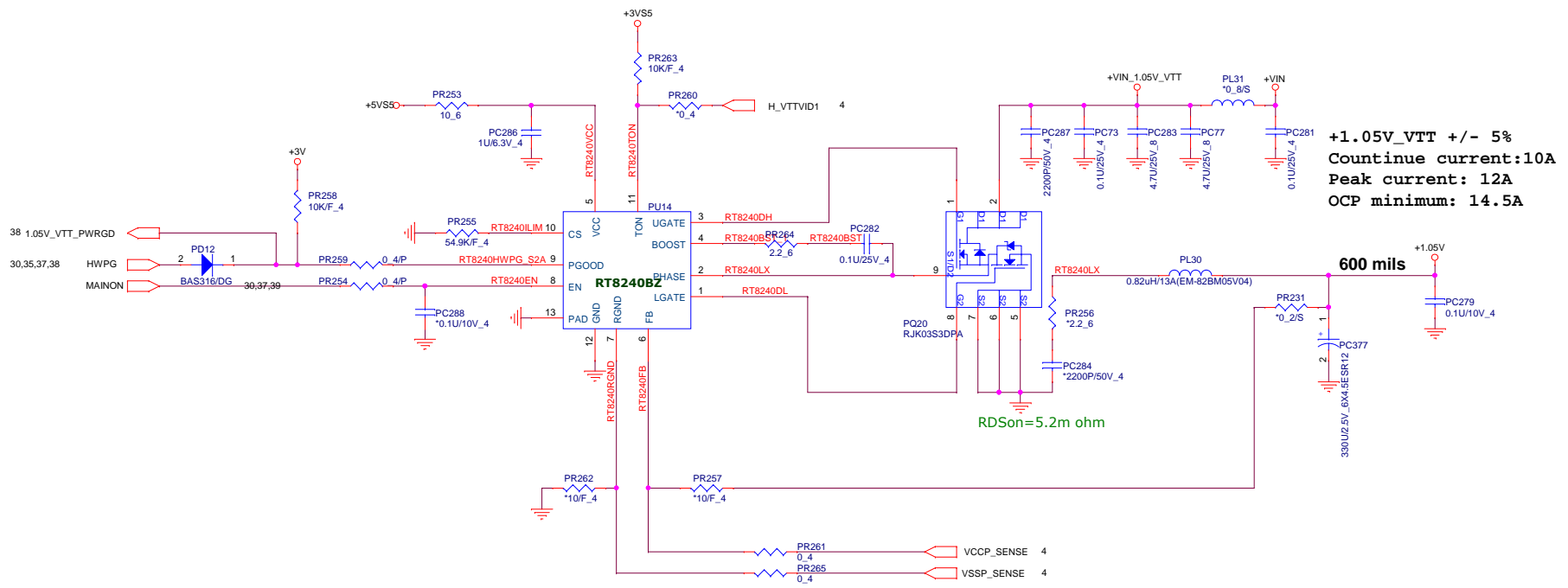
DC/DC +3VS5/+5VS5




 +3VS5
 +5VS5
 6,7,9,10,33,36,39,43
 10,28,29,33,36,37,38,39,40,41,42,43



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	Quanta Computer Inc.			
	Size Custom	Document Number 3/5VPCU(RT8243A)		
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+1.05V_VTT +/- 5%
Countinue current:10A
Peak current: 12A
OCP minimum: 14.5A

600 mils

RDSon=5.2m ohm

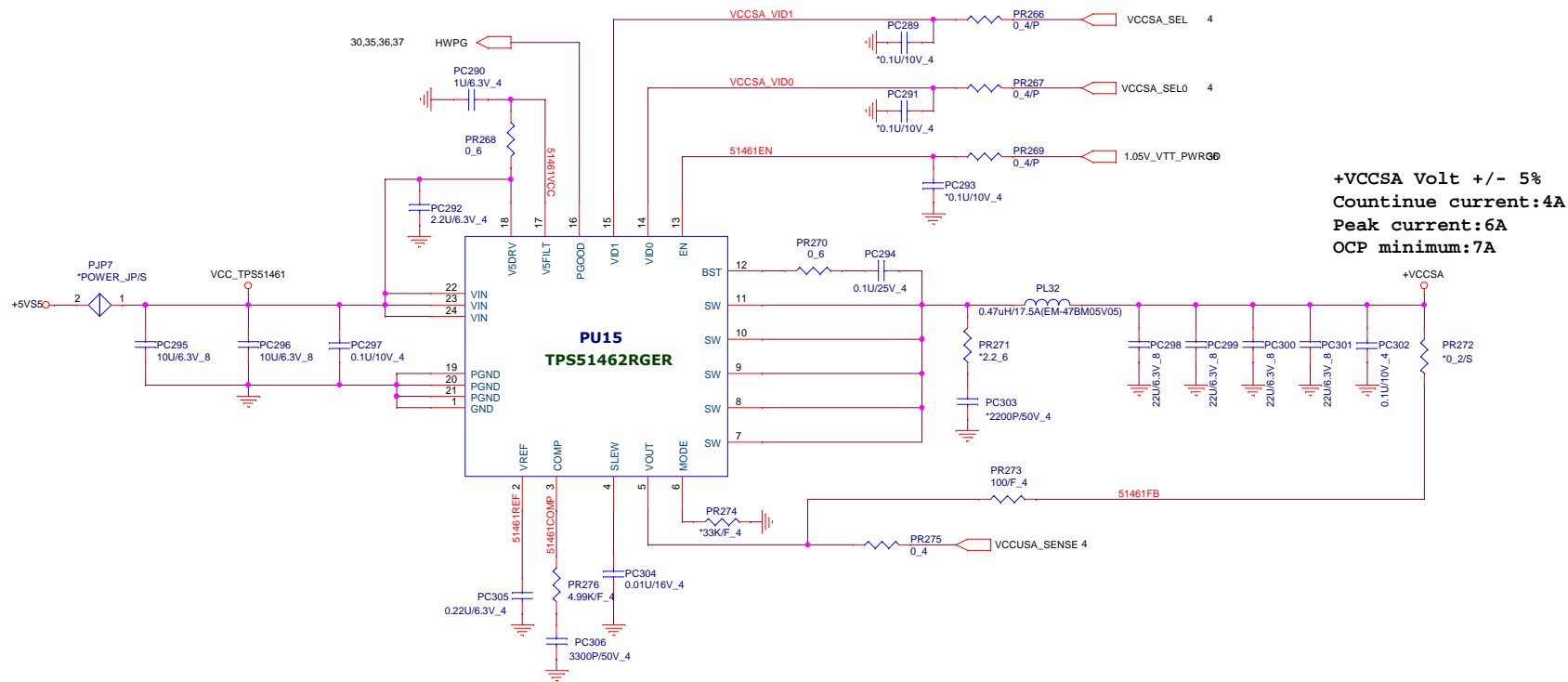
+1.05V 2,4,6,7,8,9,10,25,30,40


	PROJECT : R62		Rev 1A
	Quanta Computer Inc.		
	Size Custom	Document Number 1.05V(RT8228BZ)	
Date: Monday, October 22, 2012		Sheet 36 of 43	

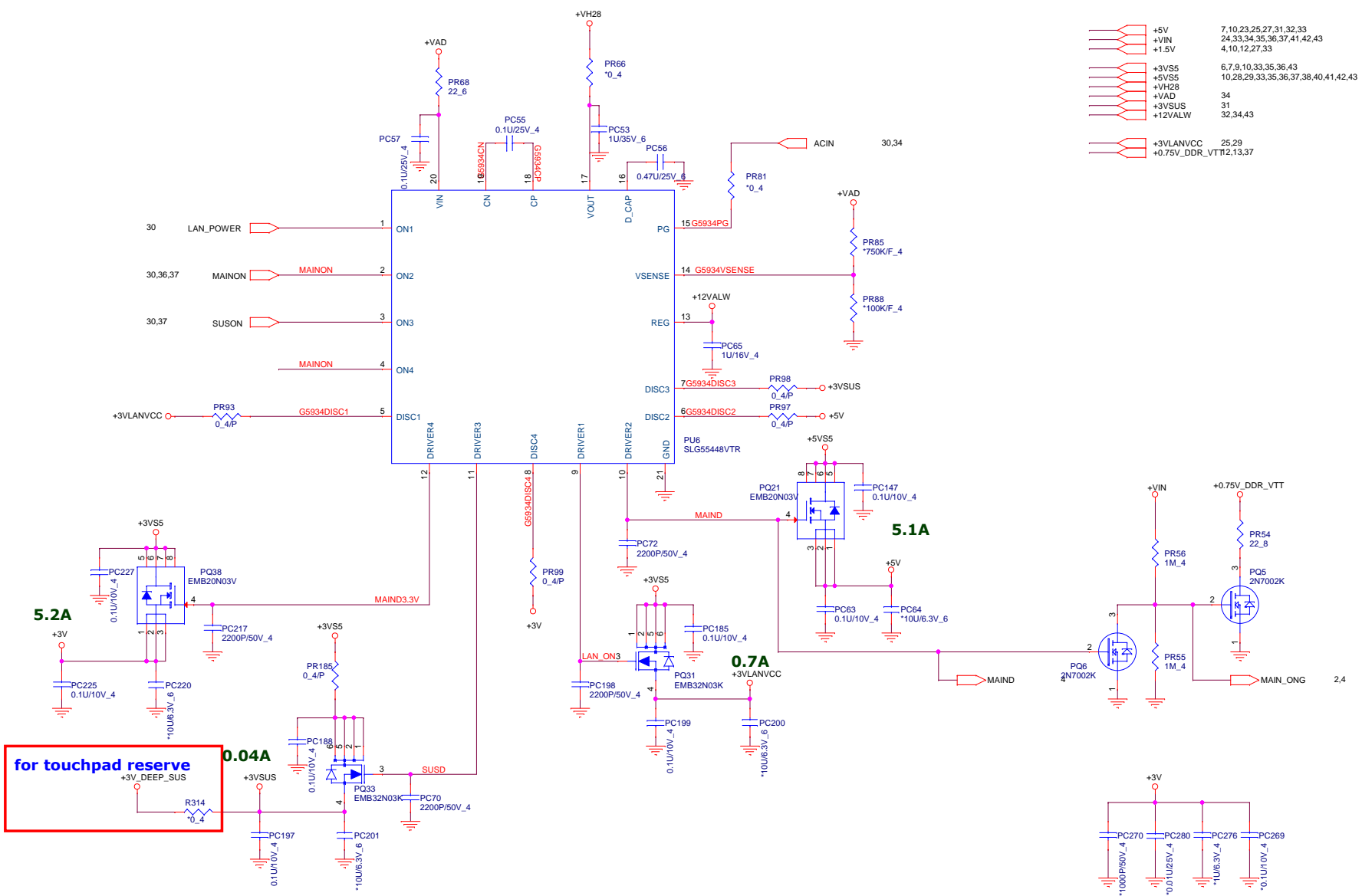
TPSS1462RGER/AL051462000

For CPU SV system agent
voltage slew rate of 0.5 -10 mV/ μ s

SEL0	SEL1	+VCCSA
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

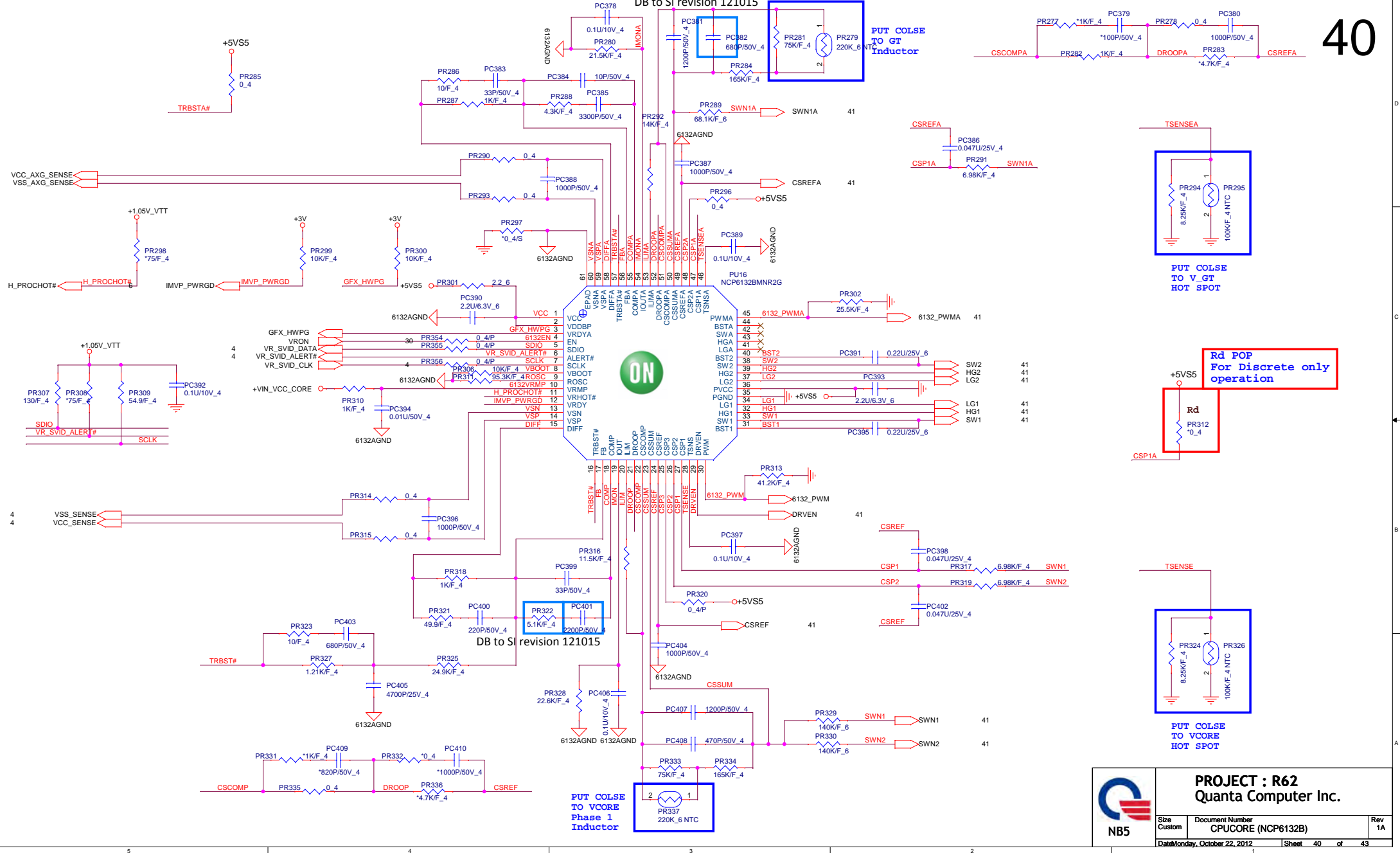


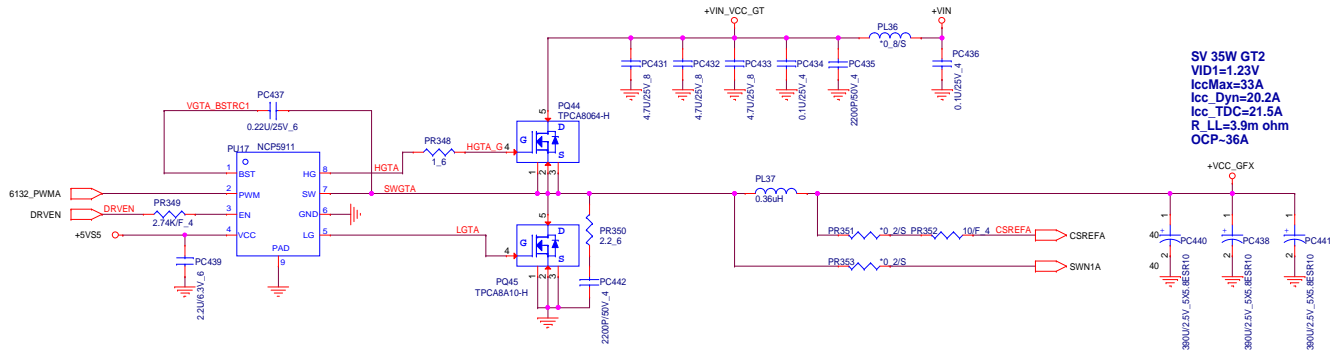
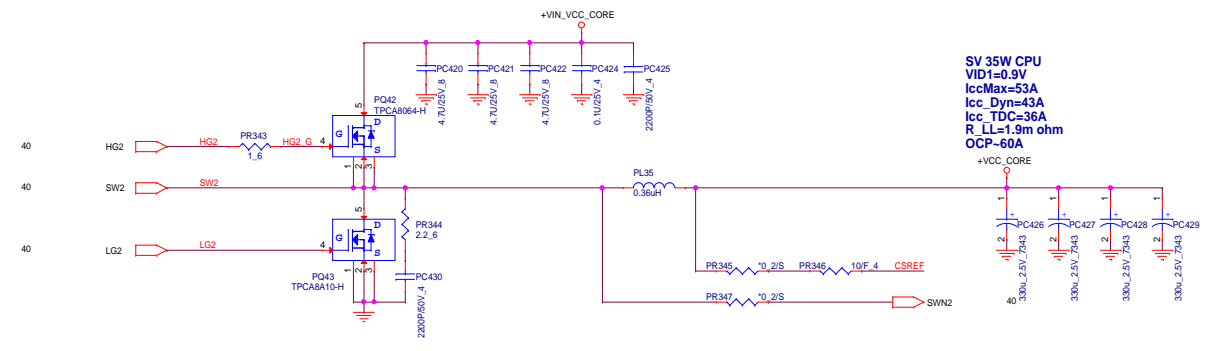
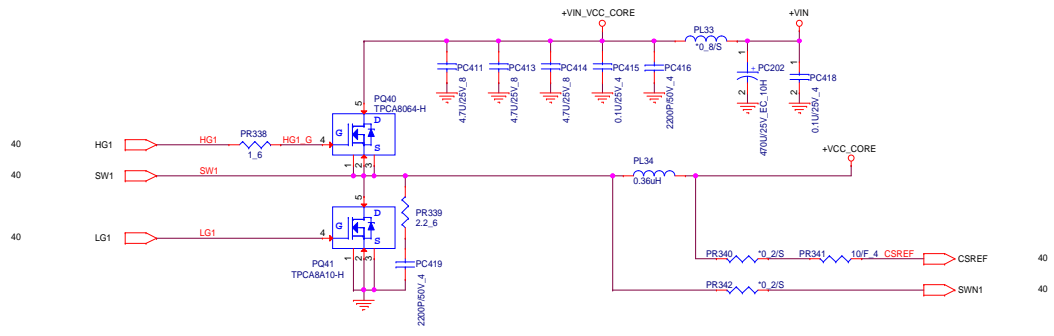
	PROJECT : R62 Quanta Computer Inc.		
	Size Custom	Document Number DDR3L(APW8819)	Rev 1A
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+5V	7,10,23,25,27,31,32,33
+1.5V	24,33,34,35,36,37,41,42,43
+3VS5	6,7,9,10,33,35,36,43
+5VS5	10,28,29,33,35,36,37,38,40,41,42,43
+VH28	34
+VAD	31
+3VSUS	31
+12VALW	32,34,43
+3VLANVCC	25,29
+0.75V_DDR_VTT	2,13,37

	PROJECT : R62 Quanta Computer Inc.		
	Size Custom	Document Number Dis-charge IC (G5934)	Rev 1A
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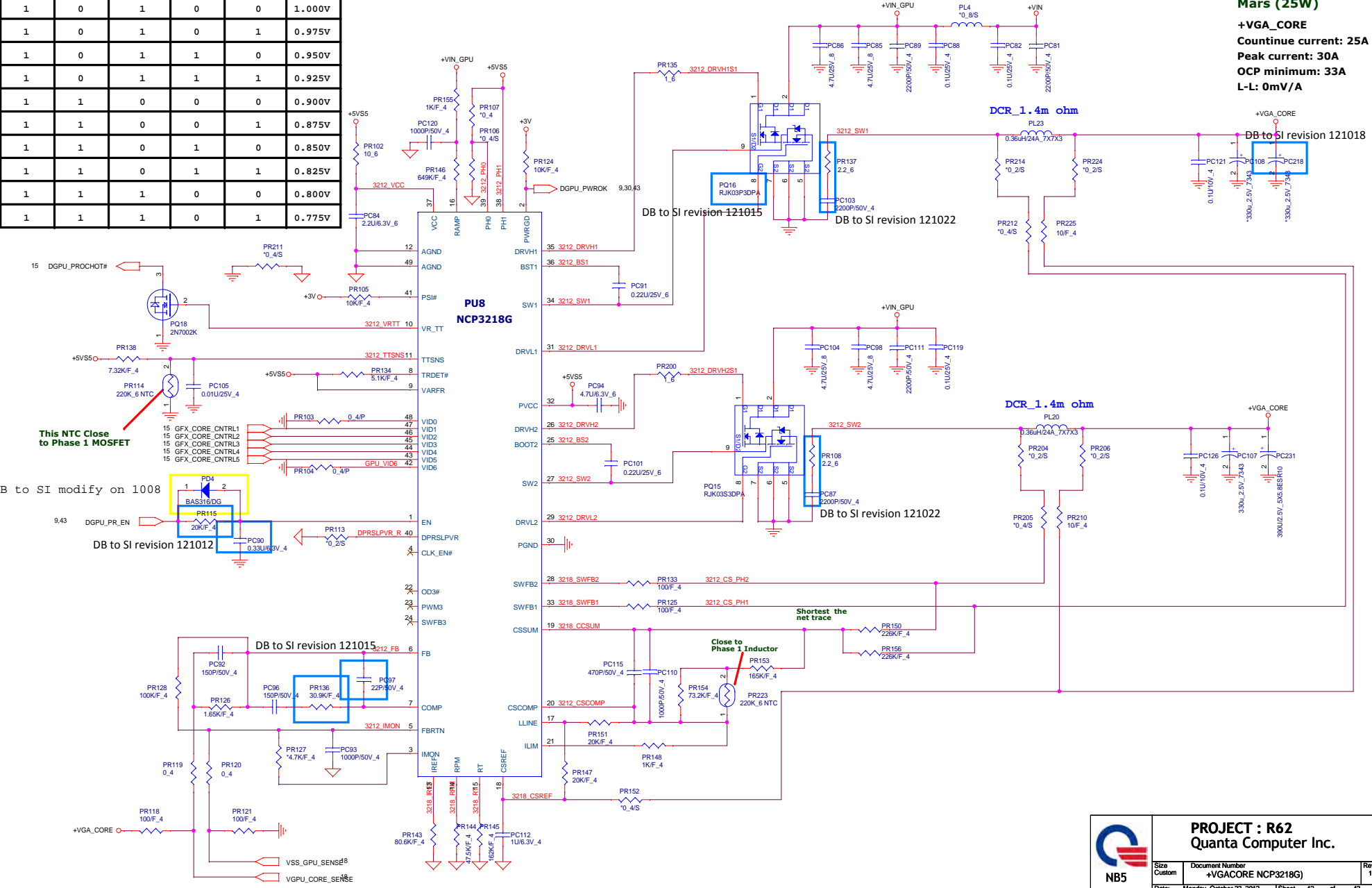
VGA Core

GPIO10 GPIO12 GPIO16 GPIO20 GPIO15 Mars XT

PWRCNTL5	PWRCNTL4	PWRCNTL3	PWRCNTL2	PWRCNTL1	V-CORE
0	1	1	1	1	1.125V
1	0	0	0	0	1.100V
1	0	0	0	1	1.075V
1	0	0	1	0	1.050V
1	0	0	1	1	1.025V
1	0	1	0	0	1.000V
1	0	1	0	1	0.975V
1	0	1	1	0	0.950V
1	0	1	1	1	0.925V
1	1	0	0	0	0.900V
1	1	0	0	1	0.875V
1	1	0	1	0	0.850V
1	1	0	1	1	0.825V
1	1	1	0	0	0.800V
1	1	1	0	1	0.775V

Default

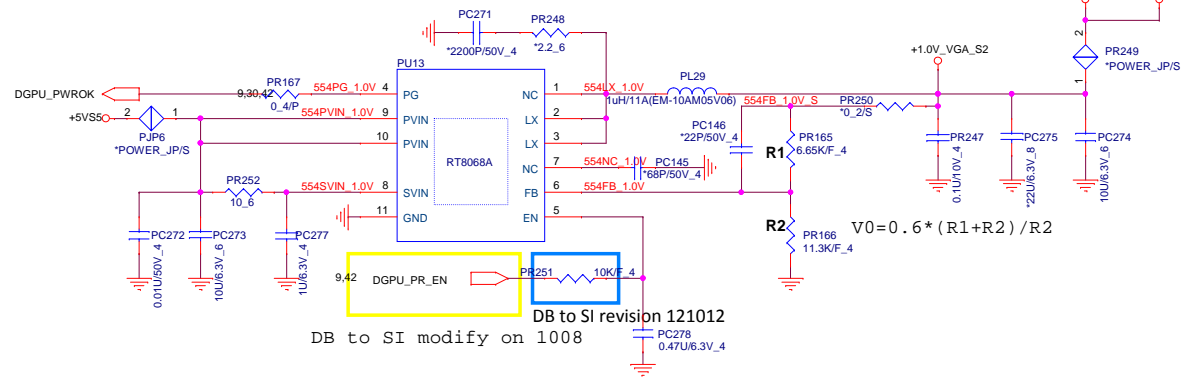
Mars (25W)
+VGA_CORE
 Continue current: 25A
 Peak current: 30A
 OCP minimum: 33A
 L-L: 0mV/A



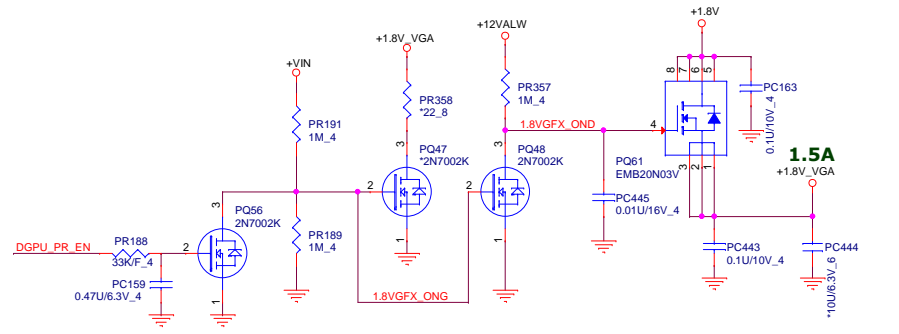
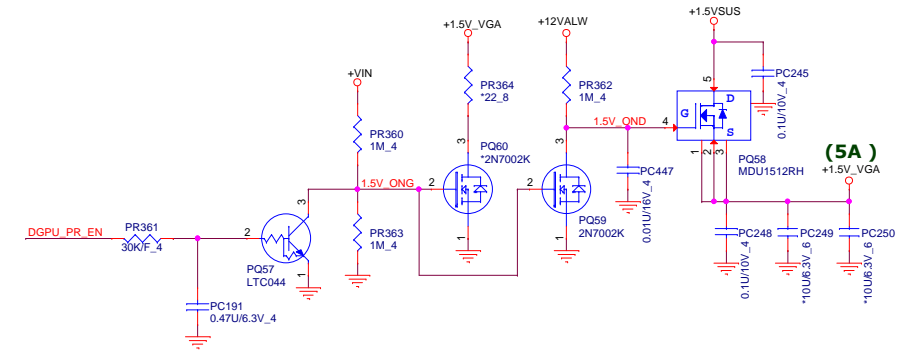
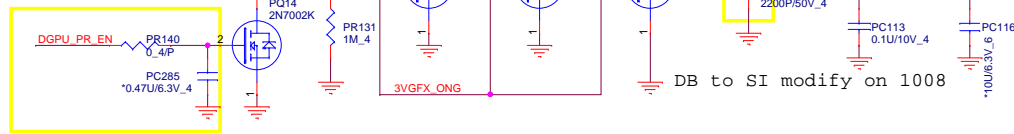
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R2 Value	P/N	1.0V_VGA
10K	CS31002FB26	1.0V
11.3K	CS31132FB07	0.95V

+0.95V +/- 3%
 Countinue current:2A
 Peak current:3A
 OCP minimum:4A



DB to SI modify on 1008



- +1.8V_VGA 15,16,18,19,25
- +1.0V_VGA 14,16,18,19
- +3V_VGA 18

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