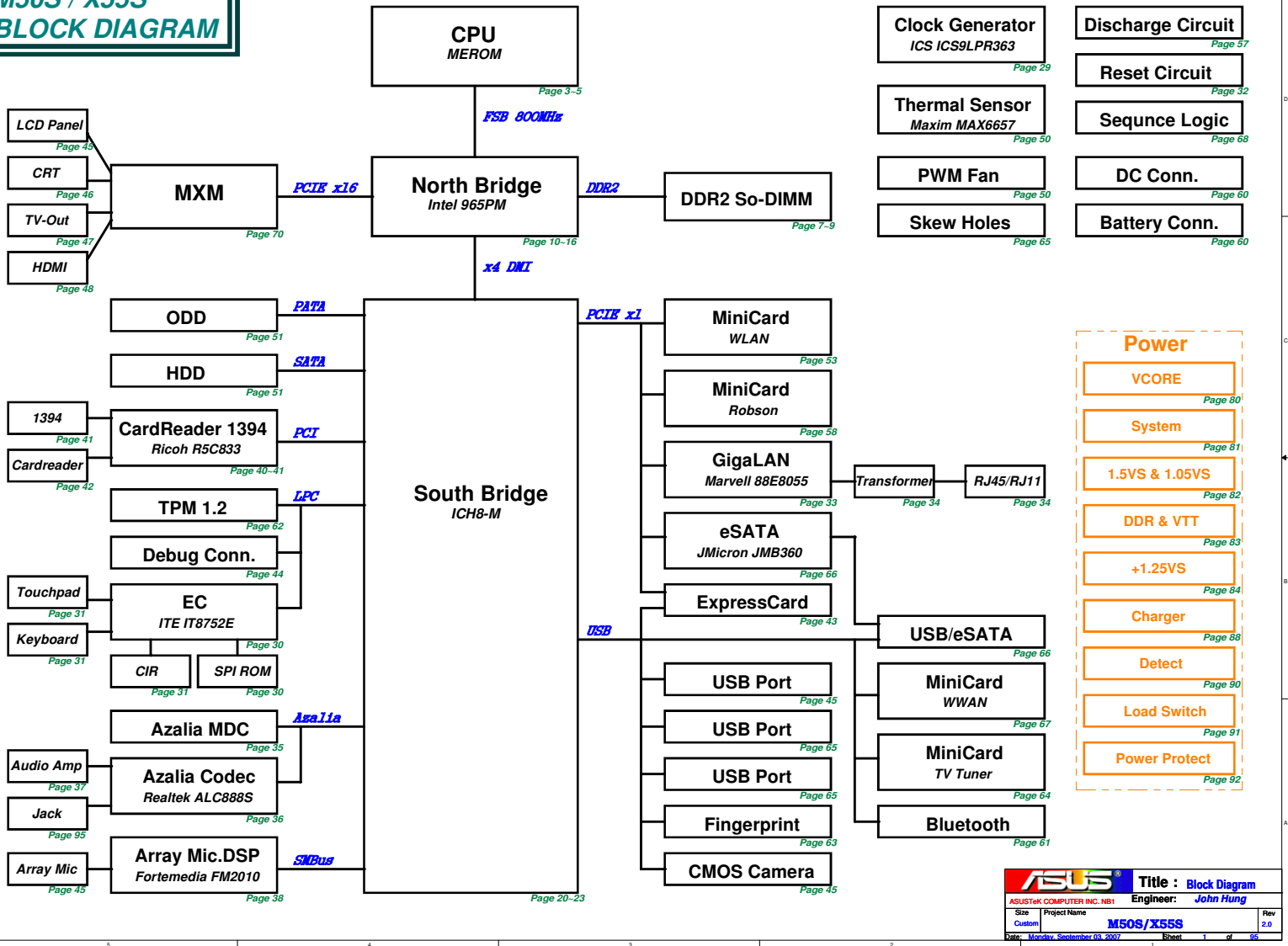


M50S / X55S BLOCK DIAGRAM



ICH8-M GPIO SETTING

Pin	Pin Name	Signal Name	Type
AG12	BM_BUSY#/GPIO0	PM_BMBUSY#	I
AJ8	TACH1/GPIO1	BT_DECT#	I
F8	PIRQE#/GPIO2	PCI_INTE#	I/OD
G11	PIRQF#/GPIO3	PCI_INTF#	I/OD
F12	PIRQG#/GPIO4	PCI_INTG#	I/OD
B3	PIRQH#/GPIO5	PCI_INTH#	I/OD
AJ9	TACH2/GPIO6		
AH9	TACH3/GPIO7	WLAN_LED_ON	O
AE16	GPI08	EXT_SMI#	I
AG19	WOL_EN/GPIO9		
AJ24	CLGPI01/GPIO10		
AG22	SMBALERT#/GPIO11	SMB_ALERT#	I
AC19	GPI012	EXT_SCI#	I
AH21	GLAN_DOCK#/GPIO13		
AF22	CLGPI02/GPIO14		
AE20	STP_PC#/GPIO15	STP_PC#	I/O
AJ14	DPRSLPVR/GPIO16	PM_DPRSLPVR	O
AG8	TACH0/GPIO17	WLAN_ON#	O
AH12	GPI018		
AJ10	GPI019/SATA1GP		
AE11	GPI020	BT_LED_ON	O
AJ12	SATA0GP/GPIO21		
AG10	SCLOCK/GPIO22		
E6	LDRQ1#/GPIO23		
AJ27	CLGPI00/GPIO24		
AG18	STP_CPU#/GPIO25	STP_CPU#	O
AH27	S4_STATE#/GPIO26		
AH25	QRT_STATE0/GPIO27	BT_ON#	O
AD16	QRT_STATE1/GPIO28	CB_SD#	O
AG17	OC#5/GPIO29	INT_USB_OC#	I
AD12	OC#6/GPIO30	INT_USB_OC#	I
AJ18	OC#7/GPIO31	INT_USB_OC#	I
AH11	CLKRUN#/GPIO32	PM_CLKRUN#	O
AE10	AZ_DOCK_EN#/GPIO33		
AG14	AZ_DOCK_RST#/GPIO34		
AG13	SATACLKREQ#/GPIO35		
AF11	SATA2GP/GPIO36	EMAIL_LED#	O
AG11	SATA3GP/GPIO37	PCB_ID0	I
AF9	SLOAD/GPIO38	PCB_ID1	I
AJ11	SDATAOUT0/GPIO39	PCB_ID2	I
AG16	OC#1/GPIO40	USB_CON01_OC#	I
AG15	OC#2/GPIO41	USB_CON23_OC#	I
AE15	OC#3/GPIO42	USB_CON23_OC#	I
AF15	OC#4/GPIO43	NEWCARD_OC#	I
AD10	SATAOUT1/GPIO48		
AG29	CPUPWRGD/GPIO49	H_PWRGD	O
E18	REQ1#/GPIO50	PCI_REQ#1	I/O
C18	GNT1#/GPIO51		
B19	REQ2#/GPIO52	PCI_REQ#2	I/O
F18	GNT2#/GPIO53		
A11	REQ3#/GPIO54	PCI_REQ#3	I/O
C10	GNT3#/GPIO55		

EC IT8752E GPIO SETTING

Pin	Pin Name	Signal Name	Type
28	PWM0/GPA0	PWR_LED_UP#	O
29	PWM1/GPA1	CHG_LED_UP#	O
32	PWM2/GPA2		
33	PWM3/GPA3		
34	PWM4/GPA4	LCD_BL_PWM	O
35	PWM5/GPA5	FAN_PWM	O
36	PWM6/GPA6		
38	PWM7/GPA7		
122	RXD/GPB0	CHG_EN#	O
123	TXD/GPB1	PRECHG	O
139	CTX0/GPB2		
124	SMCLK0/GPB3	SMB0_CLK	I/O
125	SMDAT0/GPB4	SMB0_DAT	I/O
142	GA20/GPB5	A20_GATE	O
4	KBRST#/GPB6	RC_IN#	O
126	GPB7	PM_RSMRST#	O
133	CRX0/GPC0	CRX0	I
129	SMCLK1/GPC1	SMB1_CLK	I/O
130	SMDAT1/GPC2	SMB1_DAT	I/O
64	GPC3	PM_PWRBTN#	O
136	WUI2/GPC4	AC_IN_OC#	I
65	GPC5	OP_SD#	O
140	WUI3/GPC6	BAT1_IN_OC#	I
20	GPC7	RFON_SW#	I
22	WUI0/GPD0	PWRLIMIT#	I
25	WUI1/GPD1	PM_SUSC#	I
26	WUI4/GPD2	BUF_PLT_RST#	I
27	ECSCI#/GPD3	EXT_SCI#	O
19	GPD4	EXT_SMI#	O
37	GPD5	LCD_BACKOFF#	O
53	TACH0 / GPD6	FAN0_TACH	I
54	GPD7		
23	GPE0	VSUS_ON	O
94	GPE1	SUSC_EC#	O
95	GPE2	SUSC_EC#	O
96	GPE3	CPU_VRON	O
141	PWRSW/GPE4	PWR_SW#	I
39	WUI5/GPE5	BAT2_IN_OC#	I
21	GPE6	LID_SW#	I
24	GPE7	INSTANT_ON#	I
97	PS2CLK0/GPF0		
98	PS2DAT0/GPF1	COLOREN#	I
99	PS2CLK1/GPF2	MARATHON#	I
100	PS2DAT1/GPF3	DISTP#	I
101	PS2CLK2/GPF4	TP_CLK	I/O
102	PS2DAT2/GPF5	TP_DAT	I/O
131	SMCLK2/GPF6	THRO_CPU	O
132	SMDAT2/GPF7	TP_LED	O
118	WUI7/GPG0		
121	GGP1	PM_SUSB#	I
112	GGP2		
116	GGP6		

965GM/PM co-layout option:

965PM

Change:
U1001 to 965PM, U3601 to ALC888S
R1213-R1219 to 0ohm
C1406, C1501-C1504, C1506-C1507, C1510, C1514 to 0ohm

Mount:
D4801-D4803
F4801
J4801, J7001
H7001-H7004
Q4801
R1112-R1117, R1203-R1212, R1502, R2910, R3618-R3620, R4801-R4804
RX2901-RX2902, RX4801-RX4810
CX1201-CX1232

Un-mount:
R1202, R1401-R1403, R1501, R1503-R1505, R2909, R3621, R7001-R7008
RN7001-RN7011
RNX1201, RNX2901, RNX2915
L1501-L1505
C1404-C1405, C1407-C1409, C1505, C1509, C1511-C1513
CE1404, CE1501-CE1503

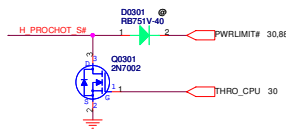
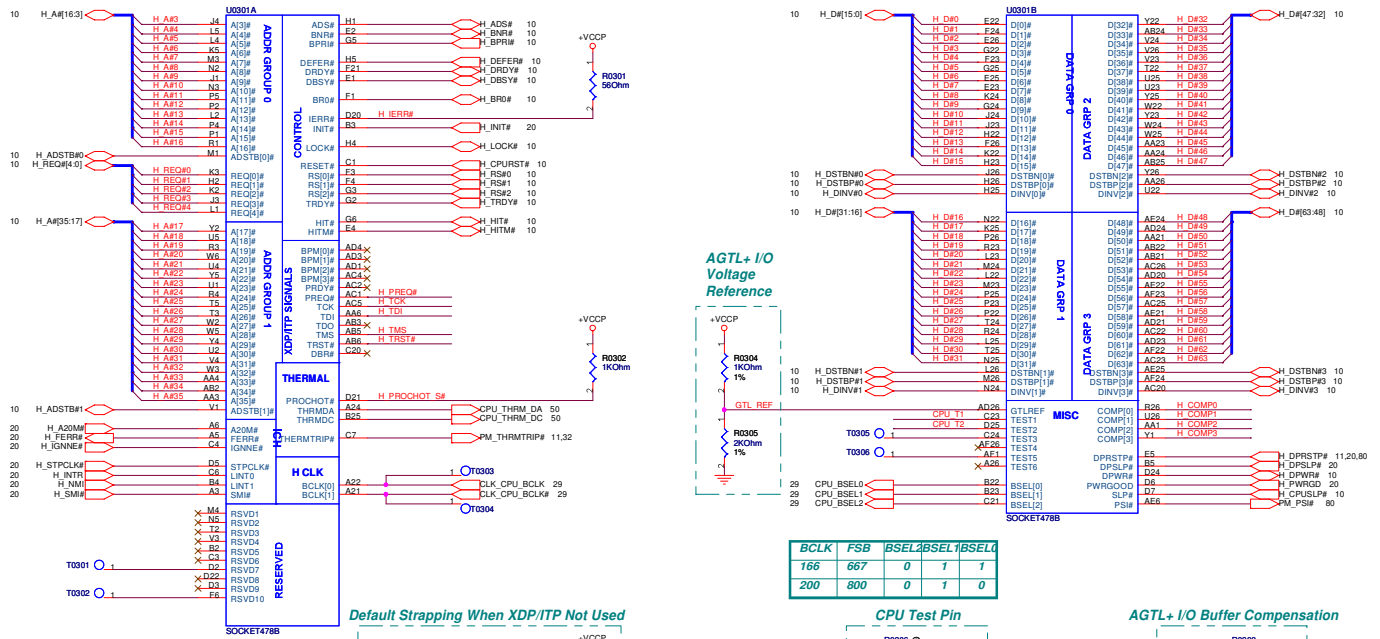
965GM

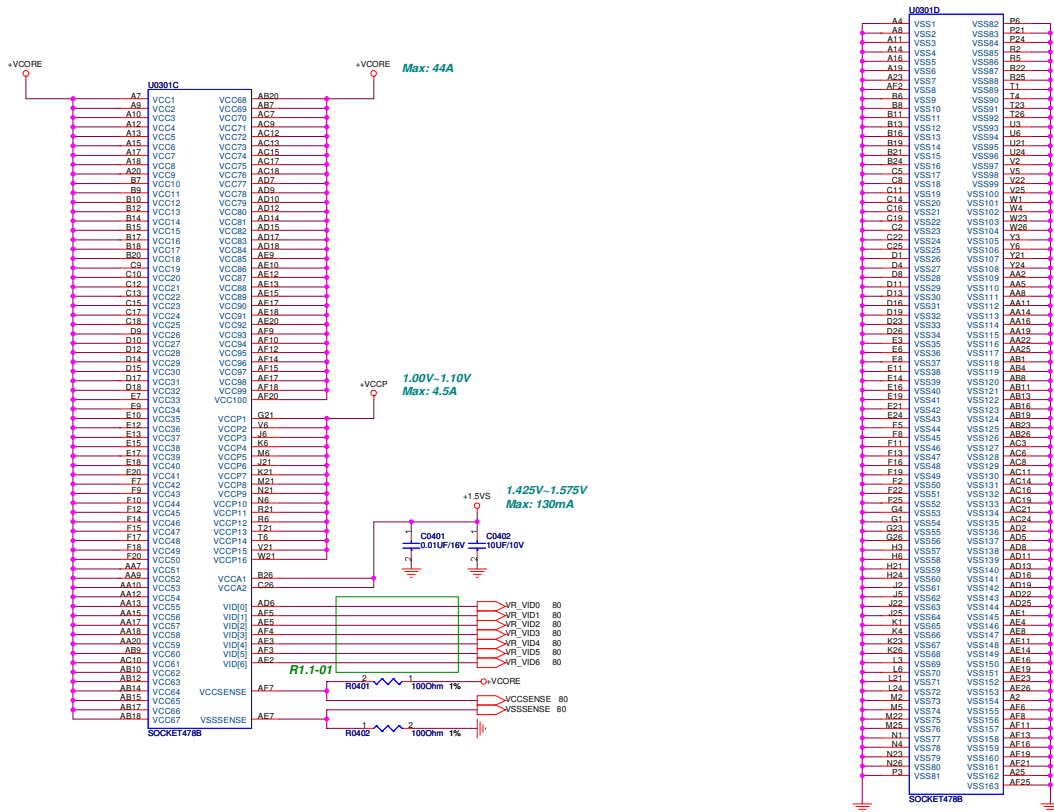
Change:
U1001 to 965GM
R1213-R1218 to 150ohm
R1219 to 1.3Kohm

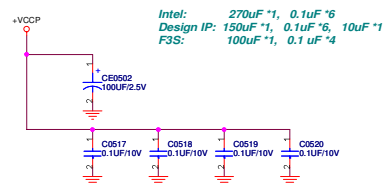
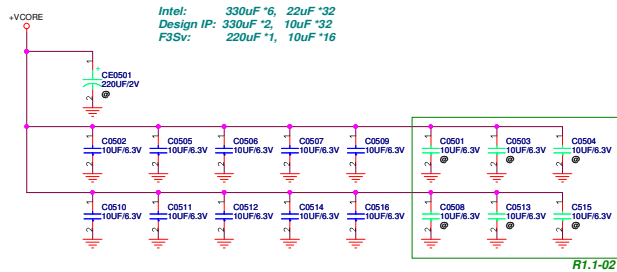
Un-mount:
D4801-D4803
F4801
J4801, J7001
H7001-H7004
Q4801
R1112-R1117, R1203-R1212, R1502, R2910, R3618-R3620, R4801-R4804
RX2901-RX2902, RX4801-RX4810
CX1201-CX1232


Mount:
R1202, R1401-R1403, R1501, R1503-R1505, R2909, R3621, R7001-R7008
RN7001-RN7011
RNX1201, RNX2901, RNX2915
L1501-L1505
C1404-C1409, C1501-C1507, C1509-C1514
CE1404, CE1501-CE1503

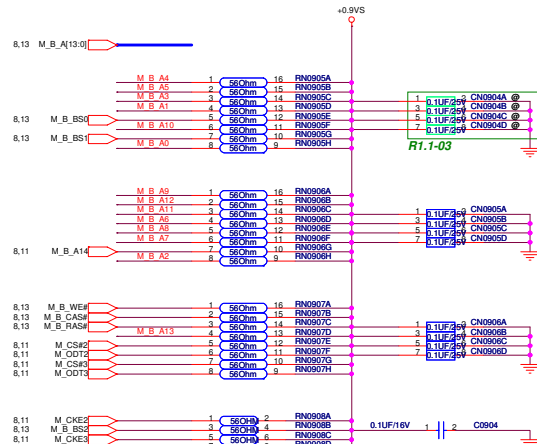
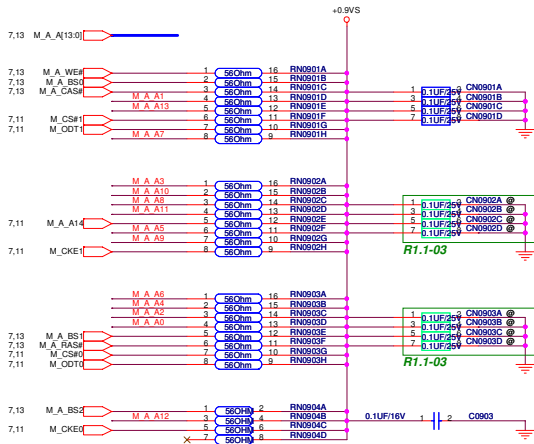
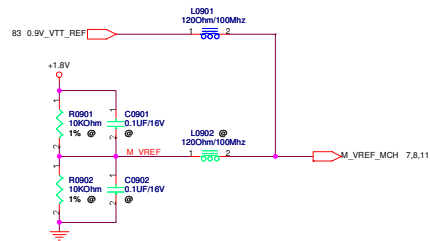
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ASUSTeK COMPUTER INC. (NBI)		Engineer: John Hung	
Size	Project Name		Rev
Custom	M50S/X55S		2.0
Date: Monday, September 03, 2007	Sheet	2	of 55







		Title : CPU****	
ASUSTeK COMPUTER INC. (NBI)		Engineer: John Hung	
Size	Project Name		Rev
Custom	M50S/X55S		2.0
Date: Monday, September 03, 2007		Sheet	8 of 88



7 M_A_DQ[63:0]

U1001D
M A DQ0 AR43 SA DQ 0
M A DQ1 AW44 SA DQ 1
M A DQ2 BA45 SA DQ 2
M A DQ3 AY46 SA DQ 3
M A DQ4 AR41 SA DQ 4
M A DQ5 AR45 SA DQ 5
M A DQ6 AT42 SA DQ 6
M A DQ7 AW47 SA DQ 7
M A DQ8 BA48 SA DQ 8
M A DQ9 BA48 SA DQ 9
M A DQ10 BA47 SA DQ 10
M A DQ11 BA45 SA DQ 11
M A DQ12 BA47 SA DQ 12
M A DQ13 BG50 SA DQ 13
M A DQ14 BA49 SA DQ 14
M A DQ15 BA45 SA DQ 15
M A DQ16 BA44 SA DQ 16
M A DQ17 BA44 SA DQ 17
M A DQ18 BA42 SA DQ 18
M A DQ19 BA40 SA DQ 19
M A DQ20 BA44 SA DQ 20
M A DQ21 BA45 SA DQ 21
M A DQ22 BA40 SA DQ 22
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M A DQ26 BA40 SA DQ 26
M A DQ27 BA40 SA DQ 27
M A DQ28 BA41 SA DQ 28
M A DQ29 BA41 SA DQ 29
M A DQ30 AV38 SA DQ 30
M A DQ31 AT38 SA DQ 31
M A DQ32 AV13 SA DQ 32
M A DQ33 AT13 SA DQ 33
M A DQ34 AW11 SA DQ 34
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M A DQ37 AT11 SA DQ 37
M A DQ38 BA13 SA DQ 38
M A DQ39 BA11 SA DQ 39
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M A DQ44 BG10 SA DQ 44
M A DQ45 AV9 SA DQ 45
M A DQ46 BG07 SA DQ 46
M A DQ47 BA09 SA DQ 47
M A DQ48 BA09 SA DQ 48
M A DQ49 AY7 SA DQ 49
M A DQ50 AT5 SA DQ 50
M A DQ51 AT5 SA DQ 51
M A DQ52 AT5 SA DQ 52
M A DQ53 BA7 SA DQ 53
M A DQ54 BA5 SA DQ 54
M A DQ55 BA9 SA DQ 55
M A DQ56 BA2 SA DQ 56
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M A DQ59 BA2 SA DQ 59
M A DQ60 AT6 SA DQ 60
M A DQ61 AN9 SA DQ 61
M A DQ62 AN9 SA DQ 62
M A DQ63 AN9 SA DQ 63

DDR SYSTEM MEMORY A

SA_BS_0 BB19 M A BS0 7.9
SA_BS_1 BK19 M A BS1 7.9
SA_BS_2 BF19 M A BS2 7.9
SA_CAS# BL17 M A CAS# 7.9
SA_DM_0 AT45 M A DM0
SA_DM_1 BA44 M A DM1
SA_DM_2 BA42 M A DM2
SA_DM_3 AW38 M A DM3
SA_DM_4 AW13 M A DM4
SA_DM_5 BG8 M A DM5
SA_DM_6 AY5 M A DM6
SA_DM_7 AN6 M A DM7
SA_DQS_0 AT46 M A DQS0
SA_DQS_1 BA48 M A DQS1
SA_DQS_2 BA44 M A DQS2
SA_DQS_3 BC37 M A DQS3
SA_DQS_4 BB16 M A DQS4
SA_DQS_5 BA6 M A DQS5
SA_DQS_6 BP2 M A DQS6
SA_DQS_7 AP3 M A DQS7
SA_DQS#_0 AT47 M A DQS#0
SA_DQS#_1 BA47 M A DQS#1
SA_DQS#_2 BA37 M A DQS#2
SA_DQS#_3 BA16 M A DQS#3
SA_DQS#_4 BA16 M A DQS#4
SA_DQS#_5 BA17 M A DQS#5
SA_DQS#_6 BA17 M A DQS#6
SA_DQS#_7 BA17 M A DQS#7
SA_MA_0 BA19 M A A0
SA_MA_1 BA20 M A A1
SA_MA_2 BK28 M A A2
SA_MA_3 BK28 M A A3
SA_MA_4 BK28 M A A4
SA_MA_5 BA27 M A A5
SA_MA_6 BA25 M A A6
SA_MA_7 BA25 M A A7
SA_MA_8 BA25 M A A8
SA_MA_9 BA25 M A A9
SA_MA_10 BA25 M A A10
SA_MA_11 BA25 M A A11
SA_MA_12 BG30 M A A12
SA_MA_13 BG16 M A A13
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SA_RCVEN# AY29 M A RCVEN#
SA_WE# BA19 M A WE# 7.9

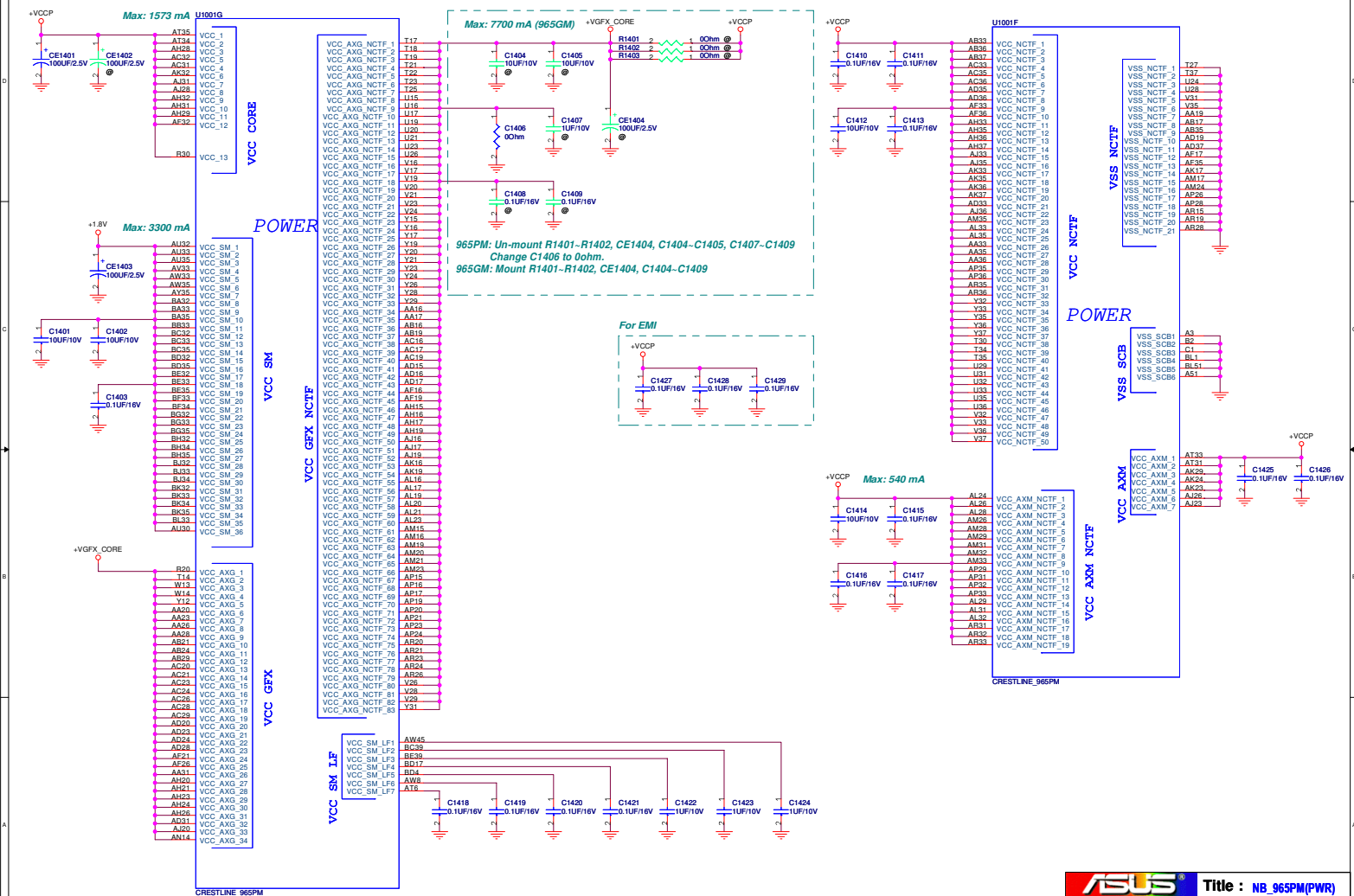
8 M_B_DQ[63:0]

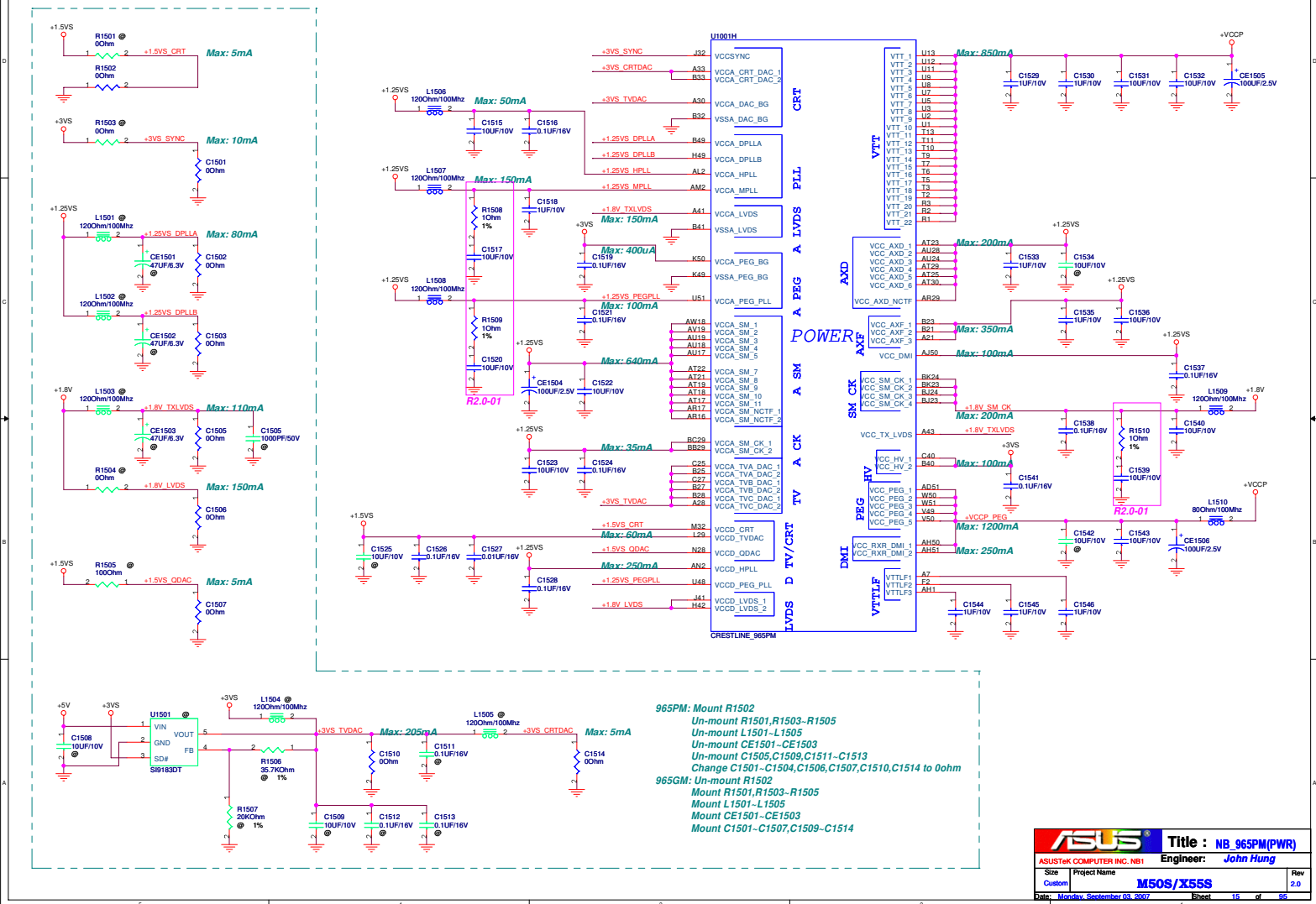
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M B DQ6 AV49 SB DQ 6
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M B DQ9 BA50 SB DQ 9
M B DQ10 BA50 SB DQ 10
M B DQ11 BA51 SB DQ 11
M B DQ12 BA51 SB DQ 12
M B DQ13 AV49 SB DQ 13
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M B DQ63 AT2 SB DQ 63

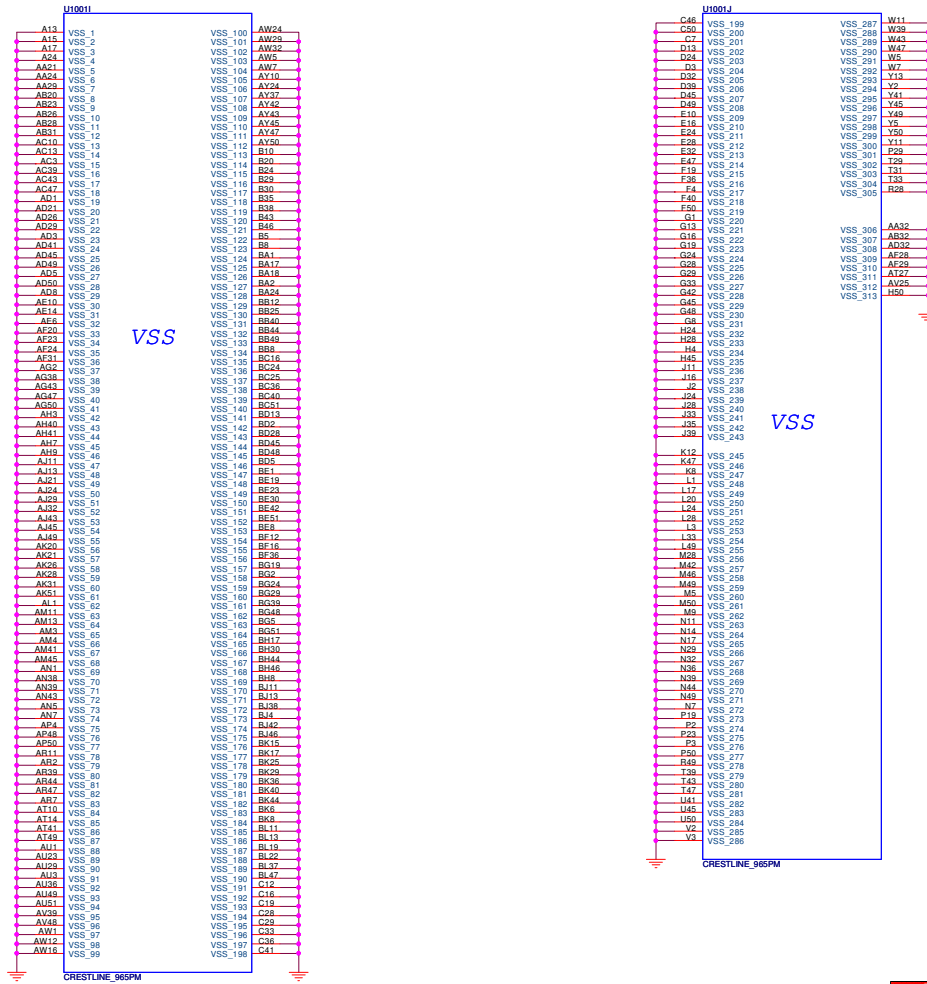
DDR SYSTEM MEMORY B

SB_BS_0 AY17 M B BS0 8.9
SB_BS_1 BG18 M B BS1 8.9
SB_BS_2 BG38 M B BS2 8.9
SB_CAS# BE17 M B CAS# 8.9
SB_DM_0 AR50 M B DM0
SB_DM_1 BA49 M B DM1
SB_DM_2 BA45 M B DM2
SB_DM_3 BA39 M B DM3
SB_DM_4 BA12 M B DM4
SB_DM_5 BA7 M B DM5
SB_DM_6 BA7 M B DM6
SB_DM_7 AW2 M B DM7
SB_DQS_0 AT50 M B DQS0
SB_DQS_1 BA50 M B DQS1
SB_DQS_2 BA46 M B DQS2
SB_DQS_3 BA39 M B DQS3
SB_DQS_4 BA12 M B DQS4
SB_DQS_5 BA7 M B DQS5
SB_DQS_6 BA7 M B DQS6
SB_DQS_7 AV2 M B DQS7
SB_DQS#_0 AU50 M B DQS#0
SB_DQS#_1 BA50 M B DQS#1
SB_DQS#_2 BA46 M B DQS#2
SB_DQS#_3 BA39 M B DQS#3
SB_DQS#_4 BA12 M B DQS#4
SB_DQS#_5 BA7 M B DQS#5
SB_DQS#_6 BA7 M B DQS#6
SB_DQS#_7 AV2 M B DQS#7
SB_MA_0 BA18 M B A0
SB_MA_1 BG28 M B A1
SB_MA_2 BG25 M B A2
SB_MA_3 AW17 M B A3
SB_MA_4 BA25 M B A4
SB_MA_5 BA25 M B A5
SB_MA_6 BA25 M B A6
SB_MA_7 BA25 M B A7
SB_MA_8 BA25 M B A8
SB_MA_9 BA25 M B A9
SB_MA_10 BA25 M B A10
SB_MA_11 BA25 M B A11
SB_MA_12 BA25 M B A12
SB_MA_13 BG13 M B A13
SB_RAS# AV18 M B RAS# 8.9
SB_RCVEN# AY18 M B RCVEN#
SB_WE# BC17 M B WE# 8.9

CRESTLINE_965PM







		Title : NB ****	
ASUSTEK COMPUTER INC. (NBI)		Engineer: John Hung	
Size	Project Name		Rev
Custom	M50S/X55S		2.0
Date: Monday, September 03, 2007		Sheet	17 of 55



		Title : NB ****	
ASUSTEK COMPUTER INC. (NEI)		Engineer: John Hung	
Size	Project Name		Rev
Custom	M50S/X55S		2.0
Date: Monday, September 03, 2007		Sheet	18 of 55

		Title : MEM ****	
ASUSTEK COMPUTER INC. NEI		Engineer: John Hung	
Size	Project Name		Rev
Custom	M50S/X55S		2.0
Date: Monday, September 03, 2007		Sheet	19 of 55

ICH_TP3, ACZ_SDOUT : XOR Chain Entrance Strap

00 = Reserved
01 = Enter XOR Chain
10 = Normal Operation (D)
11 = Set PCIe Port Config Bit 1

GNT0#, SPI_CS1 : ICH8 Boot BIOS Select

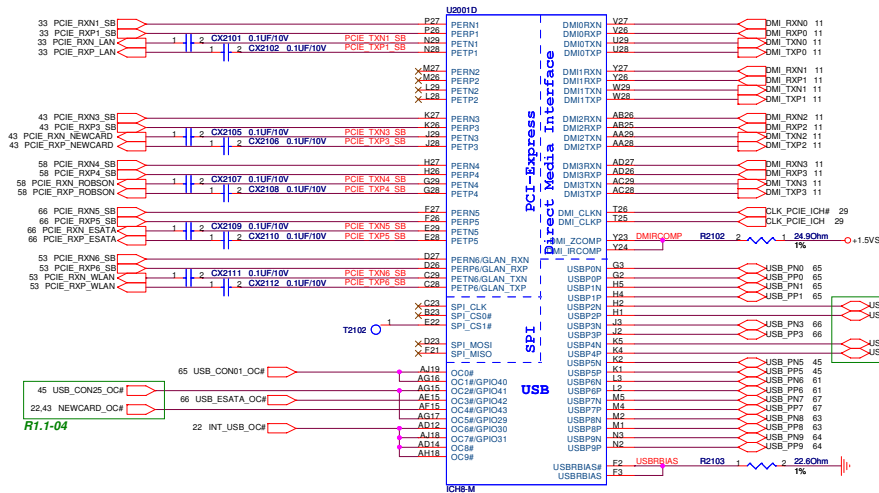
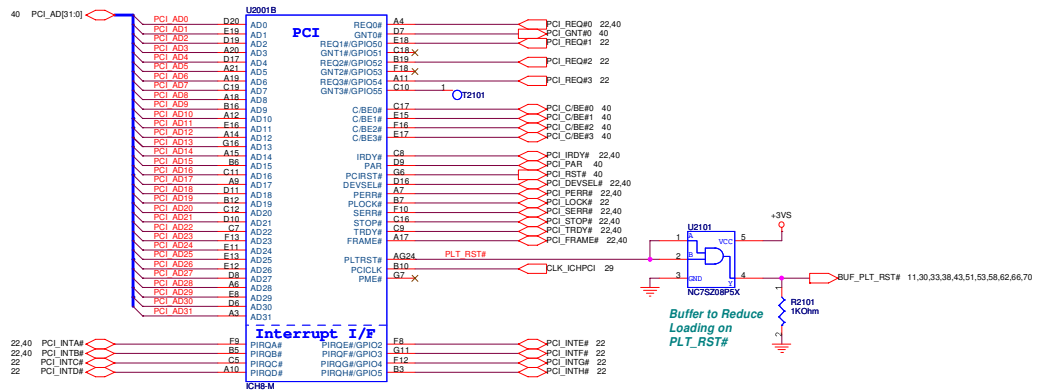
00 = Reserved
01 = SPI
10 = PCI
11 = LPC (D)

GNT2# : PCIe Port Configuration 2(Port 5/6)

0 = Port 5 (x2)
1 = Port 5 (x1), Port 6(x1) (D)

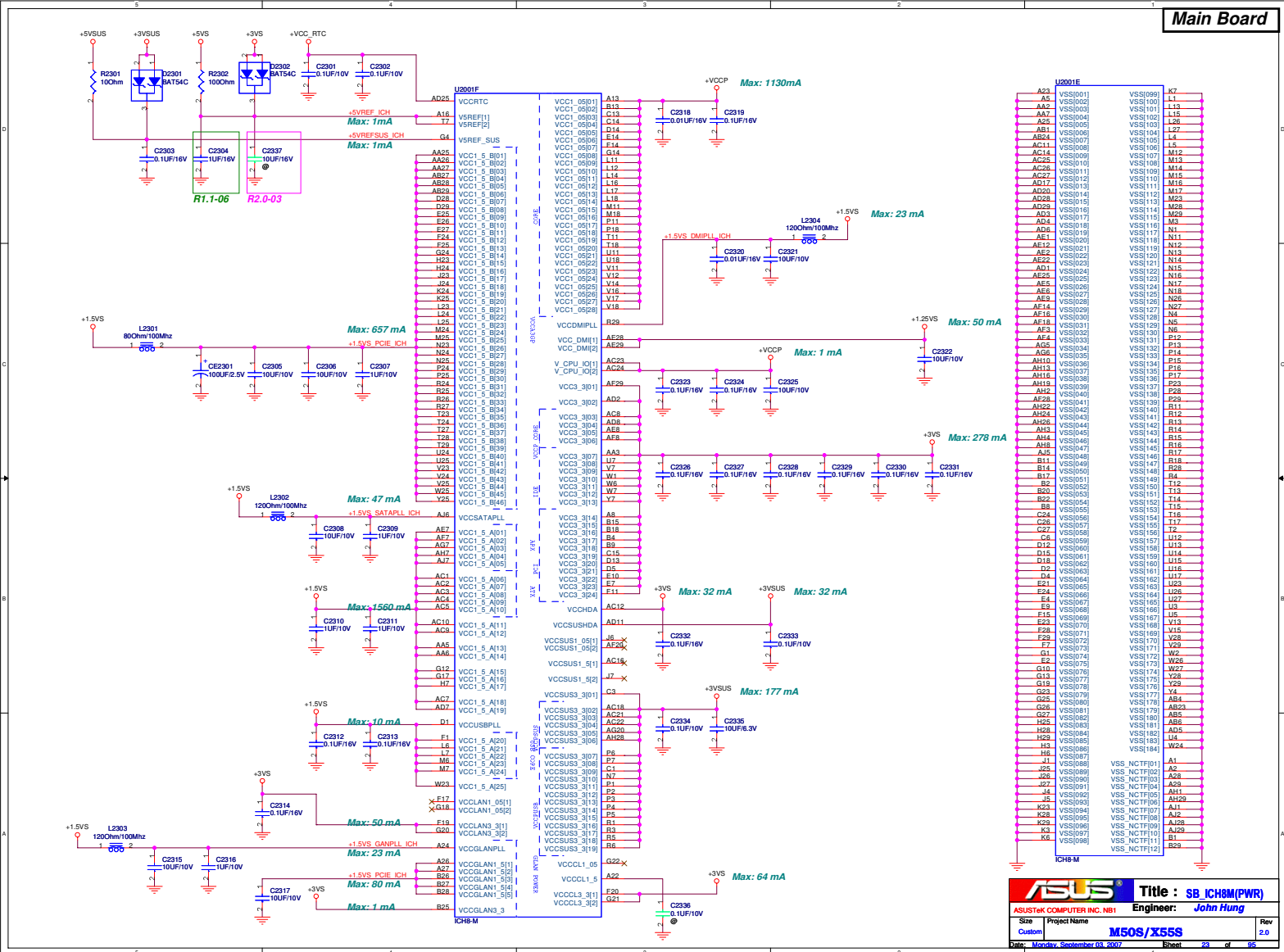
GNT3# : A16 Swap override strip

0 = Enable
1 = Default (D)



USB 0	USB Conn.
USB 1	USB Conn.
USB 2	USB Conn.
USB 3	eSATA/USB
USB 4	NewCard
USB 5	Camera
USB 6	Bluetooth
USB 7	3G Card
USB 8	Fingerprint
USB 9	TV Tuner

ASUS		Title : SB_ICH8M(2)	
ASUSTeK COMPUTER INC. NE1		Engineer: John Hung	
Size	Project Name	Rev	
Custom	M50S/X55S	2.0	
Date: Monday, September 03, 2007	Sheet	21	of 55





		Title : SB_****	
ASUSTEK COMPUTER INC. (NEI)		Engineer: John Hung	
Size	Project Name		Rev
Custom	M50S/X55S		2.0
Date: Monday, September 03, 2007		Sheet	24 of 55

		Title : SB_***	
ASUSTeK COMPUTER INC. (NBI)		Engineer: John Hung	
Size	Project Name		Rev
Custom	M50S/X55S		2.0
Date: Monday, September 03, 2007		Sheet	25 of 55



Title : SB_***

ASUSTeK COMPUTER INC. (NBI)

Engineer: John Hung

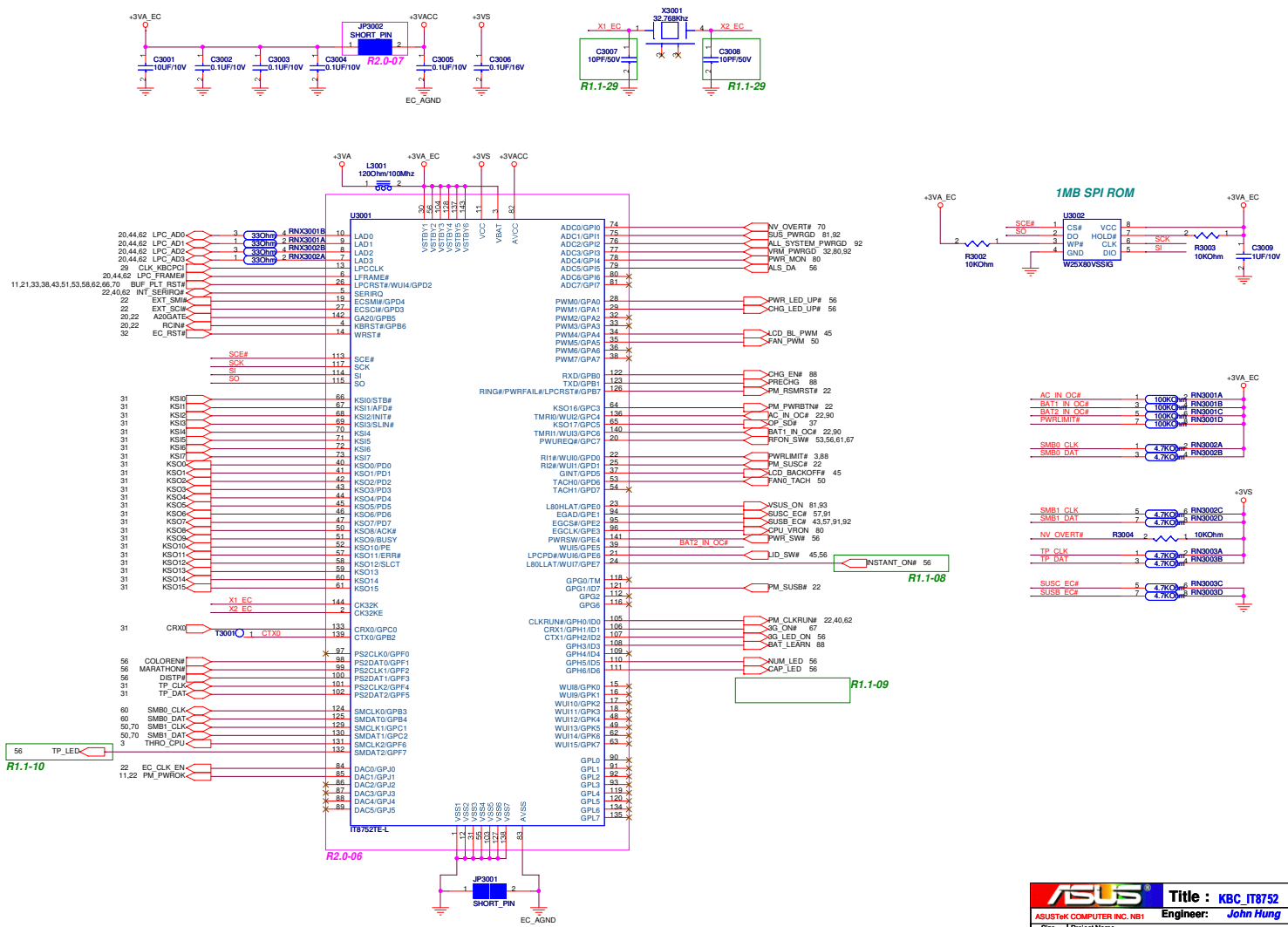
Size	Project Name	Rev
Custom	M50S/X55S	2.0

Date: Monday, September 03, 2007Sheet 26 of 55

		Title : SB_***	
ASUSTeK COMPUTER INC. (NBI)		Engineer: John Hung	
Size	Project Name		Rev
Custom	M50S/X55S		2.0
Date: Monday, September 03, 2007		Sheet	27 of 55

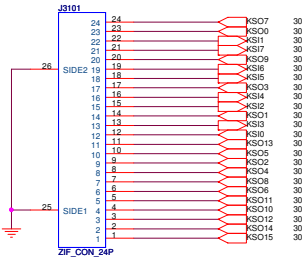
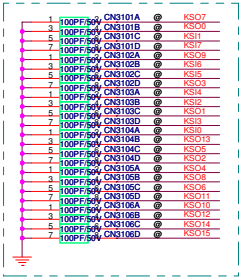


		Title : SB_****	
ASUSTEK COMPUTER INC. (NEI)		Engineer: John Hung	
Size	Project Name		Rev
Custom	M50S/X55S		2.0
Date: Monday, September 03, 2007		Sheet	28 of 55

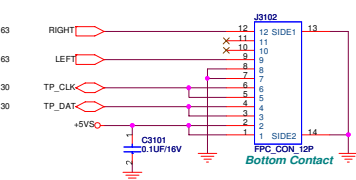


Keyboard

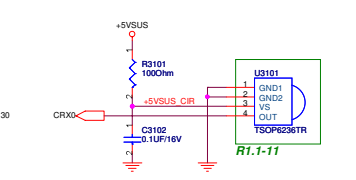
EMI



Touchpad

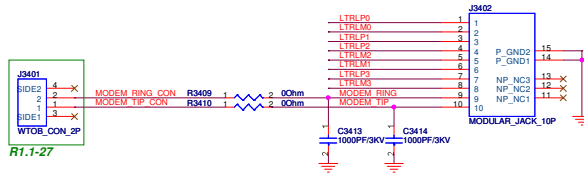
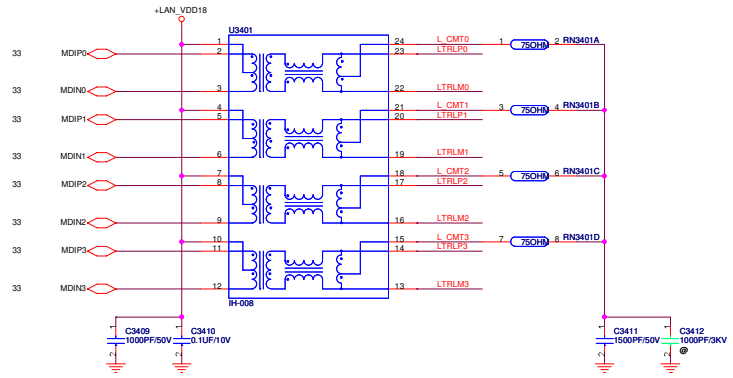
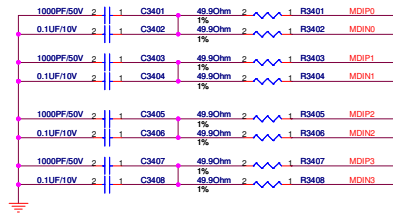


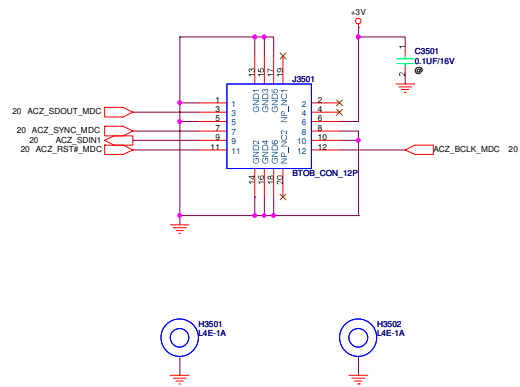
CIR



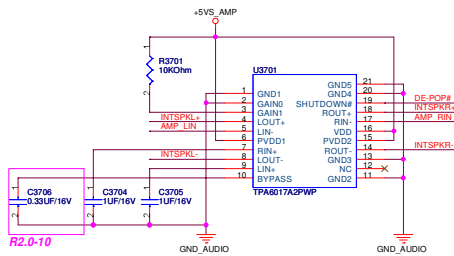
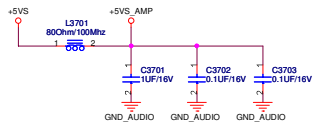
R1.1-12



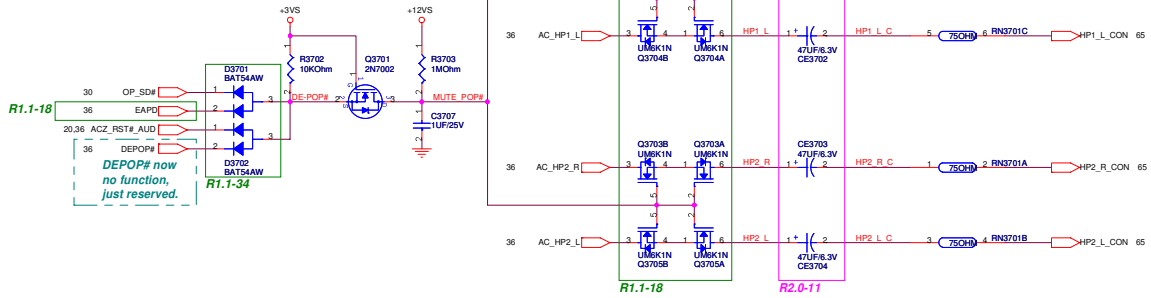
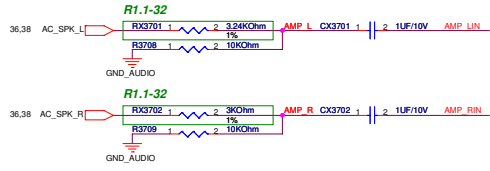
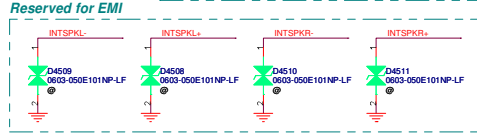
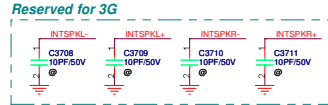
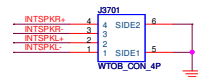


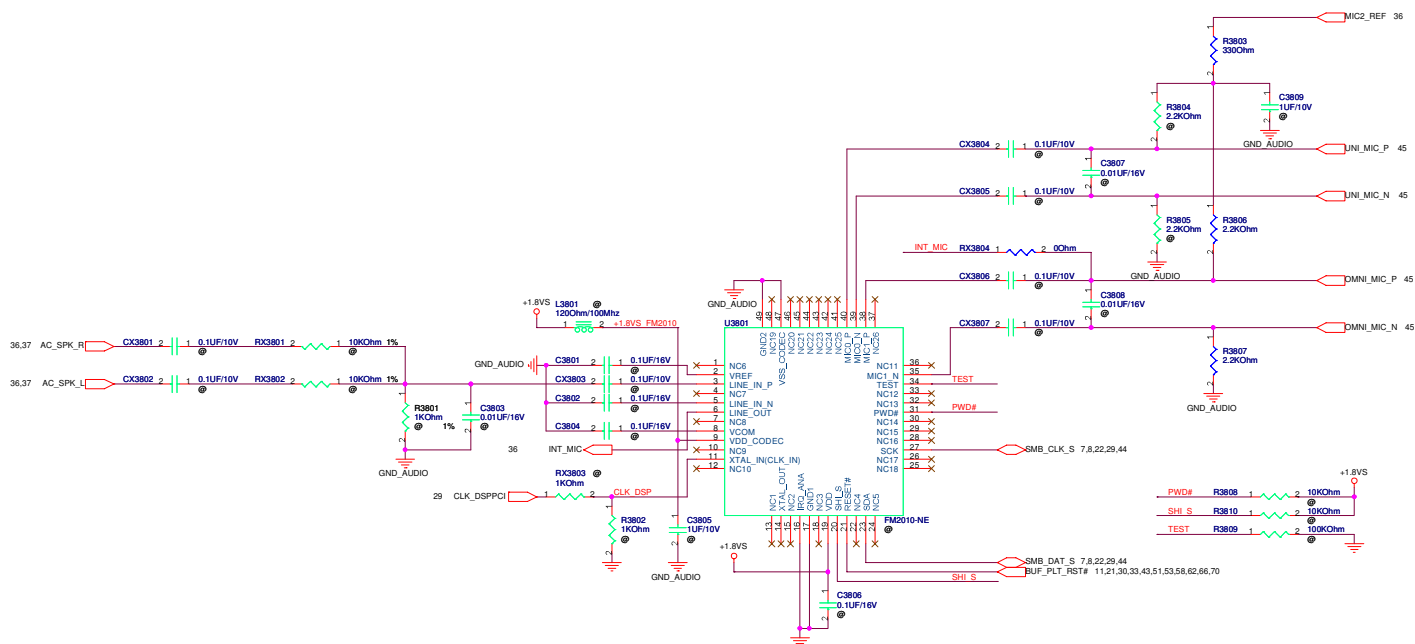


		Title : LAN_MDC	
ASUSTeK COMPUTER INC. (NBI)		Engineer: John Hung	
Size	Project Name	Rev	
Custom	M50S/X55S	2.0	
Date: Monday, September 03, 2007		Sheet	35 of 55



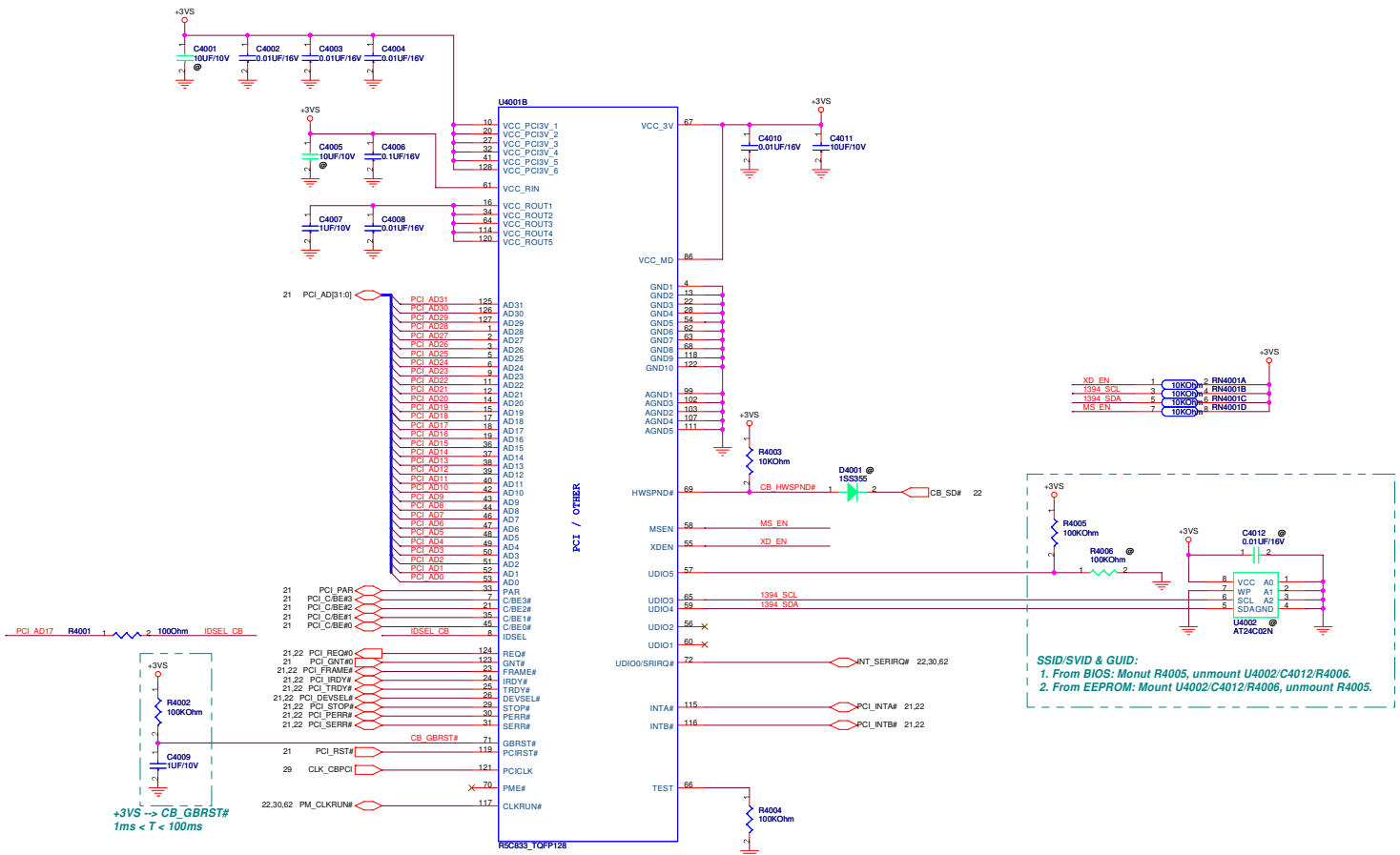
Internal Speaker Conn.

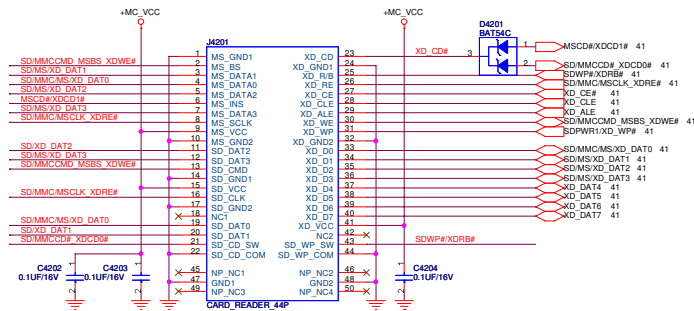
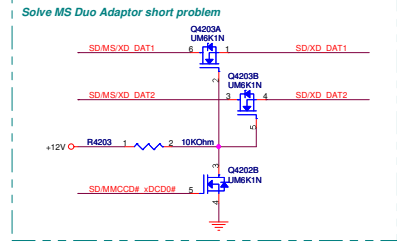
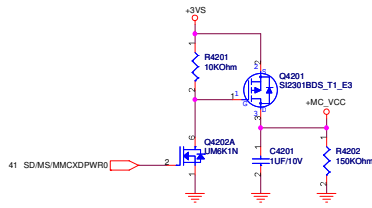


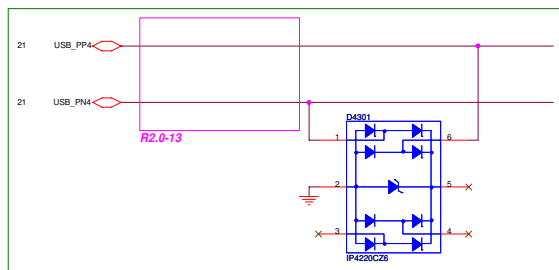


ASUS		Title : AUD_FM2010	
ASUSTek COMPUTER INC. NE1		Engineer: John Hung	
Size	Project Name		Rev
Custom	M50S/X55S		2.0
Date: Tuesday, September 04, 2017	Sheet	38	of 55

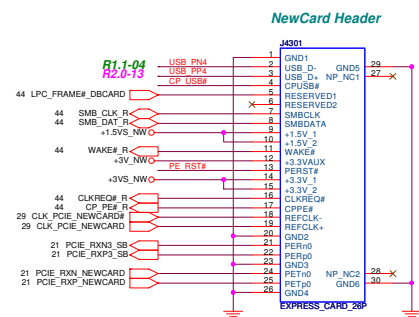
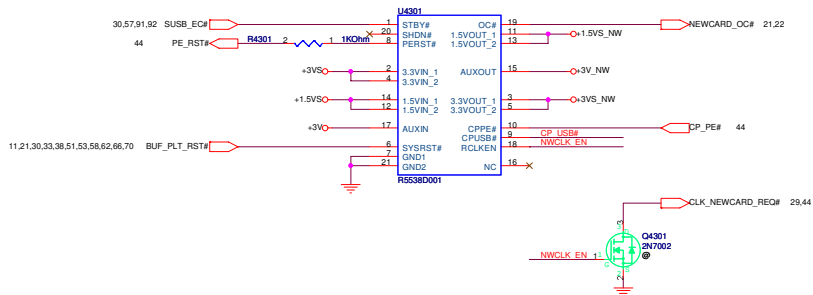
		Title : AUD ****	
ASUSTEK COMPUTER INC. NEI		Engineer: John Hung	
Size	Project Name		Rev
Custom	M50S/X55S		2.0
Date: Monday, September 03, 2007		Sheet	39 of 55



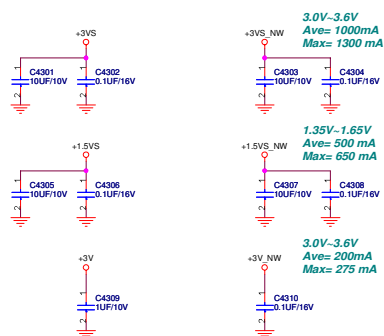
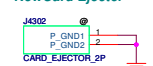




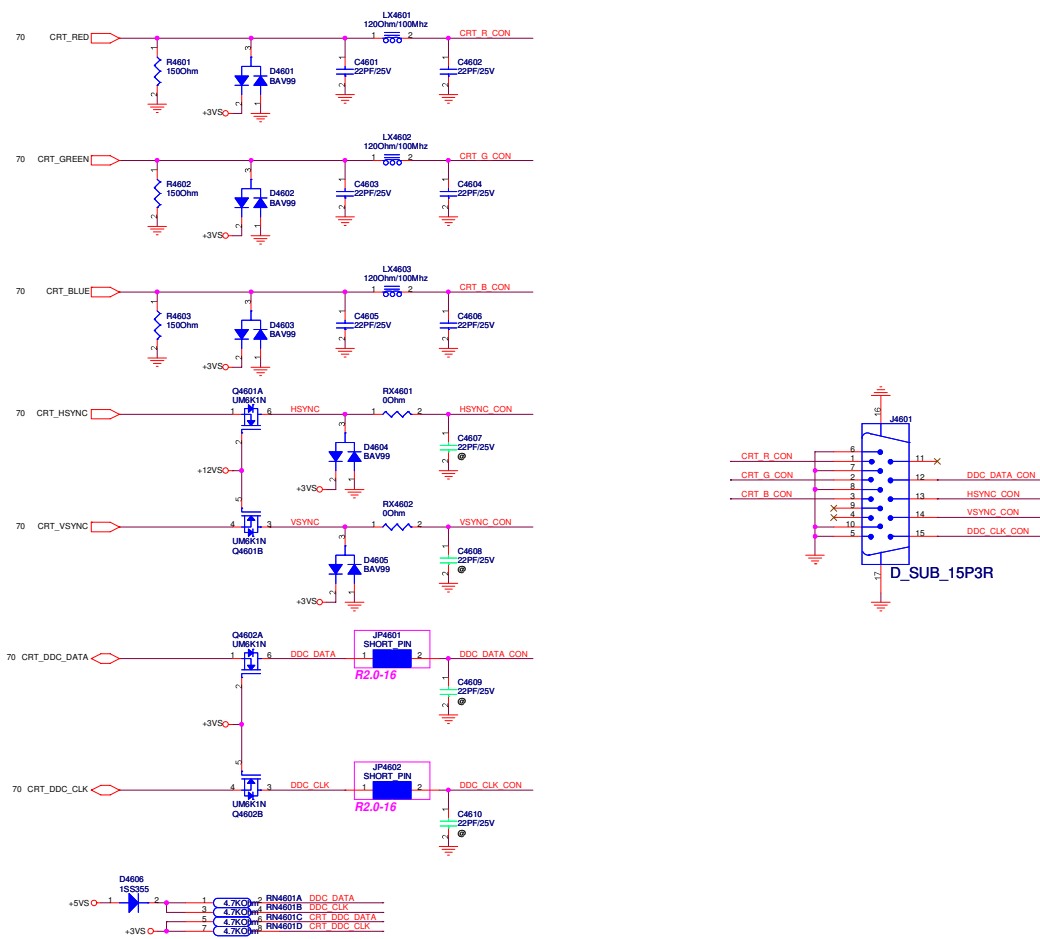
R1.1-04

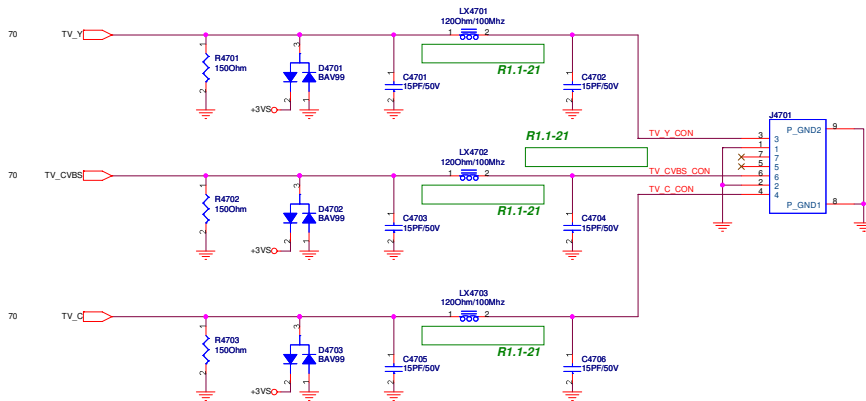


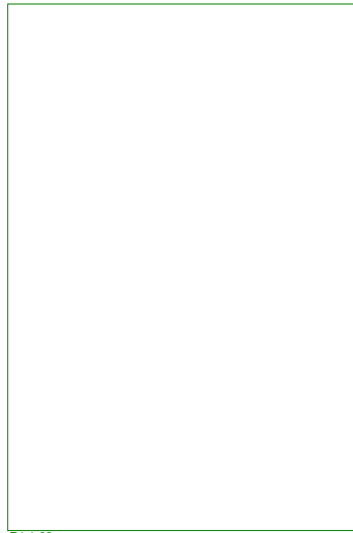
NewCard Ejector



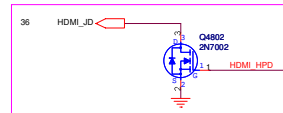
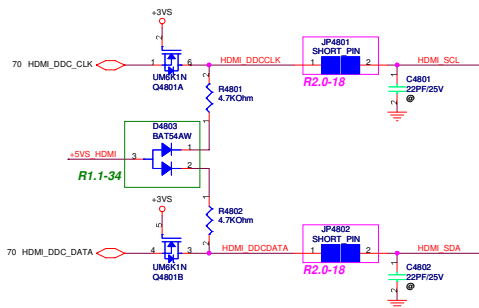
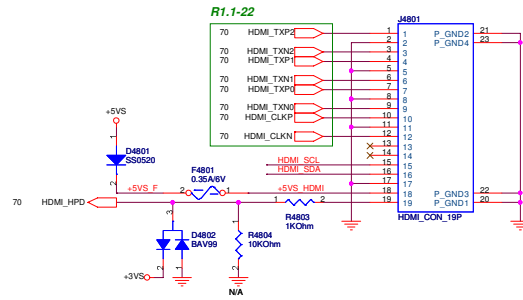
ASUS		Title : CB_NewCard	
ASUSTek COMPUTER INC. NE1		Engineer: John Hung	
Size	Project Name		Rev
Custom	M50S/X55S		1.0
Date: Monday, September 03, 2007		Sheet	43 of 55







R1.1-22

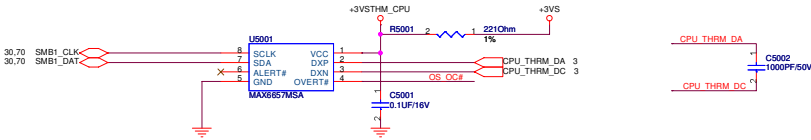


R2.0-17

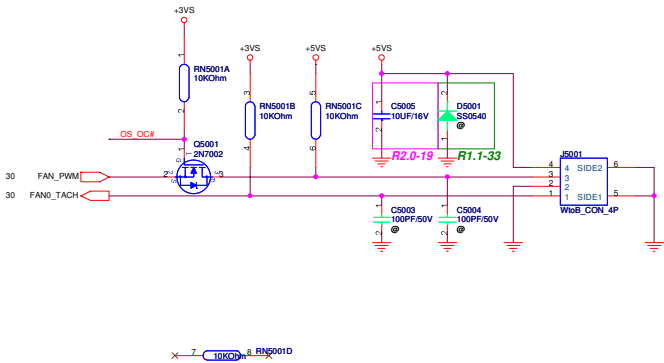
ASUS		Title : CRT_HDMI	
ASUSTeK COMPUTER INC. NE1		Engineer: John Hung	
Size	Project Name	Rev	
Custom	M50S/X55S	2.0	
Date: Monday, September 03, 2007		Sheet	48 of 55

		Title : TV ****	
ASUSTEK COMPUTER INC. NEI		Engineer: John Hung	
Size	Project Name		Rev
Custom	M50S/X55S		2.0
Date: Monday, September 03, 2007		Sheet	49 of 55

CPU Thermal Sensor



PWM Fan



X 7 10KOhm 8 RN5001D

ASUS		Title : FAN Fan & Sensor	
ASUSTeK COMPUTER INC. NE1		Engineer: John Hung	
Size	Project Name	Rev	
Custom	M50S/X55S	2.0	
Date: Monday, September 03, 2022		Sheet	50 of 55

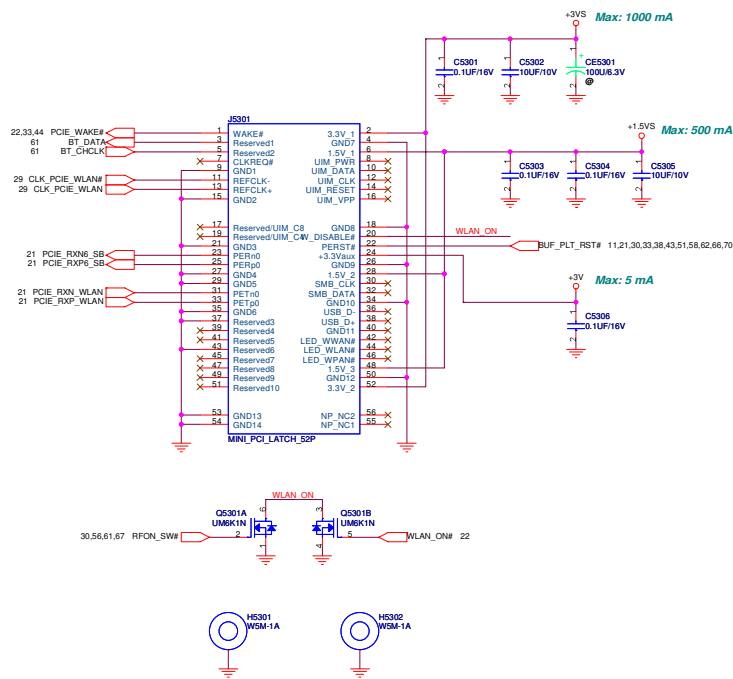


Title : USB ****

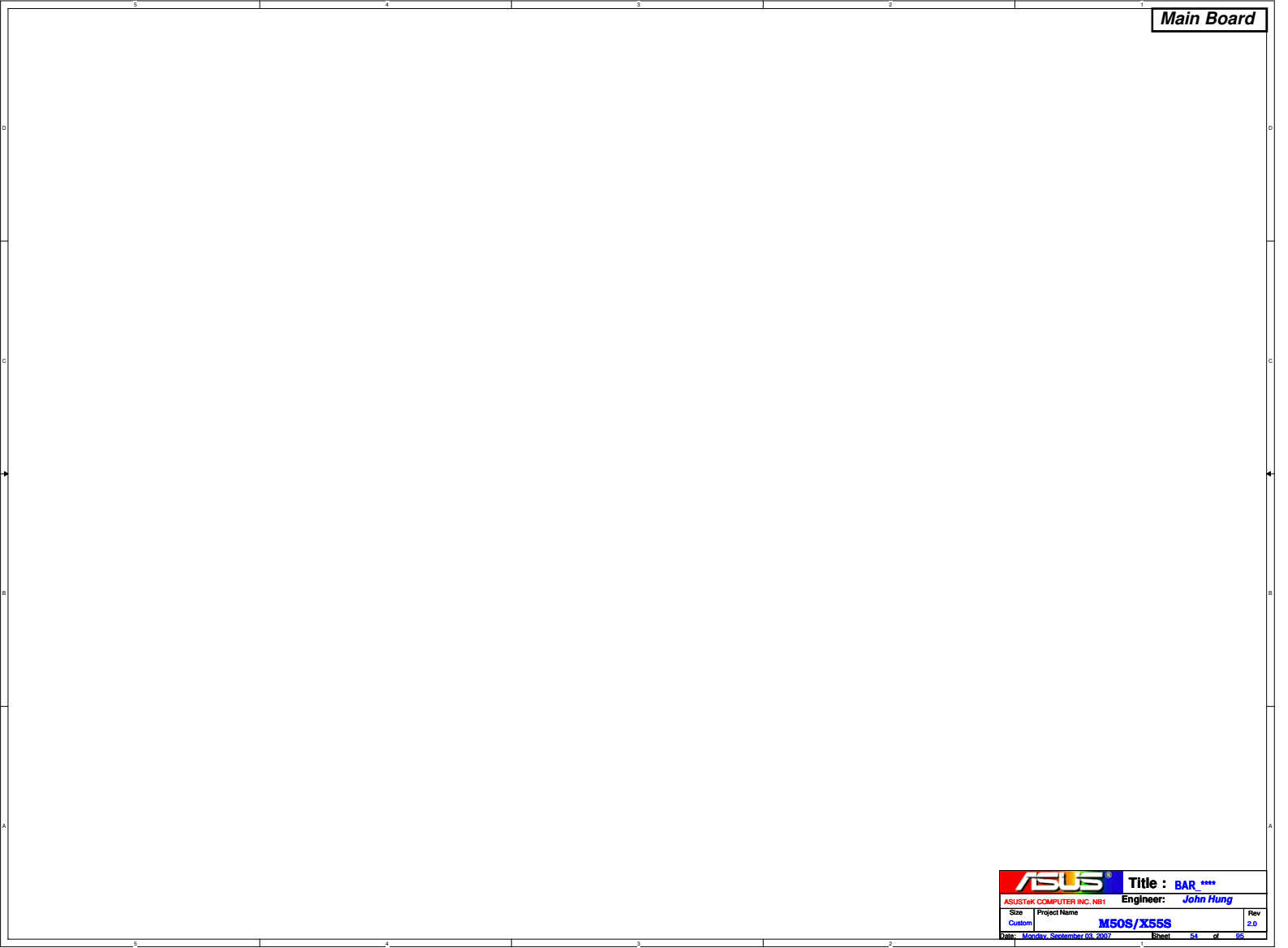
ASUSTeK COMPUTER INC. (NBI)

Engineer: John Hung

Size	Project Name	Rev
Custom	M50S/X55S	2.0
Date: Monday, September 03, 2007		Sheet 52 of 55



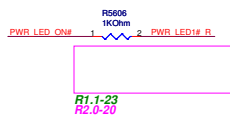
ASUS		Title : PCI WLAN	
ASUSTeK COMPUTER INC. NBI		Engineer: John Hung	
Size	Project Name	Rev	
Custom	M50S/X55S	2.0	
Date: Tuesday, September 04, 2017	Sheet	53	of 55



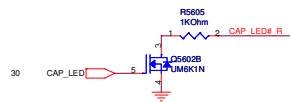
		Title : BAR ****	
ASUSTEK COMPUTER INC. NE1		Engineer: John Hung	
Size	Project Name		Rev
Custom	M50S/X55S		2.0
Date: Monday, September 03, 2007		Sheet	54 of 55

		Title : SIO ****	
ASUSTEK COMPUTER INC. NEI		Engineer: John Hung	
Size	Project Name		Rev
Custom	M50S/X55S		2.0
Date: Monday, September 03, 2007		Sheet	55 of 55

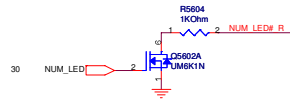
Power LED



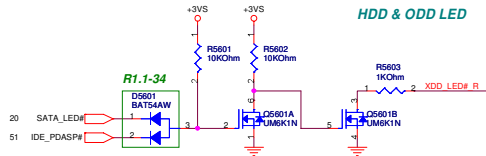
Cap Lock LED



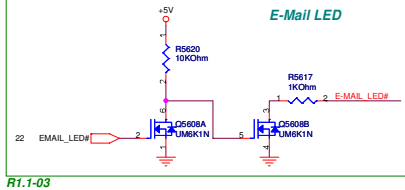
Num Lock LED



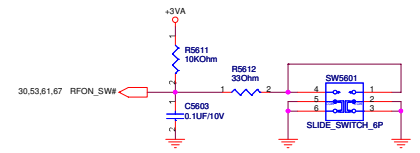
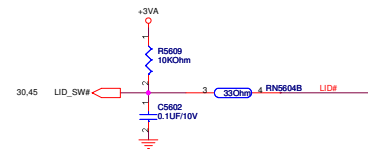
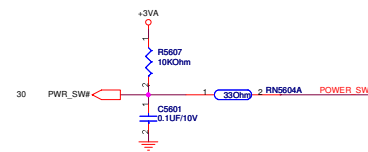
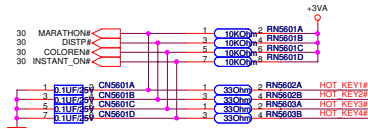
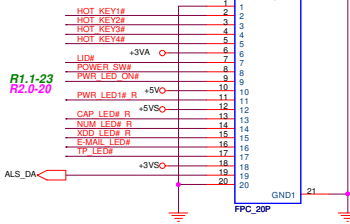
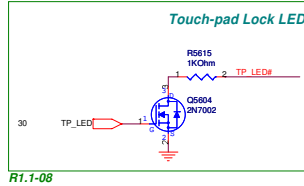
HDD & ODD LED



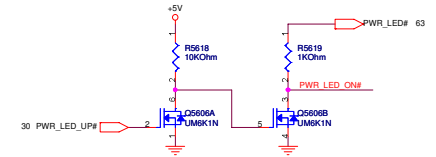
E-Mail LED



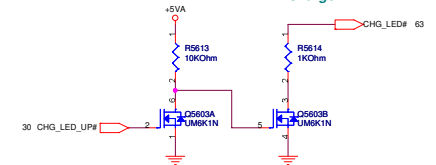
Touch-pad Lock LED



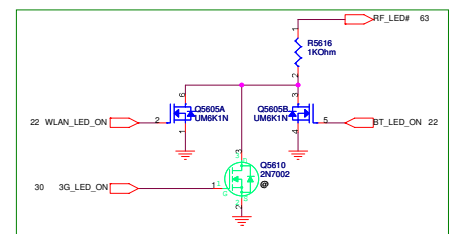
Power LED

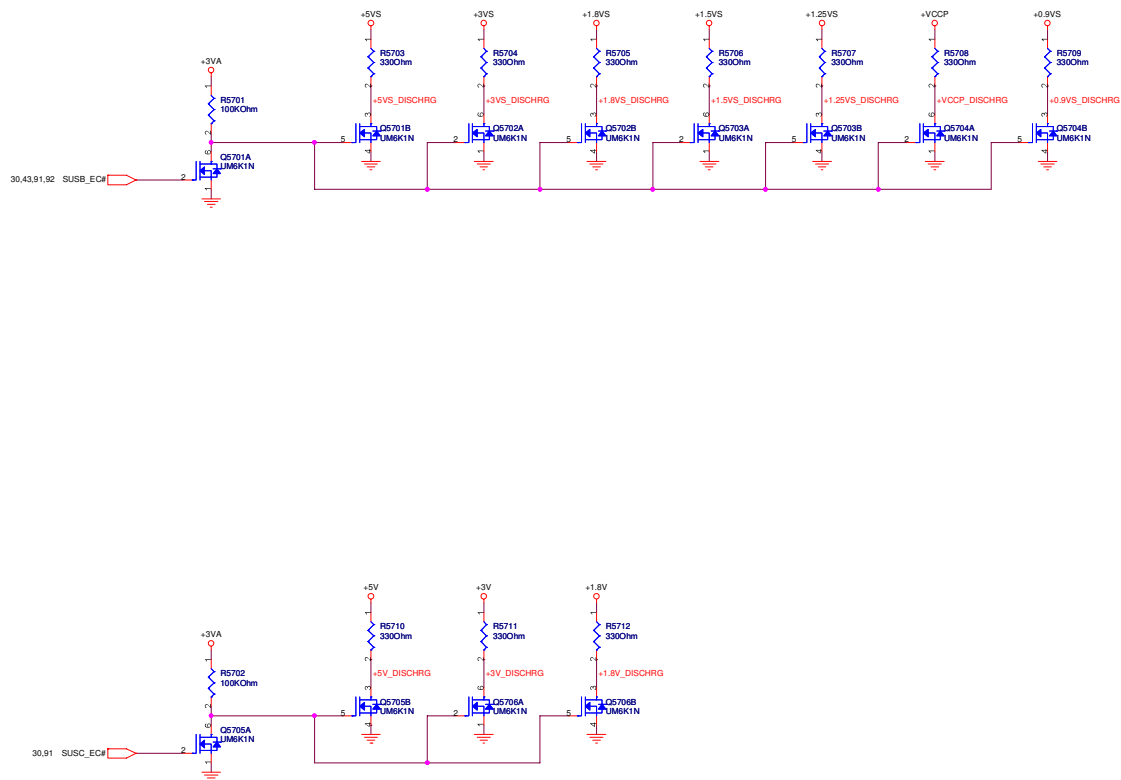


Charger LED

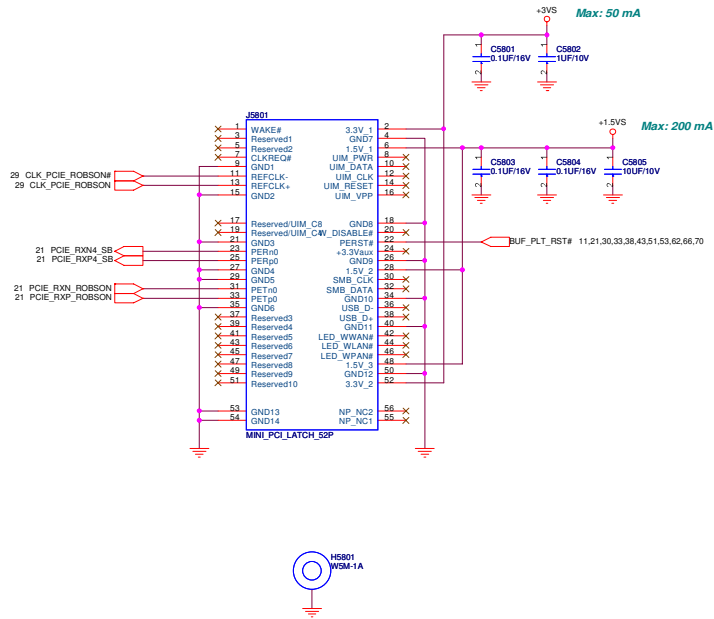


WLAN LED





ASUS		Title : DSG Discharge	
ASUSTek COMPUTER INC. NE1		Engineer: John Hung	
Size	Project Name	Rev	
Custom	M50S/X55S	2.0	
Date: Monday, September 03, 2007		Sheet	57 of 55





Title : DJ ****

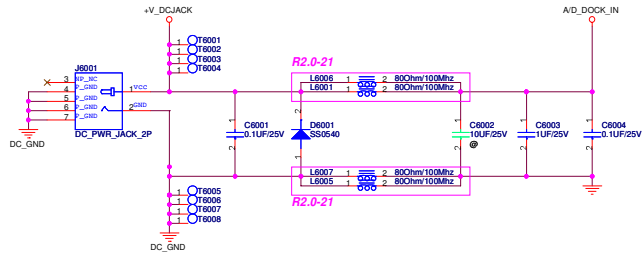
ASUSTeK COMPUTER INC. (NBI)

Engineer: John Hung

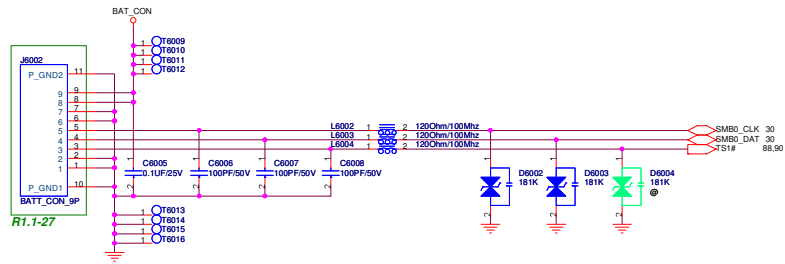
Size	Project Name	Rev
Custom	M50S/X55S	2.0

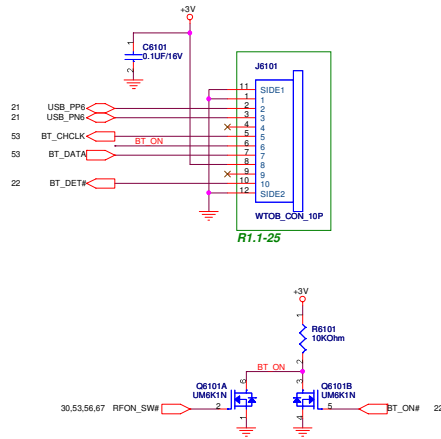
Date: Monday, September 03, 2007Sheet 59 of 59

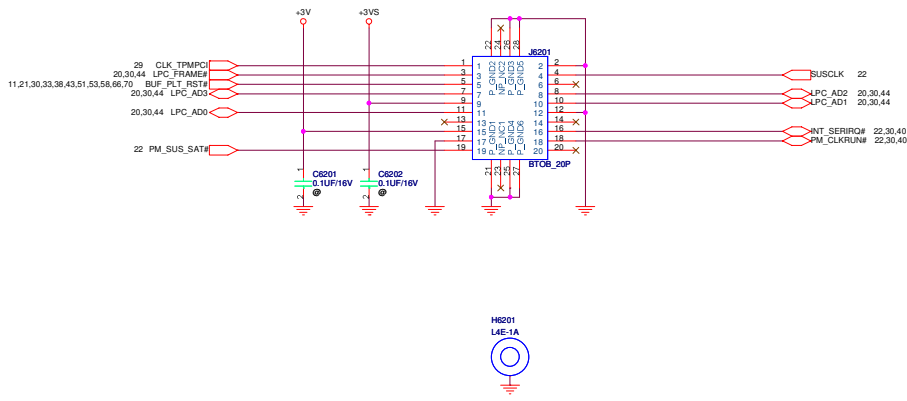
DC Jack

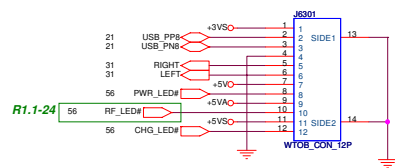


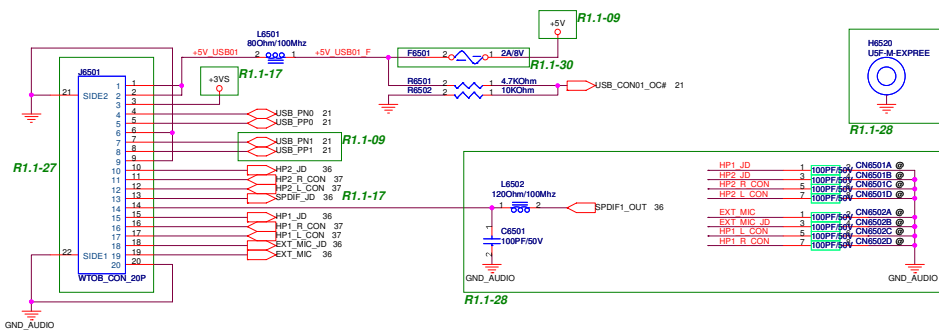
Battery Connector



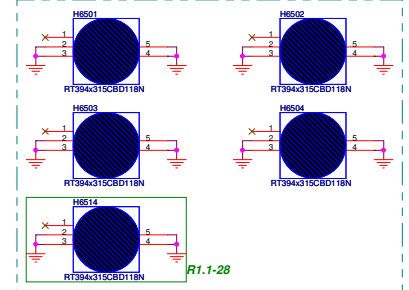








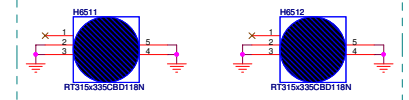
Screw Hole A



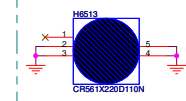
Screw Hole B



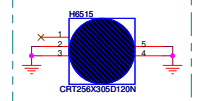
Screw Hole C



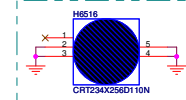
Screw Hole F



Screw Hole H



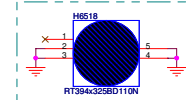
Screw Hole I



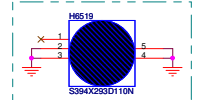
Screw Hole J

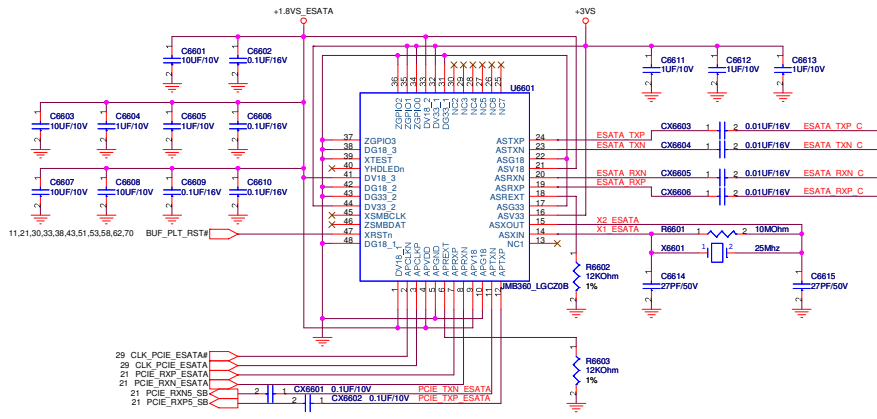


Screw Hole K



Screw Hole L



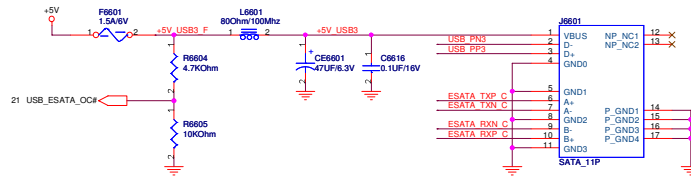
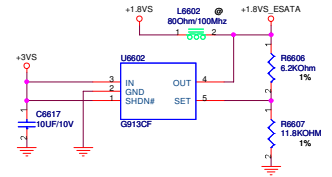
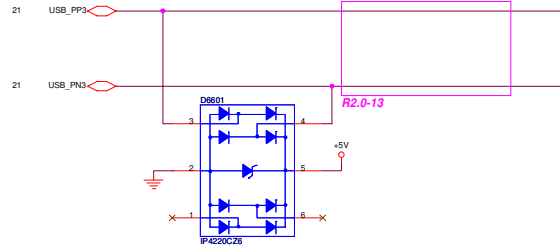


ZGPIO : Clock Type of PCI Express
0 = 25MHz Oscillator (D)
1 = 100MHz from PCI Express Finger

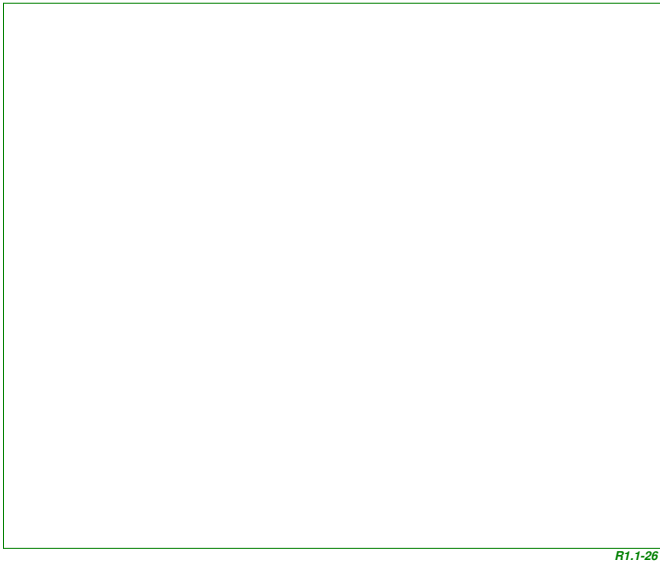
ZGPI1 : Clock Source of SATA II
0 = from Internal Clock Source (D)
1 = from ASXIN & ASXOUT

ZGPI2 : Interface to Debug Registers
0 = SMBus I/F (D)
1 = Reserved

ZGPI2 : SMBus ID Address
0 = 8'h44 (D)
1 = 8'h4A



ASUS		Title : ESA JMB360	
ASUSTek COMPUTER INC. NE1		Engineer: John Hung	
Size	Project Name	Rev	
Custom	M50S/X55S	2.0	
Date: Monday, September 03, 2007		Sheet	66 of 88



R1.1-26

		Title : OTH_****	
ASUSTEK COMPUTER INC. (NEI)		Engineer: John Hung	
Size	Project Name		Rev
Custom	M50S/X55S		2.0
Date: Monday, September 03, 2007		Sheet	68 of 68

		Title : OTH_****	
ASUSTeK COMPUTER INC. (NBI)		Engineer: John Hung	
Size	Project Name		Rev
Custom	M50S/X55S		2.0
Date: Monday, September 03, 2007		Sheet	89 of 88



Title : **VGA ******

ASUSTeK COMPUTER INC. (NBI)


Engineer: **John Hung**

Size	Project Name	Rev
Custom	M50S/X55S	1.0

Date: **Monday, September 03, 2007**

Sheet **71** of **88**

		Title : VGA_****	
ASUSTEK COMPUTER INC. (NEI)		Engineer: John Hung	
Size	Project Name		Rev
Custom	M50S/X55S		1.0
Date: Monday, September 03, 2007		Sheet	72 of 88

		Title : VGA ****	
ASUSTEK COMPUTER INC. (NEI)		Engineer: John Hung	
Size	Project Name		Rev
Custom	M50S/X55S		1.0
Date: Monday, September 03, 2007		Sheet	73 of 88

		Title : VGA_****	
ASUSTEK COMPUTER INC. NEI		Engineer: John Hung	
Size	Project Name		Rev
Custom	M50S/X55S		2.0
Date: Monday, September 03, 2007		Sheet	74 of 88

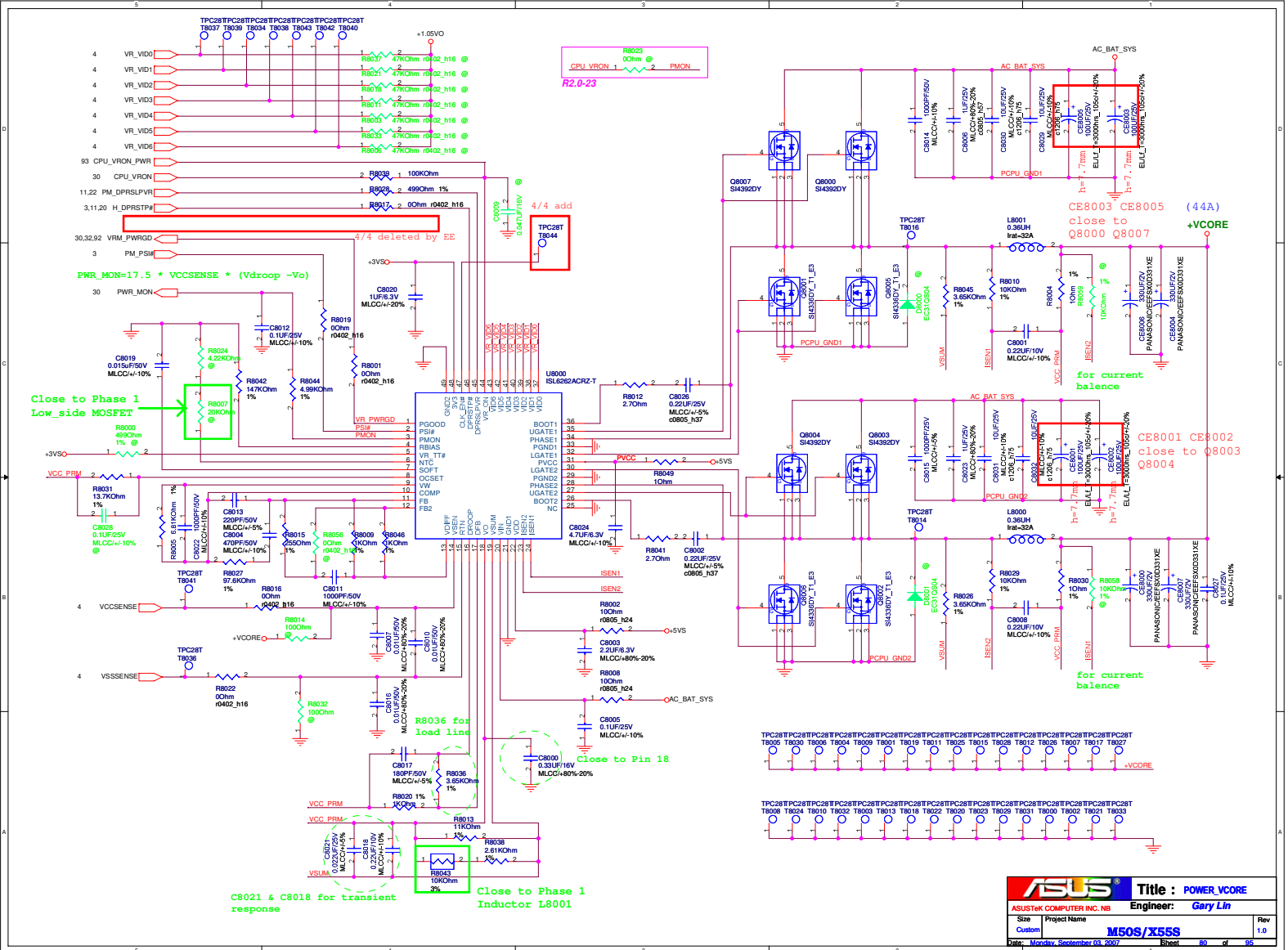
		Title : VGA_****	
ASUSTEK COMPUTER INC. NEI		Engineer: John Hung	
Size	Project Name		Rev
Custom	M50S/X55S		2.0
Date: Monday, September 03, 2007		Sheet	75 of 88

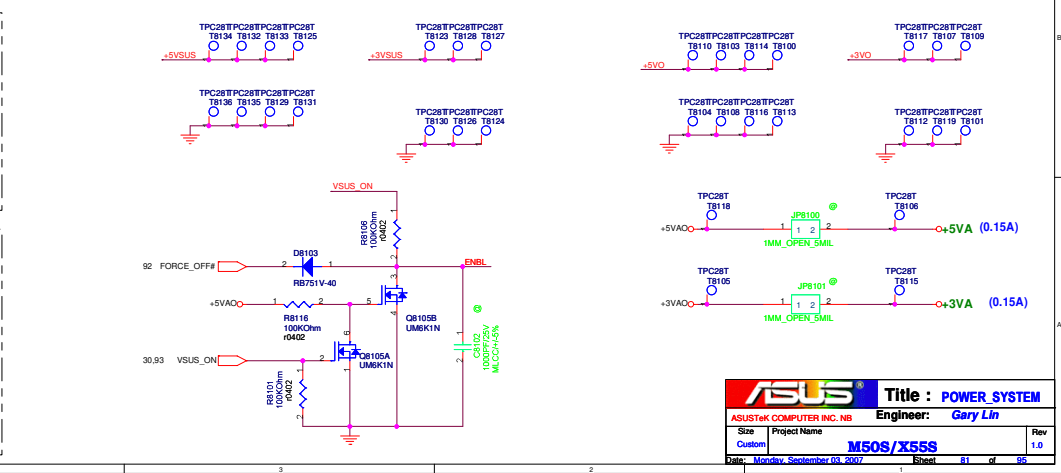
		Title : VGA_****	
ASUSTEK COMPUTER INC. (NEI)		Engineer: John Hung	
Size	Project Name		Rev
Custom	M50S/X55S		2.0
Date: Monday, September 03, 2007		Sheet	76 of 88

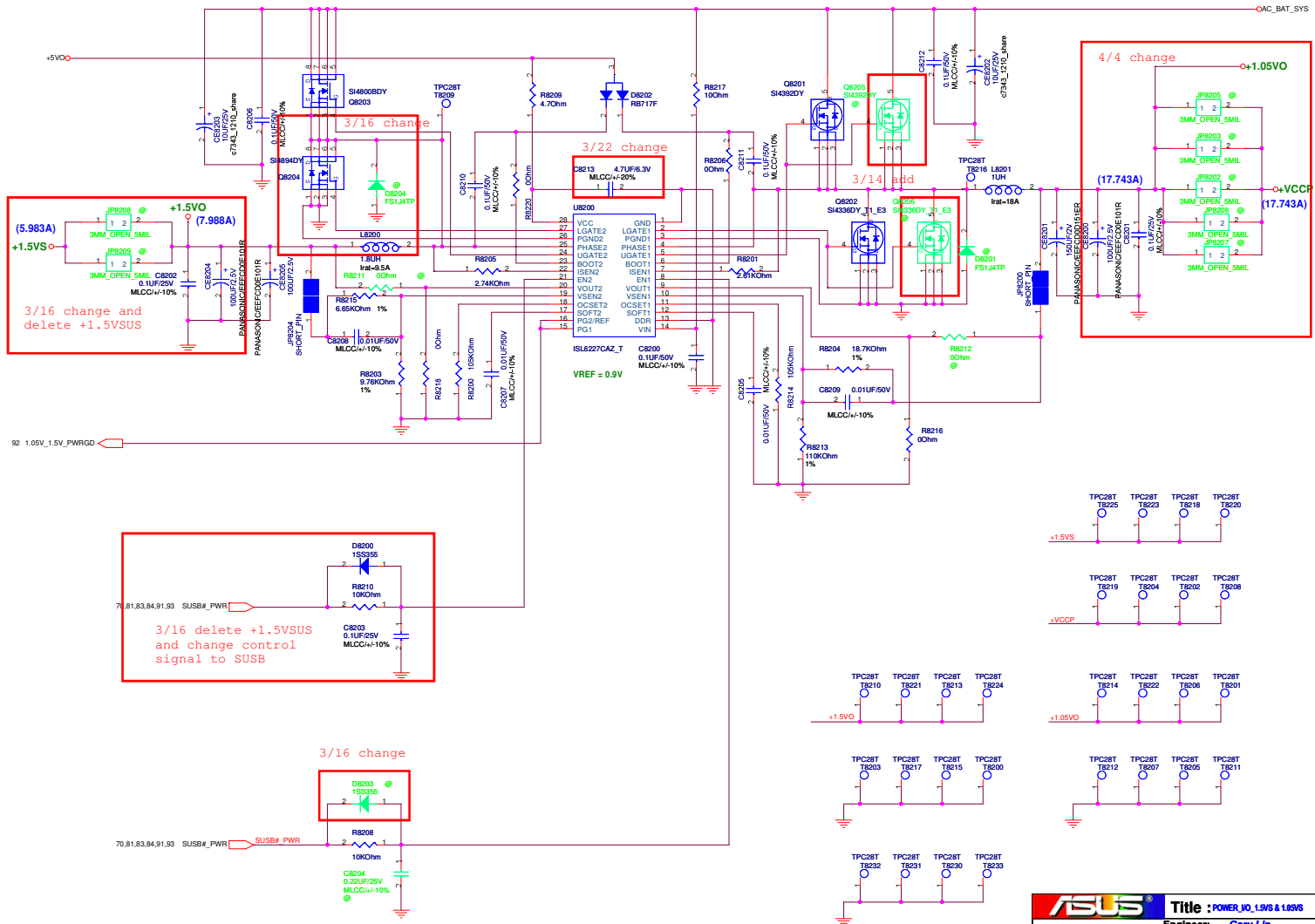
		Title : VGA_****	
ASUSTEK COMPUTER INC. (NEI)		Engineer: John Hung	
Size	Project Name		Rev
Custom	M50S/X55S		2.0
Date: Monday, September 03, 2007		Sheet	77 of 88

		Title : VGA_****	
ASUSTEK COMPUTER INC. (NEI)		Engineer: John Hung	
Size	Project Name		Rev
Custom	M50S/X55S		2.0
Date: Monday, September 03, 2007		Sheet	78 of 88

		Title : VGA_****	
ASUSTEK COMPUTER INC. NEI		Engineer: John Hung	
Size	Project Name		Rev
Custom	M50S/X55S		2.0
Date: Monday, September 03, 2007		Sheet	79 of 88







3/14 EE modify to daughter,so delete this page

		Title : N/A	
ASUSTEK COMPUTER INC. NB		Engineer: Gary Lin	
Size	Project Name		Rev
Custom	M50S/X55S		1.0
Date: Monday, September 03, 2007		Sheet	85 of 85

		Title : N/A	
ASUSTek COMPUTER INC. NB		Engineer: Gary Lin	
Size Custom	Project Name <div style="text-align: center; font-size: 1.2em; font-weight: bold;">M50S/X55S</div>		Rev 1.0
Date: Monday, September 03, 2007		Sheet 86	of 95

		Title : <i>N/A</i>	
ASUSTeK COMPUTER INC. NB		Engineer: <i>Gary Lin</i>	
Size Custom	Project Name <div style="text-align: center; font-size: 1.2em; font-weight: bold;">M50S/X55S</div>		Rev 1.0
Date: <i>Monday, September 03, 2007</i>		Sheet <i>87</i>	of <i>95</i>

POWER PATH & BAT_LEARN

90 WATT

● AC_In Threshold: 2.048Vmax AD_DOCK_IN
> 17.44V active
Adapter In(mv) = [0.075V/Rsense/Adm]/[VCLS/VREF]
Rsense=42mΩ/0.000m
VCLS=2.534V
=> In(mv)=1.5A
=> Constant Power = 13"4.5 = 85.5W
=> RST to 200mV/1500mV
Charge Current Ichg = [0.075V/Rsense/CHG]/[VCTL/3.6V]
Rsense=42mΩ/0.000m
VCTL= 3V => Ichg = 2.5A
VCTL= 1.58V => Ichg = 1.4A
VCTL= 1.58V => Ichg = 1.4A
Mode pin : Vinode > 2.8V (90% to LDO pin) => 4 Cells
2.8 > Vinode > 1.8V (Booting) => 3 Cells
0.8 > Vinode (90% to GND) => Leading mode
VCTL= 0.8V or DCIN = 7V => Charger Disable
Precharge current=150mA

3/6 change for
3S2P/3S3P only 4/4
deleted

4/4 deleted

4/4 deleted by EE

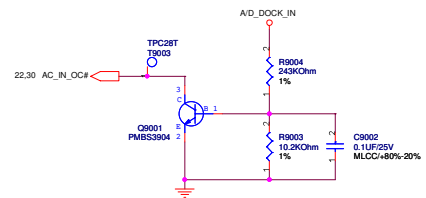
4/17 DELETE BAT_S
WITHOUT SHUTDOWN
FUNCTION

AC_BAT_SYS_INV to Inverter connect,
Power trace => 60m11(min),
Put JP8805 close to Q8800

ASUS		Title :POWER_CHARGER	
ASUSTeK COMPUTER INC. MS		Engineer: Gary Lin	
Size	Project Name	Rev	
C	M50S/X55S	1.0	
Date: March, September 10, 2007		Sheet	85 of 85

		Title : <i>N/A</i>	
ASUSTek COMPUTER INC. NB		Engineer: <i>Gary Lin</i>	
Size Custom	Project Name M50S/X55S		Rev 1.0
Date: <i>Monday, September 03, 2007</i>	Sheet	<i>89</i>	of <i>95</i>

ADAPTER IN DETECT

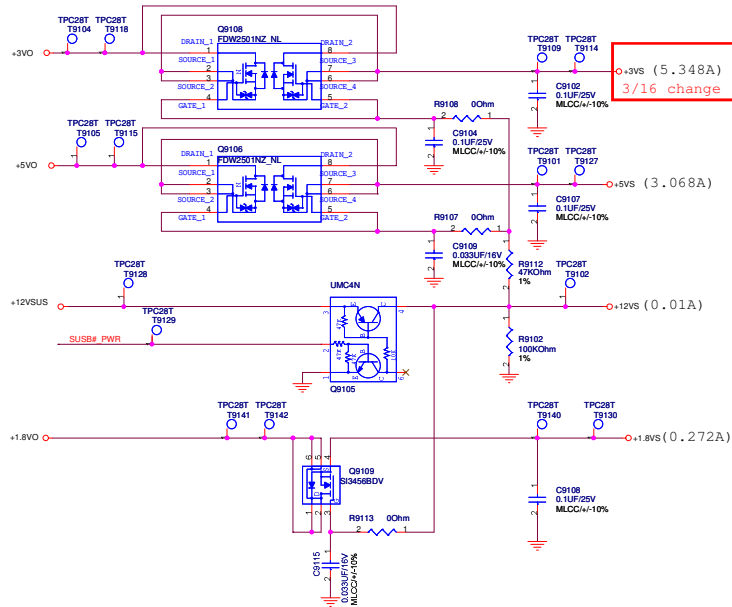


		Title : POWER_DETECT	
ASUSTeK COMPUTER INC. NB		Engineer: Gary Lin	
Size Custom	Project Name M50S/X55S		Rev 1.0
Date: Monday, September 03, 2007		Sheet 90 of 95	

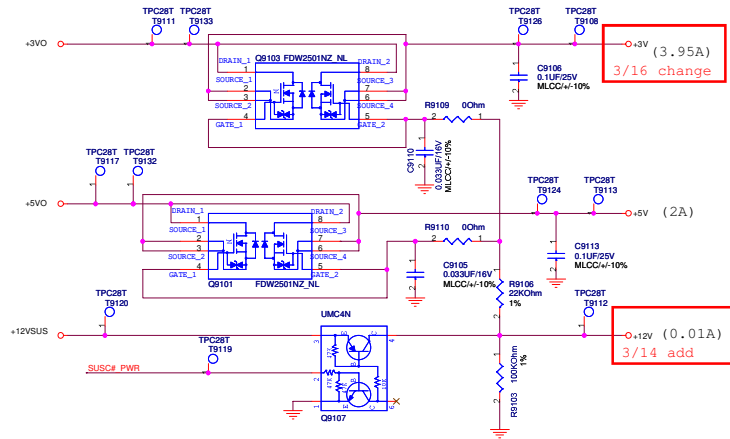
SUSB#_PWR POWER

3/16 delete +1.5VS from load switch

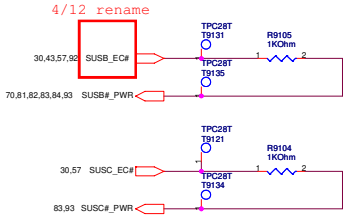
3/14 delete +VRAM



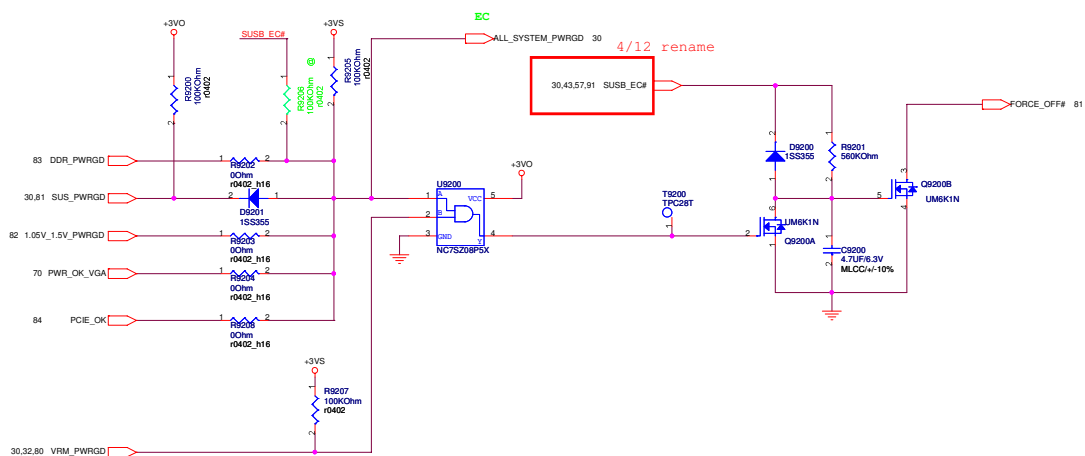
SUSC#_PWR POWER

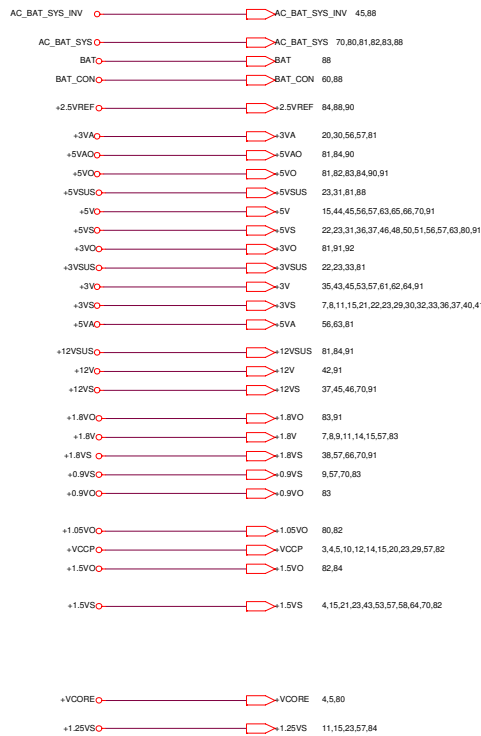


3/16 delete +1.5V

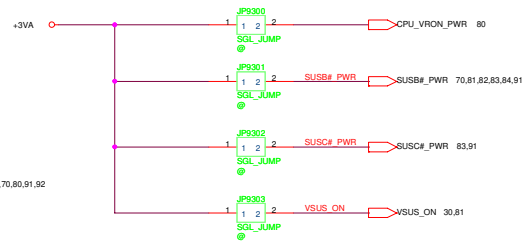


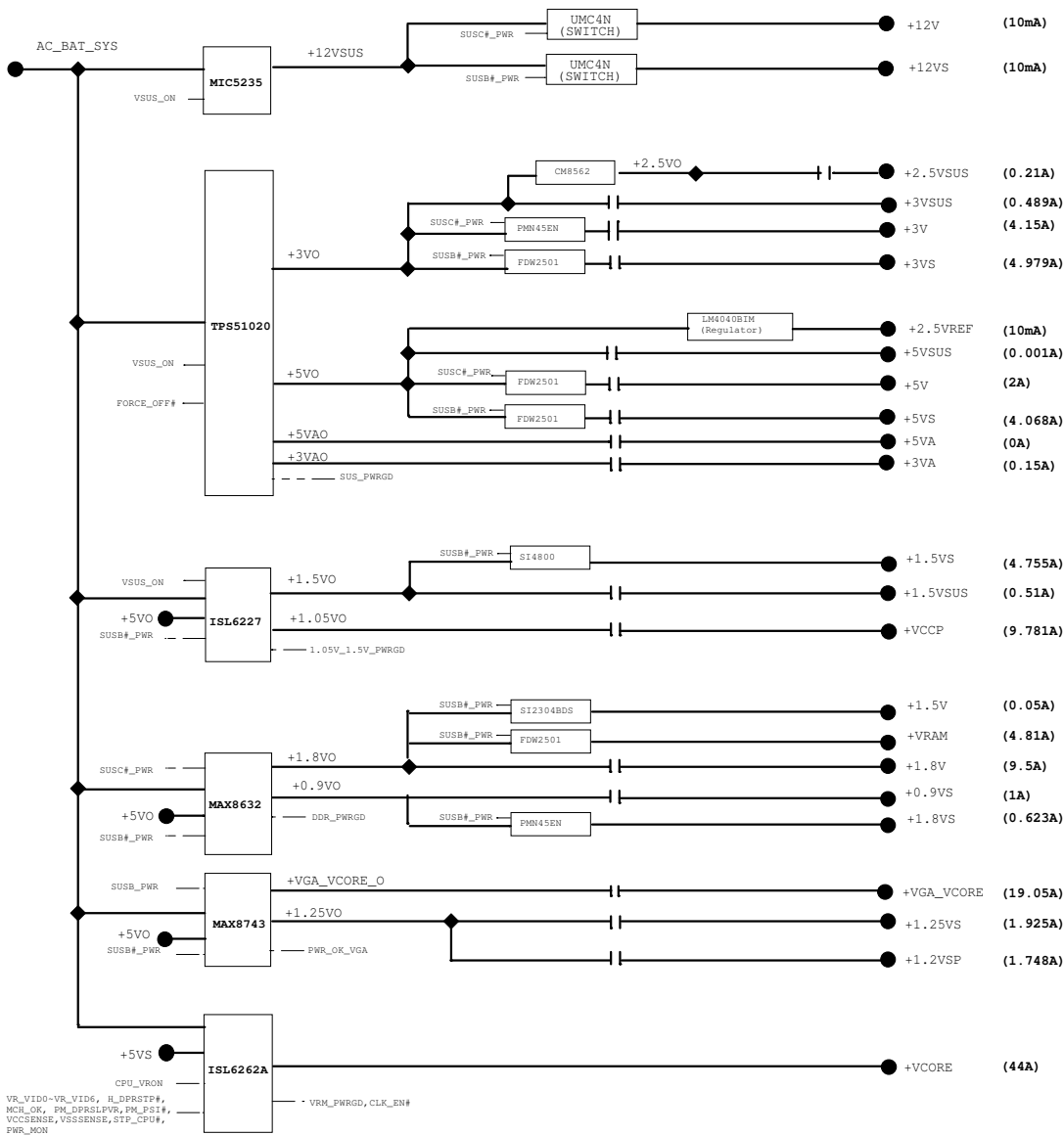
POWER GOOD DETECTOR

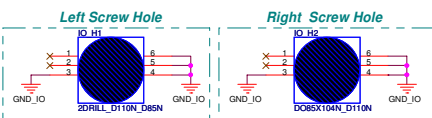
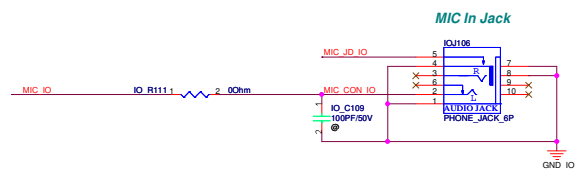
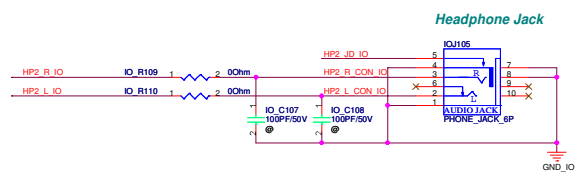
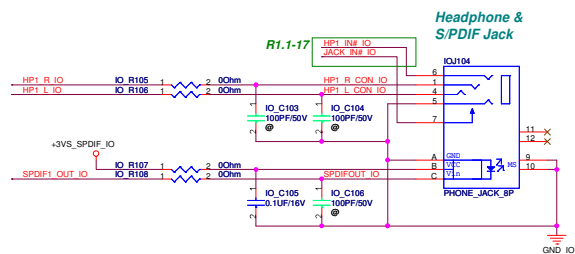
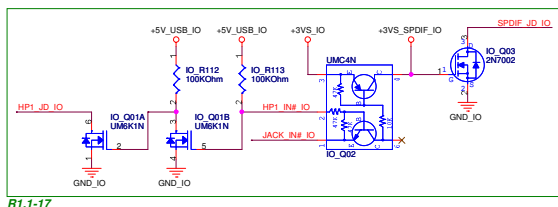
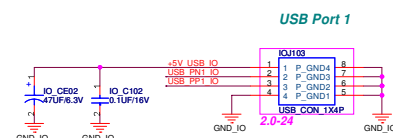
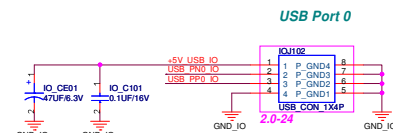
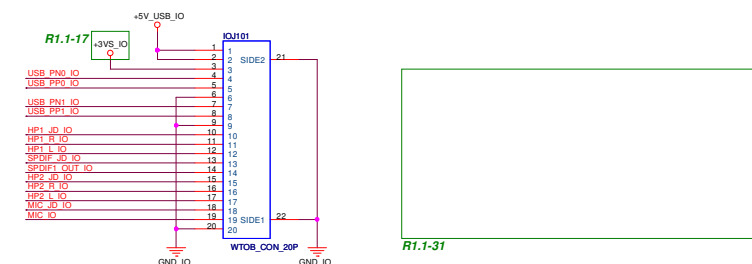




FOR POWER TEST







Rev	Date	Description
R1.0		First Release!
R1.1 Green Block		<p>** Merge IO board into main board PCB. Page 95.</p> <p>01.Remove VR_VID[6:0] testing series 0 0hm. Page 4.</p> <p>02.Change 6pcs +VCORE capacitors to No-Stuff for cost down. Page 5.</p> <p>03.Change 3pcs +0.9VS capacitors to No-Stuff for cost down. Page 9.</p> <p>04.Change N1Sv USB port to follow N2Sv, and modify USB_OC#. Page 21,43,45.</p> <p>05.PM Request: Change Bluetooth LED tp E-Mail LED. Page 22,56.</p> <p>06.Follow Intel to change C2304 to 1uF/16V(XR). Page 23.</p> <p>07.Follow R1E to change R2904 to 270ohm. Page 29.</p> <p>08.Follow IT8752/8512 EC Common Hardware Pin Assignment v0.005, change GPE7 to INSTANT_ON# and GPG0 to PM_THERM#. Page 30.</p> <p>09.PM REquest: Remove USB port charger function. Page 30,65.</p> <p>10.PM change WWAN LED to touch-pad lock LED. Page 30,56.</p> <p>11.Change IR to 36KHz to meet Vista remote control Min. range requirement. Page 31.</p> <p>12.Remove testing 2nd CIR design. Page 31.</p> <p>13.Change X3301 to 49S type for cost down. Page 33.</p> <p>14.LAN chip version change. Page 33.</p> <p>15.Audio codec chip change version. Page 36.</p> <p>16.N1Sv/X55 will not supprot 3G function. Page 36,67.</p> <p>17.Add S/PDIF & HDMI jack detect by Realtek sugesstion. Page 36,65,70,95.</p> <p>18.Modify audio de-pop circuit. Page 36,37.</p> <p>19.Modify LVDS power sequence failed bug. Page 45.</p> <p>20.Modify LCD abnormal display bug due to LVDS pair mismatch. Page 45,70.</p> <p>21.Remove HDIV support function. Page 47,70.</p> <p>22.Remove HDMI EMI filter design. Page 48.</p> <p>23.X55 need two pwer LEDs. Page 56.</p> <p>24.PM change WLAN LED to RF LED. Page 56,63.</p> <p>25.Bluetooth pin define error. Page 61.</p> <p>26.Remove co-layout sequence logic control circuit. Page 68.</p> <p>27.ME change parts: J3401,J5102,J6002,J6501. Page 34,51,60,65.</p> <p>28.EMI modification. Page 34,36,65.</p> <p>29.Crystal accuracy fine-tune. Page</p> <p>30.USB droop test fail. Page 65.</p> <p>31.Remove IO board USB common choke design. Page 95.</p> <p>32.Speaker fine-tune. Page 37.</p> <p>33.Cost down for 4-wire PWM fan. Page 50.</p> <p>34.Cost down: Change RB717F to BAT54AW. Page 37,45,48,56.</p>
R2.0 Pink Block		<p>01.Change +1.25VS_MPLL, +1.25VS_PEGPLL & +1.8V_SM_CK PLL design. Page 15.</p> <p>02.Add CMOS crack protection circuit. Page 22.</p> <p>03.Reserve C2337 (10UF/16V) for +5VREF_ICH. Page 23.</p> <p>04.Change ICS9LPR363 version from D to E for SATA clock jitter improve. Page 29.</p> <p>05.With EMI's confirmation, replace R2901, R2905, R2906 with short-pad JP2901, JP2902, JP2903. Page 29.</p> <p>06.With EC's confirmation, change ITE8752 P/N to 06G042016011. Page 30.</p> <p>07.With EMI's confirmation, replace R3001 with short-pad JP3002. Page 30.</p> <p>08.With EMI RD's confirmation, remove reserved LAN common choke circuit. Page 34.</p> <p>09.With EMI's confirmation, change R3612, R3614, R3615, R3616, R3622, R3624, R3626 to short-pad JP3601~JP3607. And change R3611, R3613, R3623, R3625 to No-Stuff. Page 36.</p> <p>10.Post wave sounds abnormal when audio amplifier use GMT G1431. Change C3706 to 0.33UF to shorten audio amplifier start-up time. Page 37.</p>

Rev	Date	Description
		<p>11.For cost down, change CE3701-CE3704 to 47UF. And after EA test, these can pass Vista audio criteria. Page 37.</p> <p>12.With EMI's confirmation, remove reserved 1394 common choke circuit. Page 41.</p> <p>13.With EMI's confirmation, remove reserved NewCard USB common choke circuit. Page 43.</p> <p>14.Add NewCard debug card co-layout circuit. Page 44.</p> <p>15.EMI modification: change reserved common choke circuit from USB port to internal camera port. Page 45.</p> <p>16.With EMI's confirmation, replace RX4603, RX4604 with JP4601, JP4602. Page 46.</p> <p>17.HDMI jack detection modification. Page 48,70.</p> <p>18.With EMI's confirmation, replace RX4809, RX4810 with JP4801, JP4802. Page 48.</p> <p>19.Change PWM FAN capacitors to 10UF. Page 50.</p> <p>20.Modify X55S power LED design. Page 56.</p> <p>21.Modify DC_IN bead for 120W design. Page 60.</p> <p>22.With EMI's confirmation, remove reserved e-SATA/USB combo port USB common choke circuit. Page 66.</p> <p>23.Reserve R8023 for shortage issue of ISL6262A. Page 80.</p> <p>24.QTR USB plug test failed, change USB connector. Page 95.</p>

**ASUSTeK COMPUTER INC. NE1**

Title : Revision History
Engineer: John Hung

Size	Project Name	Rev
Custom	M50S/X55S	1.0
Date: Wednesday, September 05, 2012	Sheet	98 of 98