

# PEGATRON CONFIDENTIAL

MODEL NAME :

PCB NO :

69- P/N :

## BA52\_CP Colay Schematic

Intel Arrandale rPGA-989

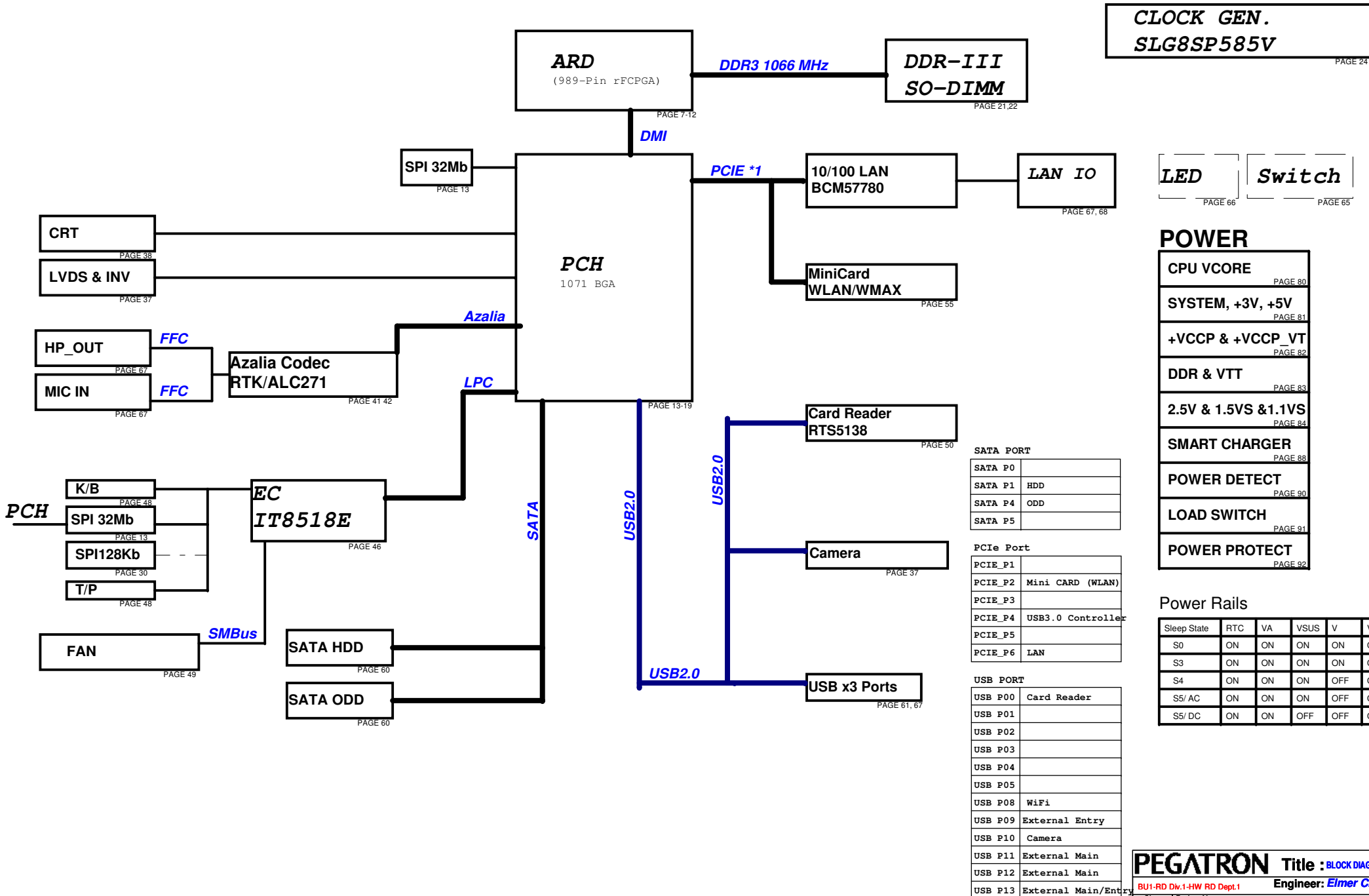
PCH BGA 1071

2011-0503

REV :R2.0

<b>PEGATRON</b> Title : <i>Cover Page</i>		
BU1-RD Div.1+HW RD Dept.1 Engineer: <i>Elmer Chiu</i>		
Size Custom	Project Name <b>BIC50</b>	Rev 2.0
Date: <i>Wednesday, May 18, 2011</i>		Sheet 1 of 77

# BA52\_CP BLOCK DIAGRAM



**CLOCK GEN.**  
**SLG8SP585V**  
PAGE 24

**LED** (PAGE 66) **Switch** (PAGE 65)

- POWER**
- CPU VCORE (PAGE 80)
  - SYSTEM, +3V, +5V (PAGE 81)
  - +VCCP & +VCCP\_VT (PAGE 82)
  - DDR & VTT (PAGE 83)
  - 2.5V & 1.5VS & 1.1VS (PAGE 84)
  - SMART CHARGER (PAGE 88)
  - POWER DETECT (PAGE 90)
  - LOAD SWITCH (PAGE 91)
  - POWER PROTECT (PAGE 92)

**SATA PORT**

SATA P0	
SATA P1	HDD
SATA P4	ODD
SATA P5	

**PCIE Port**

PCIE_P1	
PCIE_P2	Mini CARD (WLAN)
PCIE_P3	
PCIE_P4	USB3.0 Controller
PCIE_P5	
PCIE_P6	LAN

**USB PORT**

USB P00	Card Reader
USB P01	
USB P02	
USB P03	
USB P04	
USB P05	
USB P08	WiFi
USB P09	External Entry
USB P10	Camera
USB P11	External Main
USB P12	External Main
USB P13	External Main/Entry

**Power Rails**

Sleep State	RTC	VA	VSUS	V	VS
S0	ON	ON	ON	ON	ON
S3	ON	ON	ON	ON	OFF
S4	ON	ON	ON	OFF	OFF
S5/ AC	ON	ON	ON	OFF	OFF
S5/ DC	ON	ON	OFF	OFF	OFF

**PEGATRON** Title : **BLOCK DIAGRAM**  
 BU1-RD Div.1-HW RD Dept.1 Engineer: **Elmer Chiu**

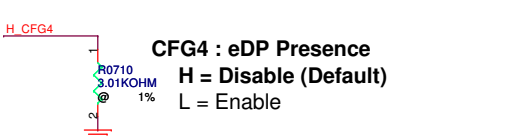
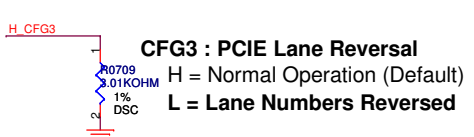
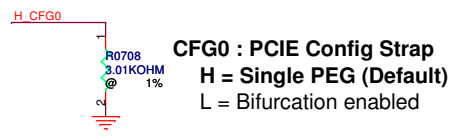
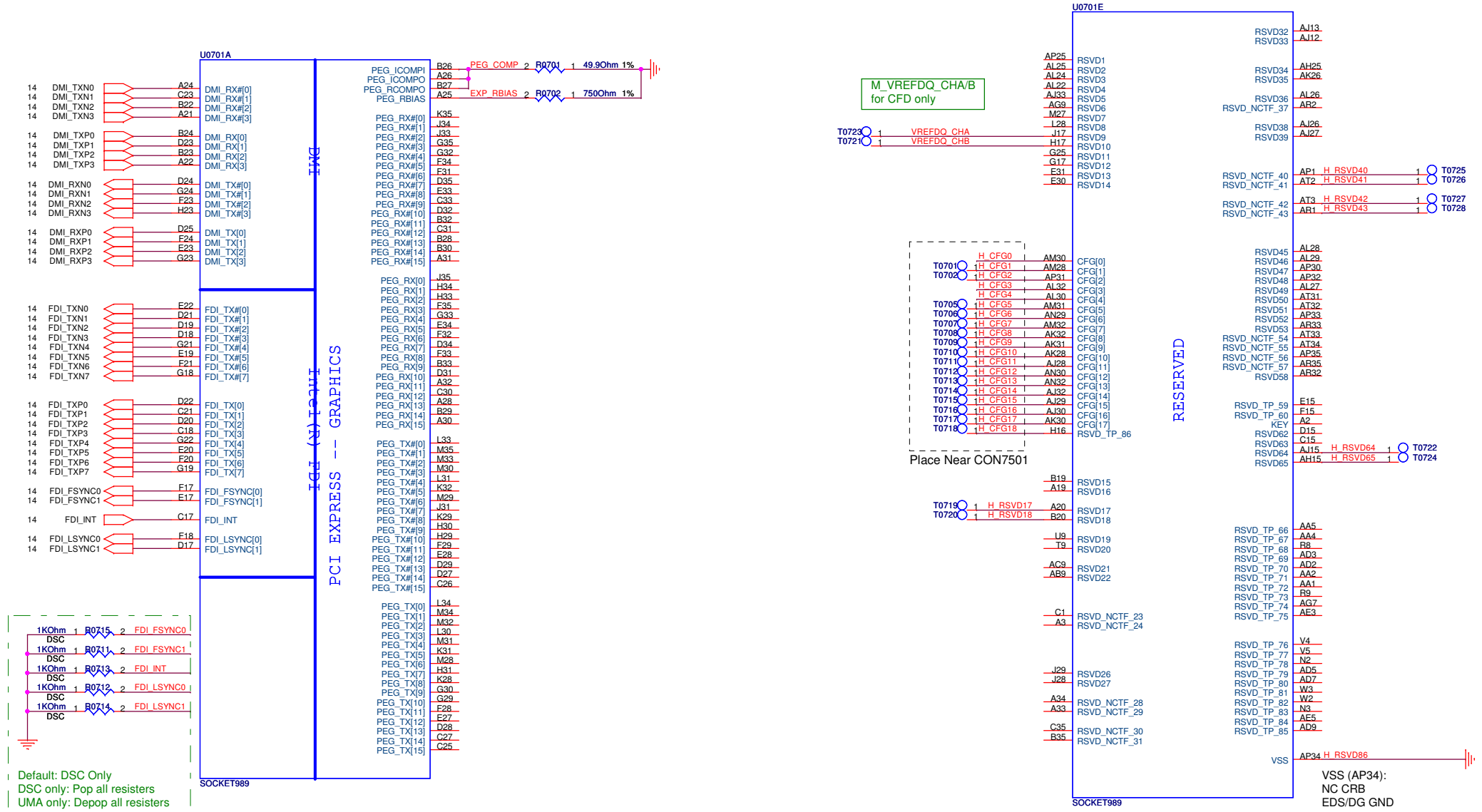
Size	Project Name	Rev
Custom	<b>BIC50</b>	2.0

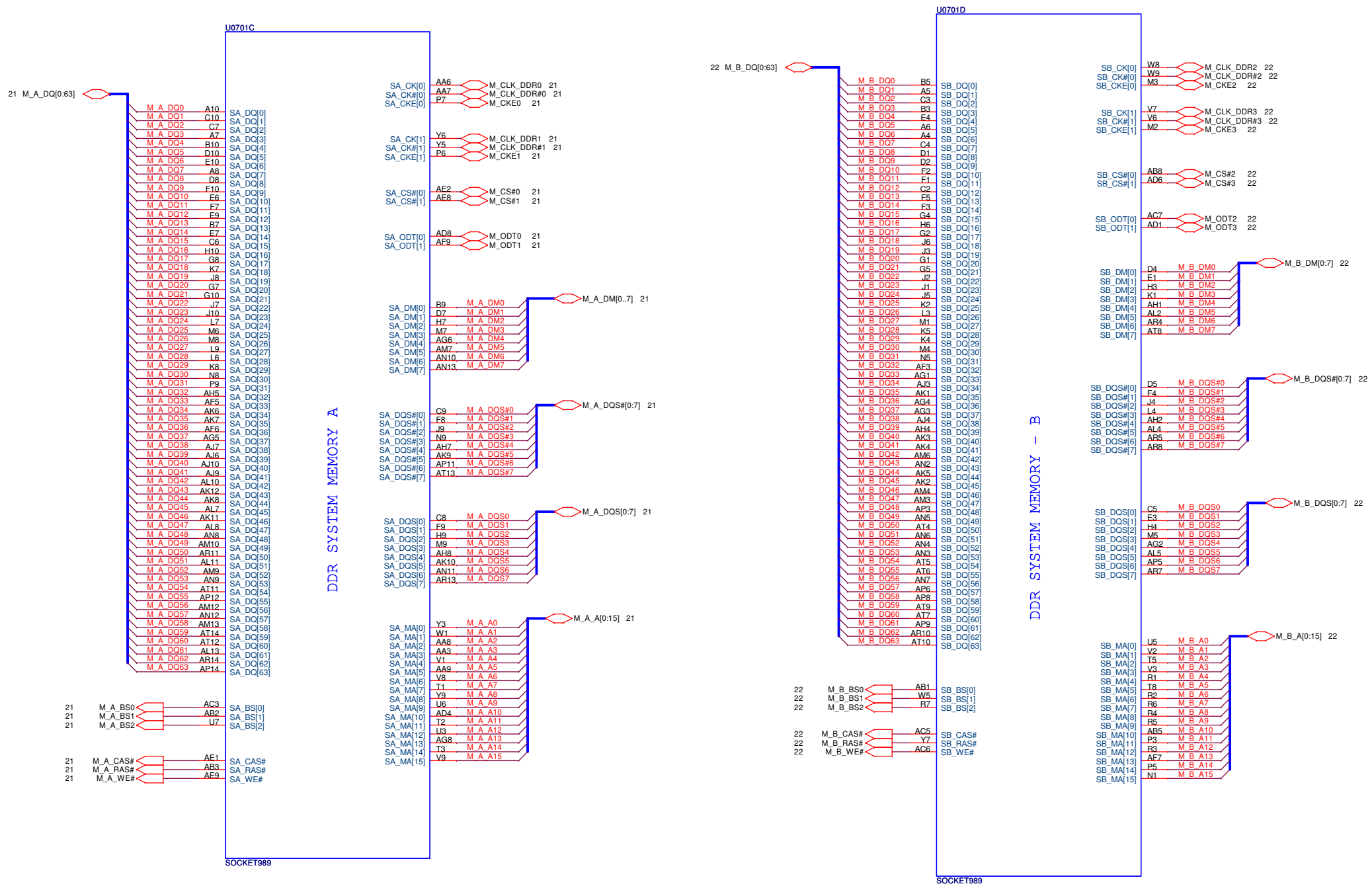
Date: **Tuesday, May 03, 2011** Sheet **2** of **77**

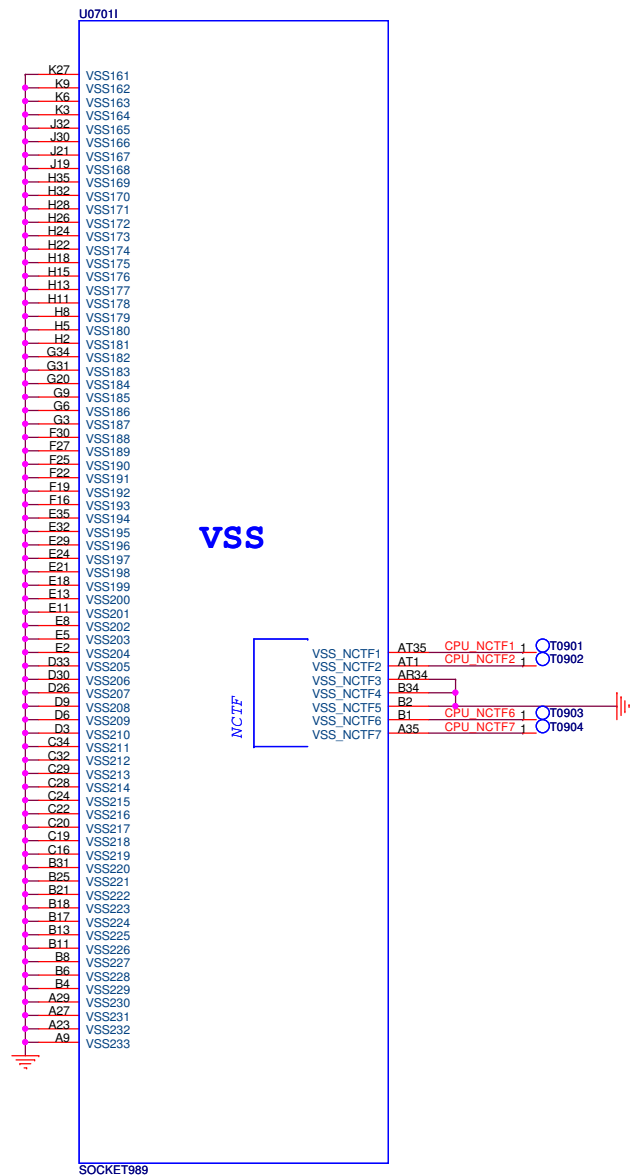
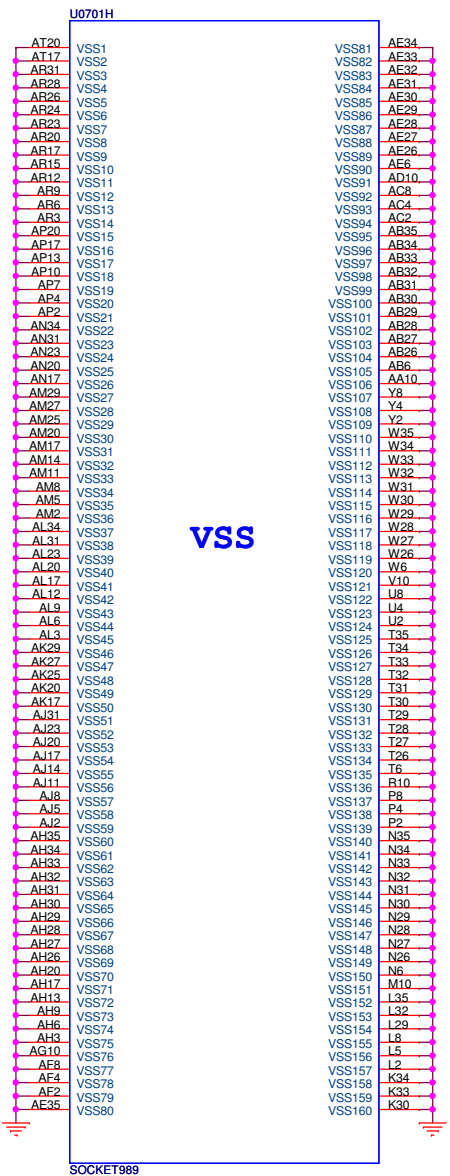
# SCHEMATIC INDEX V1.0

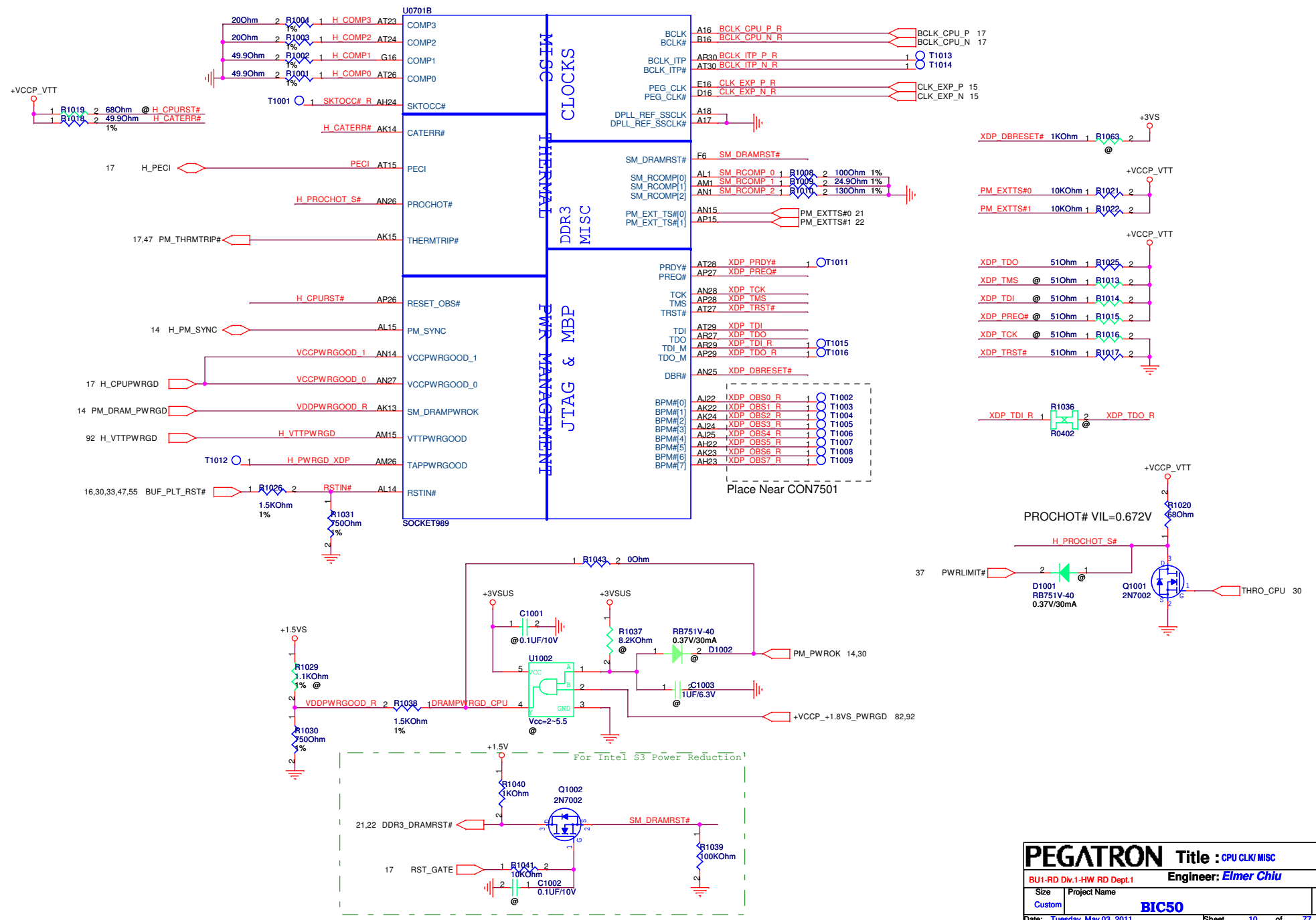
PAGE#	Description	NOTE
01	Cover Page	
02	Block Diagram	
03	PAGE INDEX	
04	Bus connection	
05	SMBus Diagram	
06	Power Rail	
07-10	CPU	
11-16	GMCH	
17-20	ICH	
21-23	DDR2/3 SO-DIMM	
24	Clock Generator	
25-33	Reserved	
34	Power Express/ SLI Logic	
35-36	Reserved VGA port	
37	LVDS CON	
38	RGB CON	
39	HDMI (Level shift for UMA)	
40	Dispaly port	
41-45	AUDIO CODEC & AMP & Jack	
46-48	EC ITE8512E / FLASH / KB / TP	
49	THERMAL / FAN	
50-52	CARD READER / 1394	
53	Smart Card	
54	PCI-Express Card	
55	MINI CARD -WUSB /UPCONVERT	
56	MINI CARD -WWAN	
57	MINI CARD -WiFi/WMAX	
58-59	Reserve	
60	SATA(HDD & CD_ROM)	
61-62	USB (Jacks & Camera & BT & FP con & eSATA)	
63-64	DC-IN / Discharge / NVM	Reserved
65-66	CIR, LID, MDC, SW, LED, Power BTN, Debug	Other int CONNs
67-68	LAN / RJ45 / RJ11	

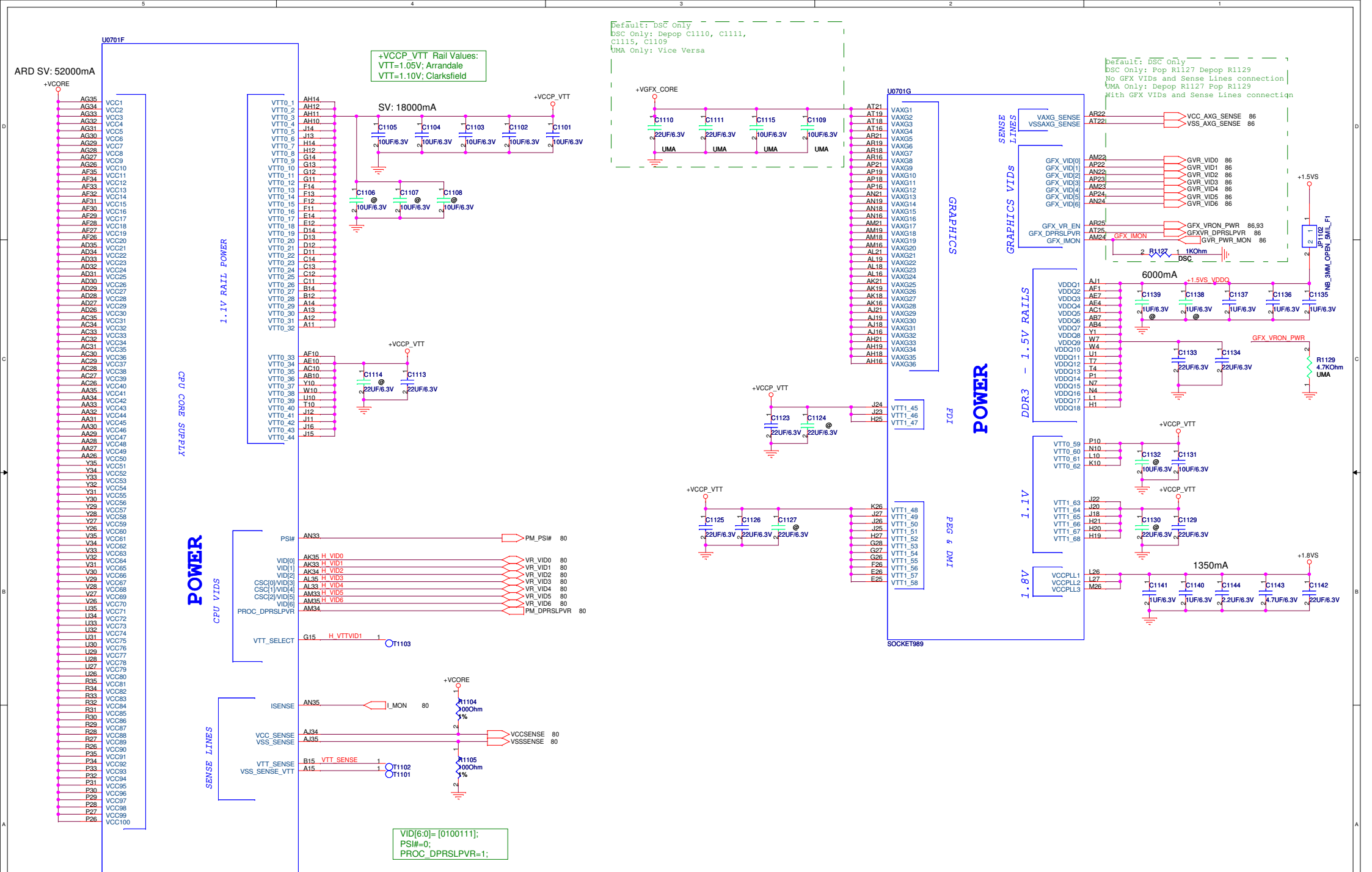
PAGE#	Description	NOTE
69	3D sensor	
70	CAP sense	
71	FM tunner	
72	SCREW PAD	
73	NAND FLASH/ HYPER FLASH	
74	Reserved	
75	XDP	
76	Port Docking	
77	DC-IN & BAT connector and discharge	
78	Power Sequence Logic	
79	POWER LOAD SWITCH	
80-100	POWER schematics	
101-	Daughter Board Combined Solutions	







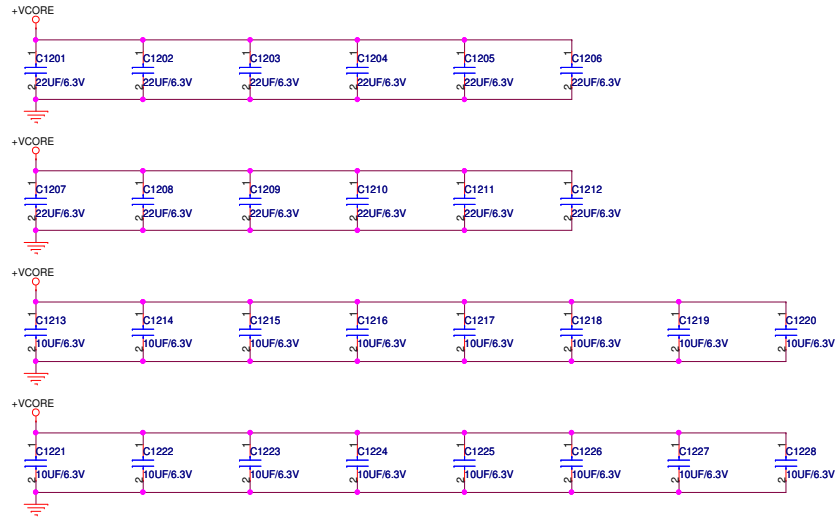


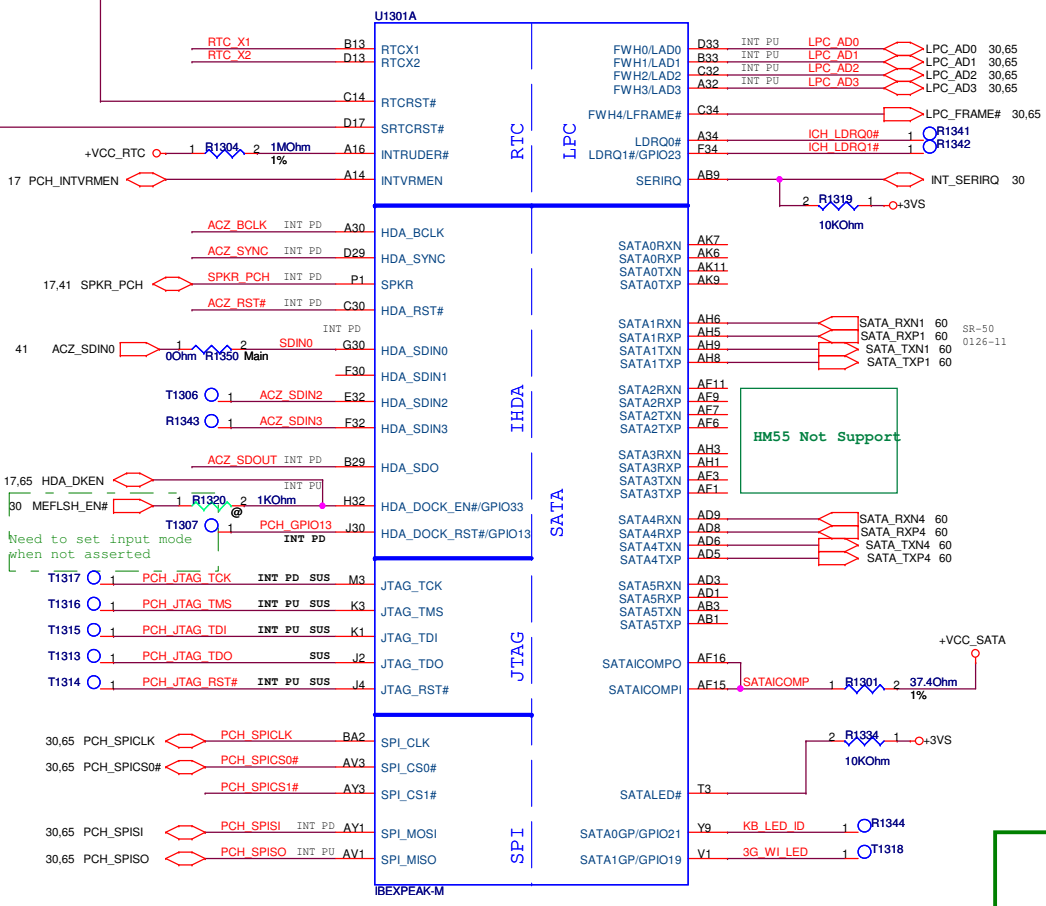
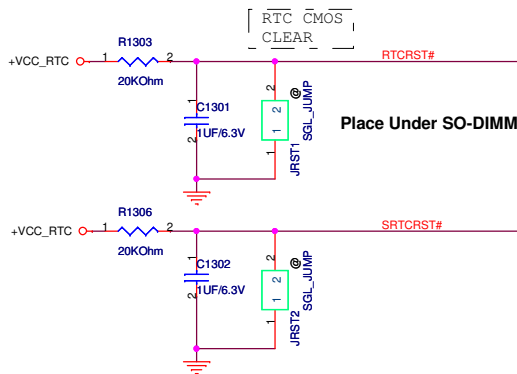




Decoupling guide from INTEL

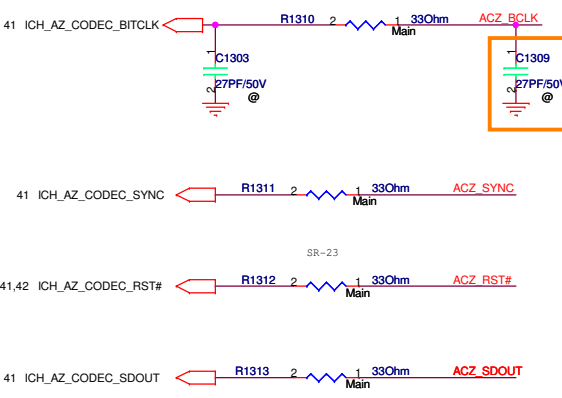
VCORE 10uF x 16pcs  
22uF x 12pcs





**SATA PORT**

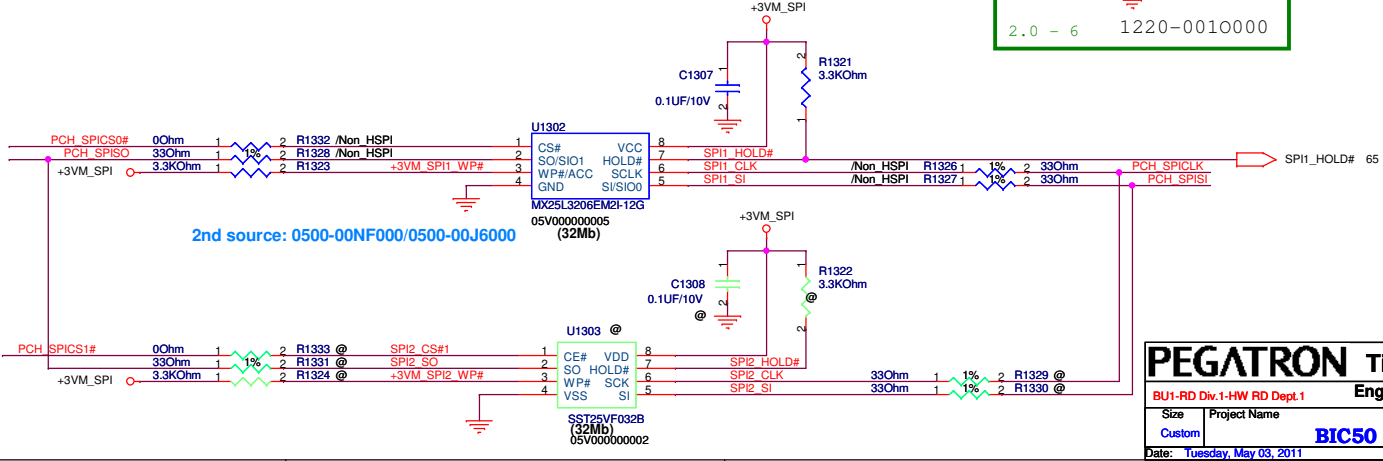
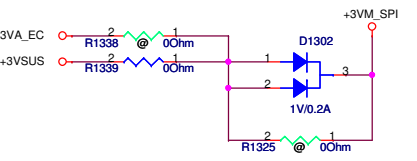
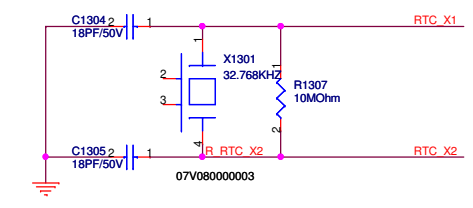
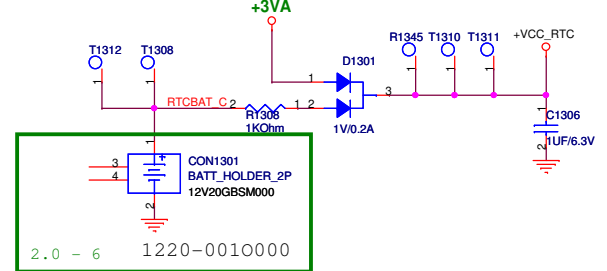
SATA P0	
SATA P1	HDD
SATA P4	ODD
SATA P5	eSATA Removed

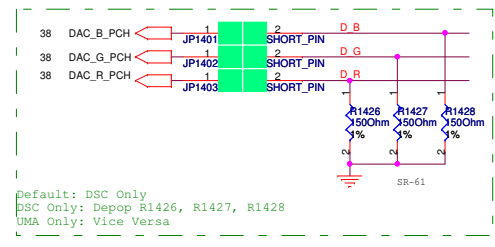
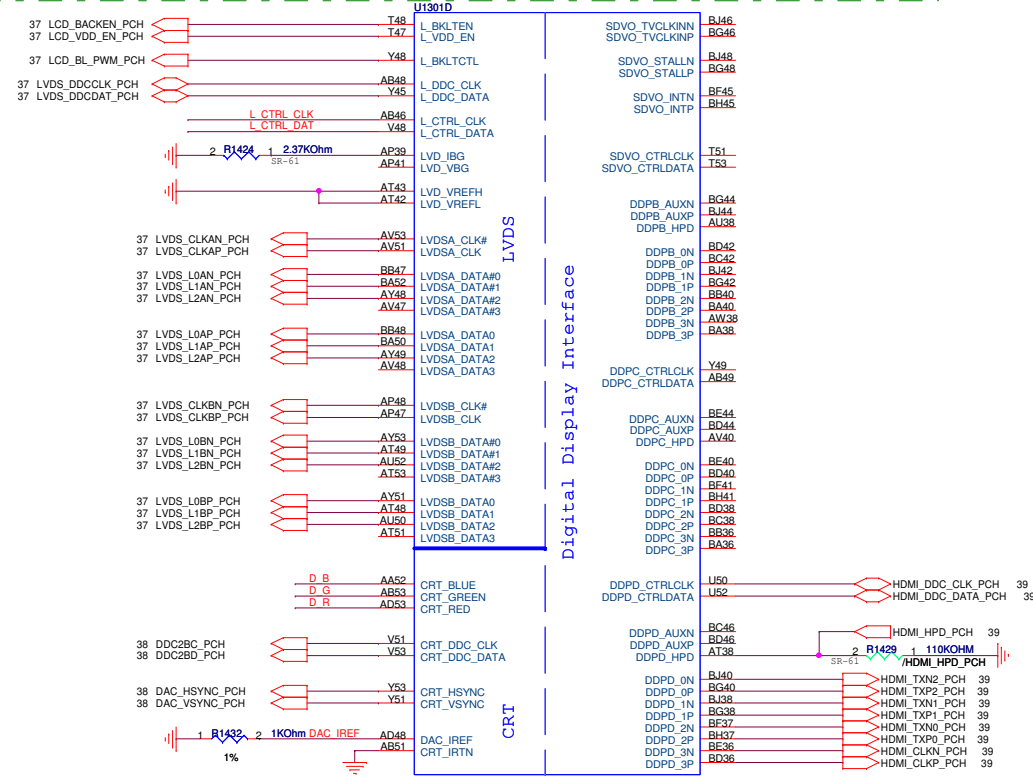
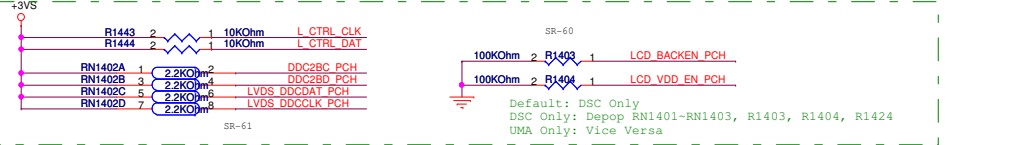
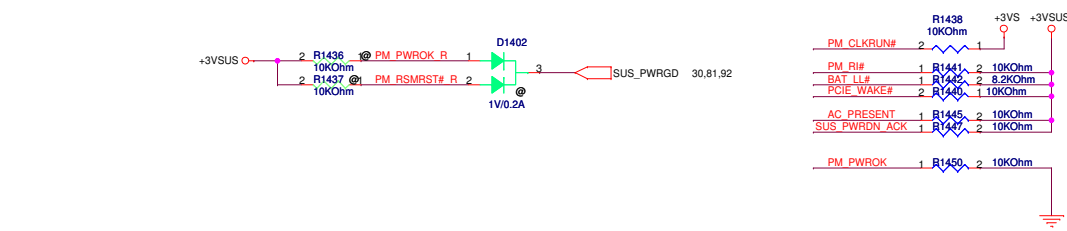
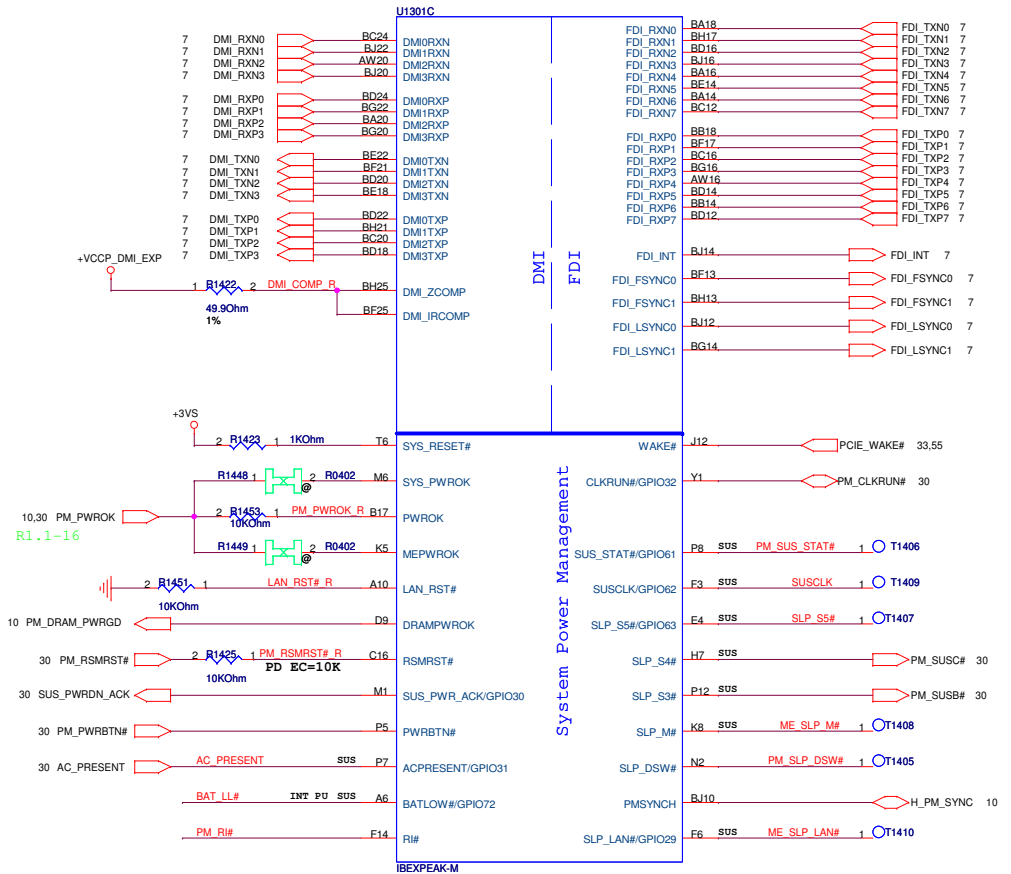


Need to set input mode when not asserted

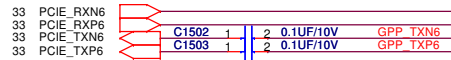
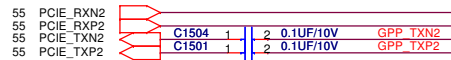
HM55 Not Support

**RTC BAT**

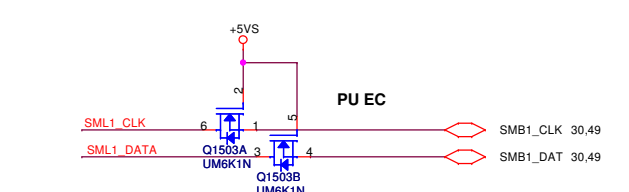
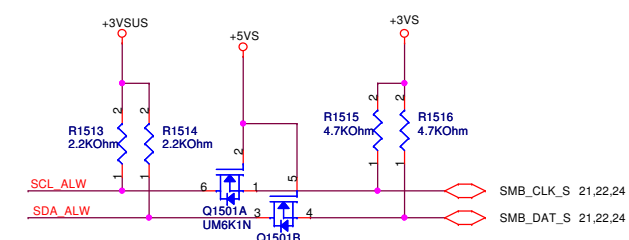
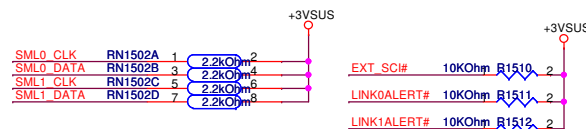
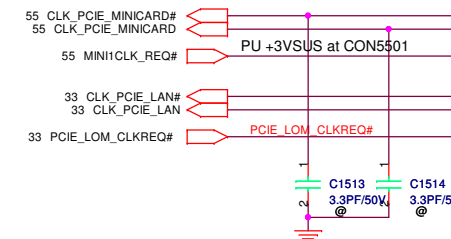
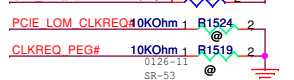
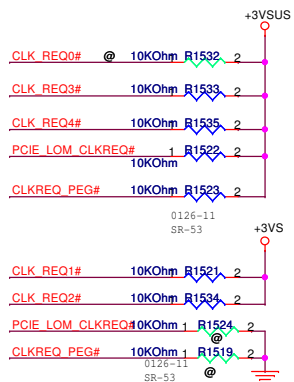




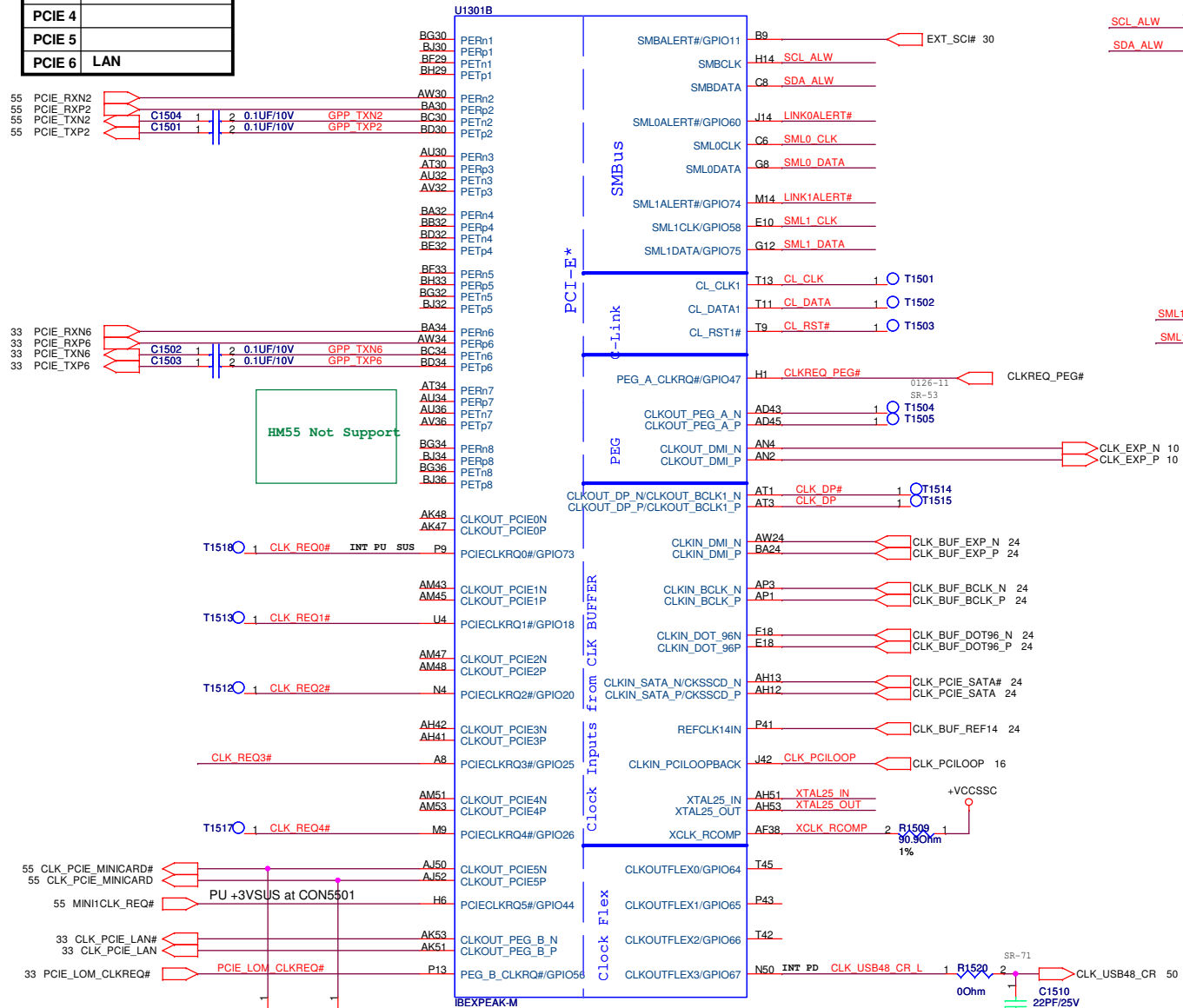
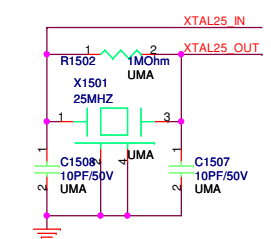
PCIE 1	
PCIE 2	Mini CARD (WLAN)
PCIE 3	
PCIE 4	
PCIE 5	
PCIE 6	LAN

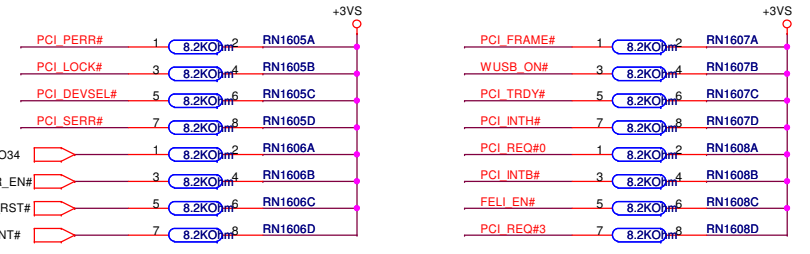
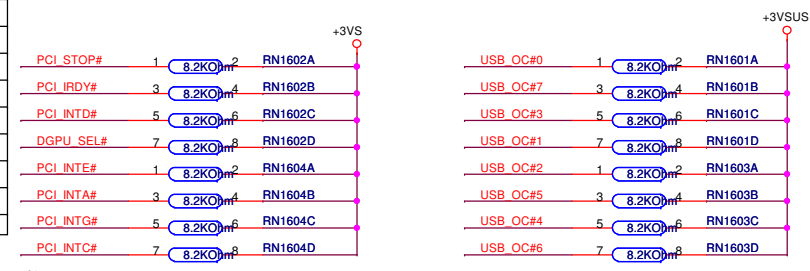
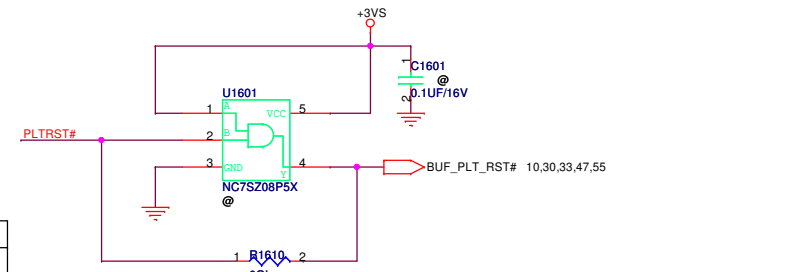
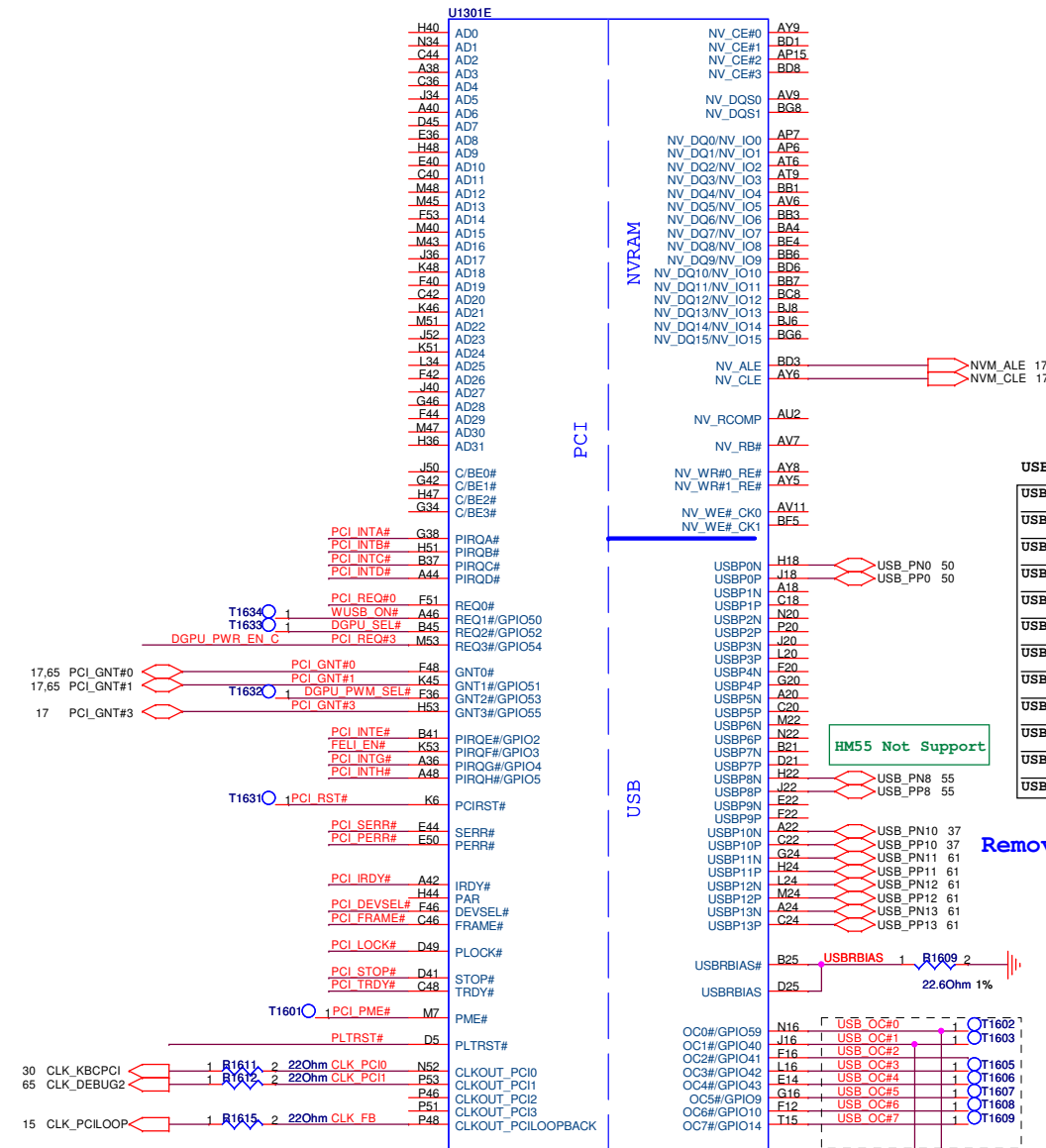


HM55 Not Support



Damping CPU Side





Remove USB\_9 (HDMI) SR-21 0124-11

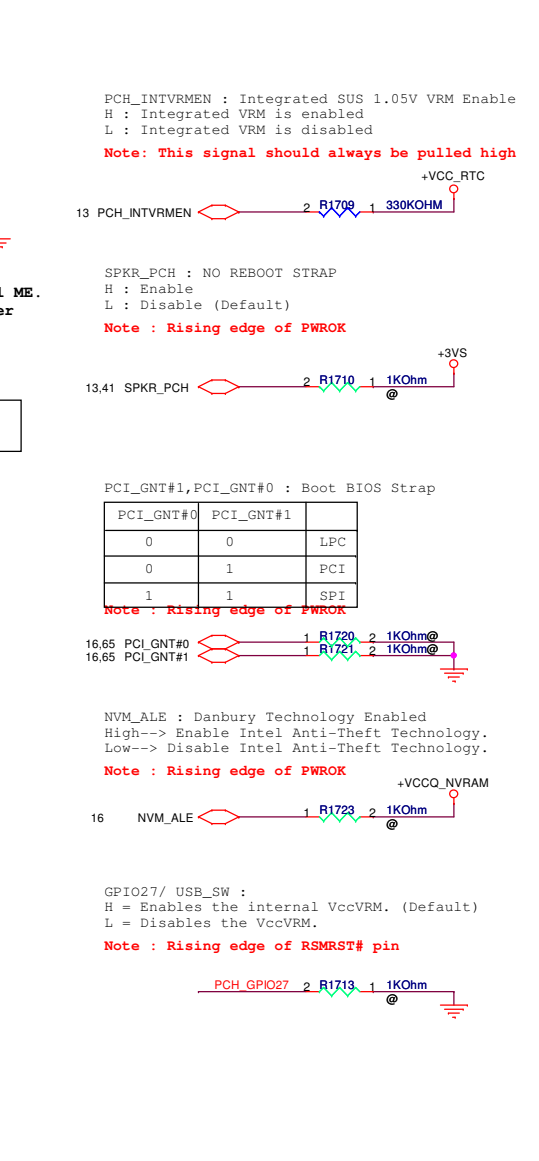
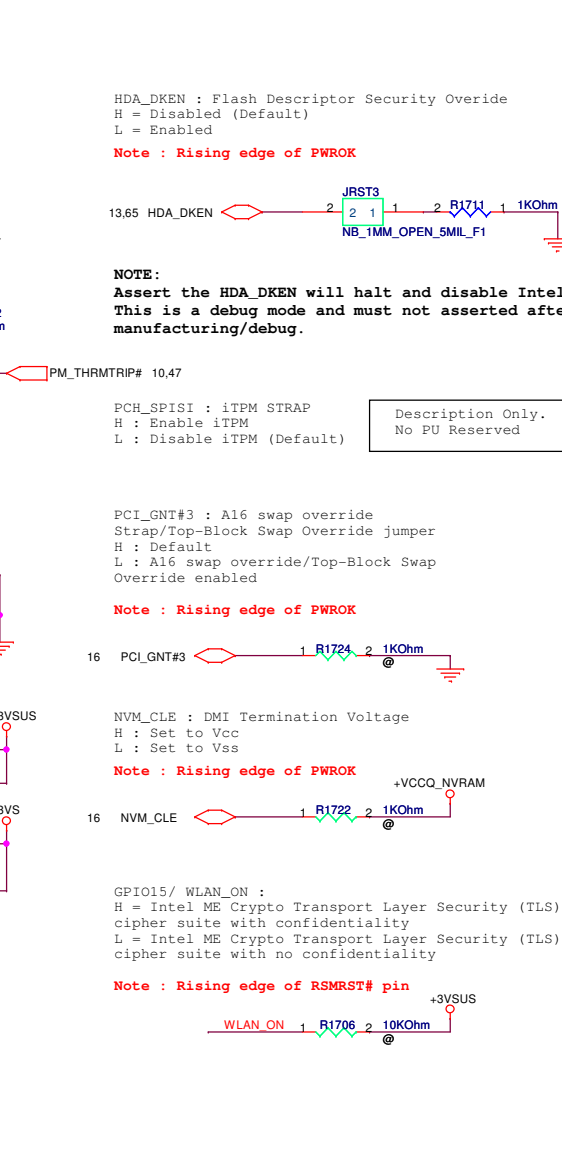
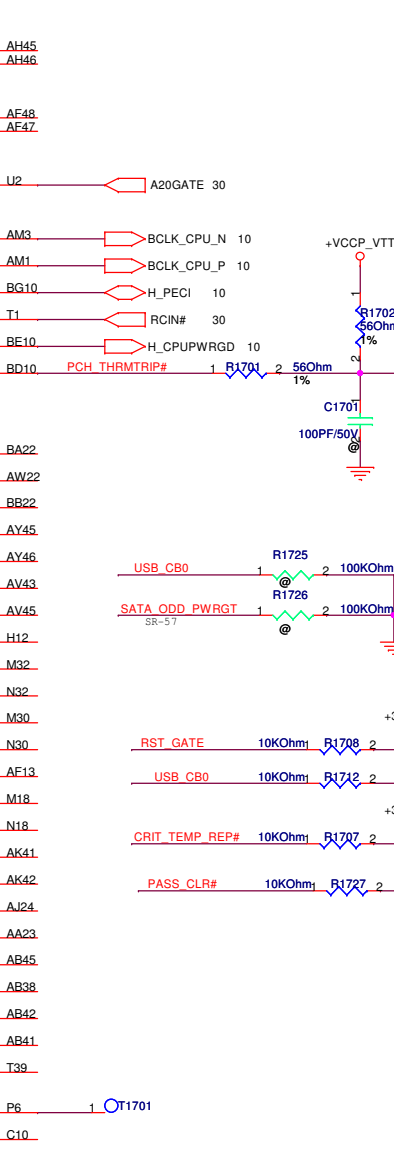
change USB power switch circuit SR-26 0124-11

**PEGATRON** Title : PCH CLK/ USB/ PCIE/ NVM

BU-1-RD Div.1-HW RD Dept.1 Engineer: Elmer Chiu

Size	Project Name	Rev
Custom	BIC50	2.0

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HDA\_DKEN : Flash Descriptor Security Override  
 H = Disabled (Default)  
 L = Enabled  
**Note : Rising edge of PWROK**

PCH\_INTVRMEN : Integrated SUS 1.05V VRM Enable  
 H : Integrated VRM is enabled  
 L : Integrated VRM is disabled  
**Note : This signal should always be pulled high**

**NOTE:**  
 Assert the HDA\_DKEN will halt and disable Intel ME.  
 This is a debug mode and must not asserted after manufacturing/debug.

PCH\_SPI1 : iTPM STRAP  
 H : Enable iTPM  
 L : Disable iTPM (Default)

Description Only.  
 No PU Reserved

PCI\_GNT#3 : A16 swap override  
 Strap/Top-Block Swap Override jumper  
 H : Default  
 L : A16 swap override/Top-Block Swap Override enabled

**Note : Rising edge of PWROK**

NVM\_CLE : DMI Termination Voltage  
 H : Set to Vcc  
 L : Set to Vss

**Note : Rising edge of PWROK**

GPIO15/ WLAN\_ON :  
 H = Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality  
 L = Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality

**Note : Rising edge of RSMRST# pin**

PCI\_GNT#1, PCI\_GNT#0 : Boot BIOS Strap

PCI_GNT#0	PCI_GNT#1	
0	0	LPC
0	1	PCI
1	1	SPI

**Note : Rising edge of PWROK**

NVM\_ALE : Danbury Technology Enabled  
 High--> Enable Intel Anti-Theft Technology.  
 Low--> Disable Intel Anti-Theft Technology.

**Note : Rising edge of PWROK**

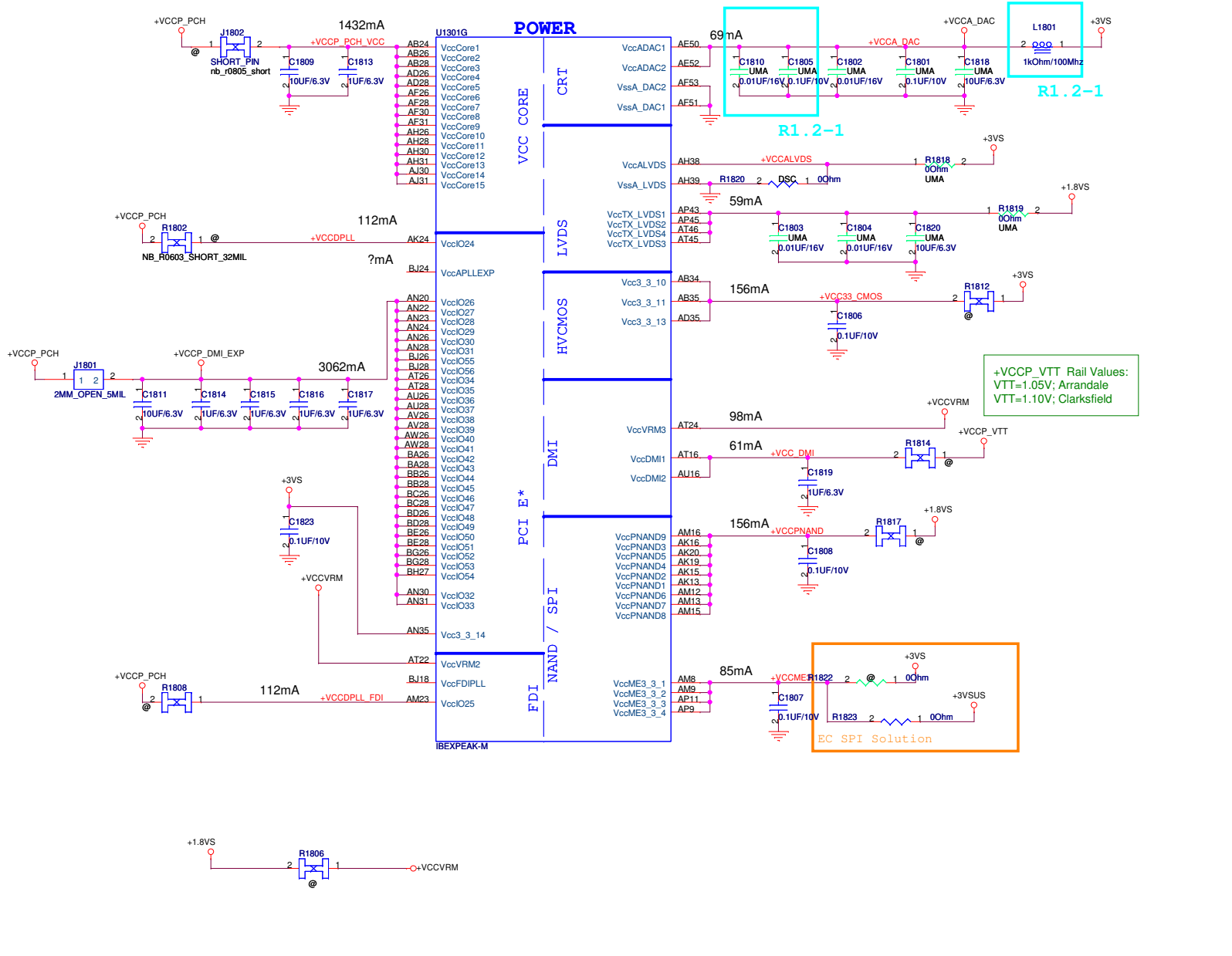
GPIO27/ USB\_SW :  
 H = Enables the internal VccVRM. (Default)  
 L = Disables the VccVRM.

**Note : Rising edge of RSMRST# pin**

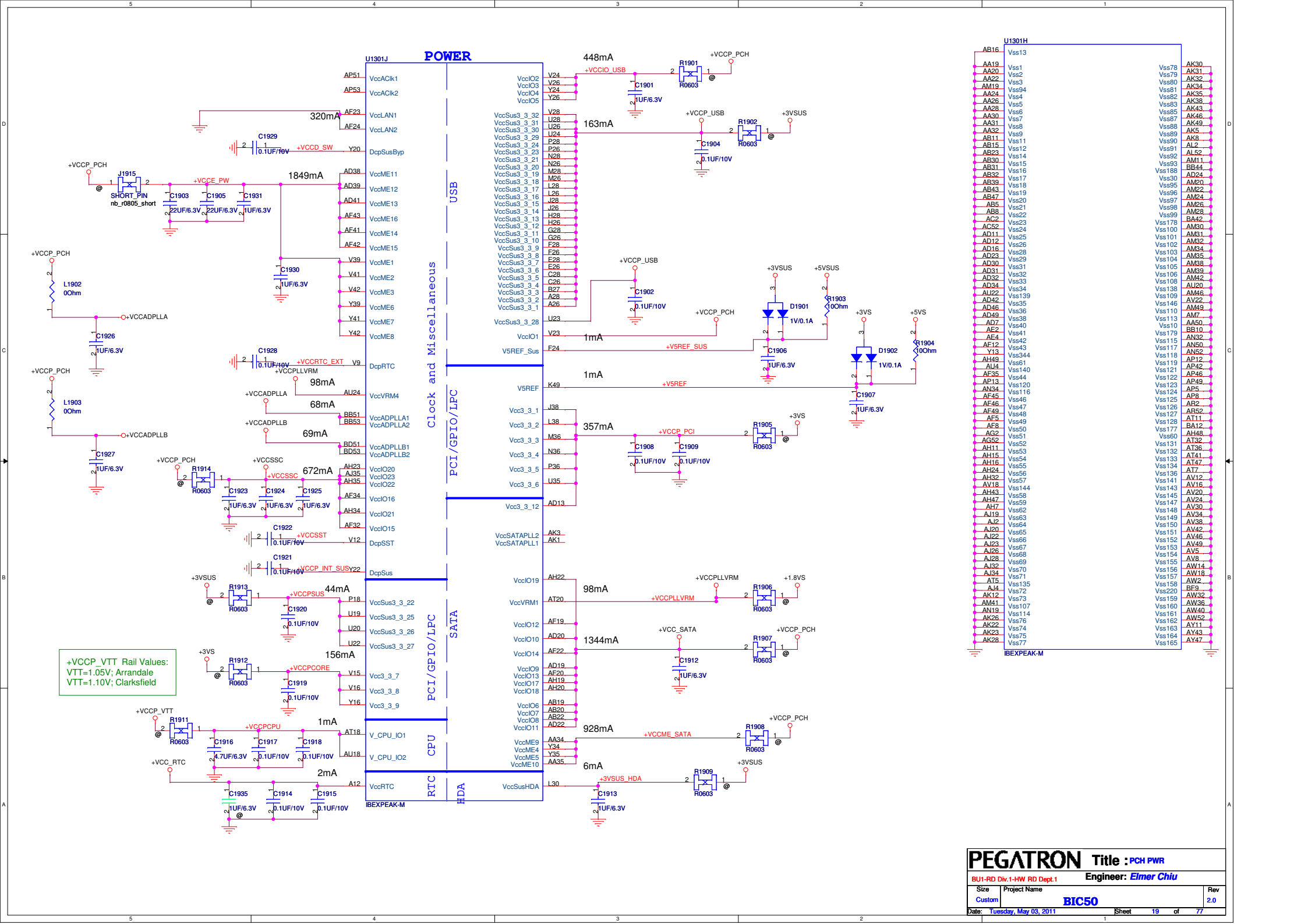
PCB_VID	0	1	2
E 1.0	0	0	0
E 1.1	0	0	1
E 2.0	0	1	0
M 1.0	1	0	0
M 1.1	1	0	1
M 2.0	1	1	0

- A4 Vss\_NCTF1
- A49 Vss\_NCTF2
- A5 Vss\_NCTF3
- A50 Vss\_NCTF4
- A52 Vss\_NCTF5
- A53 Vss\_NCTF6
- B2 Vss\_NCTF7
- B4 Vss\_NCTF8
- B53 Vss\_NCTF9
- BE1 Vss\_NCTF10
- BE53 Vss\_NCTF11
- BF1 Vss\_NCTF12
- BF53 Vss\_NCTF13
- BH1 Vss\_NCTF14
- BH2 Vss\_NCTF15
- BH52 Vss\_NCTF16
- BH53 Vss\_NCTF17
- BJ1 Vss\_NCTF18
- BJ2 Vss\_NCTF19
- BJ4 Vss\_NCTF20
- BJ49 Vss\_NCTF21
- BJ5 Vss\_NCTF22
- BJ50 Vss\_NCTF23
- BJ52 Vss\_NCTF24
- BJ53 Vss\_NCTF25
- D1 Vss\_NCTF26
- D2 Vss\_NCTF27
- D53 Vss\_NCTF28
- E1 Vss\_NCTF29
- E53 Vss\_NCTF30
- E53 Vss\_NCTF31

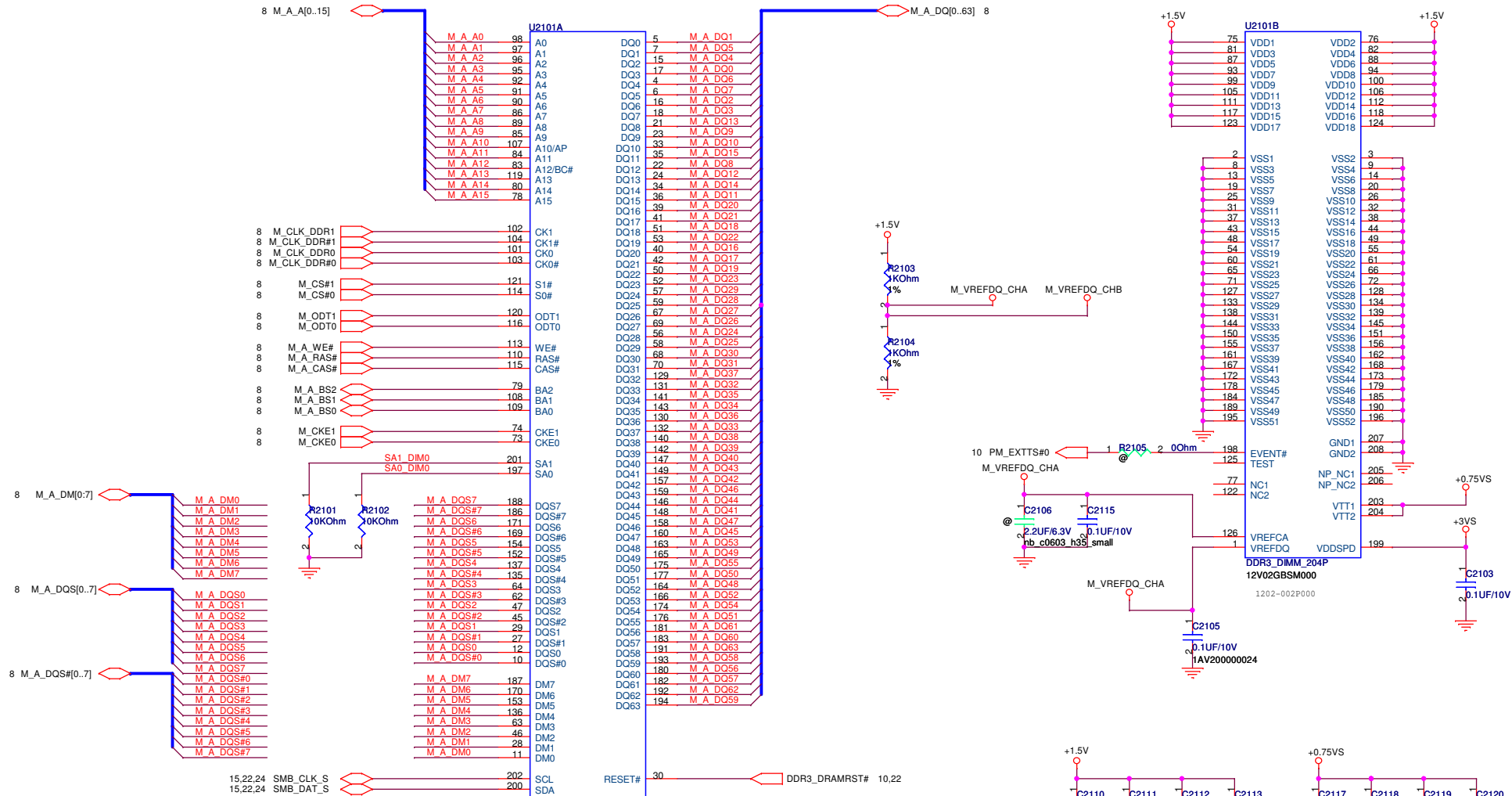
Default: DSC Only  
 DSC Only: Depop R1818, R1819, C1802, C1801, C1818  
 C1803, C1804, C1820  
 Pop R1820, and C1803 change to 0ohm  
 UMA Only: Vice Versa



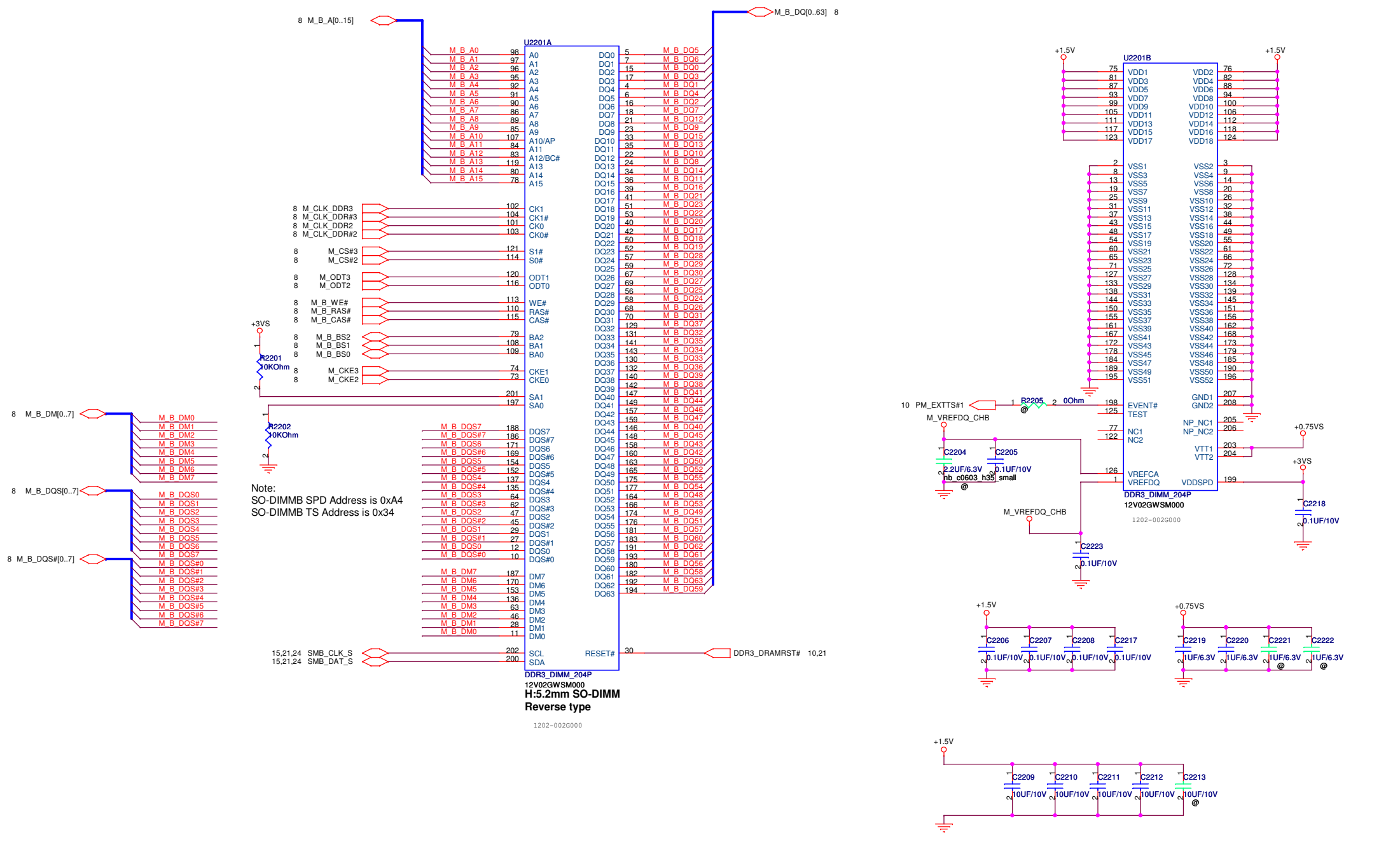
U1301I		H49	
AY7	Vss166	H49	H5
B11	Vss167	H5	J24
B15	Vss168	J24	K1
B19	Vss169	K1	K43
B23	Vss170	K43	K47
B31	Vss171	K47	K7
B35	Vss172	K7	L14
B39	Vss173	L14	L2
B43	Vss174	L2	L22
B47	Vss175	L22	L32
B7	Vss176	L32	L36
BG12	Vss177	L36	L40
BB12	Vss180	L40	L52
BB16	Vss181	L52	M12
BB20	Vss182	M12	M16
BB24	Vss183	M16	M20
BB30	Vss184	M20	M34
BB34	Vss185	M34	M42
BB38	Vss186	M42	M46
BB42	Vss187	M46	M52
BB49	Vss189	M52	M62
BB5	Vss190	M62	M72
BC10	Vss191	M72	M8
BC14	Vss192	M8	M24
BC18	Vss193	M24	M30
BC22	Vss194	M30	M36
BC26	Vss195	M36	M42
BC32	Vss196	M42	M48
BC36	Vss197	M48	M54
BC40	Vss198	M54	M60
BC44	Vss199	M60	M66
BC52	Vss200	M66	M72
BH9	Vss202	M72	M78
BD48	Vss203	M78	M84
BD5	Vss204	M84	M90
BE12	Vss205	M90	M96
BE16	Vss206	M96	P1
BE20	Vss207	P1	P22
BE24	Vss208	P22	P30
BE30	Vss209	P30	P32
BE34	Vss210	P32	P34
BE38	Vss211	P34	P42
BE42	Vss212	P42	P45
BE46	Vss213	P45	P47
BE50	Vss214	P47	P52
BE6	Vss215	P52	P62
BE8	Vss216	P62	P72
BE10	Vss217	P72	P82
BE12	Vss218	P82	P92
BE14	Vss219	P92	P102
BE16	Vss220	P102	P112
BE18	Vss221	P112	P122
BE20	Vss222	P122	P132
BE22	Vss223	P132	P142
BE24	Vss224	P142	P152
BE26	Vss225	P152	P162
BE28	Vss226	P162	P172
BE30	Vss227	P172	P182
BE32	Vss228	P182	P192
BE34	Vss229	P192	P202
BE36	Vss230	P202	P212
BE38	Vss231	P212	P222
BE40	Vss232	P222	P232
BE42	Vss233	P232	P242
BE44	Vss234	P242	P252
BE46	Vss235	P252	P262
BE48	Vss236	P262	P272
BE50	Vss237	P272	P282
BE52	Vss238	P282	P292
BE54	Vss239	P292	P302
BE56	Vss240	P302	P312
BE58	Vss241	P312	P322
BE60	Vss242	P322	P332
BE62	Vss243	P332	P342
BE64	Vss244	P342	P352
BE66	Vss245	P352	P362
BE68	Vss246	P362	P372
BE70	Vss247	P372	P382
BE72	Vss248	P382	P392
BE74	Vss249	P392	P402
BE76	Vss250	P402	P412
BE78	Vss251	P412	P422
BE80	Vss252	P422	P432
BE82	Vss253	P432	P442
BE84	Vss254	P442	P452
BE86	Vss255	P452	P462
BE88	Vss256	P462	P472
BE90	Vss257	P472	P482
BE92	Vss258	P482	P492
BE94	Vss259	P492	P502
BE96	Vss260	P502	P512
BE98	Vss261	P512	P522
BE100	Vss262	P522	P532
BE102	Vss263	P532	P542
BE104	Vss264	P542	P552
BE106	Vss265	P552	P562
BE108	Vss266	P562	P572
BE110	Vss267	P572	P582
BE112	Vss268	P582	P592
BE114	Vss269	P592	P602

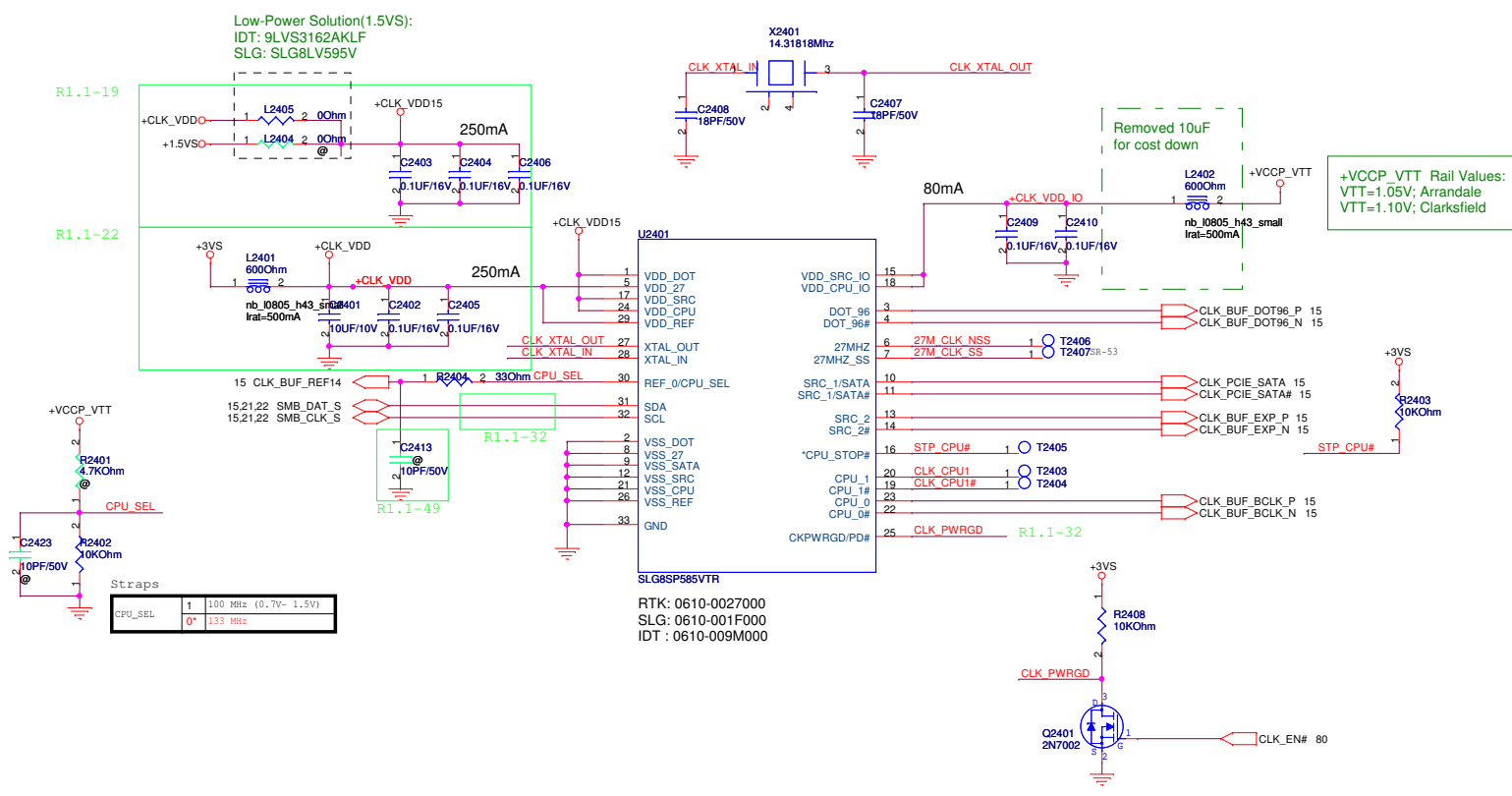


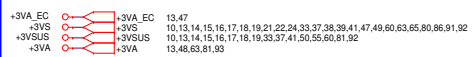
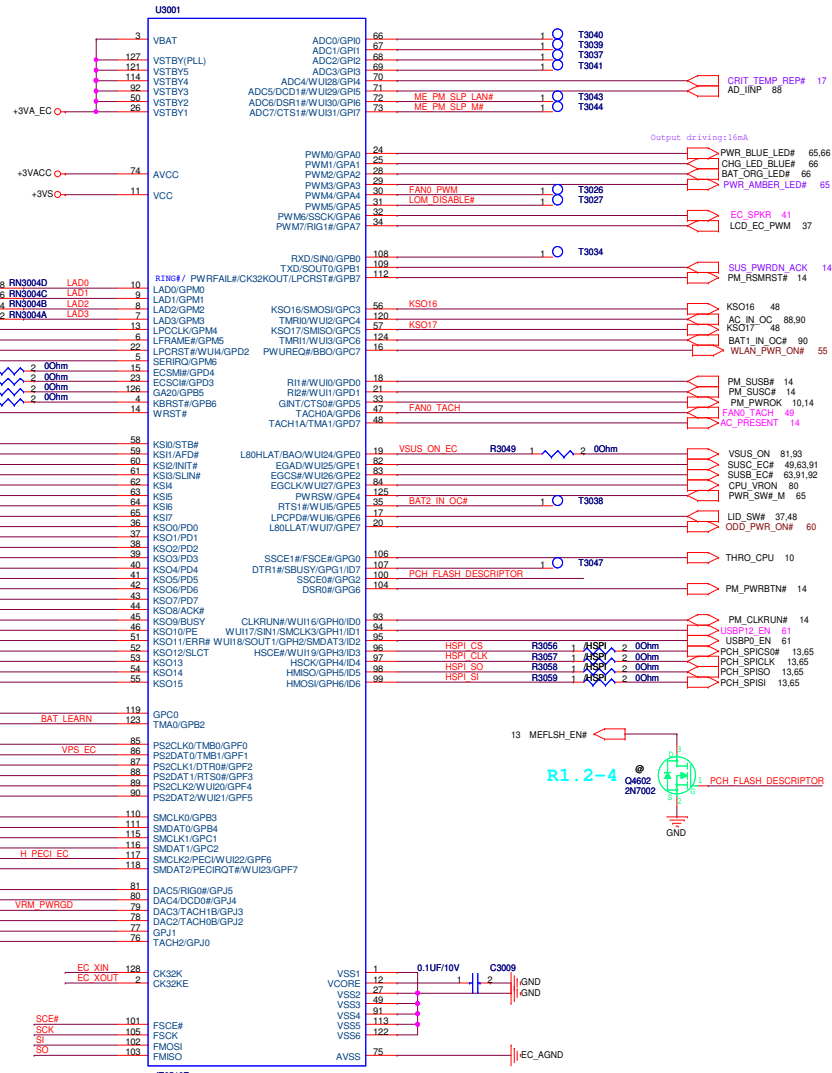




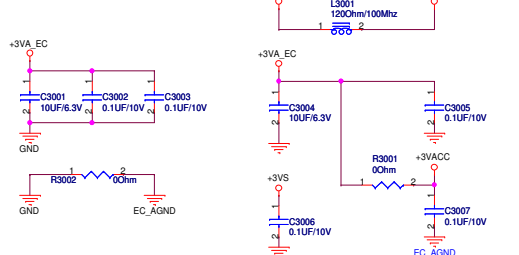
Note:  
 If SA0\_DIM0 = 0, SA1\_DIM0 = 0  
 SO-DIMMA SPD Address is 0xA0  
 SO-DIMMA TS Address is 0x30  
 If SA0\_DIM0 = 1, SA1\_DIM0 = 0  
 SO-DIMMA SPD Address is 0xA2  
 SO-DIMMA TS Address is 0x32



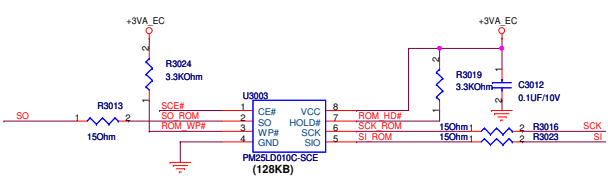
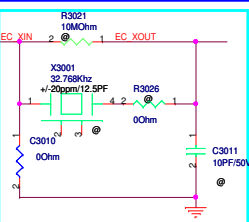
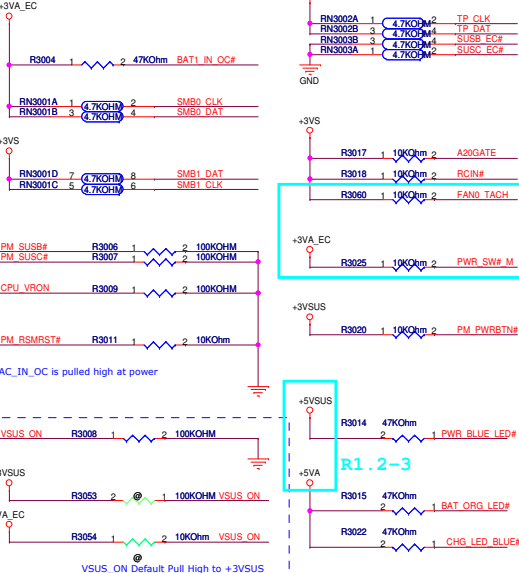


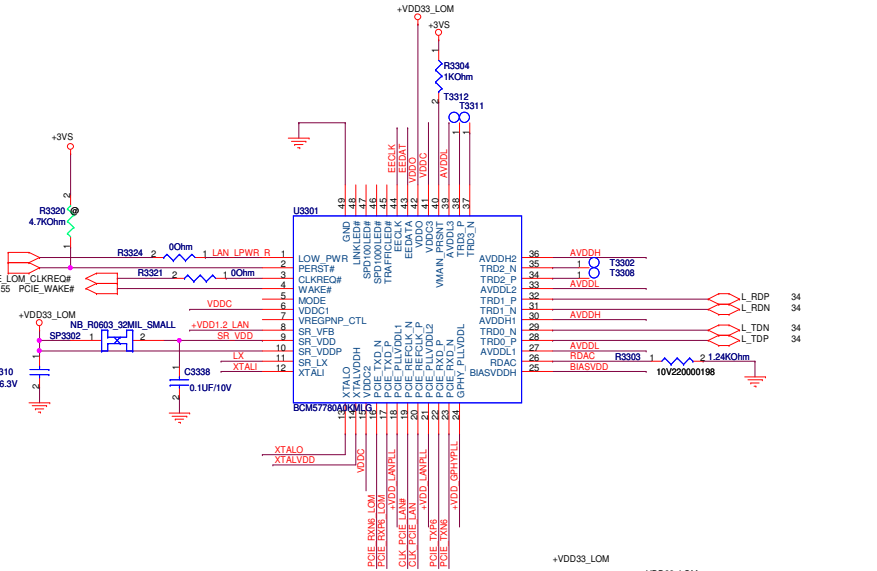
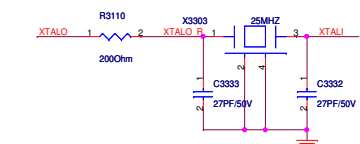
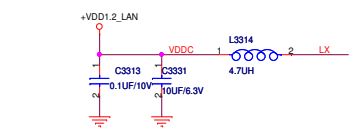
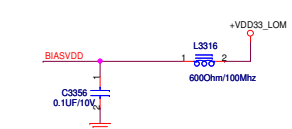
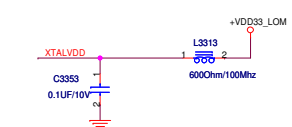
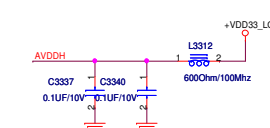
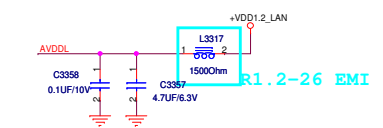
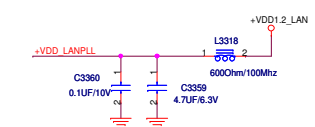
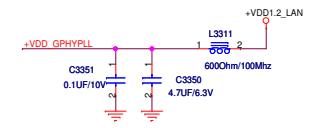
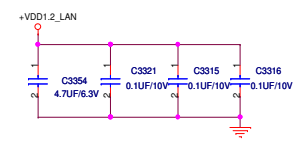
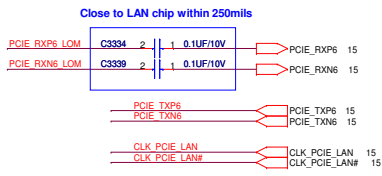


**For IT8518 Power**

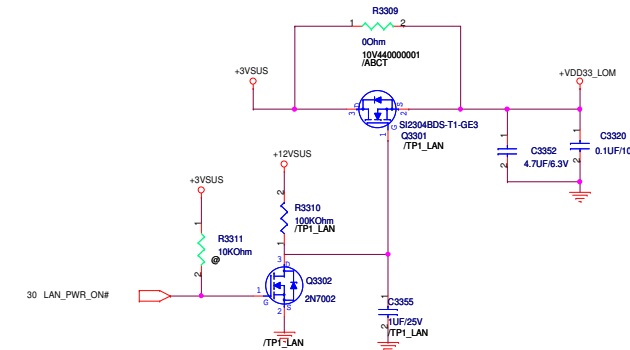
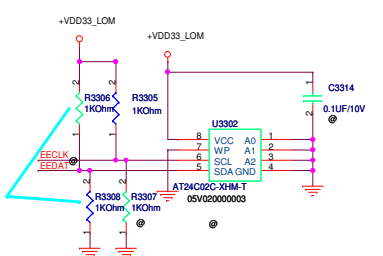


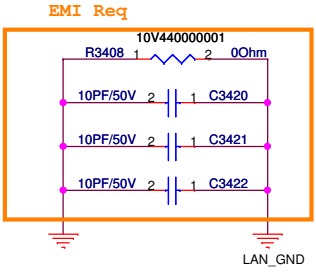
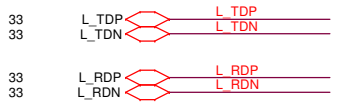
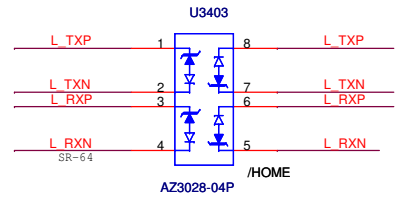
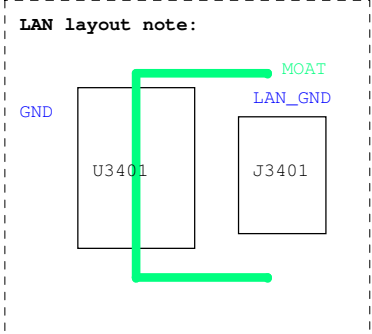
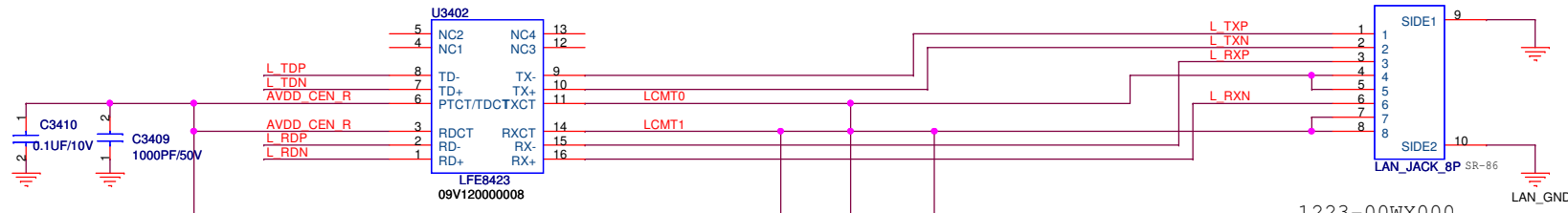
**For PU / PD**





R1.2-25  
OTP mode

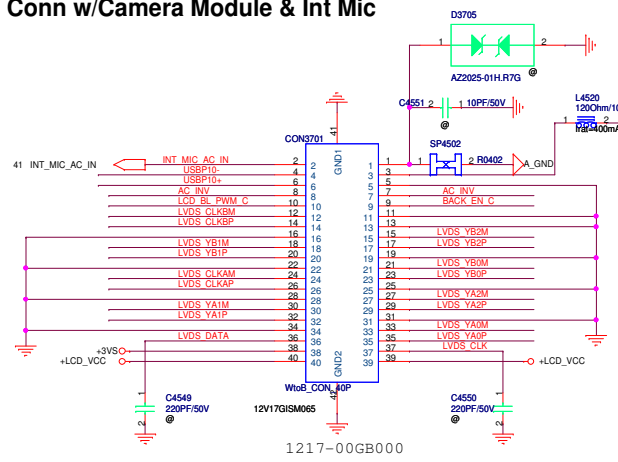




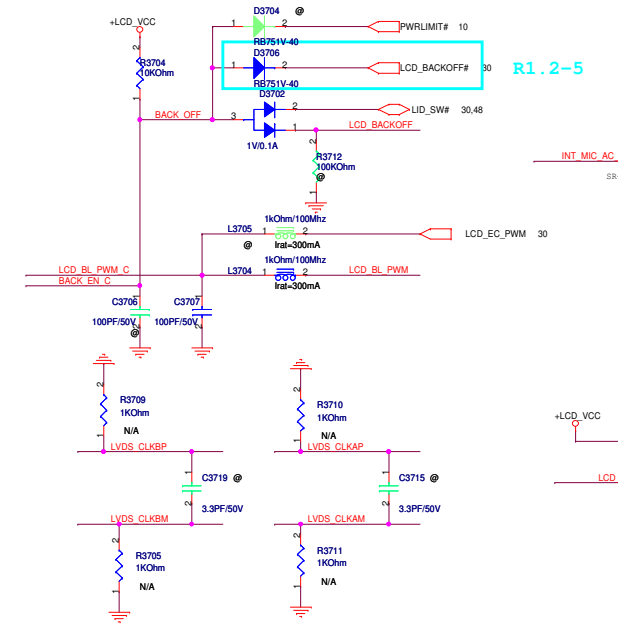
Modify LAN AR8158 circuit SR-12 0121-11  
 Modify Transformer circuit SR-40 0125-11 SR-45 0125-11 SR-48 0125-11

<b>PEGATRON</b> Title : RJ45		
BG1-HW RD Div.2-NB RD Dept.5 Engineer: Elmer Chiu		
Size B	Project Name <b>BIC50</b>	Rev 1.0
Date: Tuesday, May 03, 2011 Sheet 34 of 77		

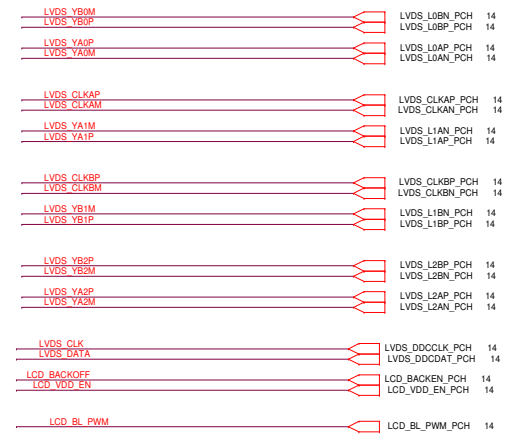
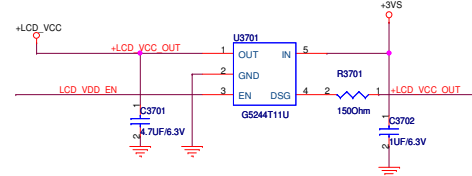
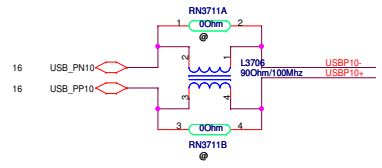
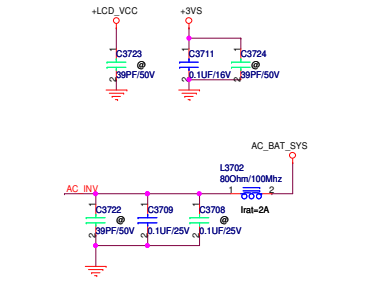
# LVDS Conn w/Camera Module & Int Mic



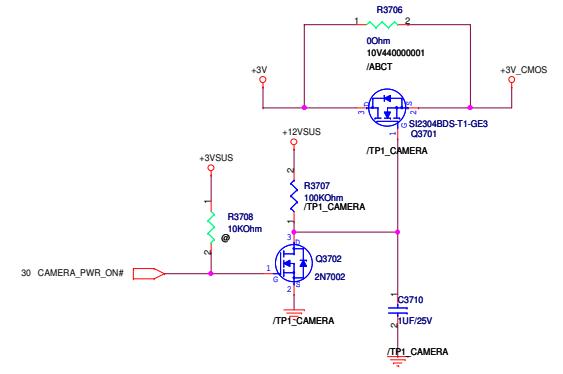
1217-00GB000  
Modify LVDS Pin definition



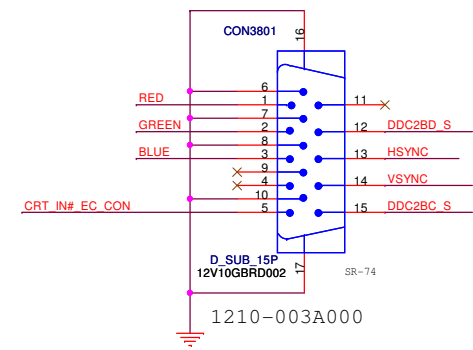
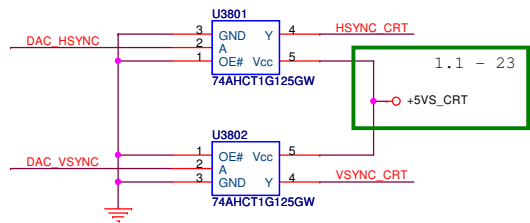
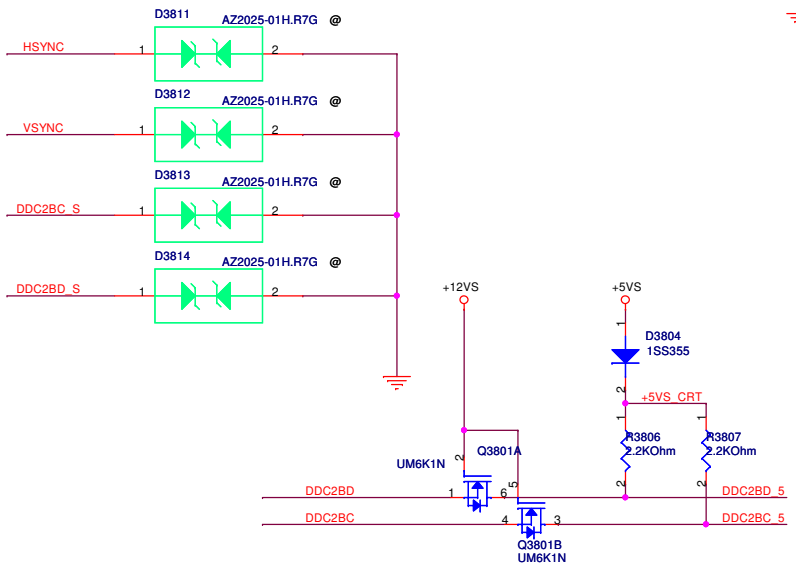
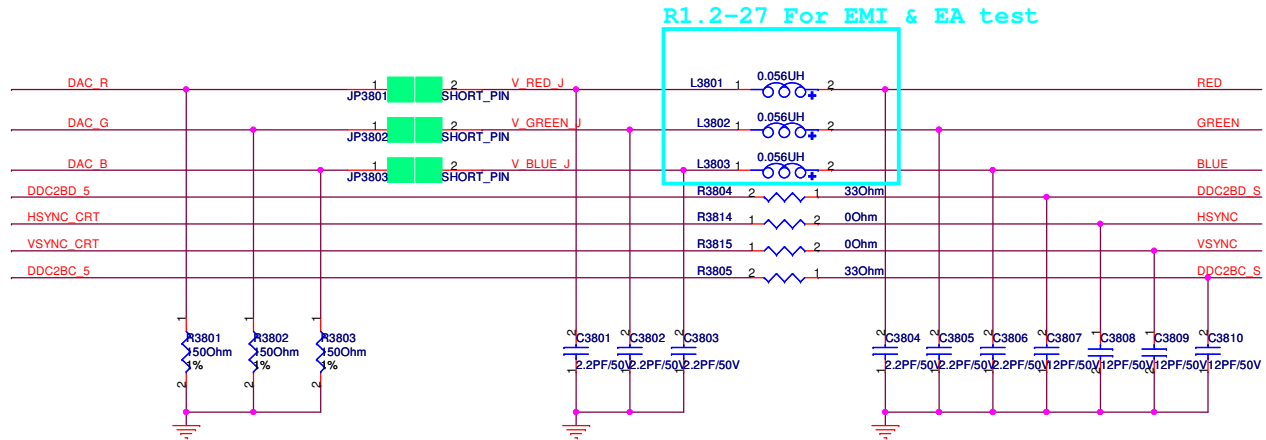
R1.2-5



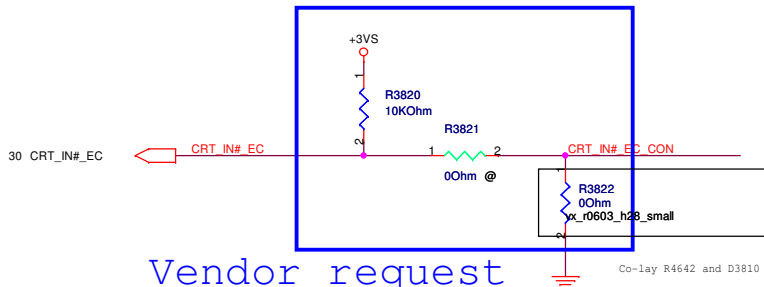
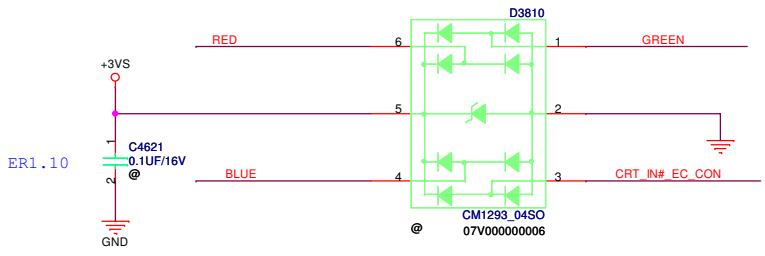
FOR TP1 02/23



- 14 DAC\_R\_PCH → DAC\_R
- 14 DAC\_G\_PCH → DAC\_G
- 14 DAC\_B\_PCH → DAC\_B
- 14 DAC\_HSYNC\_PCH → DAC\_HSYNC
- 14 DAC\_VSYNC\_PCH → DAC\_VSYNC
- 14 DDC2BD\_PCH → DDC2BD
- 14 DDC2BC\_PCH → DDC2BC

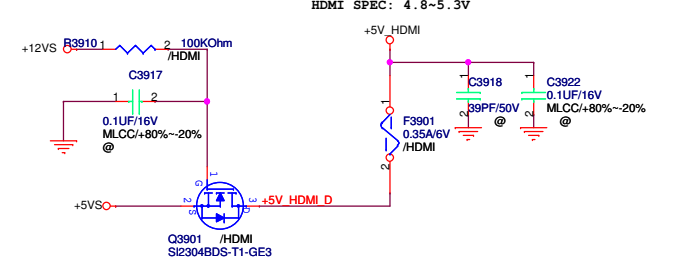
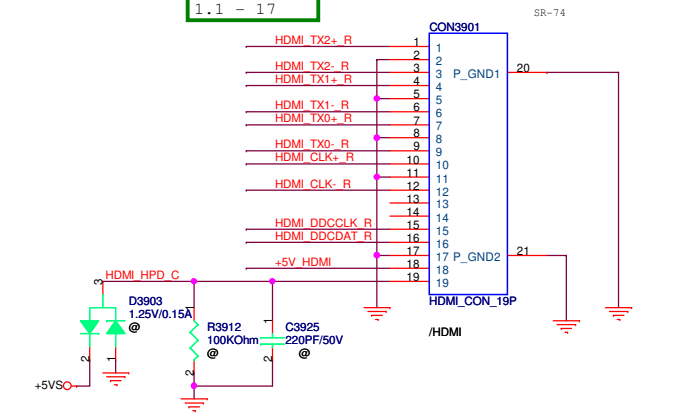
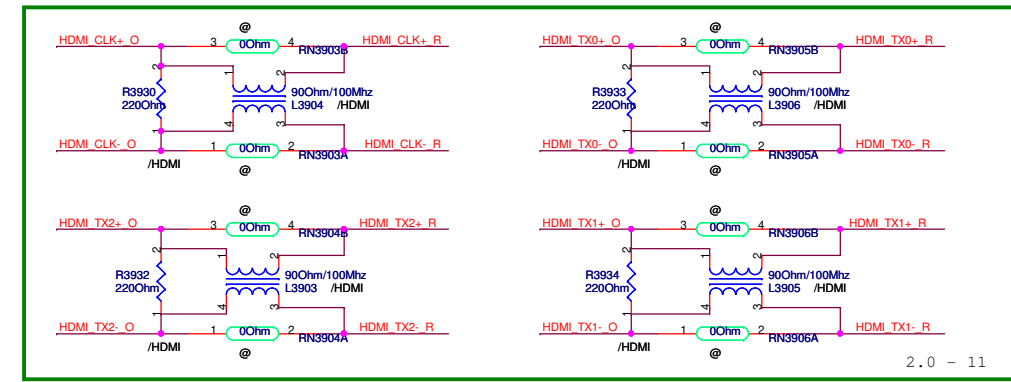
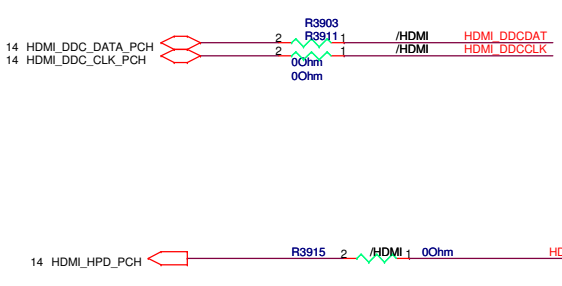
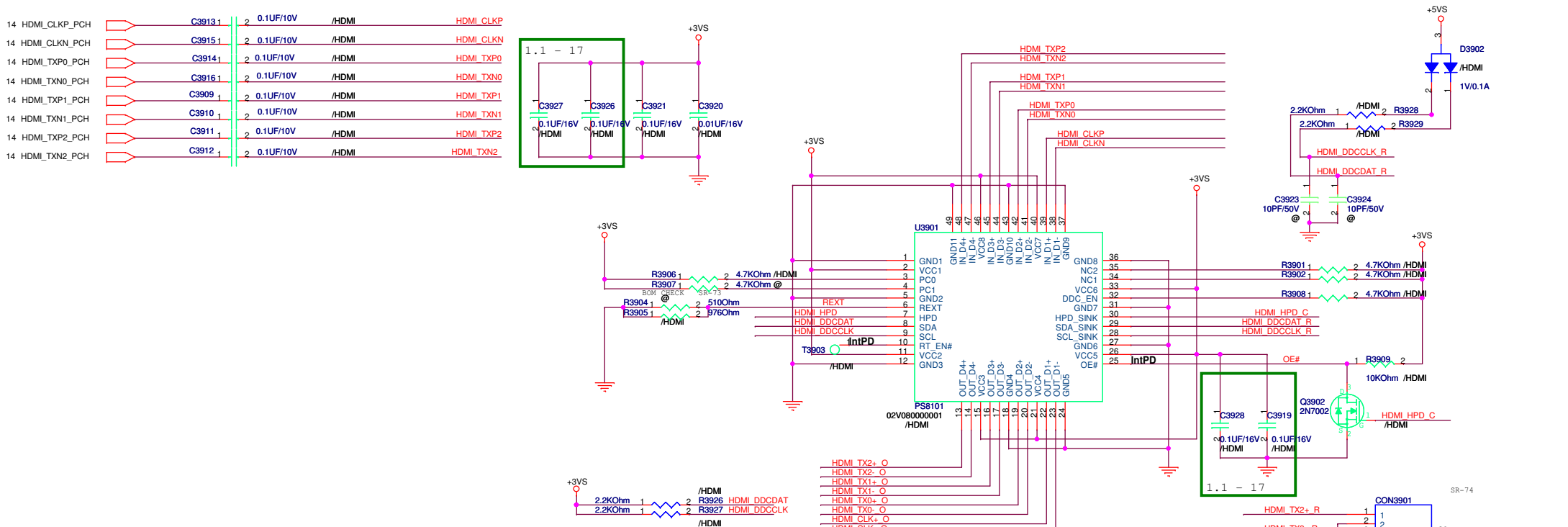


Del F3801, C3811 ADD CRT IN SR-36 0125-11



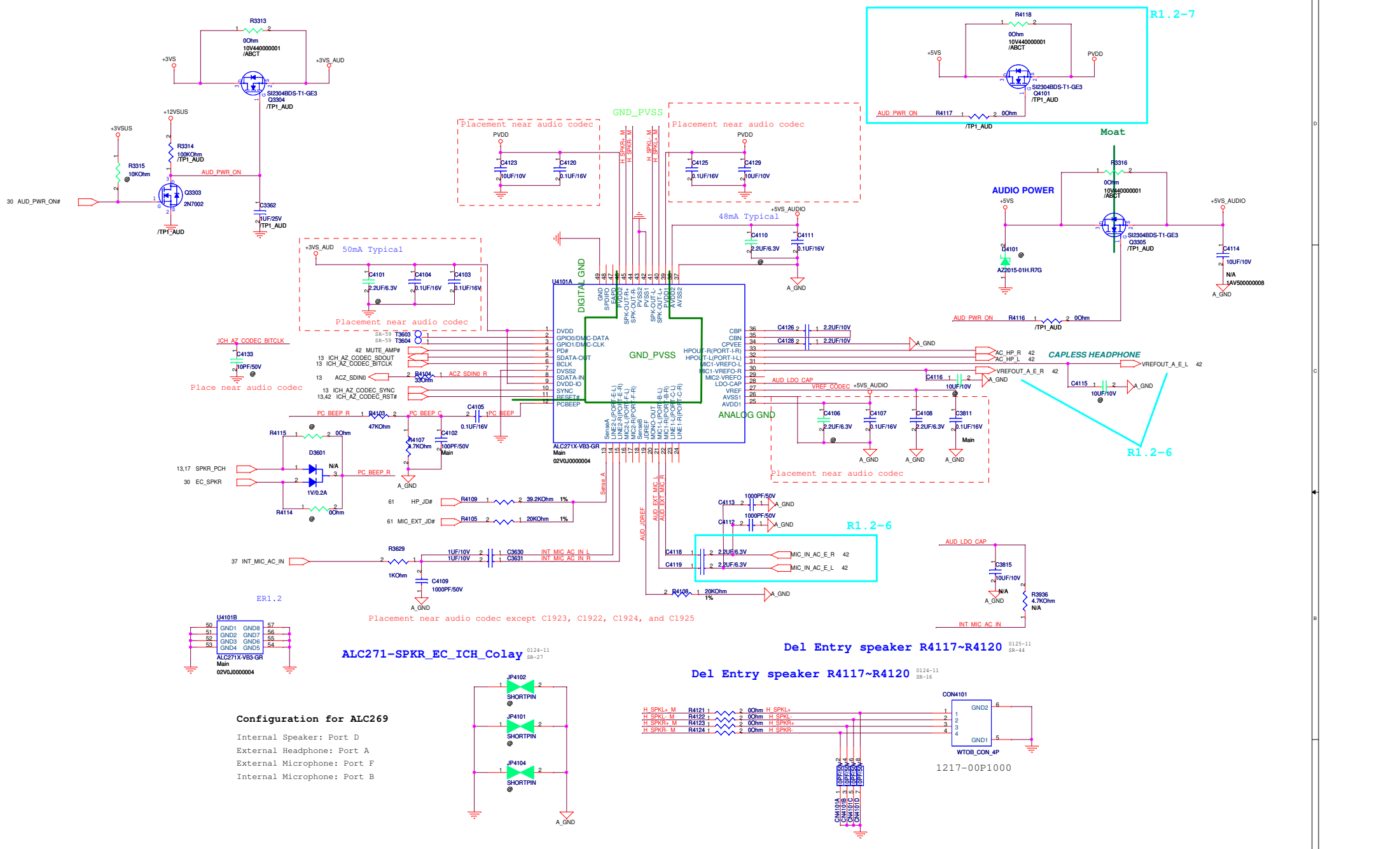
Vendor request







<b>PEGATRON</b>		Title : <i>Display Port</i>	
BU1-RD Div.1+HW RD Dept.1		Engineer: <i>Elmer Chiu</i>	
Size	Project Name		Rev
Custom	<b>BIC50</b>		2.0
Date: <i>Tuesday, May 03, 2011</i>	Sheet 40 of 77		

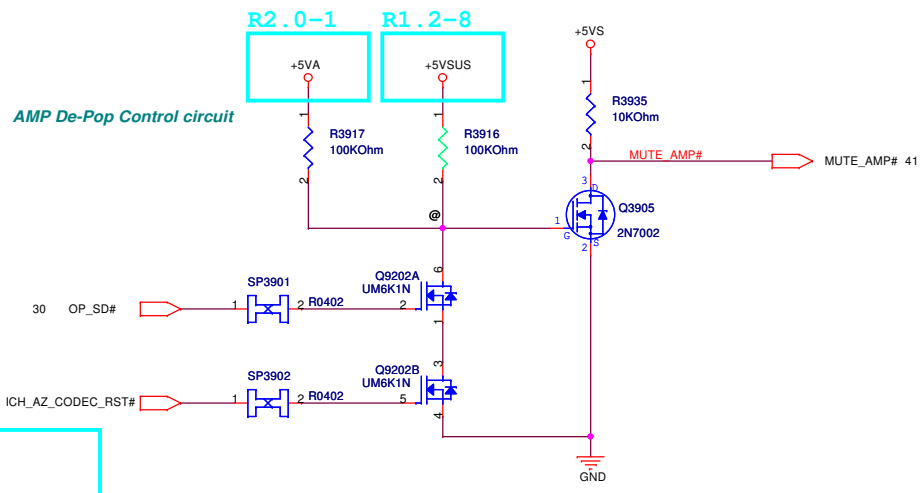


**Configuration for ALC269**  
 Internal Speaker: Port D  
 External Headphone: Port A  
 External Microphone: Port F  
 Internal Microphone: Port B

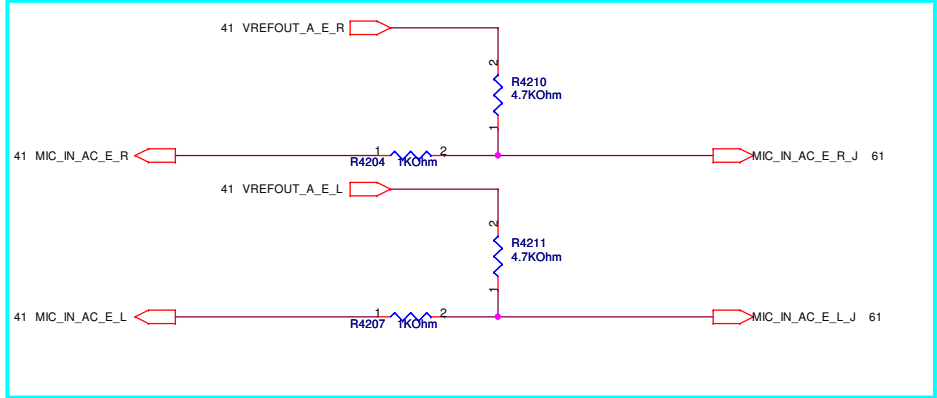
**ALC271-SPKR\_EC\_ICH\_Colay** 0124-11 SR-27

**Del Entry speaker R4117~R4120** 0125-11 SR-44

**Del Entry speaker R4117~R4120** 0124-11 SR-16



**Modify De-Pop circuit** SR-43 0125-11



**R1.2-6 Change to stereo MIC**



5

4

3

2

1

D

D

C

C

B

B

A

A

<b>PEGATRON</b>		<b>Title : MDC CONN</b>	
BG1-HW RD Div:2-NB RD Dept:5		Engineer: <i>Elmer Chiu</i>	
Size	Project Name	Rev	
C	<b>BICS0</b>	2.0	
Date: <u>Tuesday, May 03, 2011</u>		Sheet	43 of 77

5

4

3

2

1

5

4

3

2

1

D

D

C

C

B

B

A

A

Del Entry audio circuit

SR-8  
0121-11

<b>PEGATRON</b>		Title : <b>CODEC-ALC269</b>	
ASUSTeK COMPUTER INC. NB1		Engineer: <b>Elmer Chiu</b>	
Size Custom	Project Name <b>BIC50</b>	Date: <b>Tuesday, May 03, 2011</b>	Rev <b>2.0</b>
		Sheet	44 of 77

5

4

3

2

1

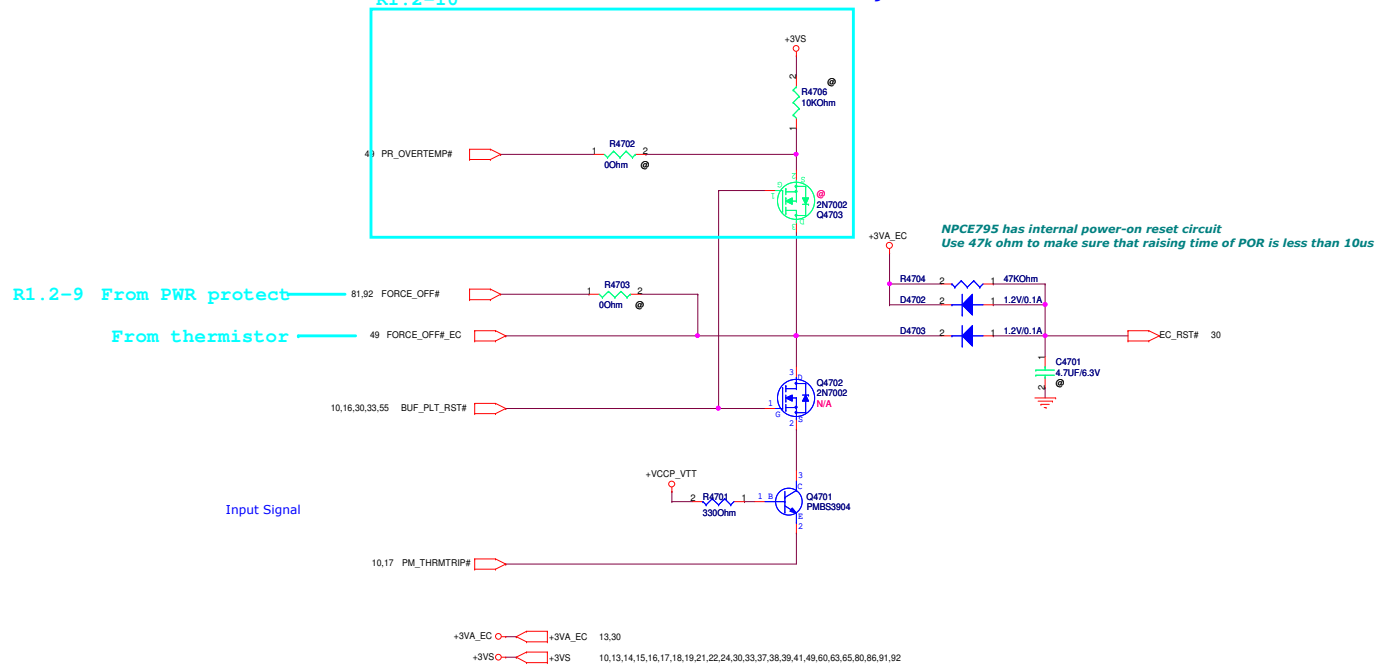
Del Entry audio circuit

SR-8  
0121-11

<b>PEGATRON</b> Title : <b>AUDIO ALC269</b>	
BU1-RD Div.1+HW RD Dept.1 Engineer: <b>Elmer Chiu</b>	
Size Custom	Project Name <b>BIC50</b>
Date: <b>Tuesday, May 03, 2011</b>	Rev <b>2.0</b>
Sheet 45 of 77	

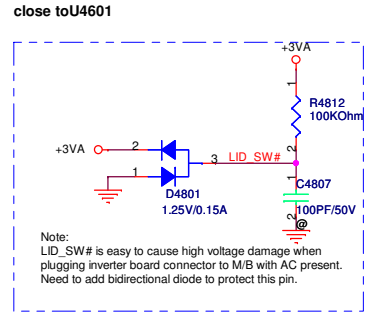
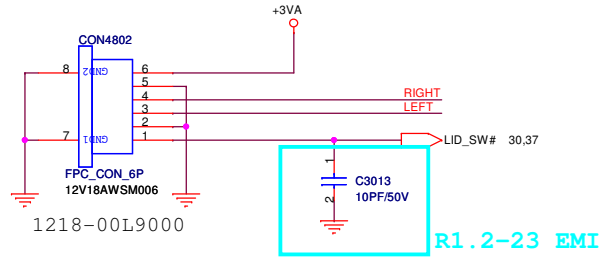
R1.2-10

### Thermal Policy

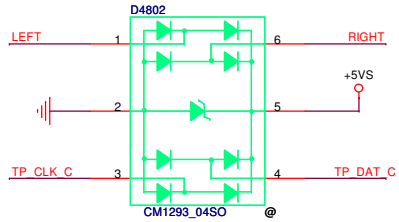
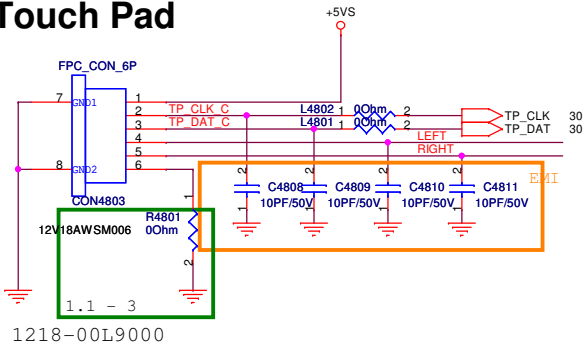




# Touch Pad Button/ Hall Sensor

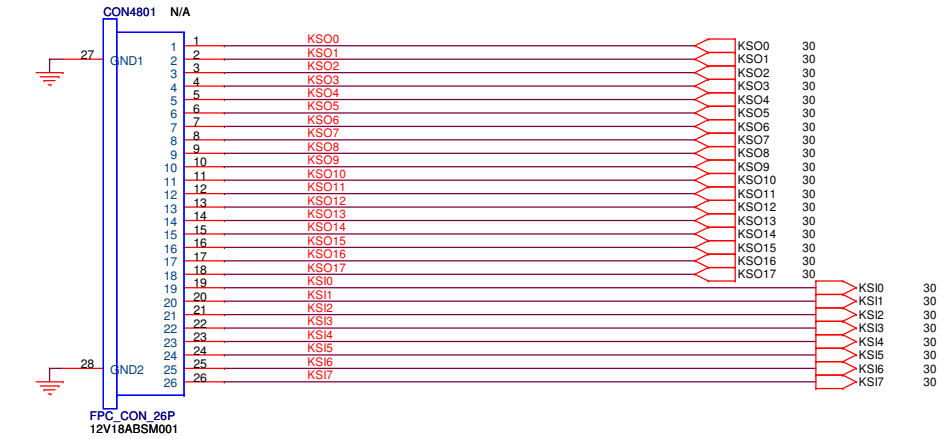


# Touch Pad

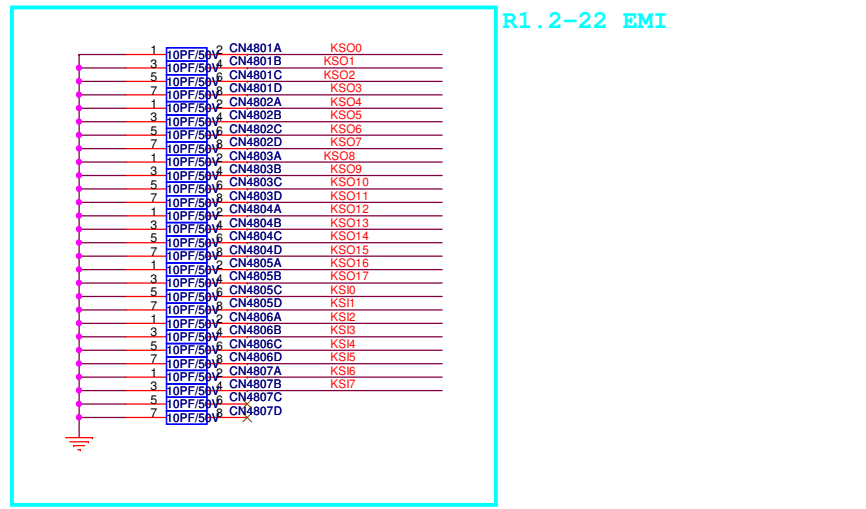


Remove TP button circuit SR-22 0124-11

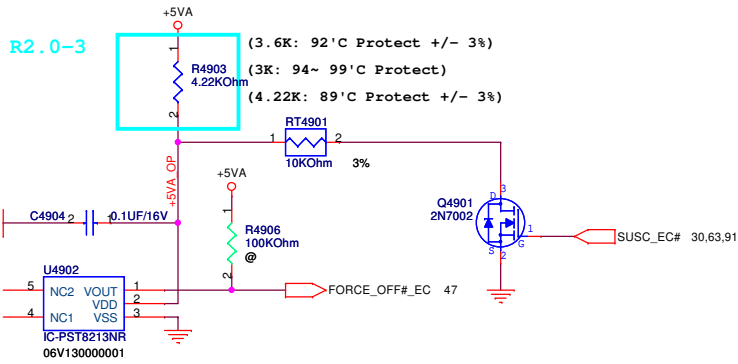
# Keyboard



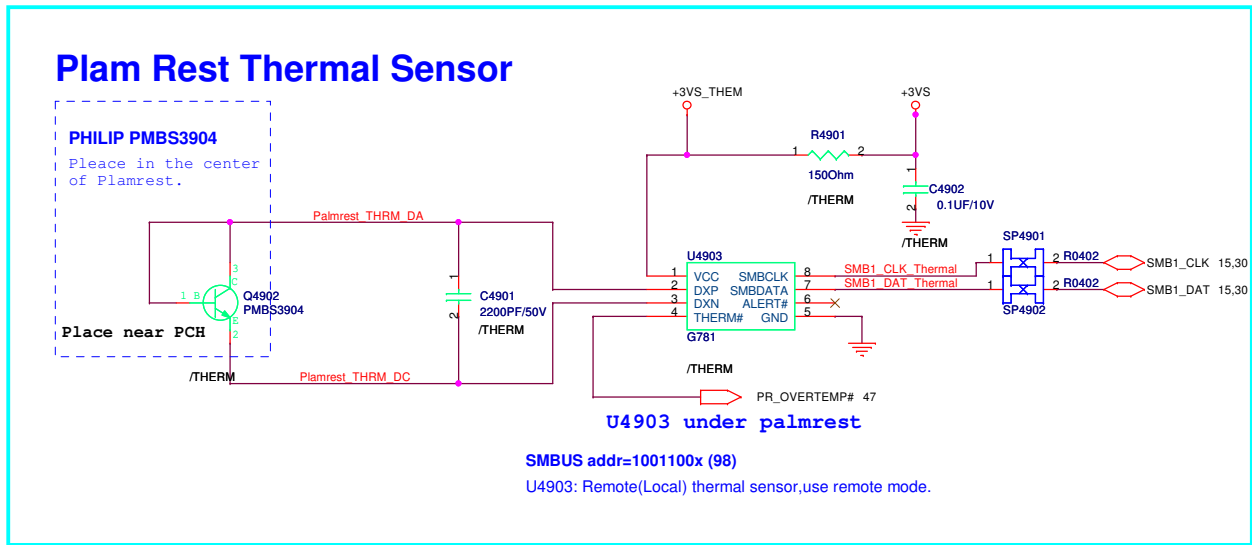
1218-00MW000



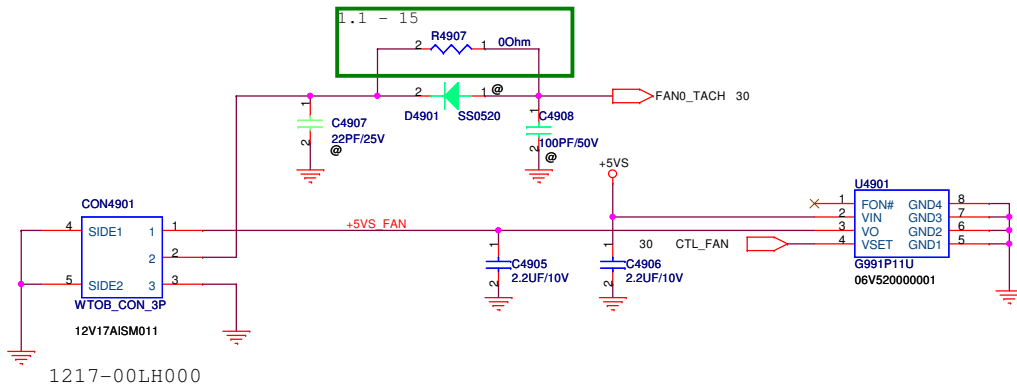
# Thermister

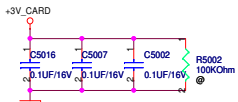
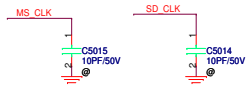
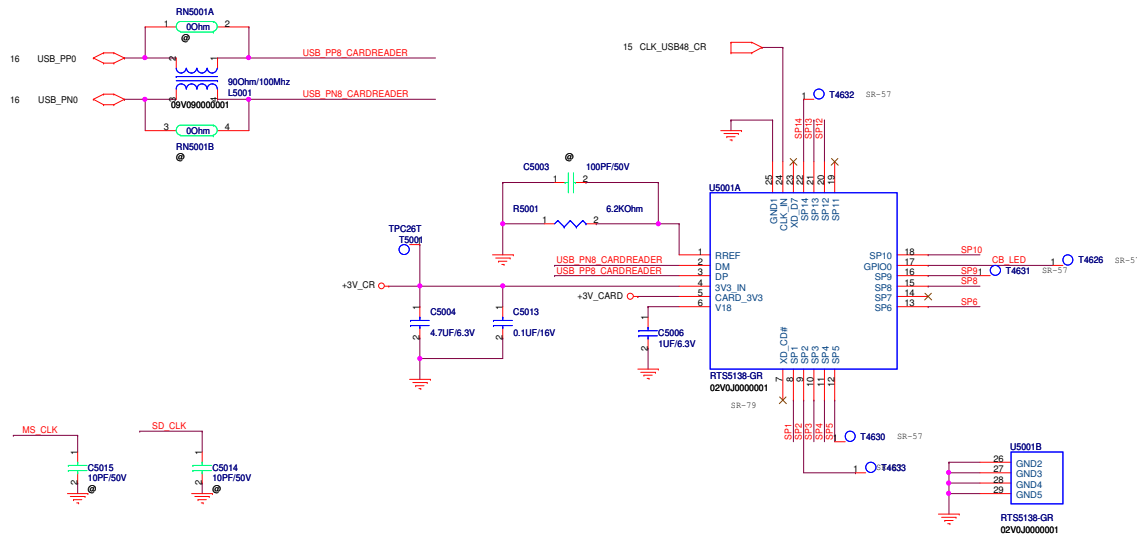


# Plam Rest Thermal Sensor



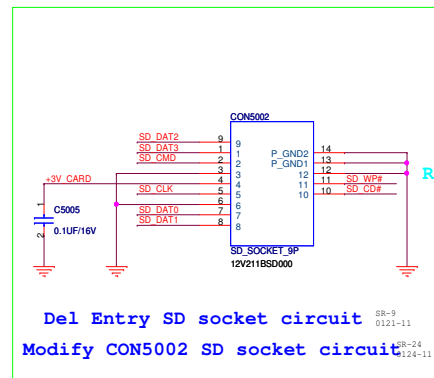
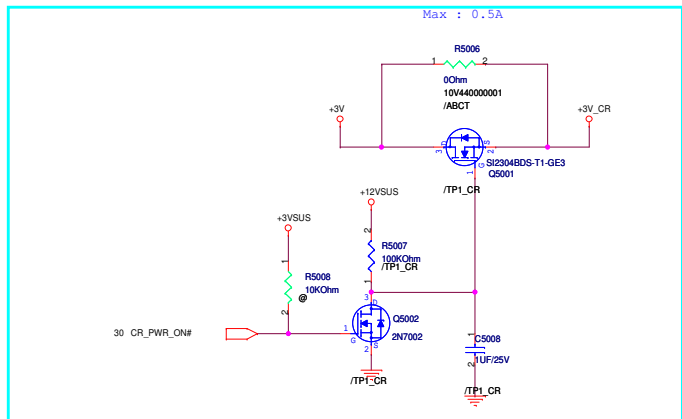
# FAN





Close to connector

FOR TP1 02/23



Del Entry SD socket circuit SR-9 0121-11  
 Modify CON5002 SD socket circuit SR-24 1124-11

Pin Name	Description
SP1	SDWP# / MSQLK
SP2	MS_INS#
SP3	SD_DAT1
SP4	SD_DAT0
SP5	MS_D3
SP6	SD_CD#
SP8	SD_CLK / MS_D2
SP9	MS_D0
SP10	SD_CMD
SP12	SD_DAT3 / MS_D1
SP13	SD_DAT2
SP14	MS_BS

SP1	SD WP#	MS CLK
SP2		MS INS#
SP3	SD DAT1	
SP4	SD DAT0	
SP5		MS D3
SP6	SD CD#	
SP8	SD CLK	MS D2
SP9		MS D0
SP10	SD CMD	
SP12	SD DAT3	MS D1
SP13	SD DAT2	
SP14		MS BS

5

4

3

2

1

D

D

C

C

B

B

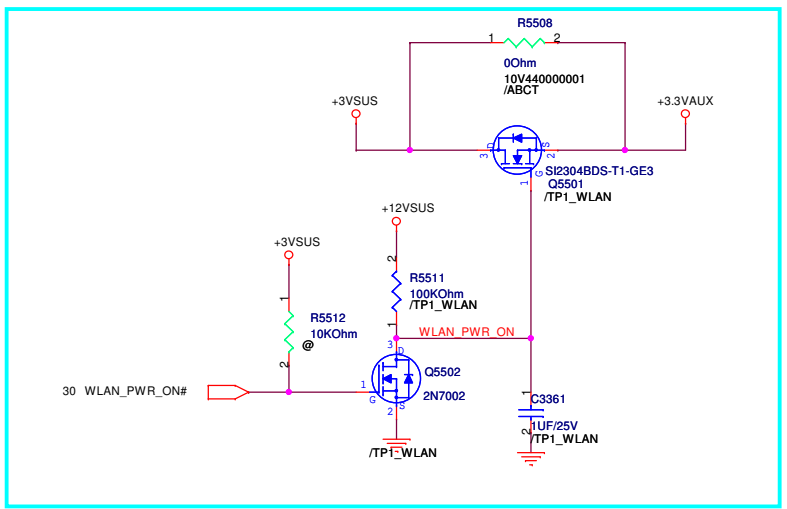
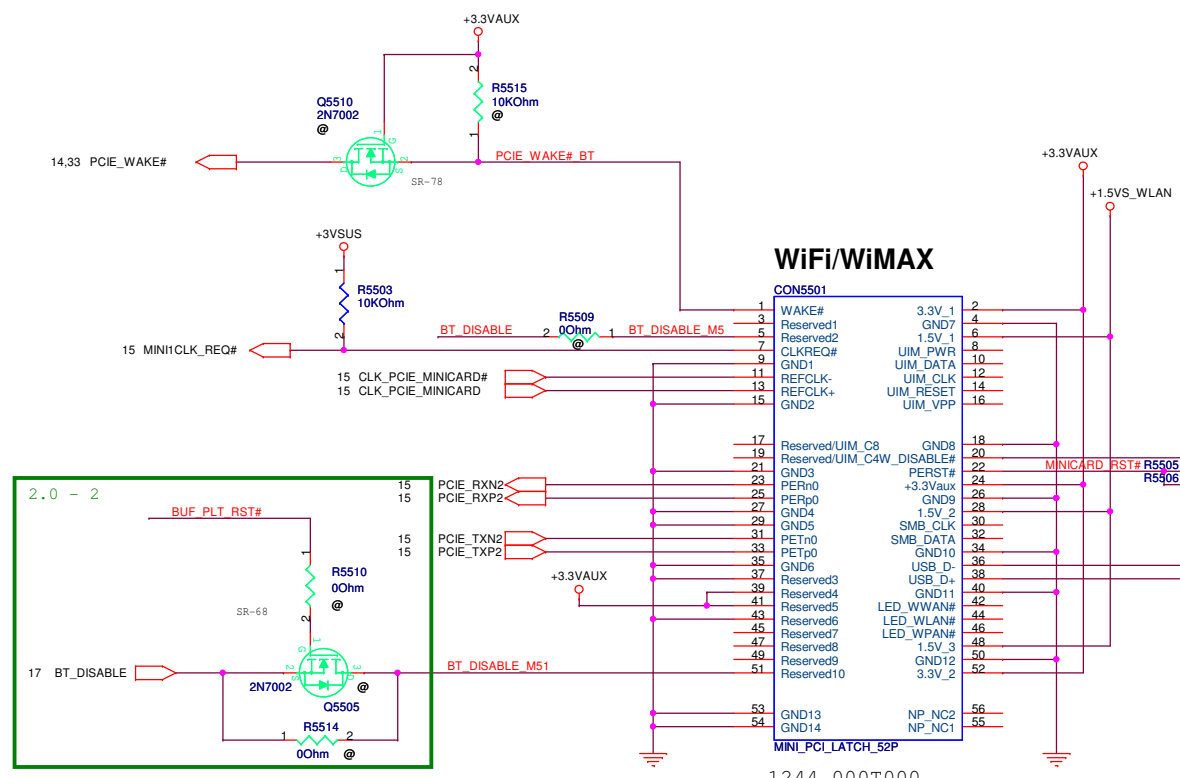
A

A

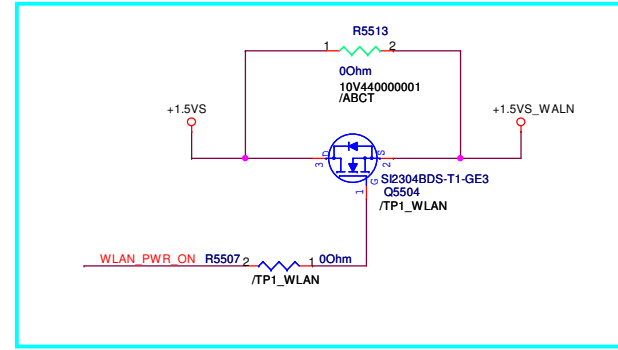
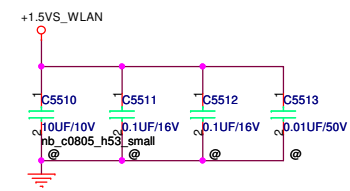
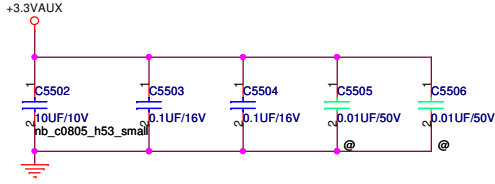
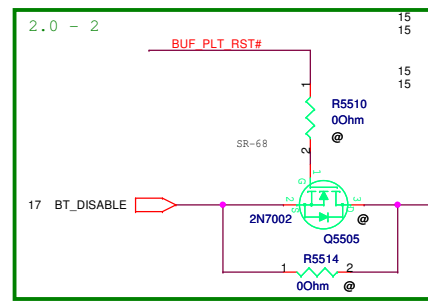
<b>PEGATRON</b>		<b>Title : USB3.0 uPD720200</b>	
<small>BG11HW1</small>		<b>Engineer: Elmer Chiu</b>	
<small>Size</small>	<small>Project Name</small>	<small>Rev</small>	
C	<b>BIC50</b>	2.0	
<small>Date: Tuesday, May 03, 2011</small>		<small>Sheet</small>	<small>53 of 77</small>



<b>PEGATRON</b> Title : <b>PCIE NEW CARD</b>	
BU1-RD Div.1+HW RD Dept.1 Engineer: <b>Elmer Chiu</b>	
Size Custom	Project Name <b>BIC50</b>
Date: <b>Tuesday, May 03, 2011</b>	Rev <b>2.0</b>
Sheet <b>54</b> of <b>77</b>	



FOR TP1 02/24



R1.2-12



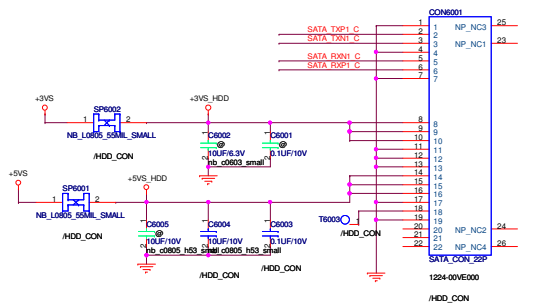
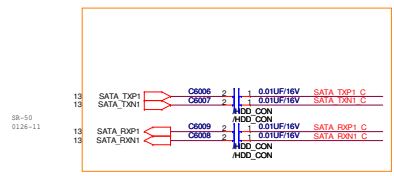
<b>PEGATRON</b>		Title : <b>MINICARD (NWAN)</b>	
BU1-RD Div.1+HW RD Dept.1		Engineer:	
Size	Project Name	Rev	
Custom		2.0	
Date: <b>Tuesday, May 03, 2011</b>	Sheet	56	of 77



<b>PEGATRON</b>		Title : <b>MINICARD (WUSB /UPCONVERT)</b>	
BU1-RD Div.1+HW RD Dept.1		Engineer: <b>Elmer Chiu</b>	
Size	Project Name		Rev
Custom	<b>BIC50</b>		2.0
Date: <b>Tuesday, May 03, 2011</b>		Sheet	57 of 77



R2.0-28

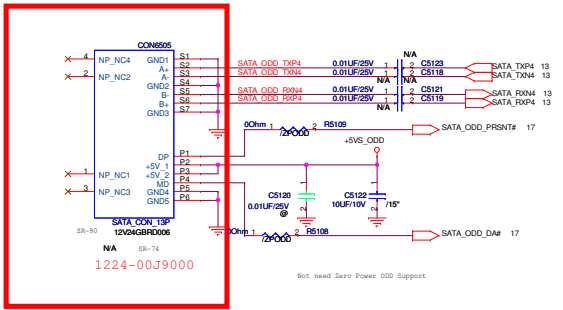


Change HDD CON6001 02/17

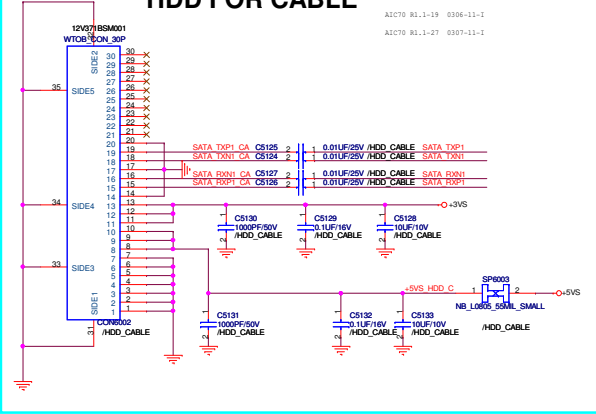
HDD

SSD

ODD



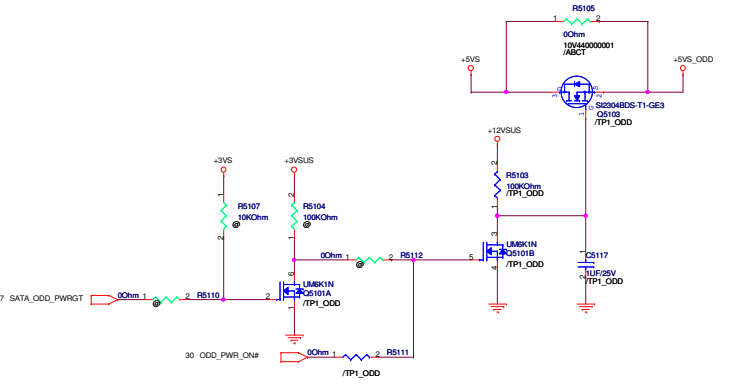
HDD FOR CABLE

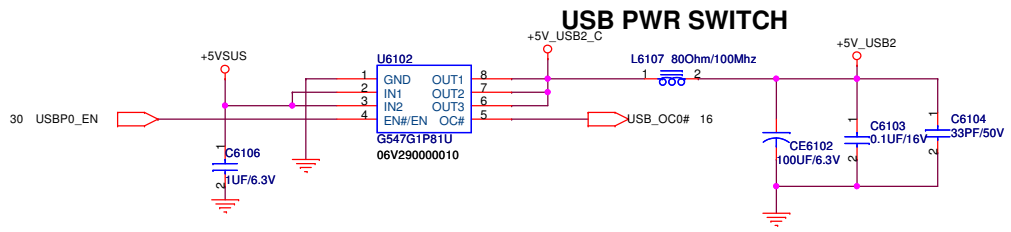


R1.2-13

ZERO POWER ODD SUPPORT

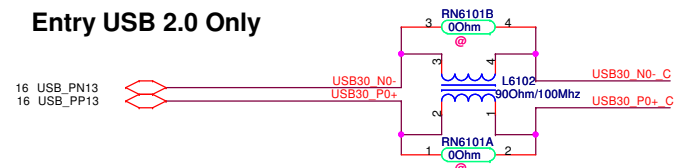
support Hokey turn off ODD power





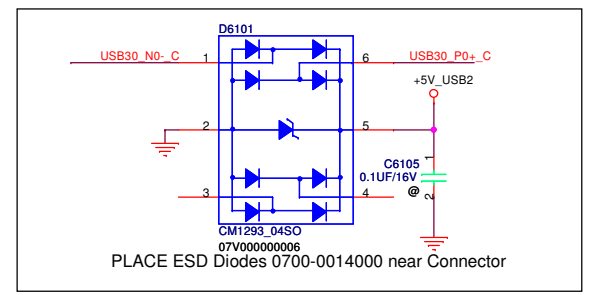
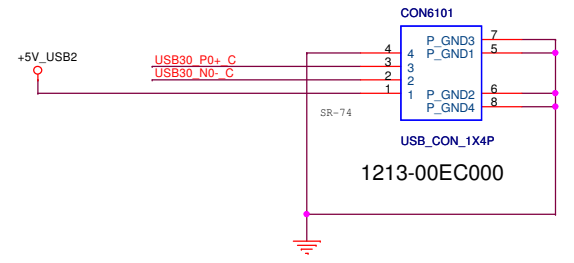
change USB power switch circuit SR-1 0120-11 SR-26 0124-11 SR-34 0125-11

Entry USB 2.0 Only



Modify D6101, RN6101, RN6105, RN6106 SR-30 0125-11

USB 2.0

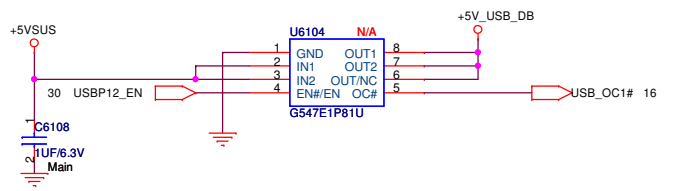


PLACE ESD Diodes 0700-0014000 near Connector

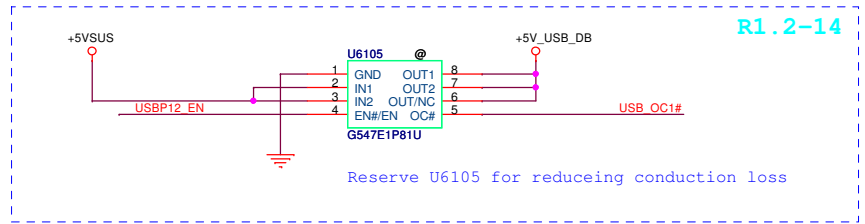
USB Conn. for Entry colay HDMI USB 2.0

Remove USB\_9 (HDMI) SR-21 0124-11

USB Power Switch for USB DB Main

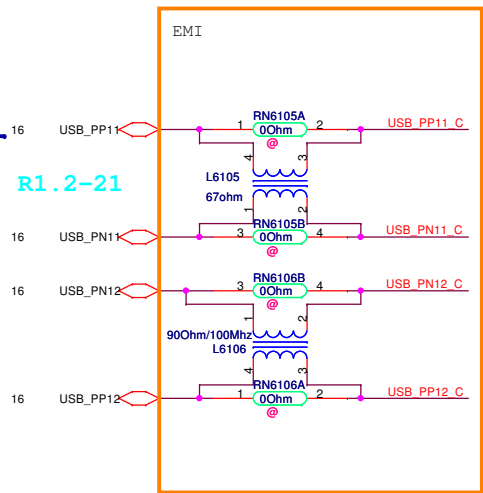


change USB power switch circuit SR-26 0124-12 SR-38 0125-13

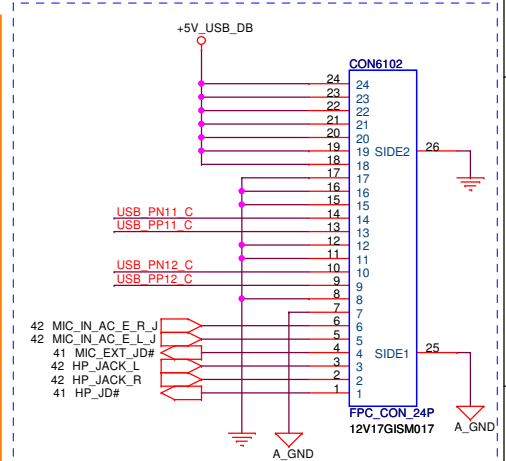


Reserve U6105 for reducing conduction loss

AUDIO BOARD/w USB2.0 x2



R1.2-21



R1.2-14 Change Connector for stereo MIC & USB PWR

TouchPanel CON

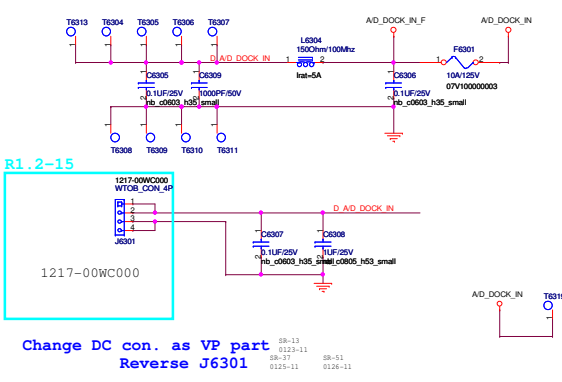
Camera Module CON

B/T MODULE

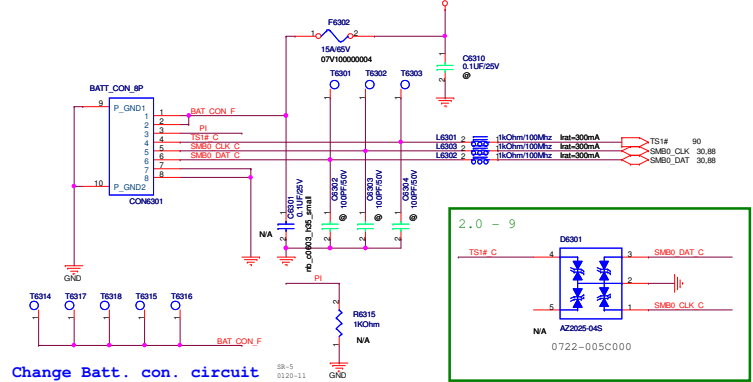
FELICA MODULE

<b>PEGATRON</b>		Title : <i>Camera/ BT/ FL CONN</i>	
BU1-RD Div.1+HW RD Dept.1		Engineer: <i>Elmer Chiu</i>	
Size	Project Name	Rev	
Custom	<b>BIC50</b>	2.0	
Date: <i>Tuesday, May 03, 2011</i>		Sheet	62 of 77

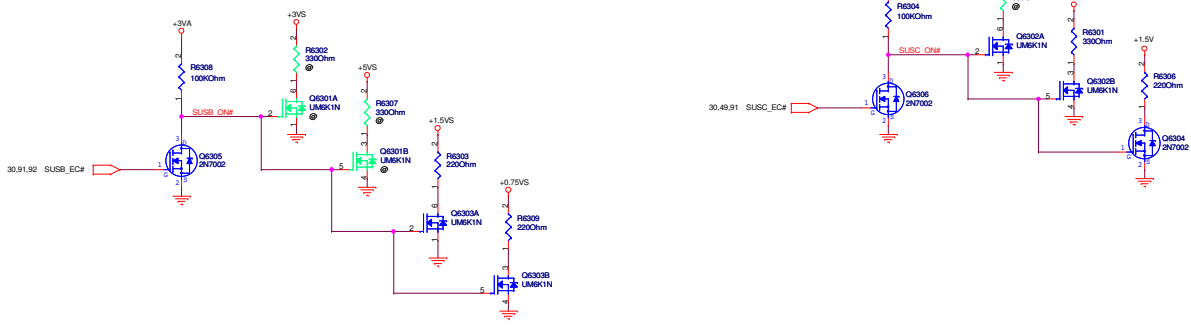
### DC IN



### Battery Connector



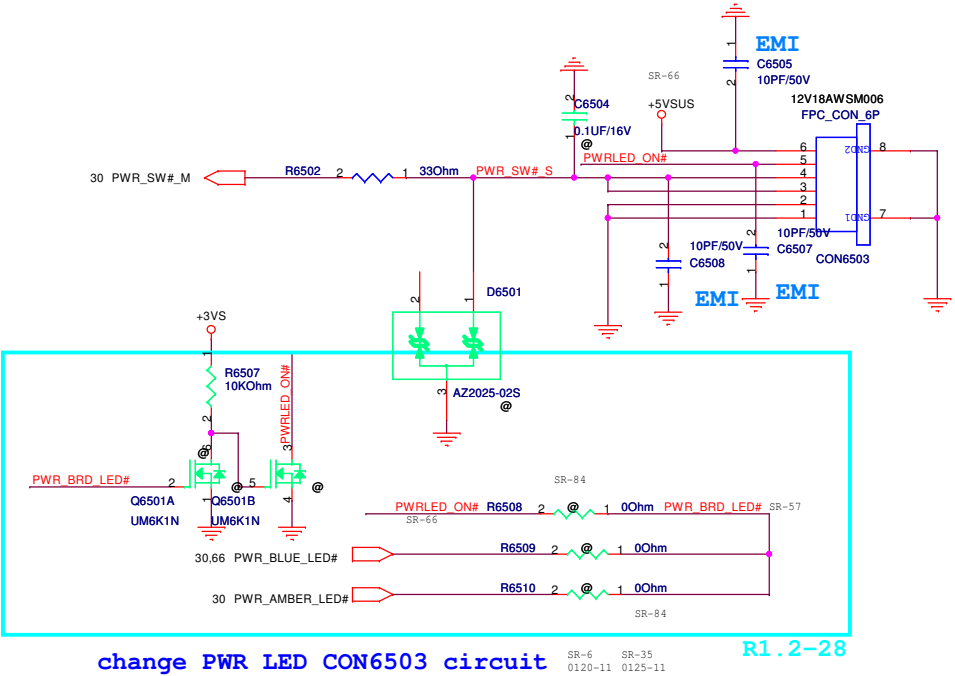
### Discharge Circuit



Notes:  
BRAIDWOOD right angled Connector (1.8V keyed)  
Compatible BRAIDWOOD Modules  
1.8V Mobile NVM 4GB 31.60mm x21.5mm  
1.8V Mobile NVM 8GB 31.60mm x 21.5mm  
1.8V Mobile NVM 16GB 31.60mm x 32.5mm

<b>PEGATRON</b> Title : <i>NVM</i>	
BU1-RD Div.1+HW RD Dept.1 Engineer: <i>Elmer Chiu</i>	
Size Custom	Project Name <b>BIC50</b>
Date: <i>Tuesday, May 03, 2011</i>	Rev 2.0
1 Sheet 64 of 77	

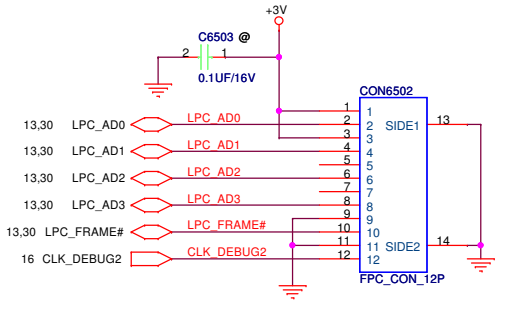
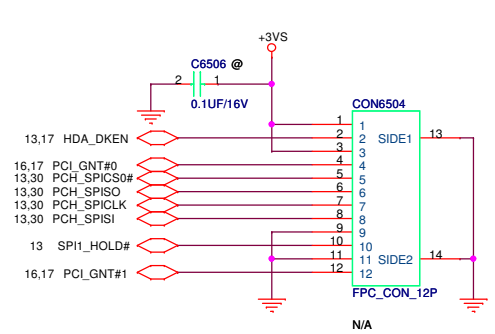
# PWR BRD/ AMBIENT/ HALL CONN.



# MODEM MODULE

# KILL SWITCH.

# DEBUG CARD CONN.



# LED (Main)

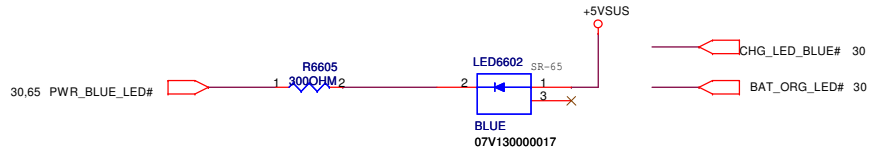
Left ← Right

- DC-IN**
- Power**
- Main Battery**
- HDD/ODD**
- Bridge Media**
- WiFi**

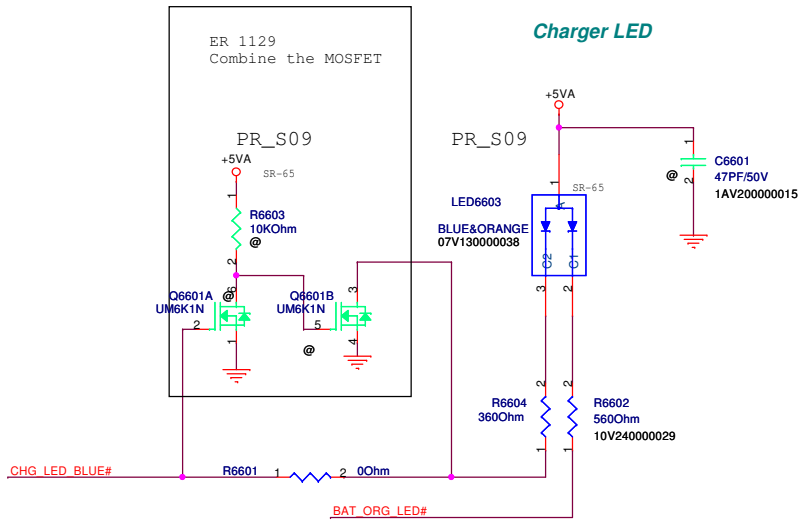
White      White Amber (Blink)      White Amber (Blink)      White      White      Amber

## Battery

### Power LED



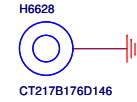
### Charger LED



Remove LED circuit SR-18 0124-11

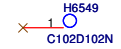
Modify LED circuit SR-28 0124-11 SR-39 0125-11

## WLAN NUT

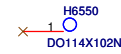


SR-69

### Fix hole

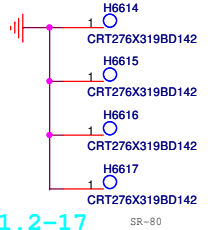
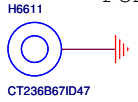


### Detail C



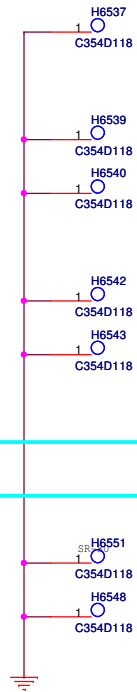
## PCH Local Side Symbol

### FCH



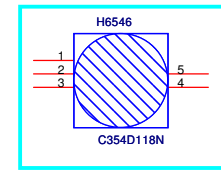
### Screw Px4 CPU

### Screw Ax15

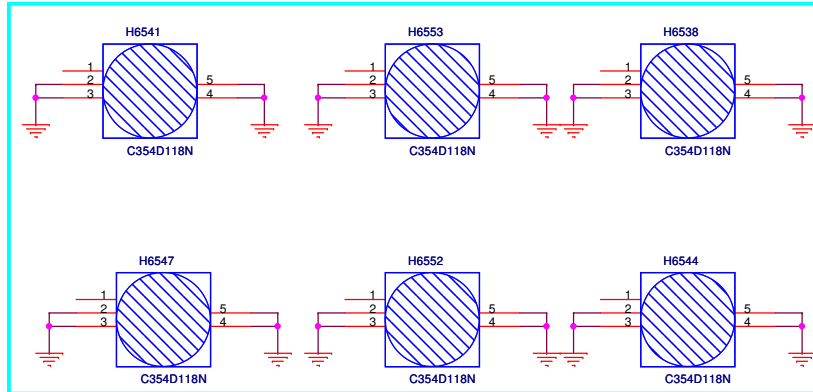


R1.2-17

### R1.2-16 EMI



### R2.0-4



**PEGATRON** Title : LED CIR/ FW SCREW

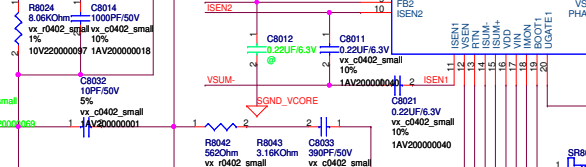
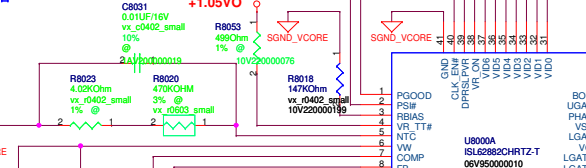
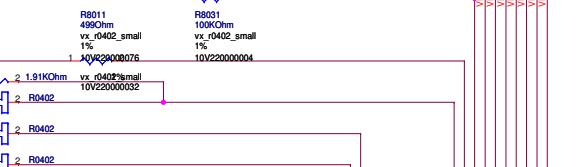
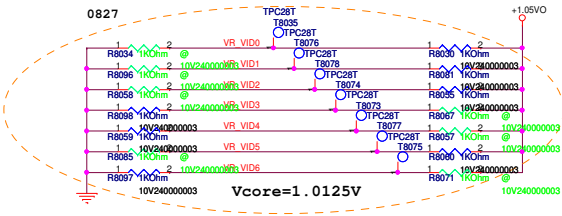
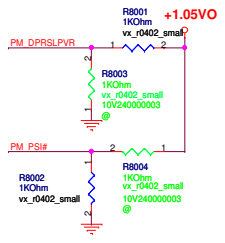
BU1-RD Div.1-HW RD Dept.1 Engineer: Elmer Chiu

Size	Project Name	Rev
Custom	<b>BIC50</b>	2.0
Date: Wednesday, May 18, 2011	Sheet	66 of 77



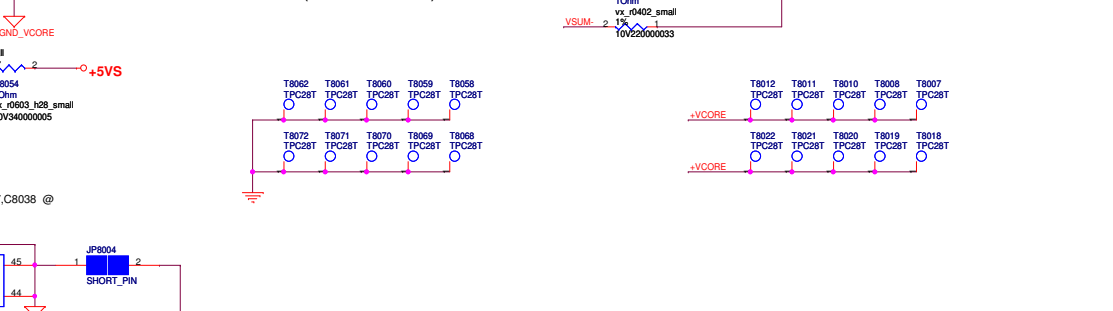
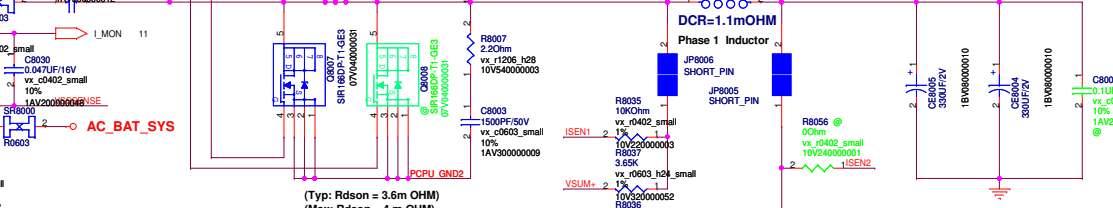
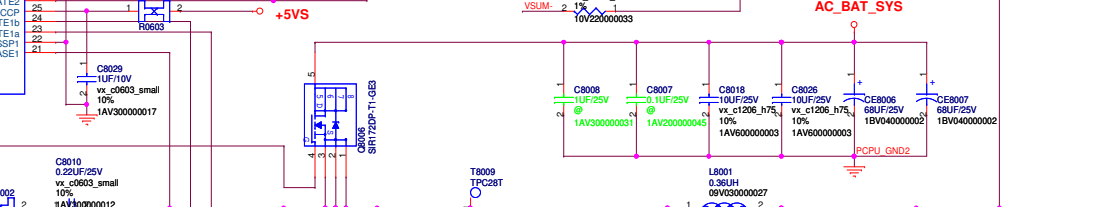
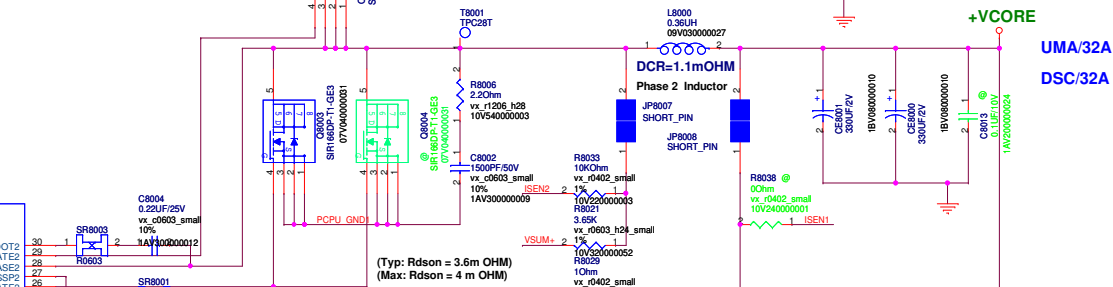
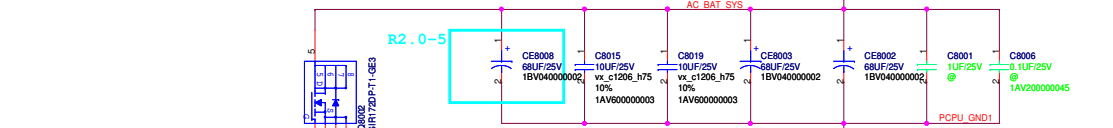
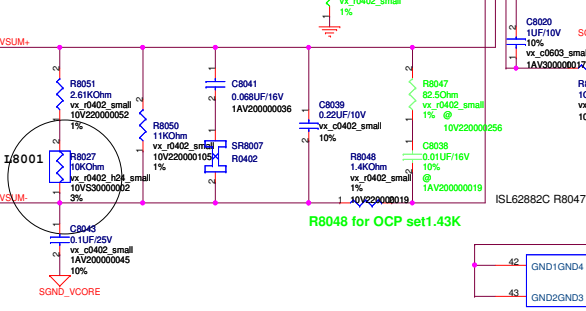
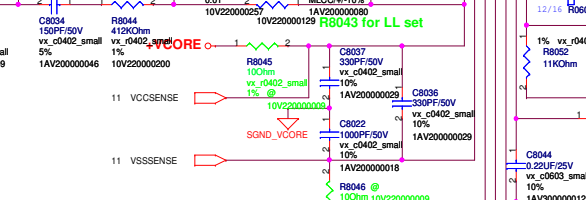
<b>PEGATRON</b>		Title : <i>G-Sensor TSH35TR</i>	
<i>BU1-RD Div.1+HW RD Dept.1</i>		Engineer: <i>Elmer Chiu</i>	
Size	Project Name		Rev
Custom			2.0
Date: <i>Tuesday, May 03, 2011</i>	Sheet <i>69</i> of <i>77</i>		

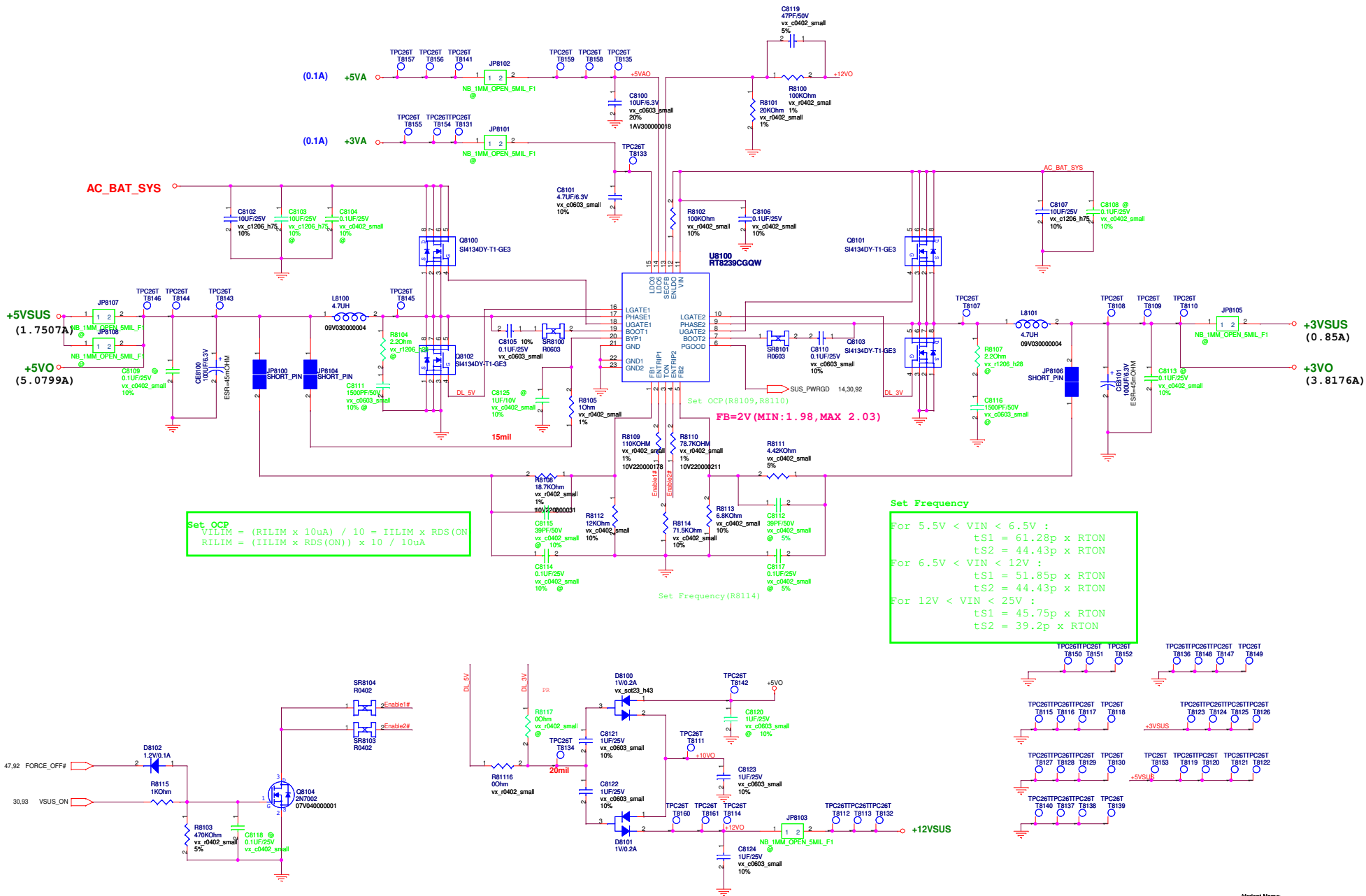




$R8024 = (\text{Period}(\text{us}) - 0.29) \cdot 2.65$   
 $\text{Period}(\text{us}) = 1/300\text{KHz}$   
 Adjust R8043 for  
 (Loadline = -1.9mV/A calpella SV)  
 R8025 Setting OCP

PM_DPRSLPVR	PM_PSI#	VO_action
L	L	1 Phase DE
H	L	1 Phase DE
L	H	2 Phase CCM
H	H	1 Phase DE



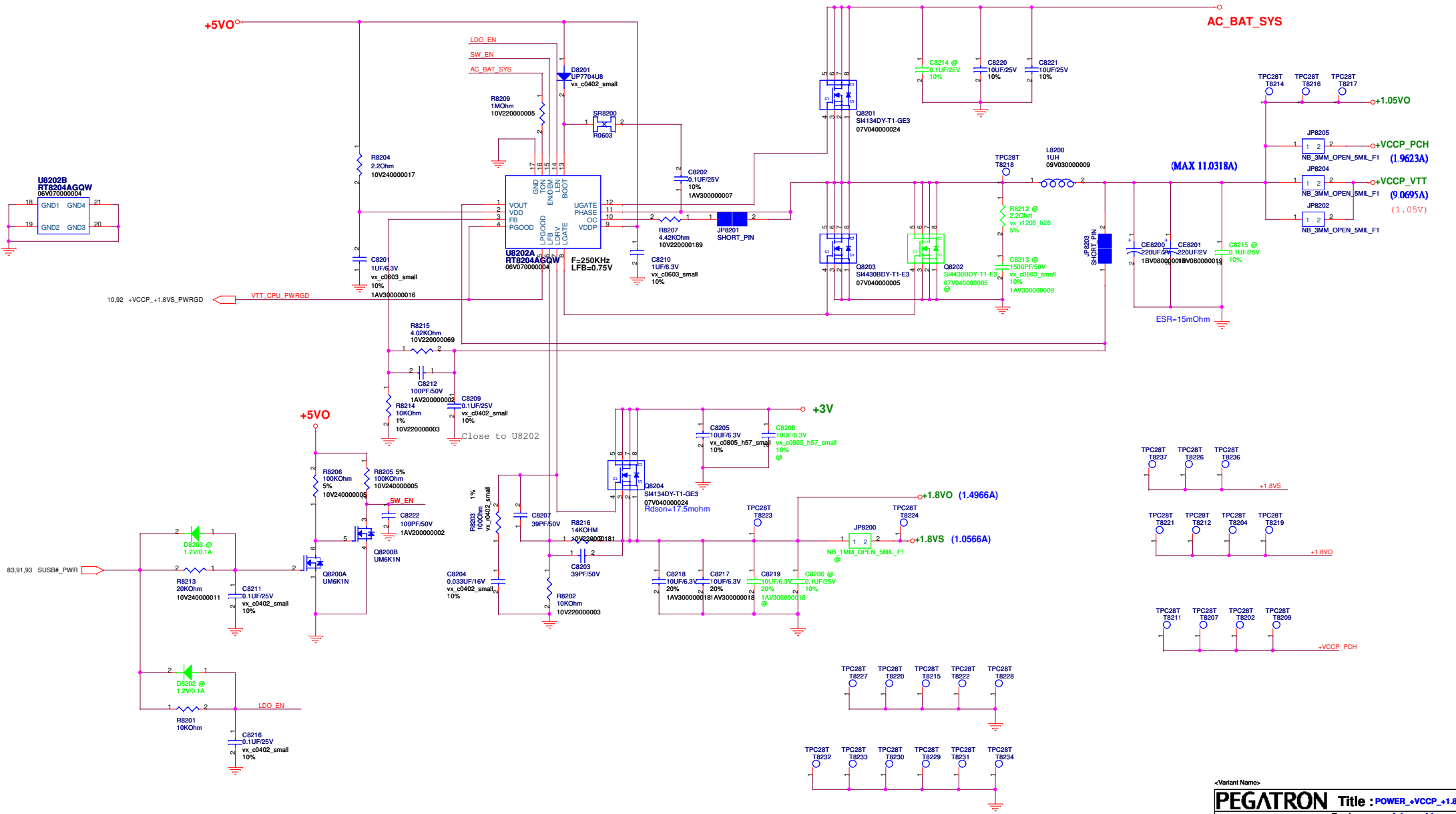


Set OCP  
 $V_{ILIM} = (R_{ILIM} \times 10\mu A) / 10 = I_{ILIM} \times R_{DS(ON)}$   
 $R_{ILIM} = (I_{ILIM} \times R_{DS(ON)}) \times 10 / 10\mu A$

Set Frequency  
 For  $5.5V < V_{IN} < 6.5V$  :  
 $t_{S1} = 61.28p \times R_{TON}$   
 $t_{S2} = 44.43p \times R_{TON}$   
 For  $6.5V < V_{IN} < 12V$  :  
 $t_{S1} = 51.85p \times R_{TON}$   
 $t_{S2} = 44.43p \times R_{TON}$   
 For  $12V < V_{IN} < 25V$  :  
 $t_{S1} = 45.75p \times R_{TON}$   
 $t_{S2} = 39.2p \times R_{TON}$

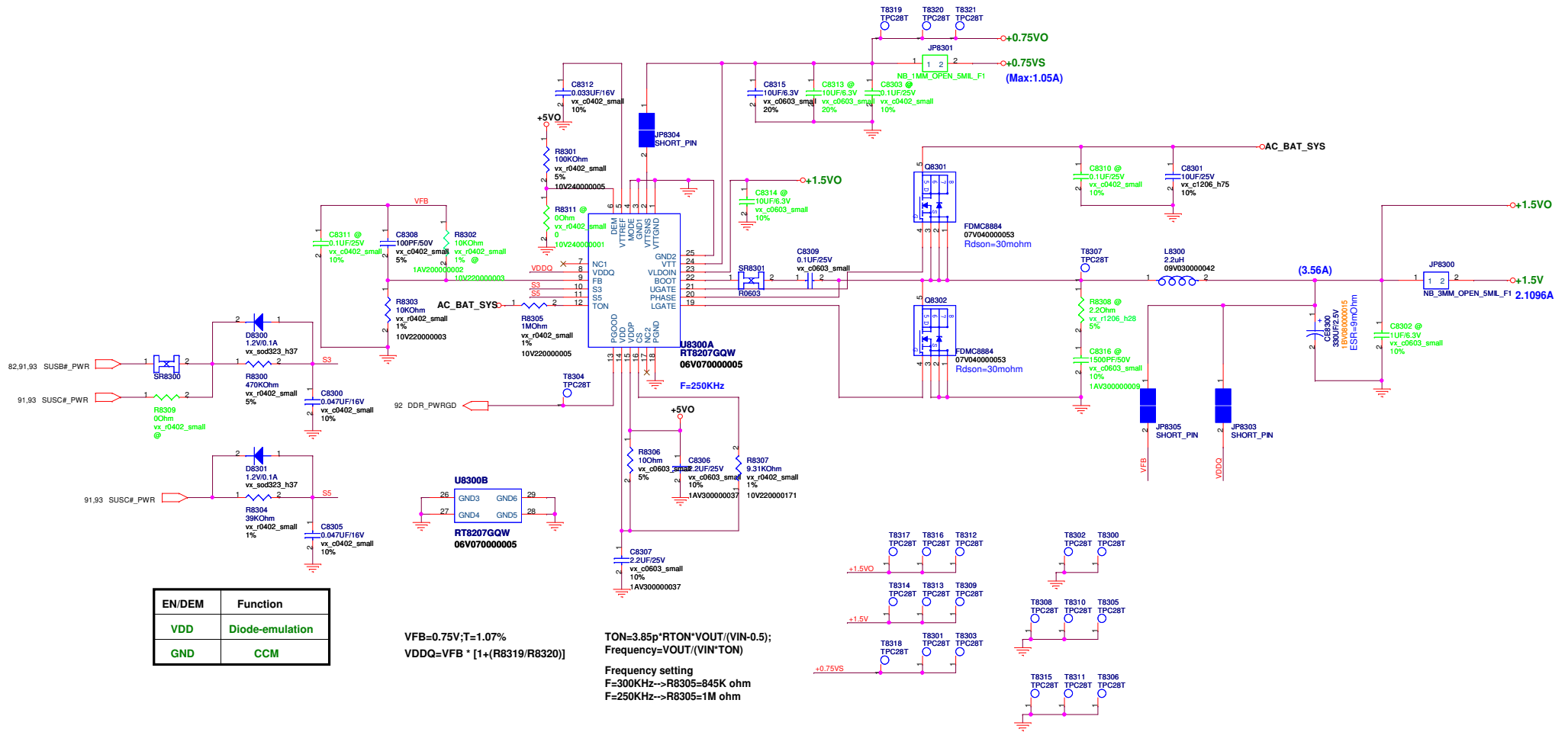
<Variant Name>

<b>PEGATRON</b> Title : <b>POWER_SYSTEM</b>	
Engineer: <b>Adams_Lin</b>	
Size	Project Name
Custom	<b>BIC50</b>
Date: <b>Tue, 03. Mar. 2011</b>	Sheet <b>81</b> of <b>77</b>



<Variant Name>

<b>PEGATRON</b>		Title : POWER_+VCCP_+1.8VS	
		Engineer: Adams_Lin	
Size	Project Name	BIC50	Rev 1.0
Custom			
Date: Tuesday, May 03, 2011		Sheet 82	of 77



EN/DEM	Function
VDD	Diode-emulation
GND	CCM

$VFB=0.75V; T=1.07\%$   
 $VDDQ=VFB * [1+(R8319/R8320)]$

$TON=3.85p \cdot RTON \cdot VOUT/(VIN-0.5);$   
 $Frequency=VOUT/(VIN \cdot TON)$

**Frequency setting**  
 $F=300KHz \rightarrow R8305=845K \text{ ohm}$   
 $F=250KHz \rightarrow R8305=1M \text{ ohm}$

~Variant Name~

<b>PEGATRON</b> Title : POWER_DDR & VTT		
Engineer: Adams_Lin		
Size	Project Name	Rev
Custom	BIC50	1.0
Date: Tuesday, May 03, 2011	Sheet 83	of 77

5

4

3

2

1

D

D

C

C

B

B

A

A

<Variant Name>

<b>PEGATRON</b>		Title : <b>POWER_N/A</b>	
		Engineer: <b>Adams_Lin</b>	
Size Custom	Project Name <b>BIC50</b>	Rev 1.0	
Date: <b>Tuesday, May 03, 2011</b>		Sheet	<b>84</b> of <b>77</b>

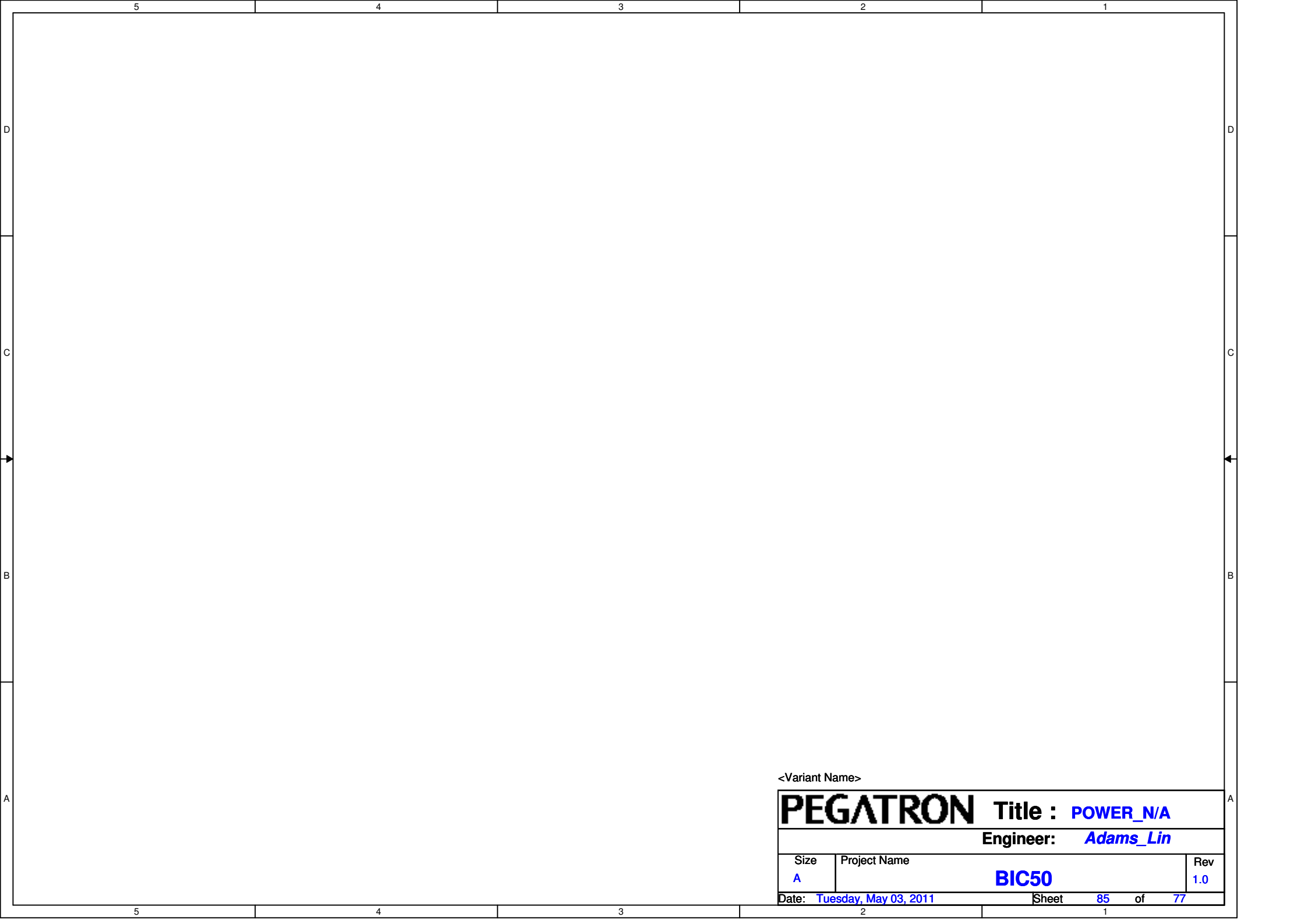
5

4

3

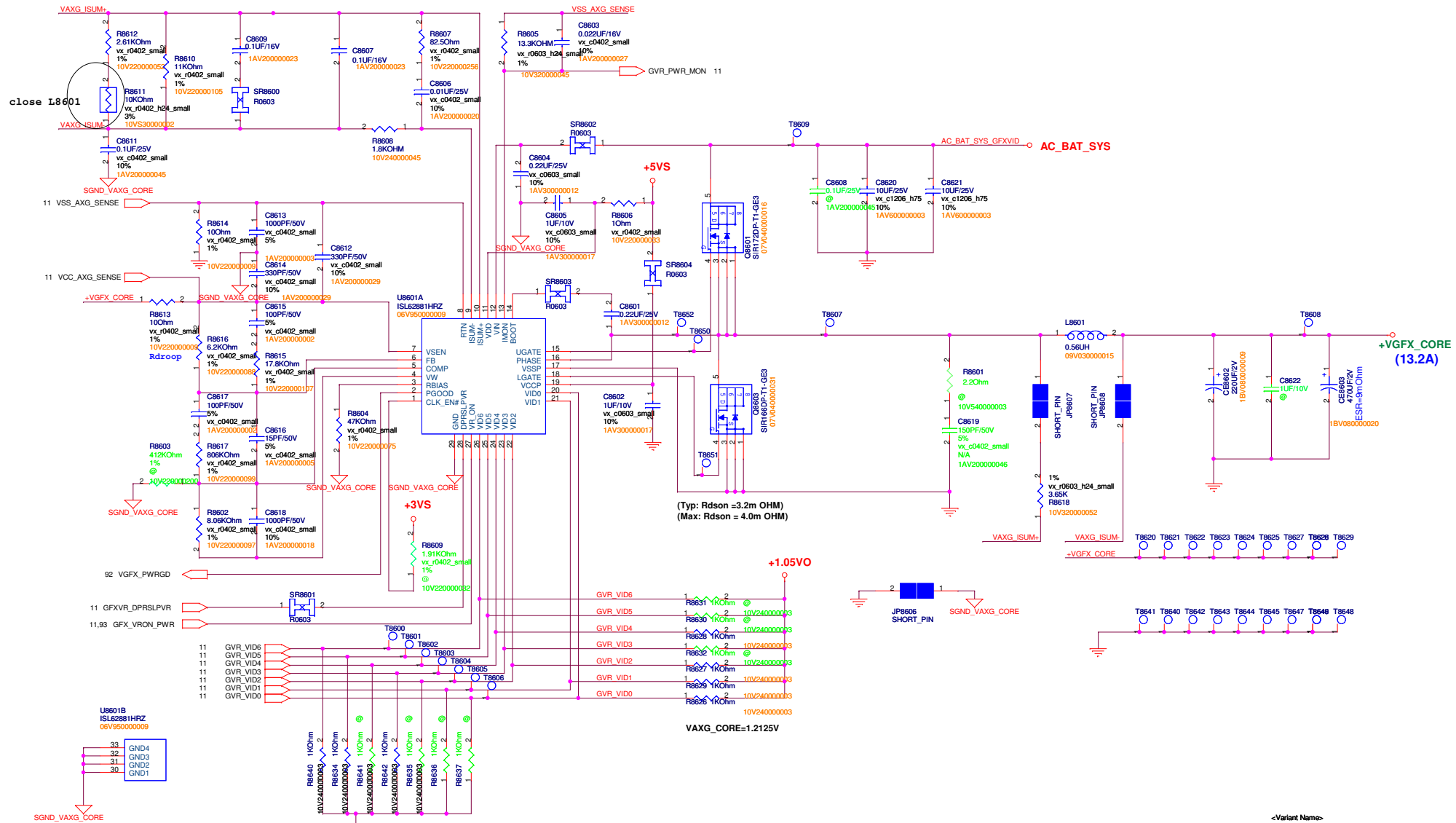
2

1



<Variant Name>

<b>PEGATRON</b> Title : <b>POWER_N/A</b>		
Engineer: <b>Adams_Lin</b>		
Size <b>A</b>	Project Name <b>BIC50</b>	Rev <b>1.0</b>
Date: <b>Tuesday, May 03, 2011</b>		Sheet <b>85</b> of <b>77</b>

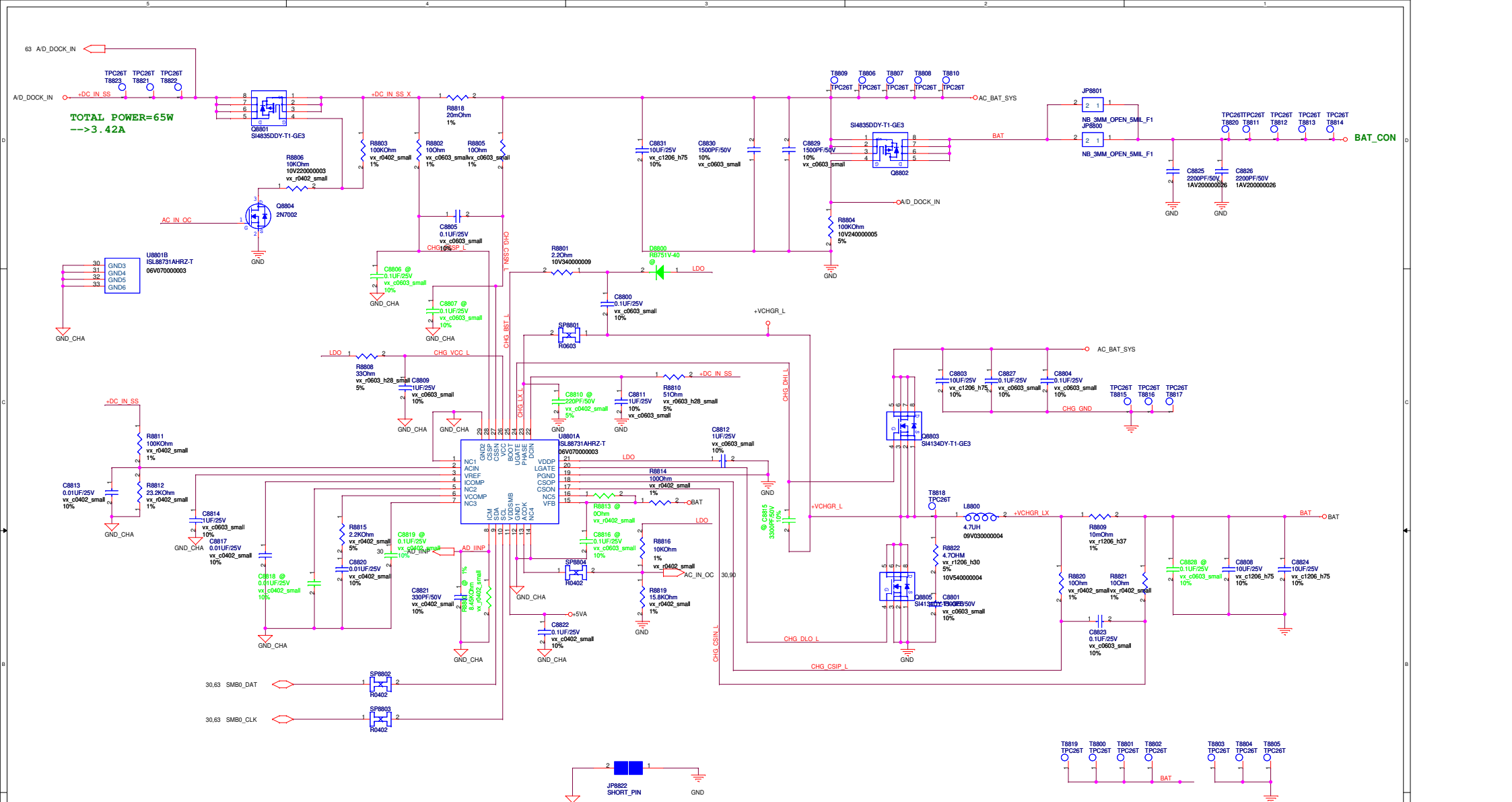




<Variant Name>

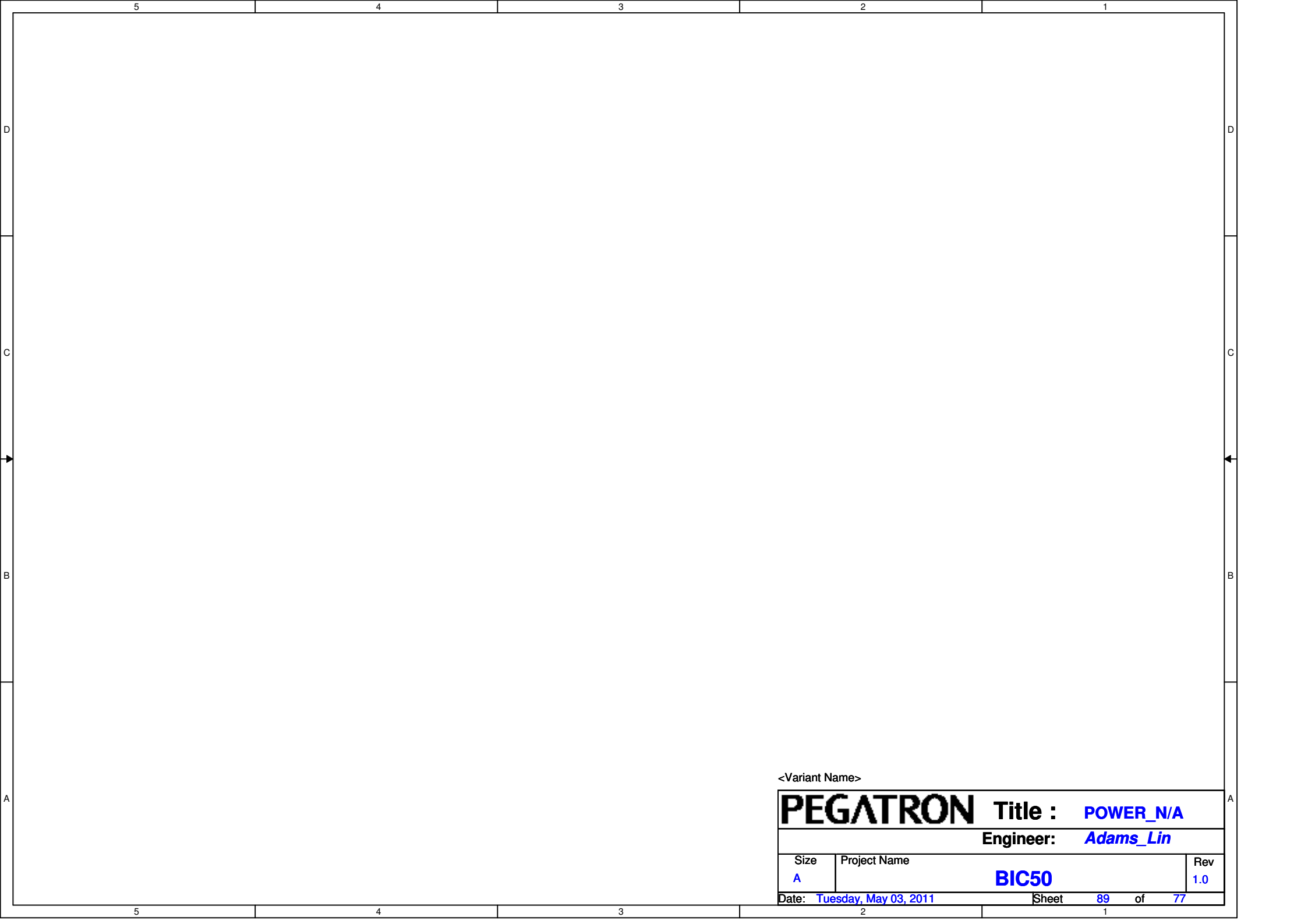
<b>PEGATRON</b>		Title :	<b>POWER *****</b>
		Engineer:	<b>Adams Lin</b>
Size	Project Name		Rev
Custom	<b>BICS50</b>		1.0
Date: <b>Tuesday, May 03, 2011</b>		Sheet	87 of 77





<Variant Name>

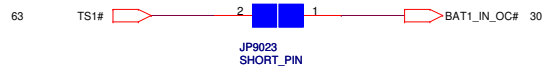
<b>PEGATRON Title POWER CHARGER</b>		
Engineer: Adams Lin		
Size C	Project Name BIC50	Rev 1.0
Date: Tuesday, May 03, 2011	Sheet 88	of 77



<Variant Name>

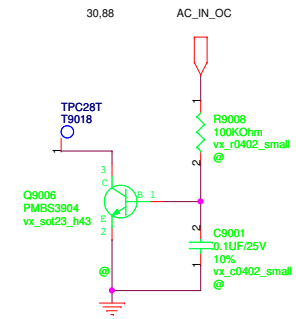
<b>PEGATRON</b>			<b>Title :</b>	<b>POWER_N/A</b>
			<b>Engineer:</b>	<b>Adams_Lin</b>
Size	Project Name			Rev
<b>A</b>	<b>BIC50</b>			<b>1.0</b>
Date: <b>Tuesday, May 03, 2011</b>			Sheet	<b>89</b> of <b>77</b>

# BATTERY IN DETECT



# ADAPTER IN DETECT

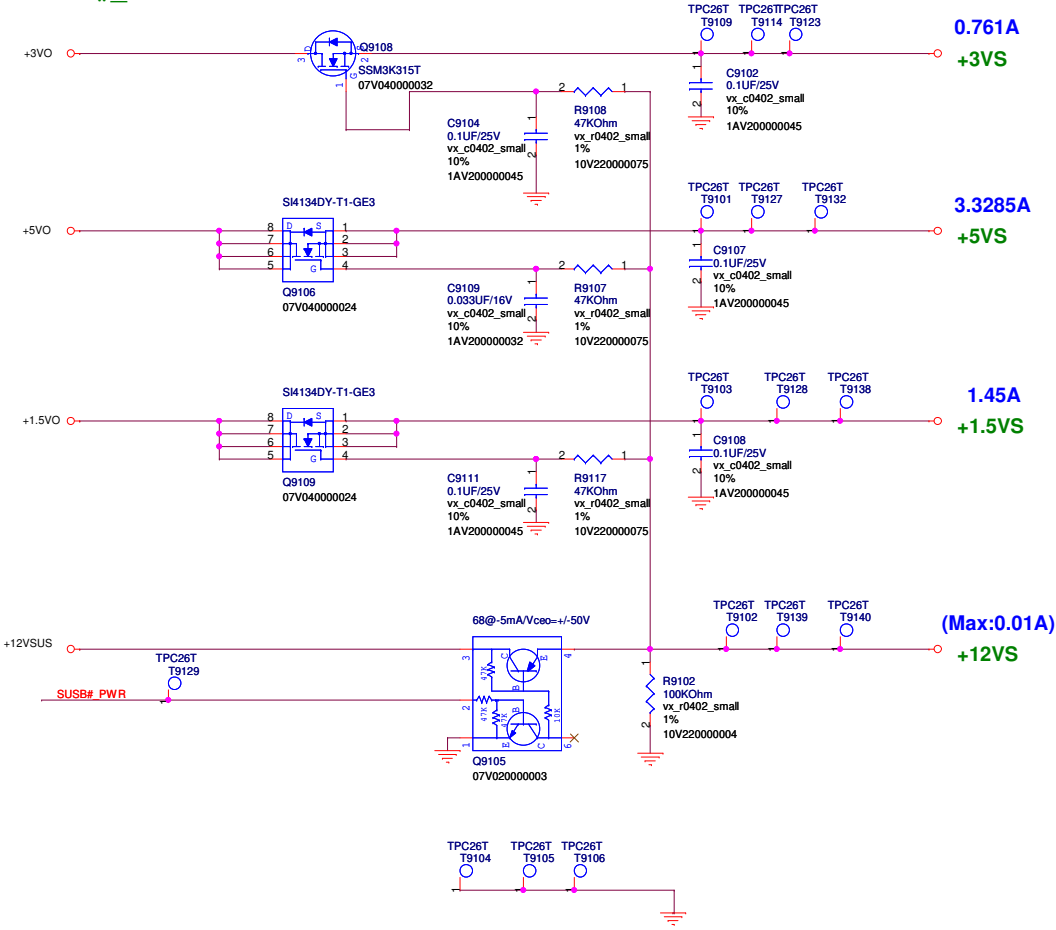
Use MAX17015 IC function to Cost down component



<Variant Name>

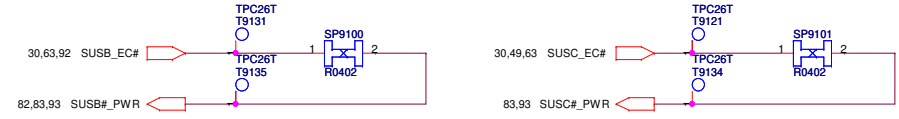
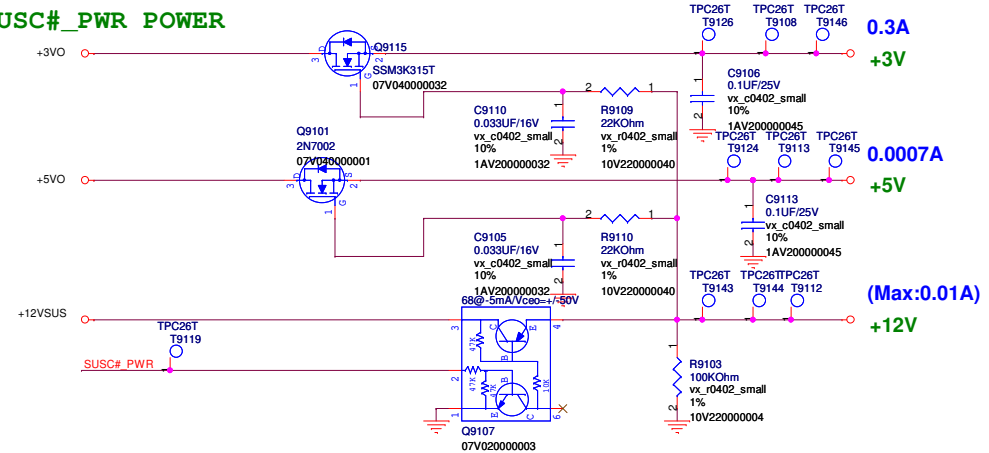
<b>PEGATRON</b> Title : <b>POWER_DETECT</b>		
Engineer: <b>Adams_Lin</b>		
Size	Project Name	Rev
Custom	<b>BIC50</b>	1.0
Date:	Tuesday, May 03, 2011	Sheet 90 of 77

### SUSB#\_PWR POWER



Ron = 41.5 mΩ (max) (θVGS = 4.5 V)  
 Ron = 27.6 mΩ (max) (θVGS = 10 V)

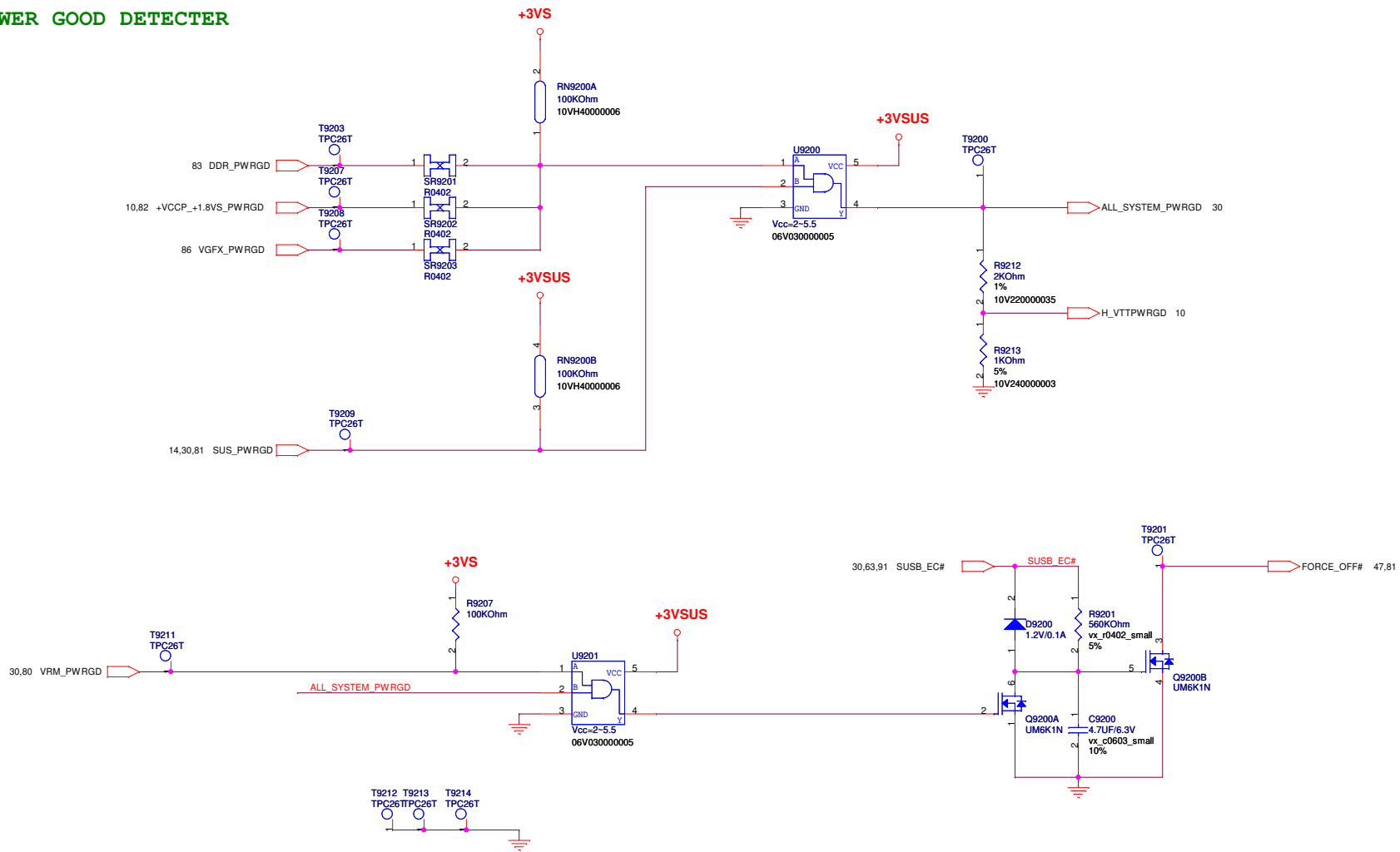
### SUSC#\_PWR POWER



<Variant Name>

<b>PEGATRON</b> Title : POWER_LOAD SWITCH			
Engineer: Adams_Lin			
Size	Project Name	Rev	
Custom	BIC50	1.0	
Date:	Tuesday, May 03, 2011	Sheet	91 of 77

# POWER GOOD DETECTOR



<Variant Name>

<b>PEGATRON</b> Title : <b>POWER_PROTECT</b>		
Engineer: <b>Adams_Lin</b>		
Size Custom	Project Name <b>BIC50</b>	Rev 1.0
Date: <b>Tuesday, May 03, 2011</b>	Sheet <b>92</b> of <b>77</b>	

AC\_BAT\_SYS ○ → AC\_BAT\_SYS 37,80,81,82,83,86,88  
 BAT\_CON ○ → BAT\_CON 63,88  
 BAT ○ → BAT 88

+5VA ○ → +5VA 30,42,49,66,81,88  
 +3VA ○ → +3VA 13,30,48,63,81

+5VO ○ → +5VO 81,82,83,91  
 +3VO ○ → +3VO 81,91  
 +1.8VO ○ → +1.8VO 82  
 +1.5VO ○ → +1.5VO 83,91  
 +1.05VO ○ → +1.05VO 80,82,86  
 +VGFX\_CORE\_O ○ → +VGFX\_CORE\_O

+0.75VO ○ → +0.75VO 83

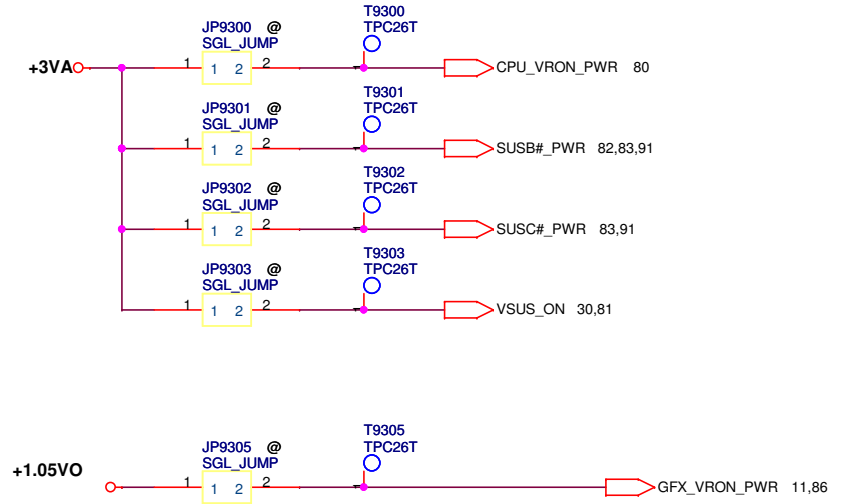
+12VS ○ → +12VS 38,39,91  
 +5VS ○ → +5VS 15,19,30,38,39,41,42,48,49,60,63,80,86,91  
 +3VS ○ → +3VS 10,13,14,15,16,17,18,19,21,22,24,30,33,37,38,39,41,47,49,60,63,65,80,86,91,92  
 +1.8VS ○ → +1.8VS 11,18,19,82  
 +1.5VS ○ → +1.5VS 10,11,24,55,63,91  
 +0.75VS ○ → +0.75VS 21,22,63,83

+VGFX\_CORE ○ → +VGFX\_CORE 11,86  
 +VCORE ○ → +VCORE 11,12,80

+12VSUS ○ → +12VSUS 33,37,41,50,55,60,81,91  
 +5VSUS ○ → +5VSUS 19,30,42,61,65,66,81  
 +3VSUS ○ → +3VSUS 10,13,14,15,16,17,18,19,30,33,37,41,50,55,60,81,92

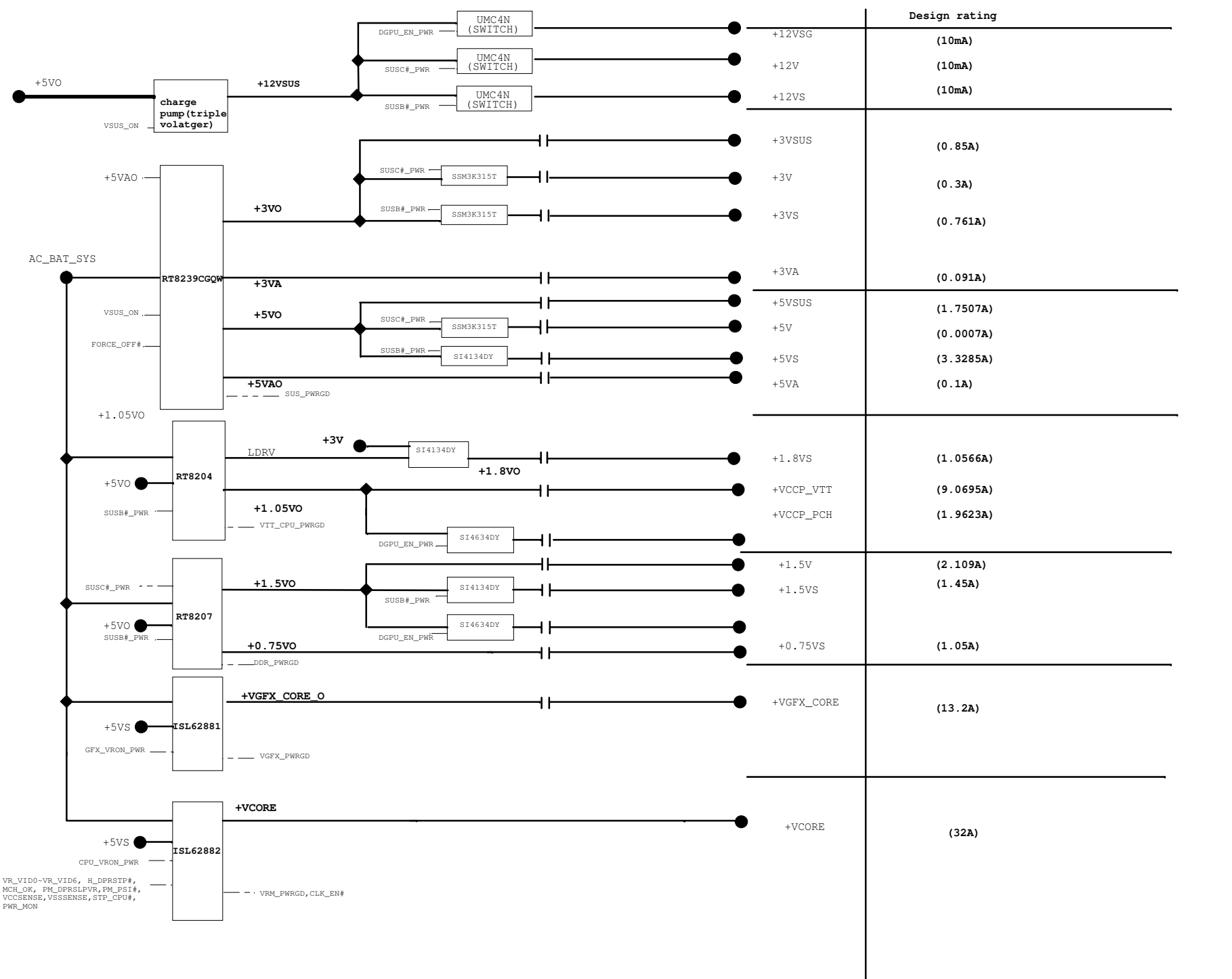
+12V ○ → +12V 91  
 +5V ○ → +5V 63,91  
 +3V ○ → +3V 37,50,63,65,82,91  
 +1.5V ○ → +1.5V 10,21,22,63,83

## FOR POWER TEST



<Variant Name>

<b>PEGATRON</b>		Title : <b>POWER_SIGNAL</b>	
		Engineer: <b>Adams_Lin</b>	
Size Custom	Project Name <b>BIC50</b>	Rev 1.0	
Date: <b>Tuesday, May 03, 2011</b>		Sheet	93 of 77



modify notice

Item	Date	Description	Item	Date	Description
SR-1	0120-11	P61, A04IO. change USB power switch circuit	SR-71	0128-11	P15. Add C1510 (22pF) for Clock fine-tune
SR-2	0120-11	Del P67, P68. Add P33, P34 for LAN	SR-72	0128-11	P33. change R3325, R3331 (4.7k ohm)
SR-3	0120-11	P48. change KB CON4801	SR-73	0128-11	P39. Un-mount R3907 (HDMI)
SR-4	0120-11	P34. change RJ45 CON3401	SR-74	0128-11	Change connector by list of 0128-11
SR-5	0120-11	P63. change BATT. con. circuit	SR-75	0129-11	Change HDD CON6001(1224-001N000)
SR-6	0120-11	P65, A02 change PWR LED CON6503 circuit	SR-76	0129-11	P97 (A02). Change Hotbar 6 Pad (PWR_U01)
SR-7	0120-11	P60. change HDD CON6001	SR-77	0129-11	P41~P50 Change VP part
SR-8	0121-11	P44, P45 Del Entry audio circuit (Full)	SR-78	0129-11	P55. Add Q5510, R5515 for BT PCI-E wake up event
SR-9	0121-11	P50. Del Entry SD socket circuit	SR-79	0130-11	P50. change footprint for U5001 Card reader controller
SR-10	0121-11	P77. Del B channel VRAM * 4 circuit	SR-80	0130-11	P66. change CPU*4, GPU*2, System screw hole*10
SR-11	0121-11	P46. Add EC GPIO35 DGPU_PWR_EN for Power	SR-81	0130-11	P46. change RN4601C (RN9202C)
SR-12	0121-11	P34, P35. Modify LAN AR8158 (Full)	SR-82	0130-11	P66. change F screw hole *2
SR-13	0123-11	P63. Change DC con. as VP part	SR-83	0130-11	P46. change SHORT PIN (R4601,R4602)
SR-14	0123-11	P60. Change HDD CON6001	SR-84	0130-11	P46, P65. change EC GPIO21 (PWR_AMBER_LED#) for PWR Brd.
SR-15	0123-11	P7~P37 Change VP part	SR-85	0130-11	Modify Sub board screw hole
SR-16	0124-11	P41 Del Entry speaker R4117~R4120	SR-86	0130-11	P34. Change RJ45 CON3401 1223-00BT000
SR-17	0124-11	P38~P39 Change VP part	SR-87	0131-11	P74. Change Q7401B(Q9203B)
SR-18	0124-11	P66 Remove LED circuit	SR-88	0131-11	P96, P99. Del Screw hole ODD_H02, change IOH3
SR-19	0124-11	P48. Reverse KB CON4801	SR-89	0131-11	P97. Change Power Board LED PWR_LED01
SR-20	0124-11	P71. Remove GPU Channel B dummy NET	SR-90	0131-11	P60. Change 15" ODD CON6505 as VP
SR-21	0124-11	P16, P61. Remove USB_9(HDMI)	SR-91	0131-11	P96~P99. Copy from AAB70 (sub board)
SR-22	0124-11	P48. Remove TP button circuit			
SR-23	0124-11	P13. Remove Entry AZ R1318, R1346, R1347, R1348, R1349	R1.2-1		P18 Add Bead and cap for CRT noise issue
SR-24	0124-11	P50. Modify CON5002 SD socket circuit	R1.2-2		P30 PWR_SW#_M 10kohm P/U to +3VA_EC
SR-25	0124-11	P48. Change KB CON4801 PIN definition	R1.2-3		P30 PWR_BLUE_LED# P/U to +5VSUS; BAT_ORG_LED# P/U to +5VA; CHG_LED_BLUE# P/U to +5VA to fix LED leakage issue
SR-26	0124-11	P16, P61. change USB power switch circuit	R1.2-4		P30 Reverse Q4602 for circuit design error
SR-27	0124-11	P41, P46. ALC271-SPKR_EC_ICH_Colay	R1.2-5		P37 add LCD_BACKOFF# for LCD on/off control by EC
SR-28	0124-11	P46, P65. Modify LED circuit and EC GPIO definition	R1.2-6		P41&P42&99 modify Int. MIC design from mono to stereo
SR-29	0125-11	P33 Remove LAN LED circuit	R1.2-7		P41 Reserve load switch to control PVDD on/off
SR-30	0125-11	P61 Modify D6101, RN6101, RN6105, RN6106	R1.2-8		P42 R3916 P/U to +5VSUS
SR-31	0125-11	P33 Change R3311 as VP	R1.2-9		P47 connect to EC_RST# for power protect
SR-32	0125-11	P33 Change U3301 to AR8158 and delete SM BUS	R1.2-10		P47,P49 Add Palm rest thermal circuit to follow thermal design spec
SR-33	0125-11	P34 Modify LAN ESD circuit	R1.2-11		P50 CON5002 pin.12 connect to GND to fix SD card can't be detected issue
SR-34	0125-11	P61. Modify Q6101	R1.2-12		P55 Reserve load switch to control +1.5VS_WLAN on/off
SR-35	0125-11	P65. Modify Q6501	R1.2-13		P60 Reserve connector for HDD connect by cable
SR-36	0125-11	P38, P46. Del F3801, C3811 Add CRT IN Detect	R1.2-14		P61 change Audio BD connector to 24 pin & reserve one more power switch for USB power test
SR-37	0125-11	P63. Reverse J6301	R1.2-15		P63 Change J6301 to 1217-00WC000 to fix SMT issue
SR-38	0125-11	P61, P46. change USB power switch and GPIO	R1.2-16		P66 H6546 floating by EMI request
SR-39	0125-11	P46,P66. change LED power and Net name	R1.2-17		P66 delete screw hole H6545
SR-40	0125-11	P34. Modify Transformer circuit	R1.2-18		P98 TP_H1 & TP_H2 change P/N by ME request
SR-41	0125-11	P33. Modify H/W strap setting	R1.2-19		P98 TP_SW1 & TP_SW2 change to 1209-00VF000 by ME request
SR-42	0125-11	P37. Modify LVDS PIN definition	R1.2-20		P98 TP_H1 & TP_H2 change P/N by ME request
SR-43	0125-11	P42. Modify De-Pop circuit	R1.2-21		P61 L6105 change to 67 ohm common choke to fix USB eye-diagram fail issue
SR-44	0125-11	P41. Modify Audio Pin 14, 15, 27~31	R1.2-22		P48 Add cap for K/B signal by EMI request
SR-45	0126-11	P34. Modify Transformer circuit	R1.2-23		P48 Add C3013 by EMI request
SR-46	0126-11	P16. GPIO54 DGPU_PWR_EN	R1.2-24		P97 hotbar pin define swap to meet cable define
SR-47	0126-11	U1301, U7001 keypad no; U4602, F6302 Modify for BOM	R1.2-25		P33 unmount R3306, mount R3308 for LAN OPT mode
SR-48	0126-11	P34. Modify Transformer circuit	R1.2-26		P33 L3317 change to 1500ohm Bead by EMI request
SR-49	0126-11	P63, P60, P17, P48. Add 15" circuit BATT, ODD, Keyboard	R1.2-27		P38 L3801,L3802,L3803 change to 0.056uH inductor for EMI & EA test
SR-50	0126-11	P13, P60 Rename SATA 0 to SATA 1	R1.2-28		P65 unmount R6507&Q6501 and delet PWR_SW BD LED circuit
SR-51	0126-11	P63. Reverse DC-IN J6301 PIN1 as GND	R2.0-1		P42 change OP_SD# to +5VA power rail to prevent DC mode has noise when shutdown (follow eih30)
SR-52	0126-11	P48. Reverse KB CON4801	R2.0-2		P30 remove EC xtal, EC clock control by EC itself.
SR-53	0126-11	DGPU Sync with EIH31	R2.0-3		P49 change R4903 to 4.22Kohm to set thermistor operating temp at 89'C (request by thermal RD)
SR-54	0126-11	P.76. T7, M7 Setting	R2.0-4		P66 change H6541,H6538,H6553,H6552,H6547,H6544 to NPTH hole for factory ICT test purpose
SR-55	0126-11	Modify as OPT display output	R2.0-5		P80 Add CE8008 to fix electrical noise over 15msones issue
SR-56	0127-11	P.76. Cancel T7, M7 Setting			
SR-57	0127-11	P.46, P50 Modify single net			
SR-58	0127-11	P.42 Change R4205, R4206 = 51 ohm			
SR-59	0127-11	P.41 DEL C4109, C4112			
SR-60	0127-11	P.14 R1403, R1404 option N/A			
SR-61	0127-11	P.14 R1443, R1444, RN1402, R1424, R1426, R1427, R1428 option N/A; R1429 option /HDMI_HPD_PCH			
SR-62	0127-11	P71, P74. R7101, R7103, R7435, R7437 option @			
SR-63	0127-11	P74. Del R7433, R7434, GPIO Test Pad			
SR-64	0128-11	P34. U3403.4 RXN			
SR-65	0128-11	P66. change R6603.1 (+5VA), LED6602, LED6603			
SR-66	0128-11	P65. change R6508.1 (PWRLED_ON#), CON6503.6 (+5VSUS)			
SR-67	0128-11	P97. Modify A04 Pwr Board			
SR-68	0128-11	P55. Un-mount Q5505, R5510			
SR-69	0128-11	P66. Modify Screw Hole (Sync with AAB70)			
SR-70	0128-11	P63. Modify Battery CON6302, D6302 signal name			

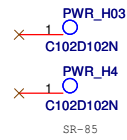
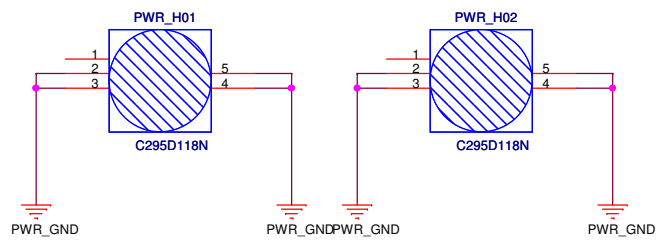
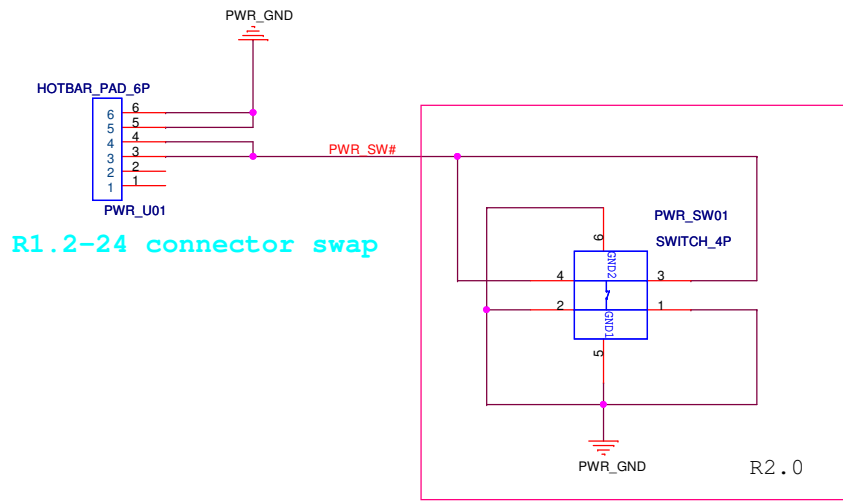
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Engineer: \_\_\_\_\_

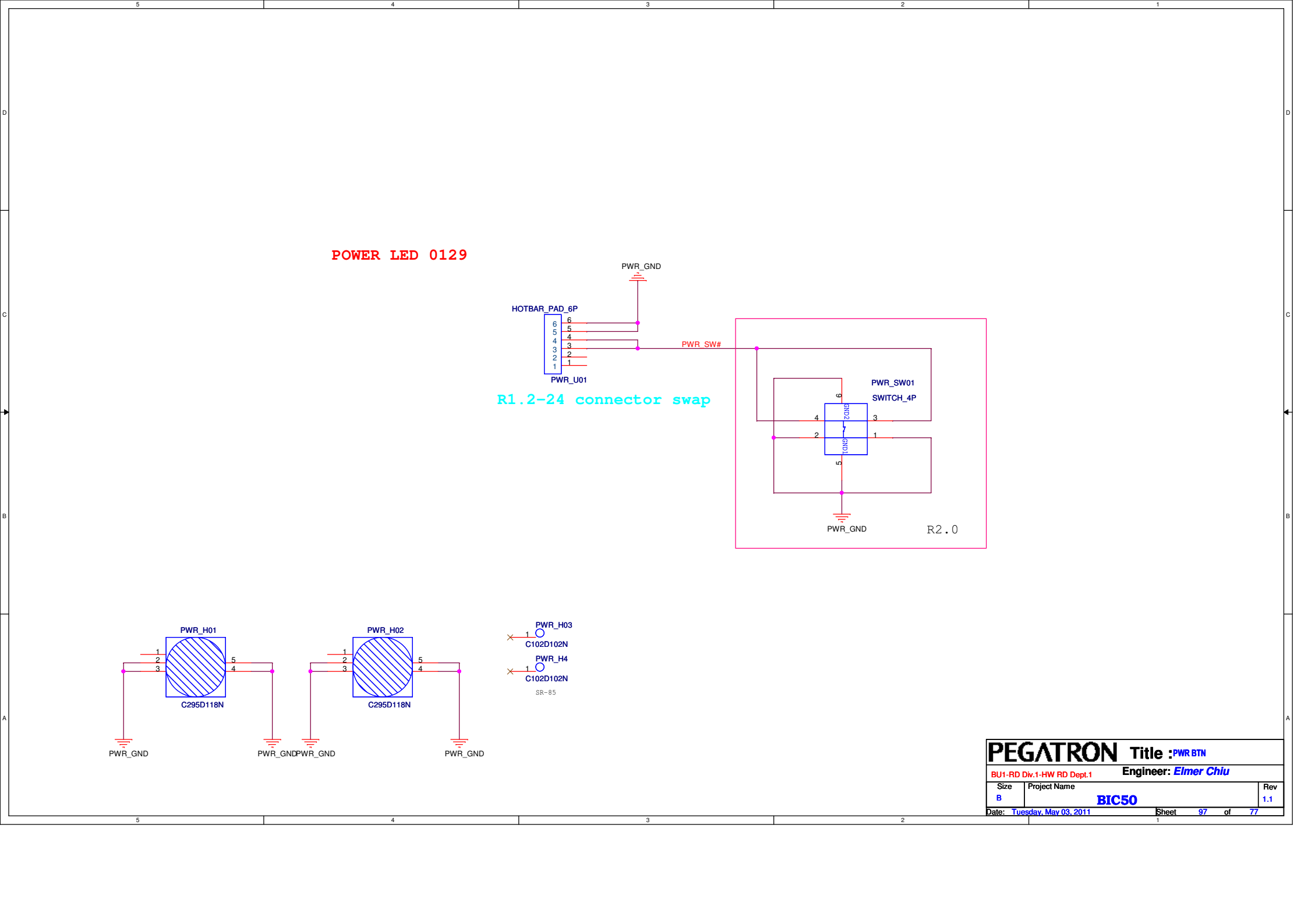
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C		1.0
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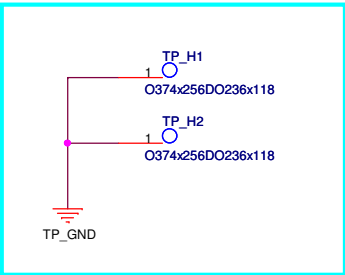


**POWER LED 0129**

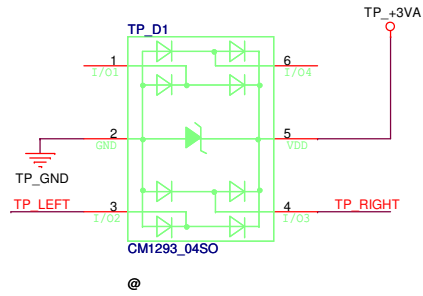


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BU1-RD Div.1-HW RD Dept.1		1.1
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B	<b>BIC50</b>	
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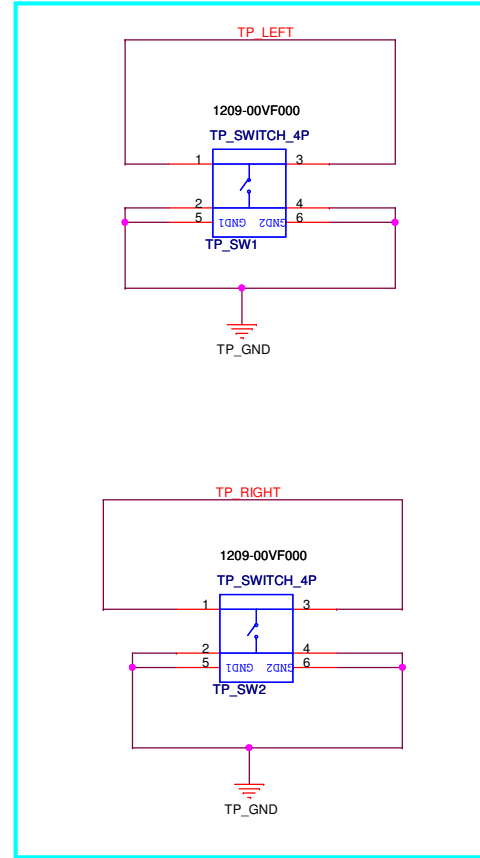
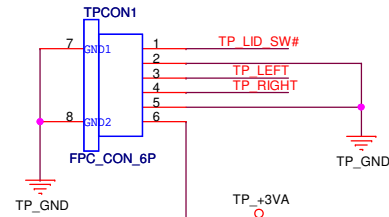
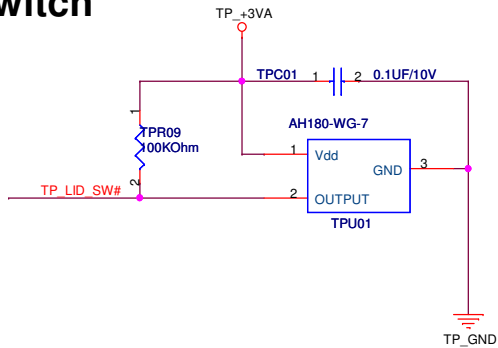




R1.2-18



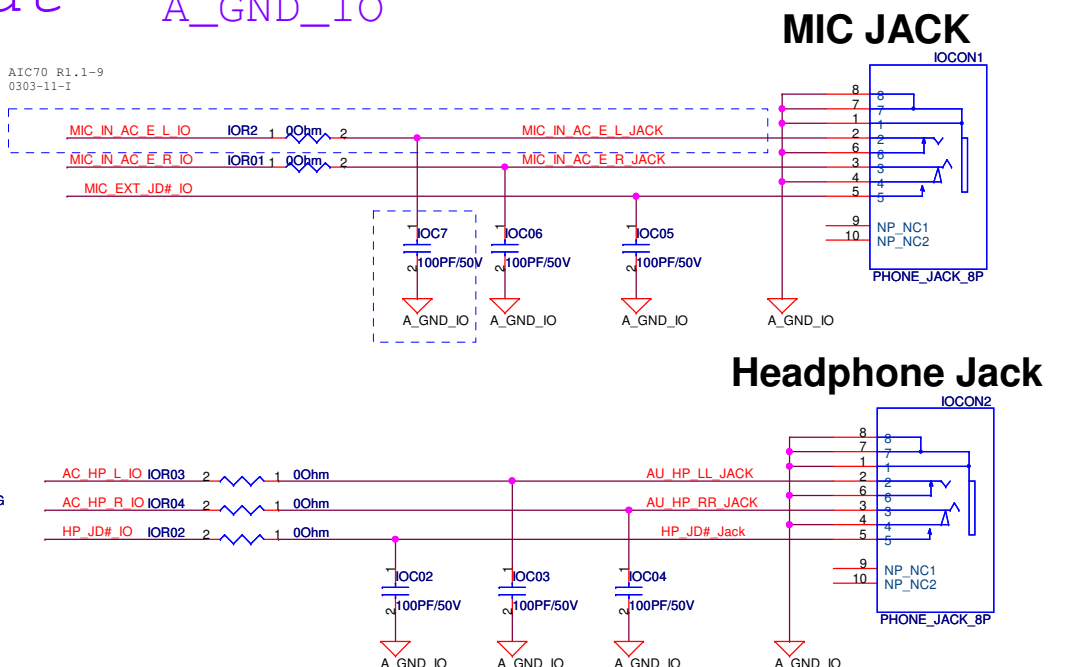
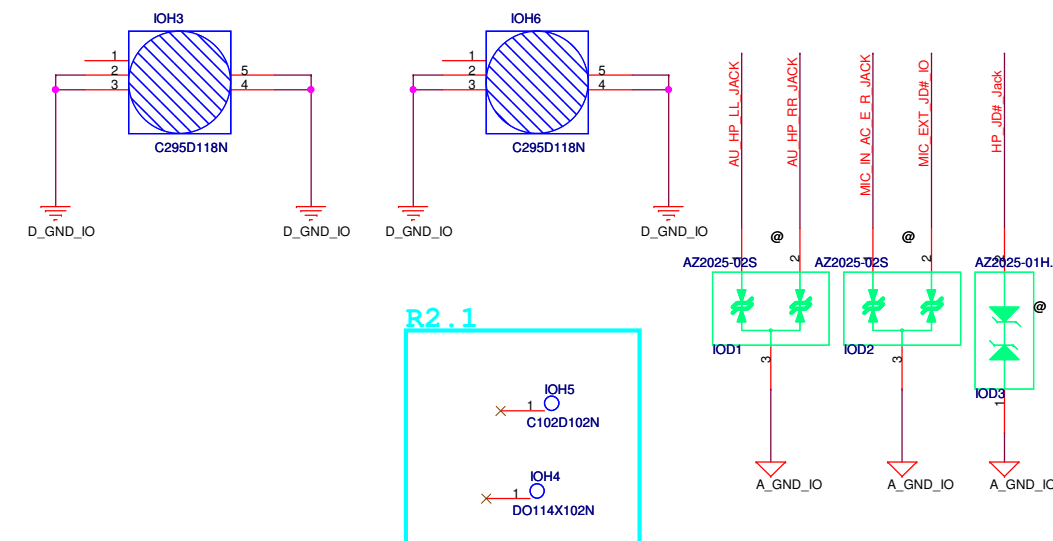
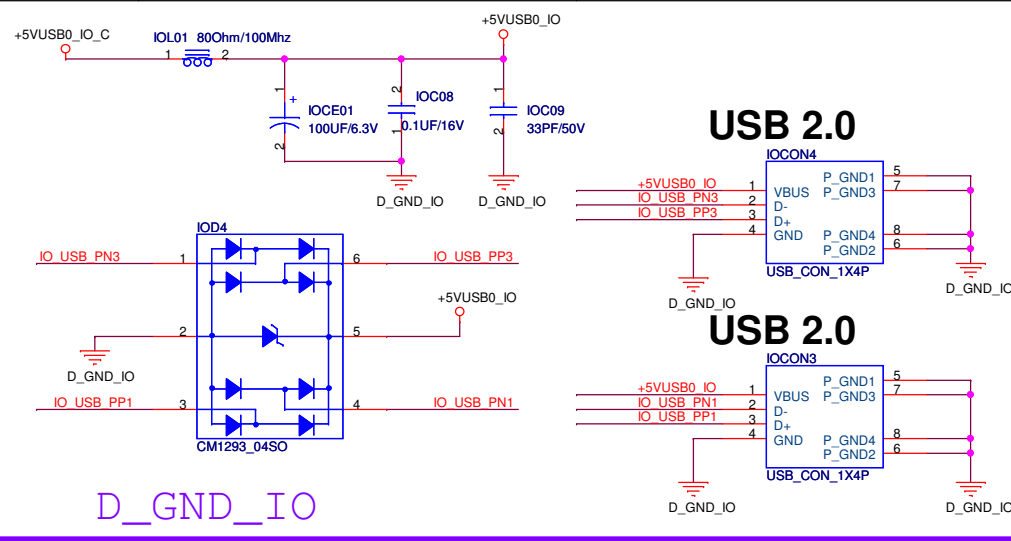
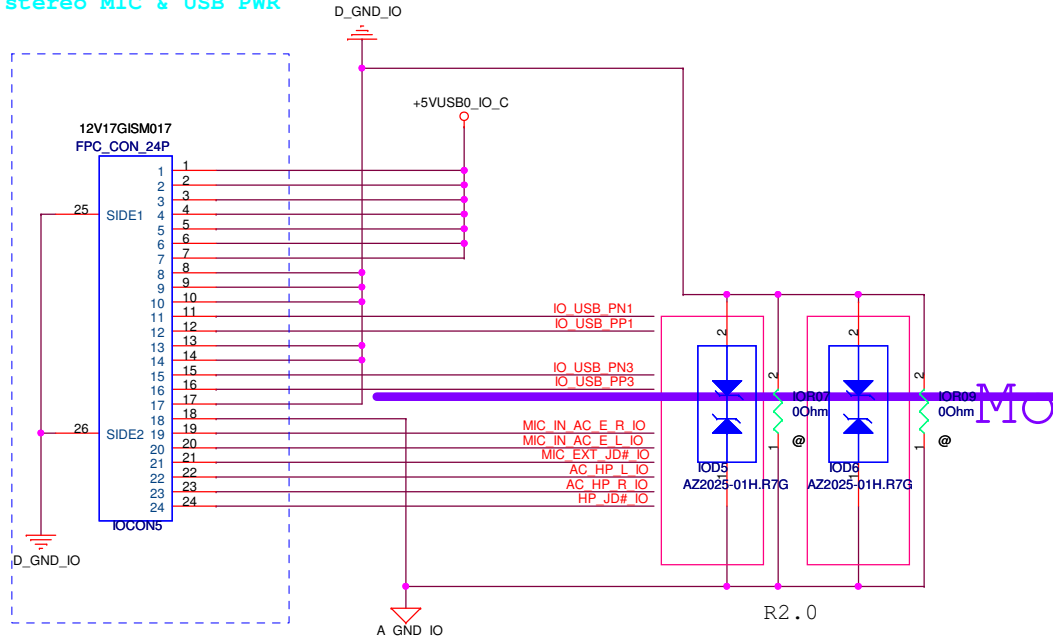
### LID Switch



R1.2-19

<b>PEGATRON</b> Title :TP_M	
BG1-HW RD Div.2-NB RD Dept.5 Engineer: <i>Elmer Chiu</i>	
Size B	Project Name <b>BIC50</b>
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**R1.2-6**  
**Change Connector for**  
**stereo MIC & USB PWR**



<b>PEGATRON</b> Title : 10		
BG1-NB1-HW-NB5		Engineer: <b>Elmer Chiu</b>
Size B	Project Name <b>BIC50</b>	Rev 1.0
Date: <b>Wednesday, May 11, 2011</b>		Sheet <b>99</b> of <b>77</b>