Microcontroller Development System

# In System Programming for 800 Series




2012. 08. 29



ABOV Semiconductor MDS Team

# 1. Getting Started / ISP Installation

The In-System Programming (ISP) is performed without removing the microcontroller from the system. The In-System Programming (ISP) facility consists of a series of internal hardware resources coupled with internal firmware through the serial port. The In-System Programming (ISP) facility has made in-circuit programming in an embedded application possible with a minimum of additional expense in components and circuit board area.

The following section details the procedure for accomplishing the installation procedure.

1. Power off a target system.

2. Configure a target system as ISP mode.
   - Refer to chapter3. Hardware Conditions to enter the ISP mode at page3.

3. Attach a ISP B/D into a target system.

4. Connect the serial(RS-232C) cable between a ISP board and available serial port of your PC.

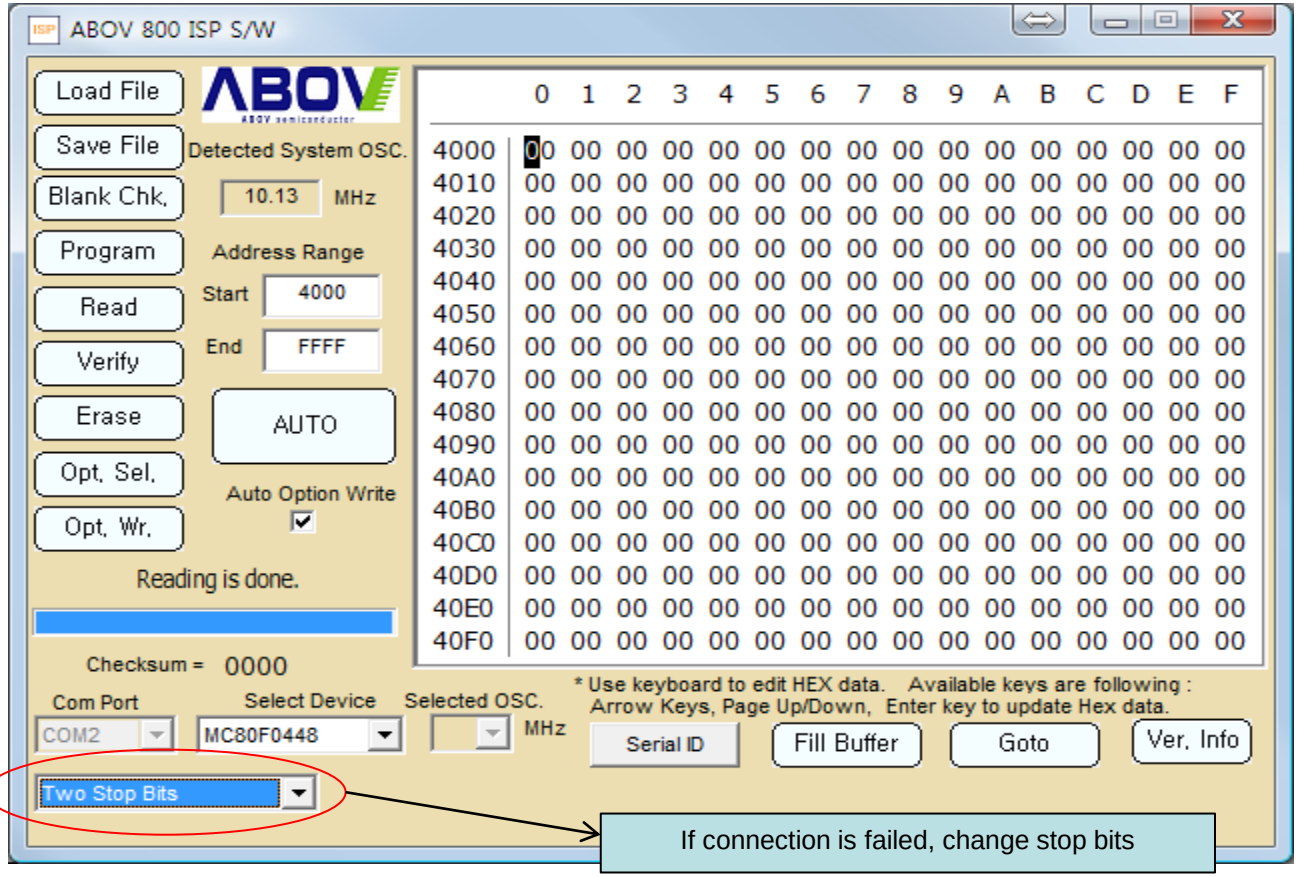
5. Run the ABOV ISP software.
   - Down load the ISP S/W from www.abov.co.kr.
   - Unzip the download file and run ISP_800.exe

6. Select a COM port and a device in the ISP S/W.

7. Power on a target system.

8. Execute ISP command such as read, program, auto... by pressing buttons on the ISP S/W.

# 2. Basic ISP S/W Information

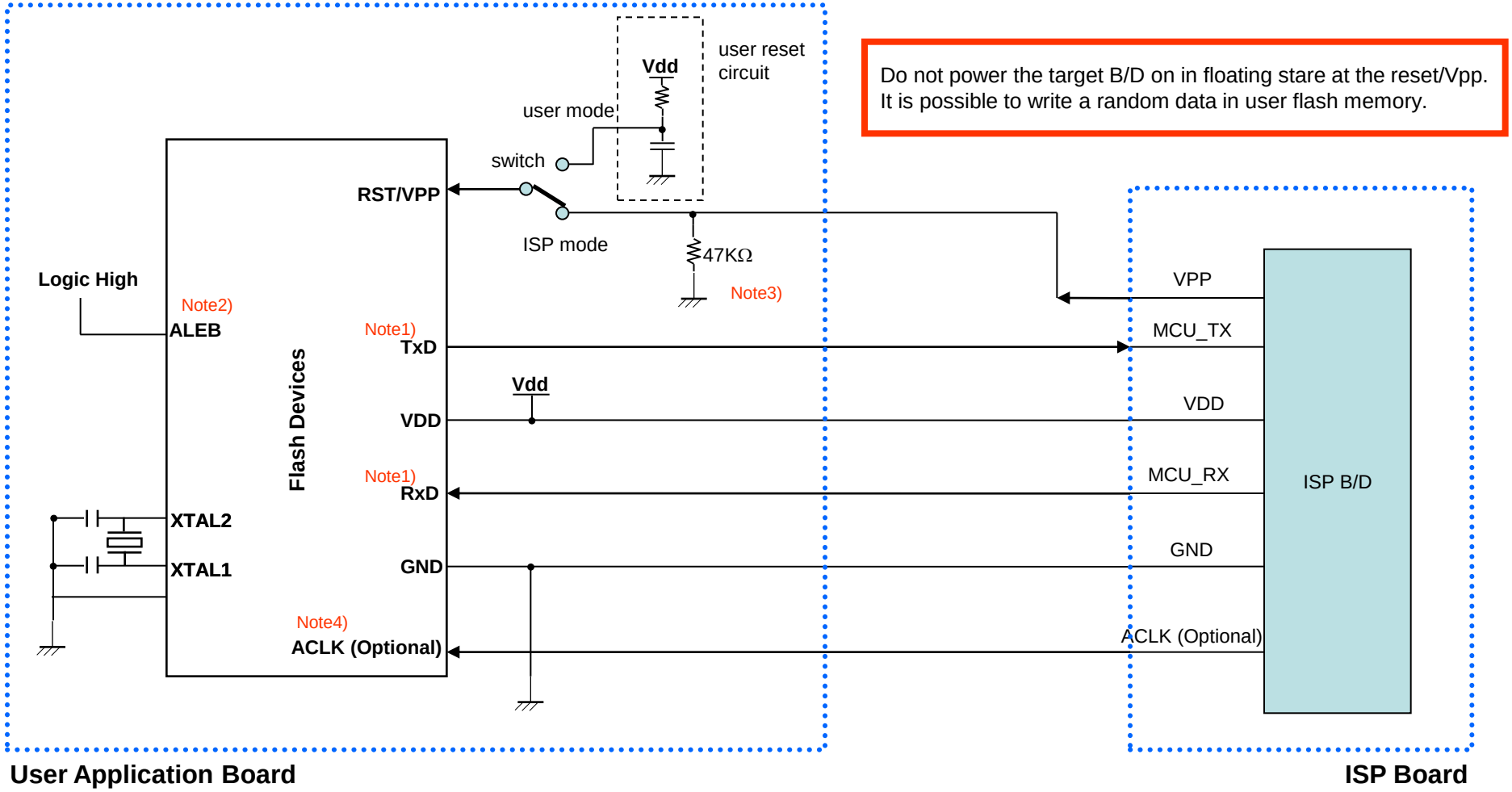



| | |
|---|---|
| Com Port | Select a serial port. |
| Select Device | Select a target MCU. User can select mode between auto baud rate and ACK. For example, MC80F0324 support both mode. Select MC80F0324 for auto baud and MC80F0324_ACK for ACK mode. |
| Selected OSC. | Specify your target oscillator value with discarding below point in ACK mode only. |

| | |
|---|---|
| Load File | Load the data from the selected file storage into the memory buffer. |
| Save File | Save the current data in your memory buffer to a disk storage by using the Motorola HEX format. |
| Blank Check | Verify whether or not a device is in an erased or un-programmed state. |
| Program | This button enables you to place new data from the memory buffer into the target device. |
| Read | Read the data in the target MCU into the buffer for examination. The checksum will be displayed on the checksum box. |
| Verify | Assures that data in the device matches data in the memory buffer. If your device is secured, a verification error is detected. |
| Option Write | Configure target MCU. |
| Erase | Erase the data in your target MCU before programming it. |
| Detected System OSC. | Display user system clock which is detected in Auto baud rate mode. |
| Auto | Following sequence is performed ; 1.Erase 2.Program 3.Verify 4.Option Write |
| Fill Buffer | Fill the selected area with a user specified data. |
| Goto | Display the selected page. |

**Note 1.** MCU configuration value is erased after erase operation. It must be configured to match with user target board. Otherwise, it is failed to enter ISP mode, or its operation is not desirable.
**Note 2.** For MC80F0204/ MC80F0316 devices, if the user selected OSC. configuration is not matched with user target board, the ISP operation is also failed. Careful attention is needed during configuring OSC. type.

# 3. Hardware Conditions to enter the ISP mode

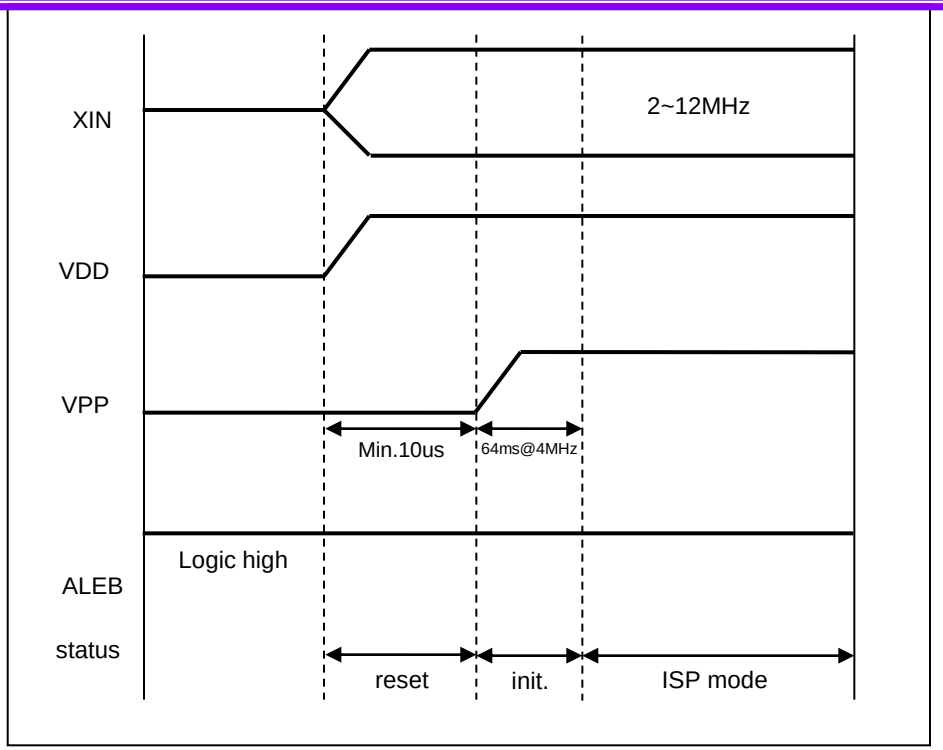



**Note1)** If other signals affect UART communication in ISP mode, disconnect these pins by using jumper or switch.
**Note2)** if ALEB is sharing with other function, toggle the port between ISP and user mode.
**Note3)** The pull down resister is optional. If user set to ISP Mode without connection ISP B/D, the Vpp/Reset Port is in floating state. The pull down resistor is for blocking this undefined state. Do not power on a application B/D in ISP mode without connecting a ISP board
**Note4)** Refer to explaining the auto baud rate and ACK mode at page5.

# 4. Sequence to enter ISP mode/user mode.

* Sequence to enter ISP mode from user mode.
1) Power off a target system.
2) Configure a target system as ISP mode.
3) Attach a ISP B/D into a target system.
4) Run the ISP S/W.
5) Select the target device.
6) Power on a target system.

*Sequence to enter user mode from ISP mode.
1) Close the ISP S/W.
2) Power off a target system
3) Configure a target system as user mode.
4) Detach a ISP B/D from a target system.
5) Power on




Timing Diagram to enter the ISP mode

**For MC80F0104, MC80F0204, MC80F0304, MC80F0308, MC80F0316, MC80F7708**
**Important!!!**

**If POR and R35 are enabled, Vdd and Vpp should be turned on simultaneously to enter ISP mode.**
**Normal sequence above can not enter ISP mode when POR and R35 options are enabled.**
**Please follow below sequence instead of normal one.**

1) Power off a target system.
2) Configure a target system as ISP mode.
3) Attach a ISP B/D into a target system.
4) Run the ISP S/W
5) Select target MCU - It makes condition to make Vpp to turn on when Vdd is turned on.
6) Power on a target system. : At this point, ISP mode is entered because the Vdd and Vpp are turned on **simultaneously.**

*** This function is applied in ISP S/W ver.1.92 release at May 4th 2006.**

# 5. Auto Baud Rate Mode and ACK mode

* Auto Baud Rate Mode

The ISP S/W detects user system clock and MCU configure a baud rate automatically. Do not need to connect the ACK pin of target MCU to ISP B/D.

*ACK mode

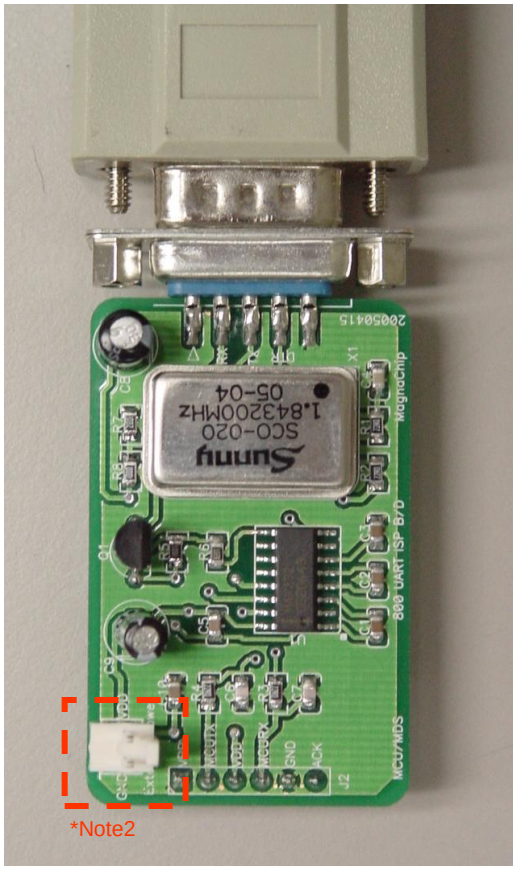
The ISP S/W can not detect user system clock. Users have to enter a user system clock. This mode is only used when failed to detect user system clock automatically. Need to connect the ACK pin to ISP B/D.

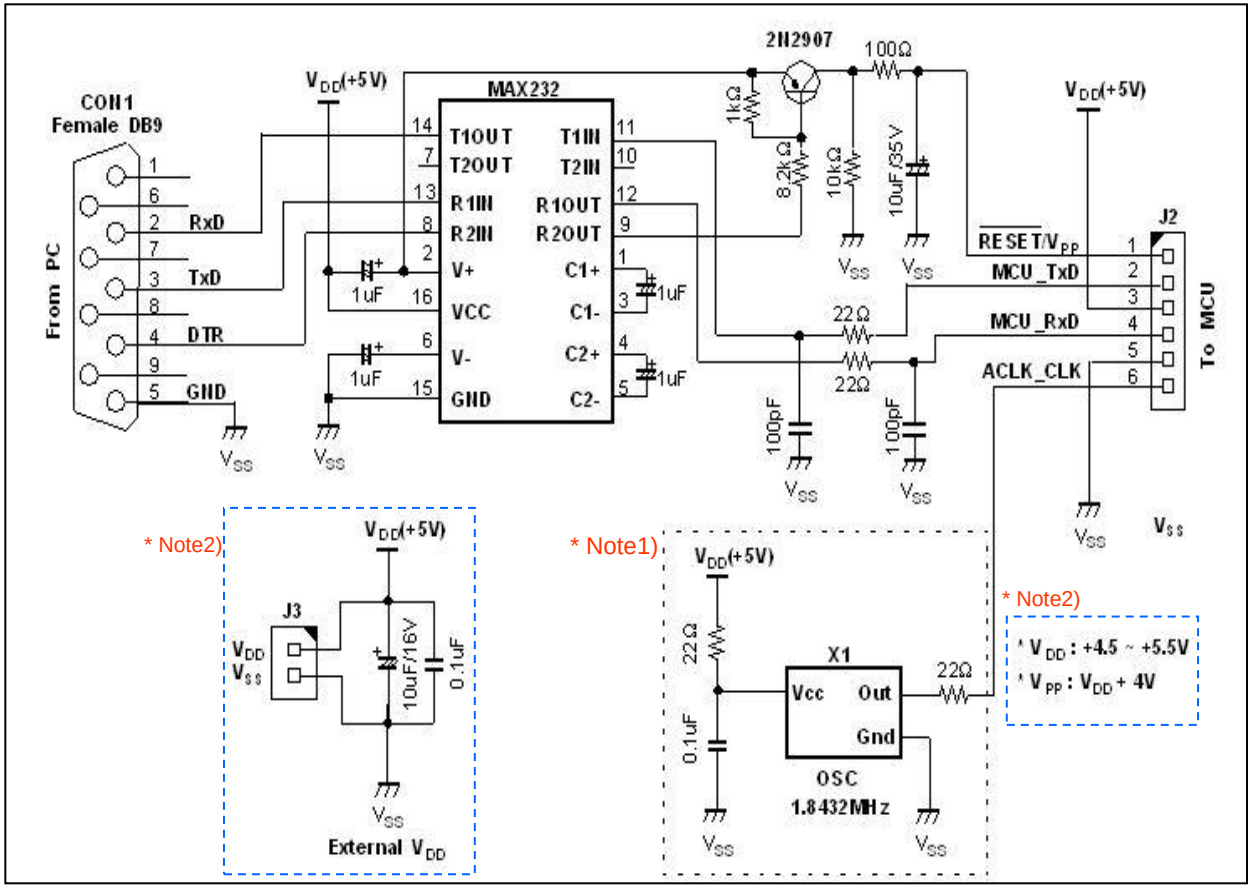
| Devices \ Mode | Auto Baud Rate | ACK. mode |
|---|---|---|
| MC80F0104<br>MC80F0204<br>MC80F0304/08/16<br>MC80F7708<br>MC80F5132 | × | o |
| MC80F0208/16/24 | o | o |
| MC80F0424/32/48 | o | o |
| MC80F7108<br>MC80F7208<br>MC80F7308<br>MC80F7408 | o | × |

**Detected MCU operating frequency in Auto Baud Rate Mode**

| Reference Frequency (MHz) | Available Frequency (MHz) | 57600 bps | 19200 bps |
|---|---|---|---|
| 1.8432 | 1.79~1.89 | × | O |
| 1.9968 | 1.94~2.05 | × | O |
| 3.0720 | 2.98~3.16 | × | O |
| 3.5328 | 3.43~3.63 | × | O |
| 3.6864 | 3.58~3.79 | O | × |
| 3.9168 | 3.80~4.03 | O | × |
| 4.1472 | 4.03~4.27 | O | × |
| 4.6080 | 4.47~4.74 | O | × |
| 5.0688 | 4.92~5.22 | O | × |
| 5.5296 | 5.37~5.69 | O | × |
| 5.9904 | 5.81~6.17 | O | × |
| 6.4512 | 6.26~6.64 | O | × |
| 6.9120 | 6.71~7.11 | O | × |
| 7.8336 | 7.60~8.06 | O | × |
| 8.7552 | 8.50~9.01 | O | × |
| 9.2160 | 8.94~9.49 | O | × |
| 10.1376 | 9.84~10.44 | O | × |
| 11.0592 | 10.73~11.39 | O | × |
| 11.9808 | 11.63~12.34 | O | × |
| 15.6672 | 15.20~16.13 | O | × |

# 6. Reference ISP Circuit Diagram Note3)

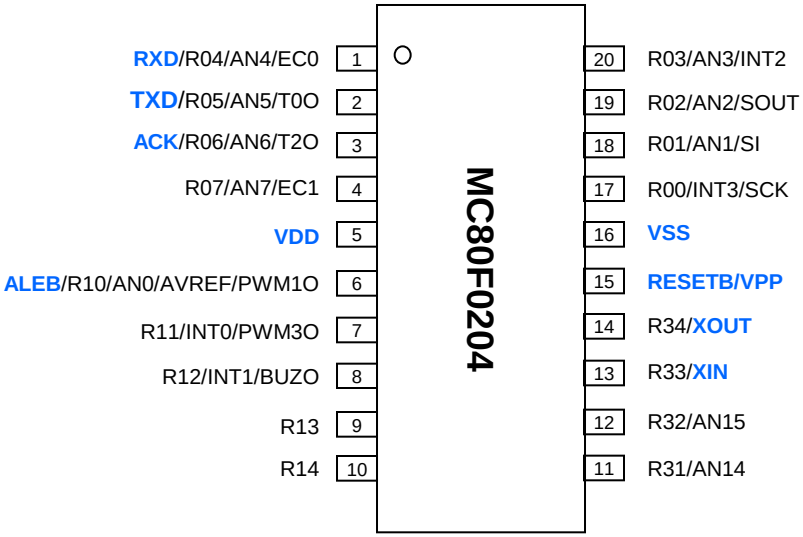


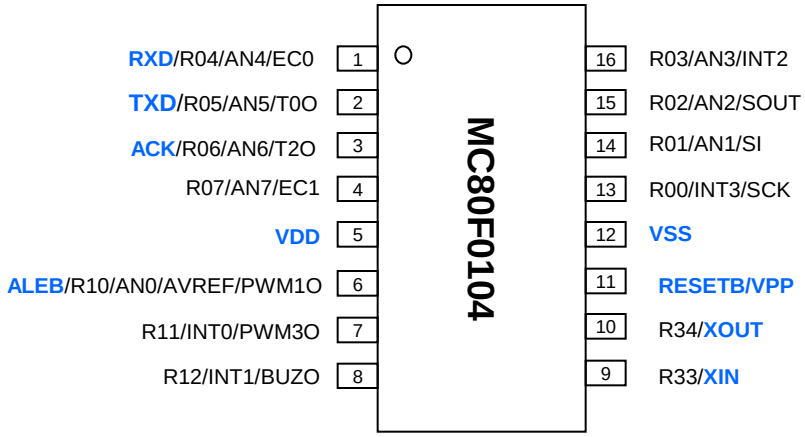




**Note1)** This block is only for ACK mode. If the auto baud rate is enabled, this circuit is not needed.
**Note2)** The external power of ISP Board is only needed when the target system Vdd is out of from 4.5 to 5.5V.
**Note3)** This circuit is same with MagnaChip supplied ISP board.

* ISP function is not supported under 2MHz system clock. For the ISP operation, power consumption required is minimum 30mA.

# 7-1 ISP configuration for MC80F0104/0204




*** ALEB** must be in logic high state.
*** Refer to at page 3. Hardware Conditions to enter the ISP mode.**

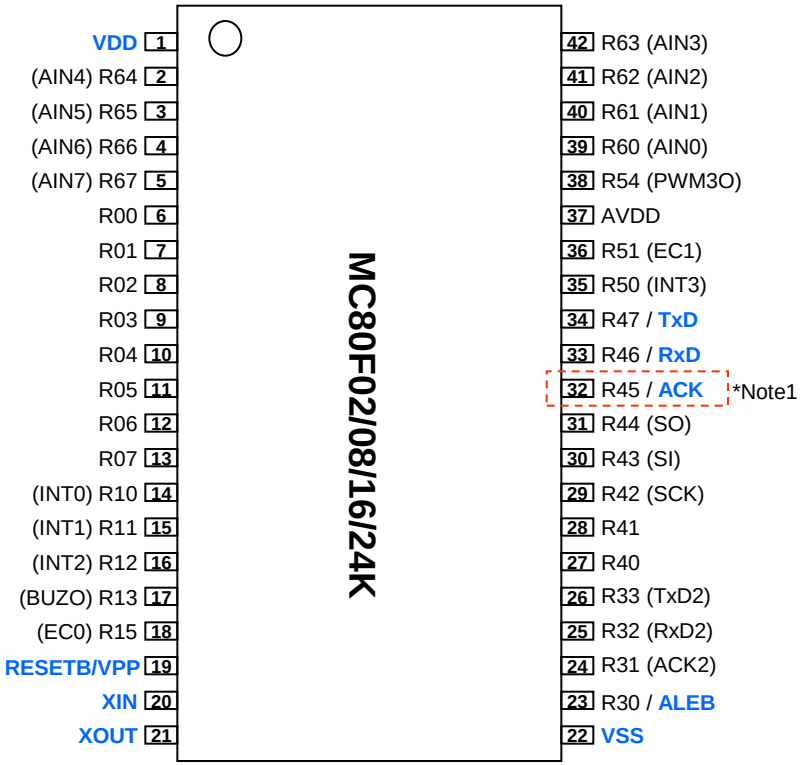
**Important!!!**

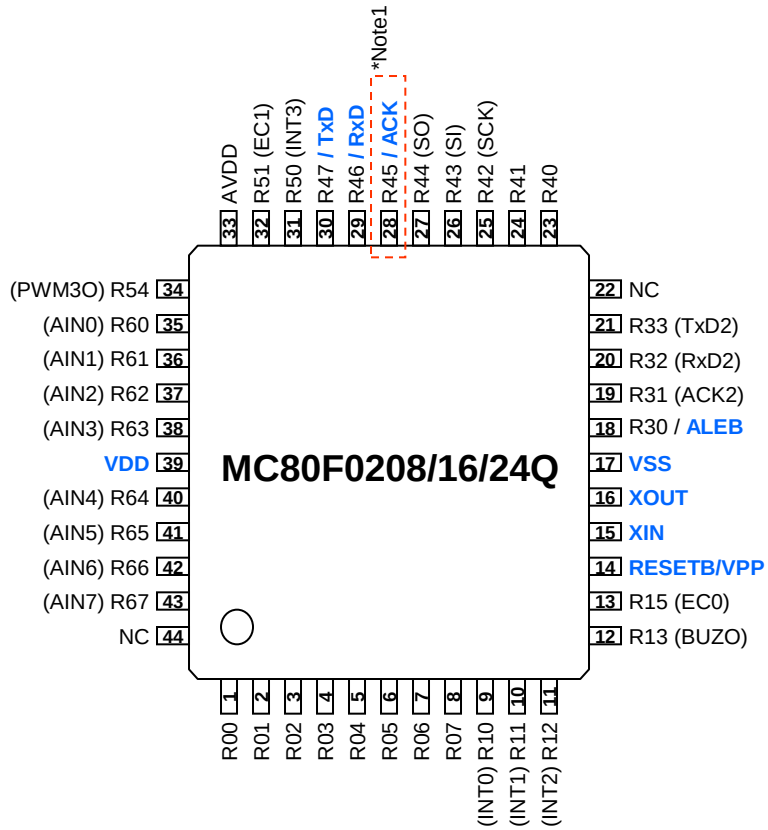
**If POR and R35 are enabled, Vdd and Vpp should be turned on simultaneously to enter ISP mode. Please follow below directions.**

1. Turn off target Vdd.
2. Select target MCU again.
   - It makes condition to make Vpp to turn on when Vdd is turned on.
3. Turn on target Vdd.

* Refer to page 4
*** This function is applied in ISP S/W ver.1.92 release at May 4th 2006.**

# 7-2 ISP configuration for MC80F0208/16/24

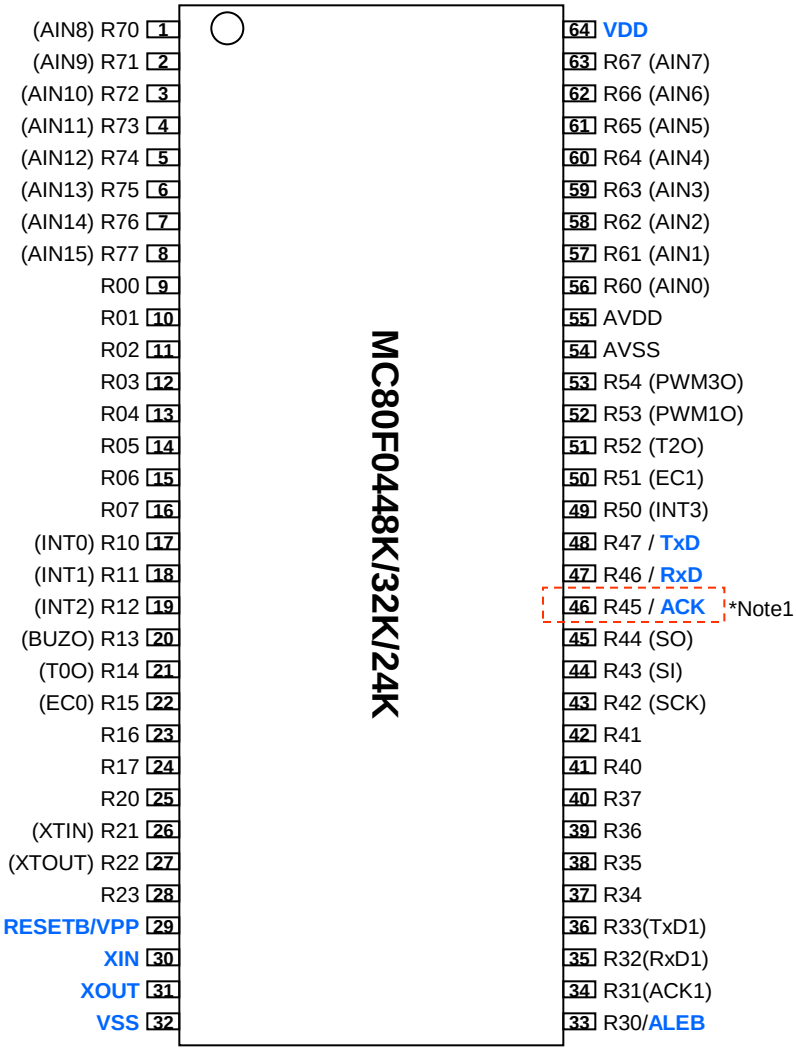


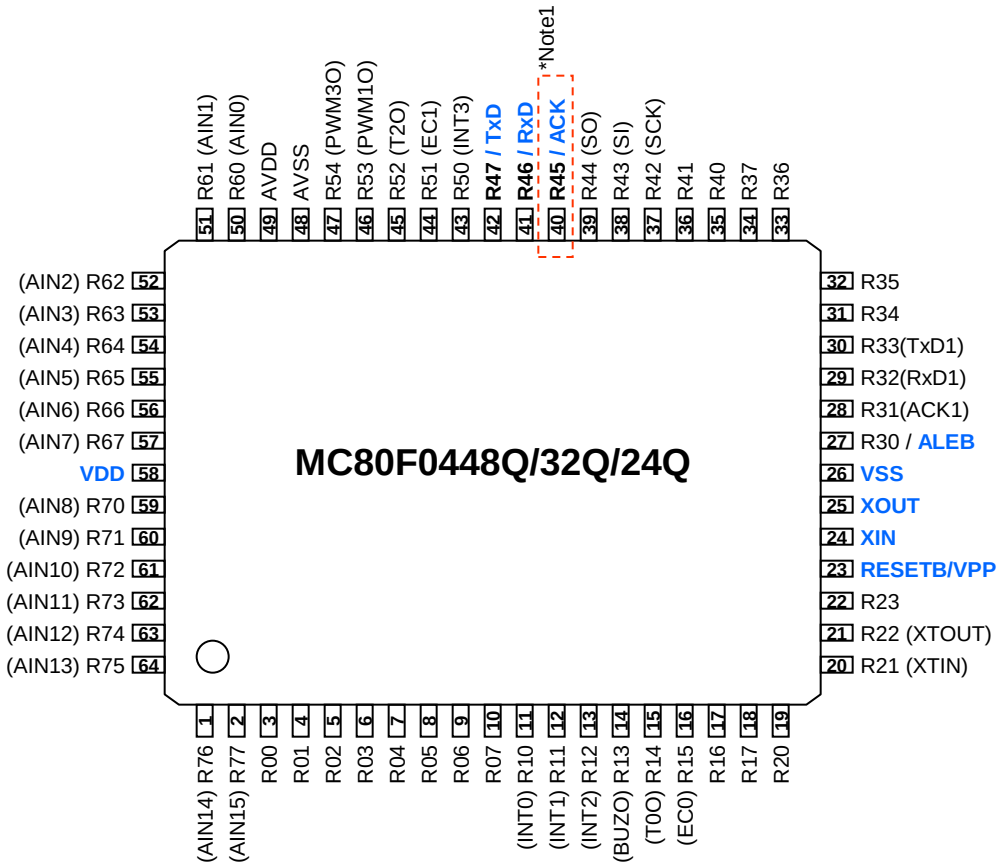




Note1) ACK pin is optional. Refer to 5. Auto Baud Rate Mode and ACK mode at page 5

* **ALEB** must be in logic high state.
* **Refer to at page 3. Hardware Conditions to enter the ISP mode.**

# 7-3-1 ISP configuration for MC80F0424/3248



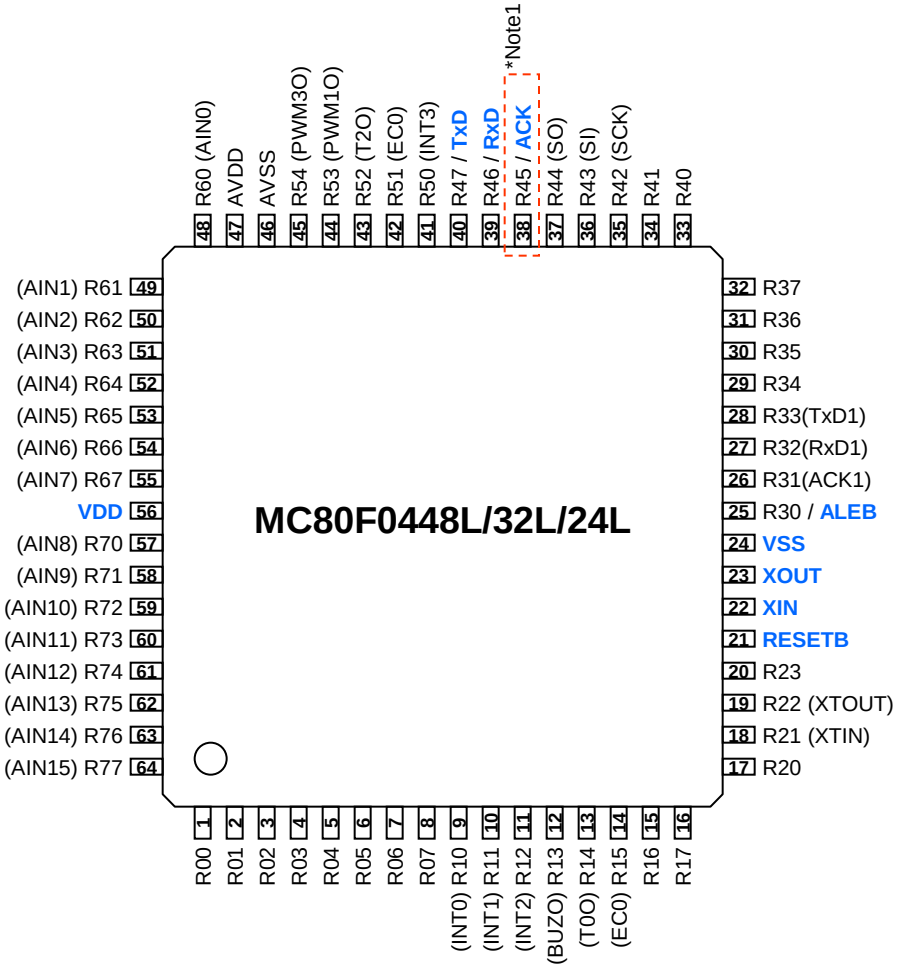




*** ALEB** must be in logic high state.

*** Refer to at page 3. Hardware Conditions to enter the ISP mode.**

Note1) ACK pin is optional. Refer to 5. Auto Baud Rate Mode and ACK mode at page 5

# 7-3-2 ISP configuration for MC80F0424/32/48

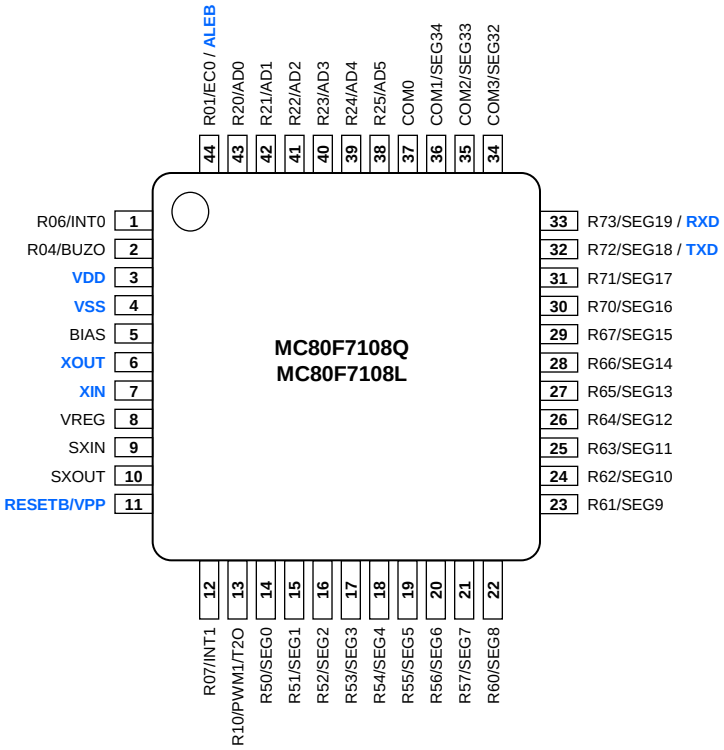


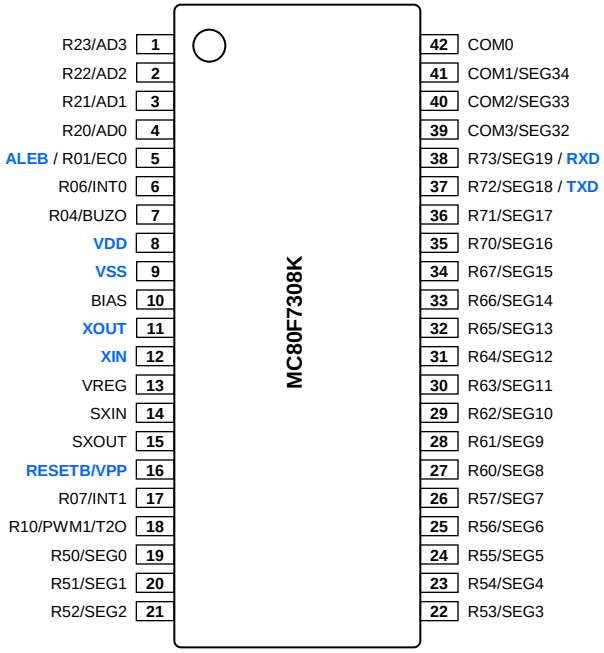

*** ALEB** must be in logic high state.

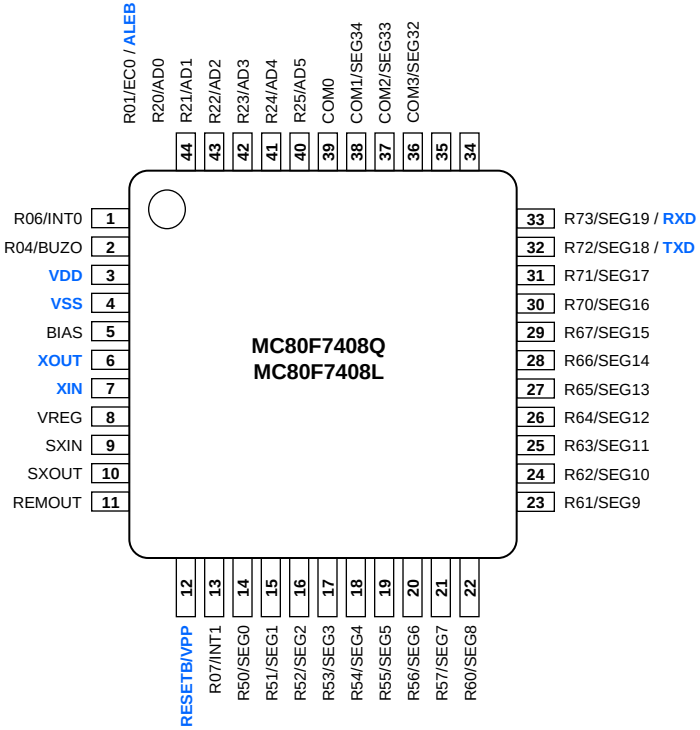
*** Refer to at page 3. Hardware Conditions to enter the ISP mode.**

Note1) ACK pin is optional. Refer to 5. Auto Baud Rate Mode and ACK mode at page 5

# 7-4 ISP configuration for MC80F7108/7308/7408



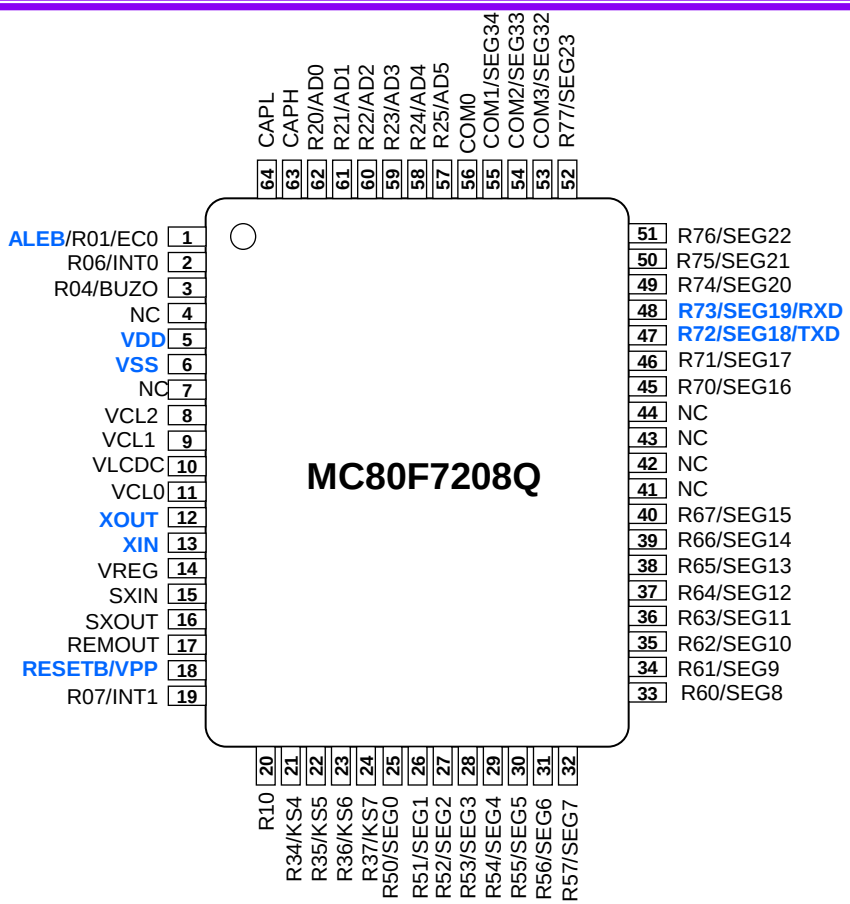



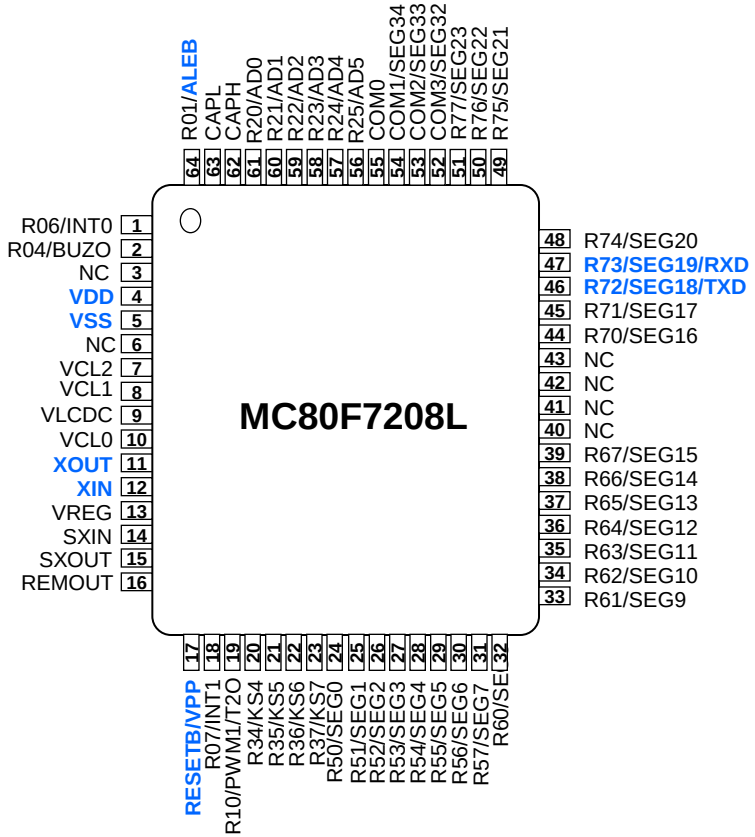




***** **ALEB** must be in logic high state.

*** Refer to at page 3. Hardware Conditions to enter the ISP mode.**

# 7-5 ISP configuration for MC80F7208

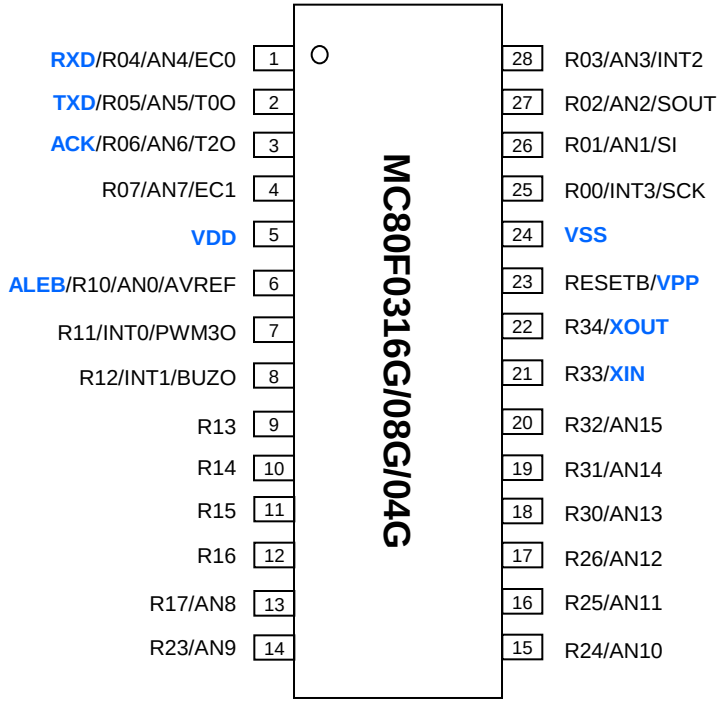


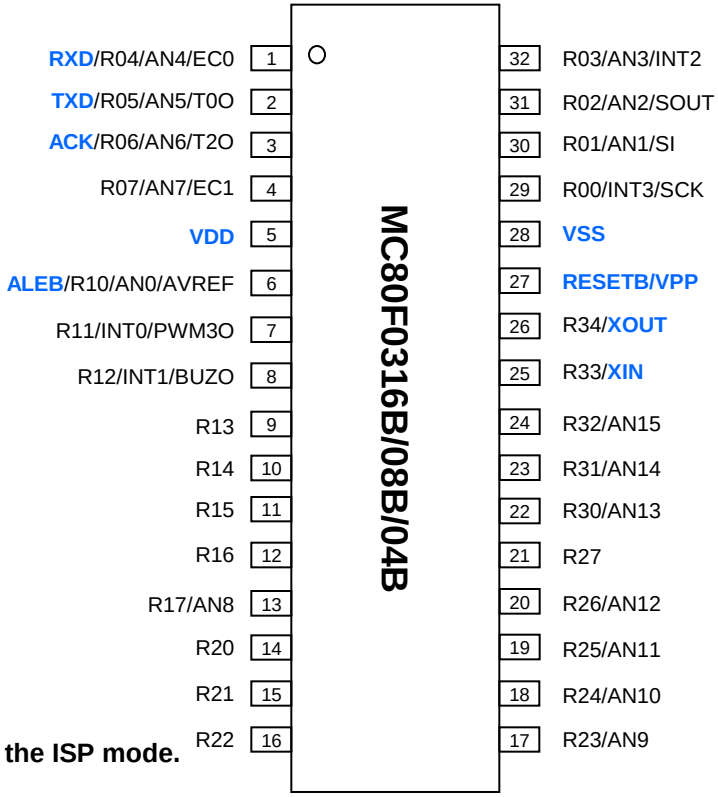




***** **ALEB** must be in logic high state.

*** Refer to at page 3. Hardware Conditions to enter the ISP mode.**

# 7-6 ISP configuration for MC80F0304/08/16




*** ALEB must be in logic high state.**

*** Refer to at page 3. Hardware Conditions to enter the ISP mode.**

**Important!!!**

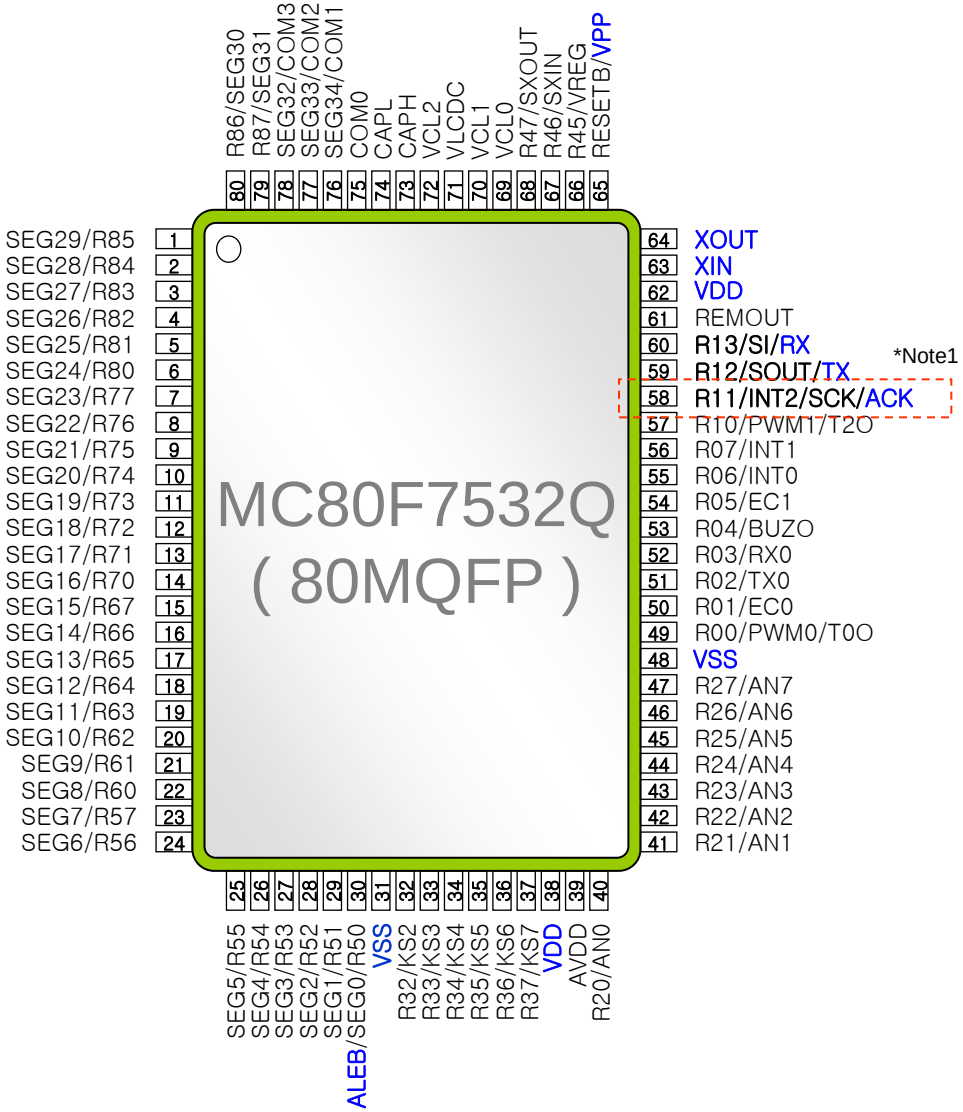
**If POR and R35 are enabled, Vdd and Vpp should be turned on simultaneously to enter ISP mode. Please follow below directions.**

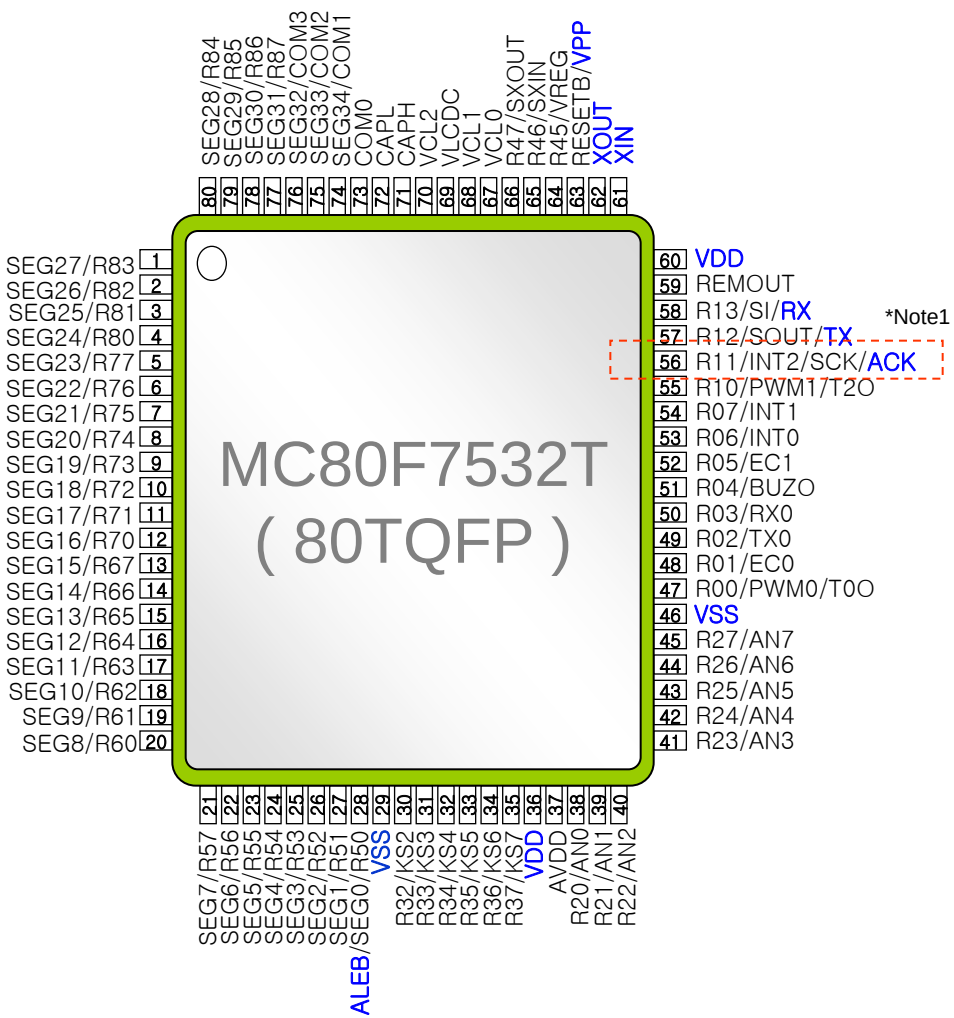
1. Turn off target Vdd.
2. Select target MCU again.
   - It makes condition to make Vpp to turn on when Vdd is turned on.
3. Turn on target Vdd.

* Refer to page 4

*** This function is applied in ISP S/W ver.1.92 release at May 4th 2006.**

# 7-7-1 ISP configuration for MC80F7532



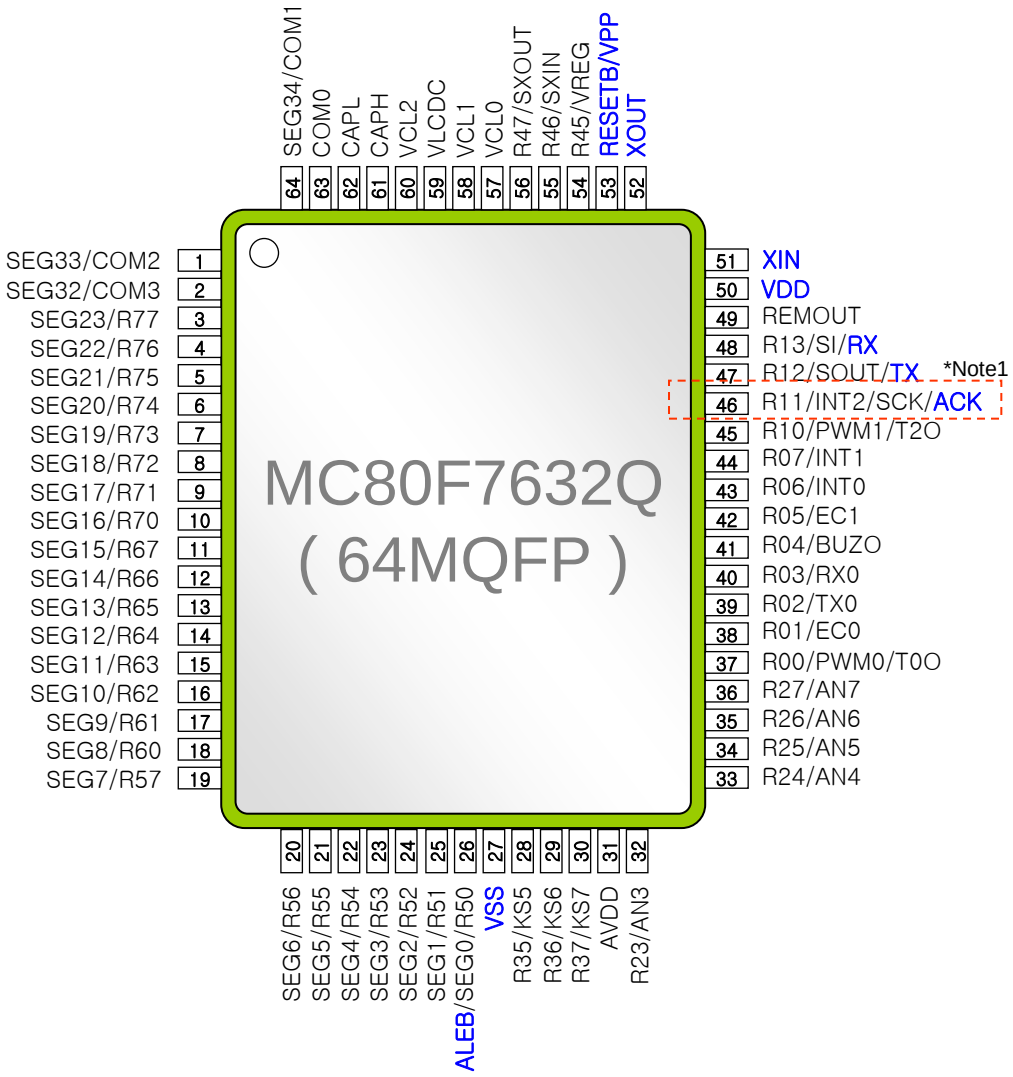



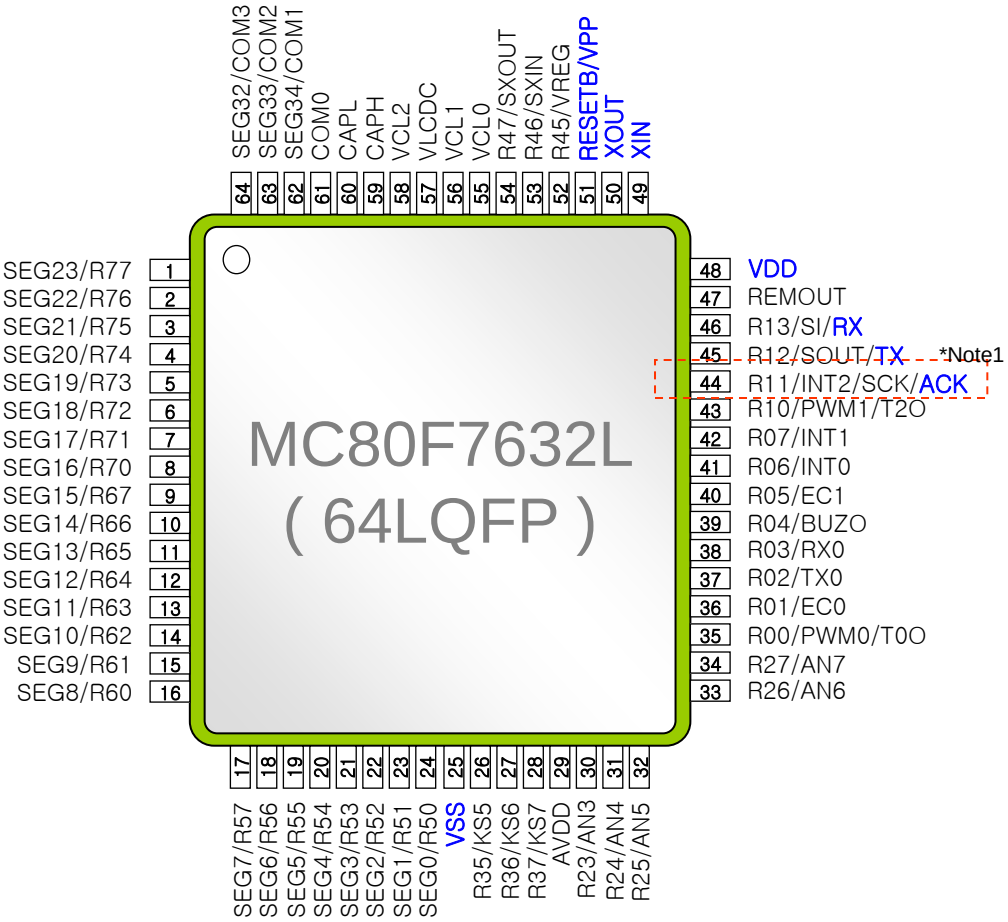

*** ALEB** must be in logic high state.

*** Refer to at page 3. Hardware Conditions to enter the ISP mode.**

Note1) ACK pin is optional. Refer to 5. Auto Baud Rate Mode and ACK mode at page 5

# 7-7-2 ISP configuration for MC80F7632



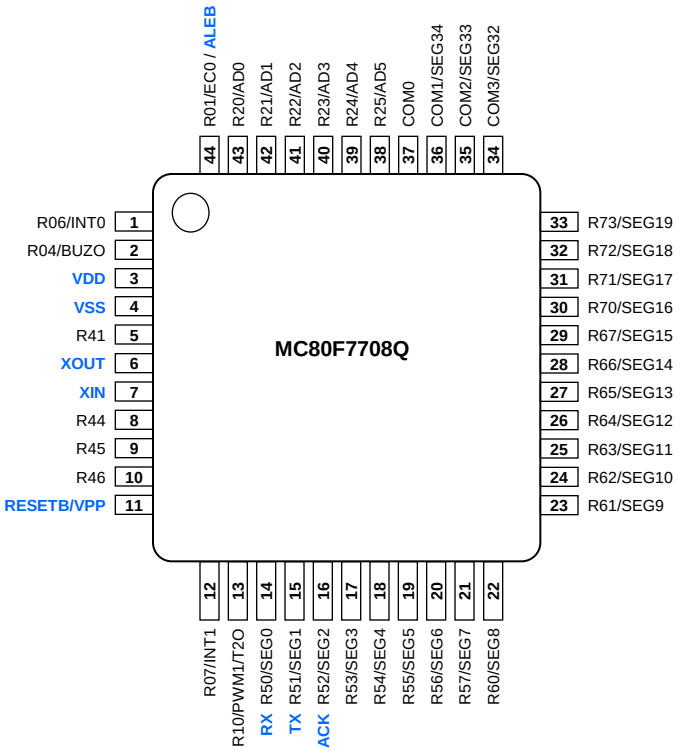



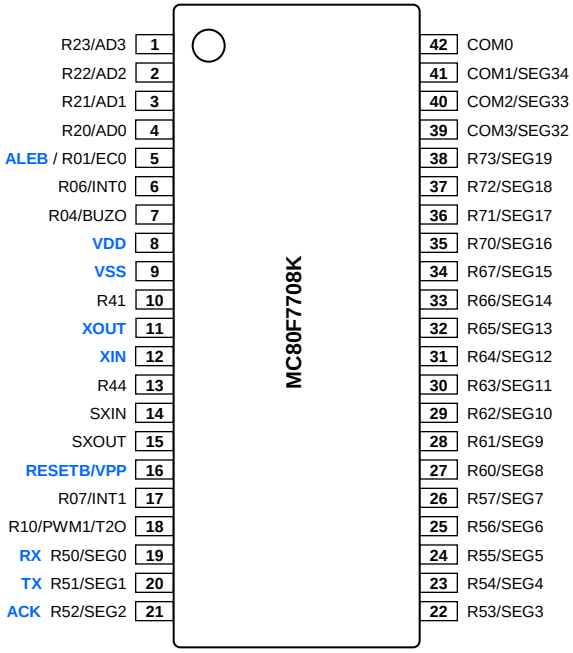

***** **ALEB** must be in logic high state.

*** Refer to at page 3. Hardware Conditions to enter the ISP mode.**

Note1) ACK pin is optional. Refer to 5. Auto Baud Rate Mode and ACK mode at page 5

# 7-8 ISP configuration for MC80F7708




***** **ALEB** must be in logic high state.

*** Refer to at page 3. Hardware Conditions to enter the ISP mode.**

**Important!!!**

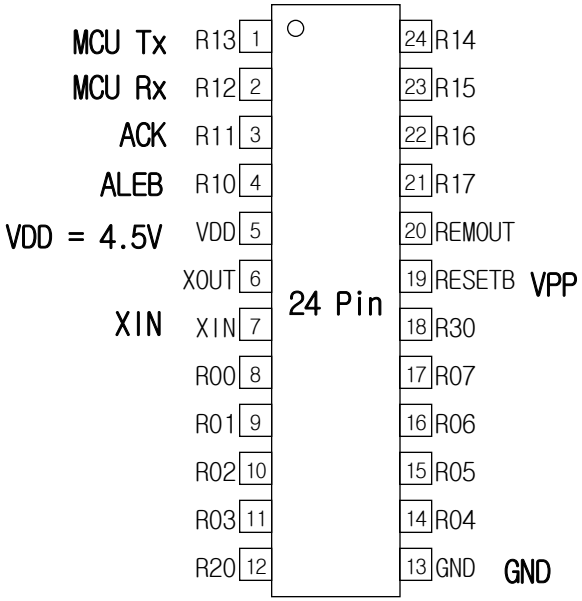
**If POR and R35 are enabled, Vdd and Vpp should be turned on simultaneously to enter ISP mode. Please follow below directions.**

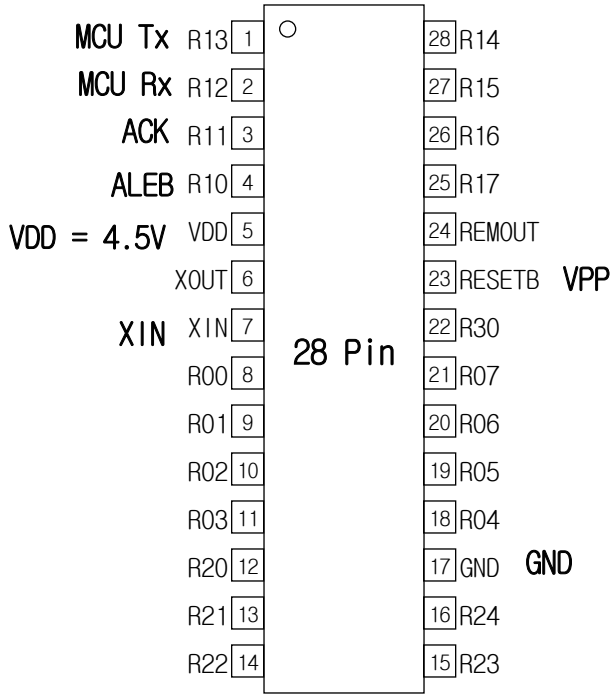
1. Turn off target Vdd.
2. Select target MCU again.
   - It makes condition to make Vpp to turn on when Vdd is turned on.
3. Turn on target Vdd.

* Refer to page 4

*** This function is applied in ISP S/W ver.1.92 release at May 4th 2006.**

# 7-9 ISP configuration for MC80F5132




***VDD must be 4.5V.**

* **ALEB** must be in logic high state.
* **Refer to at page 3. Hardware Conditions to enter the ISP mode.**

# 8. Trouble shooting

1. USB to serial cable issue (2006-08-31)
   - A USB to serial cable with a chipset(PL-2303) of prolific technology has a compatibility problem with the ISP S/W.
     If you failed to interface with ISP S/W, please use other USB to serial cable.

# 9. History

Ver. 1.52
1. MC80F7708 device support added (2007-01-10)