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Model Name : P7YE0/P7YH0/P7YS0

File Name : LA-6911P

BOM P/N:43

Compal Confidential

P7YE0/P7YH0/P7YS0 M/B Schematics Document

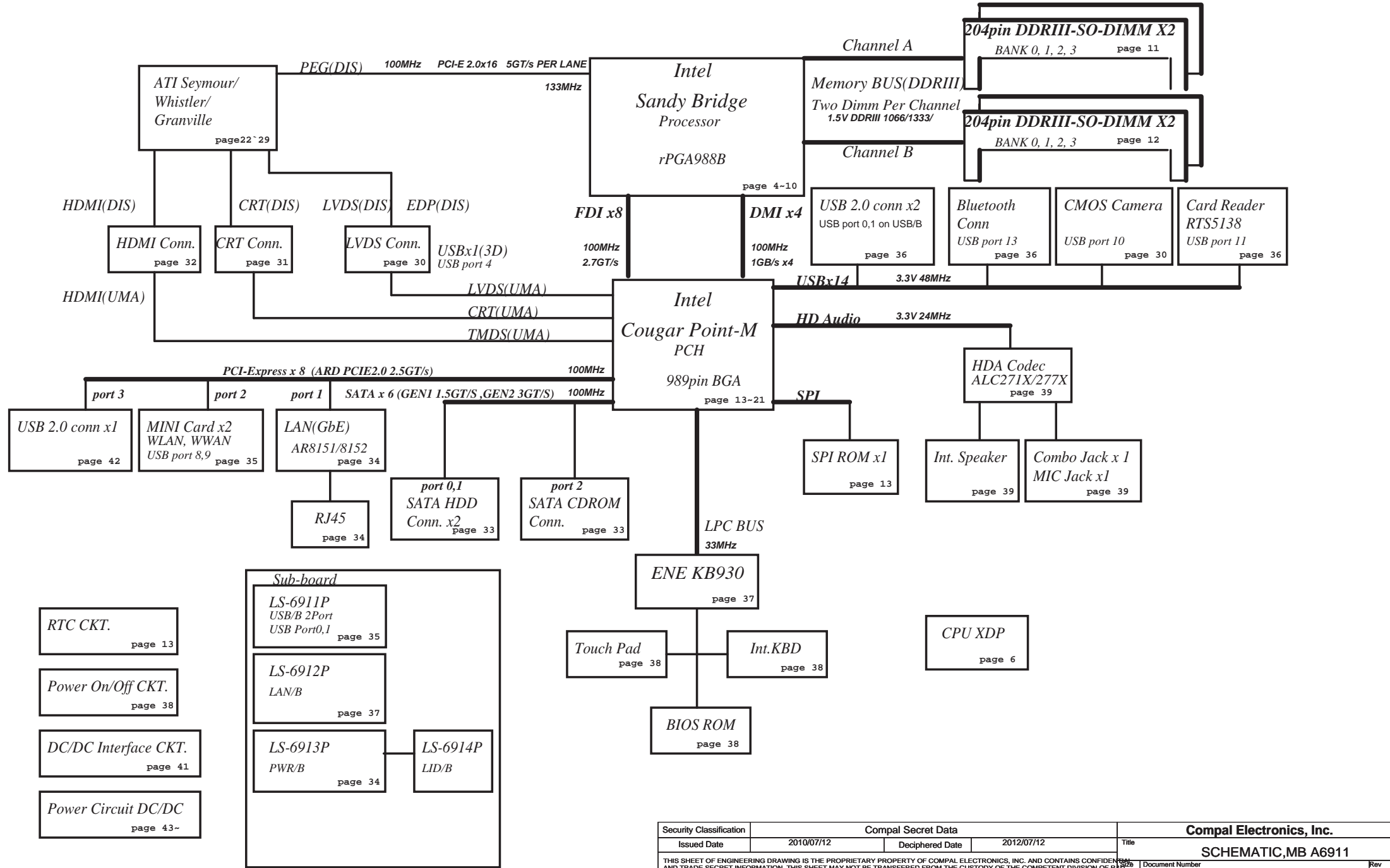
Intel Sandy Bridge Processor with DDRIII + Cougar Point PCH
ATI Seymour/Whistler/Granville

2010-11-01

REV:0.3

Security Classification	Compal Secret Data			Compal Electronics, Inc.			
Issued Date	2010/07/12	Deciphered Date	2012/07/12	Title	SCHEMATIC,MB A6911		
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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF
+VGFX_CORE	Core voltage for UMA graphic	ON	OFF	OFF
+0.75VS	+0.75VP to +0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.0VSDGPU	+1.0VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.05VS_VTT	+1.05VS_VTTP to +1.05VS_VTT switched power rail for CPU	ON	OFF	OFF
+1.05VS_PCH	+1.05VS_VTT to +1.05VS_PCH power for PCH	ON	OFF	OFF
+1.5V	+1.5VP to +1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	+1.5V to +1.5VS switched power rail	ON	OFF	OFF
+1.5VSDGPU	+1.5V to +1.5VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.8VS	(+5VALW or +3VALW) to 1.8V switched power rail to PCH & GPU	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+3VALW_PCH	+3VALW to +3VALW_PCH power rail for PCH (Short Jumper)	ON	ON	ON*
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5VALW_PCH	+5VALW to +5VALW_PCH power rail for PCH (Short resistor)	ON	ON	ON*
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+VSB	+VSBP to +VSB always on power rail for sequence control	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address

PCH SM Bus address

Device	Address	VRAM P/N
ChannelA DIMM0 A0	1010 000X	JDIMM1
DIMM1 A2	1010 001X	JDIMM3
ChannelB DIMM0 A4	1010 010X	JDIMM2
DIMM1 A6	1010 011X	JDIMM4

SAM 64*16 900M SA00004GS10(S IC D3 64Mx16 K4W1G1646G-BC11 FBGA ABOI)
 SAM 64*16 800M SA000035720(S IC D3 64Mx16 K4W1G1646G-HC12 FBGA ABOI)
 HYN 128*16 800M SA00003MG60(S IC D3 128Mx16 K4W2G1646C-HC12 FBGA ABOI)
 HYN 64*16 900M SA000041S40(S IC D3 64Mx16 H5TQ1G63DFR-11C FBGA ABOI)
 HYN 64*16 800M SA000032420(S IC D3 64Mx16 H5TQ1G63BFR-12C FBGA ABOI)
 HYN 128*16 800M SA00003VS10(S IC D3 128Mx16 H5TQ2G63BFR-12C FBGA ABOI)
 HYN 64*16 800M SA0000324G0(S IC D3 64Mx16 H5TQ1G63DFR-12C FBGA ABOI)

BT Config	GPU config	BACO config
BT SKU: BT@	Whistler: WHIS@	BACO: BACO@
4DIMM config	Seymour: SEYM@	nonBACO: NOBACO@
4 DIMM: 4DIMM@	Granville: GRAN@	Muxless config
LVDS/eDP config	Granville config	Muxless: MUXL@
UMA LVDS: ULVDS@	Granville: GRAN@ (VDDCI)	nonMuxless: NOMUXL@ (DISO,UMAO)
DIS LVDS: DLVDS@	nonGranville: NOGRAN@ (VGA_CORE)	
DIS eDP: DEDP@	GPU Frame config	
	128bit: 128@ (WHIS,GRAN)	
		VRAM BOM Config
		X76264BOL01: 64Mx16x4 Seymour 512M HYN NEW
		X76264BOL02: 64Mx16x4 Seymour 512M HYN OLD
		X76264BOL03: 64Mx16x8 Whistler/Granville 1G HYN NEW
		X76264BOL04: 64Mx16x8 Whistler/Granville 1G HYN OLD
		X76264BOL05: 128Mx16x8 Whistler/Granville 2G HYN
		X76264BOL06: 128Mx16x8 Whistler/Granville 2G SAM
		X76264BOL07: 128Mx16x4 Seymour 1G SAM
		X76264BOL08: 128Mx16x4 Seymour 1G HYN

BOM Config		
* UMA Only LVDS Panel:	BT@/UMAO@/UMA@/ULVDS@/NOMUXL@	+DIMM,USB option
* DIS Only LVDS Panel:	BT@/DIS@/VGA@/DISO@/DLVDS@/NOMUXL@	+DIMM,USB option
* DIS Only EDP Panel:	BT@/DIS@/VGA@/DISO@/DEDP@/NOMUXL@	+DIMM,USB option
* Muxless BACO LVDS Panel:	BT@/UMA@/DIS@/VGA@/ULVDS@/BACO@/MUXL@	+X76+GPU(S,W) +DIMM,USB option
* Muxless nonBACO LVDS Panel:	BT@/UMA@/DIS@/VGA@/ULVDS@/NOBACO@/MUXL@	+X76+GPU(G) +DIMM,USB option

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3(Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4(Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5(Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	V _{AD_BID} min	V _{AD_BID} typ	V _{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	
5	
6	
7	

BTO Option Table

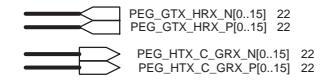
BTO Item	BOM Structure
UMA Only	UMAO@
Muxless/UMA	UMA@
DIS Only	DISO@
Muxless/DIS	DIS@
Muxless/DIS	VGA@
BACO mode	BACO@
nonBACO mode	NOBACO@
VRAM	X76@
128bit VRAM	128@
Granville GPU	GRAN@
Whistler GPU	WHIS@
Seymour GPU	SEYM@
non Granville GPU	NOGRAN@
Blue Tooth	BT@
Connector	CONN@
Unpop	@
DIS eDP	DEDP@
UMA LVDS	ULVDS@
DIS LVDS	DLVDS@
Muxless	MUXL@
non Muxless	NOMUXL@
USB2.0 Conn	USB2@
USB3.0 Conn	USB3@
4 Dimm	4DIMM@

USB Port Table

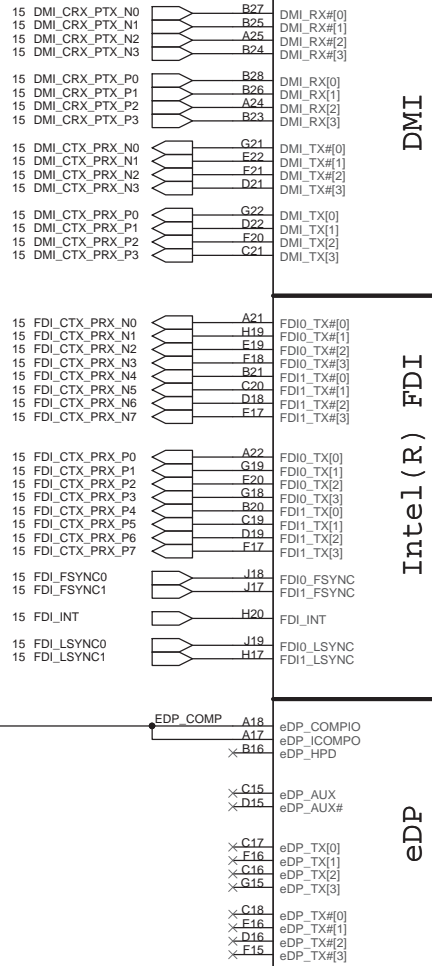
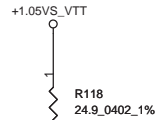
USB 2.0	USB 1.1	Port	3 External USB Port
		0	USB/B(Right side 2.0 option)
		1	USB/B(Right side 2.0 option)
		2	USB port(left side 2.0)
		3	USB/B(Right side 3.0 option)
		4	
		5	
		6	
		7	
		8	Mini Card(WLAN)
		9	Mini Card
		10	Camera
		11	Card Reader
		12	
		13	Blue Tooth

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PEG_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 mohms
 PEG_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 mohms



eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms should not be left floating ,even if disable eDP function...



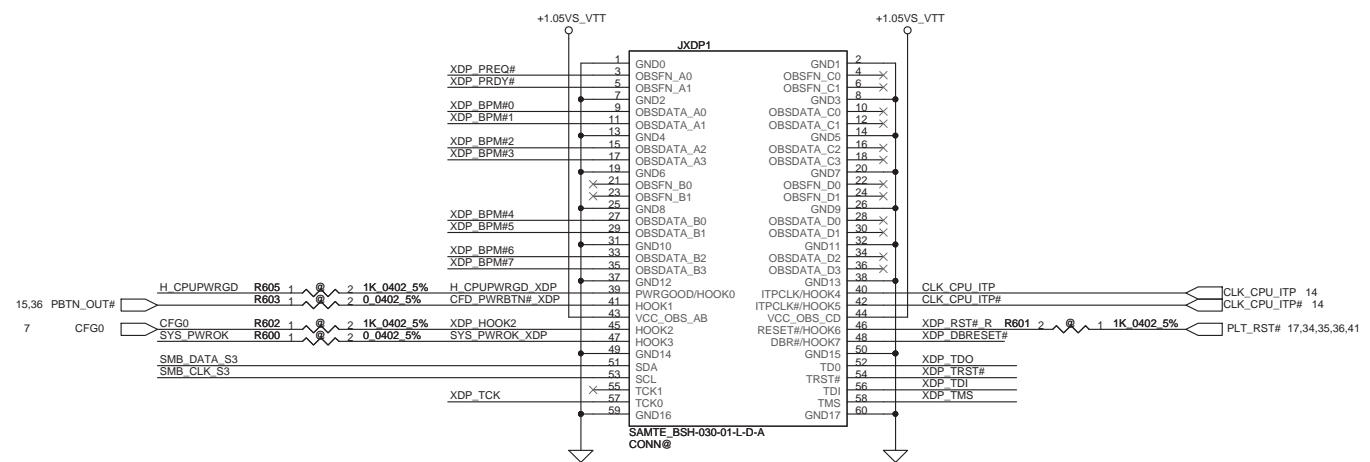
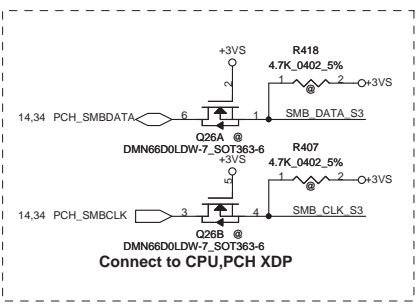
PCI EXPRESS* - GRAPHICS

Signal	Component	Value	Notes
PEG_ICOMPI	J22	PEG_COMP	
PEG_ICOMPO	J21		
PEG_RCOMPO	H22		
PEG_RX#[0]	K33	PEG GTX C HRX N15 C320	2 DIS@ 0.22u 0402 6.3V6K PEG GTX HRX N15
PEG_RX#[1]	M35	PEG GTX C HRX N14 C316	2 DIS@ 0.22u 0402 6.3V6K PEG GTX HRX N14
PEG_RX#[2]	L34	PEG GTX C HRX N13 C313	2 DIS@ 0.22u 0402 6.3V6K PEG GTX HRX N13
PEG_RX#[3]	J35	PEG GTX C HRX N12 C308	2 DIS@ 0.22u 0402 6.3V6K PEG GTX HRX N12
PEG_RX#[4]	J32	PEG GTX C HRX N11 C300	2 DIS@ 0.22u 0402 6.3V6K PEG GTX HRX N11
PEG_RX#[5]	H34	PEG GTX C HRX N10 C297	2 DIS@ 0.22u 0402 6.3V6K PEG GTX HRX N10
PEG_RX#[6]	H31	PEG GTX C HRX N9 C287	2 DIS@ 0.22u 0402 6.3V6K PEG GTX HRX N9
PEG_RX#[7]	G33	PEG GTX C HRX N8 C275	2 DIS@ 0.22u 0402 6.3V6K PEG GTX HRX N8
PEG_RX#[8]	G30	PEG GTX C HRX N7 C262	2 DIS@ 0.22u 0402 6.3V6K PEG GTX HRX N7
PEG_RX#[9]	F34	PEG GTX C HRX N6 C249	2 DIS@ 0.22u 0402 6.3V6K PEG GTX HRX N6
PEG_RX#[10]	F32	PEG GTX C HRX N5 C244	2 DIS@ 0.22u 0402 6.3V6K PEG GTX HRX N5
PEG_RX#[11]	E32	PEG GTX C HRX N4 C233	2 DIS@ 0.22u 0402 6.3V6K PEG GTX HRX N4
PEG_RX#[12]	D33	PEG GTX C HRX N3 C224	2 DIS@ 0.22u 0402 6.3V6K PEG GTX HRX N3
PEG_RX#[13]	D31	PEG GTX C HRX N2 C207	2 DIS@ 0.22u 0402 6.3V6K PEG GTX HRX N2
PEG_RX#[14]	B33	PEG GTX C HRX N1 C206	2 DIS@ 0.22u 0402 6.3V6K PEG GTX HRX N1
PEG_RX#[15]	C32	PEG GTX C HRX N0 C194	2 DIS@ 0.22u 0402 6.3V6K PEG GTX HRX N0
PEG_RX#[16]	J33	PEG GTX C HRX P15 C318	2 DIS@ 0.22u 0402 6.3V6K PEG GTX HRX P15
PEG_RX#[17]	L35	PEG GTX C HRX P14 C314	2 DIS@ 0.22u 0402 6.3V6K PEG GTX HRX P14
PEG_RX#[18]	K34	PEG GTX C HRX P13 C309	2 DIS@ 0.22u 0402 6.3V6K PEG GTX HRX P13
PEG_RX#[19]	H35	PEG GTX C HRX P12 C303	2 DIS@ 0.22u 0402 6.3V6K PEG GTX HRX P12
PEG_RX#[20]	H32	PEG GTX C HRX P11 C298	2 DIS@ 0.22u 0402 6.3V6K PEG GTX HRX P11
PEG_RX#[21]	G34	PEG GTX C HRX P10 C288	2 DIS@ 0.22u 0402 6.3V6K PEG GTX HRX P10
PEG_RX#[22]	G31	PEG GTX C HRX P9 C278	2 DIS@ 0.22u 0402 6.3V6K PEG GTX HRX P9
PEG_RX#[23]	F33	PEG GTX C HRX P8 C265	2 DIS@ 0.22u 0402 6.3V6K PEG GTX HRX P8
PEG_RX#[24]	F30	PEG GTX C HRX P7 C255	2 DIS@ 0.22u 0402 6.3V6K PEG GTX HRX P7
PEG_RX#[25]	E35	PEG GTX C HRX P6 C246	2 DIS@ 0.22u 0402 6.3V6K PEG GTX HRX P6
PEG_RX#[26]	E33	PEG GTX C HRX P5 C235	2 DIS@ 0.22u 0402 6.3V6K PEG GTX HRX P5
PEG_RX#[27]	F32	PEG GTX C HRX P4 C225	2 DIS@ 0.22u 0402 6.3V6K PEG GTX HRX P4
PEG_RX#[28]	D34	PEG GTX C HRX P3 C214	2 DIS@ 0.22u 0402 6.3V6K PEG GTX HRX P3
PEG_RX#[29]	E31	PEG GTX C HRX P2 C210	2 DIS@ 0.22u 0402 6.3V6K PEG GTX HRX P2
PEG_RX#[30]	C33	PEG GTX C HRX P1 C196	2 DIS@ 0.22u 0402 6.3V6K PEG GTX HRX P1
PEG_RX#[31]	B32	PEG GTX C HRX P0 C190	2 DIS@ 0.22u 0402 6.3V6K PEG GTX HRX P0
PEG_TX#[0]	M29	PEG HTX GRX N15 C685	2 DIS@ 0.22u 0402 6.3V6K PEG HTX C GRX N15
PEG_TX#[1]	M32	PEG HTX GRX N14 C683	2 DIS@ 0.22u 0402 6.3V6K PEG HTX C GRX N14
PEG_TX#[2]	M31	PEG HTX GRX N13 C680	2 DIS@ 0.22u 0402 6.3V6K PEG HTX C GRX N13
PEG_TX#[3]	L32	PEG HTX GRX N12 C676	2 DIS@ 0.22u 0402 6.3V6K PEG HTX C GRX N12
PEG_TX#[4]	L29	PEG HTX GRX N11 C673	2 DIS@ 0.22u 0402 6.3V6K PEG HTX C GRX N11
PEG_TX#[5]	K31	PEG HTX GRX N10 C671	2 DIS@ 0.22u 0402 6.3V6K PEG HTX C GRX N10
PEG_TX#[6]	K28	PEG HTX GRX N9 C667	2 DIS@ 0.22u 0402 6.3V6K PEG HTX C GRX N9
PEG_TX#[7]	J30	PEG HTX GRX N8 C663	2 DIS@ 0.22u 0402 6.3V6K PEG HTX C GRX N8
PEG_TX#[8]	J28	PEG HTX GRX N7 C659	2 DIS@ 0.22u 0402 6.3V6K PEG HTX C GRX N7
PEG_TX#[9]	H29	PEG HTX GRX N6 C659	2 DIS@ 0.22u 0402 6.3V6K PEG HTX C GRX N6
PEG_TX#[10]	G27	PEG HTX GRX N5 C654	2 DIS@ 0.22u 0402 6.3V6K PEG HTX C GRX N5
PEG_TX#[11]	E29	PEG HTX GRX N4 C648	2 DIS@ 0.22u 0402 6.3V6K PEG HTX C GRX N4
PEG_TX#[12]	F27	PEG HTX GRX N3 C644	2 DIS@ 0.22u 0402 6.3V6K PEG HTX C GRX N3
PEG_TX#[13]	D28	PEG HTX GRX N2 C640	2 DIS@ 0.22u 0402 6.3V6K PEG HTX C GRX N2
PEG_TX#[14]	E26	PEG HTX GRX N1 C637	2 DIS@ 0.22u 0402 6.3V6K PEG HTX C GRX N1
PEG_TX#[15]	E25	PEG HTX GRX N0 C631	2 DIS@ 0.22u 0402 6.3V6K PEG HTX C GRX N0
PEG_TX#[16]	M28	PEG HTX GRX P15 C684	2 DIS@ 0.22u 0402 6.3V6K PEG HTX C GRX P15
PEG_TX#[17]	M33	PEG HTX GRX P14 C681	2 DIS@ 0.22u 0402 6.3V6K PEG HTX C GRX P14
PEG_TX#[18]	M30	PEG HTX GRX P13 C677	2 DIS@ 0.22u 0402 6.3V6K PEG HTX C GRX P13
PEG_TX#[19]	L31	PEG HTX GRX P12 C674	2 DIS@ 0.22u 0402 6.3V6K PEG HTX C GRX P12
PEG_TX#[20]	L28	PEG HTX GRX P11 C670	2 DIS@ 0.22u 0402 6.3V6K PEG HTX C GRX P11
PEG_TX#[21]	K30	PEG HTX GRX P10 C668	2 DIS@ 0.22u 0402 6.3V6K PEG HTX C GRX P10
PEG_TX#[22]	K27	PEG HTX GRX P9 C664	2 DIS@ 0.22u 0402 6.3V6K PEG HTX C GRX P9
PEG_TX#[23]	J29	PEG HTX GRX P8 C662	2 DIS@ 0.22u 0402 6.3V6K PEG HTX C GRX P8
PEG_TX#[24]	J27	PEG HTX GRX P7 C658	2 DIS@ 0.22u 0402 6.3V6K PEG HTX C GRX P7
PEG_TX#[25]	H28	PEG HTX GRX P6 C657	2 DIS@ 0.22u 0402 6.3V6K PEG HTX C GRX P6
PEG_TX#[26]	G28	PEG HTX GRX P5 C650	2 DIS@ 0.22u 0402 6.3V6K PEG HTX C GRX P5
PEG_TX#[27]	E28	PEG HTX GRX P4 C645	2 DIS@ 0.22u 0402 6.3V6K PEG HTX C GRX P4
PEG_TX#[28]	F28	PEG HTX GRX P3 C641	2 DIS@ 0.22u 0402 6.3V6K PEG HTX C GRX P3
PEG_TX#[29]	D27	PEG HTX GRX P2 C636	2 DIS@ 0.22u 0402 6.3V6K PEG HTX C GRX P2
PEG_TX#[30]	E26	PEG HTX GRX P1 C635	2 DIS@ 0.22u 0402 6.3V6K PEG HTX C GRX P1
PEG_TX#[31]	D25	PEG HTX GRX P0 C626	2 DIS@ 0.22u 0402 6.3V6K PEG HTX C GRX P0

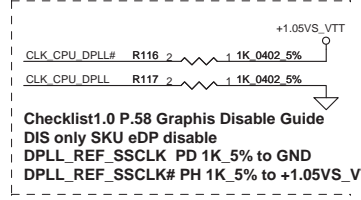
Sandy Bridge_rPGA_Rev0p61
 CONN@

Typ- suggest 220nF. The change in AC capacitor value from 100nF to 220nF is to enable compatibility with future platforms having PCIe Gen3 (8GT/s)

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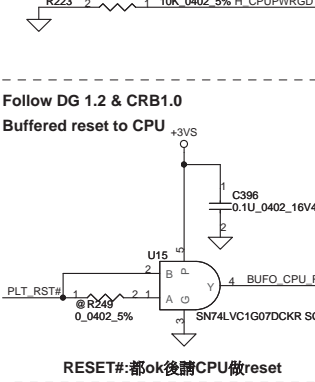
Debug port DG 0.65--
 Note: 1. These signals are optional, can be left as OPEN/No-Connect if debug by Intel will not be needed



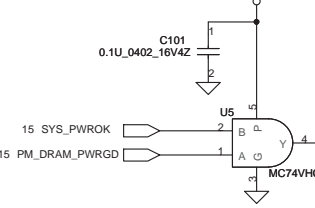
Checklist 1.0 P.58 Graphis Disable Guide
 DIS only SKU eDP disable
 DPPLL_REF_SSCLK PD 1K 5% to GND
 DPPLL_REF_SSCLK# PH 1K 5% to +1.05VS_VTT

PCH->CPU
 UNCOREPWRGOOD:非CORE外的電OK
 SM_DRAMPWROK:DRAM power ok
 RESET#:都ok後請CPU做reset

Follow DG 1.2 & CRB1.0



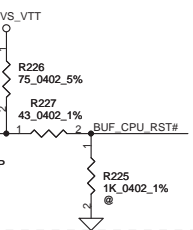
Follow DG 1.2 & CRB1.0



Processor Pullups follow CRB1.0

Follow DG 1.2 & CRB1.0

Buffered reset to CPU

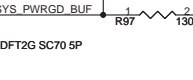


Follow DG 1.2 & CRB1.0

Use open drain MOS:

+1.05VS_VTT PH pop 75ohm

series resistor pop 43ohm



偵測CPU有無安裝

XBOX三紅功能

UNCOREPWRGOOD:非CORE外的電OK

SM_DRAMPWROK:DRAM power ok

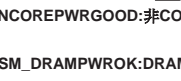
RESET#:都ok後請CPU做reset

Follow DG 1.2 & CRB1.0

Use open drain MOS:

+1.5V_CPU_VDDQ PH pop 200ohm

series resistor pop 130ohm



Follow DG 1.2 & CRB1.0

Use open drain MOS:

+1.5V_CPU_VDDQ PH pop 200ohm

series resistor pop 130ohm

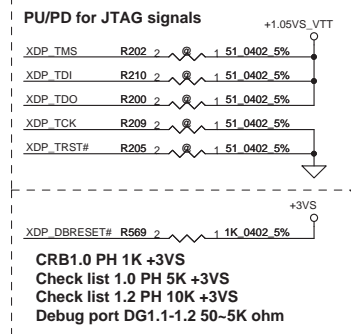
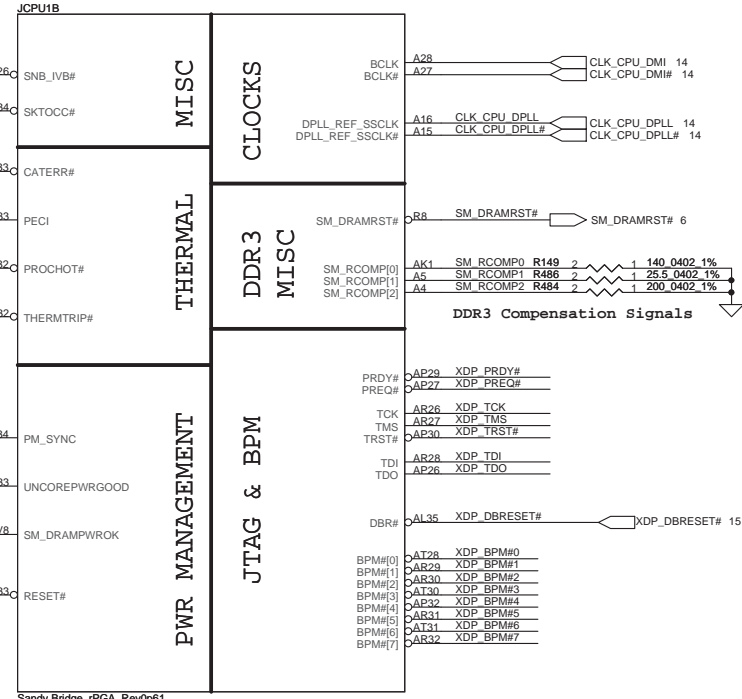


Follow DG 1.2 & CRB1.0

Use open drain MOS:

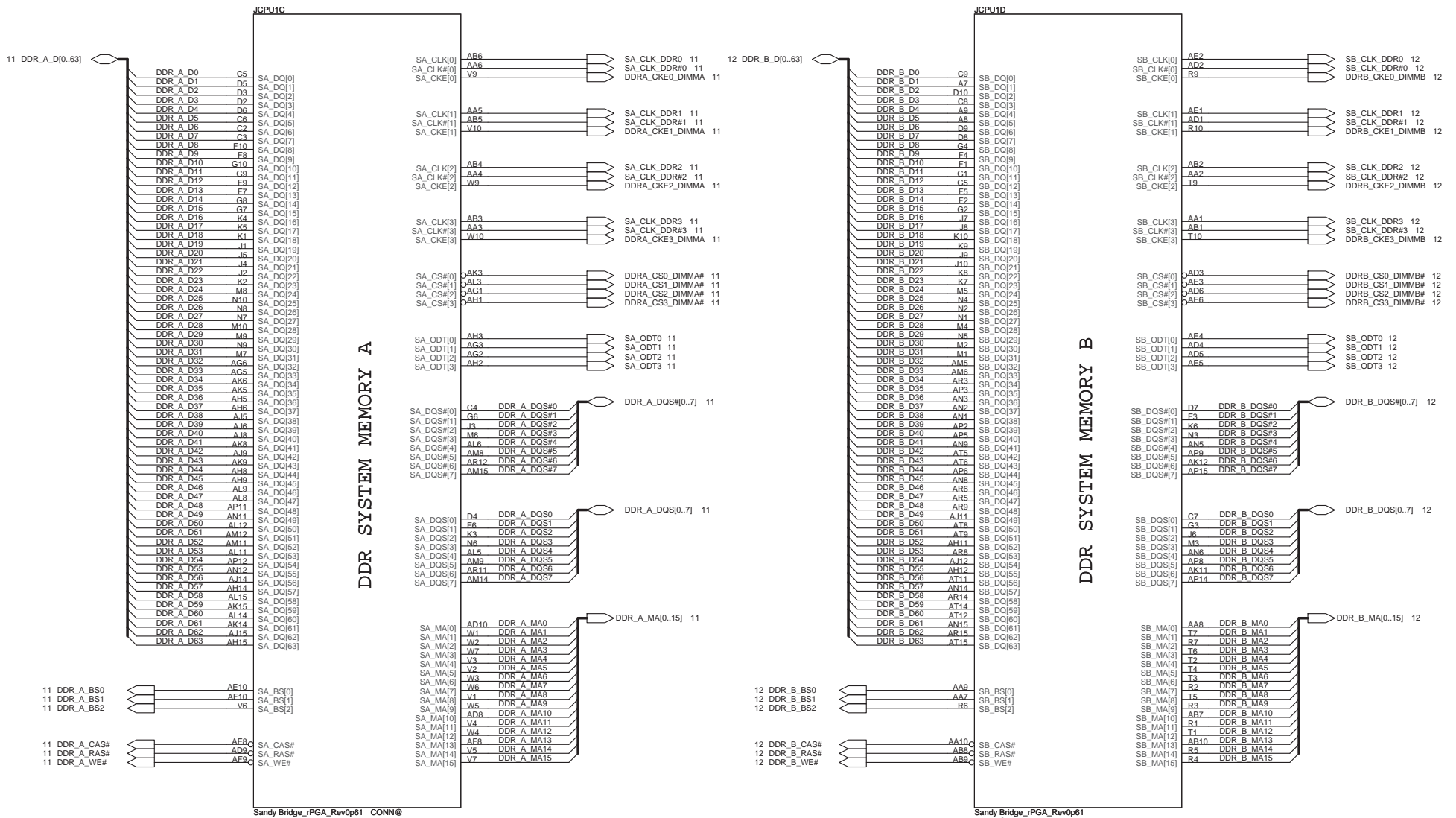
+1.5V_CPU_VDDQ PH pop 200ohm

series resistor pop 130ohm



CRB1.0 PH 1K +3VS
 Check list 1.0 PH 5K +3VS
 Check list 1.2 PH 10K +3VS
 Debug port DG1.1-1.2 50-5K ohm

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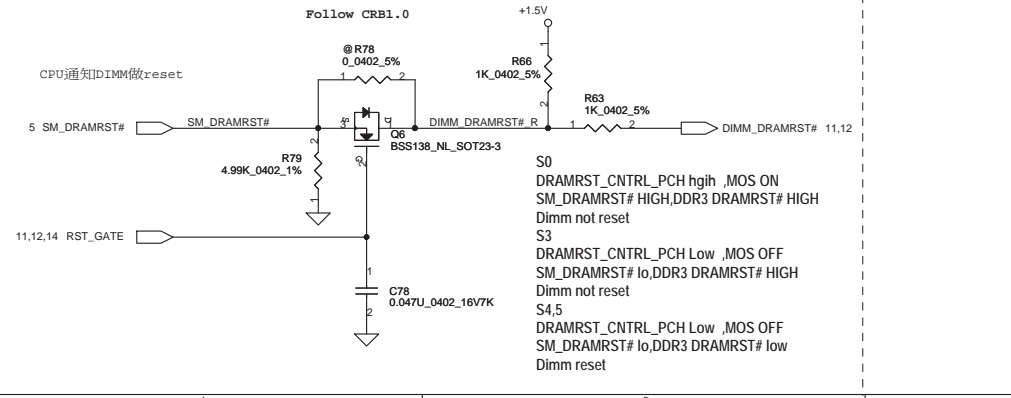


DDR SYSTEM MEMORY A

DDR SYSTEM MEMORY B

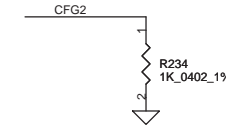
Sandy Bridge_rPGA_Rev0p61 CONN@

Sandy Bridge_rPGA_Rev0p61 CONN@

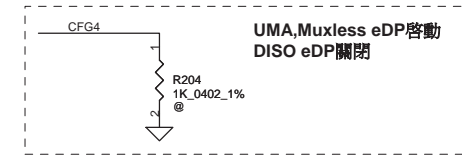


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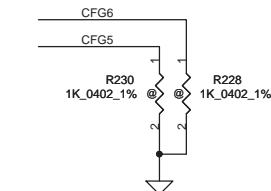
CFG Straps for Processor



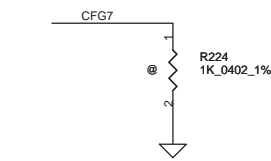
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0: Lane Reversed



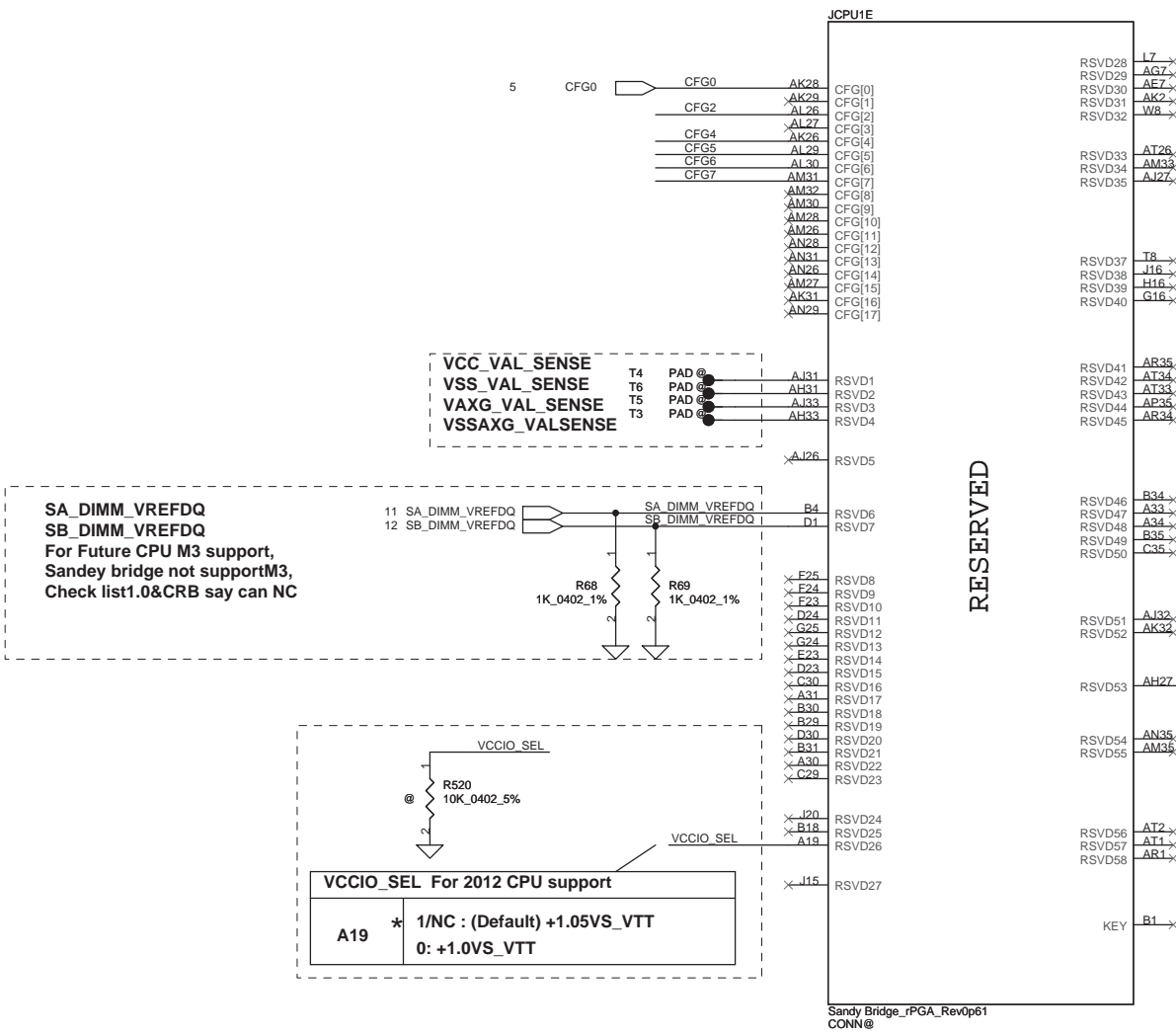
UMA, Muxless eDP 启动 DISO eDP 關閉	
CFG4	* 1: Disable 0: Enable



PCIe Port Bifurcation Straps	
CFG[6:5]	*11: (Default) 1x16 PCI Express 10: 2x8 PCI Express 01: Reserved 00: 1x8, 2x4 PCI Express

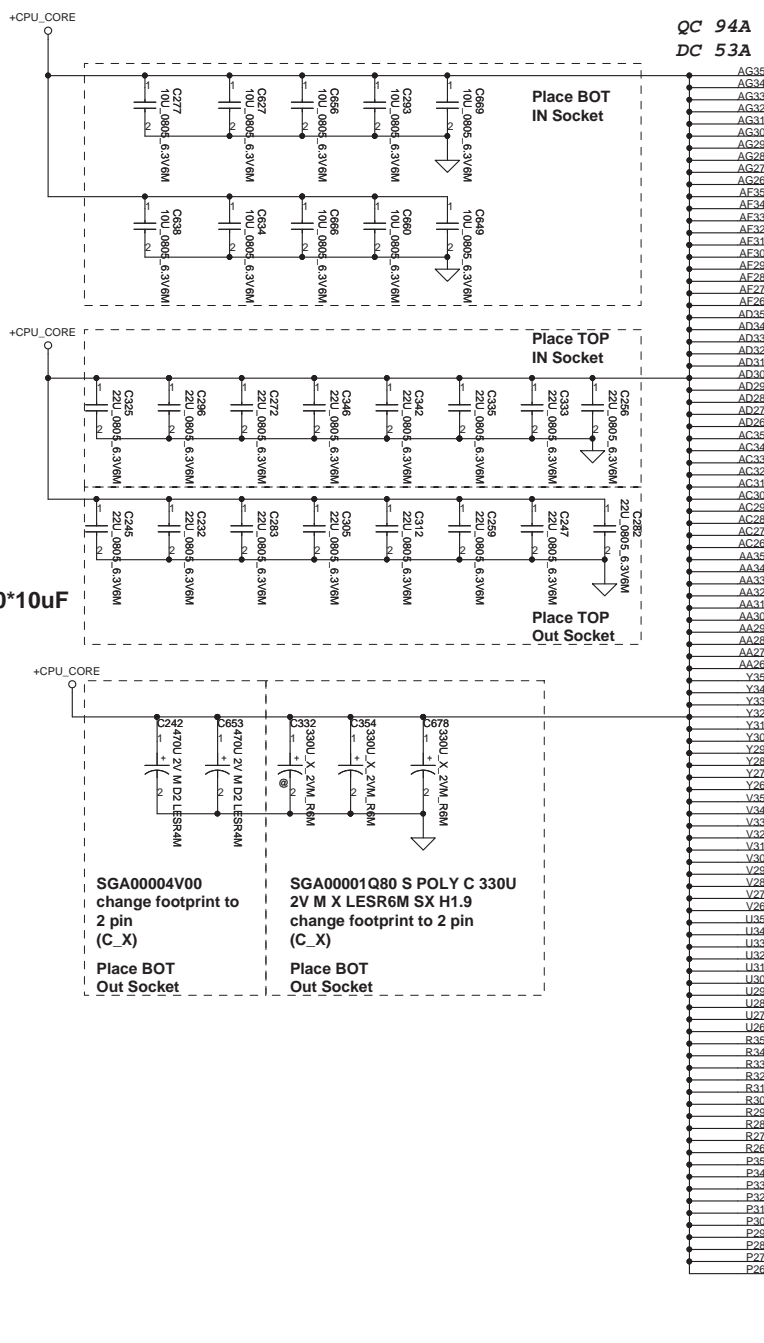


PEG DEFER TRAINING CRB1.0 P.12	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training



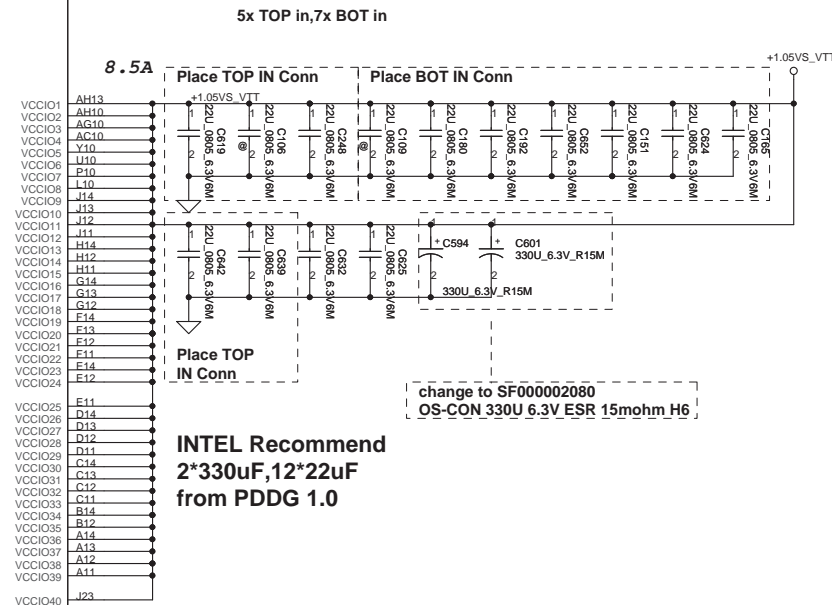
SV type CPU

POWER



- QC 94A
DC 53A
- AG35 VCC1
 - AG34 VCC2
 - AG33 VCC3
 - AG32 VCC4
 - AG31 VCC5
 - AG30 VCC6
 - AG29 VCC7
 - AG28 VCC8
 - AG27 VCC9
 - AG26 VCC10
 - AF35 VCC11
 - AF34 VCC12
 - AF33 VCC13
 - AF32 VCC14
 - AF31 VCC15
 - AF30 VCC16
 - AF29 VCC17
 - AF28 VCC18
 - AF27 VCC19
 - AF26 VCC20
 - AD35 VCC21
 - AD34 VCC22
 - AD33 VCC23
 - AD32 VCC24
 - AD31 VCC25
 - AD30 VCC26
 - AD29 VCC27
 - AD28 VCC28
 - AD27 VCC29
 - AD26 VCC30
 - AC35 VCC31
 - AC34 VCC32
 - AC33 VCC33
 - AC32 VCC34
 - AC31 VCC35
 - AC30 VCC36
 - AC29 VCC37
 - AC28 VCC38
 - AC27 VCC39
 - AC26 VCC40
 - AA35 VCC41
 - AA34 VCC42
 - AA33 VCC43
 - AA32 VCC44
 - AA31 VCC45
 - AA30 VCC46
 - AA29 VCC47
 - AA28 VCC48
 - AA27 VCC49
 - AA26 VCC50
 - VCC51
 - Y34
 - Y33
 - Y32
 - Y31
 - Y29
 - Y28
 - Y27
 - Y26
 - Y35
 - V34
 - V33
 - V32
 - V31
 - V30
 - VCC60
 - V29
 - V28
 - V27
 - V26
 - VCC70
 - U35
 - U34
 - U33
 - U32
 - U31
 - U30
 - U29
 - U28
 - U27
 - U26
 - R35
 - R34
 - R33
 - R32
 - R31
 - R30
 - R29
 - R28
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 - P28
 - P27
 - P26

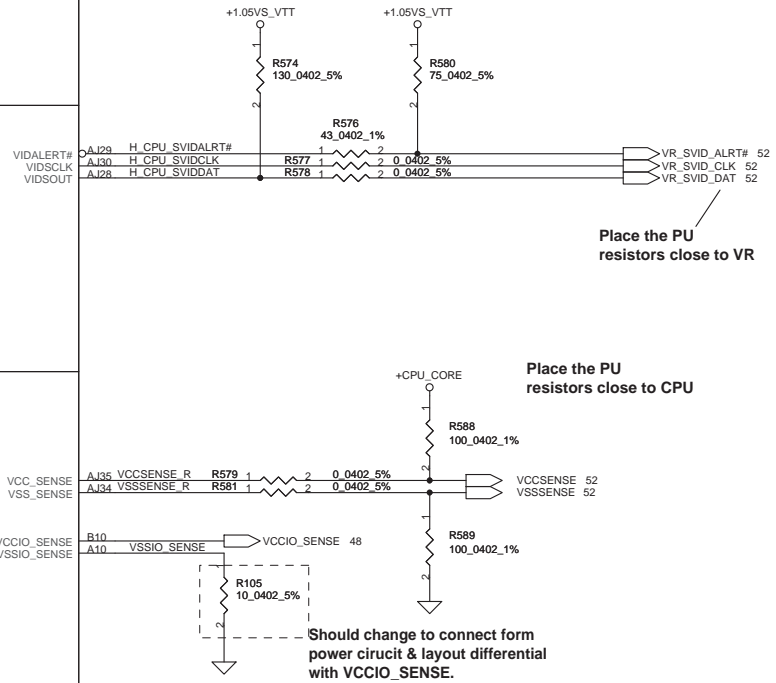
PEG AND DDR



CORE SUPPLY

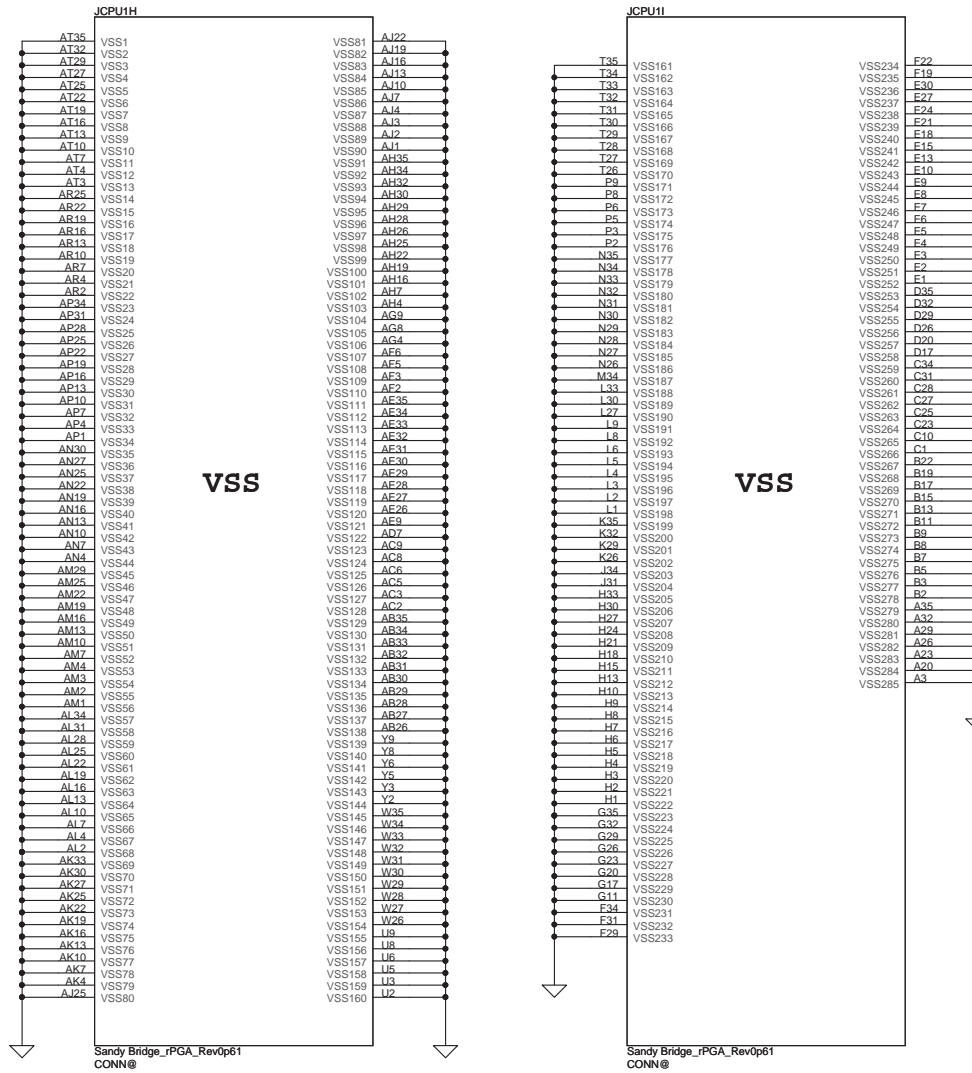
SVID

SENSE LINES

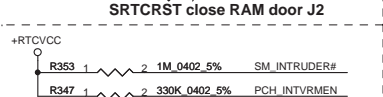
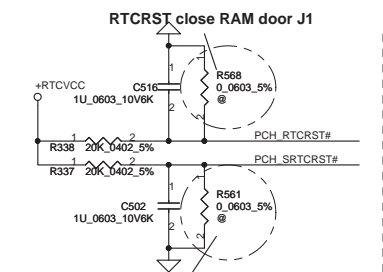


Sandy Bridge_rPGA_Rev0p61

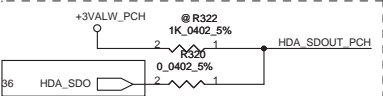
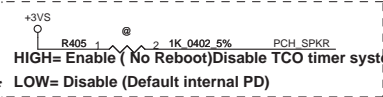
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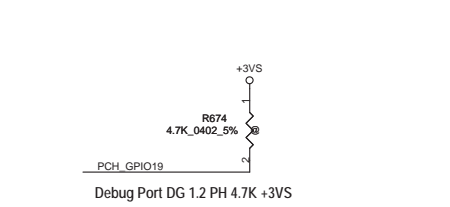
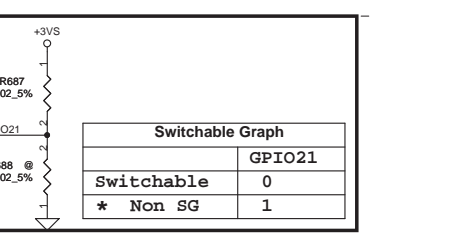
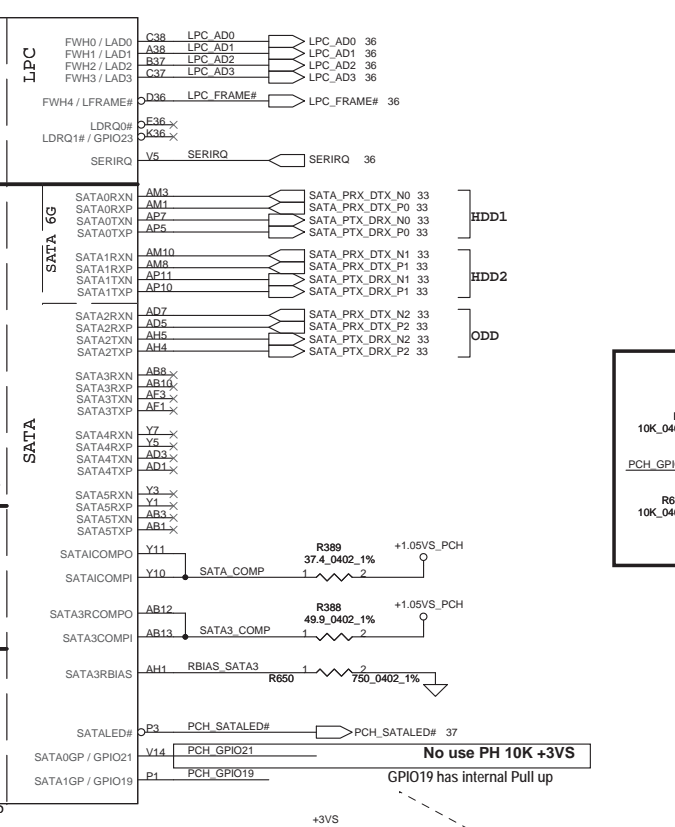
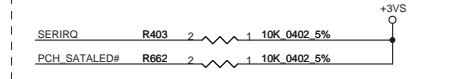
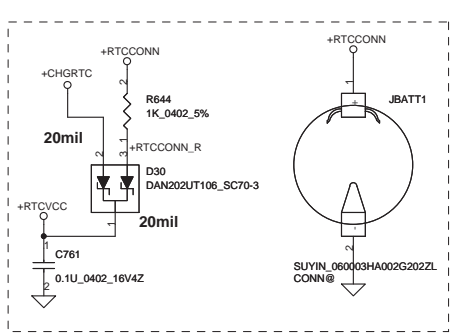
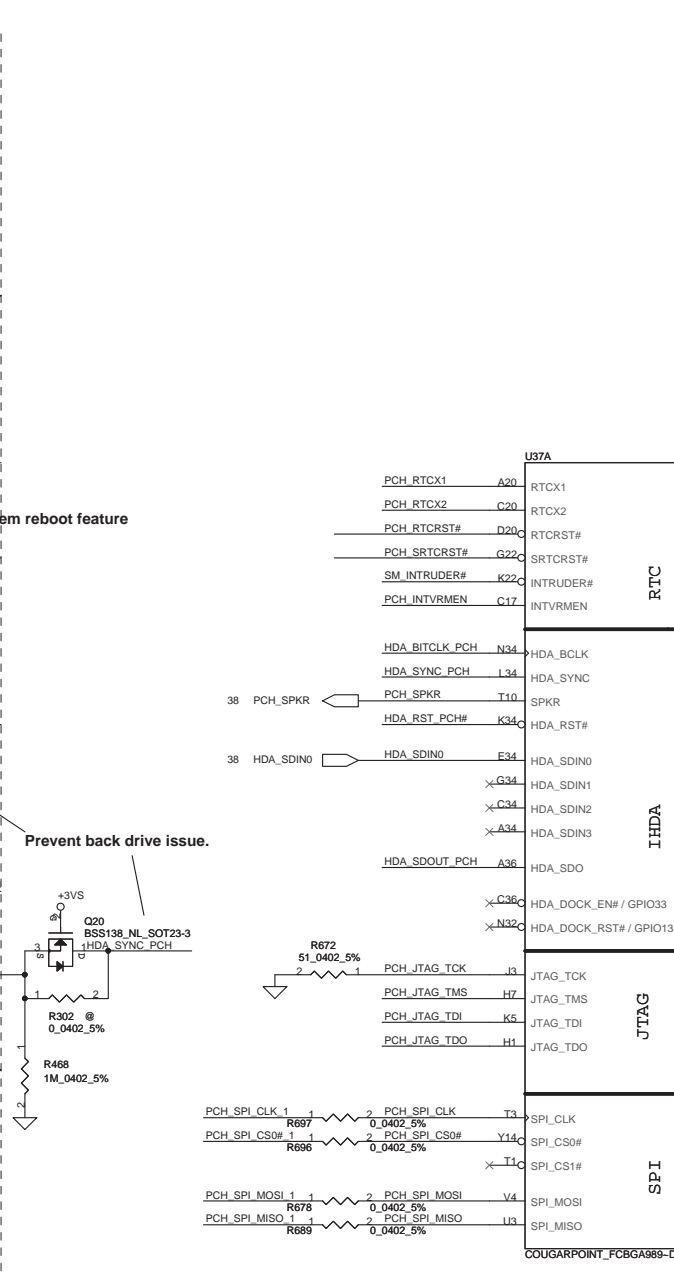
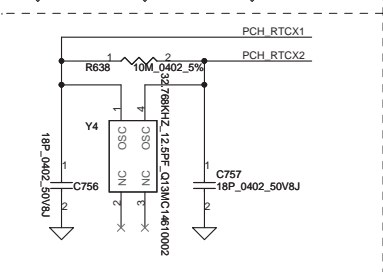
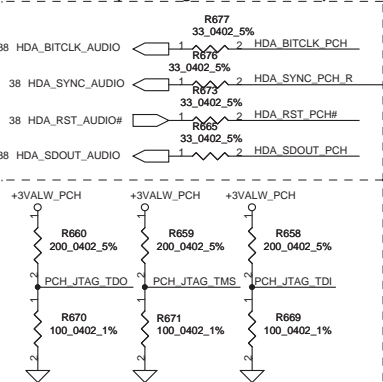
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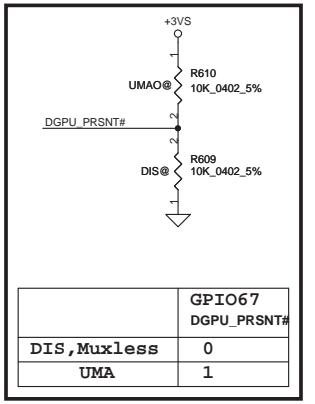
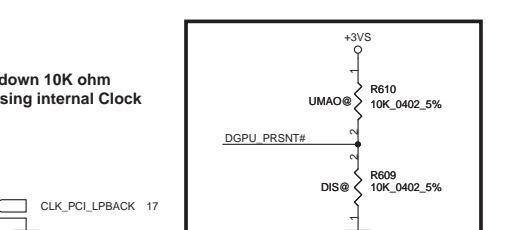
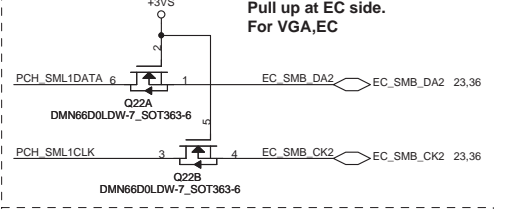
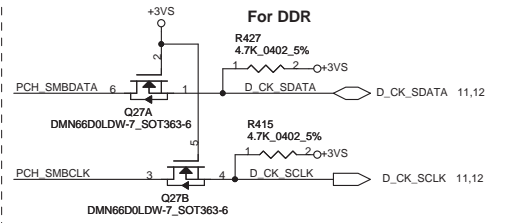
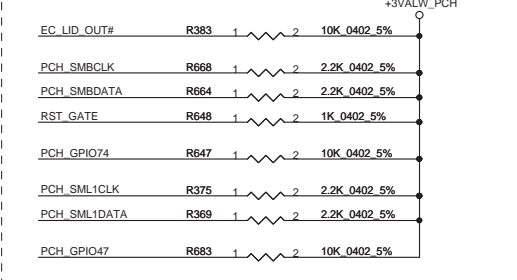
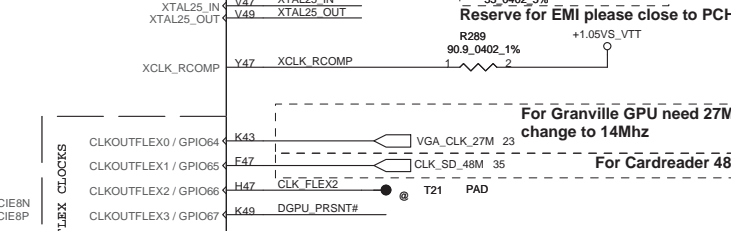
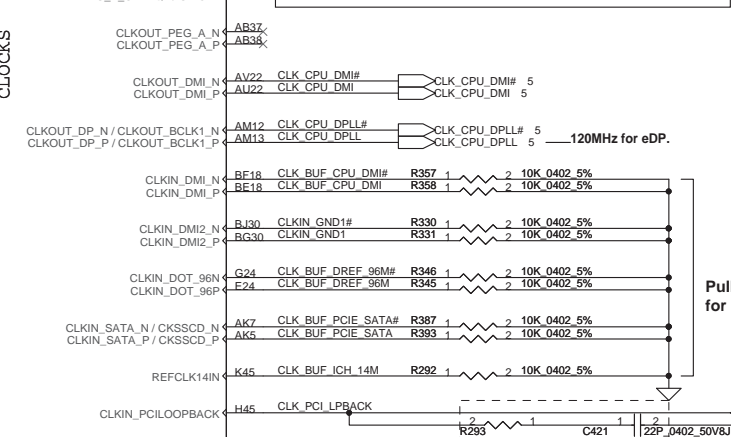
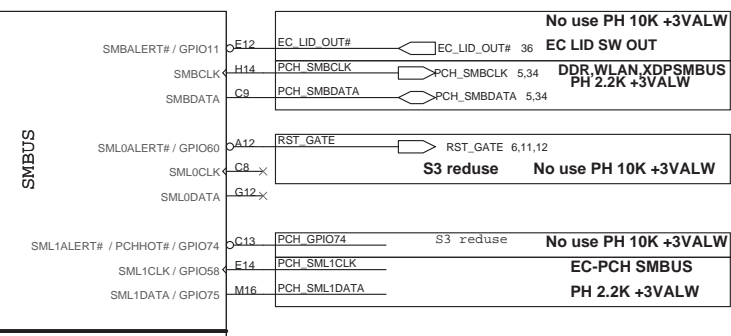
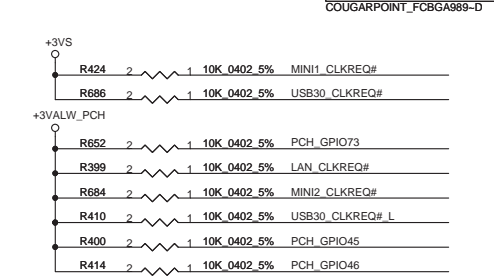
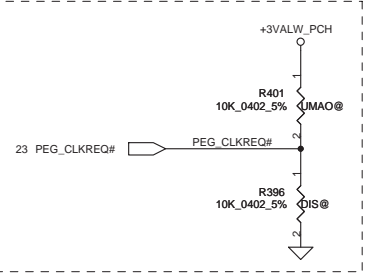
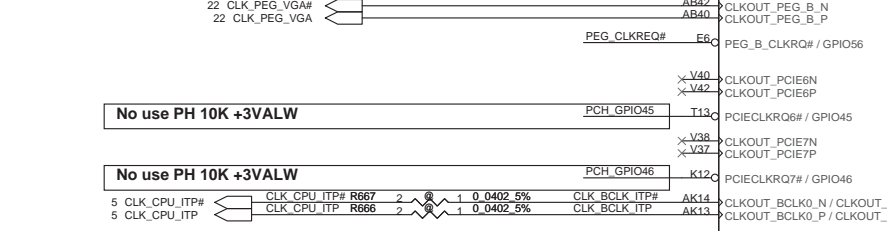
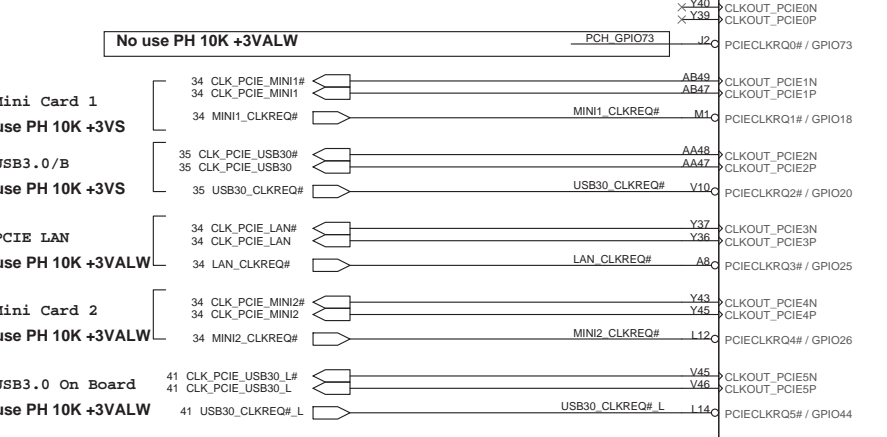
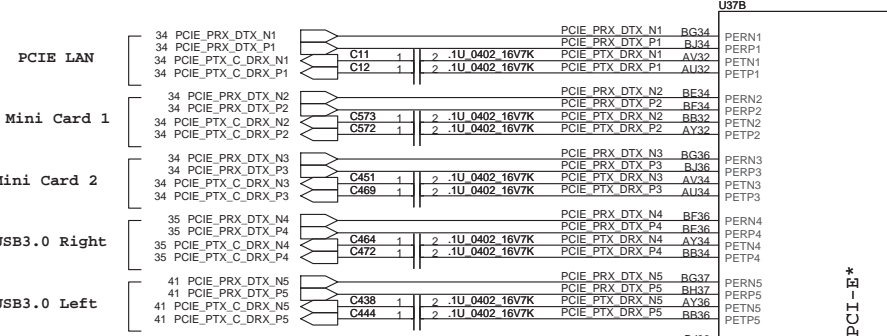
INTVRMEN
 * H : Integrated VRM enable
 L : Integrated VRM disable
 (INTVRMEN should always be pull high.)



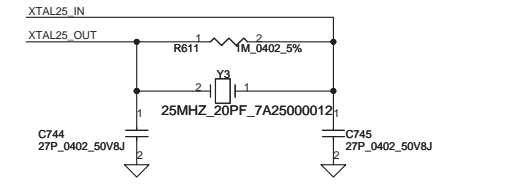
On Die PLL VR Select is supplied by
 *1.5V when sampled high
 1.8V when sampled low
 Needs to be pulled High for Huron River platform



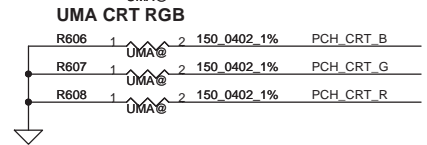
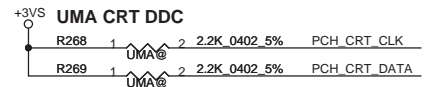
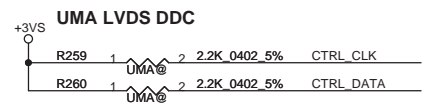
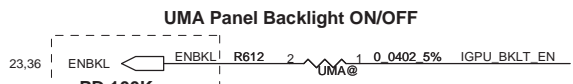
Boot BIOS Strap		
Boot BIOS	GPIO51	GPIO19
LPC	0	0
Reserved	0	1
-	1	0
* SPI	1	1



	GPIO67 DGPU_PRNST#
DIS, Muxless	0
UMA	1



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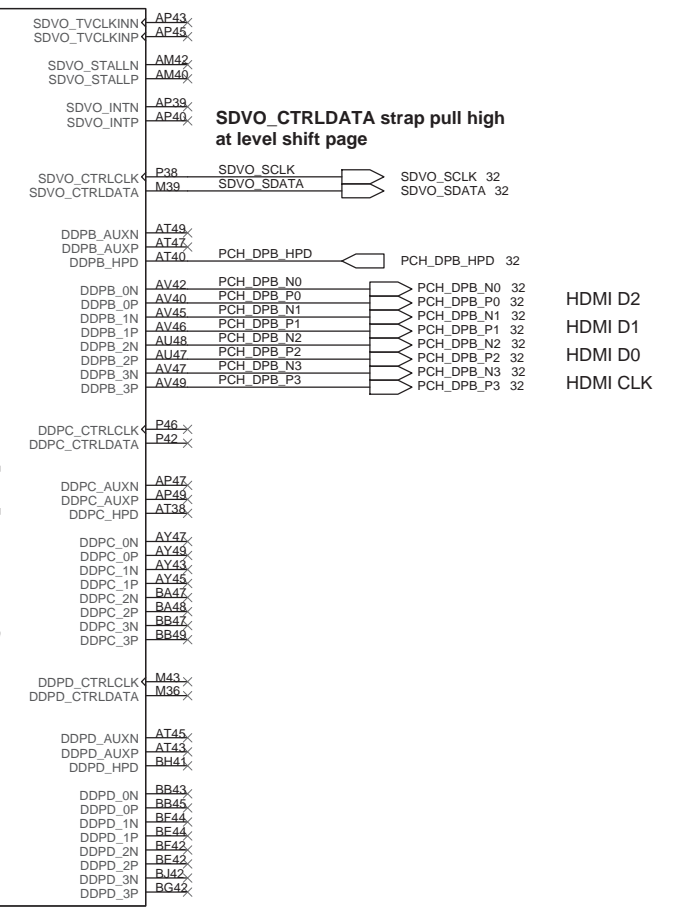
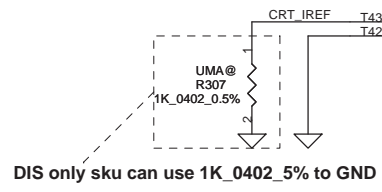
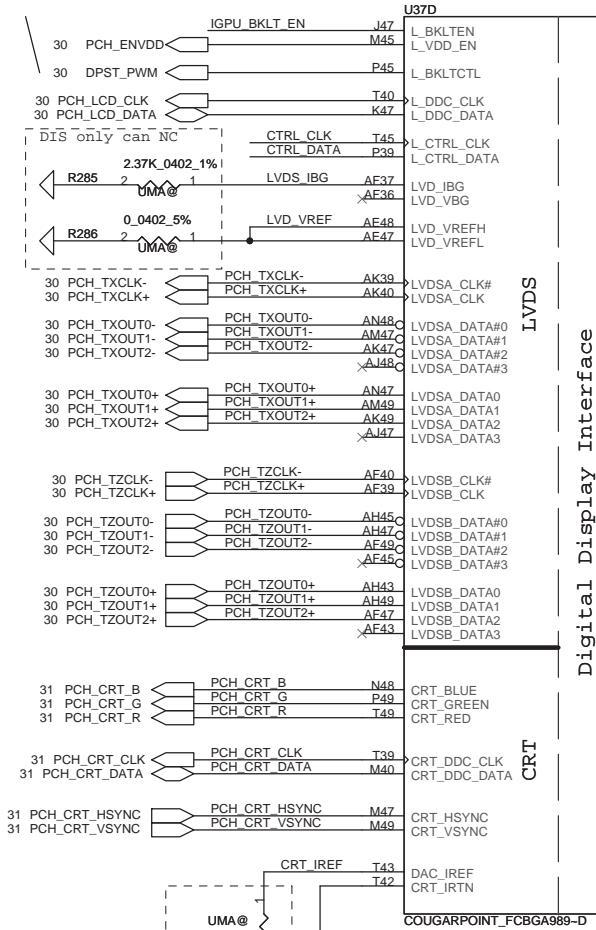


Check list1.0 P.55 disable Graphics
ALL Can NC
but DAC_IREF still need PD

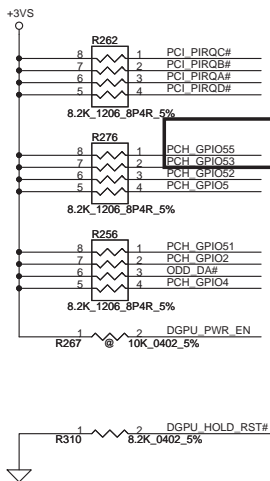
LVDS disable:
DATA/Clock/Control an NC
VCC_TX_LVDS,VCCA_LVDS PD to GND

CRT disable:
DATA/Clock/Control an NC
VCCADAC connect to +3VS

Pull high at LVDS conn side.



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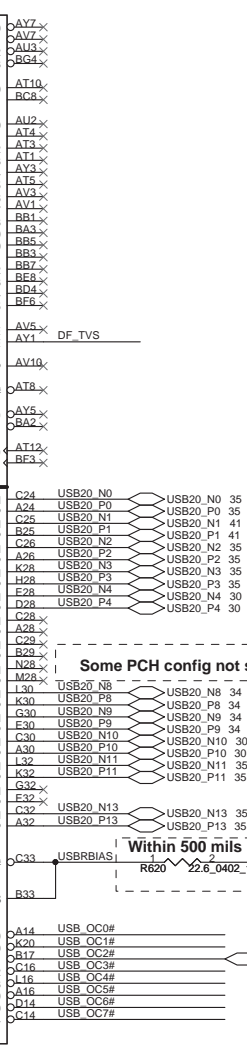
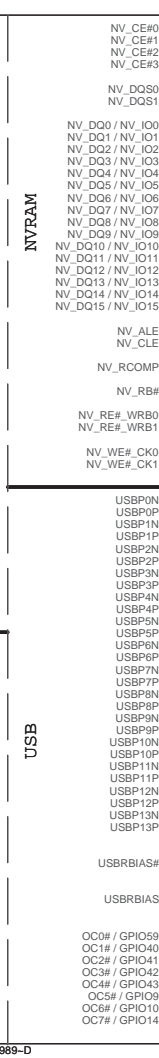
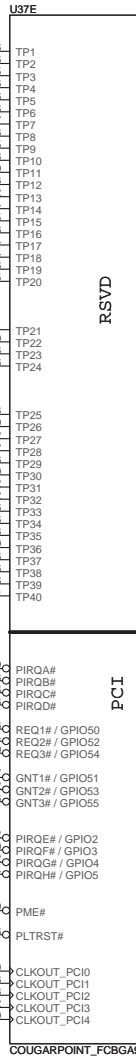
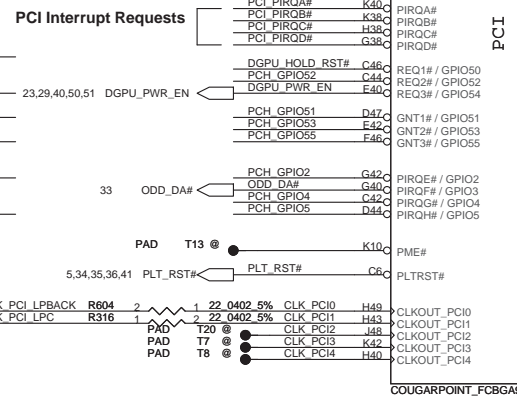
可以不用PH,如做GPIO使用PH+3VS

Boot BIOS Strap			
GNT1#/ GPIO51	GPIO19 GPIO51 Boot BIOS		Destination
	Bit11	Bit10	
Internal	0	1	Reserved
PH	1	0	PCI *
	0	0	SPI
	1	1	LPC

Only GPIO function

只剩GPIO的功能没有strap function
不做GPIO要PH +3VS,如做GPIO PH +3VS

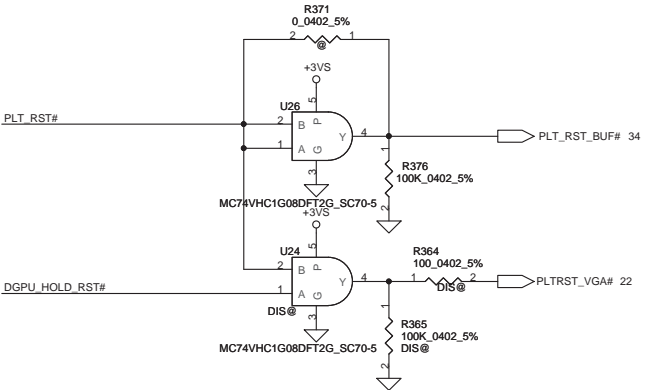
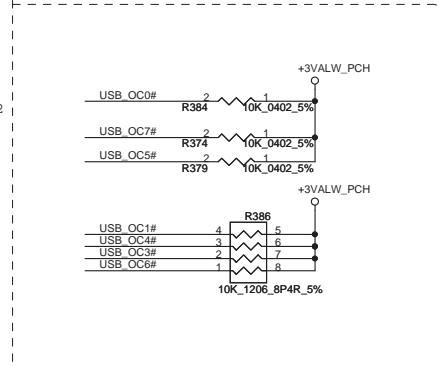
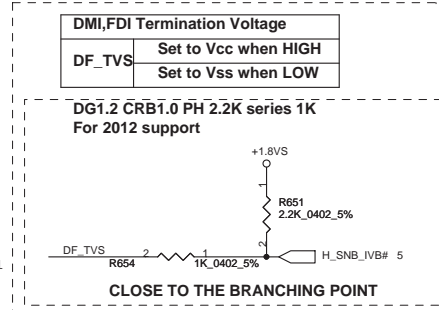
只剩GPIO的功能没有strap function
無須PH(Internal PH),如做GPIO PH +3VS



USB2/B (Right side)
USB2/B (Right side)
USB Port (Left side)
USB3/B (right side)
3D Panel

Some PCH config not support USB port 6 & 7.

Mini Card (WLAN)
Mini Card (WWAN)
CMOS Camera (LVDS)
Card Reader
Mini Card (SIM card)
Bluetooth



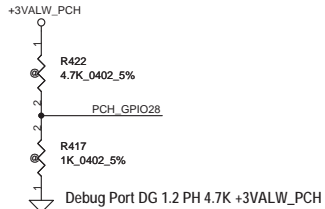
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HDA_SYNC PH(PLL =+1.5VS)

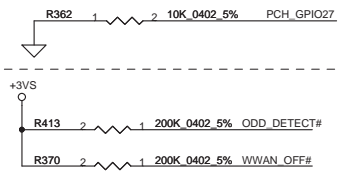
GPIO28

On-Die PLL Voltage Regulator

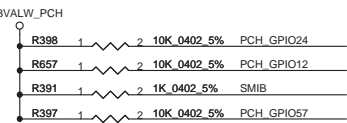
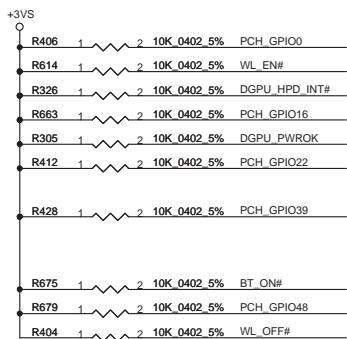
This signal has a weak internal pull up
 * H : On-Die PLL voltage regulator enable
 L : On-Die PLL Voltage Regulator disable



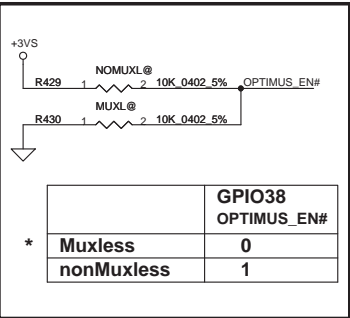
Deep S4,S5 wake event signal
 RTC alarm,Power BTN,GPIO27
 PCH_GPIO27 (Have internal Pull-High)
 Deep S4,S5 wake event signal
 No use PD to GND Check list1.0 P.70



SATA2GP/GPIO36 & SATA3GP/GPIO37
 Sampled at Rising edge of PWROK.
 Weak internal pull-down.
 (weak internal pull-down is disabled after PLTRST# de-asserts)
 NOTE: This signal should NOT be pulled high when strap is sampled

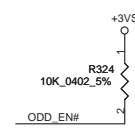


No use PH 10K +3VS	PCH_GPIO0	TZ
No use PH 10K +3VS	35 WL_EN#	A42
No use PH 10K +3VS	32 DGPU_HPD_INT#	H36
	36 EC_SCI#	E38
	36 EC_SMI#	C10
No use PH +3VALW	PCH_GPIO12	C4
USB3.0 System management Interrupt signal "SMI#".	35,41 SMIB	G2
No use PH +3VS	PCH_GPIO16	U2
	29,49 VGA_PWROK	R304
No use PH 10K +3VS	PCH_GPIO22	T5
CRB1.0 PH 10K +3VALW	PCH_GPIO24	E8
No use PD 10K to GND	PCH_GPIO27	E16
No use PH 10K +3VALW	PCH_GPIO28	P8
No use PH 10K +3VS BT ON/OFF	34,35 BT_ON#	K4
No use can NC	PAD T16 @	K4
Can't PH	33 ODD_DETECT#	V8
Can't PH	34 WWAN_OFF#	M5
No use PH 10K +3VS Optimus(L)/ non optimus(H)	OPTIMUS_EN#	N2
No use PH 10K +3VS	PCH_GPIO39	M3
No use PH 10K +3VS	PCH_GPIO48	V13
SATA5GP&TEMP_ALERT# CRB PH 10K +3VS WL_OFF#	WL_OFF#	V3
No use PH +3VALW or PD to GND	PCH_GPIO57	D6

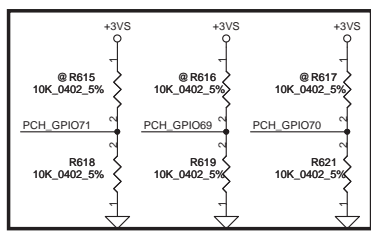


	GPIO38 OPTIMUS_EN#
* Muxless	0
nonMuxless	1

GPIO24 Unmultiplexed
 NOTE: GPIO24 configuration register bits are not cleared by CF9h reset event.
 CRB1.0 PH10K to +3VALW

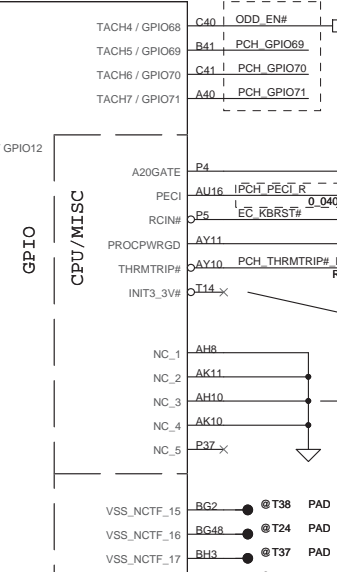


Fan Tachometer Inputs
 TACH1-7 only on server can insted to GPIO



Project ID	GPIO69	GPIO70	GPIO71
* P7YE0	0	0	0
X	0	0	1
X	0	1	0
X	0	1	1
X	1	0	0
X	0	0	1
X	0	1	0
X	0	1	1
X	1	0	0
X	1	0	1
X	1	1	0
X	1	1	1

U37F	Signal	Pin
	BMBUSY# / GPIO0	TACH4 / GPIO68
	TACH1 / GPIO1	TACH5 / GPIO69
	TACH2 / GPIO6	TACH6 / GPIO70
	TACH3 / GPIO7	TACH7 / GPIO71
	GPIO8	
	LAN_PHY_PWR_CTRL / GPIO12	
	GPIO15	
	SATA4GP / GPIO16	
	TACH0 / GPIO17	
	SCLOCK / GPIO22	
	GPIO24 / MEM_LED	
	GPIO27	
	GPIO28	
	STP_PC# / GPIO34	
	GPIO35	
	SATA2GP / GPIO36	
	SATA3GP / GPIO37	
	SLOAD / GPIO38	
	SDATAOUT0 / GPIO39	
	SDATAOUT1 / GPIO48	
	SATA5GP / GPIO49	
	GPIO57	

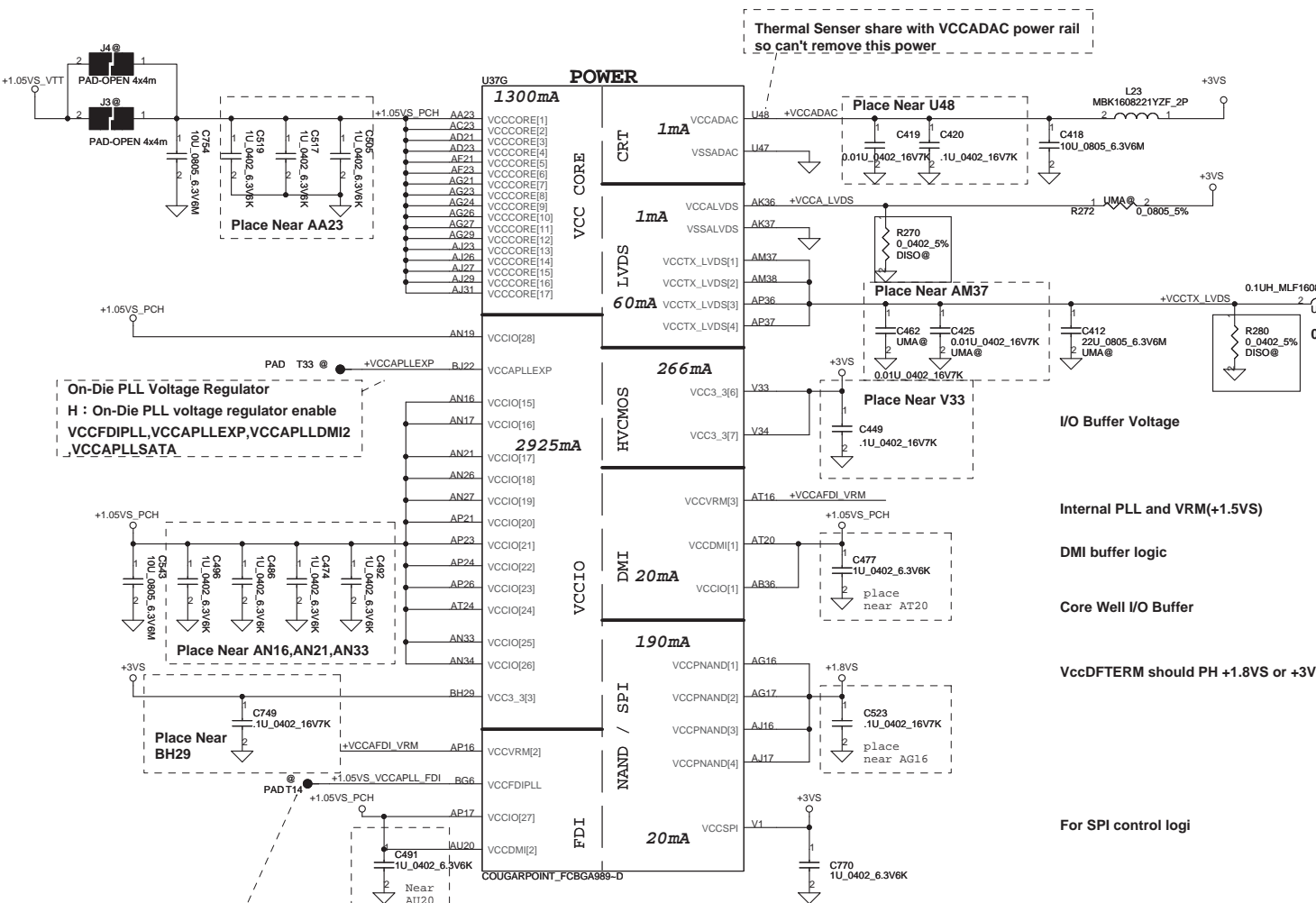


INIT3_3V Checklist1.0 P.59
 This signal has weak internal PU, can't pull low,leave NC

PECI CPU-EC
 CTRL+ALT+DEL non CPU power ok
 130c shut sown

PAD T47 @	A4	VSS_NCTF_1
PAD T30 @	A44	VSS_NCTF_2
PAD T28 @	A45	VSS_NCTF_3
PAD T27 @	A46	VSS_NCTF_4
PAD T49 @	A5	VSS_NCTF_5
PAD T46 @	A6	VSS_NCTF_6
PAD T50 @	B3	VSS_NCTF_7
PAD T26 @	B47	VSS_NCTF_8
PAD T43 @	BD1	VSS_NCTF_9
PAD T17 @	BD49	VSS_NCTF_10
PAD T44 @	BE1	VSS_NCTF_11
PAD T23 @	BE49	VSS_NCTF_12
PAD T45 @	BE1	VSS_NCTF_13
PAD T18 @	BF49	VSS_NCTF_14

COUGARPOINT_FCBGA989-D



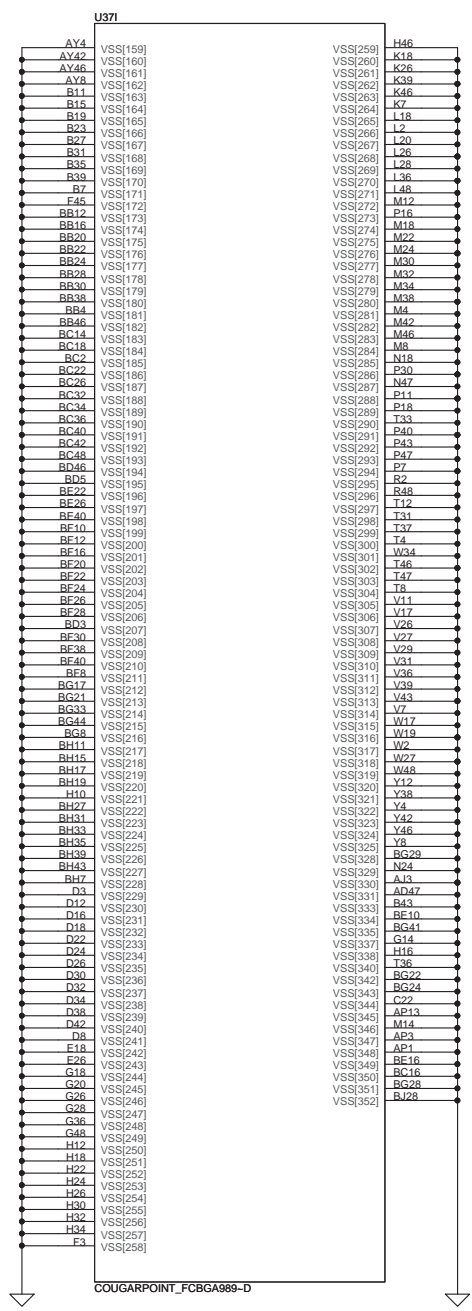
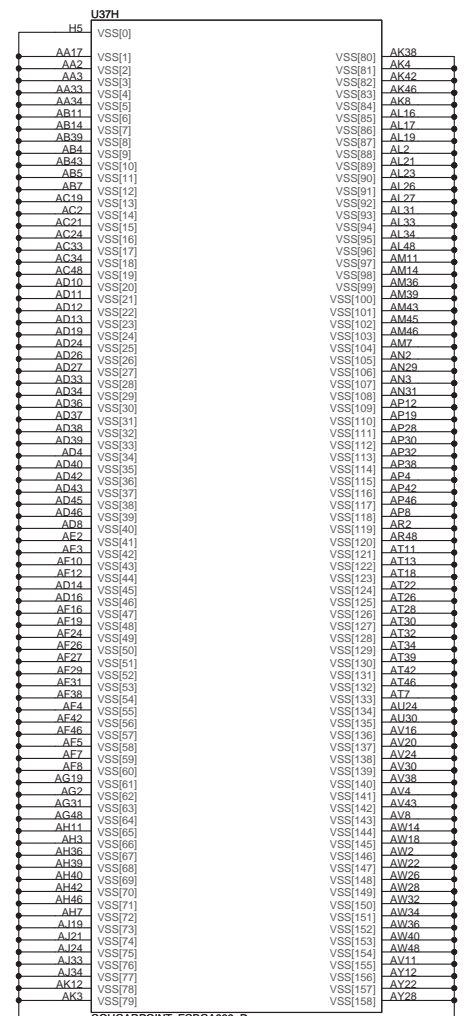
On-Die PLL Voltage Regulator
 H : On-Die PLL voltage regulator enable
 VCCFDIPLL, VCCAPLLEXP, VCCAPLLDMI2, VCCAPLLSATA

On-Die PLL Voltage Regulator
 H : On-Die PLL voltage regulator enable
 VCCFDIPLL, VCCAPLLEXP, VCCAPLLDMI2, VCCAPLLSATA

VCCVRM==>1.5V FOR MOBILE
 VCCVRM==>1.8V FOR DESKTOP
 VCCVRM = 160mA detal waiting for newest spec
 HDA_SYNC PH(PLL =+1.5VS)

Voltage Rail	Voltage	S0 Iccmax Current(A)	
V_PROC_IO	1.05	0.001	Processor I/F
V5REF	5	0.001	PCH Core Well Reference Voltage
V5REF_Sus	5	0.001	Suspend Well Reference Voltag
Vcc3_3	3.3	0.266	I/O Buffer Voltage
VccADAC	3.3	0.001	Display DAC Analog Power. This power is supplied by the core well.
VccADPLLA	1.05	0.08	Display PLL A power
VccADPLLB	1.05	0.08	Display PLL B power
VccCore	1.05	1.3	Internal Logic Voltage
VccDMI	1.05	0.042	DMI Buffer Voltage
VccIO	1.05	2.925	Core Well I/O buffers
VccASW	1.05	1.01	1.05 V Supply for Intel R Management Engine and Integrated LAN
VccSPI	3.3	0.02	3.3 V Supply for SPI Controller Logic
VccDSW	3.3	0.003	3.3v supply for Deep S4/S5 well
VccpNAND	1.8	0.19	1.8V power supply for DF_TV5
VccRTC	3.3	6 uA	Battery Voltage
VccSus3_3	3.3	0.266	Suspend Well I/O Buffer Voltage
VccSusHDA	3.3 / 1.5	0.01	High Definition Audio Controller Suspend Voltage
VccVRM	1.8 / 1.5	0.16	1.8 V Internal PLL and VRMs (1.8 V for Desktop)
VccCLKDMI	1.05	0.02	DMI Clock Buffer Voltage
VccSSC	1.05	0.095	Spread Modulators Power Supply
VccDIFFCLKN	1.05	0.055	Differential Clock Buffers Power Supply
VccALVDS	3.3	0.001	Analog power supply for LVDS (Mobile Only)
VccTX_LVDS	1.8	0.06	Analog power supply for LVDS (Mobile Only)

I/O Buffer Voltage
 Internal PLL and VRM(+1.5VS)
 DMI buffer logic
 Core Well I/O Buffer
 VccDFTERM should PH +1.8VS or +3VS
 For SPI control logi

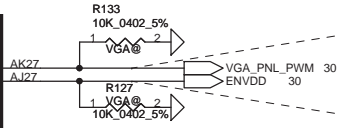
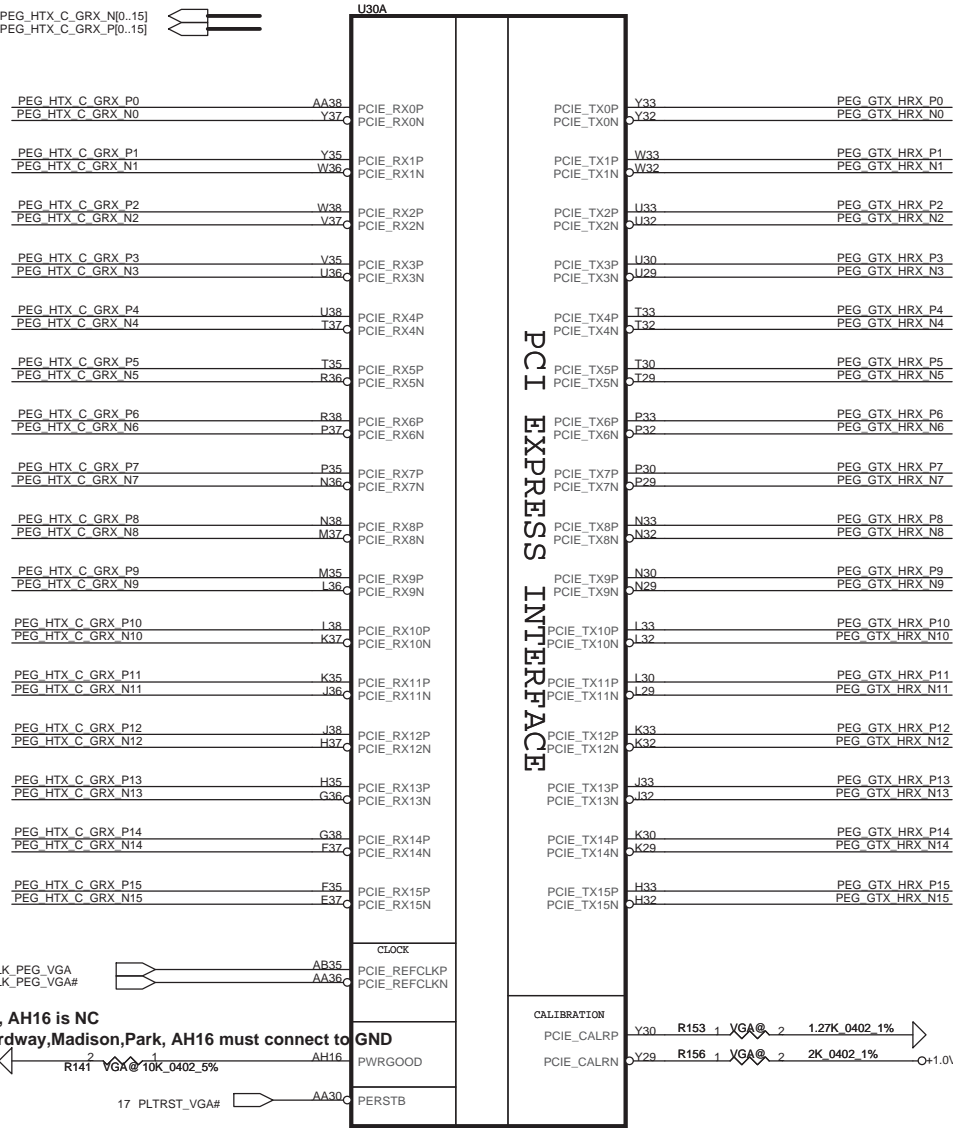


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GFX PCIE LANE REVERSAL

4 PEG_GTX_HRX_N[0..15]
4 PEG_GTX_HRX_P[0..15]

4 PEG_HTX_C_GRX_N[0..15]
4 PEG_HTX_C_GRX_P[0..15]



LCD PWM (pulse width modulated) output to adjust LCD brightness Active High ,external PD need

Controls panel digital power on/off. Active High ,external PD need

Display Port F config

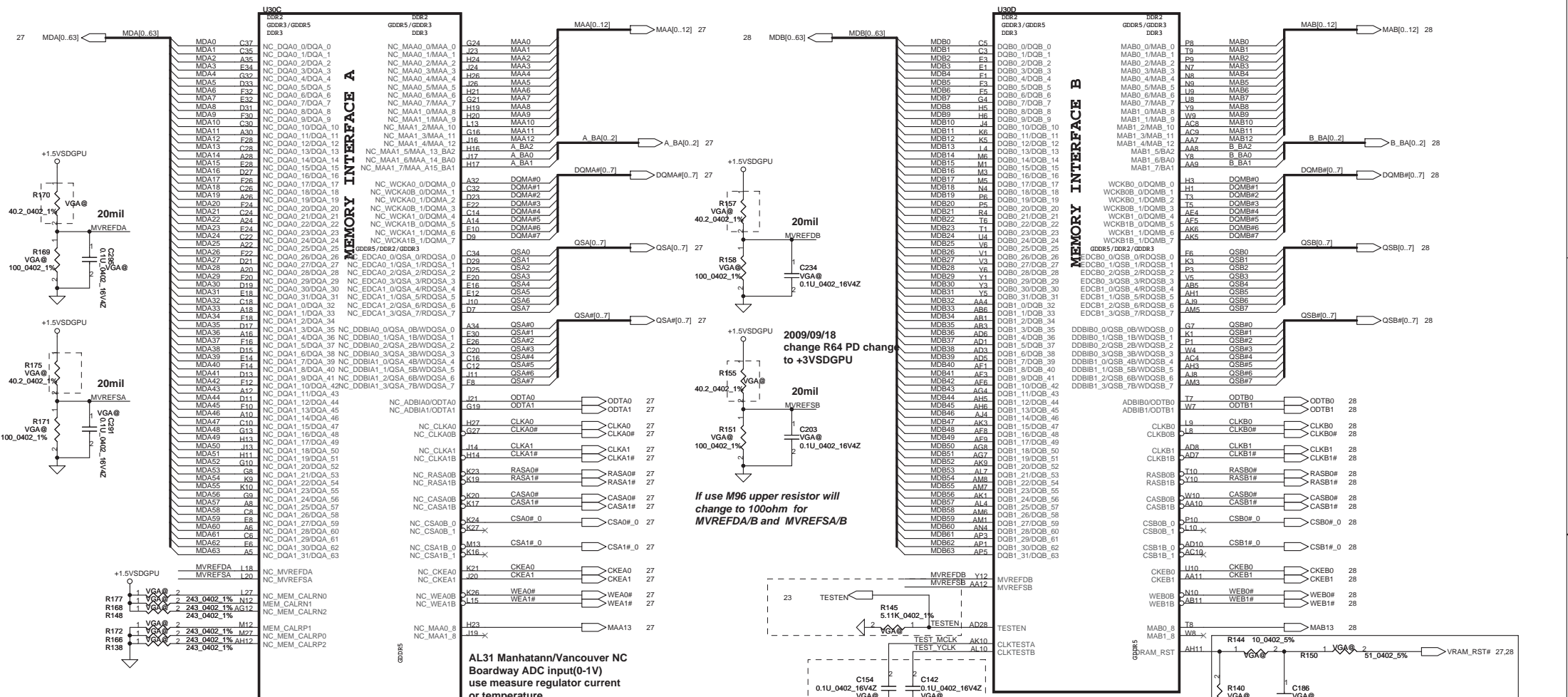
Display Port E config

eDP
DP3
DP2
DP1
DP0

For M96, AH16 is NC
For Boardway, Madison, Park, AH16 must connect to GND

SEYMOUR
Park XT P/N : SA00003M570 (S IC 216-0774009 A11 PARK XT S3 631P C38)
Madison Pro P/N : SA00003M360 (S IC 216-0772000 MADISON PRO FCBGA 0FA)
Seymour XT P/N: SA000047H00 (S IC 216-0809000 A11 SEYMOUR XT M2 0FH)

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				Document Number	B
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				Date:	Tuesday, November 09, 2010
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MEMORY INTERFACE A

MEMORY INTERFACE B

AL31 Manhattan/Vancouver NC Boardway ADC input(0-1V) use measure regulator current or temperature

AG28: VDDC_SEN feedback path to regulator no use can CN AF28:VDDC_SEN feedback path to regulator no use can CN

In M97, Medison and Park, AF28 is FB_VDDC, AG28 is FB_VDDCI, AH29 is FB_GND, GCORE_SEN and FB_GND should route as differential pair Same as VDDC_SEN and FB_GND

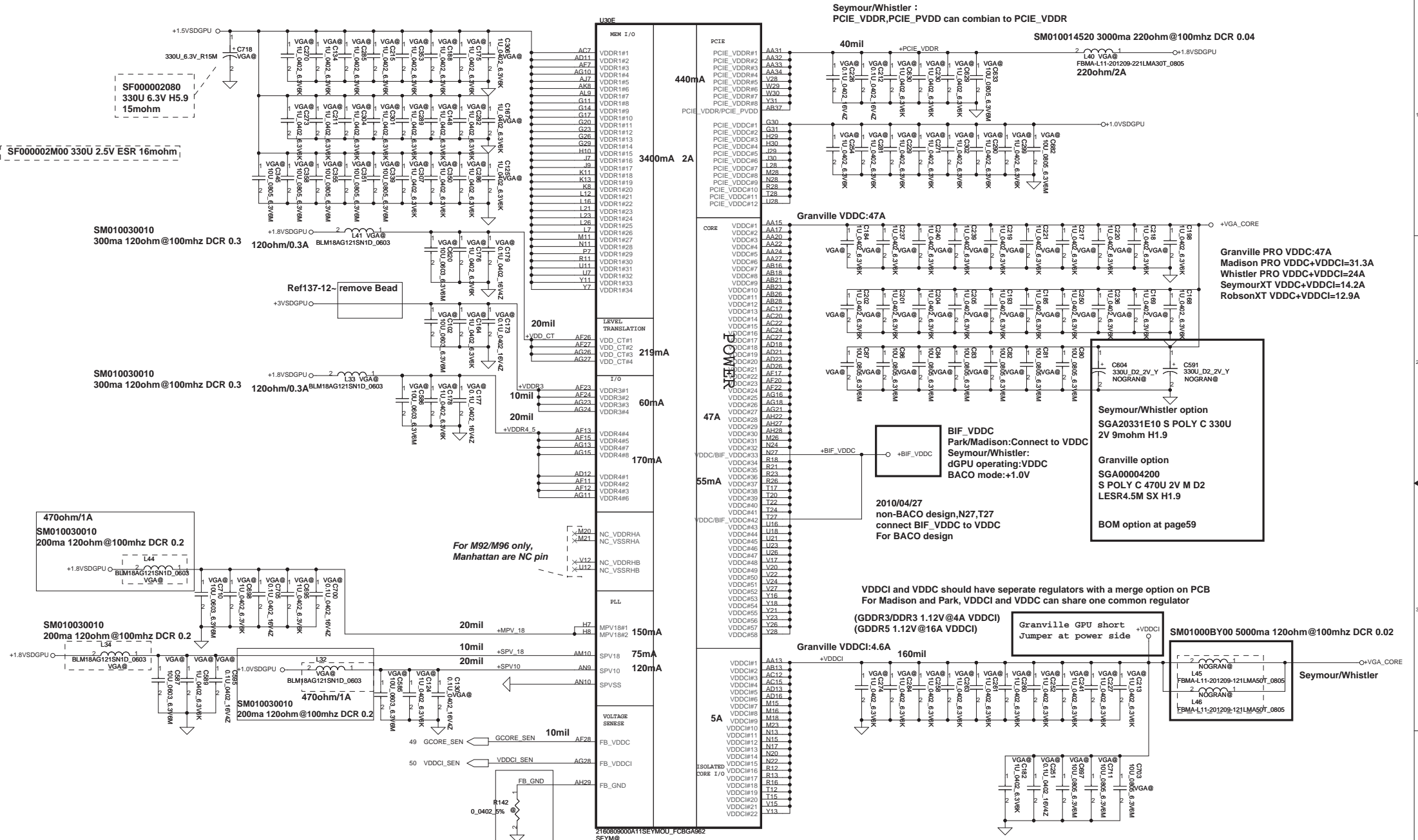
If use M96 upper resistor will change to 100ohm for MVREFDA/B and MVREFSA/B

M96 use 4.7K to PD directly.

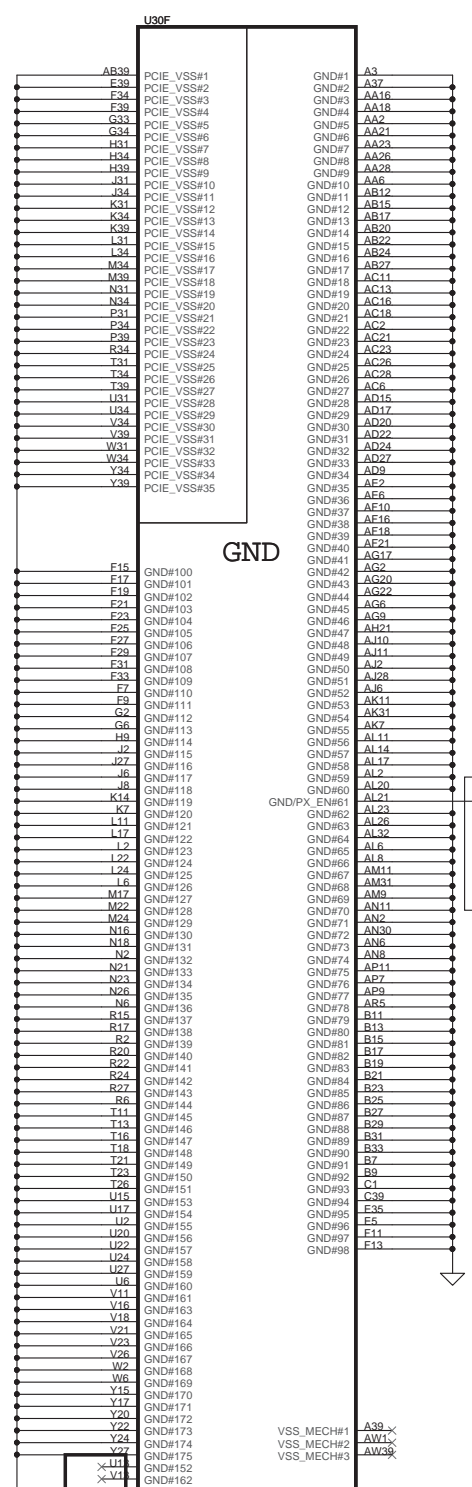
Seymour is single channel for memory (channel B only)

Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within5mm) except Rser2

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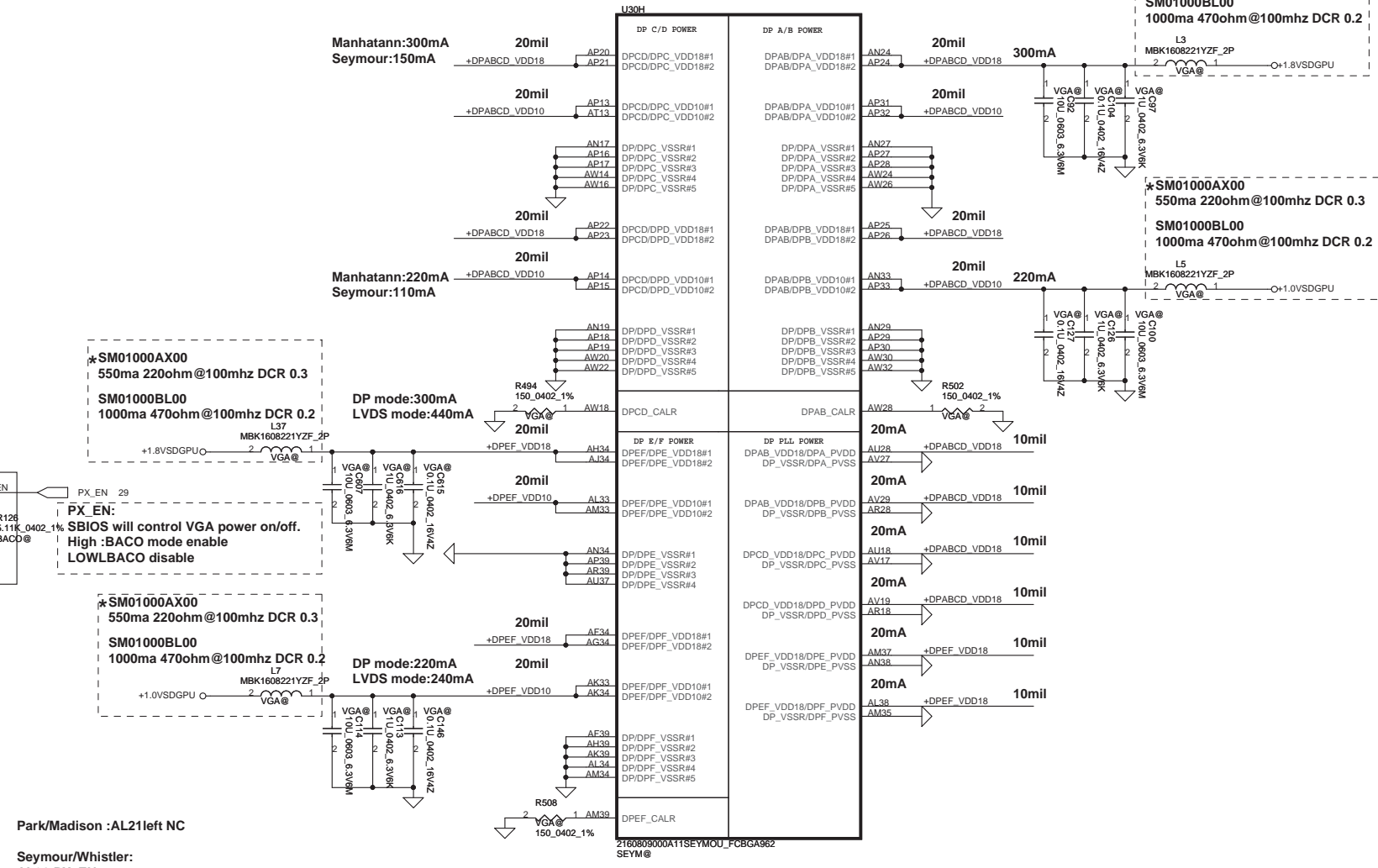


2160809000A11SEYMOU_FCBGA962
SEYM@
REF137-13 update

DPA_VDD18,DPA_PVDD,DPB_VDD18,DPB_PVDD
can combian to DPAB_VDD18
DPC_VDD18,DPC_PVDD,DPD_VDD18,DPD_PVDD
can combian to DPCD_VDD18
(DPD_VDD18,DPD_PVDD not applicable on Robson/Park)
DPE_VDD18,DPE_PVDD,DPF_VDD18,DPF_PVDD
can combian to DPEF_VDD18

DPx-VSSR,DPx_PVSS can combian to DP_VSSR
(Manhattan should have individual GND)
where x is A,B,C,D,E,F

Seymour/Whistler :
DPA_VDD10,DPB_VDD10
can combian to DPAB_VDD10
DPC_VDD10,DPD_VDD10
can combian to DPCD_VDD10
DPE_VDD10,DPD_VDD10
can combian to DPEF_VDD10

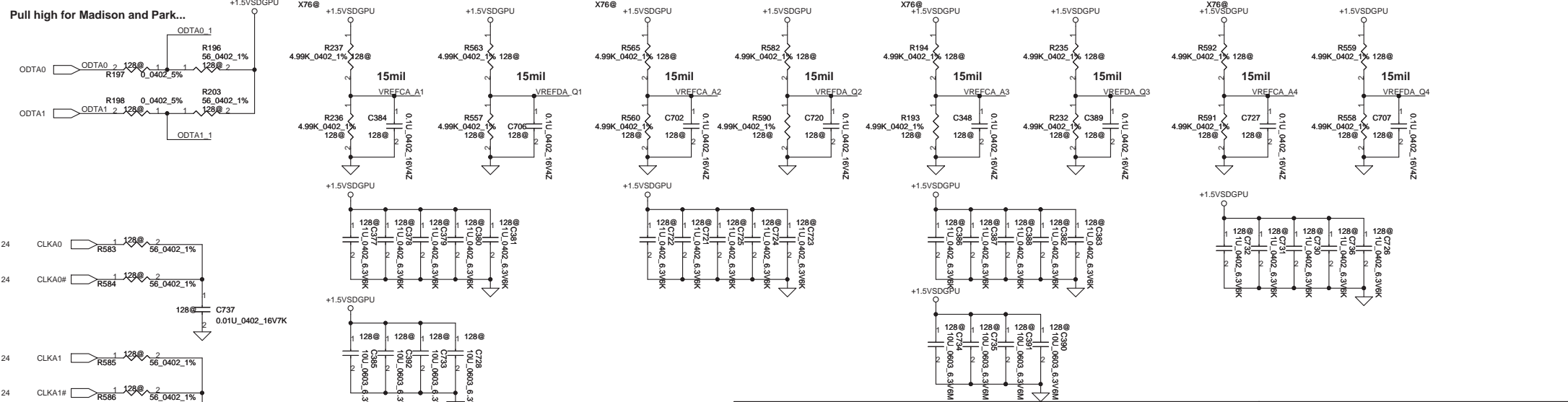
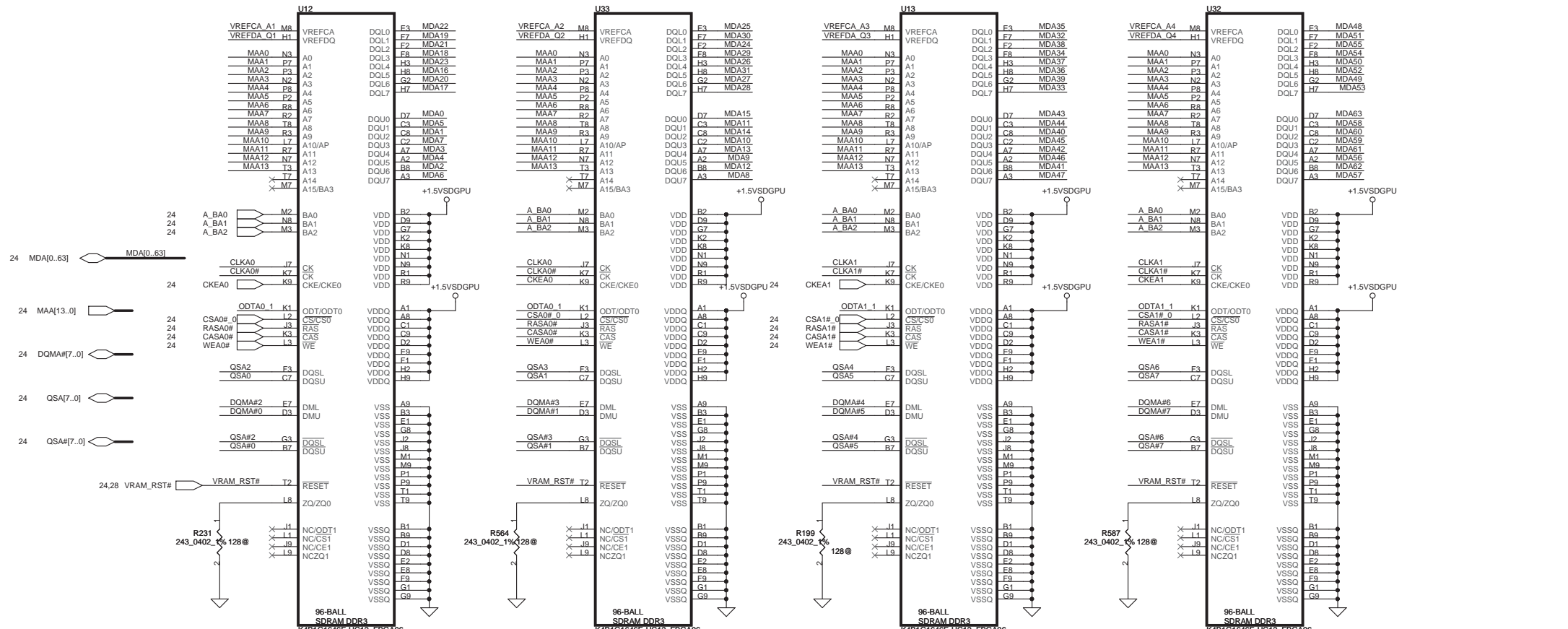


Park/Madison :AL21:left NC

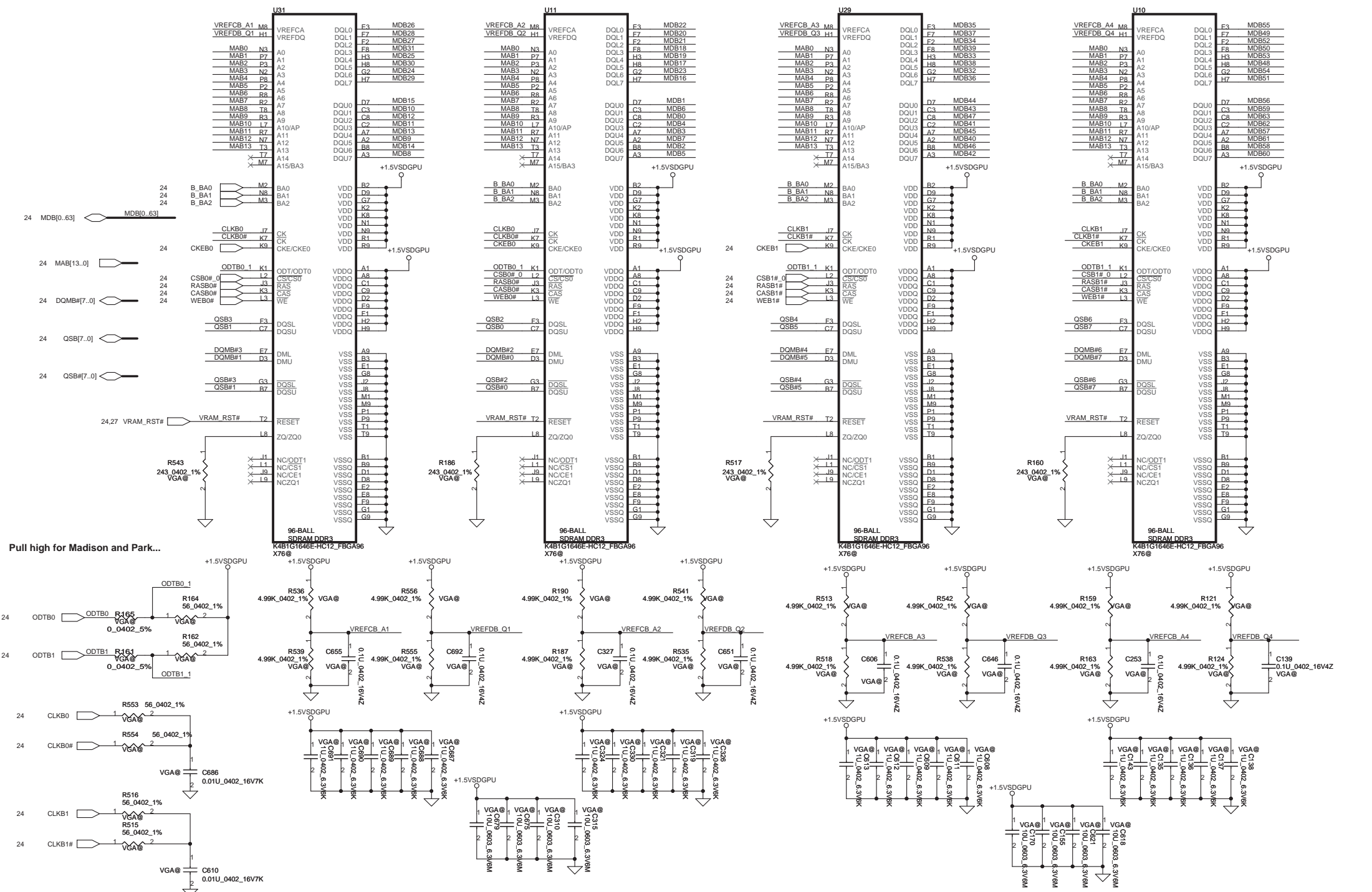
Seymour/Whistler:
AL21:PX_EN
use to control discrete GPU regulators
for power express BACO mode
Support BACO:
output High3.3V:turn off regulators (BACO mode on)
output Low0V:turn on regulators (BACO mode off)
need PD resistor
No support BACO:
left NC

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				Seymour/Whistler : DPA_VDD10,DPB_VDD10 can combian to DPAB_VDD10 DPC_VDD10,DPD_VDD10 can combian to DPCD_VDD10 DPE_VDD10,DPD_VDD10 can combian to DPEF_VDD10	
				Schematic, MB A6911	
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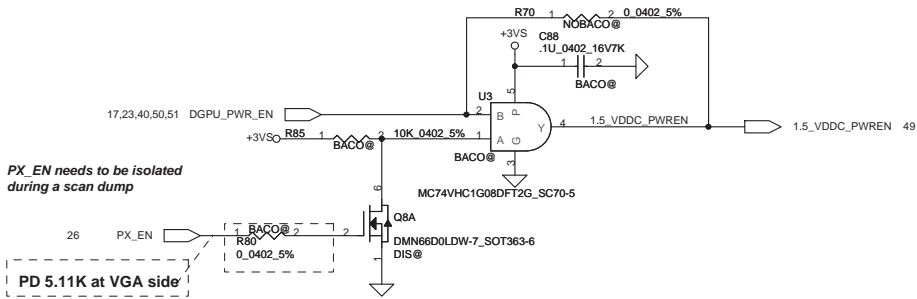


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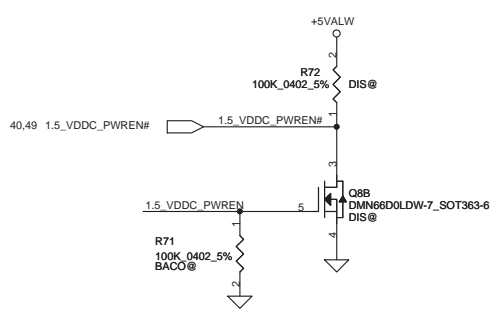
Pull high for Madison and Park...

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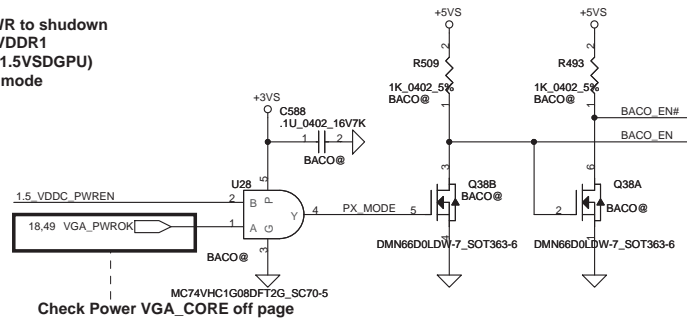


PX_EN = 1, For BACO Mode
 PX_EN = 0, For Normal Mode

PX_EN:
 Connect to PWR to shutdown
 VDDC/VDDCI/VDDR1
 (VGA_CORE,+1.5VSDGPU)
 High in BACO mode



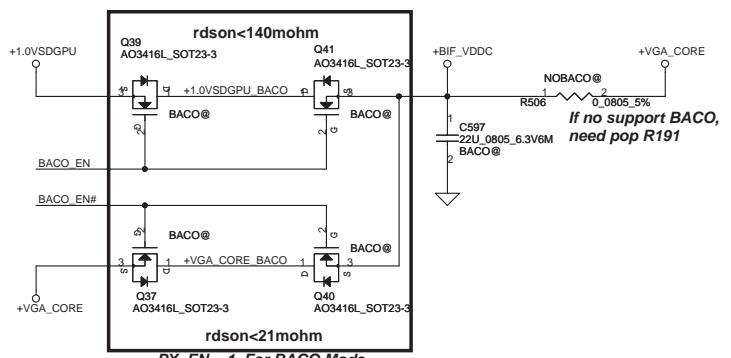
BACO_EN/BACO_EN#:
 0: BACO Mode->BACO_EN High->
 BIF_VDDC=>+1.0VSDGPU(N-MOS),VGA_CORE(P-MOS)
 1: Normal mode->BACO_EN# High->
 BIF_VDDC=>+VGA_CORE(N-MOS),VGA_CORE(N-MOS)



BACO_EN#=1 (BACO mode)
 BACO_EN#=0 (Normal mode)
 BACO_EN=0 (BACO mode)
 BACO_EN=1 (Normal mode)

VGA Status Mapping table		
	Normal mode	BACO mode
PX_EN	0	1
1.5_VDDC_PWREN	1	0
BACO_EN#	1	0
BACO_EN	0	1
+3VSDGPU	ON	ON
+1.8VSDGPU	ON	ON
+1.0VSDGPU	ON	ON
+VGA_CORE	ON	OFF
+1.5VSDGPU	ON	OFF
+BIF_VDDC	+VGA_CORE	+1.0VSDGPU

VGA Power Enable Signal Mapping table		
	Graville	Whistler and Seymour
+3VSDGPU	DGPU_PWR_EN	SUSP#
+1.8VSDGPU	DGPU_PWR_EN	DGPU_PWR_EN
+1.0VSDGPU	DGPU_PWR_EN	DGPU_PWR_EN
+VDDCI	DGPU_PWR_EN	Combine with +VGA_CORE
+VGA_CORE	DGPU_PWR_EN	1.5_VDDC_PWREN
+1.5VSDGPU	DGPU_PWR_EN	1.5_VDDC_PWREN

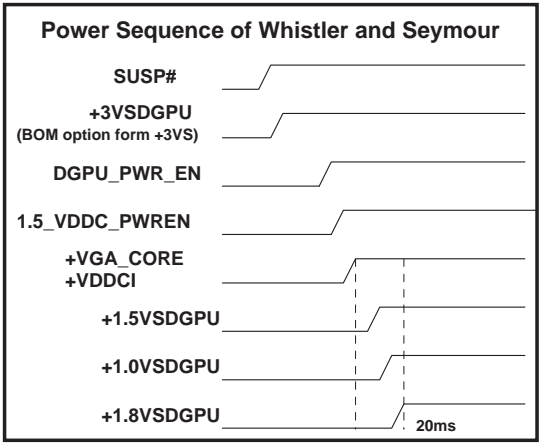
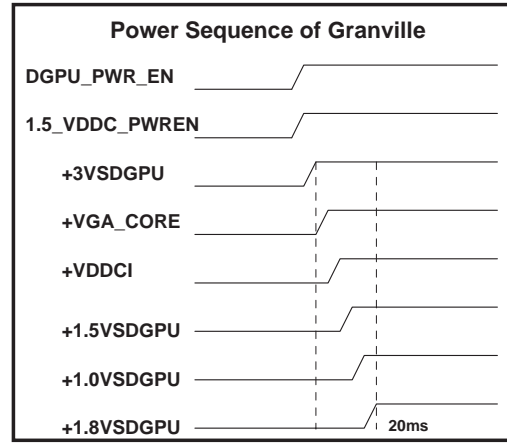


rdson<140mohm
 Q39 AO3416L_SOT23-3
 BACO@
 BACO@
 BACO@
 rdson<21mohm
 Q41 AO3416L_SOT23-3
 BACO@
 BACO@
 BACO@
 Q37 AO3416L_SOT23-3
 Q40 AO3416L_SOT23-3
 BACO@
 BACO@
 BACO@

PX_EN = 1, For BACO Mode
 BACO_EN=0
 BACO_EN#=1(5V) => BIF_VDDC=>+1.0VSDGPU
 PX_EN = 0, For Normal Mode
 BACO_EN=1(5V) => BIF_VDDC=>VGA_CORE
 BACO_EN#=0

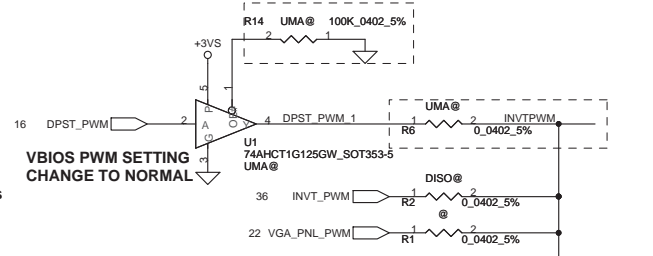
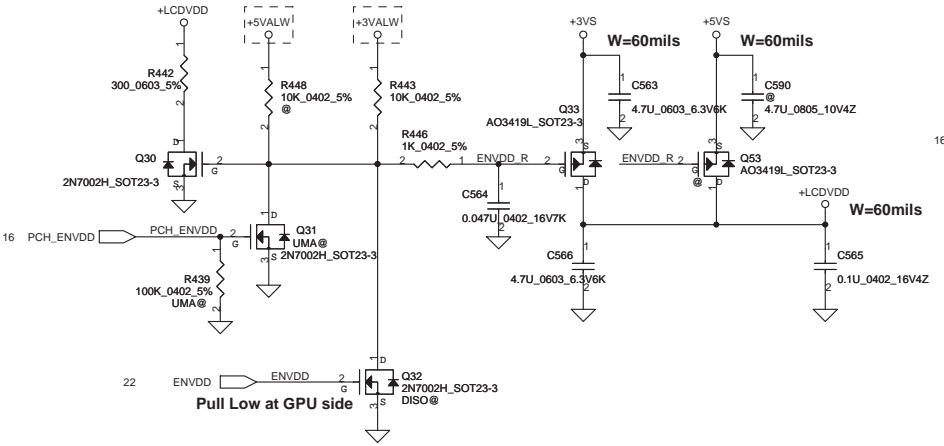
For the MOSFETS on the path of delivering
 PCIE_VDDC(+1.0VSDGPU) to
 BIF_VDDC Rds(on) of 140 mOhms or less is required.

For the MOSFETS on the path of delivering VGA_CORE to
 BIF_VDDC, Rds(on) of 21 mOhms or less is required.



100505 change to +3VALW
101029 add +5VALW

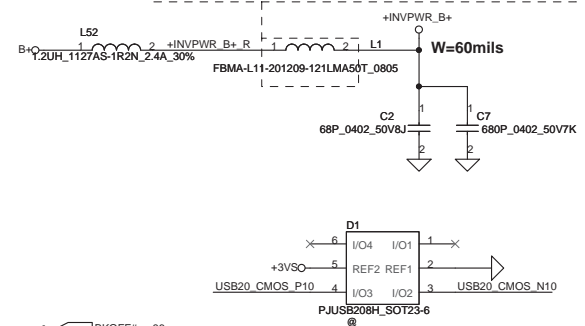
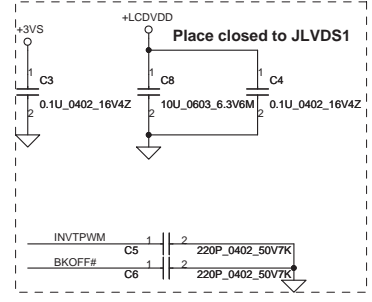
LCD POWER CIRCUIT



UMA/DIS LVDS/eDP Mapping table				
UMA	eDP	LVDS	DIS	Panel Conn.
PCH_TXOUT0+		VGA_TXOUT0+		TXOUT0+
PCH_TXOUT0-		VGA_TXOUT0-		TXOUT0-
PCH_TXOUT1+	EDP_TXP1	VGA_TXOUT1+		TXOUT1+
PCH_TXOUT1-	EDP_TXN1	VGA_TXOUT1-		TXOUT1-
PCH_TXOUT2+	EDP_TXP0	VGA_TXOUT2+		TXOUT2+
PCH_TXOUT2-	EDP_TXN0	VGA_TXOUT2-		TXOUT2-
PCH_TXCLK+		VGA_TXCLK+		TXCLK+
PCH_TXCLK-		VGA_TXCLK-		TXCLK-
PCH_TZOUT0+		VGA_TZOUT0+		TZOUT0+
PCH_TZOUT0-		VGA_TZOUT0-		TZOUT0-
PCH_TZOUT1+		VGA_TZOUT1+		TZOUT1+
PCH_TZOUT1-		VGA_TZOUT1-		TZOUT1-
PCH_TZOUT2+		VGA_TZOUT2+		TZOUT2+
PCH_TZOUT2-		VGA_TZOUT2-		TZOUT2-
PCH_TZCLK+		VGA_TZCLK+		TZCLK+
PCH_TZCLK-		VGA_TZCLK-		TZCLK-
PCH_LCD_CLK+	EDP_AUXP	VGA_LCD_CLK	AUXP	I2CC_SCL
PCH_LCD_DATA+	EDP_AUXN	VGA_LCD_DATA	AUXN	I2CC_SDA

SM010014520 3000ma 220ohm@100mhz DCR 0.04

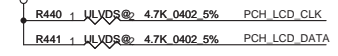
SM01000BY00 5000ma 120ohm@100mhz DCR 0.02



UMA ONLY/Muxless

16 PCH_TXOUT0+	PCH_TXOUT0+	R452	1	ULVDS@	0.0402_5%	TXOUT0+
16 PCH_TXOUT0-	PCH_TXOUT0-	R450	1	ULVDS@	0.0402_5%	TXOUT0-
16 PCH_TXOUT1+	PCH_TXOUT1+	R455	1	ULVDS@	0.0402_5%	TXOUT1+
16 PCH_TXOUT1-	PCH_TXOUT1-	R453	1	ULVDS@	0.0402_5%	TXOUT1-
16 PCH_TXOUT2+	PCH_TXOUT2+	R456	1	ULVDS@	0.0402_5%	TXOUT2+
16 PCH_TXOUT2-	PCH_TXOUT2-	R454	1	ULVDS@	0.0402_5%	TXOUT2-
16 PCH_TXCLK+	PCH_TXCLK+	R458	1	ULVDS@	0.0402_5%	TXCLK+
16 PCH_TXCLK-	PCH_TXCLK-	R457	1	ULVDS@	0.0402_5%	TXCLK-
16 PCH_TZOUT0+	PCH_TZOUT0+	R460	1	ULVDS@	0.0402_5%	TZOUT0+
16 PCH_TZOUT0-	PCH_TZOUT0-	R459	1	ULVDS@	0.0402_5%	TZOUT0-
16 PCH_TZOUT1+	PCH_TZOUT1+	R462	1	ULVDS@	0.0402_5%	TZOUT1+
16 PCH_TZOUT1-	PCH_TZOUT1-	R461	1	ULVDS@	0.0402_5%	TZOUT1-
16 PCH_TZOUT2+	PCH_TZOUT2+	R465	1	ULVDS@	0.0402_5%	TZOUT2+
16 PCH_TZOUT2-	PCH_TZOUT2-	R463	1	ULVDS@	0.0402_5%	TZOUT2-
16 PCH_TZCLK+	PCH_TZCLK+	R467	1	ULVDS@	0.0402_5%	TZCLK+
16 PCH_TZCLK-	PCH_TZCLK-	R466	1	ULVDS@	0.0402_5%	TZCLK-
16 PCH_LCD_CLK	PCH_LCD_CLK	R444	1	ULVDS@	0.0402_5%	I2CC_SCL
16 PCH_LCD_DATA	PCH_LCD_DATA	R445	1	ULVDS@	0.0402_5%	I2CC_SDA

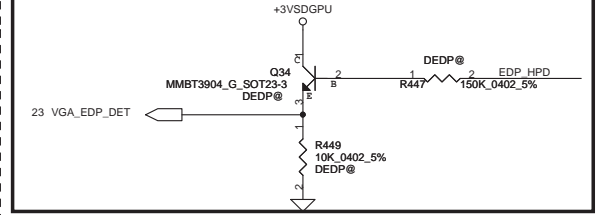
5/4 PCH_LCD_CLK & PCH_LCD_DATA
Pull high 2.2K change to 4.7K



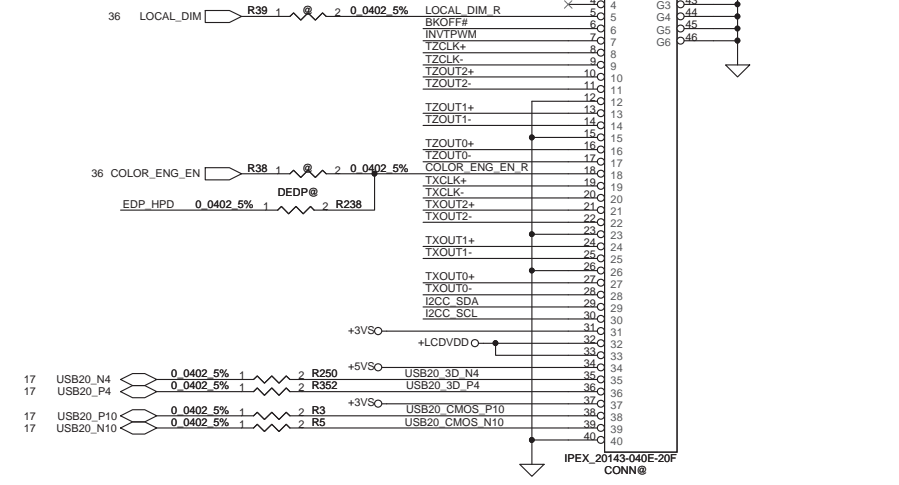
Discrete ONLY

22 VGA_TXOUT0+	VGA_TXOUT0+	R13	1	ULVDS@	0.0402_5%	TXOUT0+
22 VGA_TXOUT0-	VGA_TXOUT0-	R12	1	ULVDS@	0.0402_5%	TXOUT0-
22 VGA_TXOUT1+	VGA_TXOUT1+	R23	1	ULVDS@	0.0402_5%	TXOUT1+
22 VGA_TXOUT1-	VGA_TXOUT1-	R17	1	ULVDS@	0.0402_5%	TXOUT1-
22 VGA_TXOUT2+	VGA_TXOUT2+	R24	1	ULVDS@	0.0402_5%	TXOUT2+
22 VGA_TXOUT2-	VGA_TXOUT2-	R22	1	ULVDS@	0.0402_5%	TXOUT2-
22 VGA_TXCLK+	VGA_TXCLK+	R26	1	ULVDS@	0.0402_5%	TXCLK+
22 VGA_TXCLK-	VGA_TXCLK-	R25	1	ULVDS@	0.0402_5%	TXCLK-
22 VGA_TZOUT0+	VGA_TZOUT0+	R28	1	ULVDS@	0.0402_5%	TZOUT0+
22 VGA_TZOUT0-	VGA_TZOUT0-	R27	1	ULVDS@	0.0402_5%	TZOUT0-
22 VGA_TZOUT1+	VGA_TZOUT1+	R30	1	ULVDS@	0.0402_5%	TZOUT1+
22 VGA_TZOUT1-	VGA_TZOUT1-	R29	1	ULVDS@	0.0402_5%	TZOUT1-
22 VGA_TZOUT2+	VGA_TZOUT2+	R32	1	ULVDS@	0.0402_5%	TZOUT2+
22 VGA_TZOUT2-	VGA_TZOUT2-	R31	1	ULVDS@	0.0402_5%	TZOUT2-
22 VGA_TZCLK+	VGA_TZCLK+	R34	1	ULVDS@	0.0402_5%	TZCLK+
22 VGA_TZCLK-	VGA_TZCLK-	R33	1	ULVDS@	0.0402_5%	TZCLK-
23 VGA_LCD_CLK	VGA_LCD_CLK	R9	1	ULVDS@	0.0402_5%	I2CC_SCL
23 VGA_LCD_DATA	VGA_LCD_DATA	R7	1	ULVDS@	0.0402_5%	I2CC_SDA

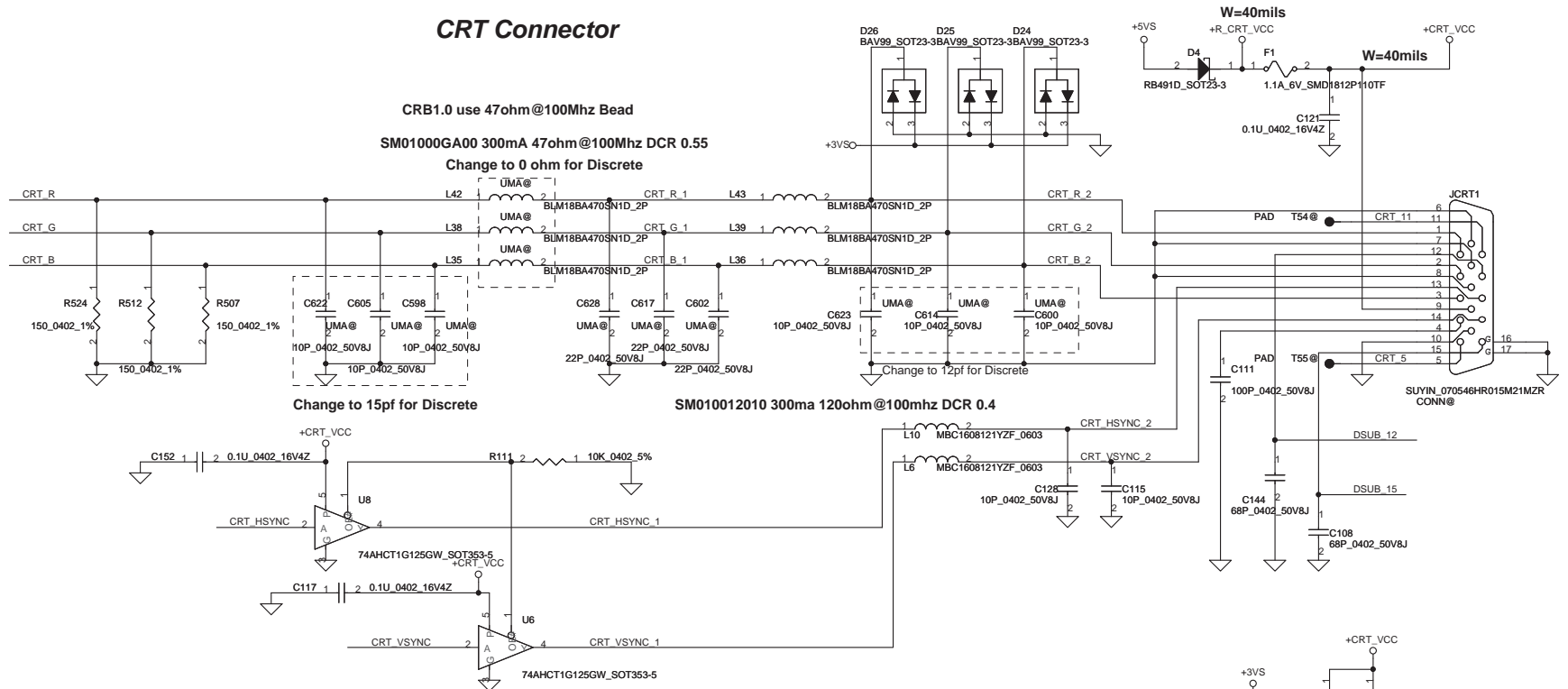
BOM option for Discrete eDP



LED PANEL Conn.

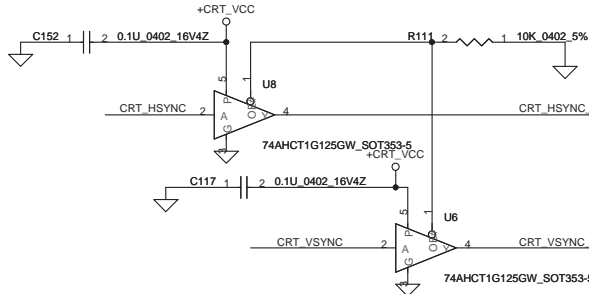


CRT Connector



Change to 15pf for Discrete

SM010012010 300ma 120ohm@100mhz DCR 0.4



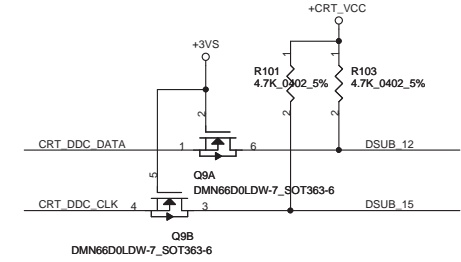
UMA only/Muxless

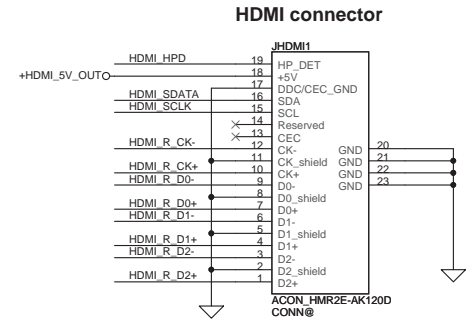
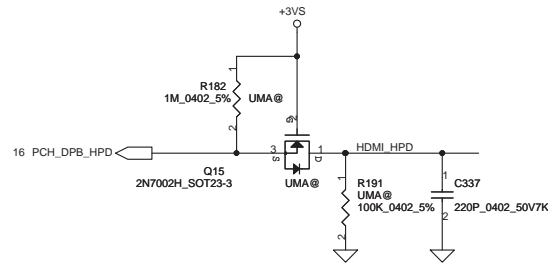
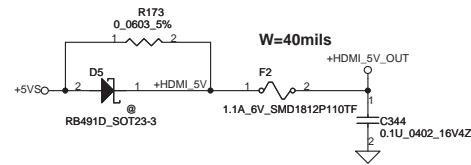
16	PCH_CRT_R	PCH CRT R	R529	UMA@	1	0.0402 5%	CRT R
16	PCH_CRT_G	PCH CRT G	R519	UMA@	1	0.0402 5%	CRT G
16	PCH_CRT_B	PCH CRT B	R511	UMA@	1	0.0402 5%	CRT B
16	PCH_CRT_HSYNC	PCH CRT HSYNC	R137	UMA@	1	33.0402 5%	CRT HSYNC
16	PCH_CRT_VSYNC	PCH CRT VSYNC	R110	UMA@	1	33.0402 5%	CRT VSYNC
16	PCH_CRT_CLK	PCH CRT CLK	R102	UMA@	1	0.0402 5%	CRT_DDC_CLK
16	PCH_CRT_DATA	PCH CRT DATA	R89	UMA@	1	0.0402 5%	CRT_DDC_DATA

PCH DDC PU 2.2K on Page 17

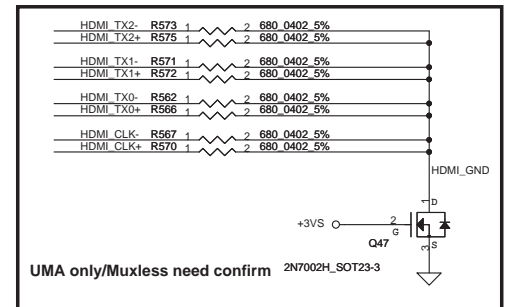
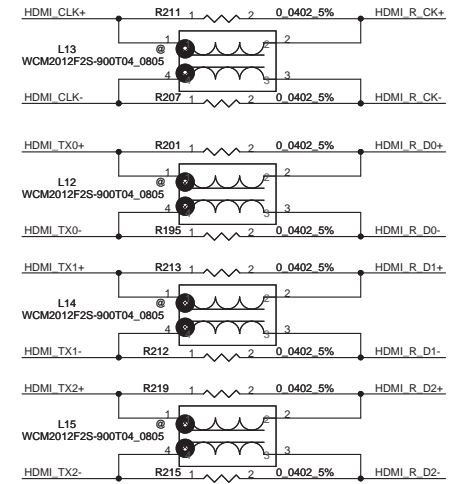
Discrete only

23	VGA_CRT_R	VGA CRT R	R527	RISOR	1	0.0402 5%	CRT R
23	VGA_CRT_G	VGA CRT G	R514	RISOR	1	0.0402 5%	CRT G
23	VGA_CRT_B	VGA CRT B	R510	RISOR	1	0.0402 5%	CRT B
23	VGA_CRT_HSYNC	VGA CRT HSYNC	R131	RISOR	1	0.0402 5%	CRT HSYNC
23	VGA_CRT_VSYNC	VGA CRT VSYNC	R107	RISOR	1	0.0402 5%	CRT VSYNC
23	VGA_DDC_CLK	VGA DDC CLK	R98	RISOR	1	0.0402 5%	CRT_DDC_CLK
23	VGA_DDC_DATA	VGA DDC DATA	R86	RISOR	1	0.0402 5%	CRT_DDC_DATA



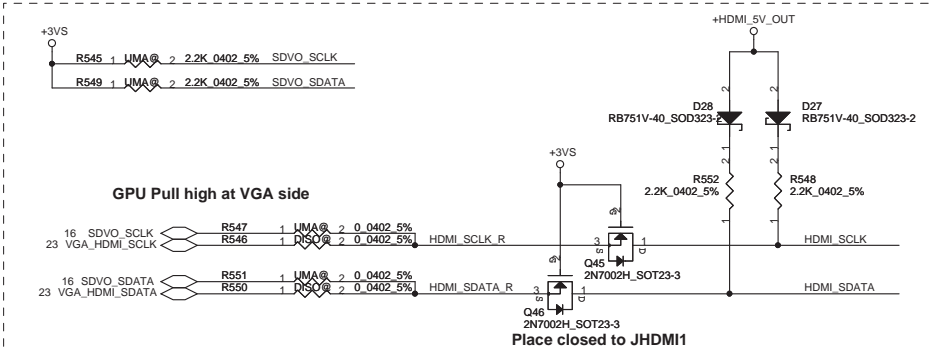
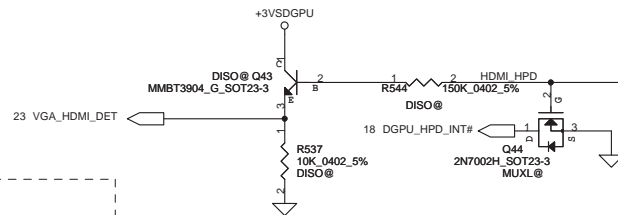


SM070001310 400ma 90ohm@100mhz DCR 0.3



UMA/Muxless			
16 PCH_DPB_N0	C364	UMA@ 2	1 .1U 0402 16V7K HDMI TX2-
16 PCH_DPB_P0	C368	UMA@ 2	1 .1U 0402 16V7K HDMI TX2+
16 PCH_DPB_N1	C357	UMA@ 2	1 .1U 0402 16V7K HDMI TX1-
16 PCH_DPB_P1	C359	UMA@ 2	1 .1U 0402 16V7K HDMI TX1+
16 PCH_DPB_N2	C347	UMA@ 2	1 .1U 0402 16V7K HDMI TX0-
16 PCH_DPB_P2	C349	UMA@ 2	1 .1U 0402 16V7K HDMI TX0+
16 PCH_DPB_N3	C352	UMA@ 2	1 .1U 0402 16V7K HDMI CLK-
16 PCH_DPB_P3	C356	UMA@ 2	1 .1U 0402 16V7K HDMI CLK+

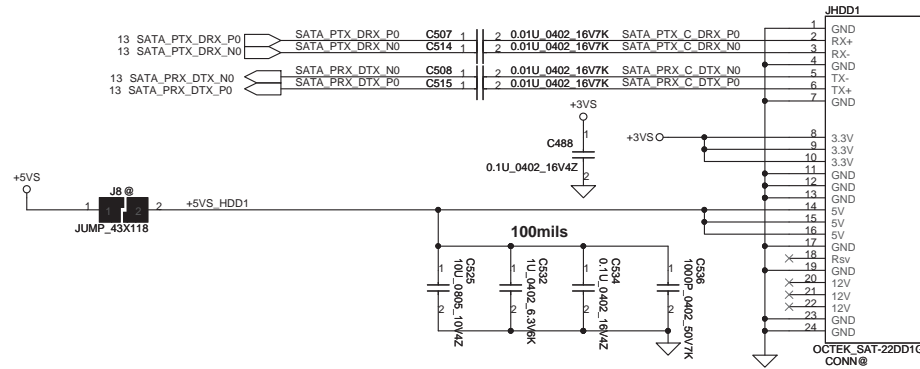
DIS Only			
23 VGA_HDMI_TXD2-	C716	DISO@ 2	1 .1U 0402 16V7K HDMI TX2-
23 VGA_HDMI_TXD2+	C717	DISO@ 2	1 .1U 0402 16V7K HDMI TX2+
23 VGA_HDMI_TXD1-	C714	DISO@ 2	1 .1U 0402 16V7K HDMI TX1-
23 VGA_HDMI_TXD1+	C715	DISO@ 2	1 .1U 0402 16V7K HDMI TX1+
23 VGA_HDMI_TXD0-	C704	DISO@ 2	1 .1U 0402 16V7K HDMI TX0-
23 VGA_HDMI_TXD0+	C709	DISO@ 2	1 .1U 0402 16V7K HDMI TX0+
23 VGA_HDMI_TXC-	C712	DISO@ 2	1 .1U 0402 16V7K HDMI CLK-
23 VGA_HDMI_TXC+	C713	DISO@ 2	1 .1U 0402 16V7K HDMI CLK+



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Revision	1	Revision	1	Document Number	4019A9
Date:	Tuesday, November 09, 2010	Sheet	32	of	60

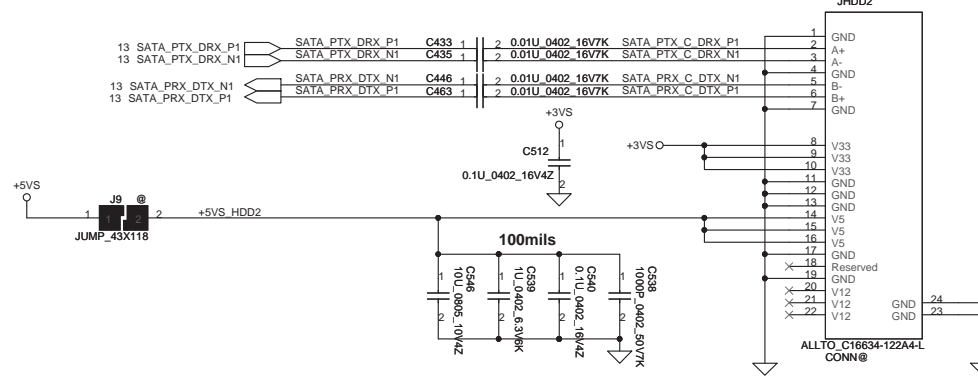
SATA HDD1 Conn.

CL 2.9 mm



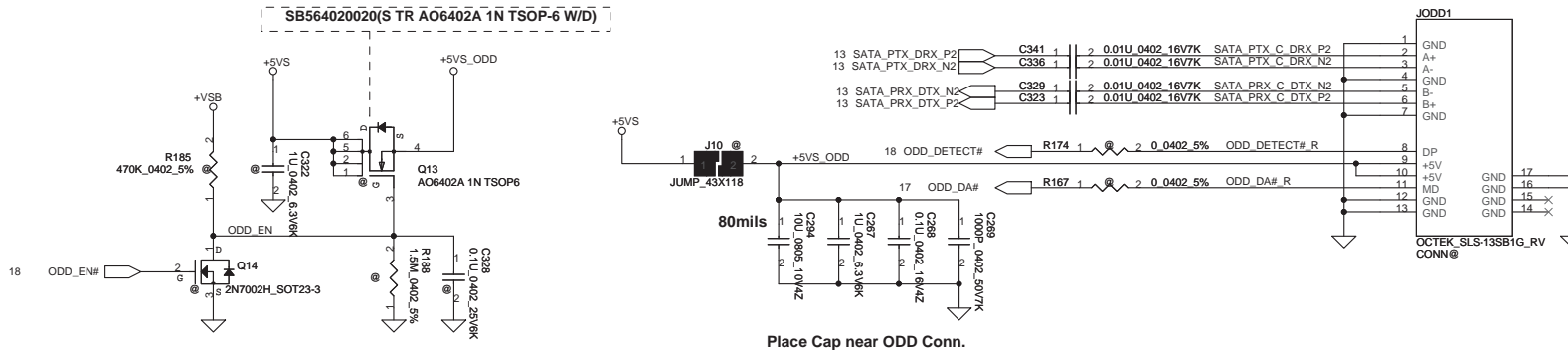
SATA HDD2 Conn.

CL 4.4 mm



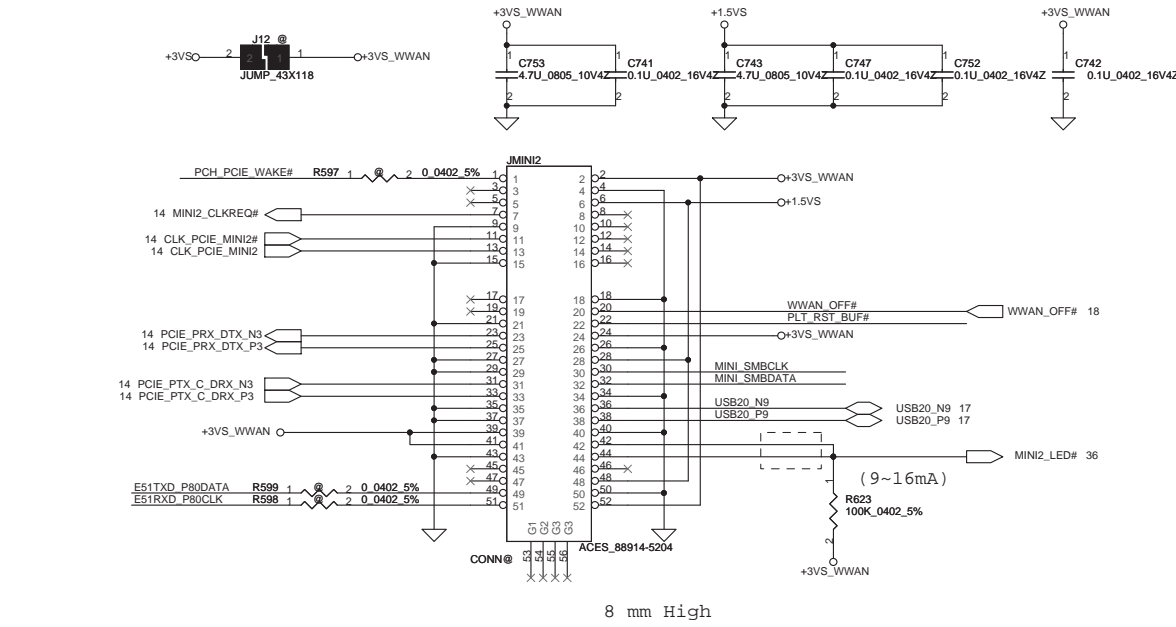
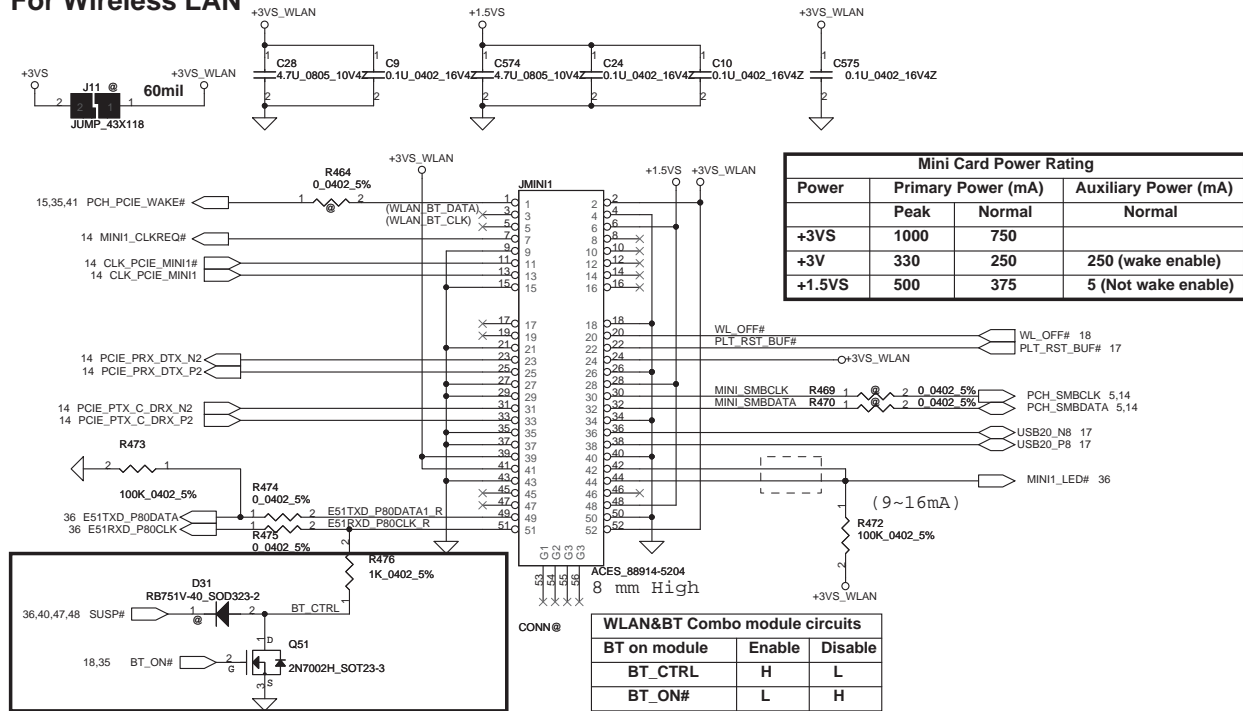
SATA ODD Conn.

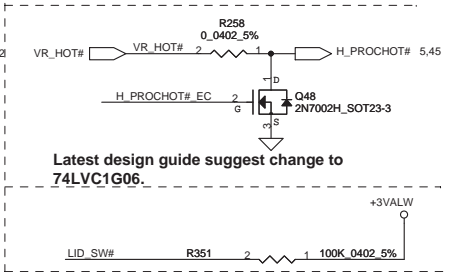
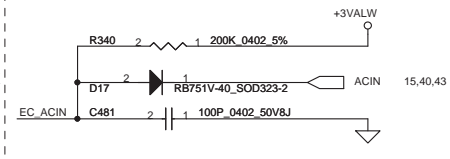
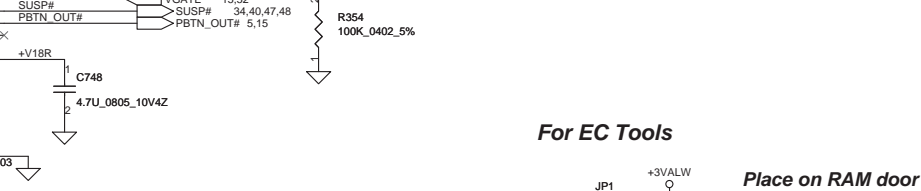
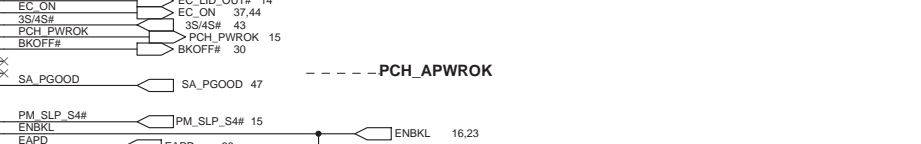
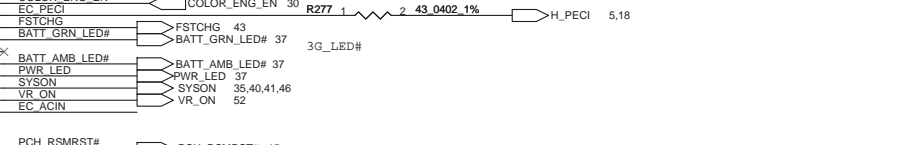
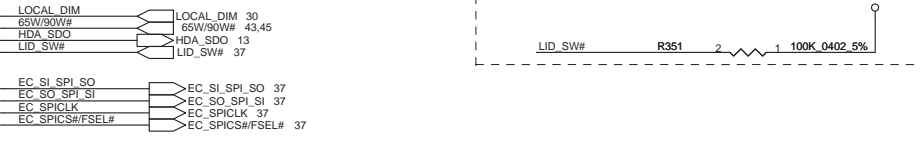
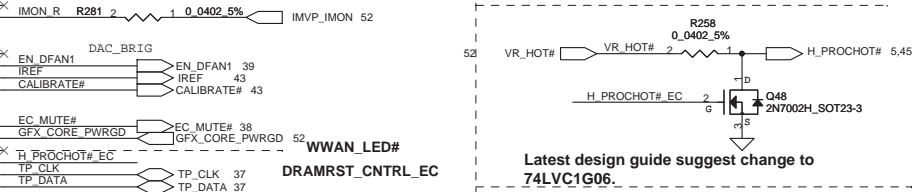
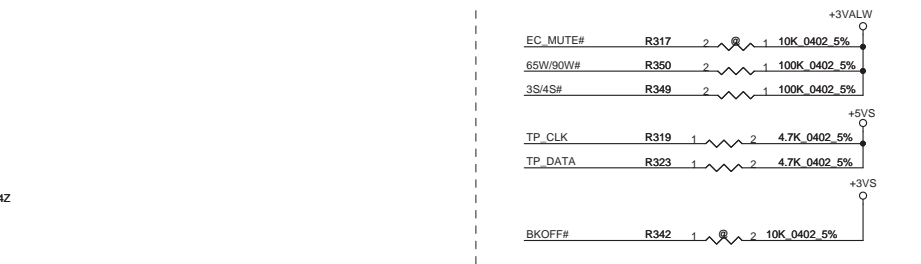
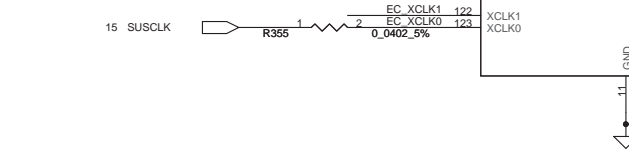
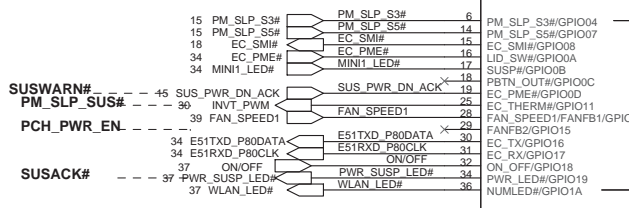
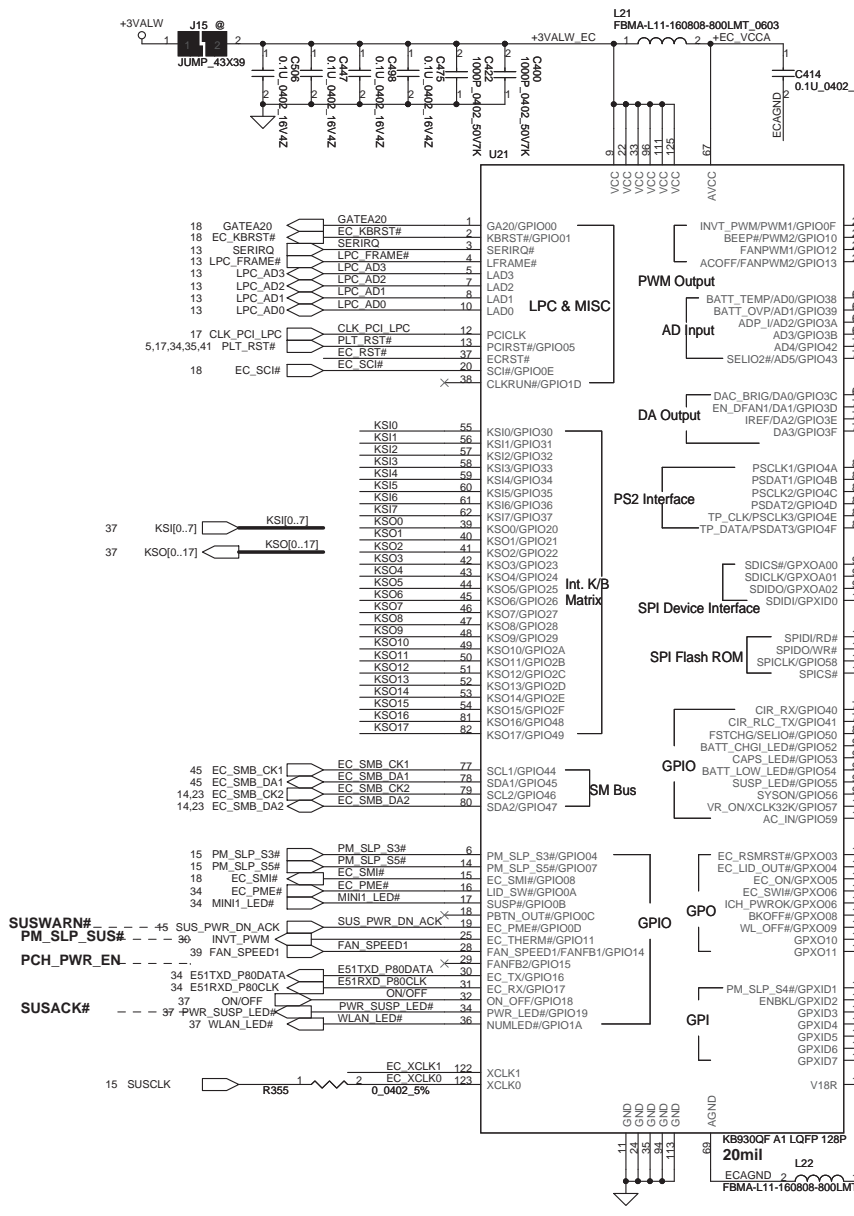
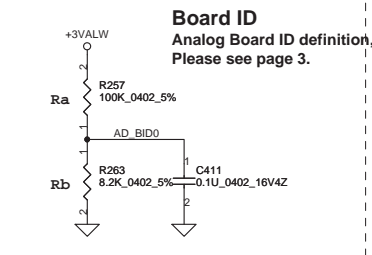
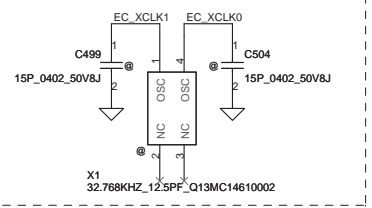
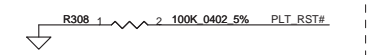
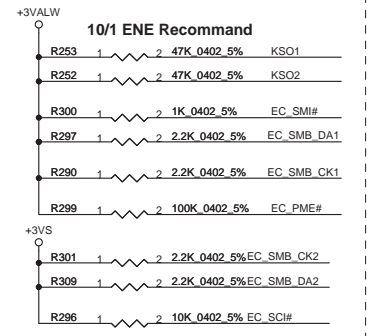
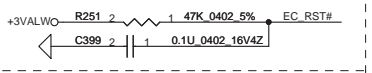
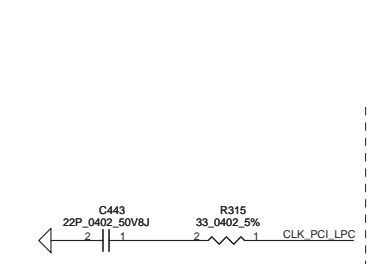
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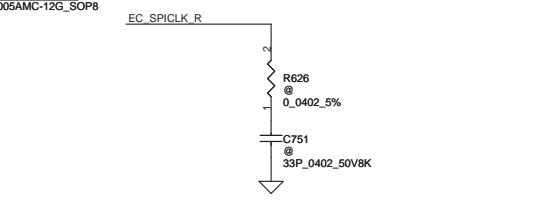
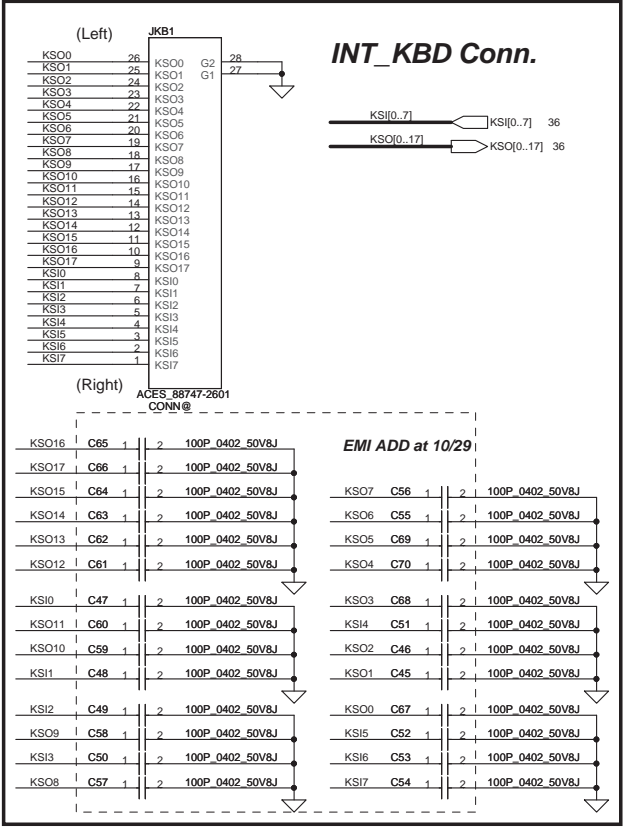
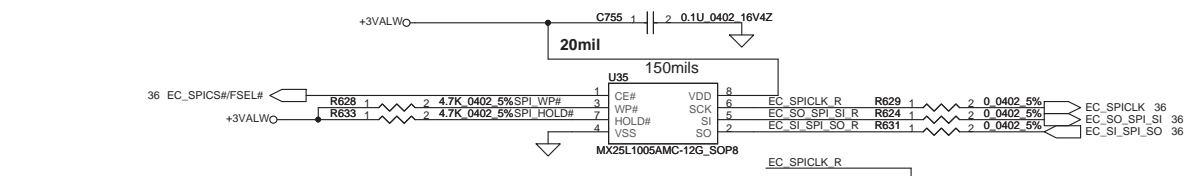
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For Wireless LAN

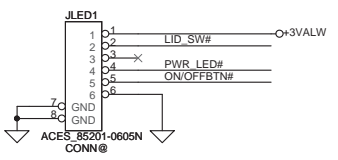




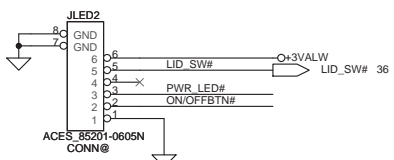
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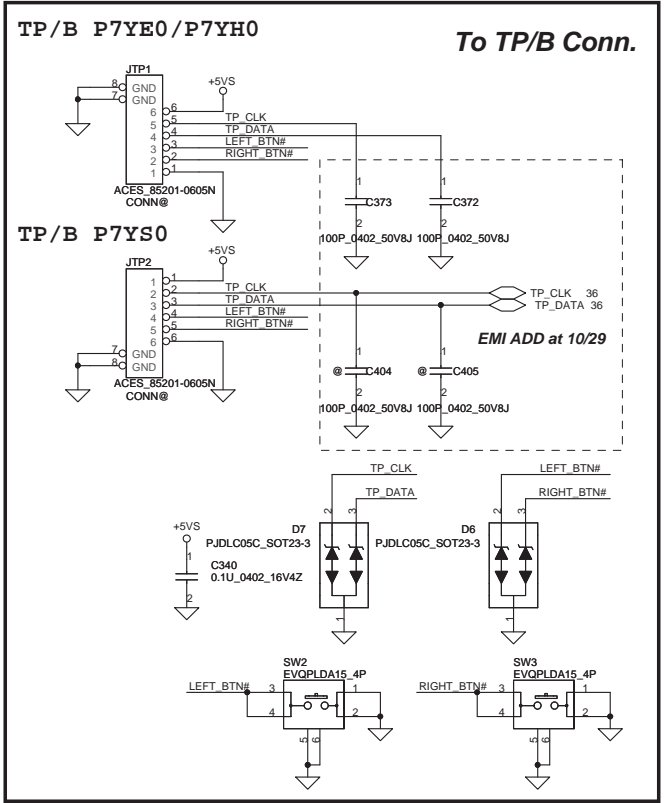
LED/B P7YE0/P7YH0
LS-6913P



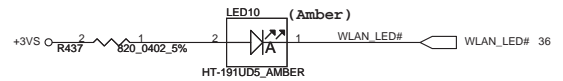
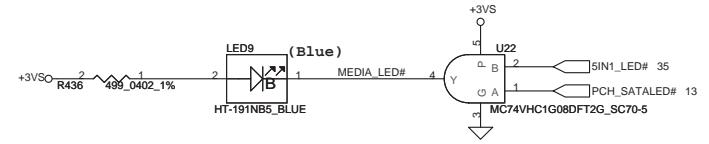
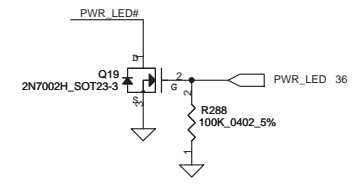
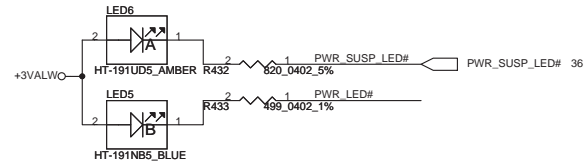
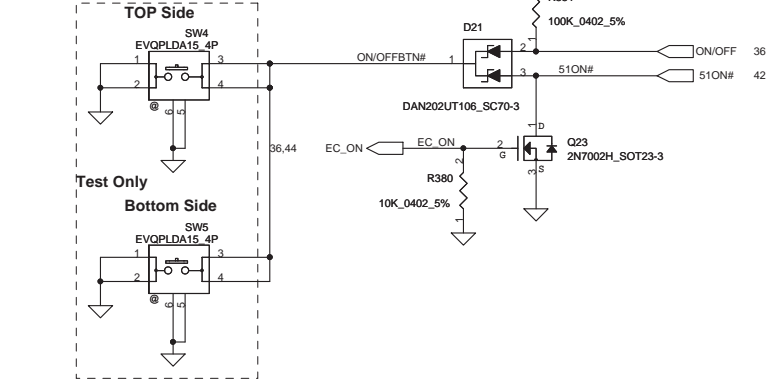
LED/B P7YS0
LS-6913P

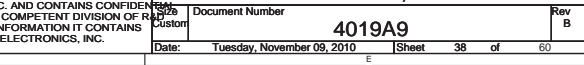
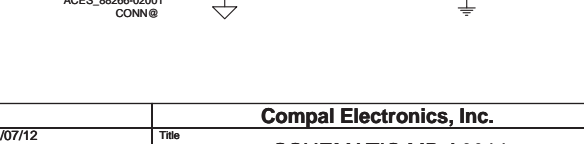
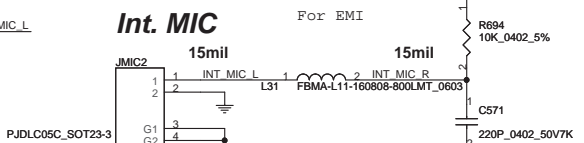
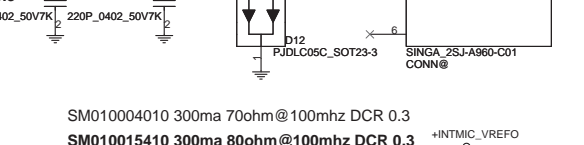
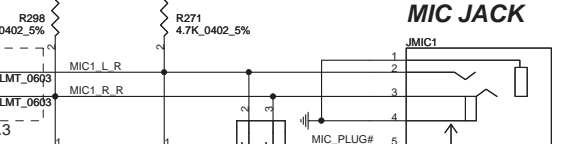
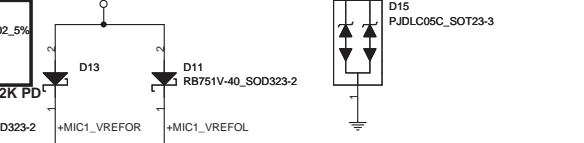
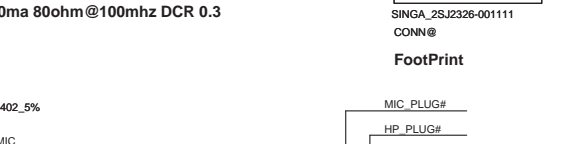
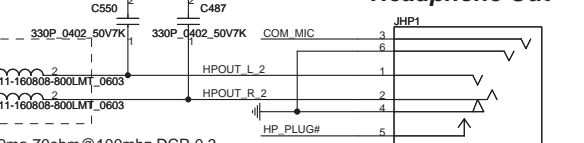
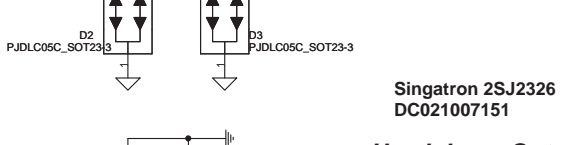
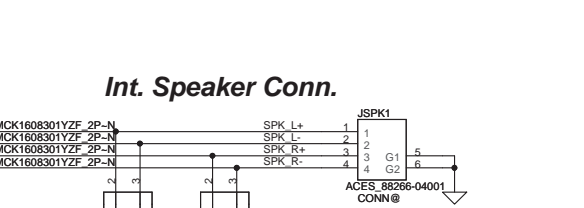
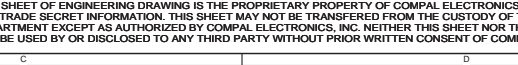
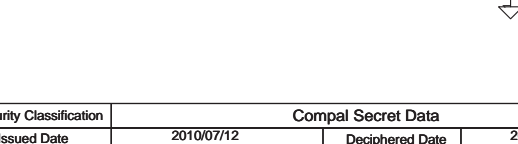
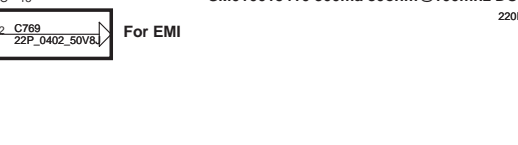
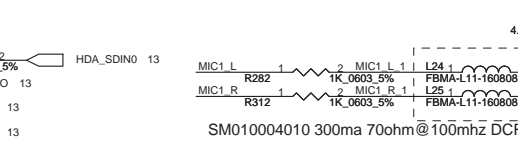
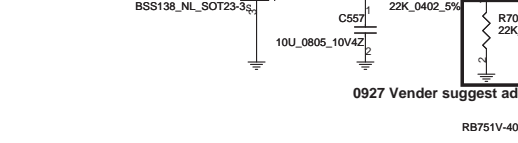
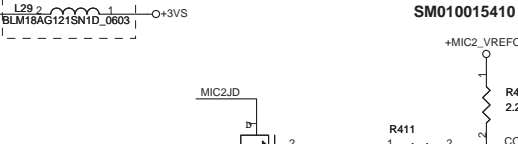
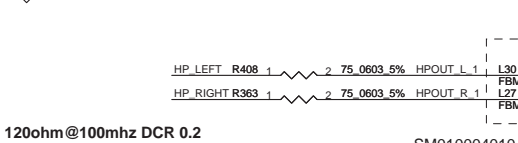
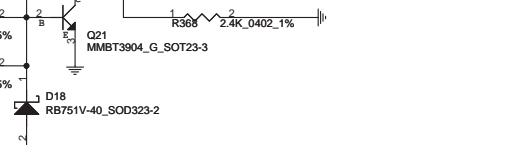
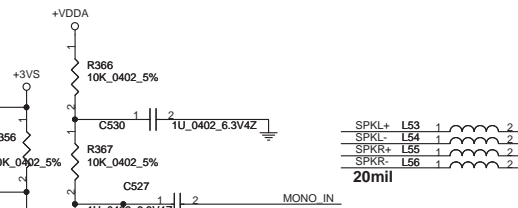
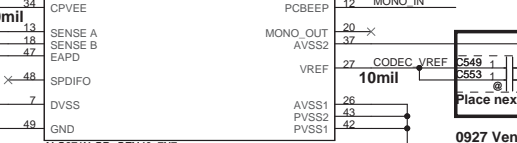
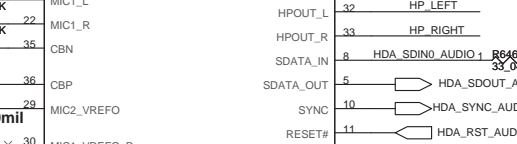
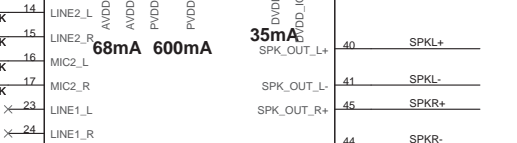
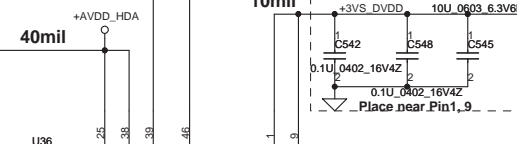
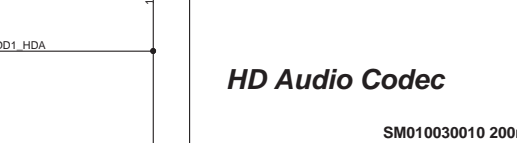
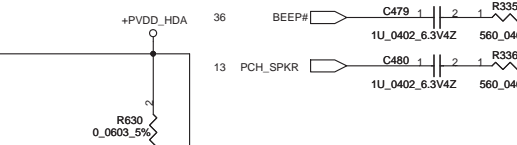
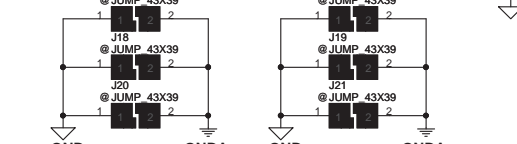
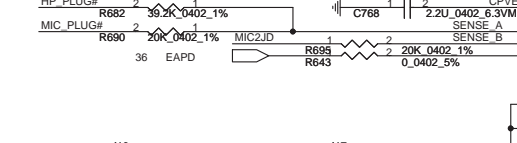
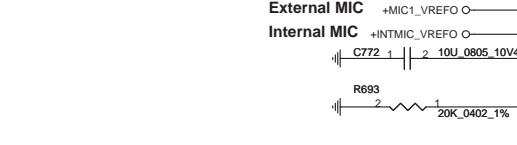
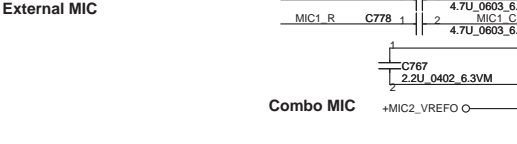
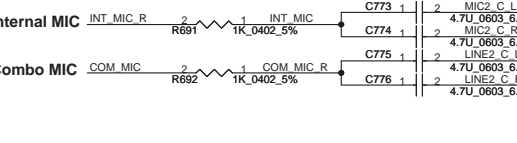
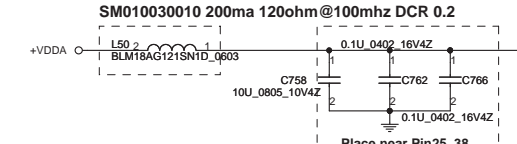
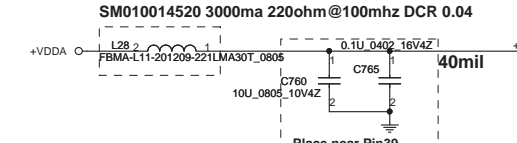
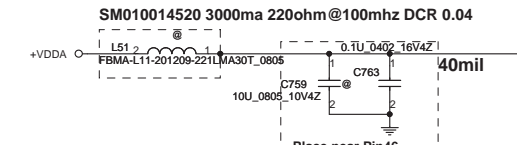
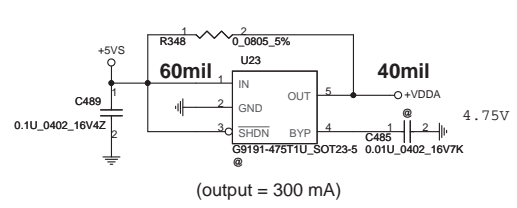


LED Status	Power/SUS		Battery		3G/WLAN	BlueTooth	ACIN
	ON	SUS	Full	Charge	3G	WLAN	
NEW70/80/90	Blue	Amber	Blue		Blue	Amber	



Power Button
ON/OFF switch





HD Audio Codec

Int. Speaker Conn.

Singatron 2SJ2326
DC021007151

Headphone Out

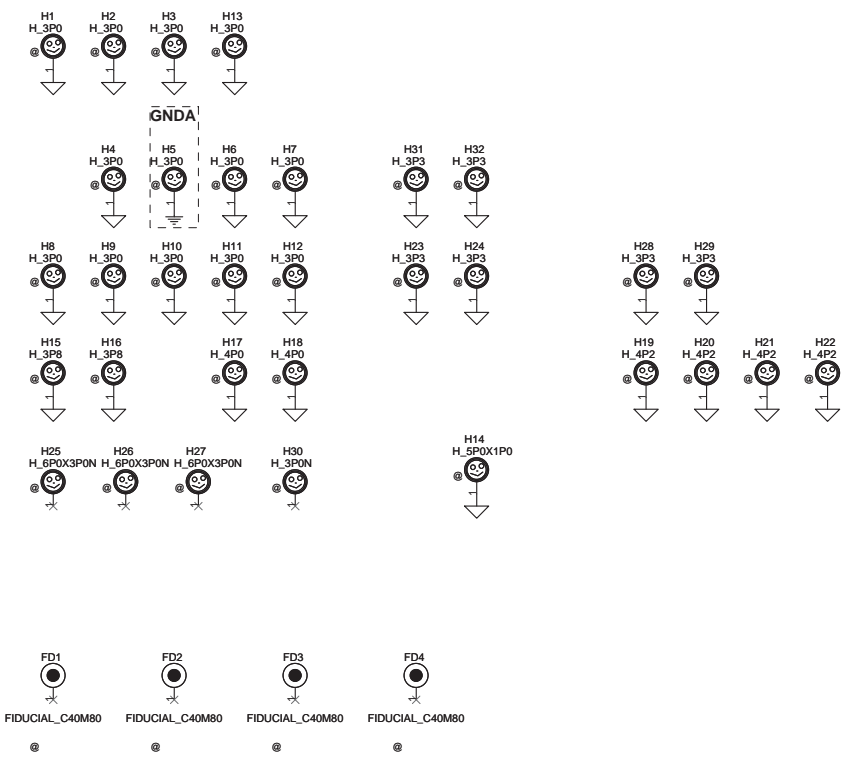
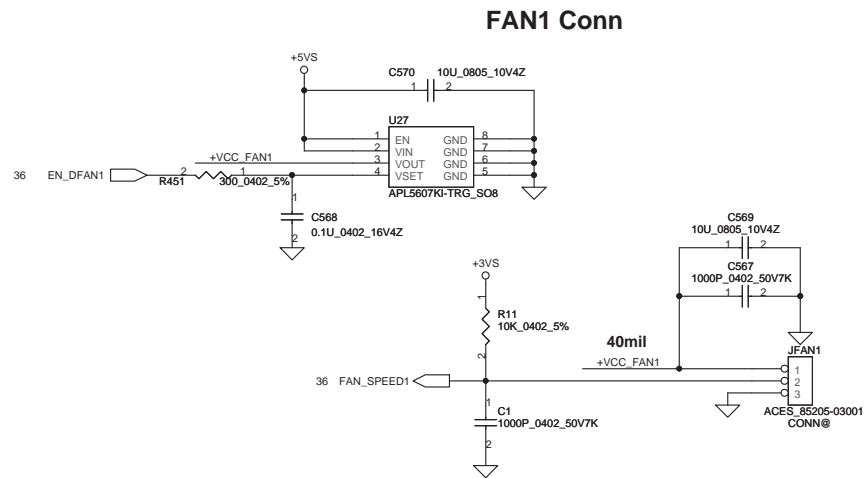
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CONN@

FootPrint

MIC JACK

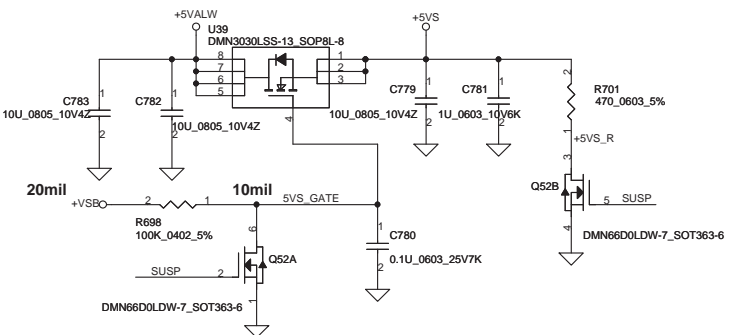
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CONN@

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<p>4019A9</p>				Rev B
<p>Date: Tuesday, November 09, 2010 Sheet 38 of 60</p>				

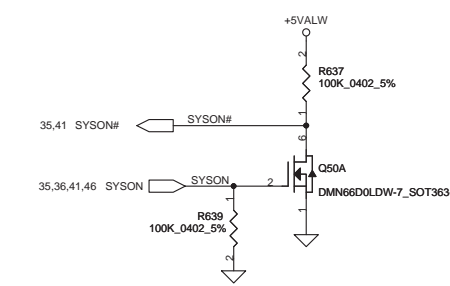
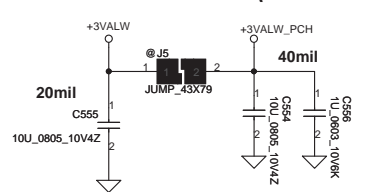


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				Date:	Tuesday, November 09, 2010
				Sheet	39 of 60
				Rev	B

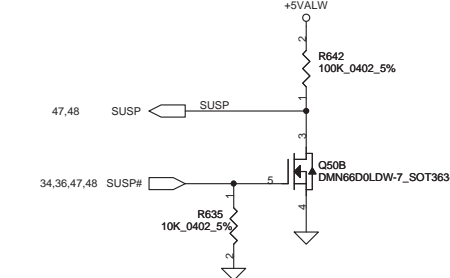
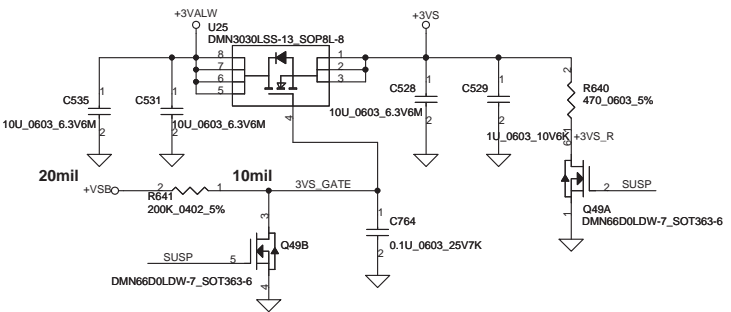
+5VALW TO +5VS



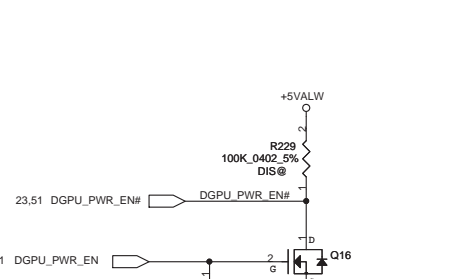
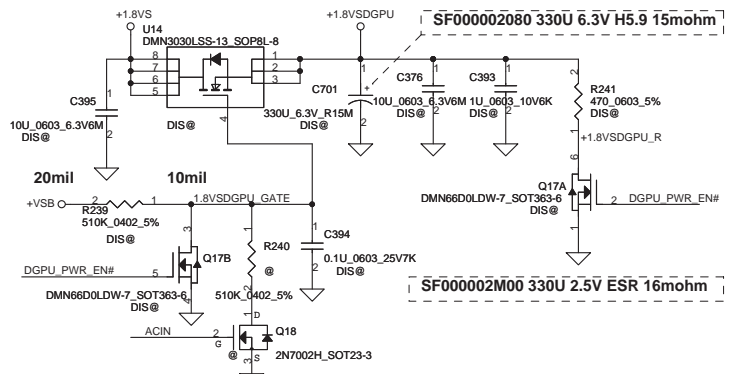
+3VALW TO +3VALW(PCH AUX Power)



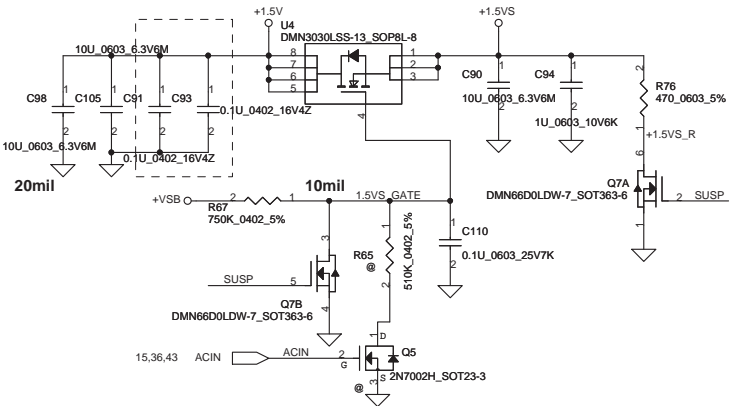
+3VALW TO +3VS



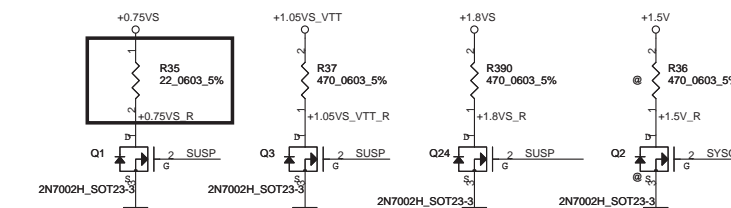
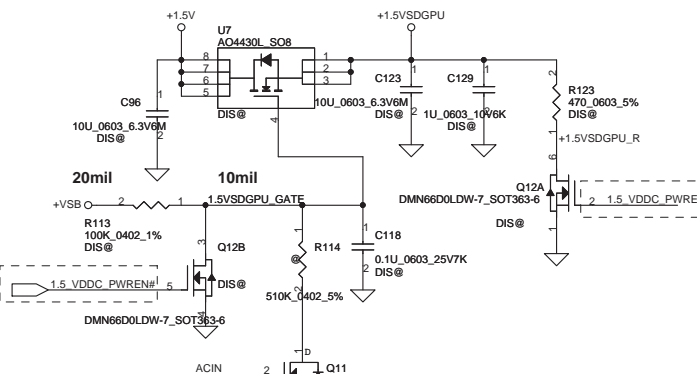
+1.8VS to +1.8VSDGPU for GPU



1211 EMI ADD 0.1U close PJ5 +1.5V to +1.5VS

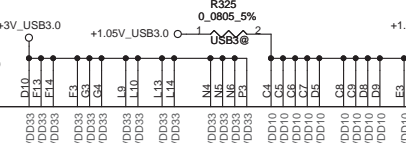
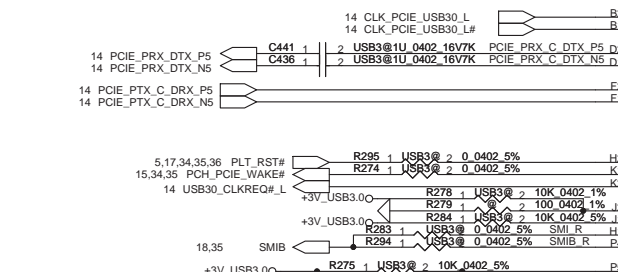
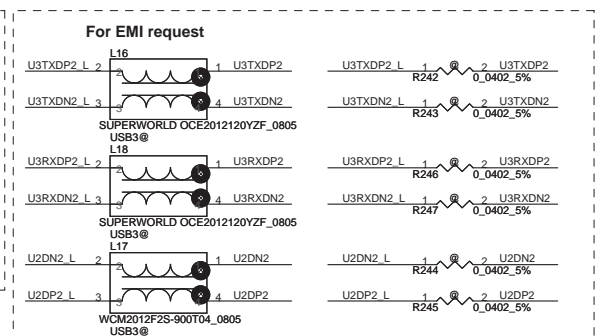
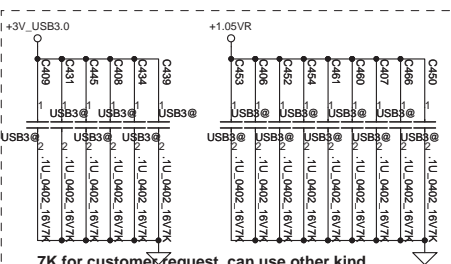
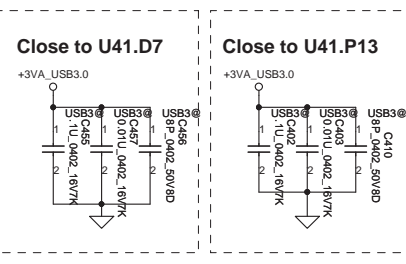
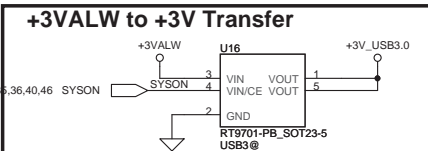
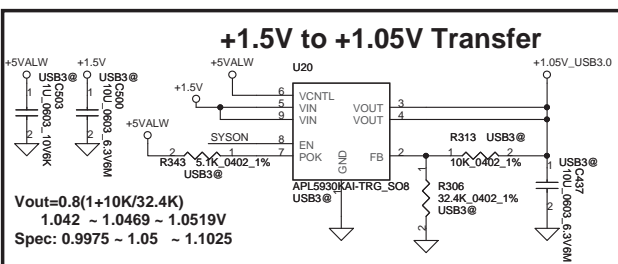


+1.5V to +1.5VSDGPU for GPU



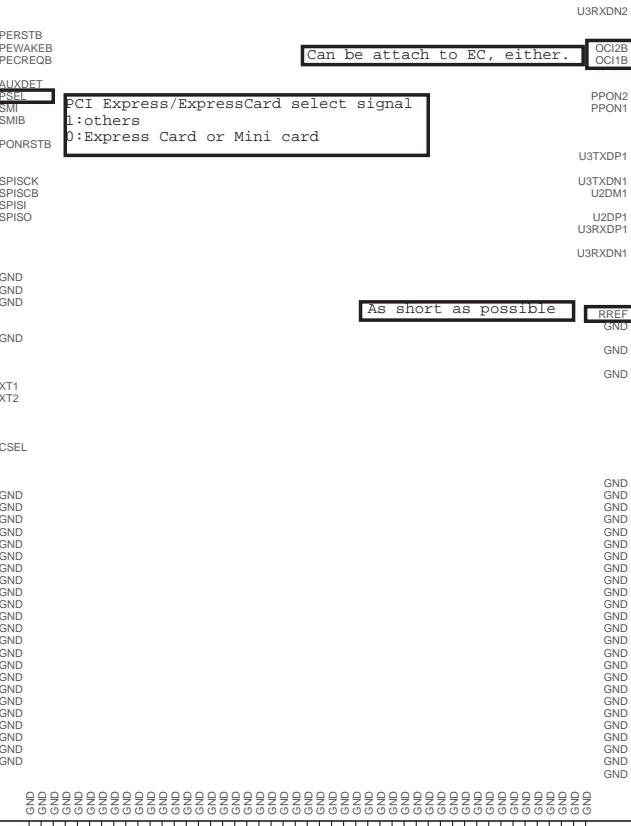
2009/08/14
 CP_S3PowerReduction
 WhitePaper_Rev0.9
 0.75VS speed up discharge

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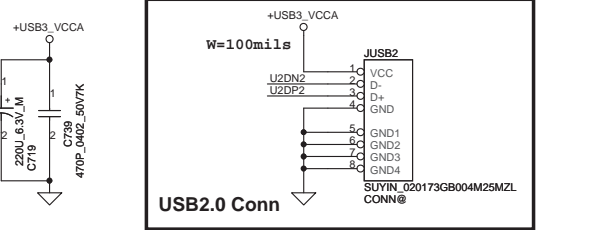
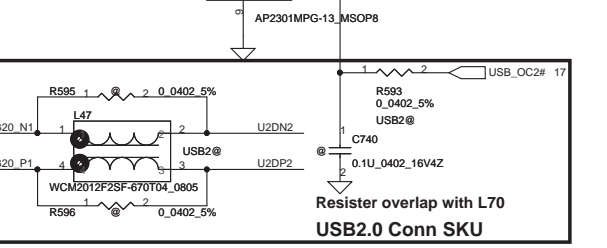
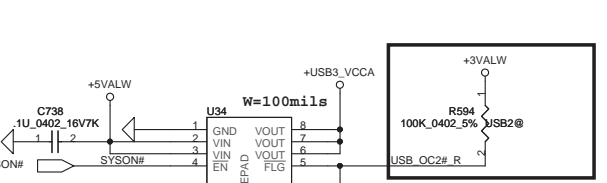
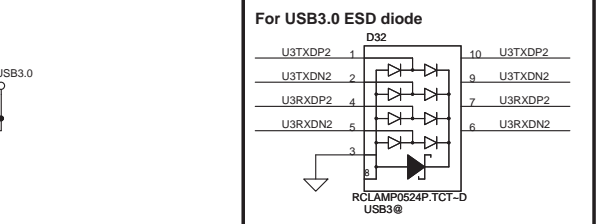
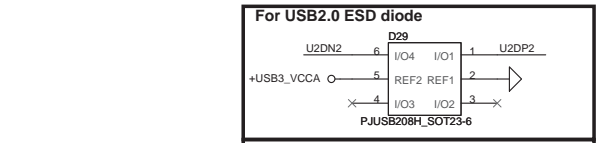
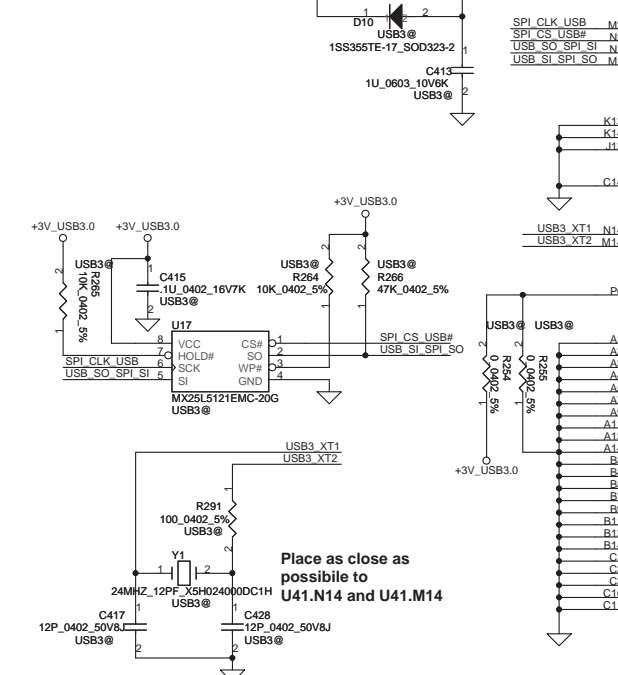
SPEC Max: +3V---200mA; +1.05V---800mA
Idle mode: 0.489W;
+3V---43mA; +1.05V---328mA
D3 mode: 0.066W;
+3V---5.4mA; +1.05V---45mA

7K for customer request, can use other kind of capacitor, like Y5V.



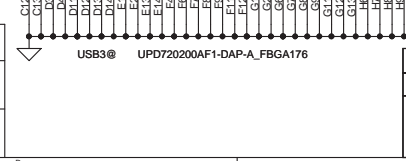
Can be attach to EC, either.

As short as possible



Pin compare table for support USB remote wakeup or not

	AUXDET(Pin J2)	CSEL(Pin P6)	CLK
Support USB remote wakeup	pull high 10k to VDD33	Tied to GND	Must use 24MHz crystal: mount Y5,R816,C879,C880
Not support USB remote wakeup	Tied to GND	pull high to VDD33	Can use either 48MHz or 24MHz When use 48MHz clock: mount R22,R25

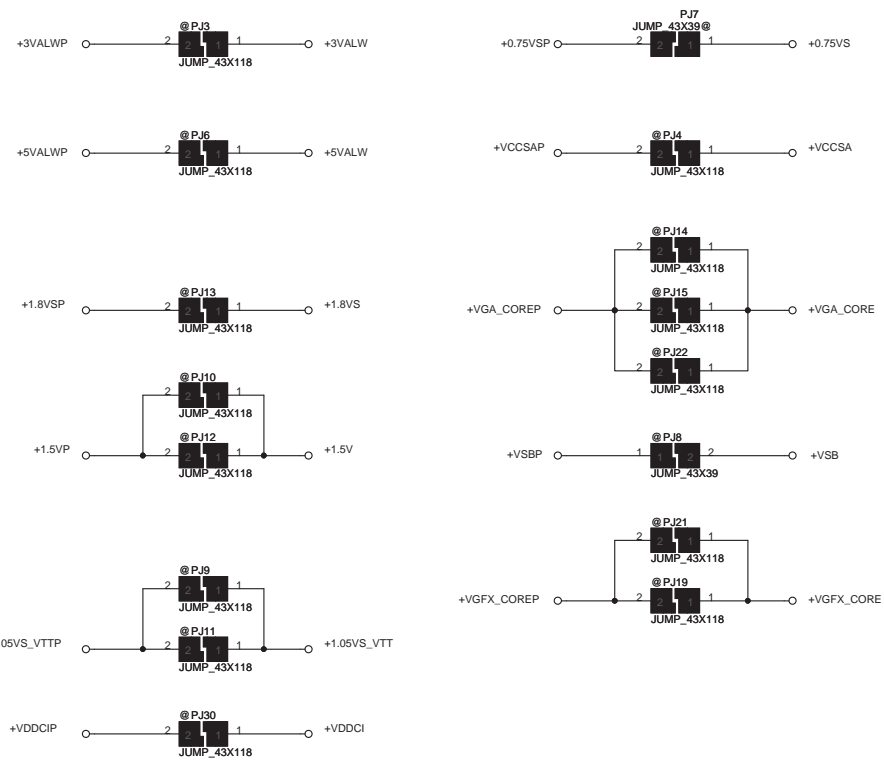
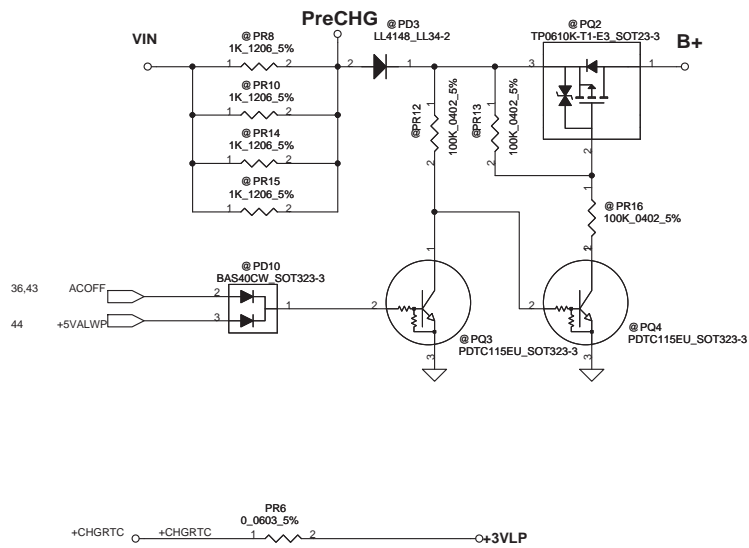
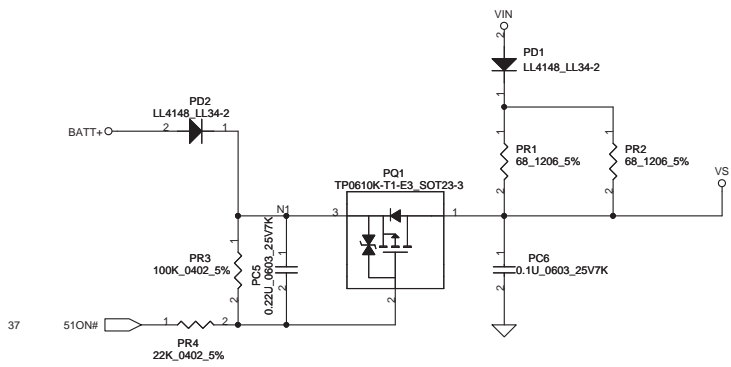
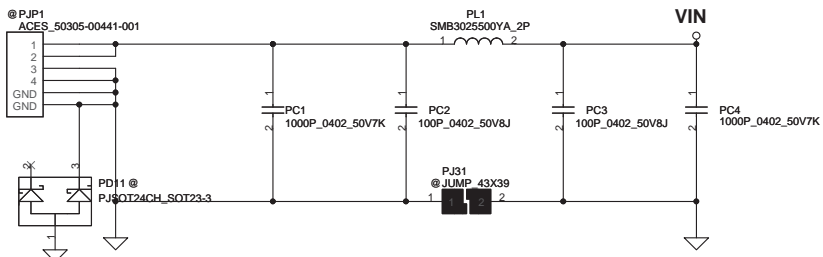


P/N: SA00048H10 (S IC UPD720200AF1-DAP-SSA-A FBGA USB3.0)

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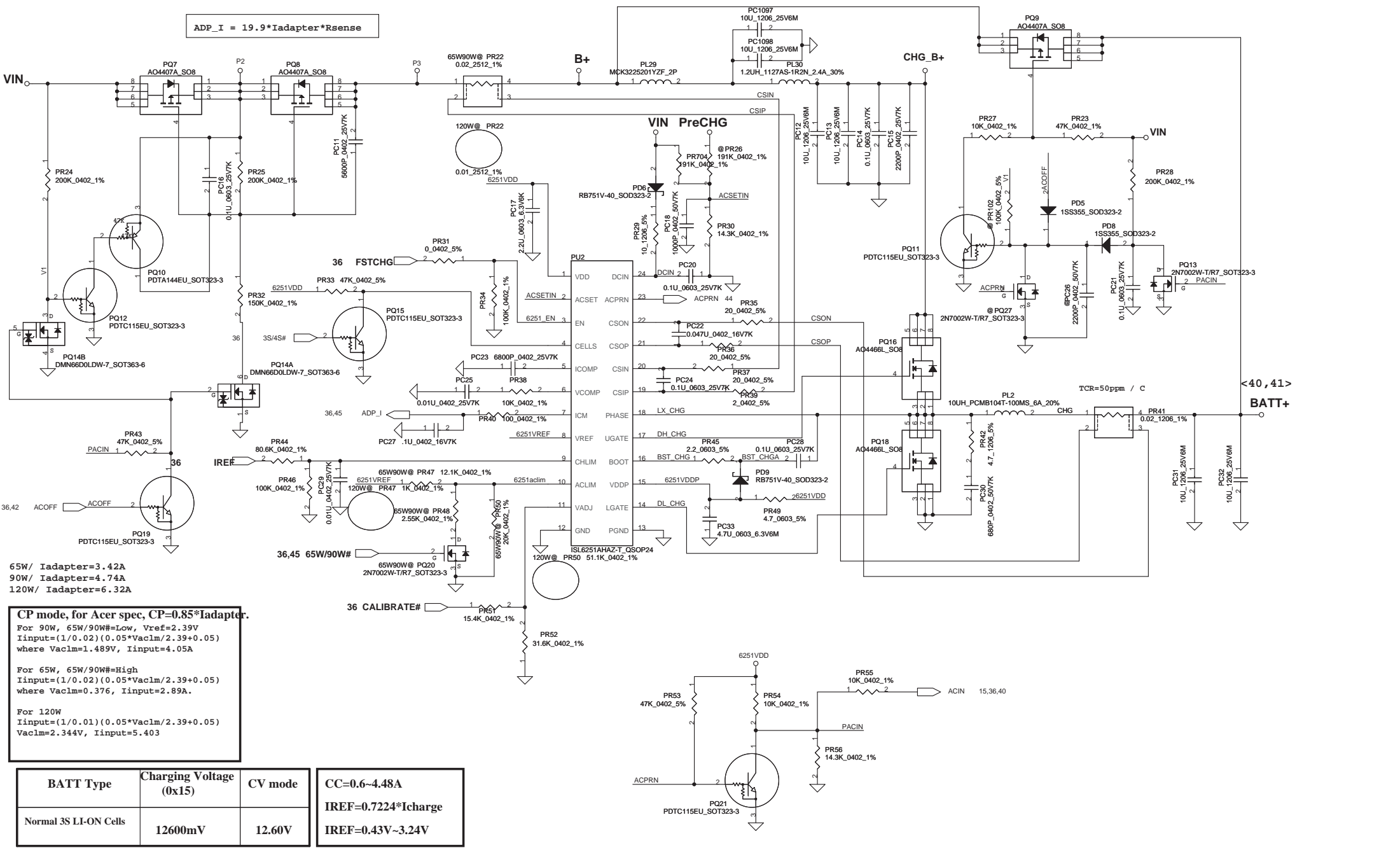
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$$ADP_I = 19.9 * I_{adapter} * R_{sense}$$



65W/ Iadapter=3.42A
 90W/ Iadapter=4.74A
 120W/ Iadapter=6.32A

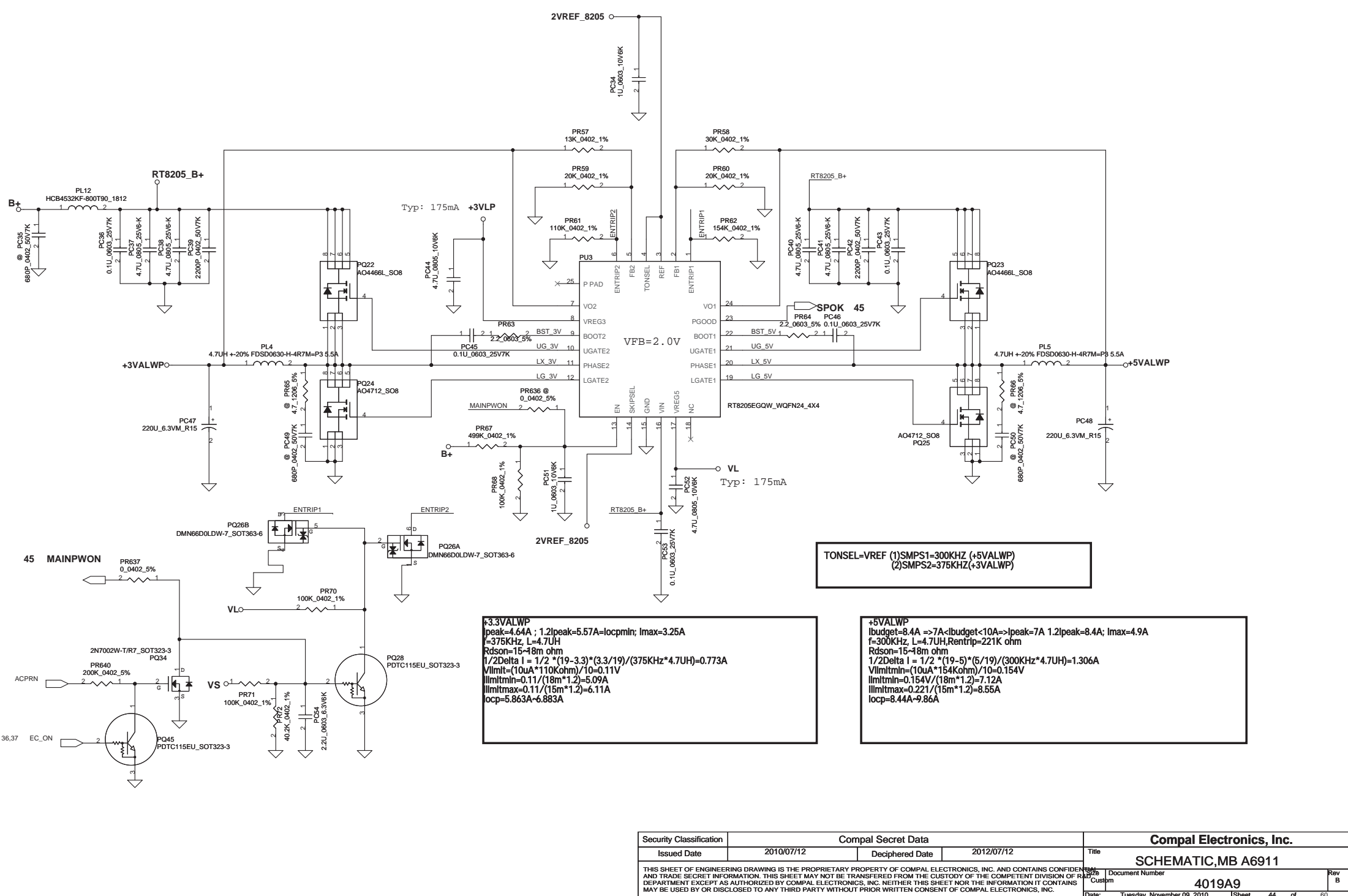
CP mode, for Acer spec, CP=0.85*Iadapter.
 For 90W, 65W/90W#=Low, Vref=2.39V
 $I_{input} = (1/0.02) (0.05 * V_{acim} / 2.39 + 0.05)$
 where $V_{acim} = 1.489V$, $I_{input} = 4.05A$
 For 65W, 65W/90W#=#High
 $I_{input} = (1/0.02) (0.05 * V_{acim} / 2.39 + 0.05)$
 where $V_{acim} = 0.376V$, $I_{input} = 2.89A$
 For 120W
 $I_{input} = (1/0.01) (0.05 * V_{acim} / 2.39 + 0.05)$
 $V_{acim} = 2.344V$, $I_{input} = 5.403$

BATT Type	Charging Voltage (0x15)	CV mode	CC=0.6~4.48A
Normal 3S LI-ON Cells	12600mV	12.60V	IREF=0.7224*Icharge
			IREF=0.43V~3.24V

Kv
 Rinternal ic=514K Rec=3K R1=PR379=15.4K
 R2=PR381=31.6K
 R=514K//31.6K/(15.4K+3K)=11.372K
 r=514K//514K//31.6K=28.14K
 Vcell=0.175*Vadj+3.99V
 4.2V=0.175*Vadj+3.99V =>Vadj=1.2V
 Vadj=Vref*(R/(R+514K))+CALIBRATE*(r/(r+514K))
 1.1483=CALIBRATE*0.6046 =>CALIBRATE=1.899
 1.899=(4.2-(Vcell+A*0.175))*Kv=(4.2-(4.2+A*0.175))*Kv
 A=Vref*(R/(R+514K))=0.052
 Kv=9.451

Ki
 Vchlim=Iref*(PR46/(PR44+PR46))
 =Iref*(100K/(80.6K+100K))
 =Iref*0.5537
 Ichange=(165mV/PR22)*(Vchlim/3.3V)
 =165m/20m*(1/3.3V)*Iref*0.5537
 =1.3842*Iref
 Iref=0.7224*Ichange =>Ki=0.7224

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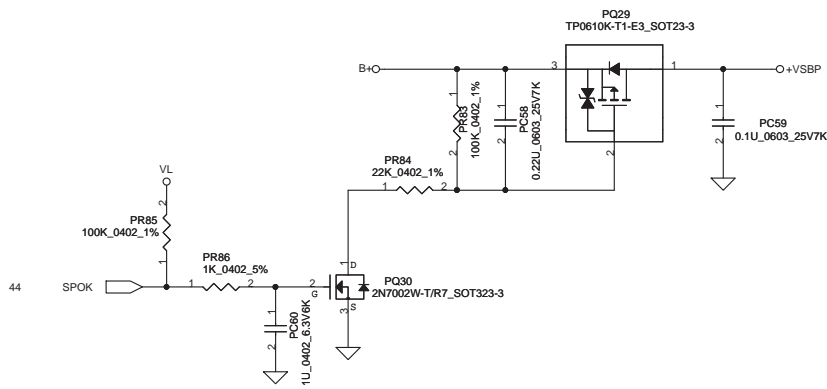
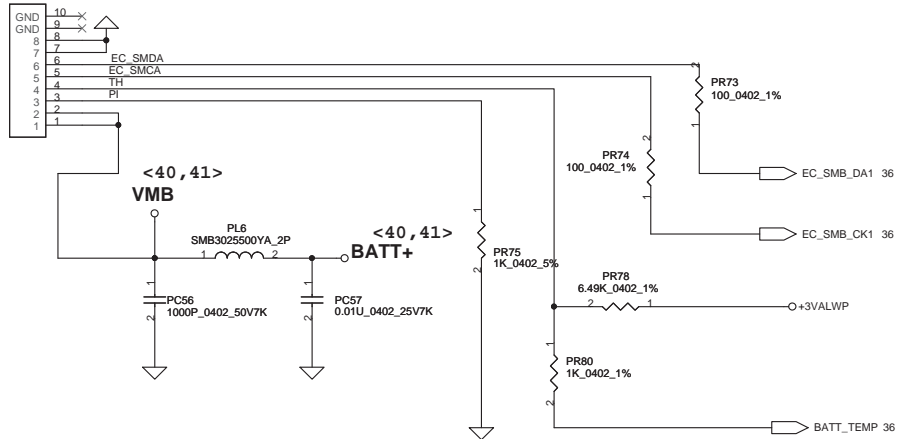
TONSEL=VREF (1)SMPS1=300KHZ (+5VALWP)
 (2)SMPS2=375KHZ(+3VALWP)

+3.3VALWP
 Ipeak=4.64A ; 1.2Ipeak=5.57A=Iocpmin; Imax=3.25A
 f=375KHz, L=4.7UH
 Rds(on)=15-18m ohm
 $1/2\Delta I = 1/2 * (19-3.3) * (3.3/19) / (375KHz * 4.7UH) = 0.773A$
 $V_{limin} = (10uA * 110Kohm) / 10 = 0.11V$
 $I_{limin} = 0.11V / (18m * 1.2) = 5.09A$
 $I_{limmax} = 0.11V / (15m * 1.2) = 6.11A$
 Iocp=5.863A~6.883A

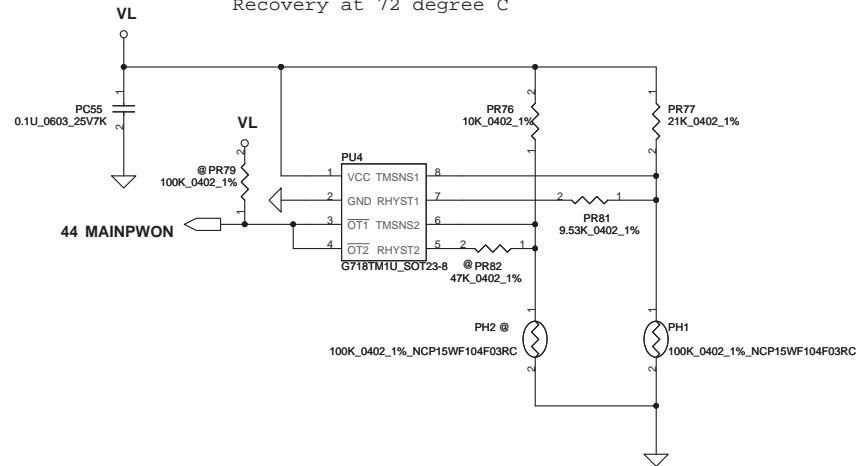
+5VALWP
 Ibudget=8.4A => 7A < Ibudget < 10A => Ipeak=7A 1.2Ipeak=8.4A; Imax=4.9A
 f=300KHz, L=4.7UH, Rentrtp=221K ohm
 Rds(on)=15-18m ohm
 $1/2\Delta I = 1/2 * (19-5) * (5/19) / (300KHz * 4.7UH) = 1.306A$
 $V_{limin} = (10uA * 154Kohm) / 10 = 0.154V$
 $I_{limin} = 0.154V / (18m * 1.2) = 7.12A$
 $I_{limmax} = 0.221V / (15m * 1.2) = 8.55A$
 Iocp=8.44A~9.86A

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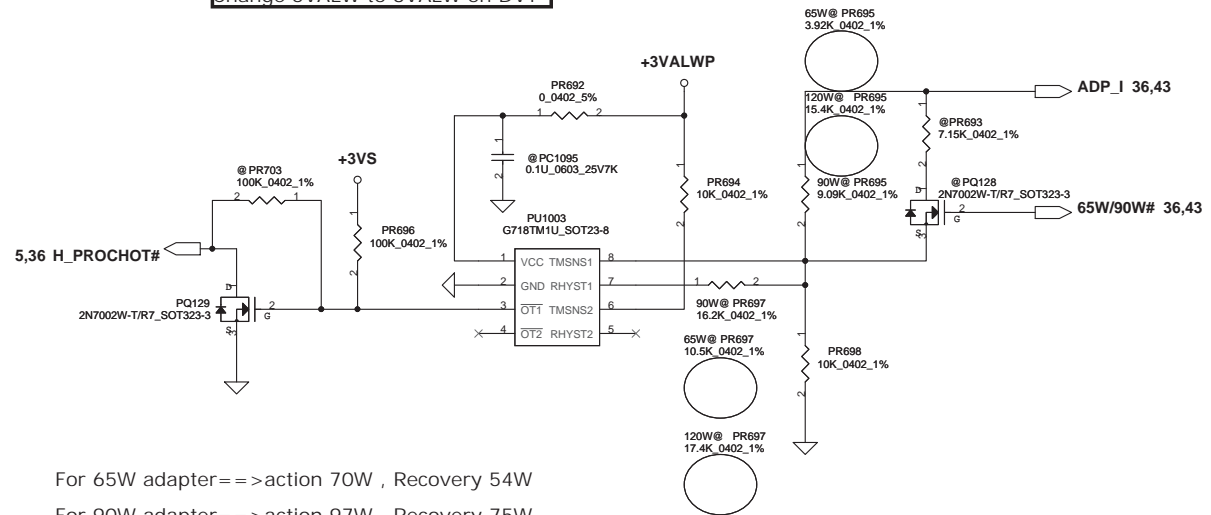
@PJ2
SUYIN_200275GR008G13GZR



PH1 under CPU botten side :
CPU thermal protection at 92 degree C
Recovery at 72 degree C

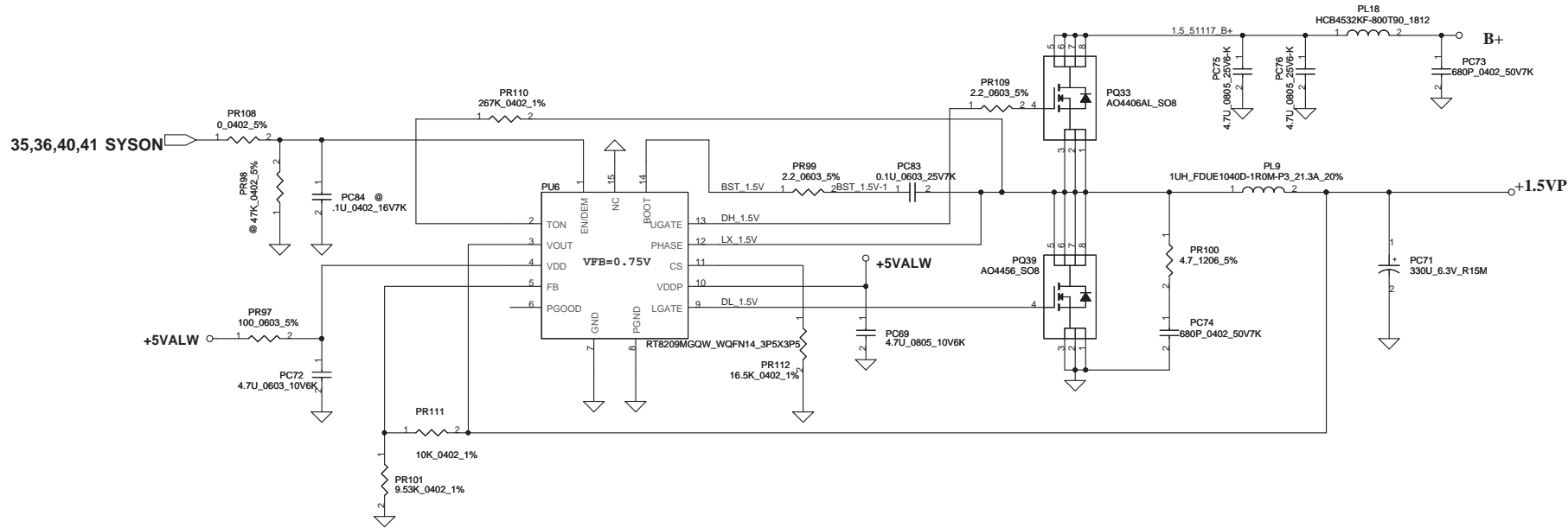


Change 5VALW to 3VALW on DVT



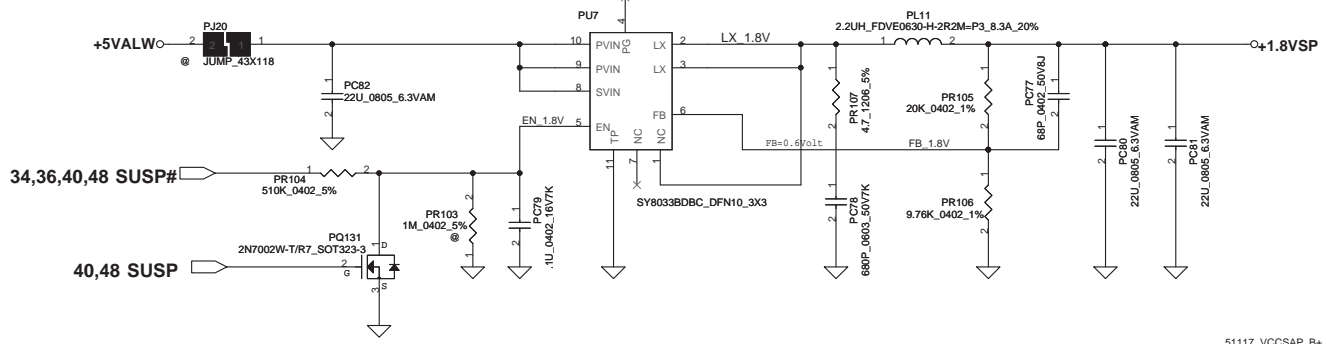
For 65W adapter==>action 70W , Recovery 54W
For 90W adapter==>action 97W , Recovery 75W
For 120W adapter==>action 135W , Recovery 100W

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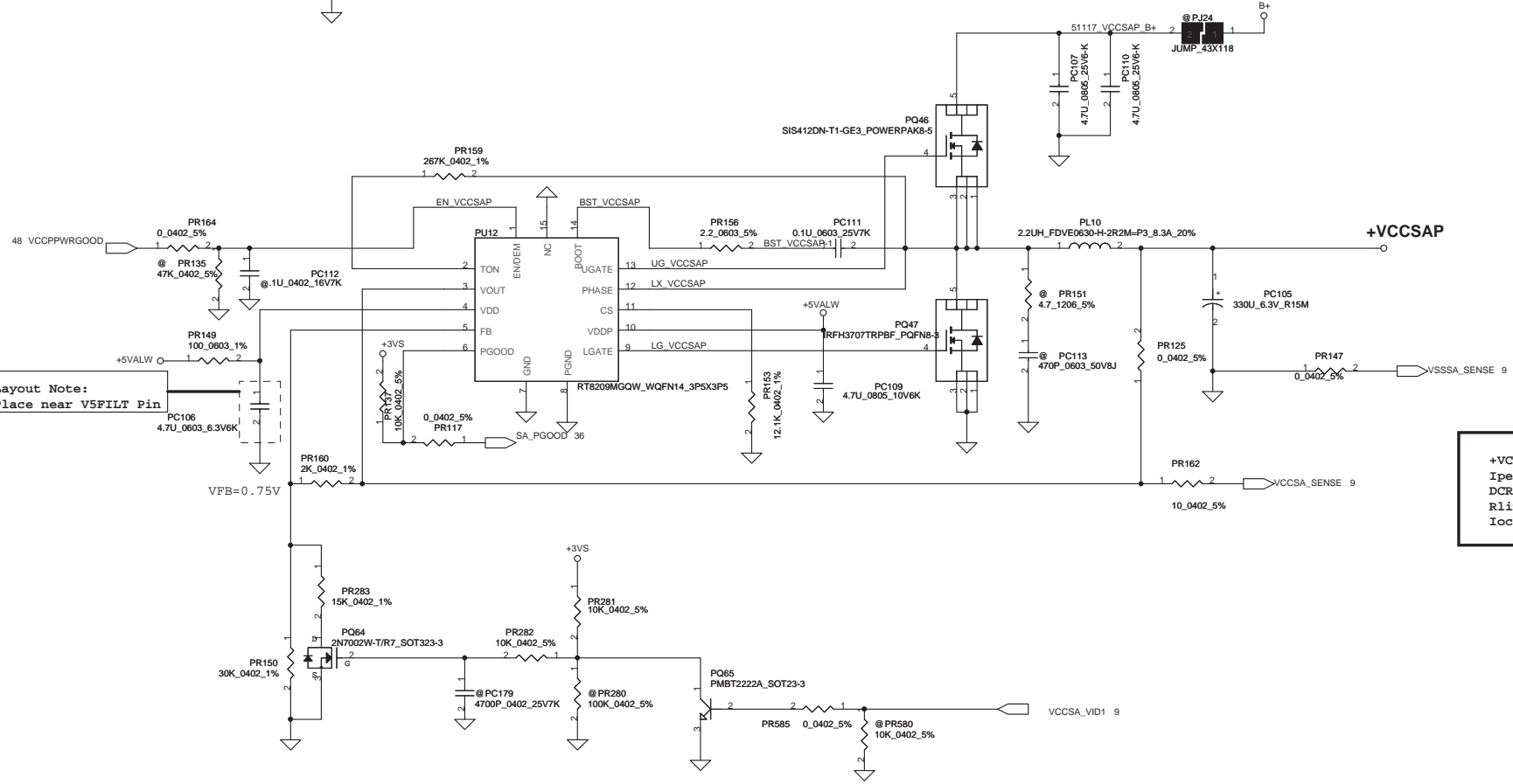


+1.5VP
 Ipeak=21.56A;1.2Ipeak=25.87A ;Imax=15.09A
 Rton=267K, Fsw=298KHz ,Rdson=4.5-5.6mohm
 Rtrip=16.5K
 Iocp=25.97A-42.41A

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1.8VSP
 Ipeak=3.35A ; 1.2Ipeak=4.02 ; Imax=2.345A
 Vout=0.6*(1+(20K/10K))=1.8V
 -DVT-



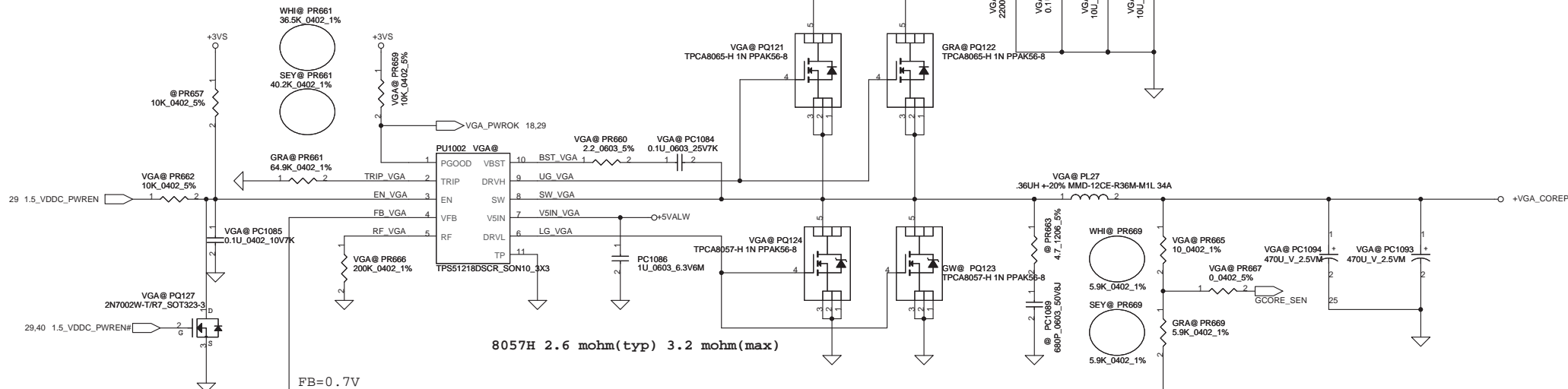
+VCCSAP
 Ipeak=6A , Imax=4.2A, 1.2Ipeak=7.2A
 DCR= 9 m(typ)-10 m(max)
 Rlimit=12.1K,Rds(on)=14.5-17.9mohm
 Iocp=7.24A-12.59A

Layout Note:
 Place near V5FILT Pin

VID[0]	VID[1]	VCCSA Vout	Require on 2011/ 2012	Required
0	0	0.9 V	Yes/Yes	Yes/Yes
0	1	0.8 V	Yes/Yes	Yes/Yes
1	1	0.75V	No/Yes	No/Yes
1	1	0.65V	No/Yes	No/Yes

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Note: Use VCCSA_SEL to switch High & Low Level for VID[1]

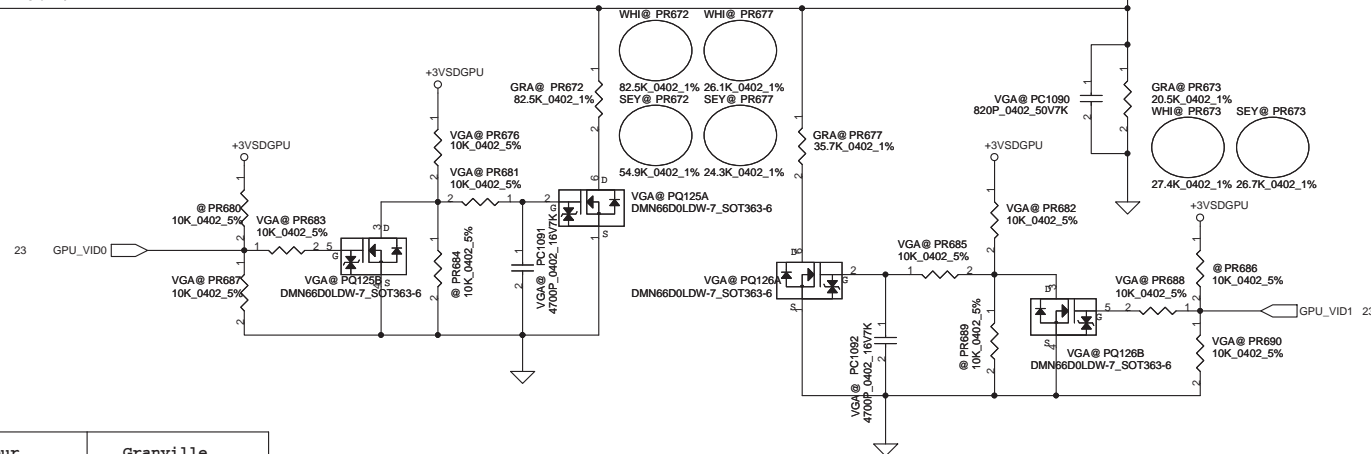


8057H 2.6 mohm(typ) 3.2 mohm(max)

FB=0.7V

Ipeak
Granville(35W) 47A
Whistler(25W) 27A(VDDC+VDDCI)
Seymour(15W) 14.2A(VDDC+VDDCI)

Switch freq. (RF pin setting)
 47K ==>450KHz
 100K ==>390KHz
 200K ==>350KHz (Currently setting)
 470K ==>300KHz



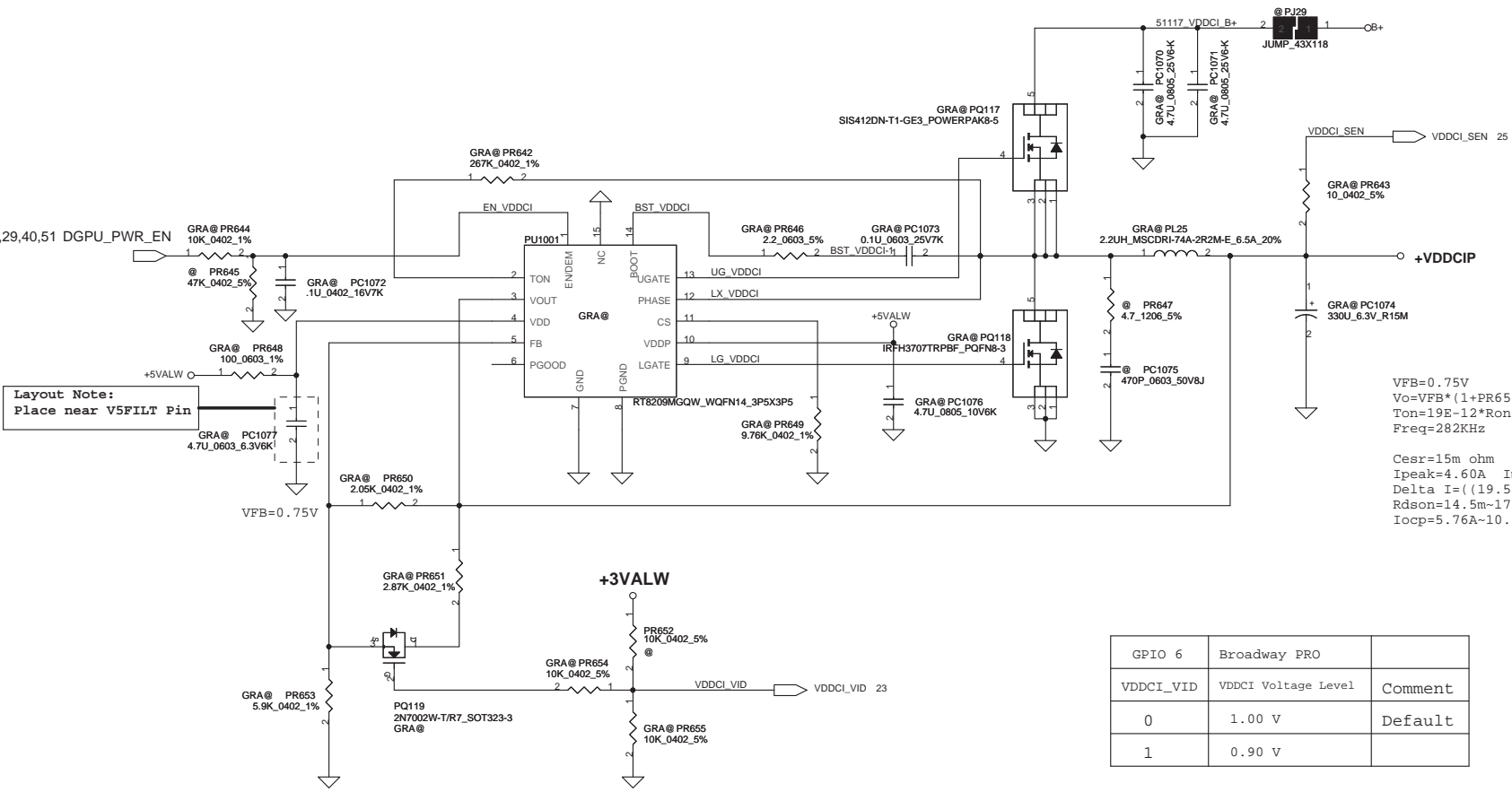
GPIO 15	GPIO 20	Whistler	Seymour	Granville
GPU_VID0	GPU_VID1	Core Voltage Level	Core Voltage Level	Core Voltage Level
1	1	0.85V	0.85V(0.855V)	0.90V
0	1	0.9V	0.9V(0.930V)	0.95V
1	0	1.00V	1.00V(1.025V)	1.00V
0	0		1.1V(1.100V)	1.05V

For Whistler
 $1/2\Delta I = 4.05A$
 $V_{trip} = 36.5K * 10\mu A = 0.365V$
 $I_{ocpmin} = 0.365V / (8 * 1.6m) + 1/2\Delta I = 28.51A + 4.05A = 32.56A$

For Granville
 $1/2\Delta I = 4.05A$
 $V_{trip} = R_{trip} * I_{trip} = 64.9K * 10\mu A = 0.649V$
 $I_{ocpmin} = (V_{trip} / (8 * R_{dson}) + 1/2\Delta I) = (0.649V / (8 * 1.6m \text{ ohm})) + 4.052A = 50.7A + 4.05A = 54.75A$

For Seymour
 $1/2\Delta I = 4.31A$
 $V_{trip} = 40.2K * 10\mu A = 0.402V$
 $I_{ocp} = 0.402V / (8 * 3.2m) + 1/2\Delta I = 15.70A + 4.31A = 20.01A$

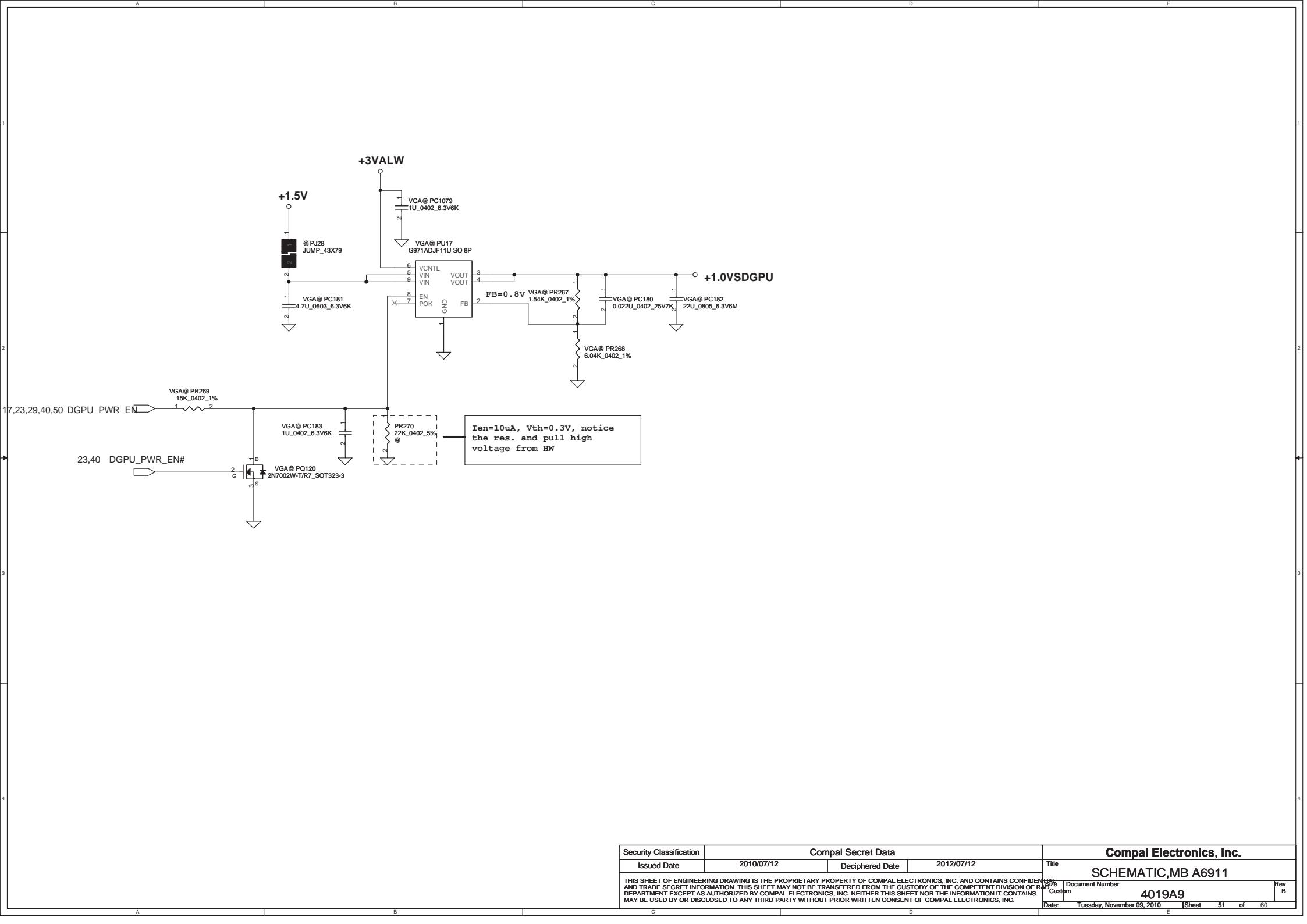
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Layout Note:
Place near V5FILT Pin

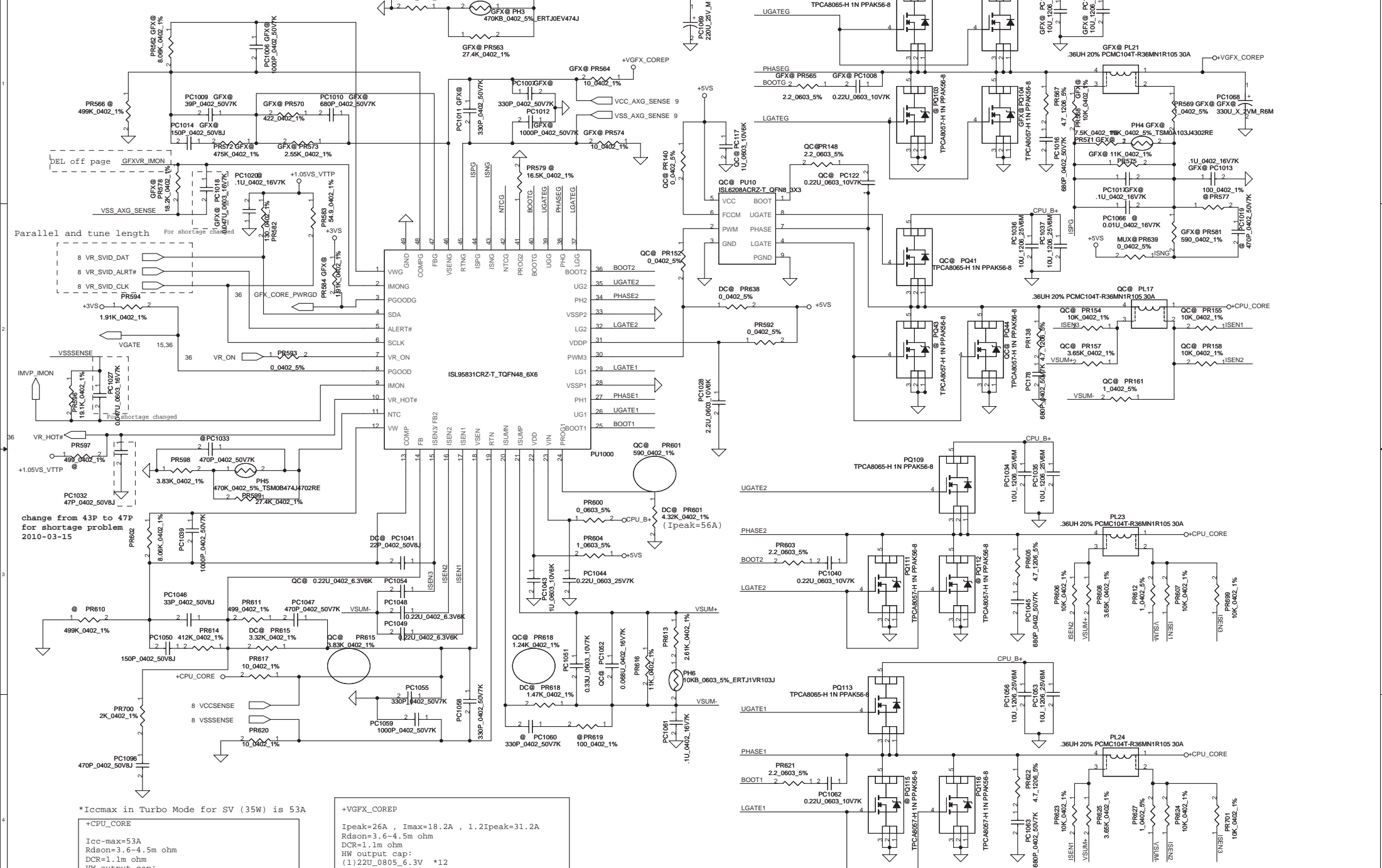
VFB=0.75V
 $V_o = VFB * (1 + PR650 / PR653) = 1.01V$
 $Ton = 19E - 12 * Ron * ((2/3) * V_o + 150mV) / Vin + 50ns = 2.4E - 7$
 Freq=282KHz
 Ccsr=15m ohm
 $I_{peak} = 4.60A$ $I_{max} = 2.70A$ $1.2I_{peak} = 5.52A$
 $\Delta I = ((19.5 - 1.0) * (1.0 / 19.5)) / (L * Freq) = 1.48A$
 $R_{dson} = 14.5m - 17.9m$ ohm
 $I_{ocp} = 5.76A - 10.19A$

GPIO 6	Broadway PRO	
VDDCI_VID	VDDCI Voltage Level	Comment
0	1.00 V	Default
1	0.90 V	



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Alert# PU resistor need close CPU, so the PU resistor in HW schematic. but DAT and CLK need close PWM-IC, so the PU resistor in POWER schematic.



Parallel and tune length For shortage changed

change from 43P to 47P for shortage problem 2010-03-15

*Iccmax in Turbo Mode for SV (35W) is 53A

+CPU_CORE
 Icc-max=53A
 Rds-on=3.6~4.5m ohm
 DCR=1.1m ohm
 HW output cap:
 (1)10U_0805_4V *10
 (2)22U_0805_6.3V *15
 (3)470U_D2_2V *4(ESR=4.5m ohm)

+VGF_X_COREP
 Ipeak=26A , Imax=18.2A , 1.2Ipeak=31.2A
 Rds-on=3.6~4.5m ohm
 DCR=1.1m ohm
 HW output cap:
 (1)22U_0805_6.3V *12
 (2)470U_D2_2V *2(ESR=4.5m ohm)

Rdroop is PR615
 Ri is PR618

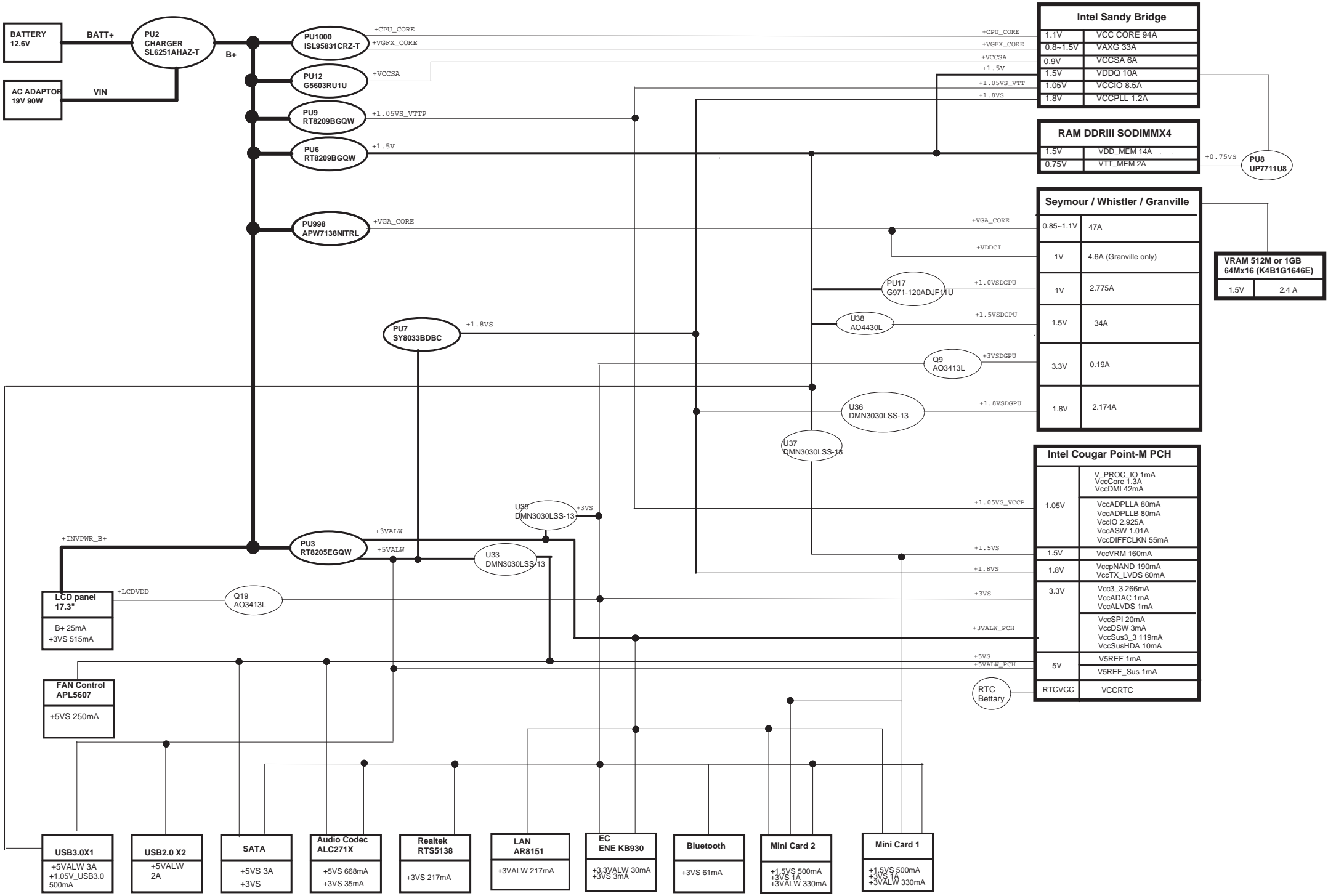
*Dual Core OCP setting value=70A
 *Qual Core OCP setting value=120A

*OCP setting value=40A

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	HW increase 1.8V voltage.	HW need to increase 1.8V voltage.	0.1	47	Change PR106 from SD034100280 to SD034976180.	2010/09/23	DVT
2	VGA Granville OVP issue.	Because VGA has happened OVP issue in Granville SKU, that is caused by output capacitor too small. change PC1094 to SGA00004200 to solve it. PC1088 must remove.	0.1	49	Add PC1094 to SGA00004200 and delete PC1088 SF000002000.	2010/09/23	DVT
3	1.8V Power sequence adjust.	HW adjust 1.8V power sequence.	0.1	47	change PR104 from SD028100380 to SD028150380.	2010/09/23	DVT
4	0.75V Power sequence adjust.	HW adjust 0.75V power sequence.	0.1	48	Change PR127 from SD028150380 to SD034267380.	2010/09/23	DVT
5	adjust +1.05VS_VTT power sequence	HW adjust +1.05VS_VTT power sequence	0.1	48	Change PC99 from SE107475K80 to SE076104K80.	2010/09/23	DVT
6	adjust +VDDCI power sequence	HW adjust +VDDCI power sequence	0.1	50	Change PR644 from SD034301380 to SD034100280.	2010/09/23	DVT
7	HW request to delete PR103.	HW request to delete PR103.	0.2	47	Delete PR103 SD028100480.	2010/09/28	DVT
8	PR104 BOM error.	PR104 BOM error for power sequence.	0.2	47	Change PR104 from SD034150380 to SD034510380.	2010/09/28	DVT
9	PR669 BOM error for Seymour only.	PR669 BOM error for Seymour only.	0.2	49	Change PR669 from SD034681180 to SD034590180.	2010/09/28	DVT
10	To same as P5WE0 VCCSAP choke.	To same as P5WE0 VCCSAP choke.	0.2	47	Change PL10 from SH000009Q00 to SH00000M700.	2010/09/28	DVT
11	HW request to add PQ130 and PQ131 to speed up to 放电.	HW request to add PQ130 and PQ131 to speed up to 放电.	0.3	47 48	Add PQ130 and PQ131 SB000006800.	2010/10/05	DVT
12	Remove chargeable RTC battery.	We reserve chargeable RTC battery to prevent over heat issue, Thermal team result is pass, so remove chargeable RTC battery.	0.3	42	Delete PR691 SD013000080 Change PR6 from SD013560080 to SD013000080.	2010/10/05	DVT
13	Change PL4 and PL5 to TOKO new part.	Change PL4 and PL5 to TOKO new part.	0.3	44	Change PL4 and PL5 from SH000006J80 to SH00000MB00	2010/10/05	DVT
14	for ISN issue.	for ISN issue.	0.3	43	Add PL30 SH000009Q00 Delete PL28 SM010018210	2010/10/05	DVT
15	to same as P5WE0 choke.	to same as P5WE0 choke.	0.3	47	Change PL10 and PL11 from SH000009Q00 to SH00000F800	2010/10/05	DVT
16	for QC+25WGPU and QC+35W GPU change CP point.	Because Acer deine QC with 25W/35W GPU to be 120W SKU, change CP point to meet Acer request.	0.3	43	Delete PQ20 SB000006800. Delete PR48 SD034255180 Change PR22 from SD000001F00 to SD021100B80.	2010/10/05	DVT
17	for QC+25WGPU and QC+35W GPU change CP point.	Because Acer deine QC with 25W/35W GPU to be 120W SKU, change CP point to meet Acer request.	0.3	43	Change PR47 from SD034121280 to SD034100180 Change PR50 from SD034200280 to SD034511280	2010/10/05	DVT
18	Modify adapter throttling at turbo mode setting point.	Modify adapter throttling at turbo mode setting point.	0.3	45	Add PR695 SD034154280 Add PR697 SD034174280	2010/10/05	DVT
19	CPU Transient responds issue.	Change CPU transient responds RC time constant.	0.4	52	Add PC1052 SE000003J80. Add PC1096 SE071471J80. Add PR700 SD034200180.	2010/10/07	DVT
20	for ISN issue.	for ISN issue.	0.4	43	Change PL30 from SH000009Q00 to SH00000M700.	2010/10/07	DVT
21	Make BOM same as P5WE0.	Make BOM same as P5WE0.	0.4	52	Change PL21,PL23,PL24 from SH000005680 to SH00000HK00.	2010/10/07	DVT
22	BOM loss.	Because BOM Config loss 65@ and 90W@, so miss PR695 and PR697.	0.5	45	Add PR695 SD034909180 9.09K_0402_1% ADD PR697 SD034162280 16.2K_0402_1%	2010/10/26	PVT
23	Modify CPU OCP.	Because original design is for 3 phase DC, now change to 2 phase DC, so modify OCP.	0.5	52	Change PR618 from SD034698080 to SD000009480	2010/10/26	PVT
24	Modify DC LL.	Because DC OCP was modified, must also update LL of DC.	0.5	52	Change PR615 from SD034215180 to SD034332180	2010/10/26	PVT

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Intel Sandy Bridge	
1.1V	VCC CORE 94A
0.8-1.5V	VAXG 33A
0.9V	VCCSA 6A
1.5V	VDDQ 10A
1.05V	VCCIO 8.5A
1.8V	VCCPLL 1.2A

RAM DDRIII SODIMMX4	
1.5V	VDD_MEM 14A
0.75V	VTT_MEM 2A

Seymour / Whistler / Granville	
0.85-1.1V	47A
1V	4.6A (Granville only)
1V	2.775A
1.5V	34A
3.3V	0.19A
1.8V	2.174A

Intel Cougar Point-M PCH	
1.05V	V_PROC_IO 1mA VccCore 1.3A VccDMI 42mA VccADPLL 80mA VccADPLL 80mA VccIO 2.925A VccASW 1.01A VccDIFFCLKN 55mA
1.5V	VccVRM 160mA
1.8V	VccpNAND 190mA VccTX_LVDS 60mA
3.3V	Vcc3_3 266mA VccDAC 1mA VccALVDS 1mA VccSPI 20mA VccDSW 3mA VccSus3_3 119mA VccSusHDA 10mA
5V	V5REF 1mA V5REF_Sus 1mA
RTC	RTCVCC VCCRTC

VRAM 512M or 1GB 64Mx16 (K4B1G1646E)	
1.5V	2.4 A

LCD panel 17.3"	
B+	25mA
+3VS	515mA

FAN Control APL5607	
+5VS	250mA

USB3.0X1	
+5VALW	3A
+1.05V_USB3.0	500mA

USB2.0 X2	
+5VALW	2A

SATA	
+5VS	3A
+3VS	

Audio Codec ALC271X	
+5VS	668mA
+3VS	35mA

Realtek RTS5138	
+3VS	217mA

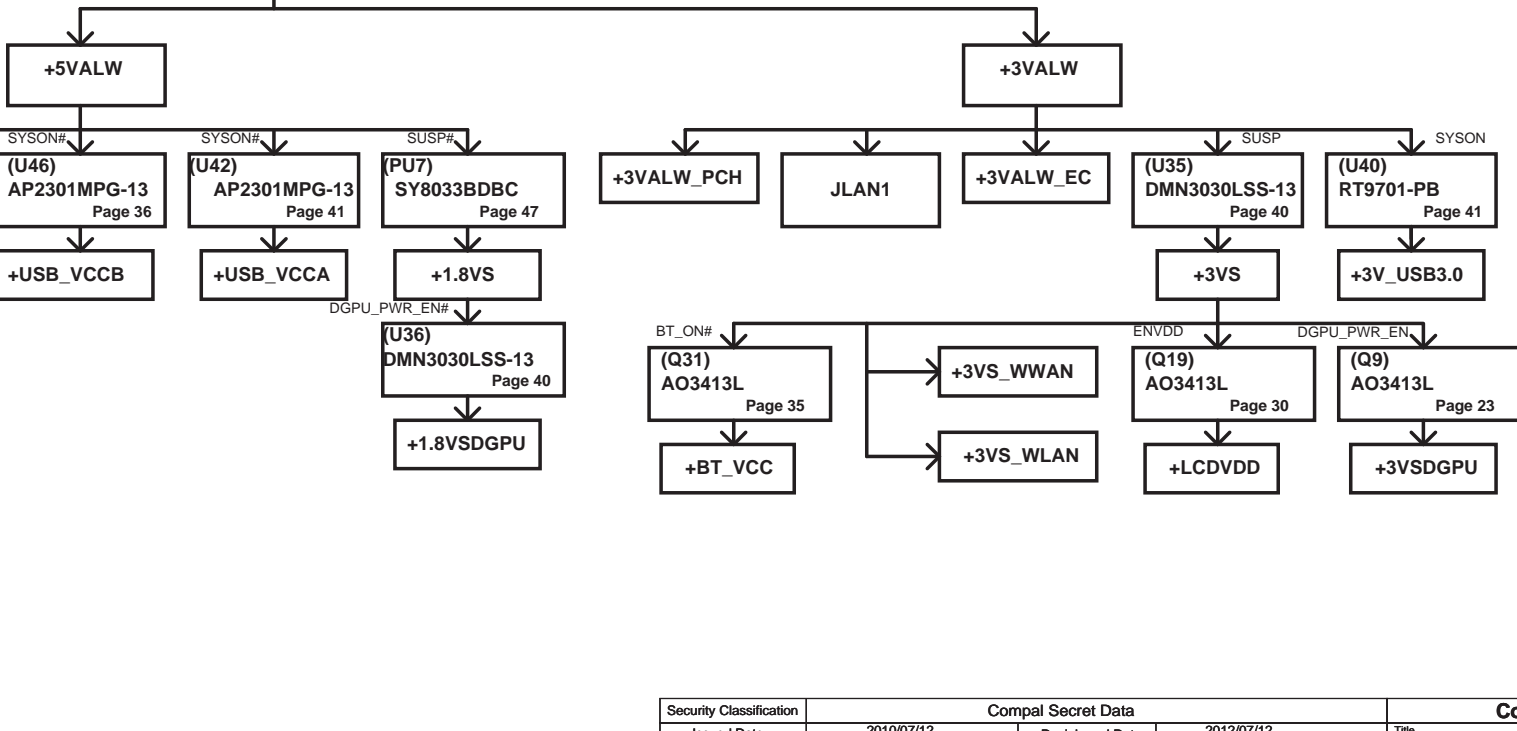
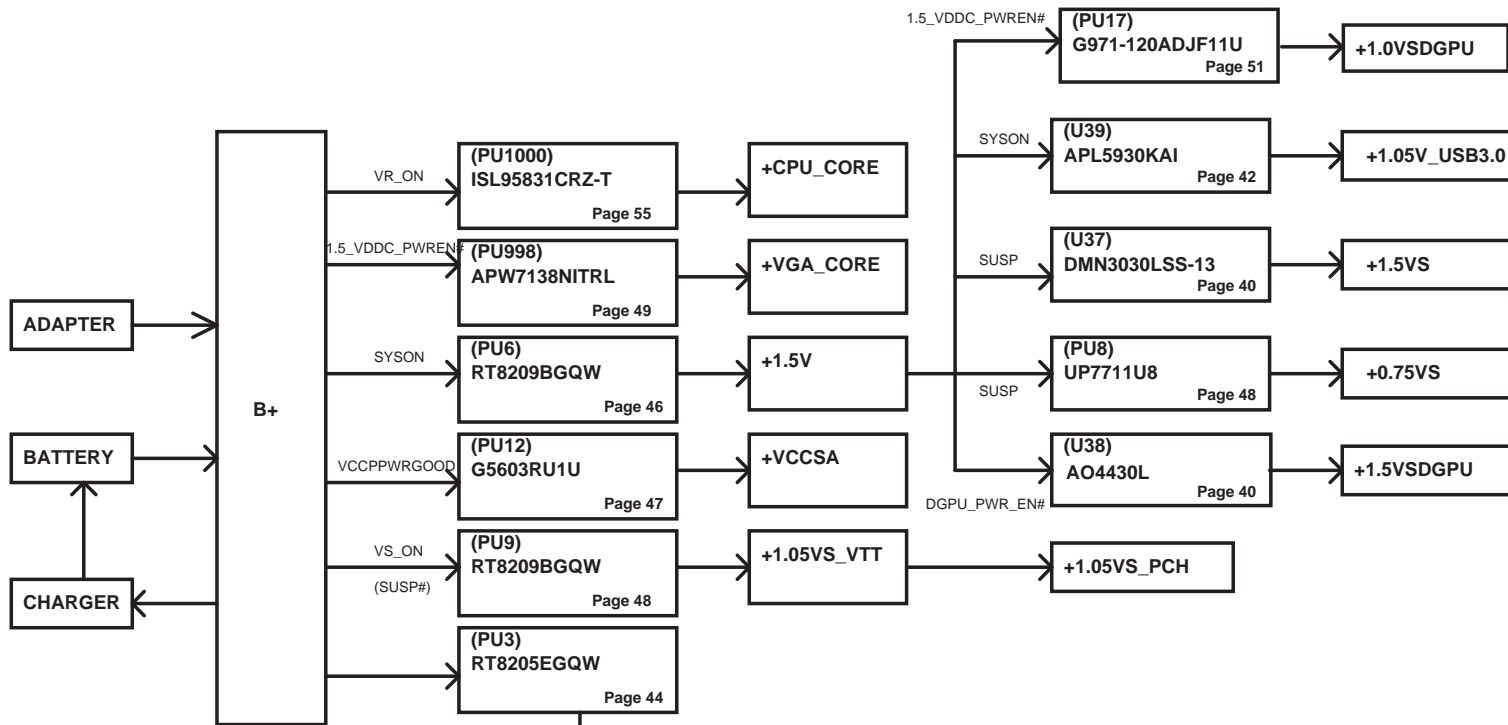
LAN AR8151	
+3VALW	217mA

EC ENE KB930	
+3.3VALW	30mA
+3VS	3mA

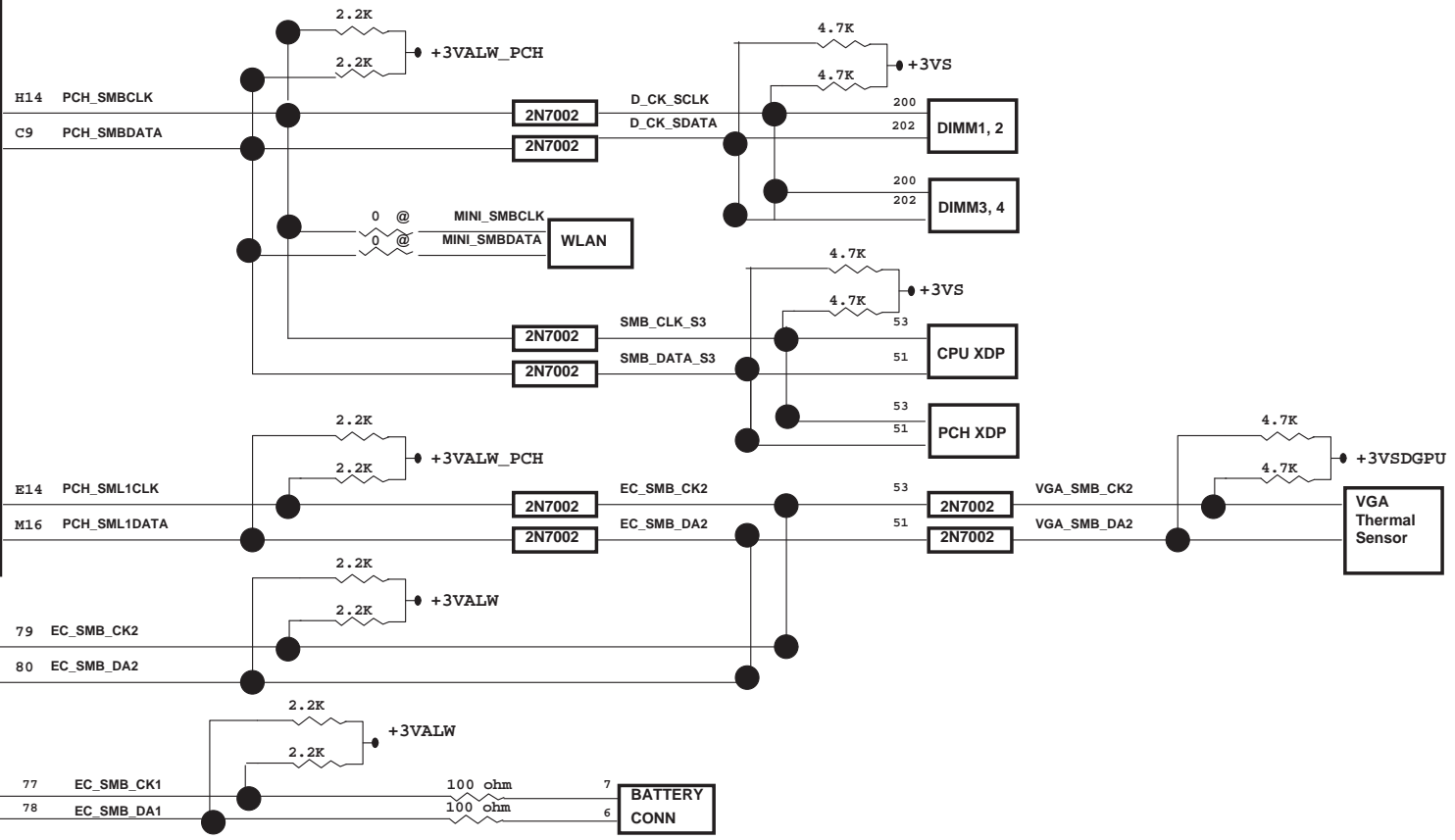
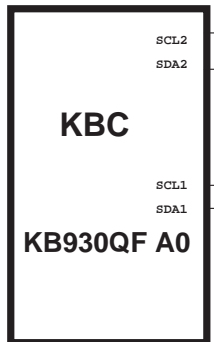
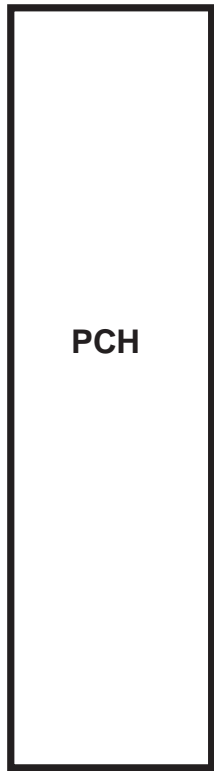
Bluetooth	
+3VS	61mA

Mini Card 2	
+1.5VS	500mA
+3VS 1A	
+3VALW	330mA

Mini Card 1	
+1.5VS	500mA
+3VS 1A	
+3VALW	330mA

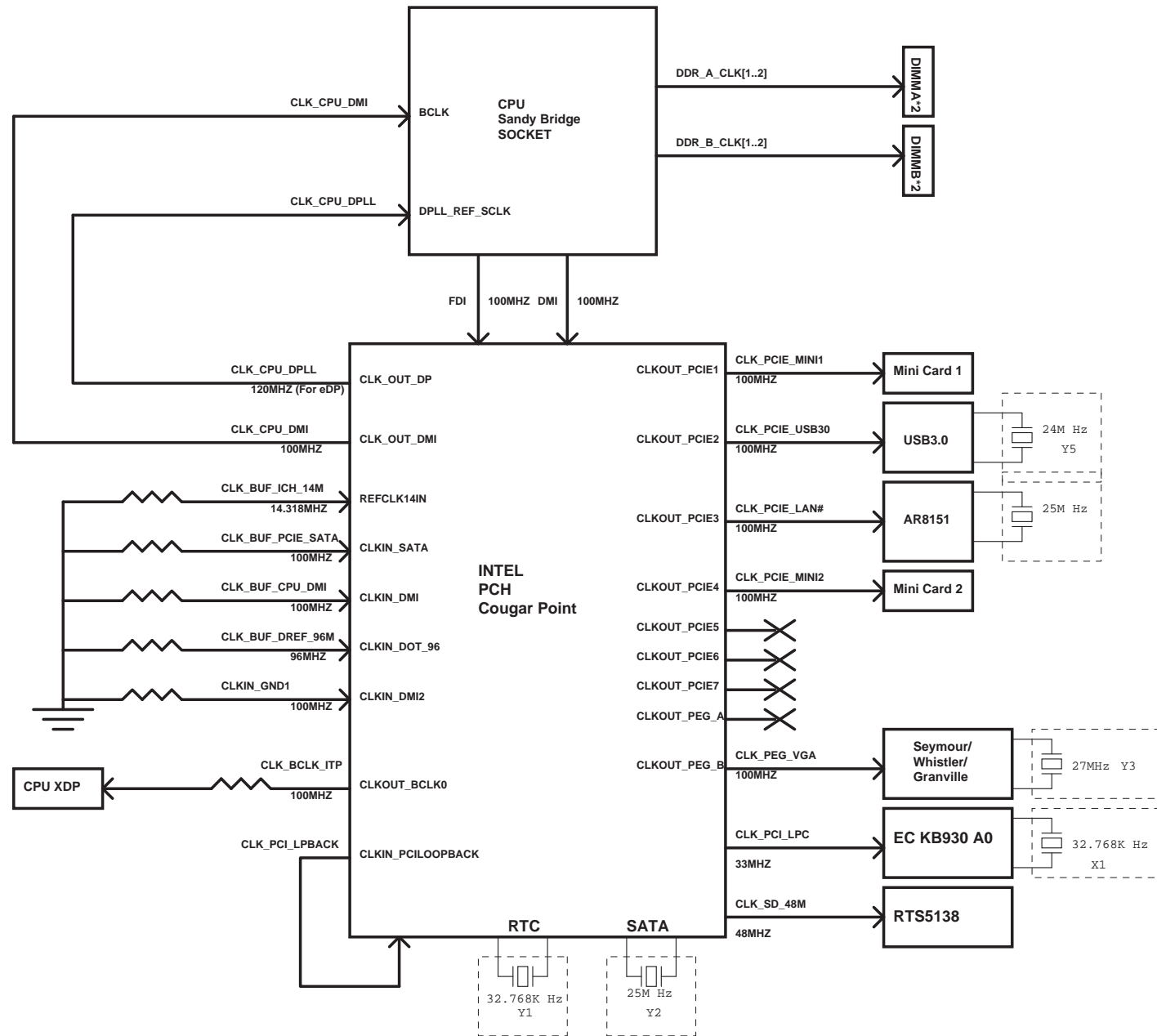


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PCH SM Bus address

Device	Address
ChannelA DIMM0	A0 1010 000X
DIMM1	A2 1010 001X
ChannelB DIMM0	A4 1010 010X
DIMM1	A6 1010 011X





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PCB


ZZZ
 LA-6911P MB Rev0: DA80000LC00
 LA-6911P MB Rev1: DA80000LC10
 LA-6911P MB with Small Board Rev1: DAZ
 LA-6911P REV0 MB

VGA

U30
 GRAN@ Granville PRO M2 A12:
 SA00004C820(S IC 216-0769024 A12 GRANVILLE PRO ABO!)

U30
 WHIS@ WHISTLER PRO M2 A11:
 SA00004C720(S IC 216-0810005 A11 WHISTLER PRO FCBGA 962P ABO !)


X76

ZZZ X76264BOL01
 X761@ X76264BOL01 VRAM 512M SAM P7YE0
 Samsung : SA000035720 (S IC D3 64MX16 K4W1G1646E-HC12 FBGA ABO!)


X76264BOL01 64Mx16x4 Seymour

ZZZ X76264BOL02
 X762@ X76264BOL02 VRAM 512M HYN P7YE0
 Hynix : SA000032420 (S IC D3 64MX16 H5TQ1G63BFR-12C FBGA ABO!)


X76264BOL02 64Mx16x4 Seymour

ZZZ X76264BOL03
 X763@ X76264BOL03 VRAM 1G SAM P7YE0
 Samsung : SA000035720 (S IC D3 64MX16 K4W1G1646E-HC12 FBGA ABO!)


X76264BOL03 64Mx16x8 Whistler/Granville

ZZZ X76264BOL04
 X764@ X76264BOL04 VRAM 1G HYN P7YE0
 Hynix : SA000032420 (S IC D3 64MX16 H5TQ1G63BFR-12C FBGA ABO!)


X76264BOL04 64Mx16x8 Whistler/Granville

ZZZ X76264BOL05
 X765@ X76264BOL05 VRAM 2G HYN P7YE0
 Hynix : SA00003VS10 (S IC D3 128M16 H5TQ2G63BFR-12C FBGA ABO!)


X76264BOL05 128Mx16x8 Whistler/Granville

ZZZ X76264BOL06
 X766@ X76264BOL06 VRAM 2G SAM P7YE0
 Samsung : SA00003MQ60 (S IC D3 128M16 K4W2G1646C-HC12 FBGA ABO!)

X76264BOL06 128Mx16x8 Whistler/Granville

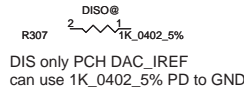
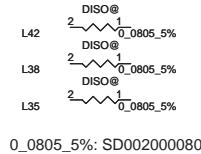
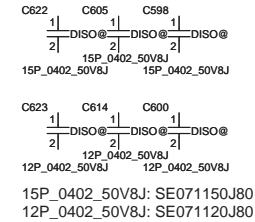
ZZZ X76264BOL07
 X767@ X76264BOL07 VRAM 1G SAM P7YE0
 Samsung : SA00003MQ60 (S IC D3 128M16 K4W2G1646C-HC12 FBGA ABO!)

X76264BOL07 128Mx16x4 Seymour

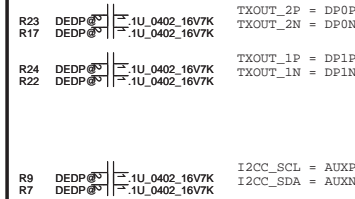
ZZZ X76264BOL08
 X768@ X76264BOL08 VRAM 1G HYN P7YE0
 Hynix : SA00003VS10 (S IC D3 128M16 H5TQ2G63BFR-12C FBGA ABO!)

X76264BOL08 128Mx16x4 Seymour

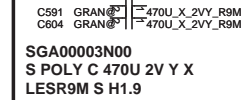
CRT Option Components



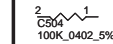
DIS EDP Option Components



Granville VGA_CORE CAP Option



EC susclk/crystal Option Components



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0923:
 REWORK:
 ADD Q8 DMN66D0LDW-7(SB00000DH00) & change BOM structure to DIS@(DIS@ Granville can't power on issue)
 R72 100K_0402_5%(SD028100380)change BOM structure to DIS@(DIS@ Granville can't power on issue)
 R674 4.7K PH change BOM structure to @(+3VS GPIO19 leakage)
 D31 change BOM structure to @(EC debug CLK leakage)
 R531,R530 change BOM structure to DISO@(HSYN:VSYNC 11: Audio for both DisplayPort and HDMI)
 ADD C591 C604 BOM option
 (Seymour/Whistler option NOGRAN@ SGA20331E10 S POLY C 330U 2V 9mohm H1.9)
 (Granville option GRAN@ SGA00004200 S POLY C 470U 2V M D2 LESR4.5M SX H1.9)
 C746,C750 change from SF000001500 to SF000001580

Power sequence:
 1. BOT (adjust +5VS power sequence)
 R698 change from 200K to 100K_0402_5% (SD028100380)
 2. BOT (adjust +1.8VS power sequence)
 PR104 change from 100K to 510K_0402_5%(SD028510380)
 remove PR103 1M_0402_5%
 3. TOP (adjust +1.5VS power sequence)
 R67 change from 510K_0402_5% to 750K_0402_5%(SD028750380)
 4. TOP (adjust +0.75VS power sequence)
 PR127 change from 150K_0402_5% to 267K_0402_1%(SD034267380)
 5. TOP (adjust +1.05VS_VTT power sequence)
 PC99 change from 4.7U to .1U_0402_16V7K (SE076104K80)
 6. TOP (adjust +1.5VSDGPU power sequence)
 R113 510K change to 100K_0402_1% (SD034100380)
 7. BOT (adjust +VDDCI power sequence)
 PR644 301K change to 10K_0402_1% (SD034100280)

Power:
 PR101 change from 10K to 9.53K (adjust +1.5V power)
 PR106 change from 10K to 9.76K (adjust +1.8VS power)
 Layout:
 D21 change to SC600000B00 (for sourcer 2nd source)
 DEL C590,C603 (DEL colay Cap)
 L24,25,27,30,31 change from SM010004010 to SM010015410
 BATT Blue light place at front side
 H1 change H3P0 to H4P6
 DEL LED1,LED2,LED3,LED4

0924:
 Q37,Q39,Q40,Q41, change from SB00000FG00 to SB00000FG10
 U7 change from SB000007000 to SB000007010
 USB3.0 schmetic change to unpop
 XDP change to unpop
 U19 A10,N10,P10,B12 connect to GND

0925:
 R249 change from U15.2 to U15.1(footprint issue)
 R105 change form 10K to 10_0402_5%(SD028100A80)
 R422 change BOM structure to @(crystal issue debug port1.2)
 R422 change +3VS to +3VALW_PCH (GPIO28)
 R674 change BOM structure to @(leakage issue debug port1.2)
 R674 change +3VALW_PCH to +3VS (GPIO19)
 ADD LED11 pop WLAN_LED#(SC500007700),LED12 @ MEDIA_LED#(SC591NB5A30)
 LED10 WLAN_LED#(SC500007700) change BOM structure to @
 DEL D9,D10 USB3.0 old ESD diode
 ADD D32 new USB3.0 ESD diode (SC300001D00)
 DEL R238,R250,C401 USB3.0 conn PD resistor & CAP
 EMI request:
 R595,R596 change to @ L47 change to POP(USB2.0 common mode choke)

0927:
 Audio vender suggest:
 C913 change BOM structure to @
 ADD C702 22K_0402_5%(SD028220280)
 change USB conn to USB2.0(SUYIN_020133GB004M25MZL_4P-T)
 modify Debug port note(GPIO19 PH +3VS GPIO28 PH +3VALW_PCH)
 R667,R666 change BOM structure to @(XDP CLK source)
 change SW4,SW5 BOM structure to @ (debug PWRBTN)
 change R432,R435,R437 from 1K_0402_5% to 300_0402_5%(orange LED resistor)
 change USB3.0 schmetic BOM structure back to USB3@
 C746,C750 change from SF000001500 to SF000001580
 D4,D5 change from SC5H491D010(S SCH DIO CH491DPT SOT-23) to SC500002000(S SCH DIO RB491D SOT-23 PANJIT)
 Q29,Q33,Q36 change from SB934130020(S TR A034113L 1P SOT23-3) to SB000006R10(S TR A034119L 1P SOT23-3)

0928:
 DEL R468
 JMINI1.24 change power source from +3VS to +3VS_WLAN
 DEL R613
 JMINI2.24change power source from +3VS to +3VS_WWAN
 DEL R352
 change power source from +XDPWR_SDPWR MSPWR to +CARDPWR
 Q21 change from SB324110080(2SC2411K) to SB039040020(MMBT3904)
 Change JUSB2 footprint to "SUYIN_020173GB004M25MZL_4P"
 ADD R613 1M PD to GND(HDA_SYNC_PCH_R)
 ADD SLP_A# at U37.G10 test point(for DFT request)
 ADD JTAG_TDI at U30.AN23 test point(for DFT request)
 ADD JTAG_TDO at U30.AM24 test point(for DFT request)
 JREAD1 change conn from TAITW_R013-P12-HM_44P_NR to TAITW_R013-P17-HM_40P_NR

0929:
 DEL Rechargeable RTC schematic D21,R425,C551

0930:
 R534,R540 change from 100_0402_1% to 1K_0402_5%(SD028100180)(DGL1.5 change save cost)
 C744,C745 change from 18P_0402_50V8J to 27P_0402_50V8J(SE071270J80)(25Mhz Crystal modify)
 R357,R358,R330,R331,R345,R346,R387,R393,R292 change BOM structure to @ (10K_0402_5%)PD to GND(DGL1.5 unuse CLK NC)
 R666,R667 change BOM structure to @(XDP unuse)
 R573,R575,R571,R572,R562,R564,R567,R570 DEL option 499_0402_1% leave 680_0402_5%
 R318,R332 change from 0ohm to 22_0402_5%(SD028220A80)
 C448,C483 change to 4.7P_0402_50V8J(SE07147AC80)
 L47 change to 67ohm common mode choke CHENG HANN WCM2012F2SF-670T04(SM070000S80)

1025:
 R370,R413 change from SD028100380(100K_0402_5%) to SD028200380(200K_0402_5%)
 PCH_GPIO1 change net to WL_EN#
 LVDS
 Add +5VS (Pin34) & USB20_N4/P4 (Pin35, 36)
 change EDP_HPD to Pin18
 PCH side add USB20_N4/P4 (Pin35, 36)

For eDP interface AUX channel, please request Layout routing as differential signal to follow eDP Layout Guide.
 (VGA_LCD_CLK & VGA_LCD_DATA / I2CC_SCL & I2CC_SDA)

DEL DDR DM
 R50,R58,R59,R48,R56,R51,R60,R49 DIMMA
 R39,R52,R44,R43,R46,R38,R45,R40 DIMMA
 R77,R73,R109,R112,R180,R181,R192,R206 DIMMB
 R64,R83,R108,R115,R179,R183,R189,R208 DIMMB

1026:
 C604,C591 change from SGA00004200(470 4.5mohm)to SGA00003N00(470 9mohm)
 Pop R257(SD028100380 100K_0402_5%),R622(SD028820180 8.2K_0402_5%) Board ID
 R443 change from 100K_0402_5% to 10K_0402_5% (SD028100280)

remove R471,R622(JMINI1,JMINI2 Pin42 0ohm series resistor)
 J1,J2 change location to J6,J7
 remove R222 0ohm_0402 (H_CUPWRGRD_R)
 remove R423,0ohm_0402 (MINI1_CLKREQ#_R)
 remove R392 0ohm_0402 (LAN_CLKREQ#_R)
 remove R685 0ohm_0402 (MINI2_CLKREQ#_R)
 remove R655 0ohm_0402 (WAKE#)
 remove R636 0ohm_0402 (PCH_RSMRST#)
 remove R377 0ohm_0402 (SDS_PWR_DM_ACK)
 remove R339 0ohm_0402 (PBTN_OUT#)
 remove R359 0ohm_0402 (DGPU_HOLD_RST#)
 remove R16 0ohm_0402 (BKOPF#)
 remove R448 0ohm_0402 (VGA_EDP_DET)
 remove R533 0ohm_0402 (VGA_HDMI_DET)
 remove R627 0ohm_0603 (+SP1_VCC)

ADD R39 0ohm_0402 LOCAL_DIM
 ADD R38 0ohm_0402 COLOR_ENG_EN

C242,C653,C332,C354,C678 change footprint to C_X(2pin)

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