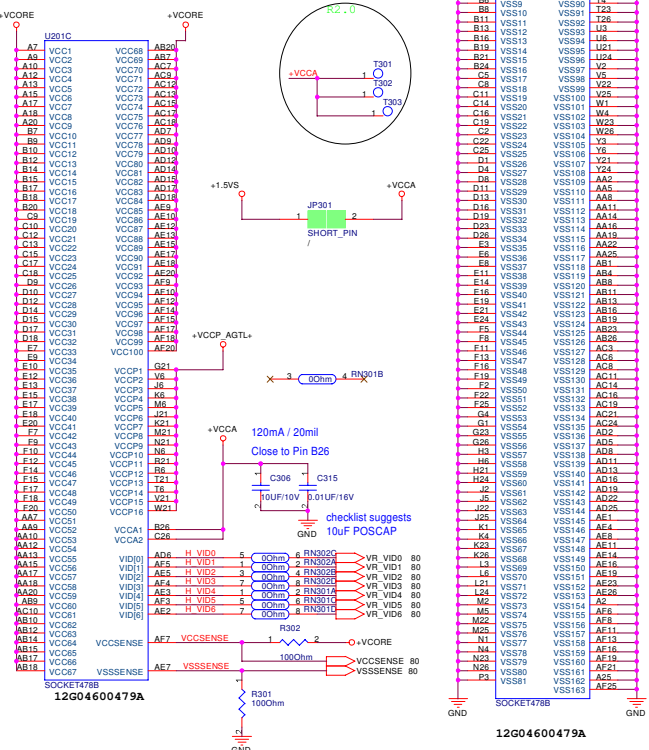
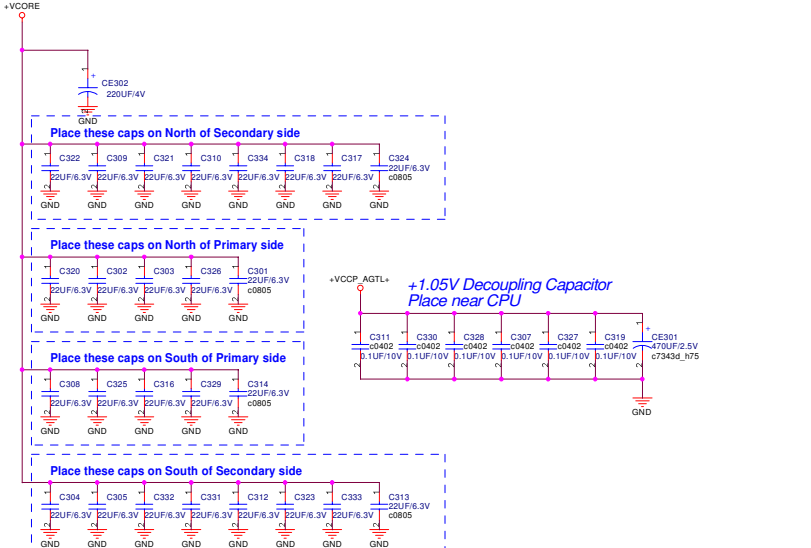


YUNAH FSB667			
LFM	TYP	HFH	
VCC	1.14V	1.2V	1.356V
C4	C3	C0	
ICC	0.9A	7.59A	27A

YUNAH FSB667			
Min	TYP	Max	
VCCP	0.997V	1.05V	1.102V
Min	TYP	Max	
ICCP			2.5A

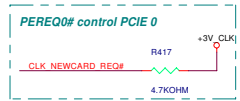
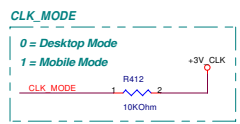
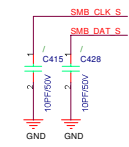
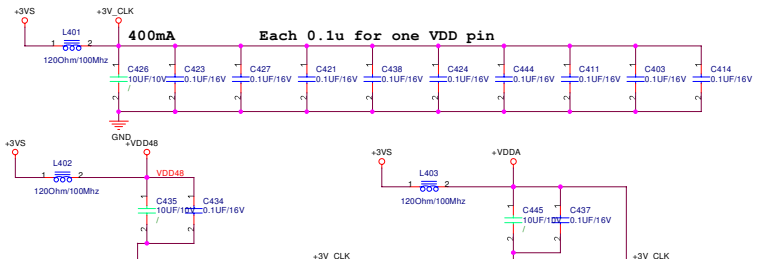
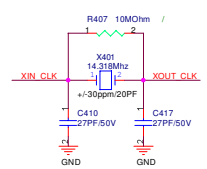


J201D		
A4	VSS1	VSS2
A8	VSS3	VSS4
A11	VSS5	VSS6
A14	VSS7	VSS8
A16	VSS9	VSS10
A18	VSS11	VSS12
A23	VSS13	VSS14
A25	VSS15	VSS16
A26	VSS17	VSS18
B6	VSS19	VSS20
B8	VSS21	VSS22
B11	VSS23	VSS24
B13	VSS25	VSS26
B16	VSS27	VSS28
B19	VSS29	VSS30
B21	VSS31	VSS32
B24	VSS33	VSS34
B25	VSS35	VSS36
C8	VSS37	VSS38
C9	VSS39	VSS40
C11	VSS41	VSS42
C14	VSS43	VSS44
C16	VSS45	VSS46
C19	VSS47	VSS48
C22	VSS49	VSS50
C23	VSS51	VSS52
C24	VSS53	VSS54
D1	VSS55	VSS56
D11	VSS57	VSS58
D13	VSS59	VSS60
D19	VSS61	VSS62
D23	VSS63	VSS64
D28	VSS65	VSS66
E6	VSS67	VSS68
E8	VSS69	VSS70
E11	VSS71	VSS72
E14	VSS73	VSS74
E16	VSS75	VSS76
E19	VSS77	VSS78
E21	VSS79	VSS80
E24	VSS81	VSS82
F8	VSS83	VSS84
F11	VSS85	VSS86
F13	VSS87	VSS88
F16	VSS89	VSS90
F19	VSS91	VSS92
F22	VSS93	VSS94
F25	VSS95	VSS96
F26	VSS97	VSS98
G4	VSS99	VSS100
G1	VSS101	VSS102
G2	VSS103	VSS104
G28	VSS105	VSS106
H3	VSS107	VSS108
H6	VSS109	VSS110
H11	VSS111	VSS112
H2	VSS113	VSS114
H21	VSS115	VSS116
H24	VSS117	VSS118
J2	VSS119	VSS120
J22	VSS121	VSS122
J25	VSS123	VSS124
K1	VSS125	VSS126
K4	VSS127	VSS128
K28	VSS129	VSS130
L3	VSS131	VSS132
L6	VSS133	VSS134
L21	VSS135	VSS136
L24	VSS137	VSS138
M2	VSS139	VSS140
M22	VSS141	VSS142
M25	VSS143	VSS144
N1	VSS145	VSS146
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N31	VSS151	VSS152
N38	VSS153	VSS154
P3	VSS155	VSS156

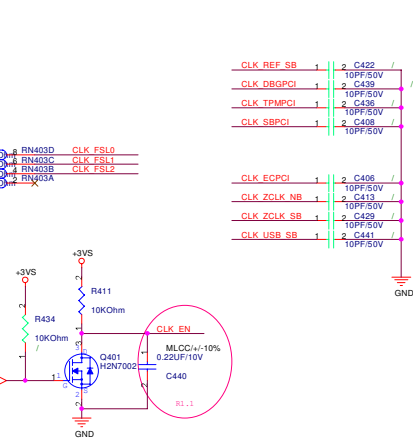
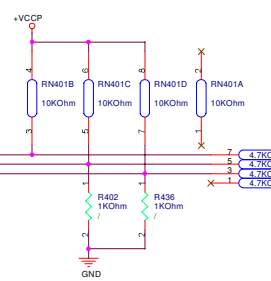


Layout Note:
 VCCSENSE/VSSSENSE lines between the CPU and the VR should have a trace width of 18 mils on 7 mils spacing, with a trace impedance of Zo=27.4 Ohm.
 The VCCSENSE/VSSSENSE should be length matched to within 25 mils.
 These resistors should be placed within 2 inch of the CPU.

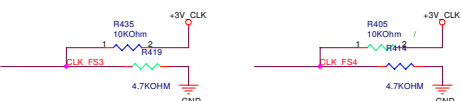
ASUS		Title : Yonah CPU (2)	
ASUSTEK COMPUTER INC		Engineer: Hawk Zhu	
Size	Project Name	Rev	
A3	FSV	1.0	
Date: 08/23/2007	Sheet: 3	of	94



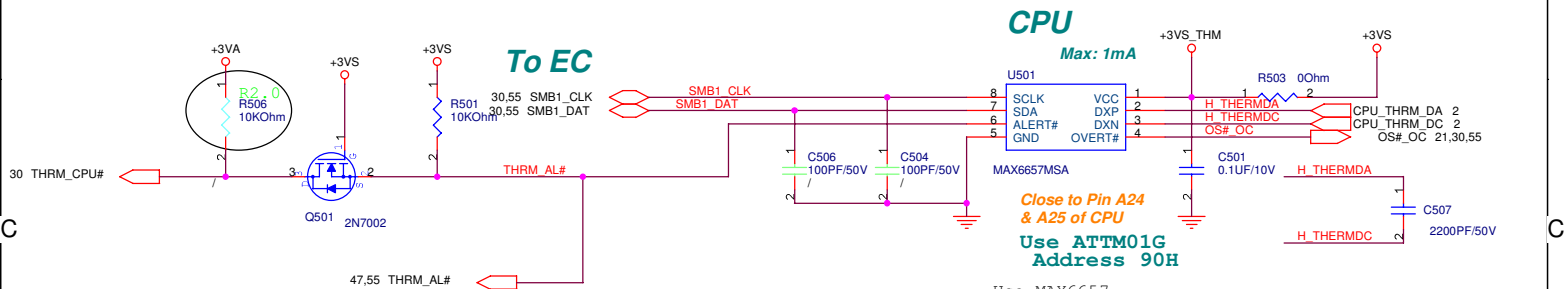
FS4	FS3	FSL2	FSL1	FSL0	CPU	PCI	ZCLK	PCIE	SATA
0	1	0	0	1	133	33	133	100	100
0	1	0	1	1	166	33	133	100	100



CLK_ITP_BCLK	1	2	C404
CLK_ITP_BCLK#	1	2	C401
CLK_CPU_BCLK	1	2	C402
CLK_CPU_BCLK#	1	2	C403
CLK_NB_BCLK	1	2	C412
CLK_NB_BCLK#	1	2	C411
CLK_PCIE_NB	1	2	C419
CLK_PCIE_NB#	1	2	C418
CLK_PCIE_SB	1	2	C409
CLK_PCIE_SB#	1	2	C410
PCIE_REFCLK+	1	2	C420
PCIE_REFCLK-	1	2	C421
CLK_PCIE_MINICARD+	1	2	C424
CLK_PCIE_MINICARD-	1	2	C423
CLK_PCIE_NEWCARD+	1	2	C430
CLK_PCIE_NEWCARD-	1	2	C429
CLK_USB_NEWCARD+	1	2	C419
CLK_USB_NEWCARD-	1	2	C418



Thermal Sensor

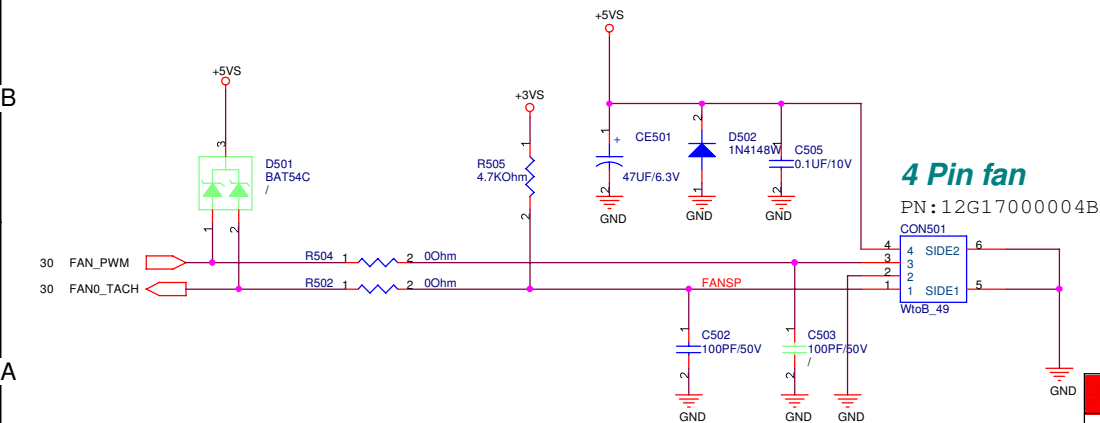


Route H_THERMDA and H_THERMDC on the same layer

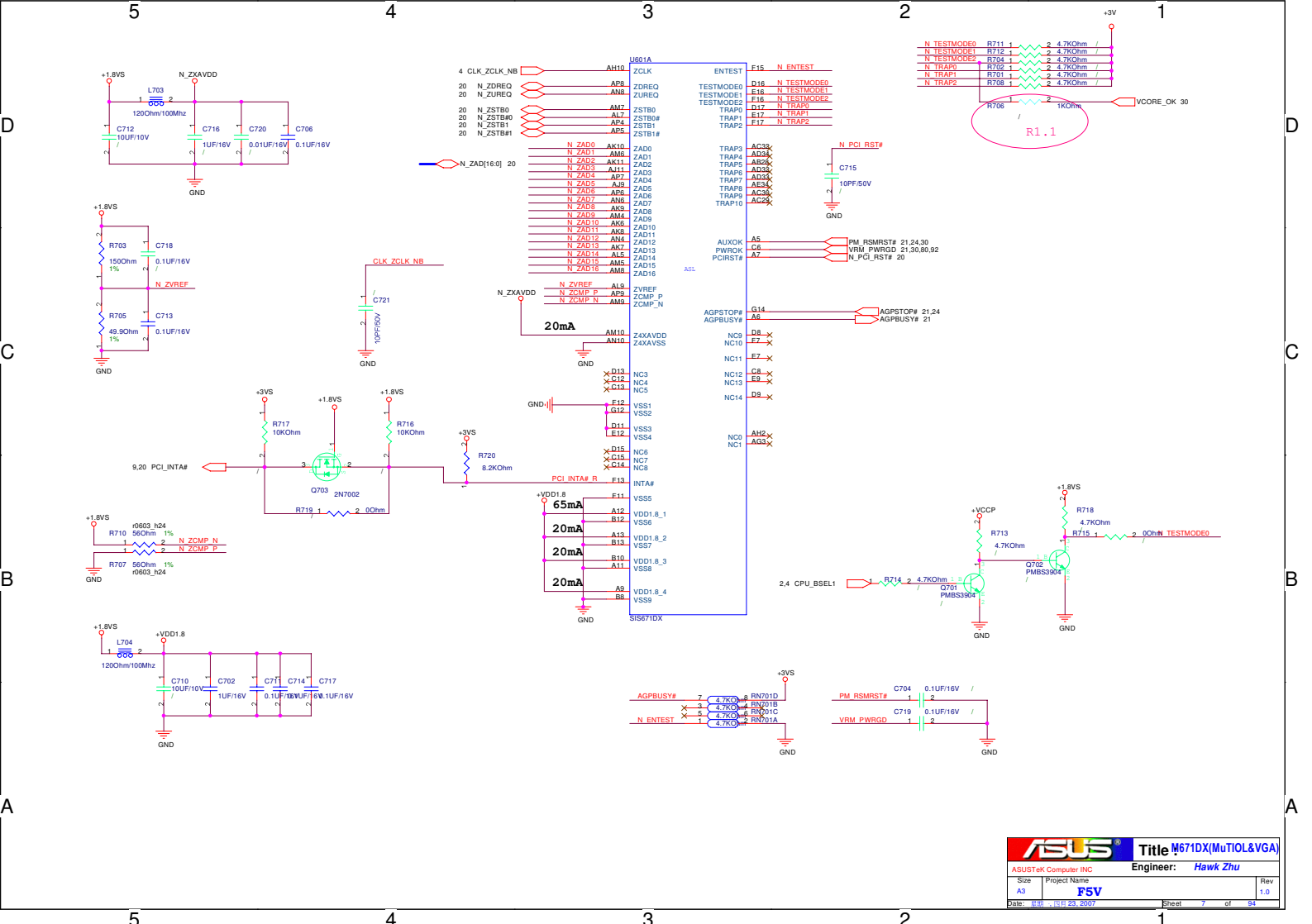
-----OTHER SIGNALS
=====GND
-----H_THERMDA(10 mils)
-----H_THERMDC(10 mils)
-----GND
-----OTHER SIGNALS

Avoid FSB,Power

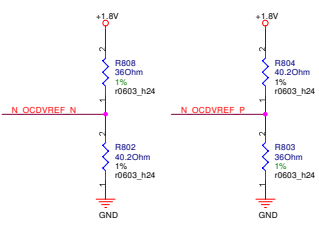
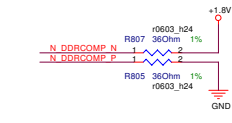
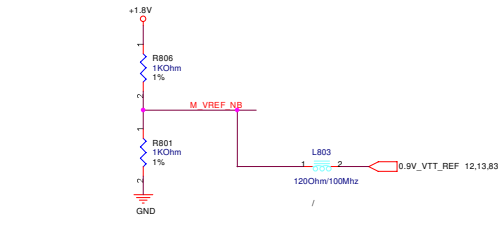
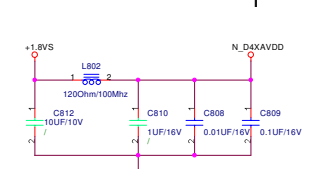
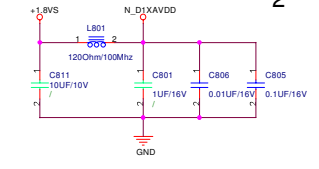
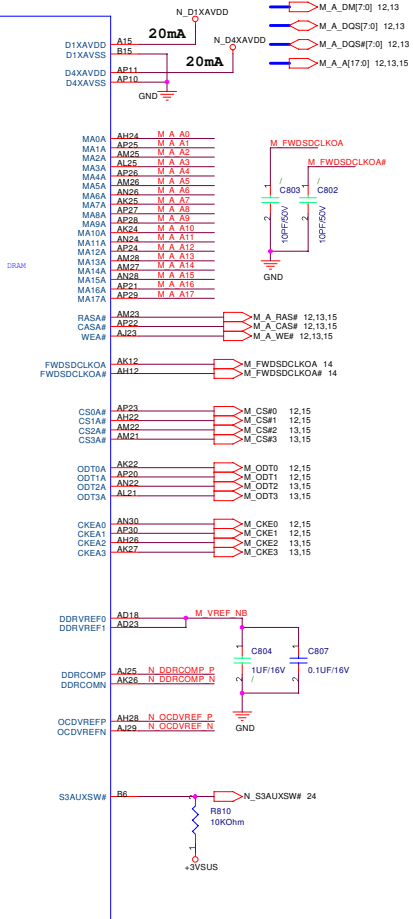
DC FAN Control



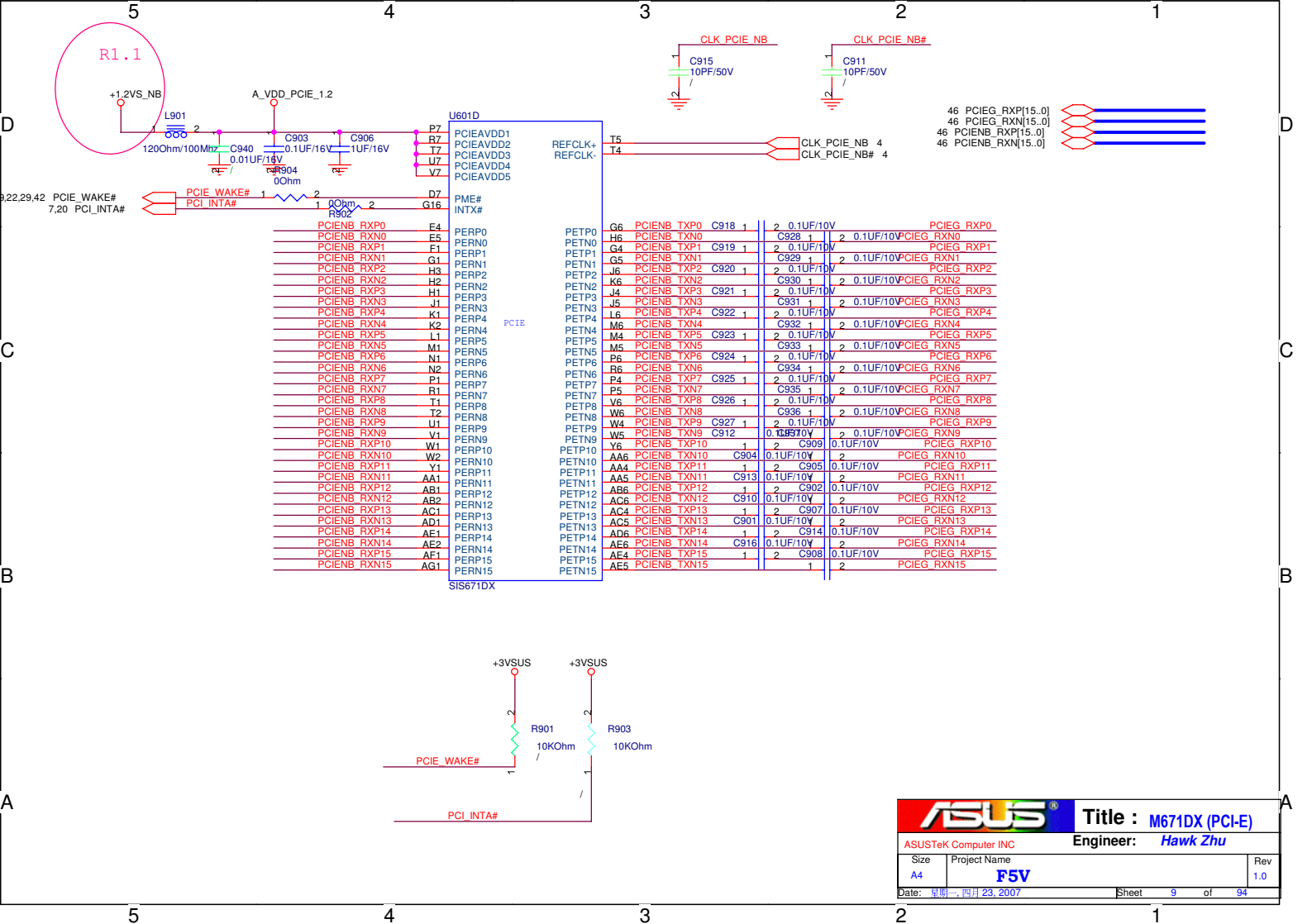
ASUS		Title : Thermal Sensor	
ASUSTek Computer INC		Engineer: Hawk Zhu	
Size A4	Project Name F5V	Rev 1.0	
Date: 2007.04.23		Sheet 5 of 94	



M_A_DQ0	AD31	MD0B
M_A_DQ1	AD30	MD0A
M_A_DQ2	AG34	MD2A
M_A_DQ3	AE36	MD1A
M_A_DQ4	AE32	MD5A
M_A_DQ5	AE34	MD4A
M_A_DQ6	AE34	MD5A
M_A_DQ7	AE30	MD6A
M_A_DQ8	AE30	MD6A
M_A_DQ9	AD28	MD7A
M_A_DQ8D0	AE32	DM0A
M_A_DQ8D1	AE32	DM0A
M_A_DQ8D0	AE31	DQ80A#
M_A_DQ8D1	AE31	DQ80A#
M_A_DQ8	AE29	MD8A
M_A_DQ9	AH34	MD9A
M_A_DQ10	AH31	MD10A
M_A_DQ11	AG30	MD11A
M_A_DQ12	AE30	MD12A
M_A_DQ13	AG32	MD13A
M_A_DQ14	AJ32	MD14A
M_A_DQ15	AJ31	MD15A
M_A_DQ1	AH34	DM1A
M_A_DQ8D1	AH32	DM1A
M_A_DQ8D0	AH32	DM1A
M_A_DQ8D1	AH32	DQ81A#
M_A_DQ8D0	AH32	DQ81A#
M_A_DQ16	AK34	MD16A
M_A_DQ17	AH30	MD17A
M_A_DQ18	AL32	MD18A
M_A_DQ19	AM31	MD19A
M_A_DQ20	AK32	MD20A
M_A_DQ21	AG29	MD21A
M_A_DQ22	AK34	MD22A
M_A_DQ23	AL31	MD23A
M_A_DQ24	AJ32	MD24A
M_A_DQ25	AK33	MD25A
M_A_DQ26	AL34	MD26A
M_A_DQ27	AK34	MD27A
M_A_DQ28	AK30	MD28A
M_A_DQ29	AK29	MD29A
M_A_DQ30	AJ27	MD30A
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M_A_DQ32	AK28	MD31A
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M_A_DQ37	AN30	MD34A
M_A_DQ38	AJ21	MD37A
M_A_DQ39	AP18	MD38A
M_A_DQ40	AH20	MD39A
M_A_DQ41	AK21	DM4A
M_A_DQ42	AK19	DQ4A#
M_A_DQ43	AL19	DQ4A#
M_A_DQ40	AK18	MD40A
M_A_DQ41	AJ17	MD41A
M_A_DQ42	AJ17	MD42A
M_A_DQ43	AP16	MD43A
M_A_DQ44	AH18	MD44A
M_A_DQ45	AP18	MD45A
M_A_DQ46	AN18	MD46A
M_A_DQ47	AP17	MD47A
M_A_DQ48	AM18	DM5A
M_A_DQ49	AL17	DQ5A#
M_A_DQ50	AM17	DQ5A#
M_A_DQ48	AN16	MD48A
M_A_DQ49	AK16	MD49A
M_A_DQ50	AN14	MD50A
M_A_DQ51	AJ15	MD51A
M_A_DQ52	AP15	MD52A
M_A_DQ53	AM16	MD52A
M_A_DQ54	AK15	MD53A
M_A_DQ55	AP14	MD54A
M_A_DQ56	AH16	MD55A
M_A_DQ57	AL15	DM6A
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M_A_DQ59	AM15	DQ6A#
M_A_DQ56	AL13	MD56A
M_A_DQ57	AM13	MD57A
M_A_DQ58	AM12	MD58A
M_A_DQ59	AJ13	MD59A
M_A_DQ60	AM14	MD59A
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M_A_DQ63	AN12	MD62A
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M_A_DQ66	AP12	DQ7A#
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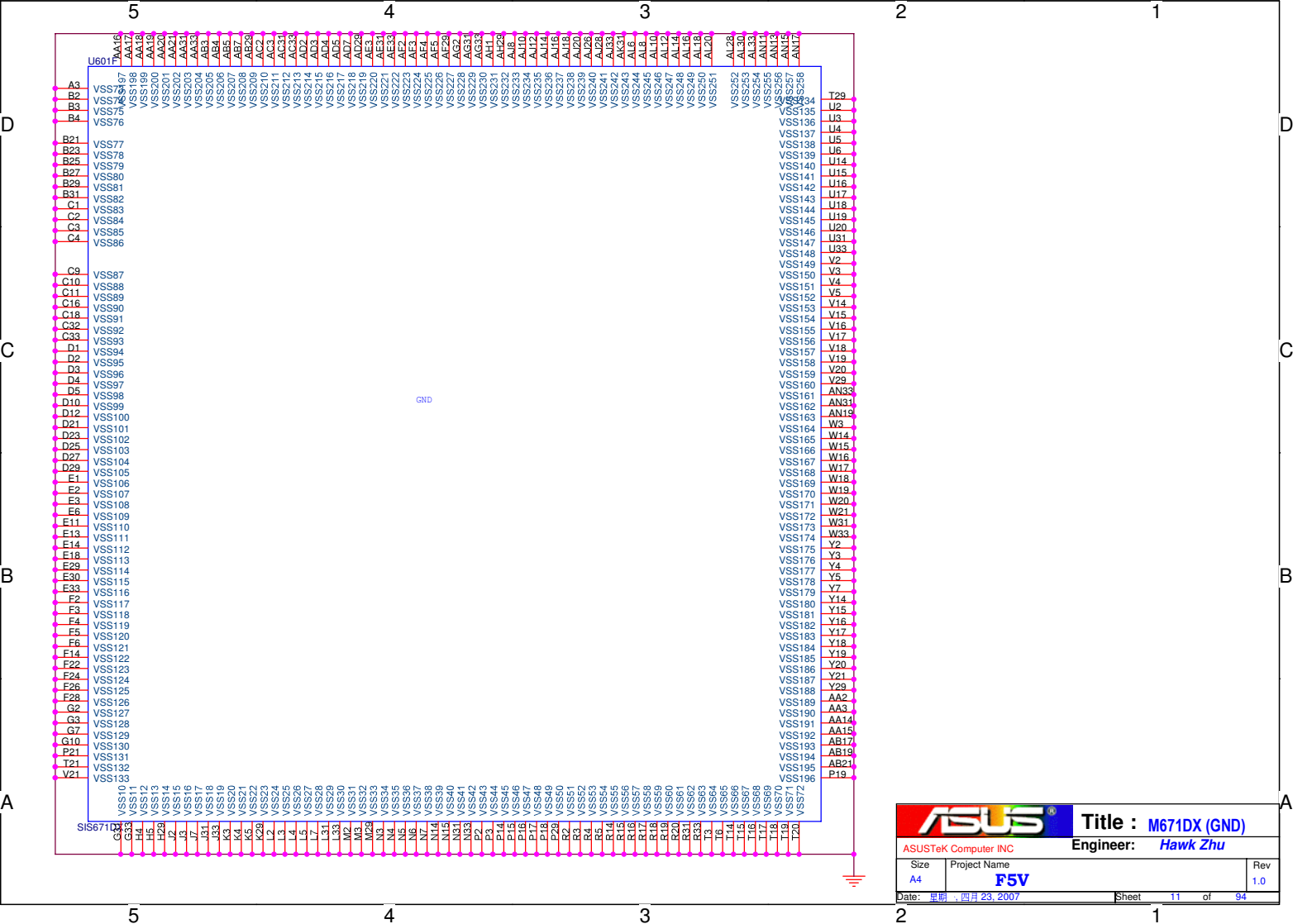
Layout Note:
Route as short as possible



ASUS Title : M671DX (PCI-E)
 ASUSTek Computer INC Engineer: Hawk Zhu

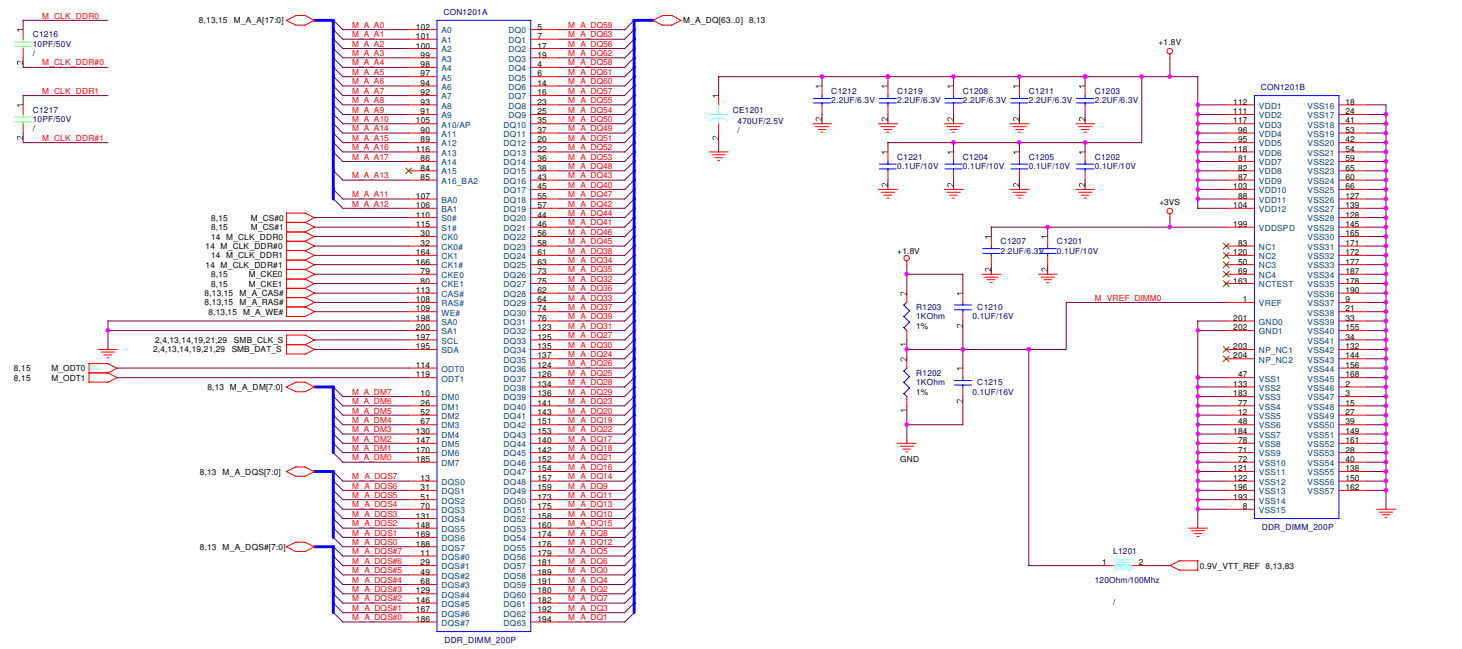
Size	Project Name	Rev
A4	F5V	1.0

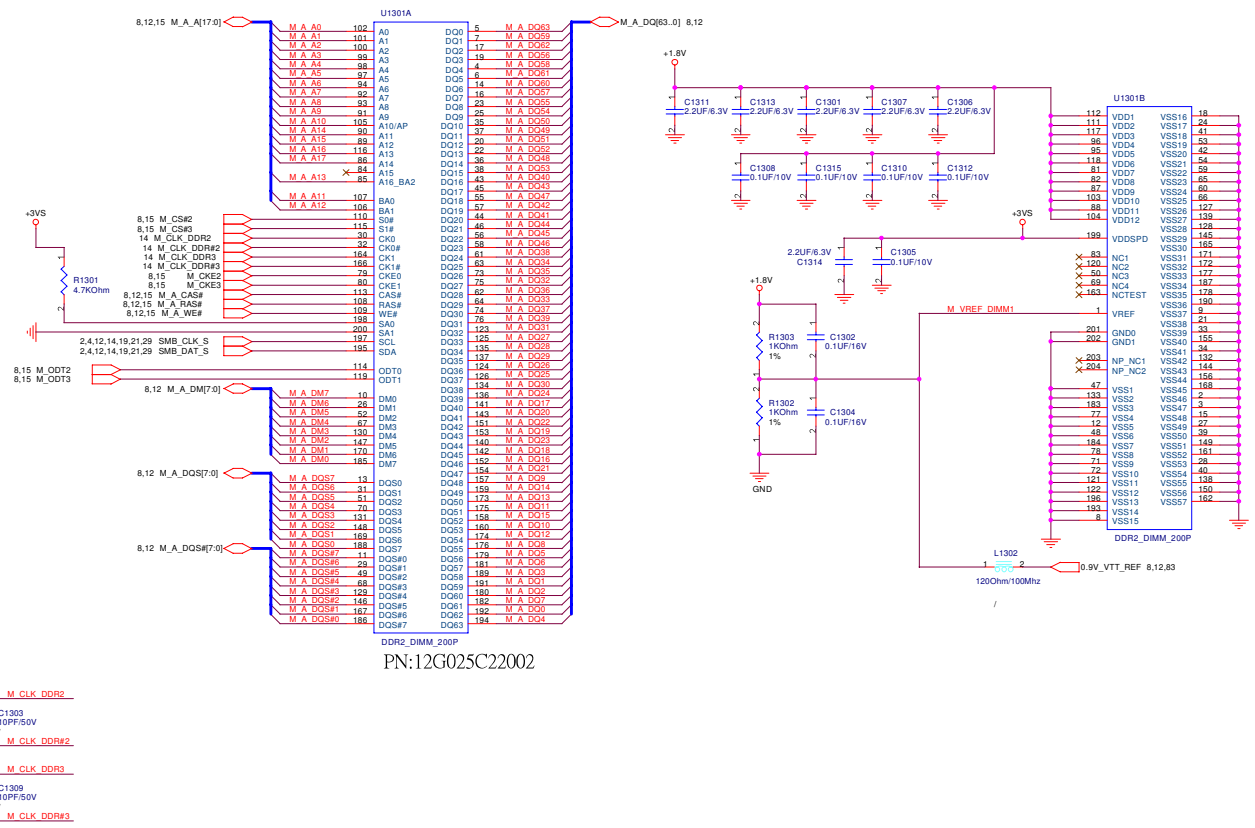
Date: 星期三, 四月 23, 2007 Sheet 9 of 94



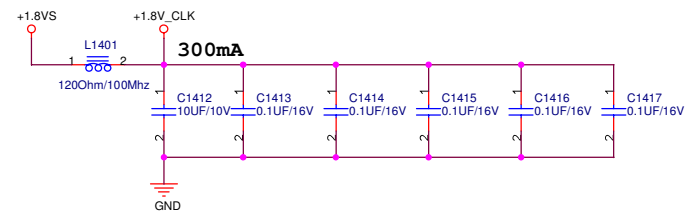
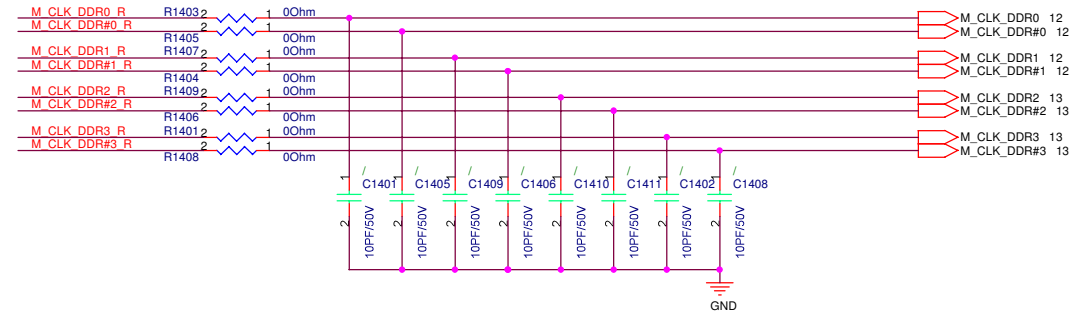
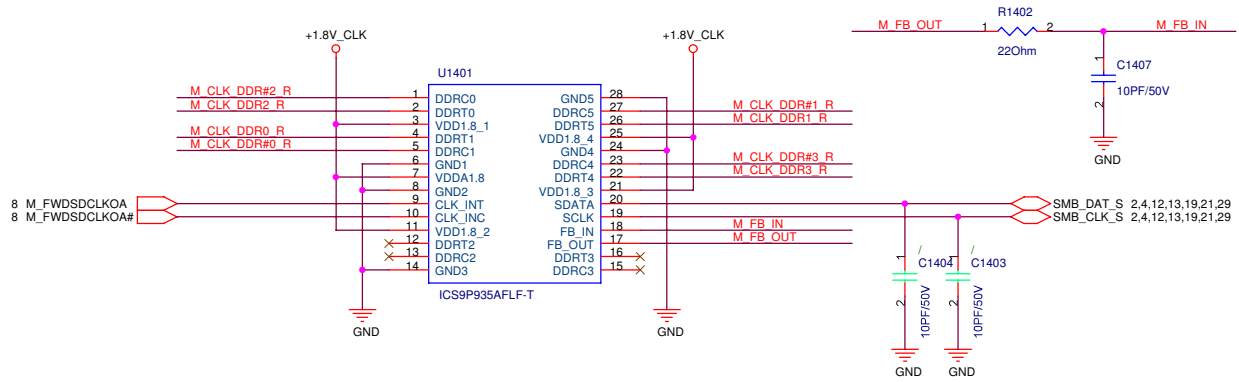
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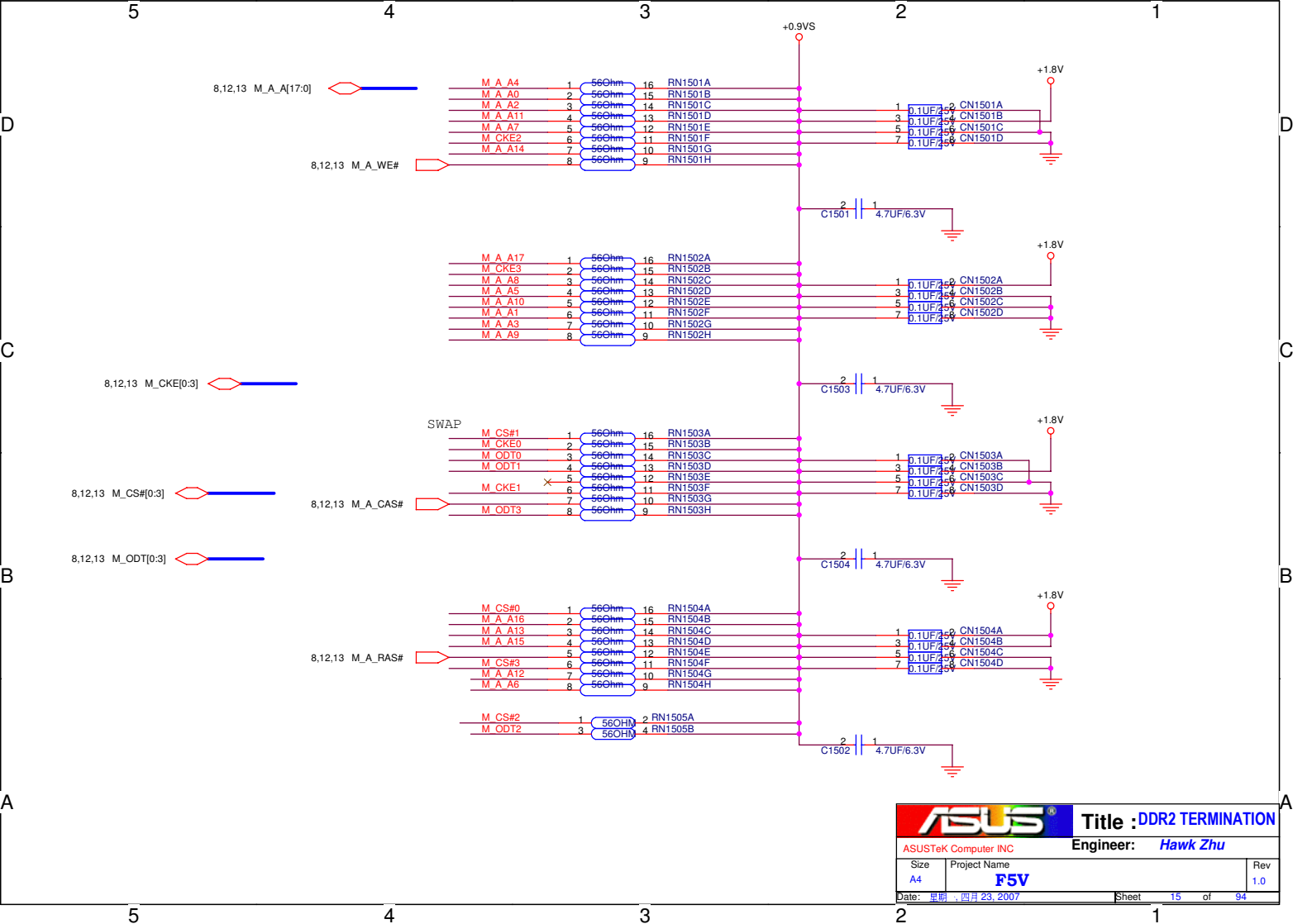


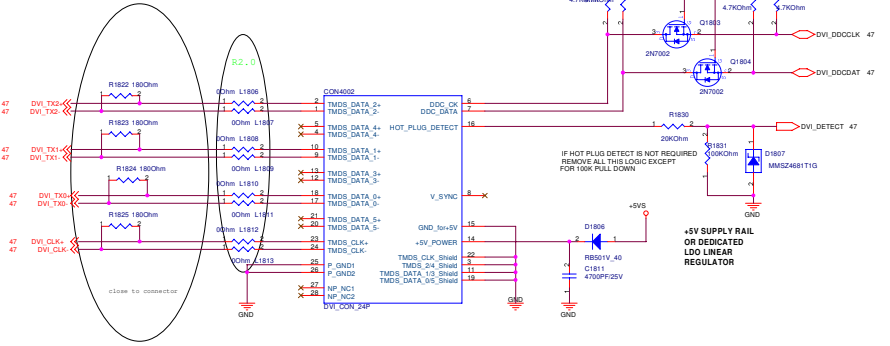
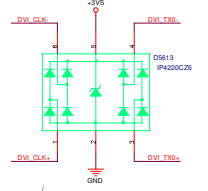
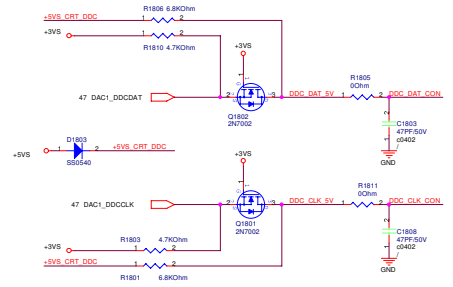
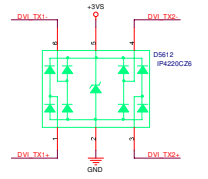
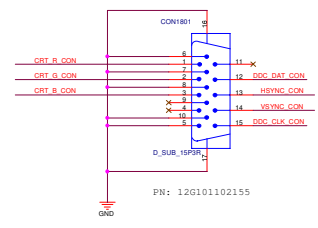
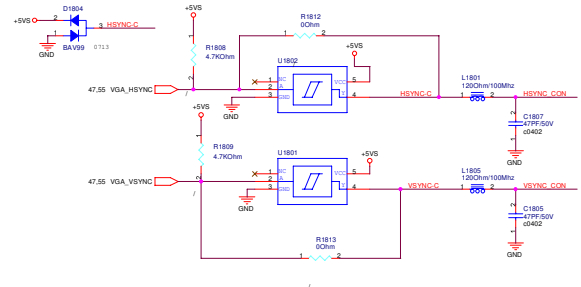
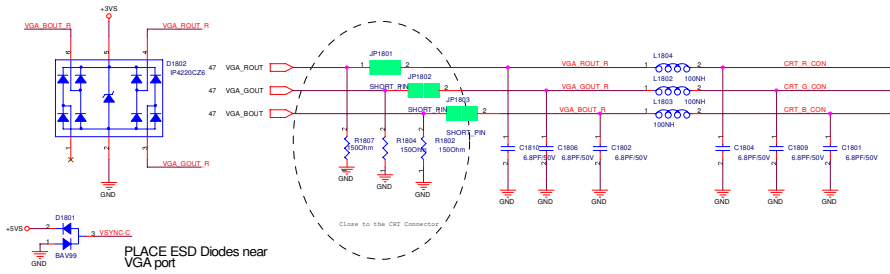


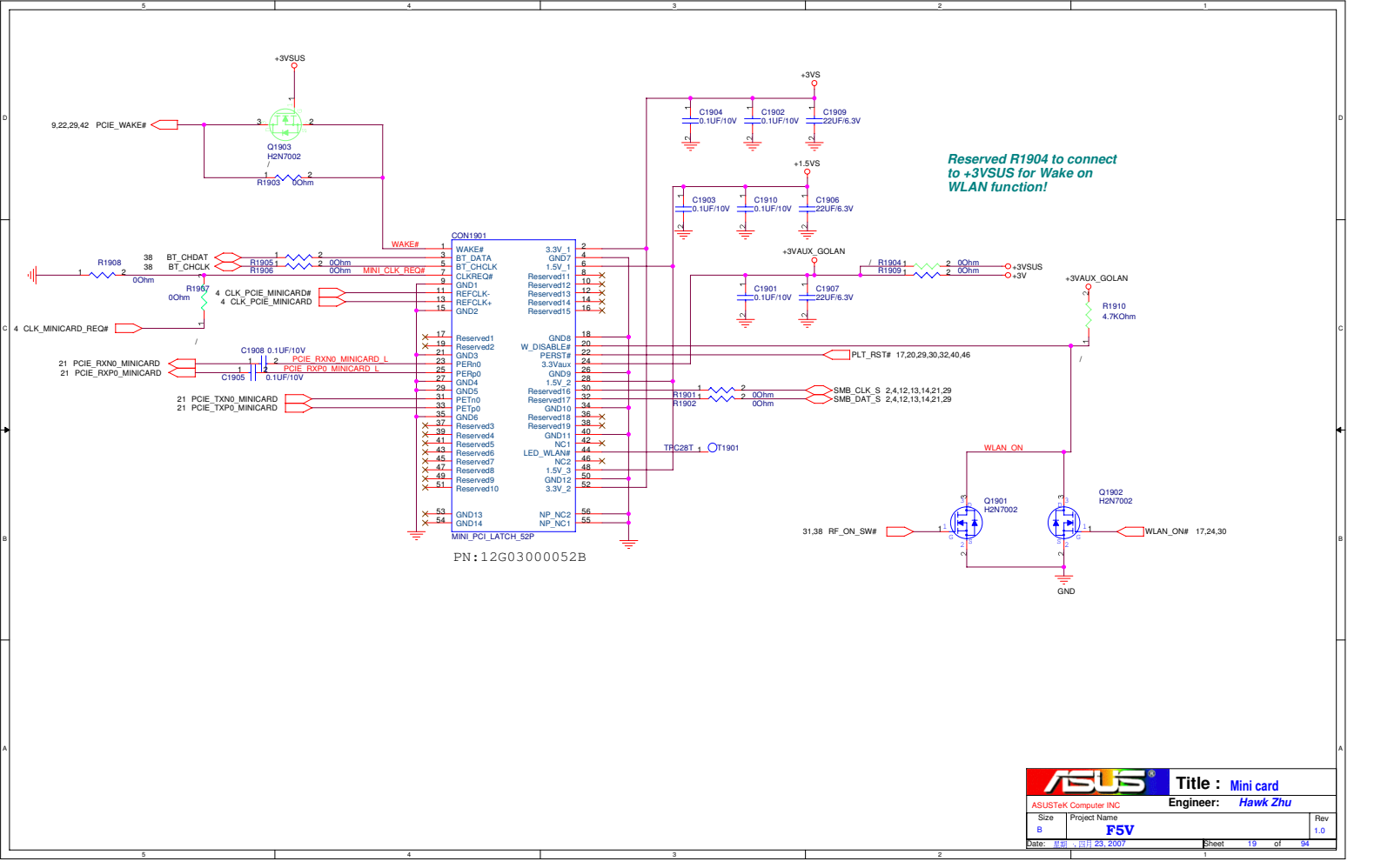
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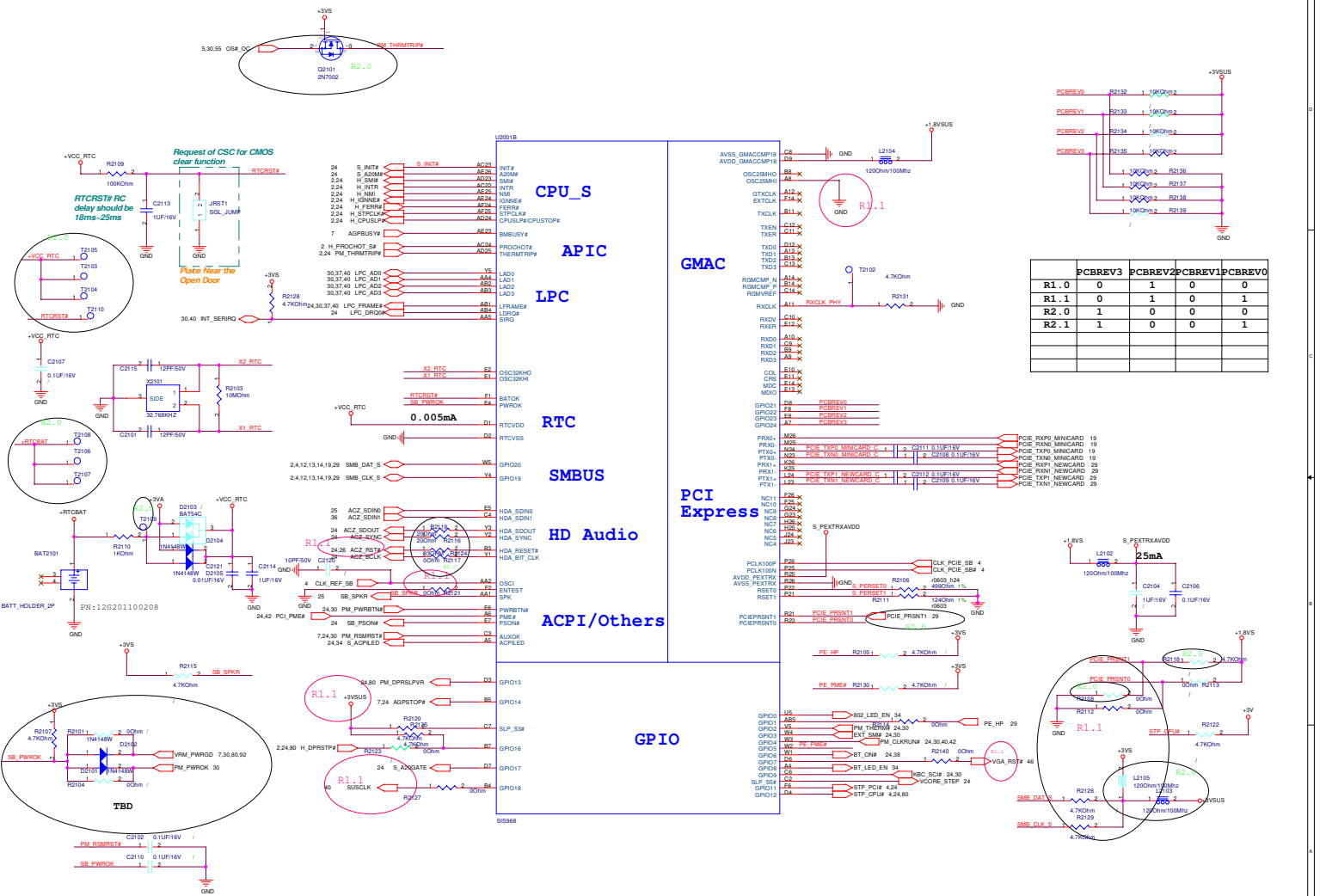


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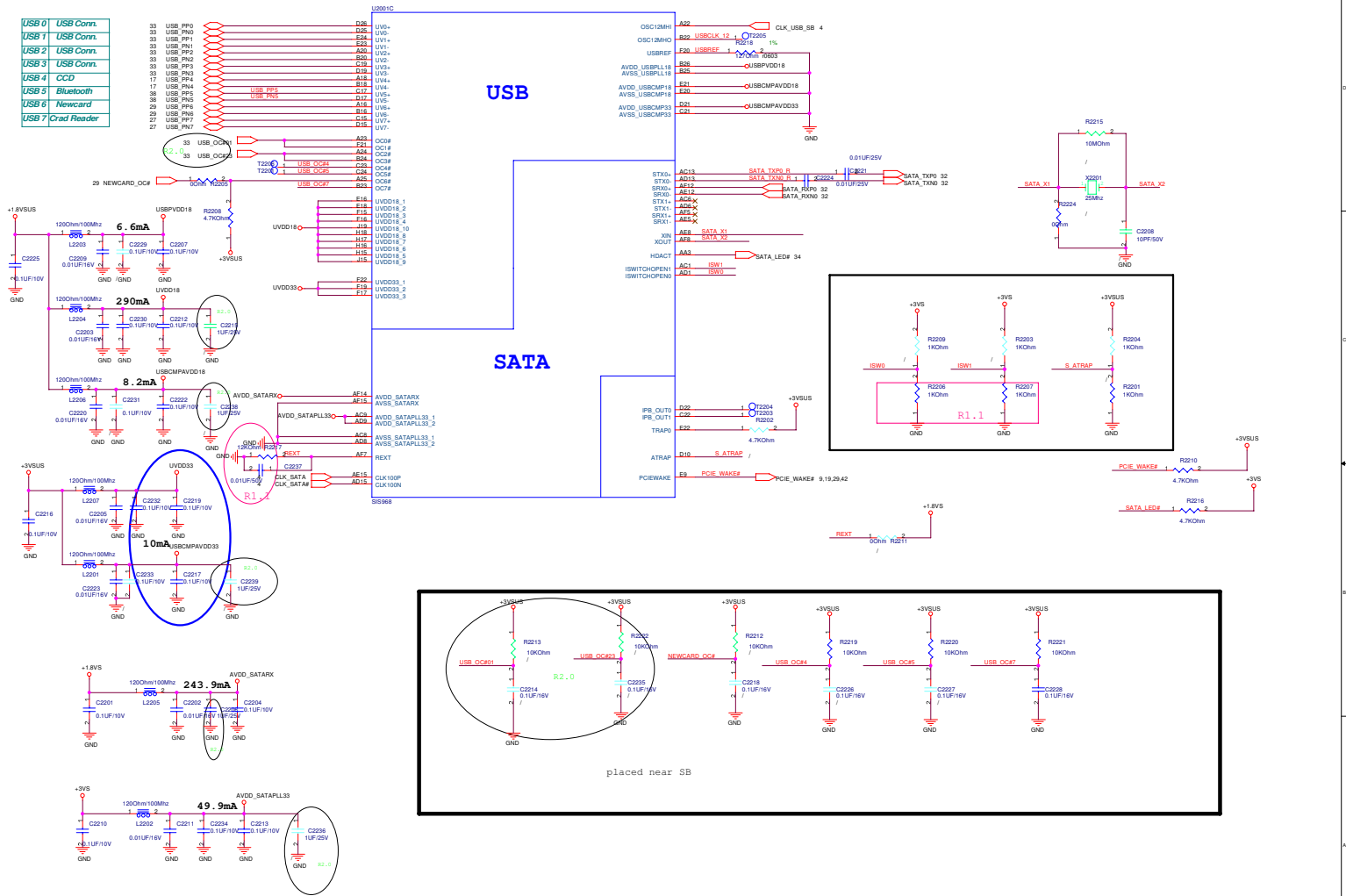


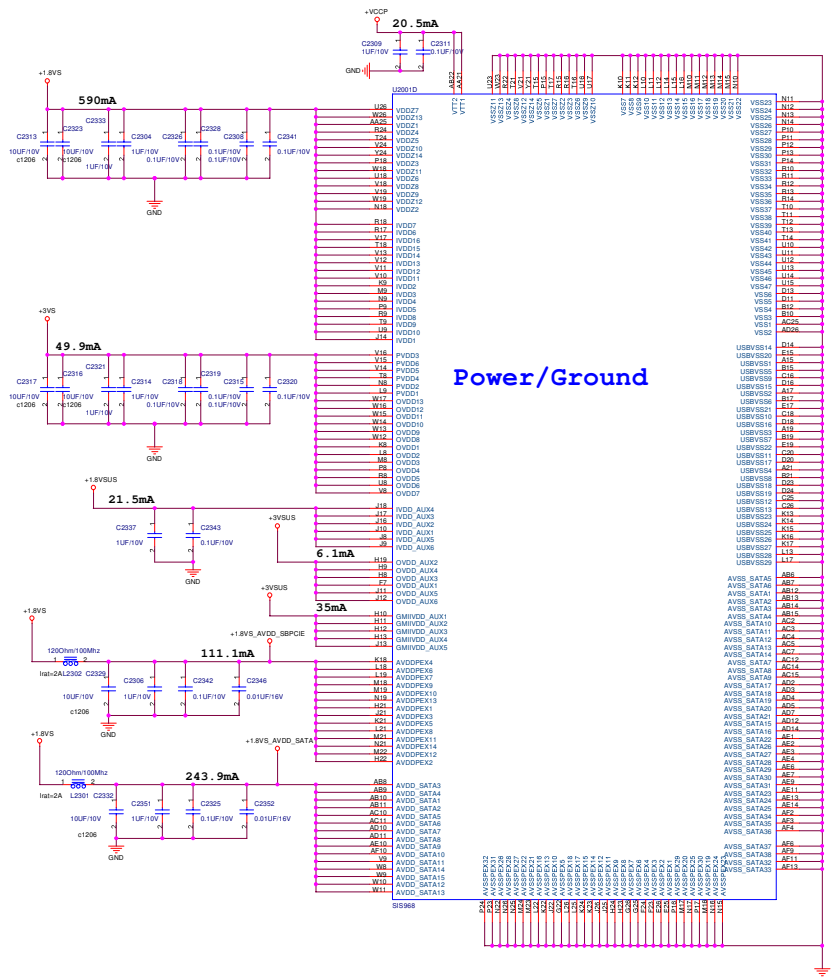




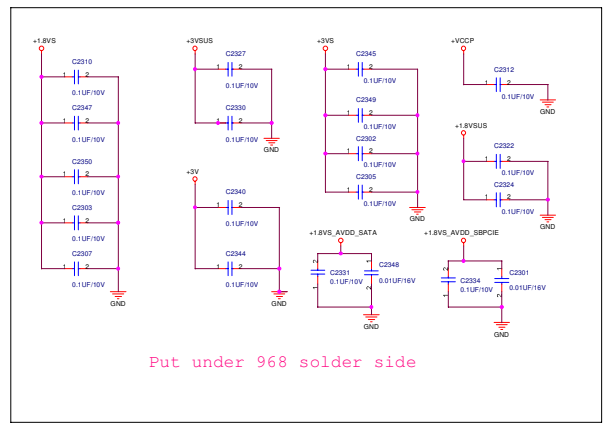
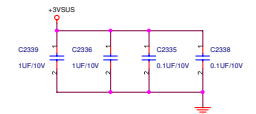


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- USB 1 USB Conn.
- USB 2 USB Conn.
- USB 3 USB Conn.
- USB 4 CCD
- USB 5 Bluetooth
- USB 6 Newcard
- USB 7 Crad Reader



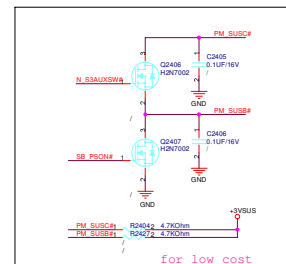
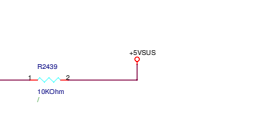
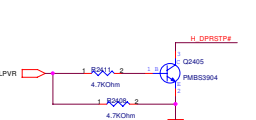
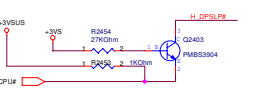
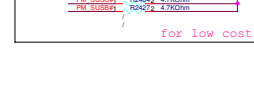
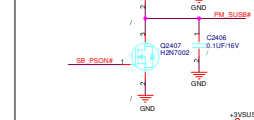
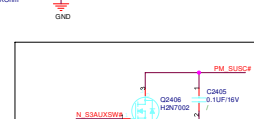
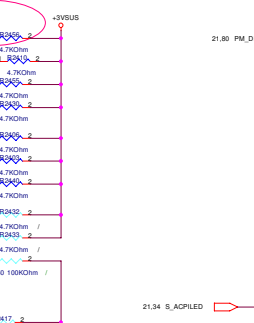
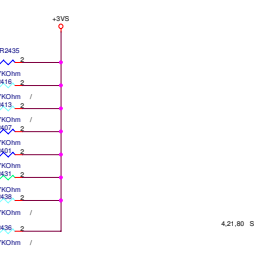
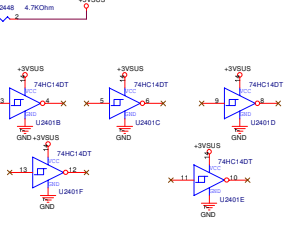
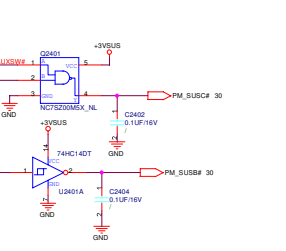
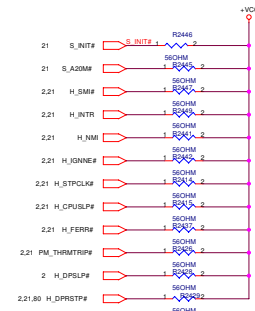
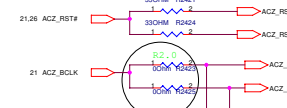
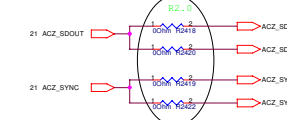
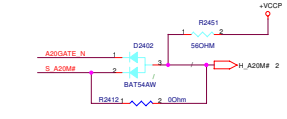
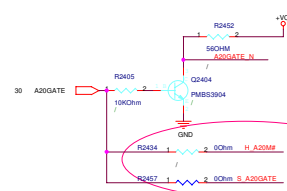
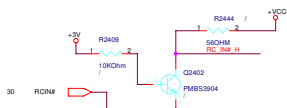
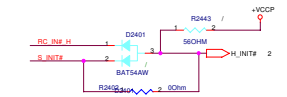


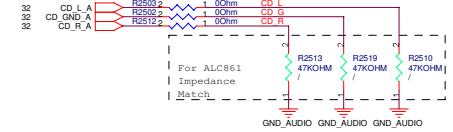
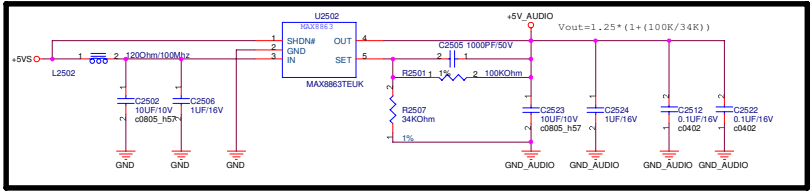
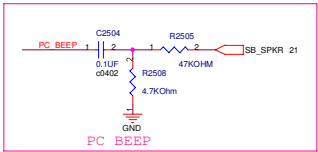
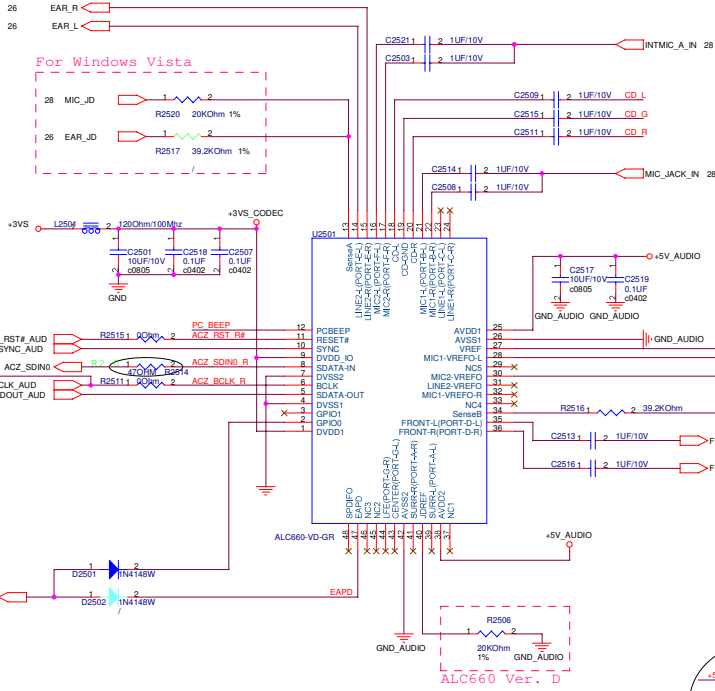
Power/Ground

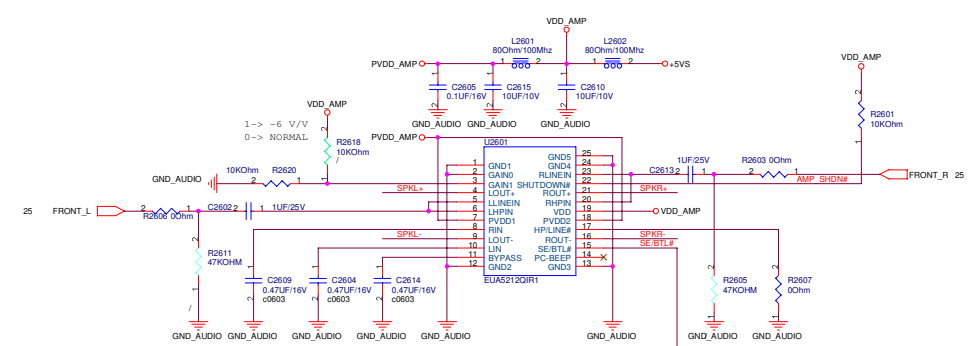


Put under 968 solder side

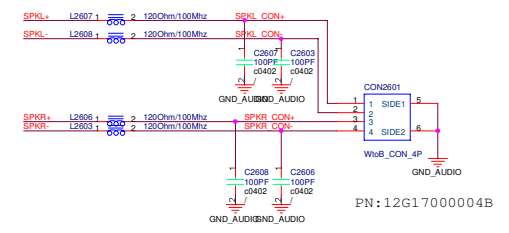
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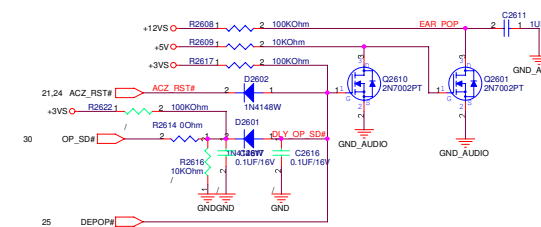
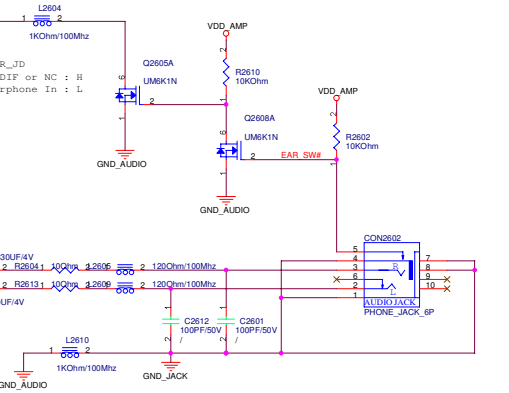
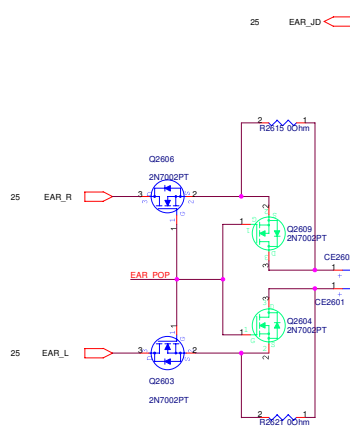
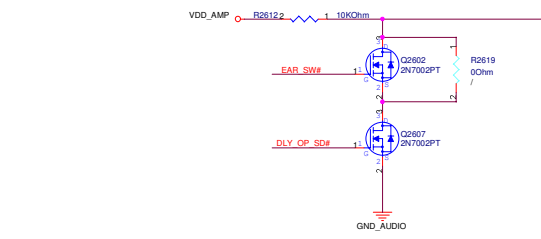


change P/N to 06G045064010

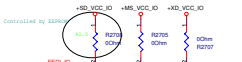
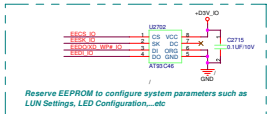
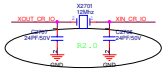
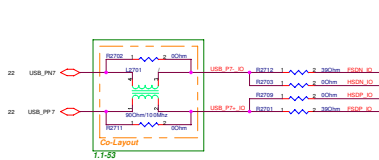


PN:12G1700004B

SPEAKER CONNET



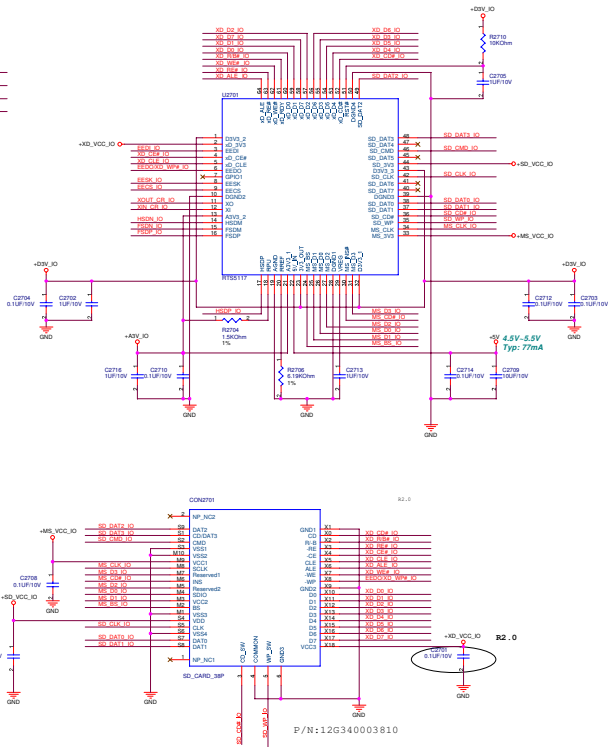
ASUS		Title : AMPLIFIER 2 CHANNEL	
-<OrgName>		Engineer: Kaxidy Jiang	
Size	Project Name	Rev	
Custom	FSV	1.0	
DATE: 2007-11-21 20:07		Sheet	28 of 34

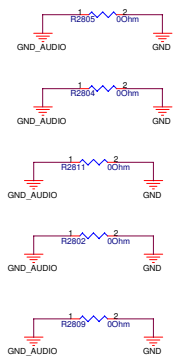


	IO_R2706	IO_R2705
SD/MMC only	No Stuff	No Stuff
xD-SD/MMC/MS/MS-Pro Combo	No Stuff	No Stuff
Support CPU C3 State	No Stuff	4.7K
SD/MMC/MS/MS-Pro Combo	4.7K	No Stuff
Don't Support CPU C3 State	No Stuff	4.7K
SD/MMC/MS/MS-Pro Combo	4.7K	No Stuff
Don't Support CPU C3 State	No Stuff	4.7K

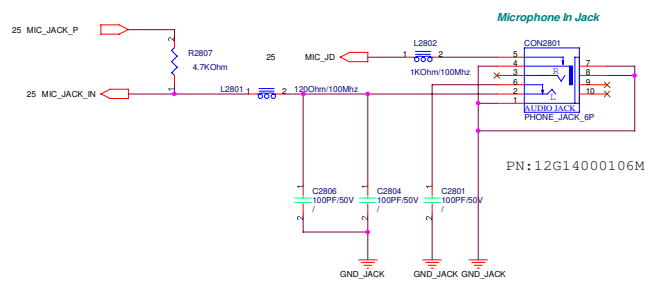
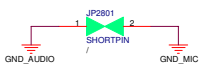
IO_R41 should be present if system doesn't use EEPROM to configure LED.

Through these pull-up resistors, EEPROM can be saved if no other requirement about other parameters.

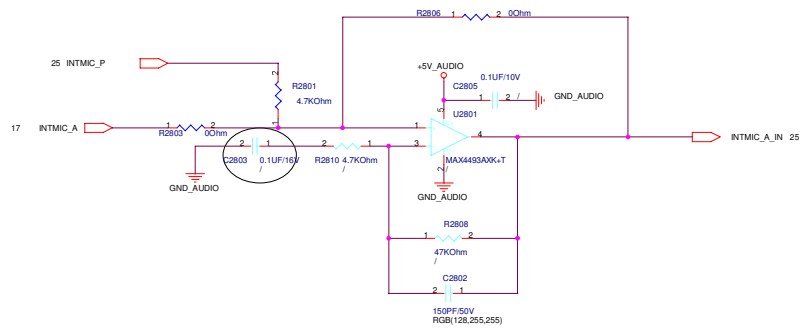




INTMIC_A:GND_AUDIO
: W/P/X = 12/5/15mils

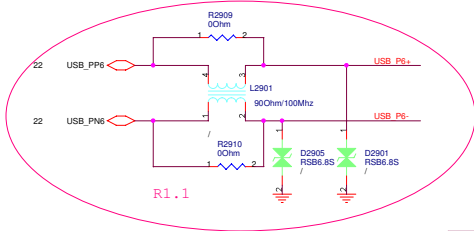


Pre-AMP For Test Function

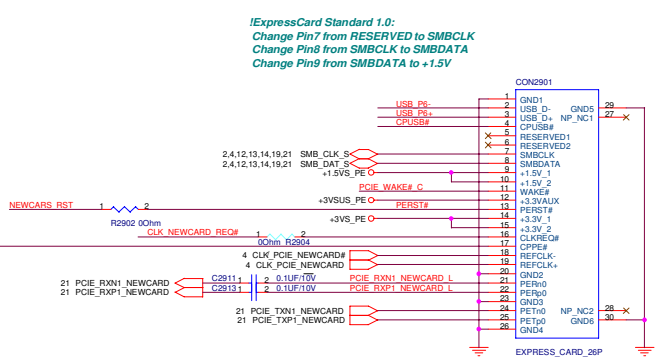
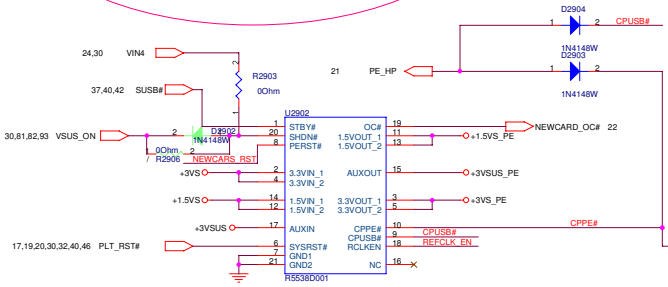


		Title : MIC.LINE-IN JACK	
-OrgName-		Engineer: <i>Kaxidy Jiang</i>	
Size	Project Name		Rev
Custom	FSV		1.0
Date: 2007-11-24	Sheet	28	of 34

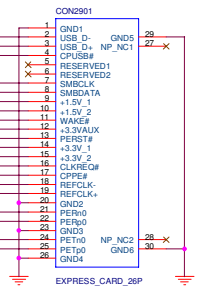
FOR SWAP



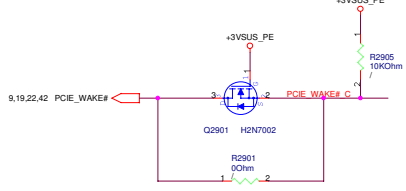
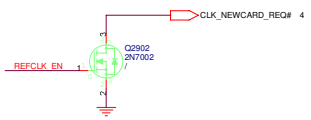
R1.1



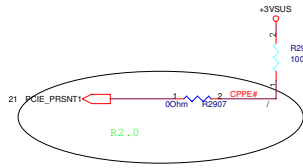
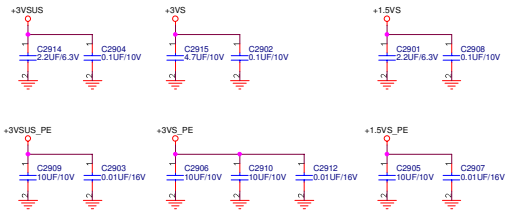
!ExpressCard Standard 1.0:
 Change Pin7 from RESERVED to SMBCLK
 Change Pin8 from SMBCLK to SMBDATA
 Change Pin9 from SMBDATA to +1.5V



PN:12G161300261 06/07



PN:12G21C102604



R2.0

ASUS		Title : NEWCARD
ASUSTek COMPUTER INC		Engineer: <i>Kaxidy Jiang</i>
Size	Project Name	Rev
Custom	F5V	1.0
Date: 10/11/2007	Sheet 29	of 34

For Battery

Single Battery

BAT1_CNT1#, BAT1_CNT2#,
BAT2_CNT1#, BAT2_CNT2#
don't connect to Battery
Connector.

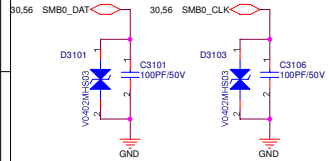
Dual Battery

BAT1_CNT1#, BAT1_CNT2#,
BAT2_CNT1#, BAT2_CNT2#
must connect to Battery
Connector.

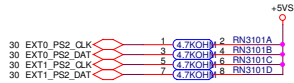
Note:

When we plug in or plug out the
battery, it may cause a spike to
damage the EC and gas gauge. It
needed to add these varistors to
protect those pins.

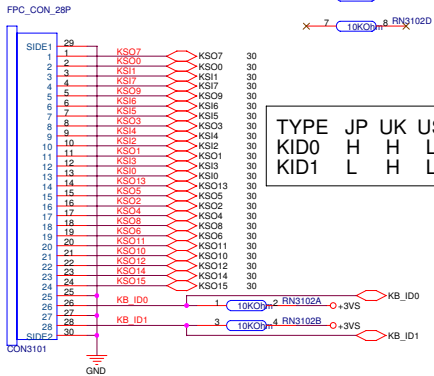
close to connector



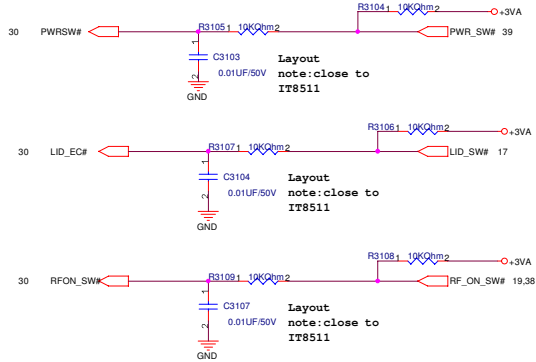
For External PS/2 I/F



For Keyboard



For Switch



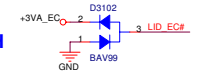
Note:

This LID_EC# is a signal
from inverter board, it is
easy to cause high voltage
damage when plugging
inverter board connector to
M/B with AC present. It
needed to add bidirectional
diode to protect this pin.

PWR SWITCH

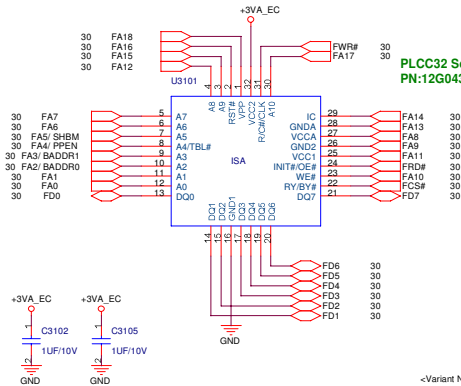
LID SWITCH

RF SWITCH



Layout
note: close to
connector

For 4M bits ISA ROM



Note:

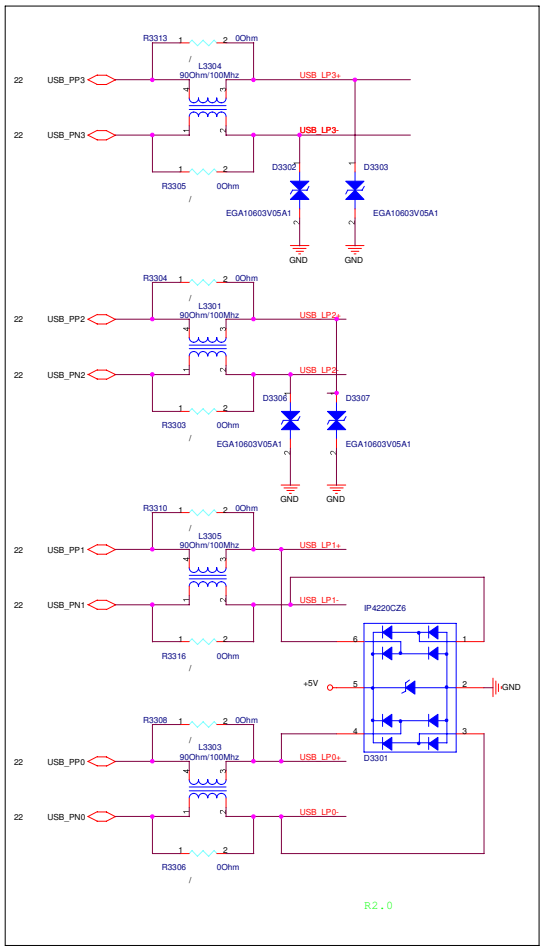
If you use 8M bits ROM, you need
to connect FA19 to EC side.

PLCC32 Socket
PN:12G04300032F

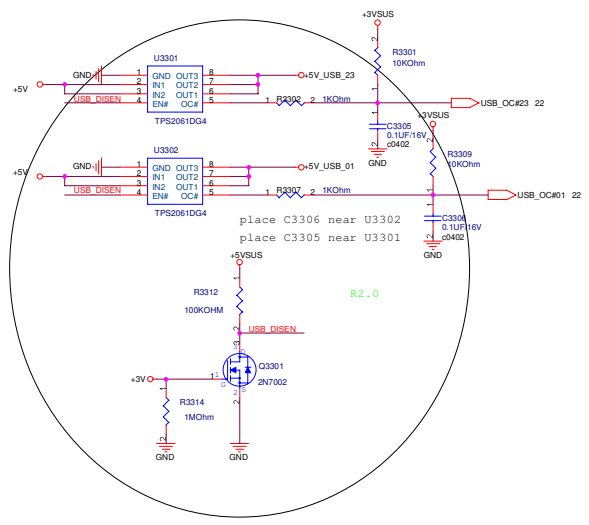
SST-PLCC32 4Mbits Flash ROM
PN:05G001027221

<Variant Name>

ASUS		Title :KB&ISA ROM	
ASUSTek COMPUTER INC. NB1		Engineer: <i>Kaxidy Jiang</i>	
Size	Project Name		Rev
Custom	F5V		1.0
Date: 08/11/2007	Esheet	31	of 94

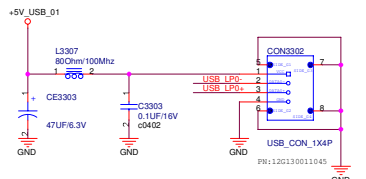
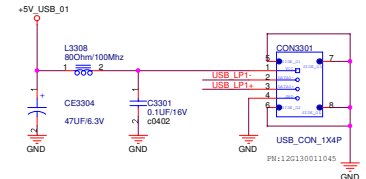
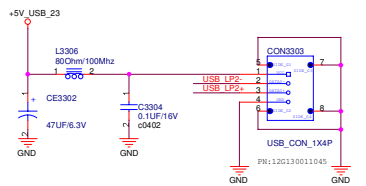
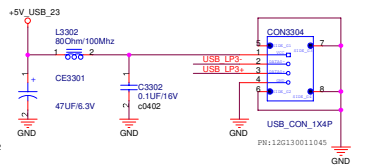


R2.0



place C3306 near U3302
place C3305 near U3301

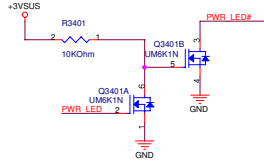
R2.0



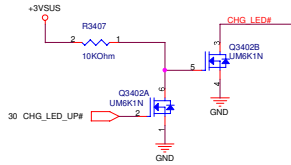
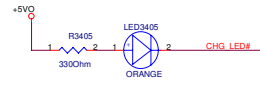
<Variant Name>

ASUS		Title : USB CONN	
ASUSTek COMPUTER INC. NBI		Engineer: <i>Kaxidy Jiang</i>	
Size	Project Name		Rev
Custom	F5V		1.0
Date: 9/11/07 23:2007		Sheet	33 of 94

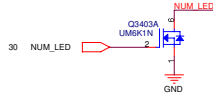
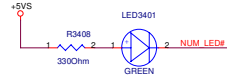
For POWER LED



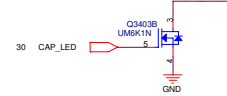
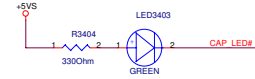
BATTERY LED



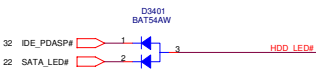
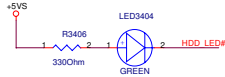
Num Lock



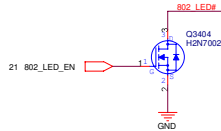
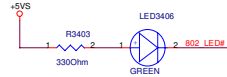
Cap Lock



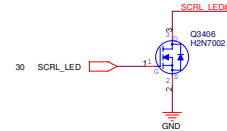
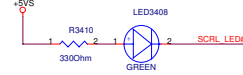
SATA/IDE LED



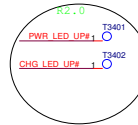
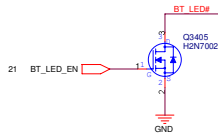
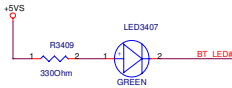
WireLess LED



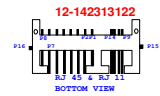
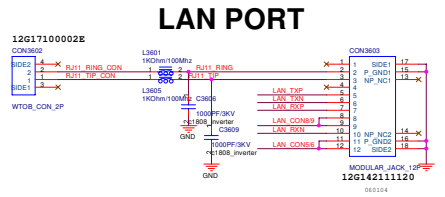
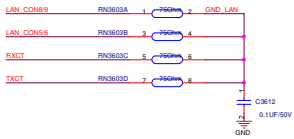
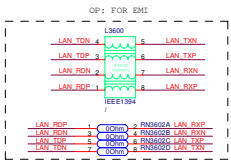
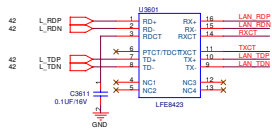
Scroll Lock



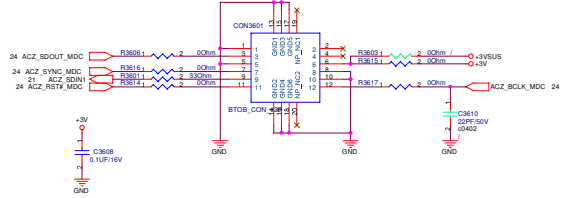
BT LED

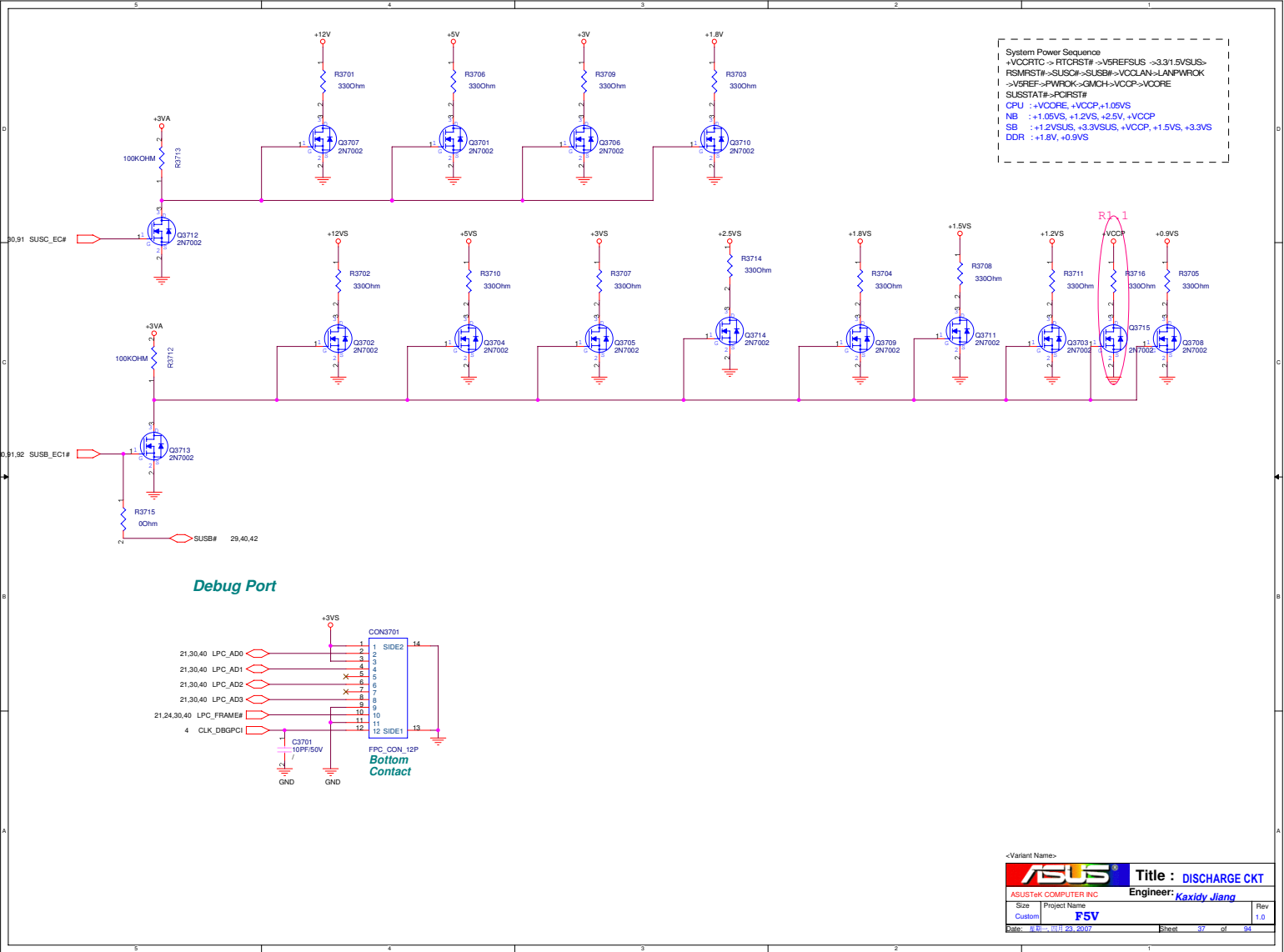


ASUSTek COMPUTER INC		Title : LED	
Size	Project Name	Engineer: <i>Kaxidy Jiang</i>	Rev
Custom	FSV		1.0
Date: 11/01/2007	Sheet	34	of 34



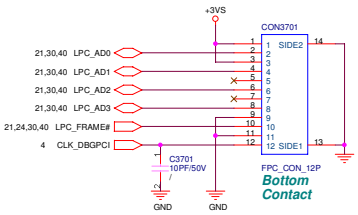
MDC





System Power Sequence
 +VCCRTC -> RTCRST# -> VSRFSUS -> +3.15VSUS->
 RSMRST# -> SUSCS# -> SUSB# -> VCCLAN -> LANPWCK ->
 +VSRF -> PWCK -> GMCH -> VCCP -> VCCRE
 | SUSSTAT# -> PCIRST#
 | CPU -> VCCPRE -> VCCP -> +1.0VS
 NB : +1.0VS, +1.2VS, +2.5V, +VCCP
 SB : +1.2VSUS, +3.3VSUS, +VCCP, +1.5VS, +3.3VS
 DDR : +1.8V, +0.9VS

Debug Port

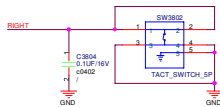
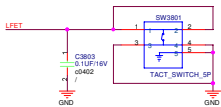
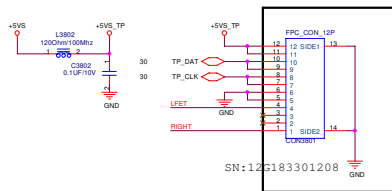


<Variant Name>

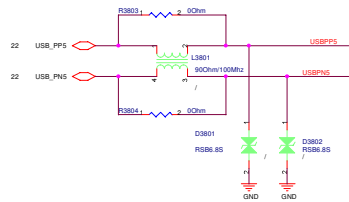
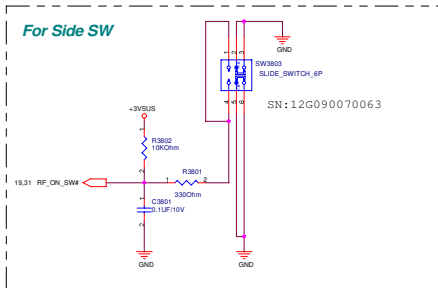
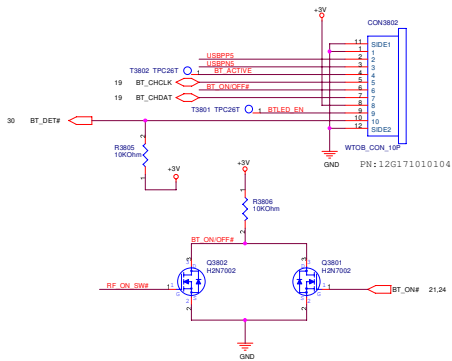
ASUS		Title : DISCHARGE CKT
ASUSTek COMPUTER INC		Engineer: <i>Kaxidy Jiang</i>
Size	Project Name	Rev
Custom	F5V	1.0
Date: 11/01/2007	Sheet 37 of 38	

Touch-Pad

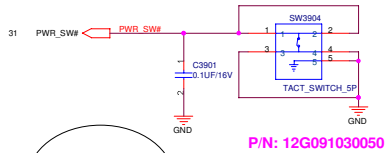
R1.1



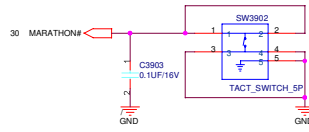
For Bluetooth



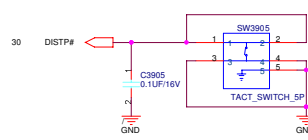
Power SW.



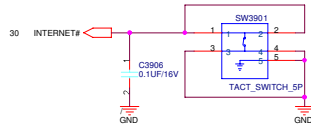
Marathon SW.



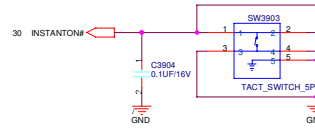
Disable Touch Pad SW.



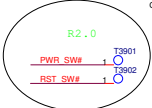
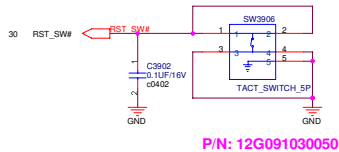
Internet SW.



IstantON SW.



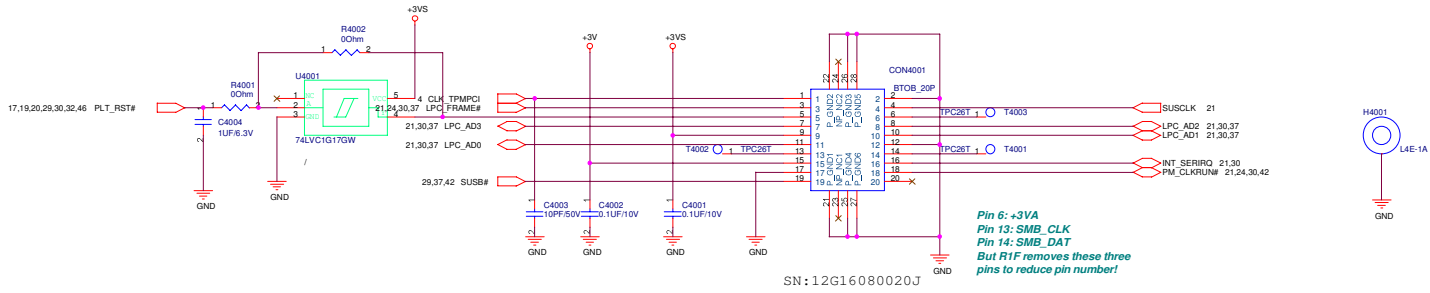
RESET SW.



<Variant Name>

ASUS		Title : SWITCH	
ASUSTek COMPUTER INC		Engineer: <i>Kaxidy jiang</i>	
Size	Project Name	Rev	
Custom	FSV	1.0	
Date: 11/01/2007	Sheet 39 of 34		

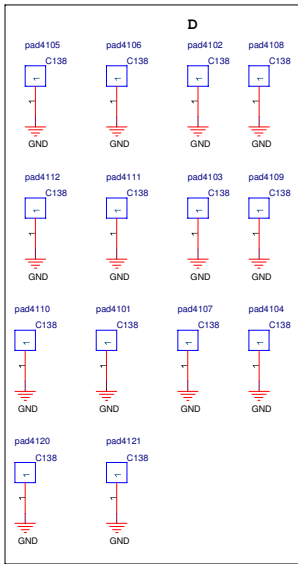
For TPM Module



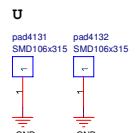
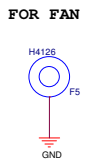
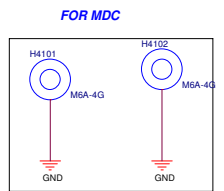
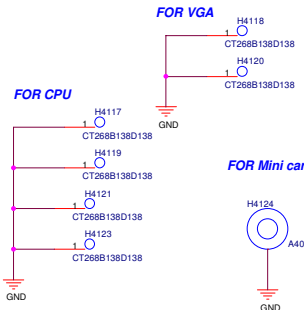
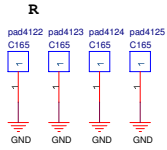
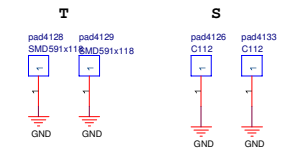
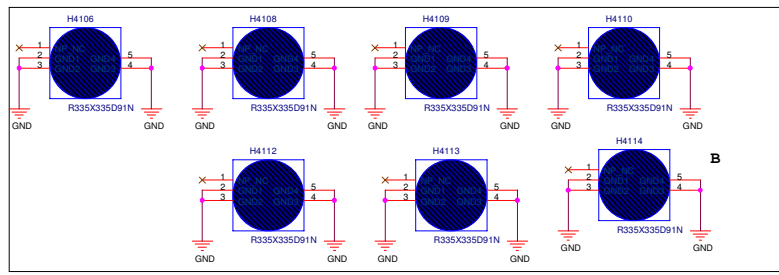
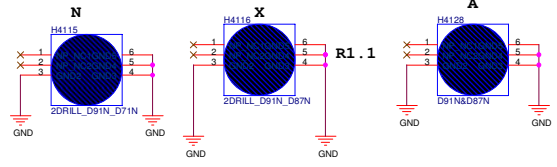
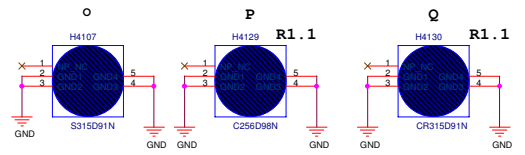
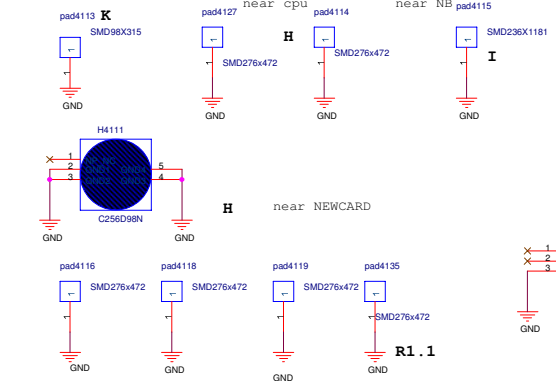
SN:12G16080020J

Pin 6: +3VA
 Pin 13: SMB_CLK
 Pin 14: SMB_DAT
 But R1F removes these three pins to reduce pin number!

ASUS		Title : TPM	
ASUSTek COMPUTER INC. NB1		Engineer: Kaxidy Jiang	
Size	Project Name	Rev	
Custom	FSV	1.0	
Date: 2007.03.23	Sheet: 40	of	44

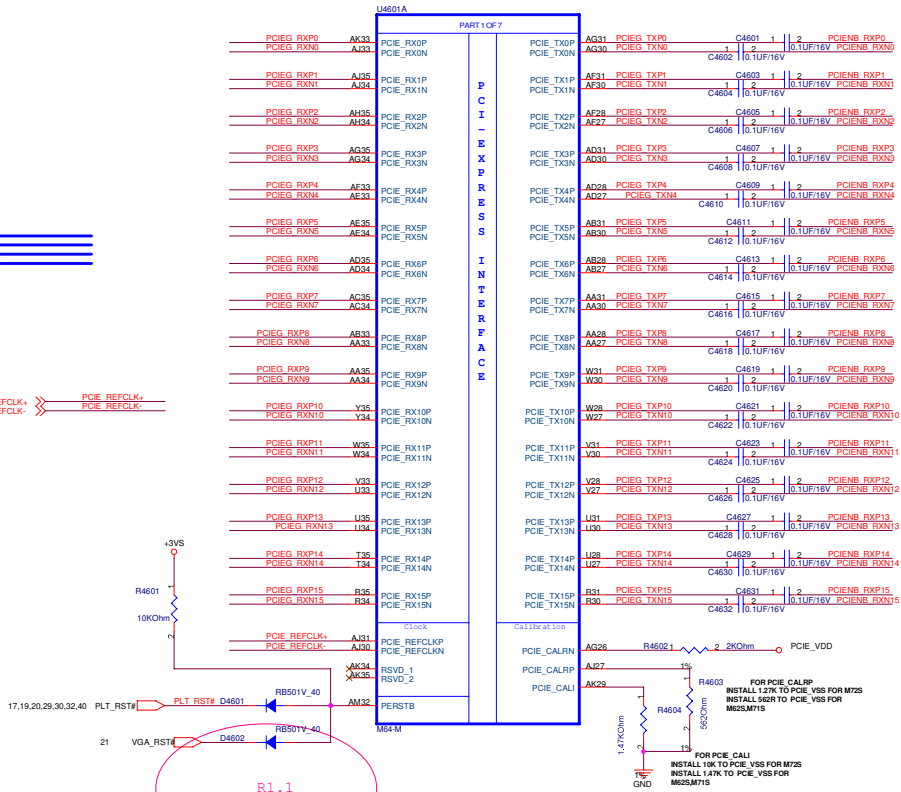


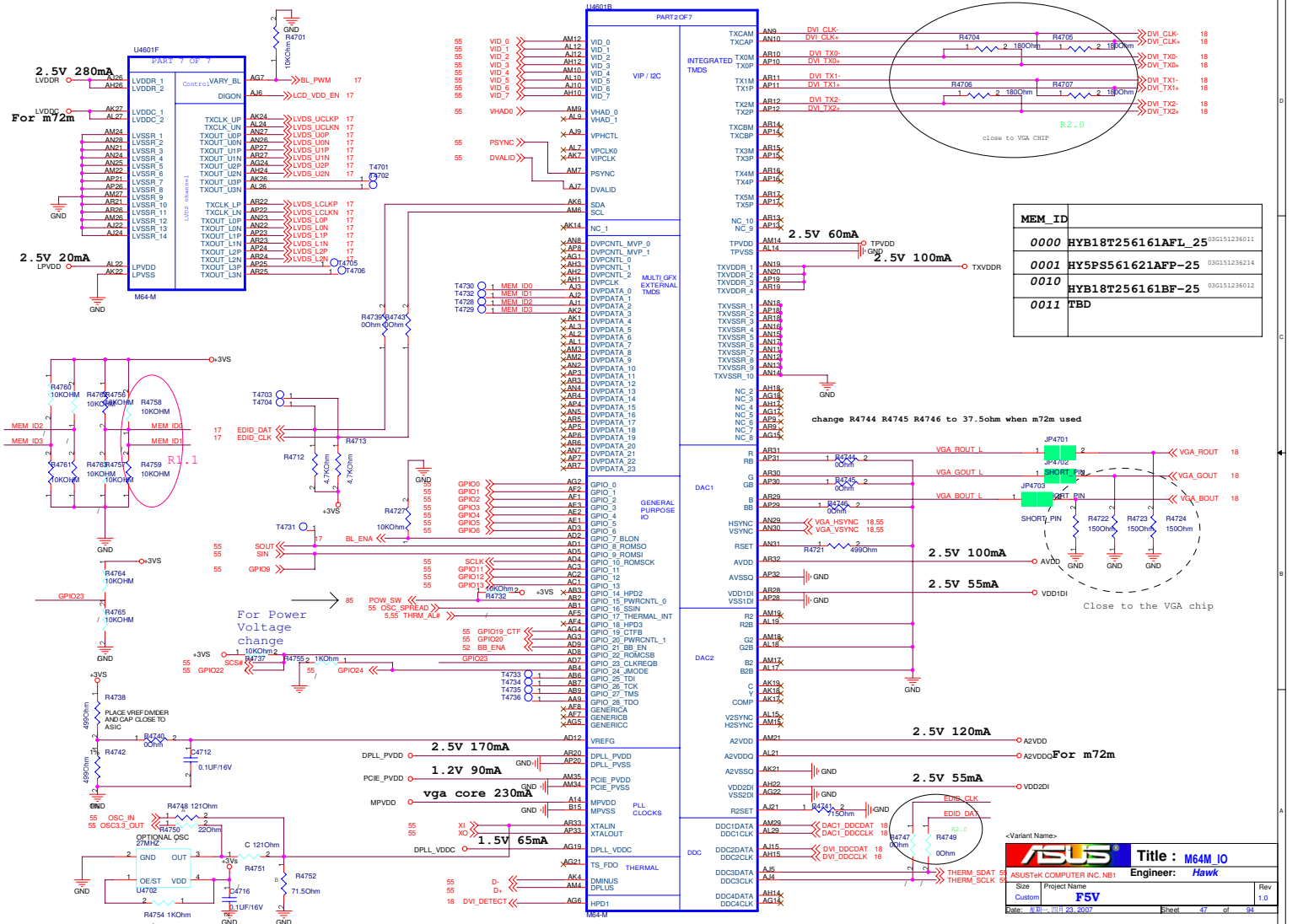
above ODD connector



R2.0 change to P/N:13GN9980M090-1 for high limit

		Title : Screw hole	
		ASUSTeK COMPUTER INC. NBI Engineer: <i>Kaxidy/Hawk</i>	
Size	Project Name		Rev
B	FSV		1.0
Date: #0 - 10/23, 2007		Sheet 41 of 94	





MEM ID	MEM ID
0000	HYB18T256161AFL-25 03G151236011
0001	HY5P5561621AEP-25 03G151236214
0010	HYB18T256161BF-25 03G151236012
0011	TBD

ASUS Title: M64M I/O
 ASUSTeK COMPUTER INC. NBI Engineer: Hawk
 Size: Custom Project Name: FSV
 Date: 11/01/2007 Sheet: 47 of 34

For m72m

2.5V 20mA

3VS

MEM ID2

MEM ID3

GPIOD23

3VS

3VS

3VS

55 VID_0 AM10
 55 VID_1 AM12
 55 VID_2 AM13
 55 VID_3 AM14
 55 VID_4 AM15
 55 VID_5 AM16
 55 VID_6 AM17
 55 VID_7 AM18

55 PSYNC AM9
 55 DVALID AM7
 55 PSYNC AM7
 55 DVALID AM7

T4730 1 MEM ID0
 T4728 1 MEM ID2
 T4726 1 MEM ID3

AG2 GPIO0
 AG3 GPIO1
 AG4 GPIO2
 AG5 GPIO3
 AG6 GPIO4
 AG7 GPIO5
 AG8 GPIO6

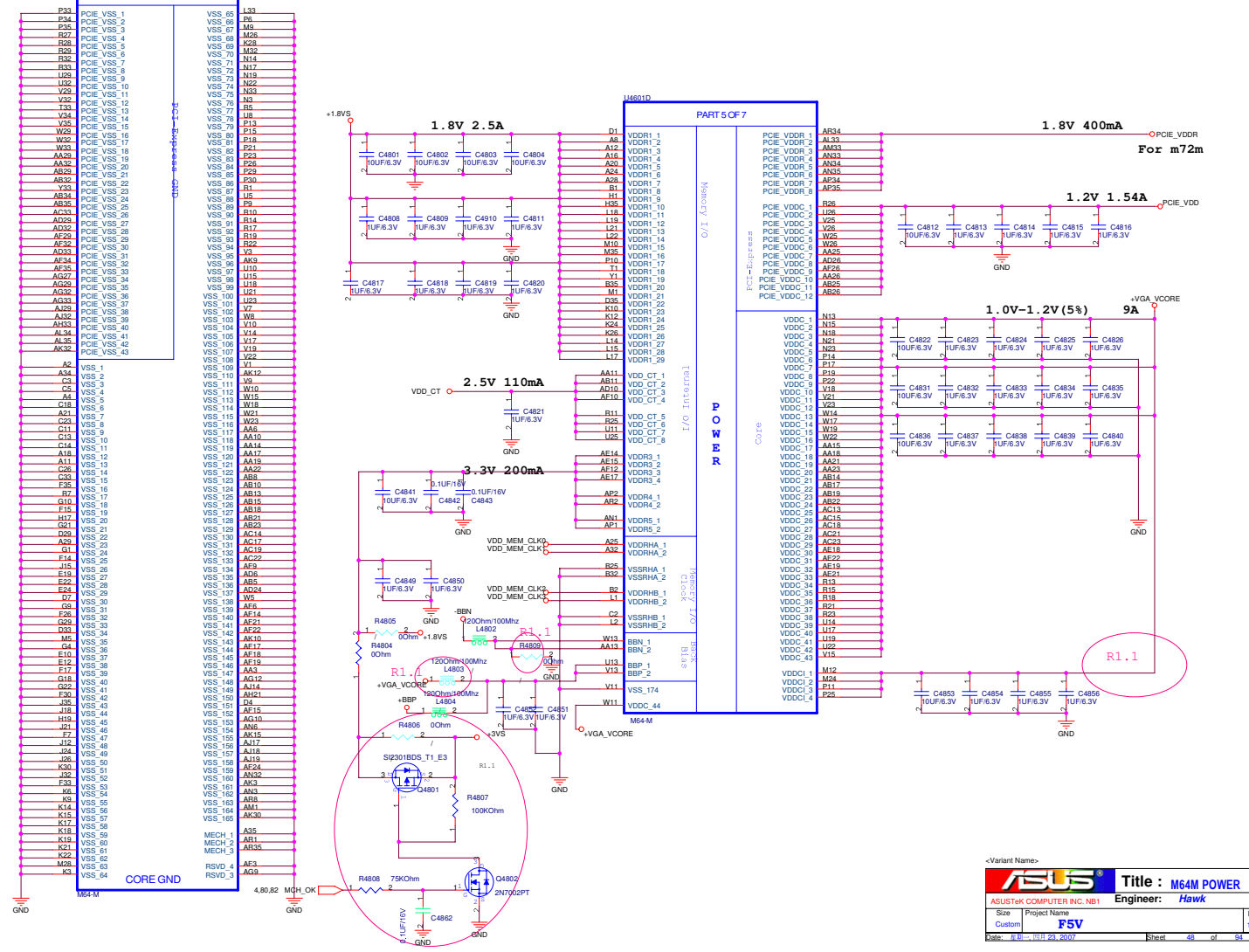
AG10 GPIO9
 AG11 SCLK
 AG12 GPIO11
 AG13 GPIO12
 AG14 GPIO13

AG15 GPIO19 CTF
 AG16 SCS4
 AG17 CS4

AG18 DPLL_PVDD 2.5V 170mA
 AG19 PCI_E_PVDD 1.2V 90mA
 AG20 MPVDD vga core 230mA
 AG21 DPLL_VDDC 1.5V 65mA

AG22 AG4
 AG23 AG4
 AG24 AG6
 AG25 AG6
 AG26 AG6
 AG27 AG6
 AG28 AG6
 AG29 AG6
 AG30 AG6
 AG31 AG6
 AG32 AG6
 AG33 AG6
 AG34 AG6
 AG35 AG6
 AG36 AG6
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 AG46 AG6
 AG47 AG6
 AG48 AG6
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U4601B PART2 OF 7
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<Variant Name>

ASUS Title : M46M POWER

ASUSTek COMPUTER INC.NB1 Engineer: Hawk

Size	Project Name	Rev
Custom	FSV	1.0

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51 ODTA0 << ODTA0

51 ODTA1 << ODTA1

51 RASAO# << RASAO#

51 RASAI# << RASAI#

51 CASAO# << CASAO#

51 CASAI# << CASAI#

51 WEAO# << WEAO#

51 WEAI# << WEAI#

51 CKEAO << CKEAO

51 CKEAI << CKEAI

51 CSA0_0# << CSA0_0#

51 CSA1_0# << CSA1_0#

51 CLKA0 << CLKA0

51 CLKA0# << CLKA0#

51 CLKA1 << CLKA1

51 CLKA1# << CLKA1#

51 WDQSA7_0 << WDQSA7_0

51 RDQSA7_0 << RDQSA7_0

51 DQMA7_0 << DQMA7_0

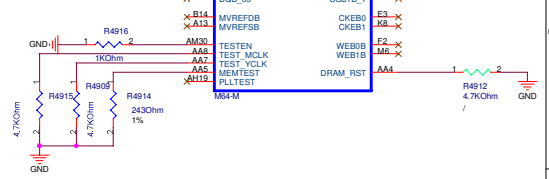
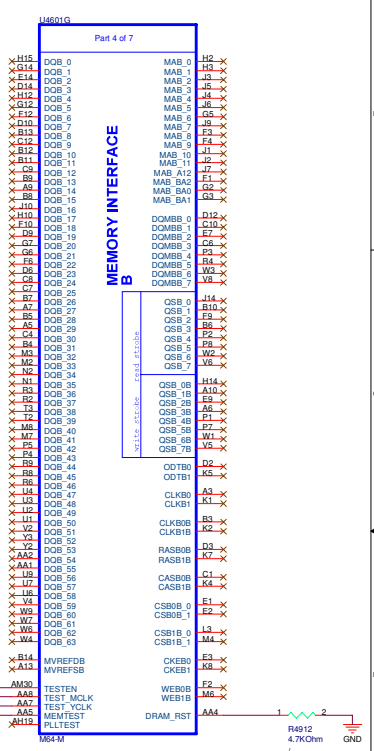
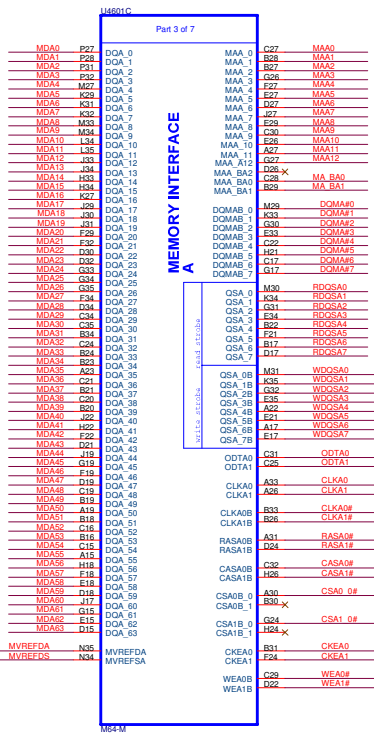
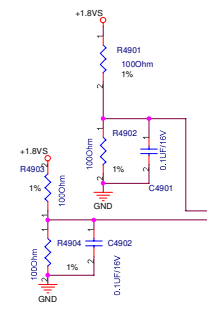
51 MDAS3_0 << MDAS3_0

51 MAI12_0 << MAI12_0

51 MA_BA0 << MA_BA0

51 MA_BA1 << MA_BA1

PLACE MVREF DIVIDERS
AND CAPS CLOSE TO
ASIC



COMPONENTS SHOWN ARE EXAMPLES ONLY AND NOT NECESSARILY QUALIFIED

BB_ENA = 0V FOR BACK BIASING DISABLED

MAX1673 SHUTDOWN

-BBN = 0V VIA MAX1673 INTERNAL 1 OHM TO GROUND

N FET A = OFF, P FET B = OFF, N FET C = ON

+BBP = VDD_CORE

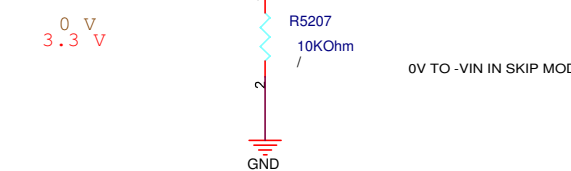
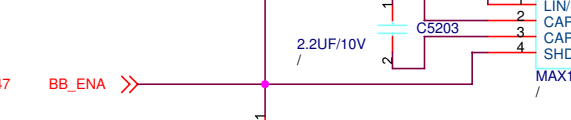
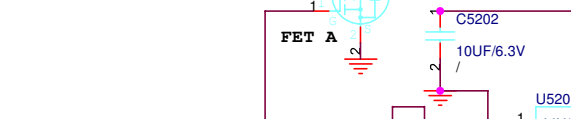
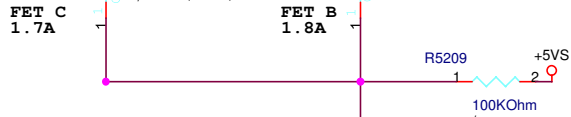
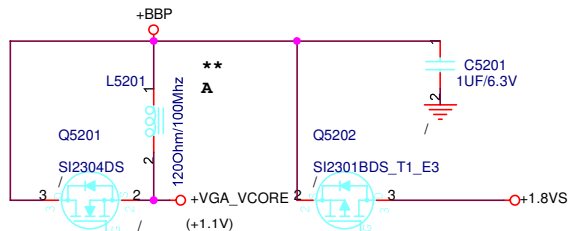
BB_ENA = +3.3V FOR BACK BIASING ENABLED

MAX1673 ENABLED

-BBN = -.5V

N FET A = ON, P FET B = ON, N FET C = OFF

+BBP = +1.5V



** FOR NO BACK BIASING

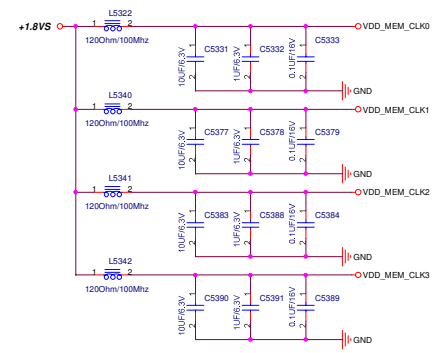
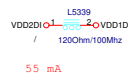
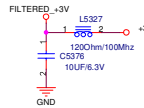
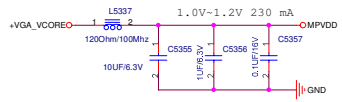
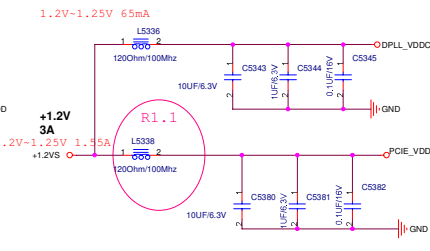
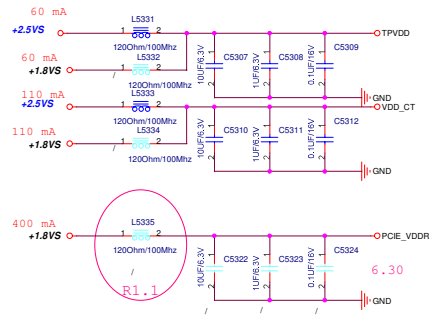
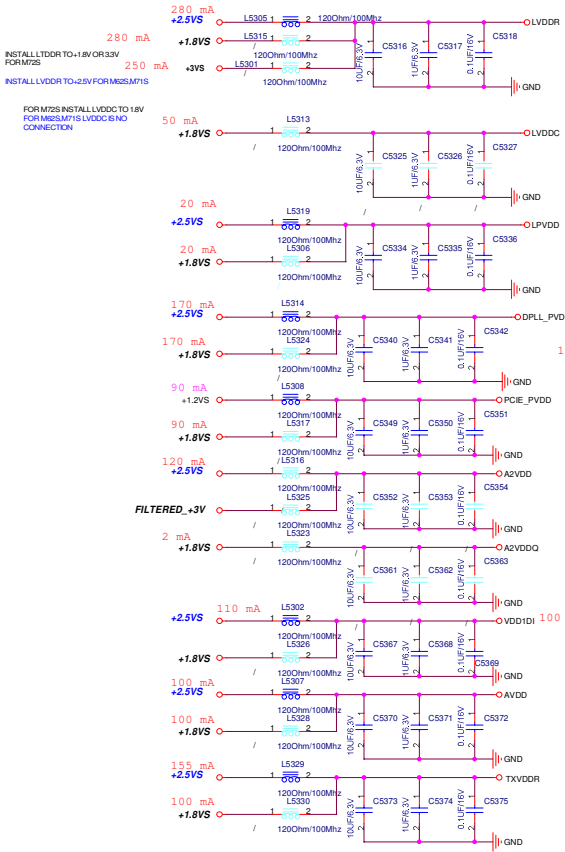
DO NOT INSTALL FETS OR REGULATOR LOGIC
AND INSTALL BEAD A AND RESISTOR A

		Title : BACK BIAS	
ASUSTeK COMPUTER INC. NB1		Engineer: Hawk	
Size A	Project Name F5V	Rev 1.0	
Date: 星期一, 四月 23, 2007		Sheet 52 of 94	

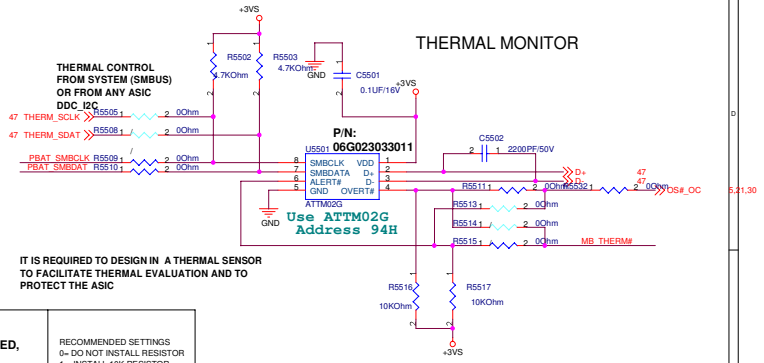
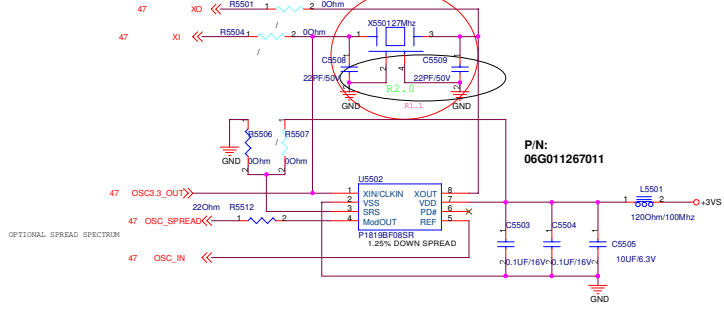
**COMPONENTS SHOWN ARE EXAMPLES ONLY
AND NOT NECESSARILY QUALIFIED**

LTPVSS18 DVSSDI TPVSS MPVSS
* PCIE_PVSS PVSS A2VSSQ AVSSQ

PLACE CAPS FOR THESE GROUNDS CLOSE TO ASIC AND RUN DEDICATED TRACKS FROM PINS TO JOIN THE GROUND PLANE WITH ONE VIA AT CAP



ASUS		Title : IO capacitor	
ASUSTek COMPUTER INC.NB1		Engineer: Hawk	
Size	Project Name	Rev	
Custom	FSV	1.0	
Date: 2007.11.24	Sheet: 53	of	94



IT IS REQUIRED TO DESIGN IN A THERMAL SENSOR TO FACILITATE THERMAL EVALUATION AND TO PROTECT THE ASIC

47	GPIO0	R5518	2	10K0Ohm
47	GPIO1	R5519	2	10K0Ohm
47	GPIO2	R5520	2	10K0Ohm
47	GPIO3	R5521	2	10K0Ohm
47	GPIO4	R5522	2	10K0Ohm
47	GPIO5	R5523	2	10K0Ohm
47	GPIO6	R5524	2	10K0Ohm
47	GPIO9	R5525	2	10K0Ohm
47	GPIO11	R5526	2	10K0Ohm
47	GPIO12	R5527	2	10K0Ohm
47	GPIO13	R5528	2	10K0Ohm
47	GPIO15_CTF	R5529	2	10K0Ohm
47	GPIO20	R5530	2	10K0Ohm
47	GPIO22	R5531	2	10K0Ohm
47	GPIO24	R5532	2	10K0Ohm
47	VID	R5533	2	10K0Ohm
47	VID	R5534	2	10K0Ohm
47	VID	R5535	2	10K0Ohm
47	VID	R5536	2	10K0Ohm
47	VID	R5537	2	10K0Ohm
47	DVALID	R5538	2	10K0Ohm
47	PSYNC	R5539	2	10K0Ohm
18,47	VGA_HSYNC	R5540	2	10K0Ohm
18,47	VGA_VSYNC	R5541	2	10K0Ohm
47	VHADD	R5542	2	10K0Ohm

CONFIGURATION STRAPS

ALLOW FOR PULLUP STRAPS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	M62S.M71S	M72S
BIF_MSI_DIS	VID1	MESSAGE SIGNAL INTERRUPT ENABLED	NA	0
BIF_64BAR_EN_A	VID5	64 BIT BARS DISABLED	NA	0
TX_PWR5_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	X	X
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	1	1
BIF_DEBUG_ACCESS	GPIO4	DEBUG SIGNALS NOT MIXED OUT	0	0
VID	GPIO6[5]	BIAS CURRENT FOR PCIE PHY PLL	0	1
PLL_BIAS_RD_1.0	GPIO6[5]	BIAS CURRENT FOR PCIE PHY PLL	0	1
BIOS_ROM_EN	GPIO19_CTF	SERIAL EXTERNAL BIOS ROM	NA	X
ROMIDCFG(3,0)	GPIO[13:11,9]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	XX X X	X X X X
VIP_DEVICE_STRAP_ENA	VSYN0	IGNORE VIP DEVICE STRAPS	0	0
VIP_VGA_DIS	PSYN0	VGA ENABLED	NA	0
MEM_TYPE	UNUSED GPIO	MEMORY TYPE MAKE AND SIZE INFO	X X X	X X X

RECOMMENDED SETTINGS
 0= DO NOT INSTALL RESISTOR
 1= INSTALL 10K RESISTOR
 X= DESIGN DEPENDANT
 NA= NOT APPLICABLE

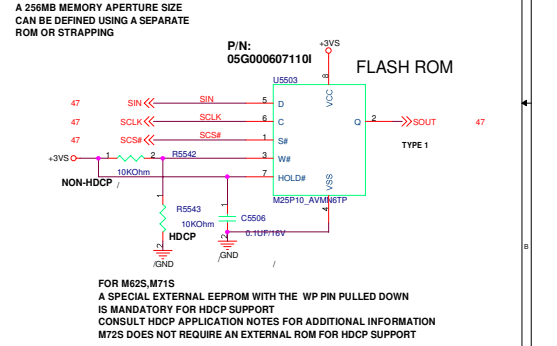
ATI RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

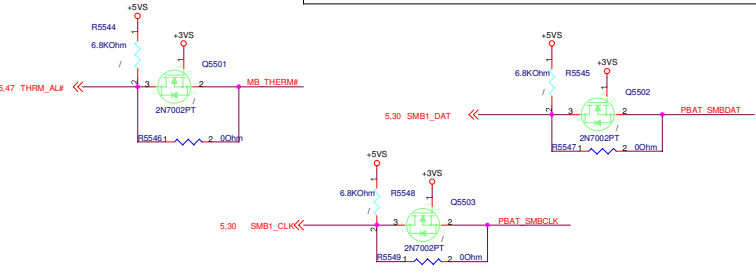
VID0	VID2	VID3	VID4	VID6	VID7	HSYN0	GPIO8	DVALID	GPIO2	GPIO3

PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

GENERIC	GPIO18_HPxD3	GPIO23_CLKREQ0B

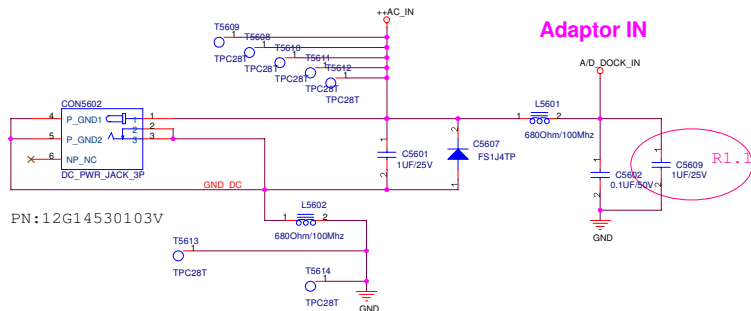
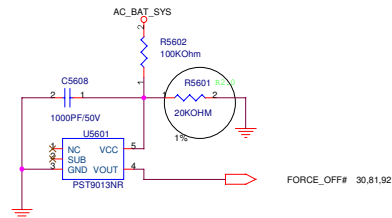
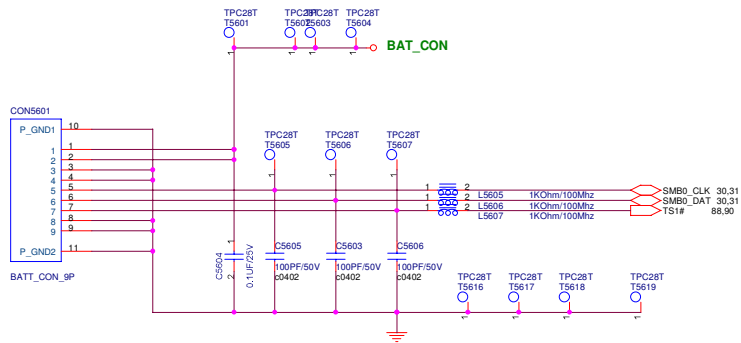


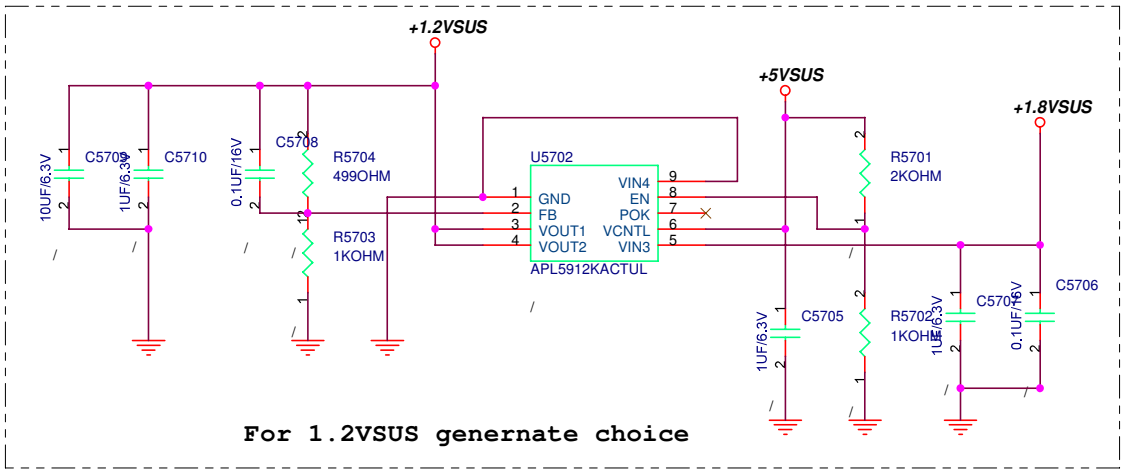
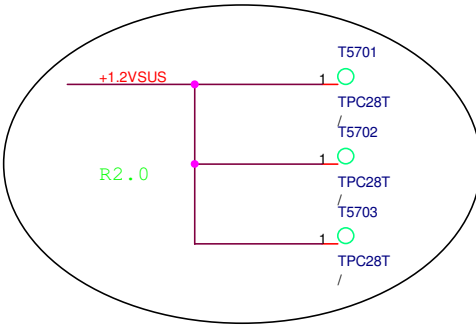
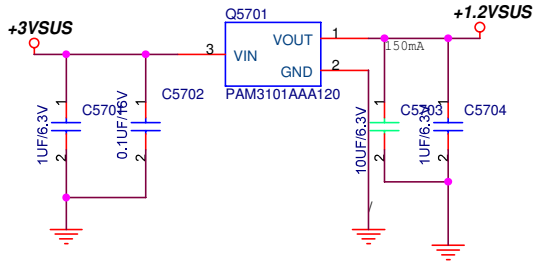
FOR M62S.M71S A SPECIAL EXTERNAL EEPROM WITH THE WP PIN PULLED DOWN IS MANDATORY FOR HDCP SUPPORT CONSULT HDCP APPLICATION NOTES FOR ADDITIONAL INFORMATION M72S DOES NOT REQUIRE AN EXTERNAL ROM FOR HDCP SUPPORT



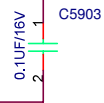
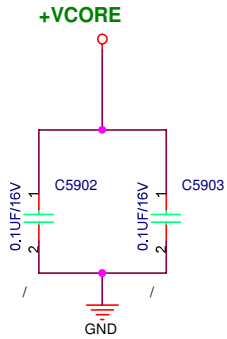
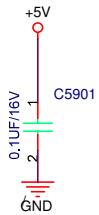
COMPONENTS SHOWN ARE EXAMPLES ONLY AND NOT NECESSARILY QUALIFIED

ASUS		Title :	SS STRAPS
ASUSTek COMPUTER INC. N81	Size	Project Name	Engineer: Hawk Kaxidy
Custom	Size	Project Name	Rev
Date: 11/01/2007	1.0	Sheet	56 of 94





		Title : +1.2VSUS
ASUSTeK COMPUTER INC. NB1		Engineer: <i>Kaxidy/Hawk</i>
Size	Project Name	
A	F5V	
Date: 星期一, 四月 23, 2007		Sheet 57 of 94
		Rev 1.0



		Title : EMI
ASUSTeK COMPUTER INC. NB1		Engineer: Kaxidy/Hawk
Size A	Project Name F5V	Rev 1.0
Date: 星期一, 四月 23, 2007		Sheet 59 of 94

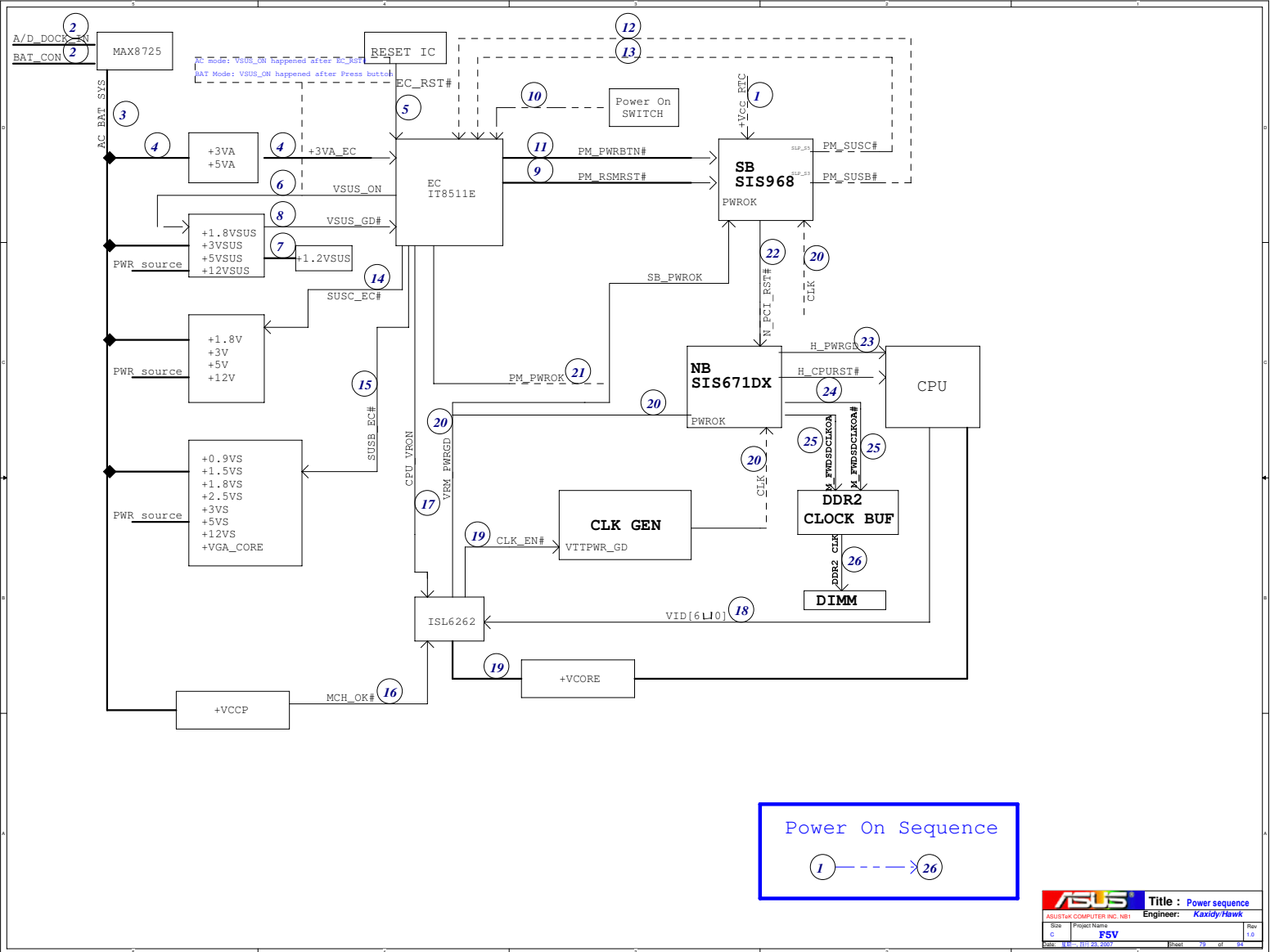
1. P2 unmount R201 for H_CPURST#, add T205/T206 for CLK_CPU_BCLK#/CLK_CPU_BCLK test.
2. P6 mount R605 for H_PWRGD timing, add T603/T604/T605/T606 to HA[32:35]#.
3. P7 unmount R706
4. P20 mount R2001/R2002/R2003/R2009/R2011 for PCI_REQ#[0:4]
5. P21 change R2121 to 00hm
add R2124(330hm) for AC2_RST# according to 968 ACT.
add R2108/R2112(00hm) for PCIEPRSNTO/1 according to sis ACT
ADD GMAC OS22RMIH to GND according to sis ACT.
unmount L2103, mount L2105 according to spec.
unmount R2122 for repeat with R2453, change R2120/R2125 PU to +3VSUS according to spec.
change GPIO17 from VIN4 to S_A20GATE, add R2127(00hm) for reserve SUSCLK
6. P17 add R1708 and R1709 to change BL_PWM to BL_ENA to fix garbage
7. P22 change R2217 to 12K0hm, add C2237(22pF) for SATA REXT according to 968 ACT.
8. P24 add R2434 for A20GATE to H_A20M#, add R2457 for A20GATE to S_A20GATE, add R2456 to PU S_A20GATE
9. P29 add R2909/R2910(00hm), unmount L2901 for EMI.
10. P30 change D3002 to R3009 for OS#_OC to avoid no EC reset, .
delete D3004 for DDR power are not SUS power,
add R3045 for VSUS_GD# PU, change GPJ0 to VIN4 to control NEW card shutdown, add R3046 for VIN4,
Add R3019 for INSTANTON#
11. P33/P5/P32 change the P/N of CE3202/CE501/CE3301/CE3302/CE3303/CE3304 for low cost
12. P37 mount R3716/Q3715 for +VCCP discharge
13. P42 change IDSEL to PCI_AD24
14. P46 add D4602 for VGA_RST#
15. P48 unmount L4803/R4809, delete L4801
unmount R4806, mount Q4801/R4807/Q4802/R4808
16. P53 change L5335/L5338 to match the current.
17. P55 change X5501 to +-10ppm to follow spec, add C5508/C5509 to match X5501
18. P56 add C5609 for over current damaging charge IC.
19. P4 Change C440 from 0.1UF to 0.22UF
20. P10 change L1001 to 2A to match the current, Add +1.2VS delay circuit.
21. P21 add VGA_RST# to GPIO7, add R2140 for VGA_RST#.
22. P47 Unmount R4759, mount R4758 for Vram changed from 03G151236011 to 03G151236012.

F5VL

1. P2/3 change CPU socket to P
2. P32 delete R3205/R3212
3. P59 add C5902/C5903 for EMI

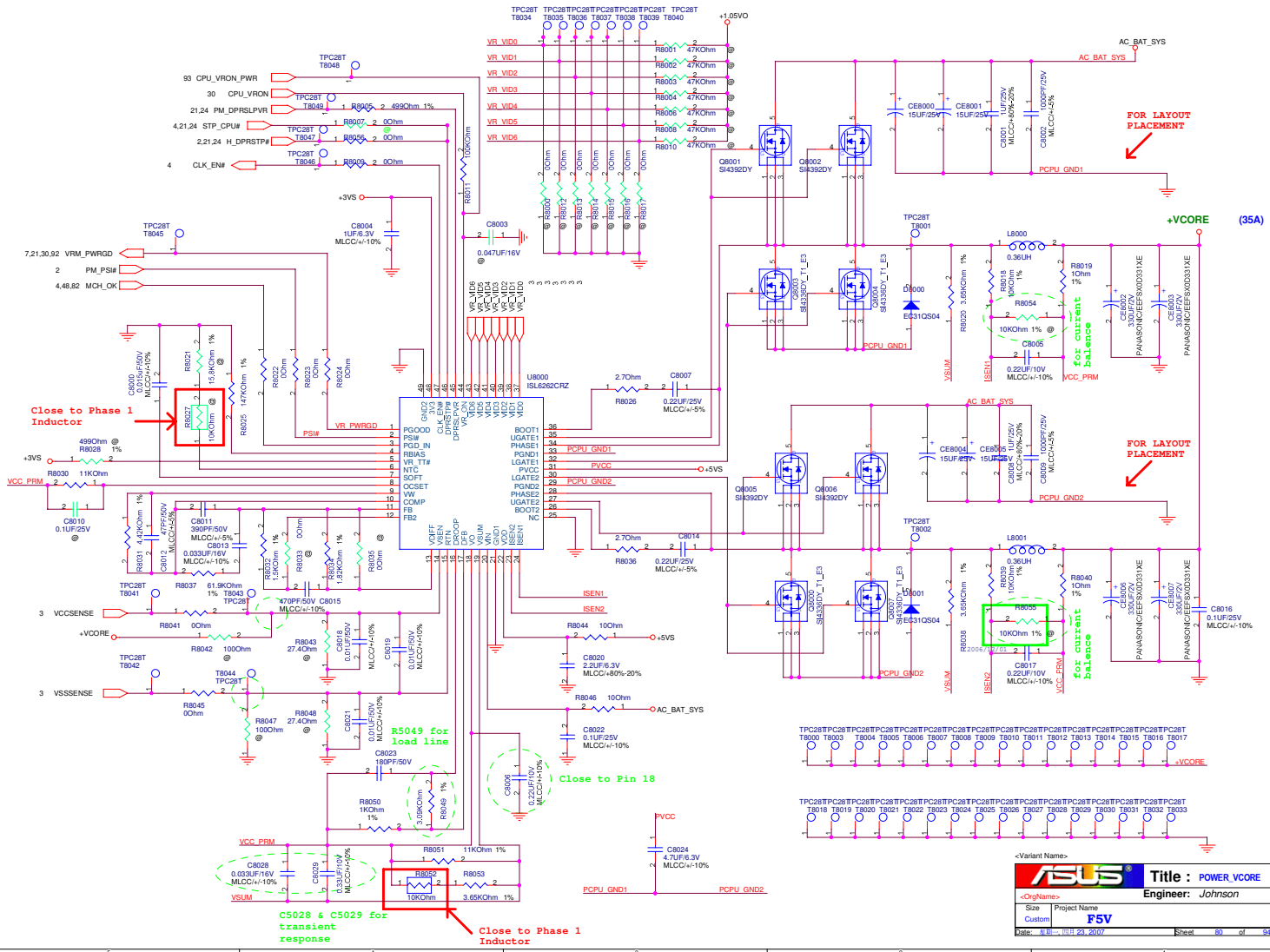
R2.0

1. P25 mount R2907 connect PCIE_PRSNT1 to GPP#
2. P21 unmount R2108, mount R2119, change R2118 from 00hm to 4.7K0hm but unmount R2118
2. P27 change R2708 to 00hm and mount it to not support C3 mode
3. P33422 add two TPS2061 (U3301/U3302) to avoid not start up caused by USB device with external power supply
4. P21 add R2141 to connect OS#_OC to PM_THERMTRIP#, change R2141 to Q2101
5. P30 change C3009/C3003 to 6.8pF
6. P27 change C2706/C2707 to 24pF
7. P55 change C5508/C5509 to 22pF
8. P33 unmount R3313/R3305/R3304/R3303/R3310/R3316/R3308/R3306, mount L3304/L3301/L3305/L3303, mount D3302/D3303/D3306/D3307/D3301
9. P47 add R4747/R4749 to reserve EDID_DAT/EDID_CLK to DDC3
10. P30 change Q3003 PU from +5V to +5VS
11. P5 unmount R506
12. P56 change R5601 to 20K0hm
13. P20 unmount R2054, add and mount C2010
- P32 add R3215 to connect S_CBLIDA to IDE_DIAG, unmount C3206
- P22 add and unmount C2215/C2238/C2239/C2236, add and mount C2206
14. P27 change 4in1 cardreader
15. P47 mount R4704/R4705/R4706/R4707
- P18 change DVI bead to R1832/R1833/R1834/R1835/R1836/R1837/R1838/R1839, change R1832/R1833/R1834/R1835/R1836/R1837/R1838/R1839 reference to L1806/L1807/L1808/L1809/L1810/L1811/L1812/L1813
16. P21 Unmount L2105, mount L2103
17. P21 change R2116 from 330hm to 200hm, change R2117 from 330hm to 00hm, change R2119 from 330hm to 200hm
- P24 change R2418 from 330hm to 00hm, change R2420 from 330hm to 00hm, change R2419 from 330hm to 00hm, change R2422 from 330hm to 00hm, change R2423 from 330hm to 00hm, change R2425 from 330hm to 00hm
- P25 change R2514 from 330hm to 470hm

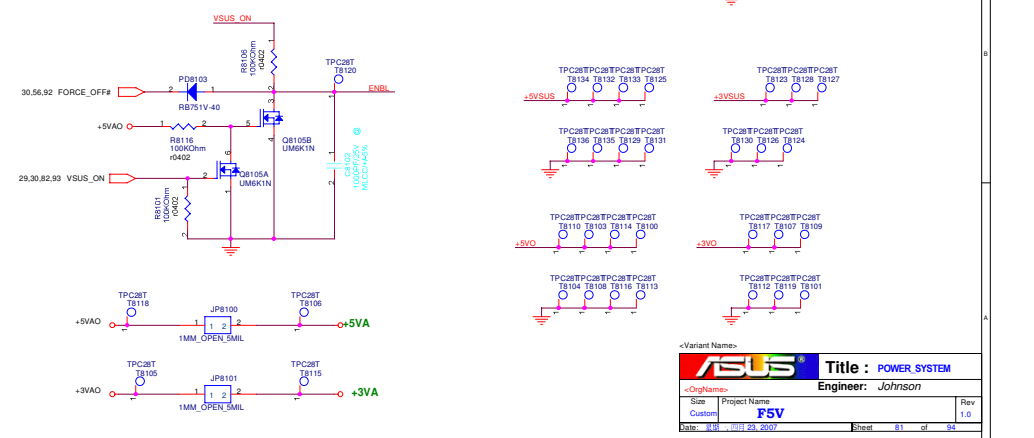
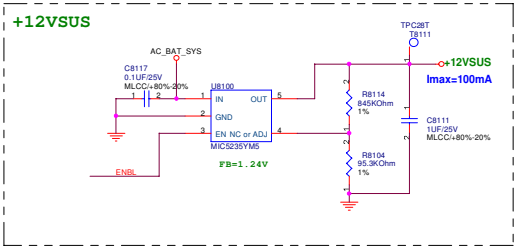
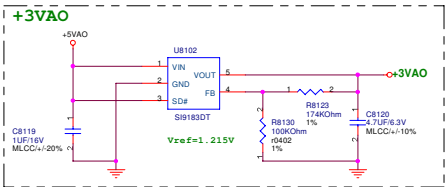
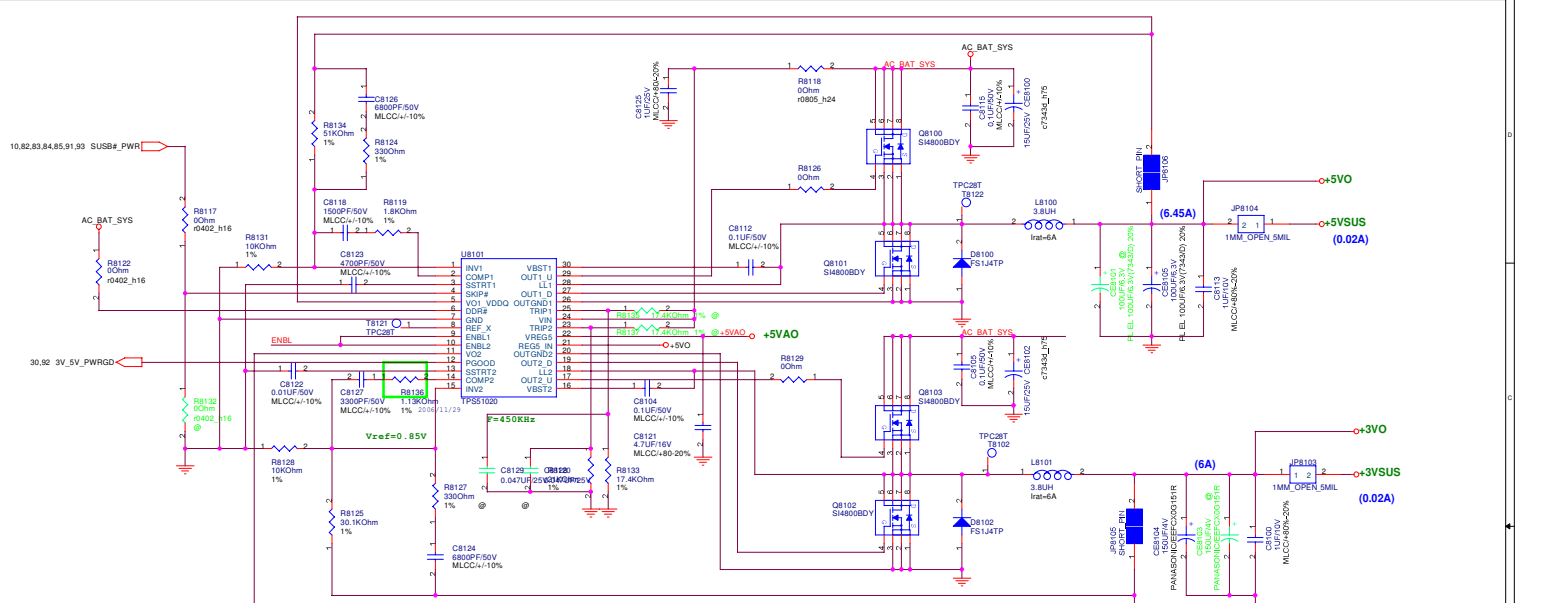


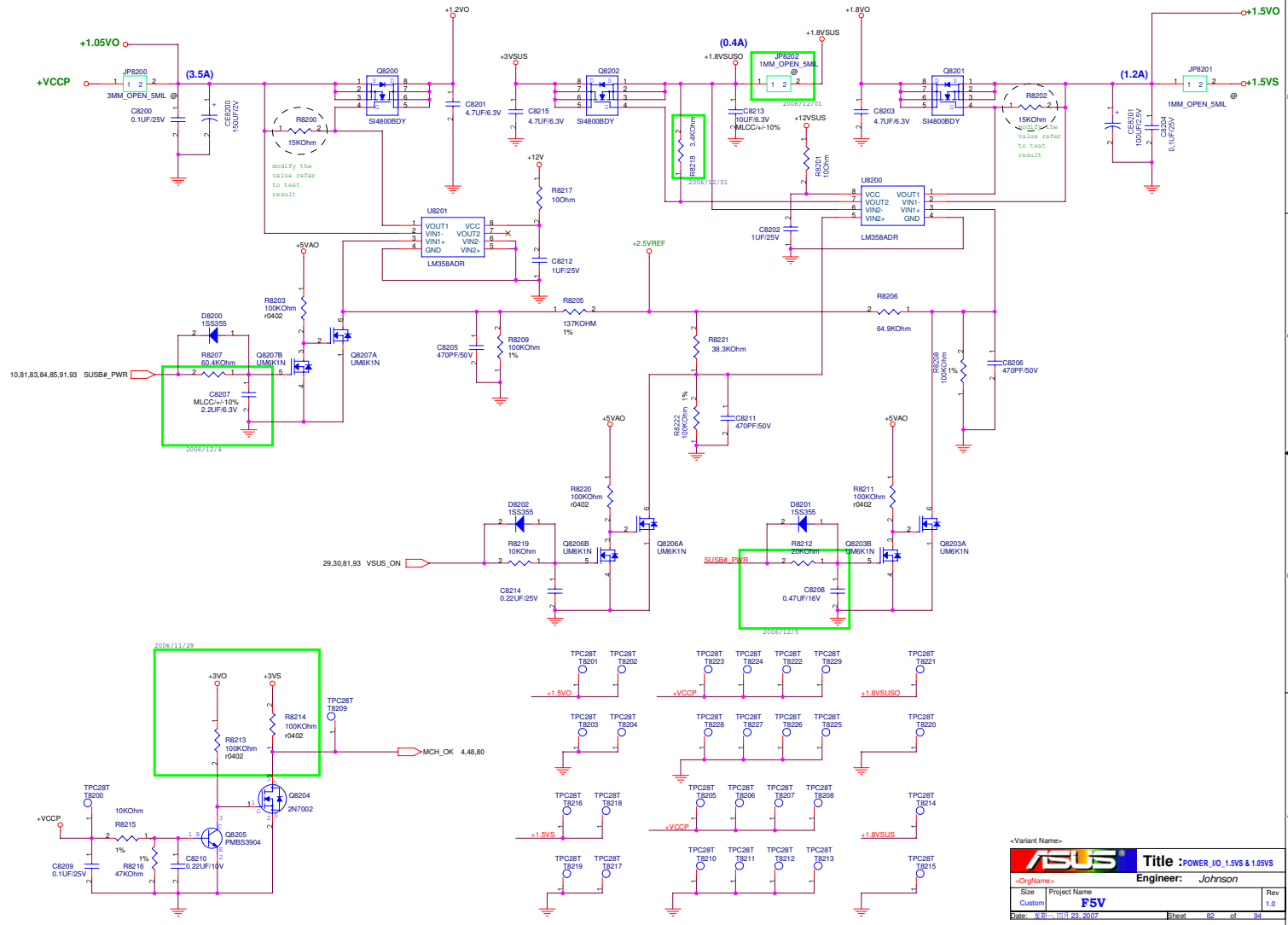
A/D_CONVERTER
BAT_CON

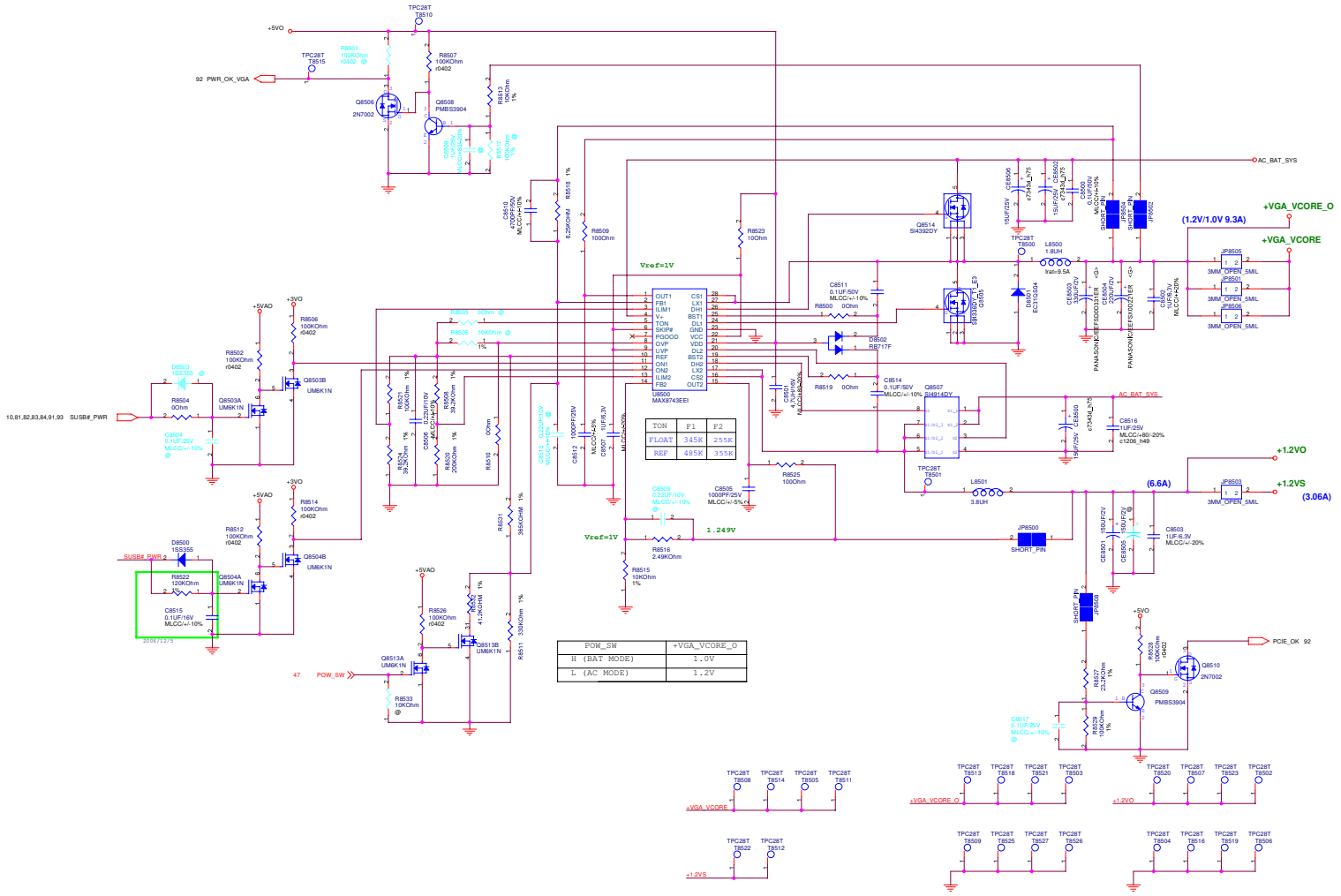
EC Mode: VSUS_ON happened before To_Bat
BAT Mode: VSUS_ON happened after Press buttk



ASUS		Title : POWER VCORE
Engineer: Johnson		
Size	Project Name	Rev
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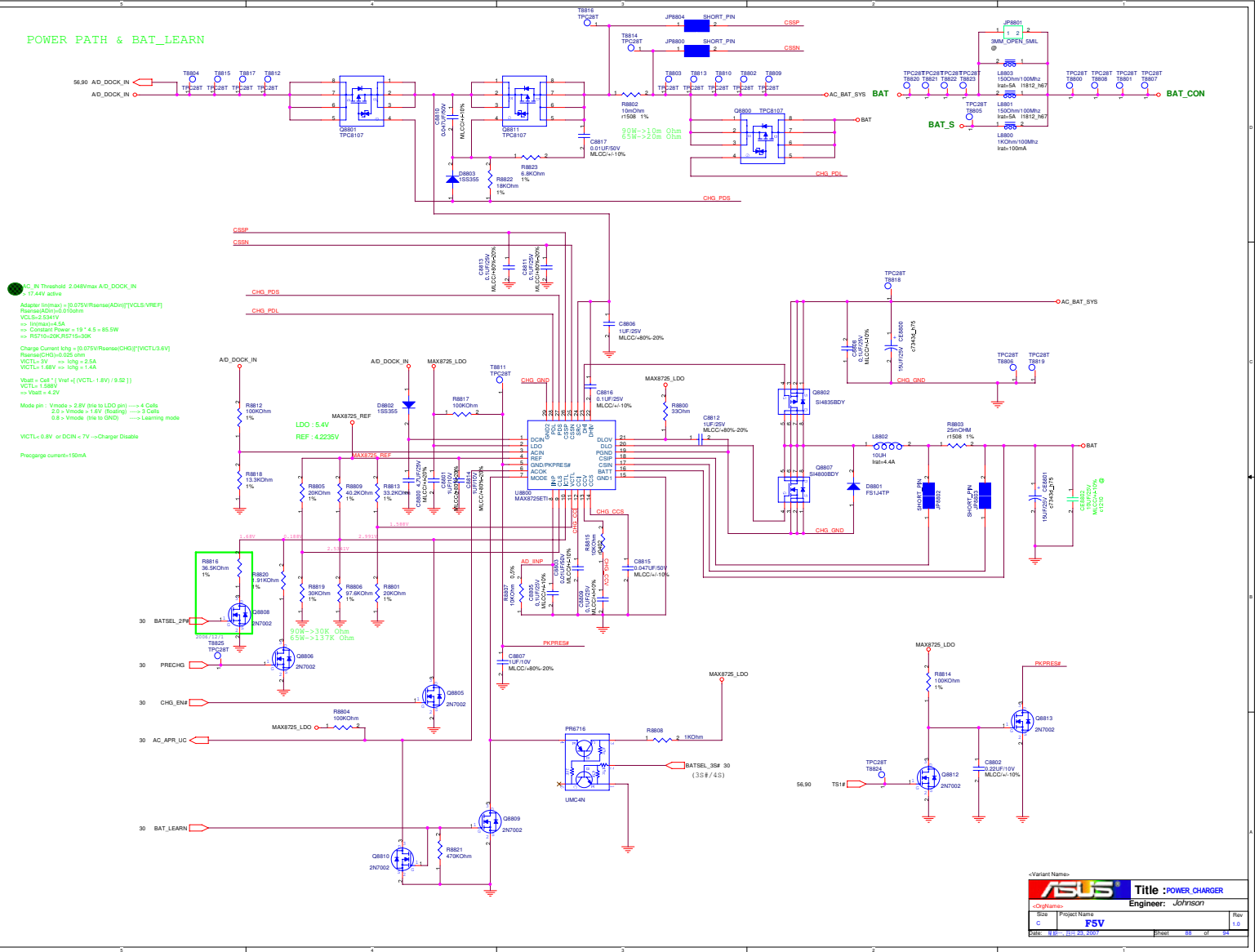




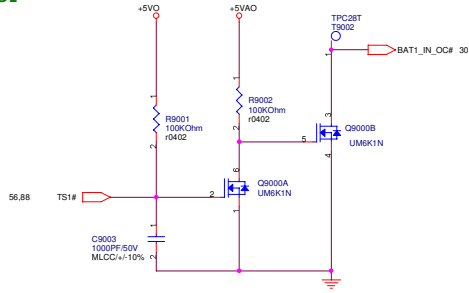


POWER PATH & BAT_LEARN

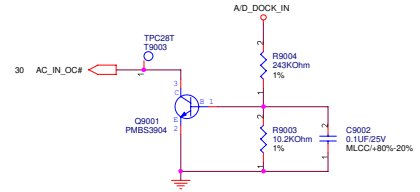
AC_IN Threshold 2.048Vmax AD_DOCK_IN > 17.44V active
Adapter (nominal) = (0.075V/Rsense(ADIN))*(VCL5_VREF/Rsense(ADIN)+0.000000)
VCL5=2.541V
 \Rightarrow $1000\text{mA} \times 4.54$
 \Rightarrow Constant Power = $13 \times 4.5 = 85.5\text{W}$
 \Rightarrow $R5710=20k, R5715=50k$
Charge Current $I_{chg} = (0.075\text{V}/\text{Rsense(CHG))*(VCTL3_V)/\text{Rsense(CHG)+0.000000}$
VCTL3=0.000000
 \Rightarrow $VCTL3 = 3\text{V} \Rightarrow I_{chg} = 2.5\text{A}$
 \Rightarrow $VCTL3 = 5.65\text{V} \Rightarrow I_{chg} = 1.4\text{A}$
Yhat = $Cd \times (V_{in} - (VCTL1 - 1.5\text{V}) / 9.52)$
VCTL1 = 1.58V
 \Rightarrow $V_{in} = 4.2\text{V}$
Mode pin: $V_{mode} > 2.5\text{V}$ (sig to LDO pin) \rightarrow 4 Cells
 $2.0 < V_{mode} < 1.6\text{V}$ (floating) \rightarrow 3 Cells
 $0.8 < V_{mode}$ (sig to GND) \rightarrow Learning mode
VCTL4=0.6V or DCIN = 7V \rightarrow Charger Disable
Precharge current=150mA



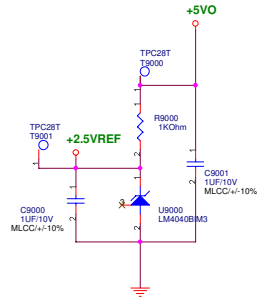
BATTERY IN DETECT



ADAPTER IN DETECT

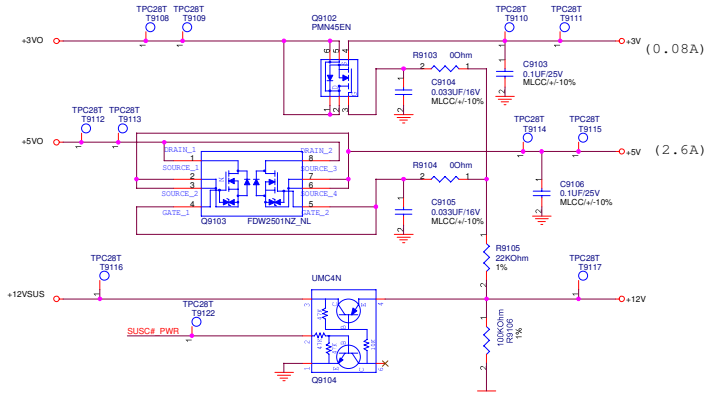
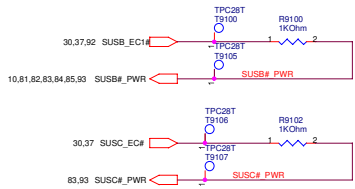


+2.5VREF

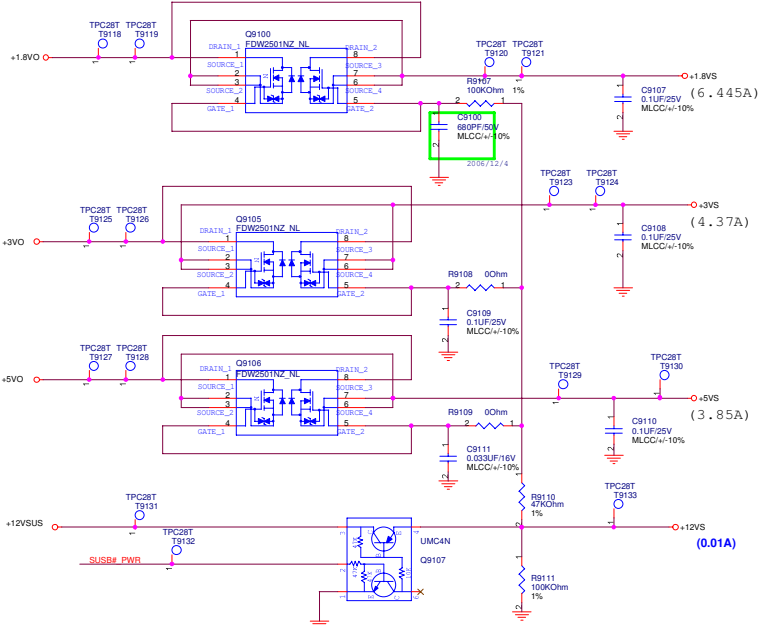


-Variant Name-		ASUS Title :POWER_DETECT	
-OrigName-		Engineer: Johnson	
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Custom	FSV	1.0	
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SUSC#_STAGE POWER



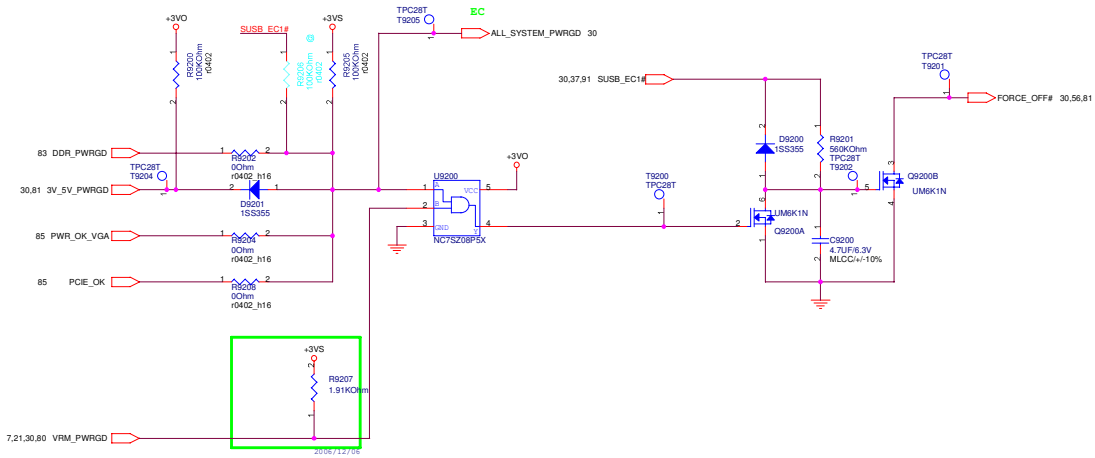
SUSB#_PWR POWER



<Variant Name>

ASUS		Title :POWER LOAD SWITCH
<OrigName>		Engineer: Johnson
Size	Project Name	Rev
Custom	FSV	1.0
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POWER GOOD DETECTOR



<Variant Name>

ASUS		Title :POWER_PROTECT
<OrigName>		Engineer: Johnson
Size	Project Name	Rev
Custom	FSV	1.0
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