Compal confidential

Schematics Document
Mobile Yonah uFCPGA with Intel
Calistoga_GM+ICH7-M core logic

2006-02-27

REV:0.5

硬體二部
機密
解密日期 *Feb 27, 2007*

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Compal Electronics, Inc.

Title: *Cover Sheet*

Size | Document Number: *LA-3031P* | Rev: 0.5

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File Name : LA-3031

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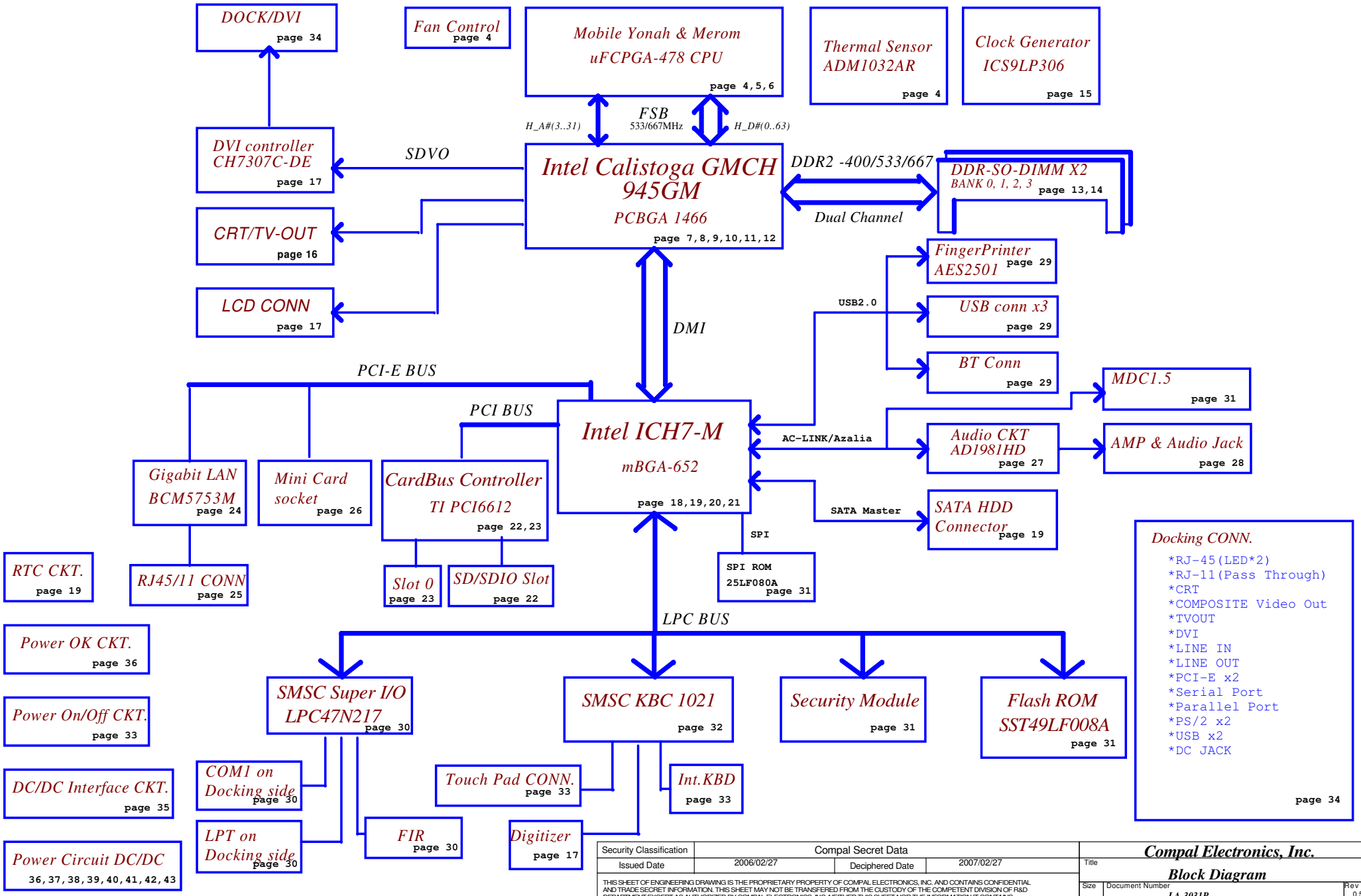

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Title	Block Diagram		
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Voltage Rails

Power Plane	Description	S0-S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VCCP	1.05V power rail for Processor I/O and MCH core power	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDRII Vtt	ON	OFF	OFF
+1.5VS	1.5V switched power rail for PCI-E interface	ON	OFF	OFF
+1.8V	1.8V power rail for DDRII	ON	ON	OFF
+2.5VALW	2.5V always on power rail	ON	ON	ON*
+2.5VS	2.5V switched power rail for MCH video PLL	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3V power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5V	5V power rail	ON	ON	OFF
+5VS	5V switched power rail	ON	OFF	OFF
RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

Symbol note:

:means digital ground.

:means analog ground.

@ :means reserved.

@ : means just reserve , no build
SPI@ : means just build when SPI I/F BIOS function enable.
FWH@ : means just build when FWH I/F BIOS function enable.
NOXDP@ : means just build when XDP function disable.
XDP@ : means just build when XDP function enable. When this time, docking PCI express will not work.
TPM@ : means just build when TPM1.2 function enable.
250@ : means just build when SMsC LPC47N250 chip selected.
1021@ : means just build when SMsC KBC1021 chip selected.
45@ : means need be mounted when 45 level assy or rework stage.
ACCEL@ : means just build when Accelerometer chip LIS3LV02DQ selected.
DVI_7307@ : means just build when DVI chip CH7307 selected.
DVI_1362@ : means just build when DVI chip SIL1362 selected.

Internal PCI Devices

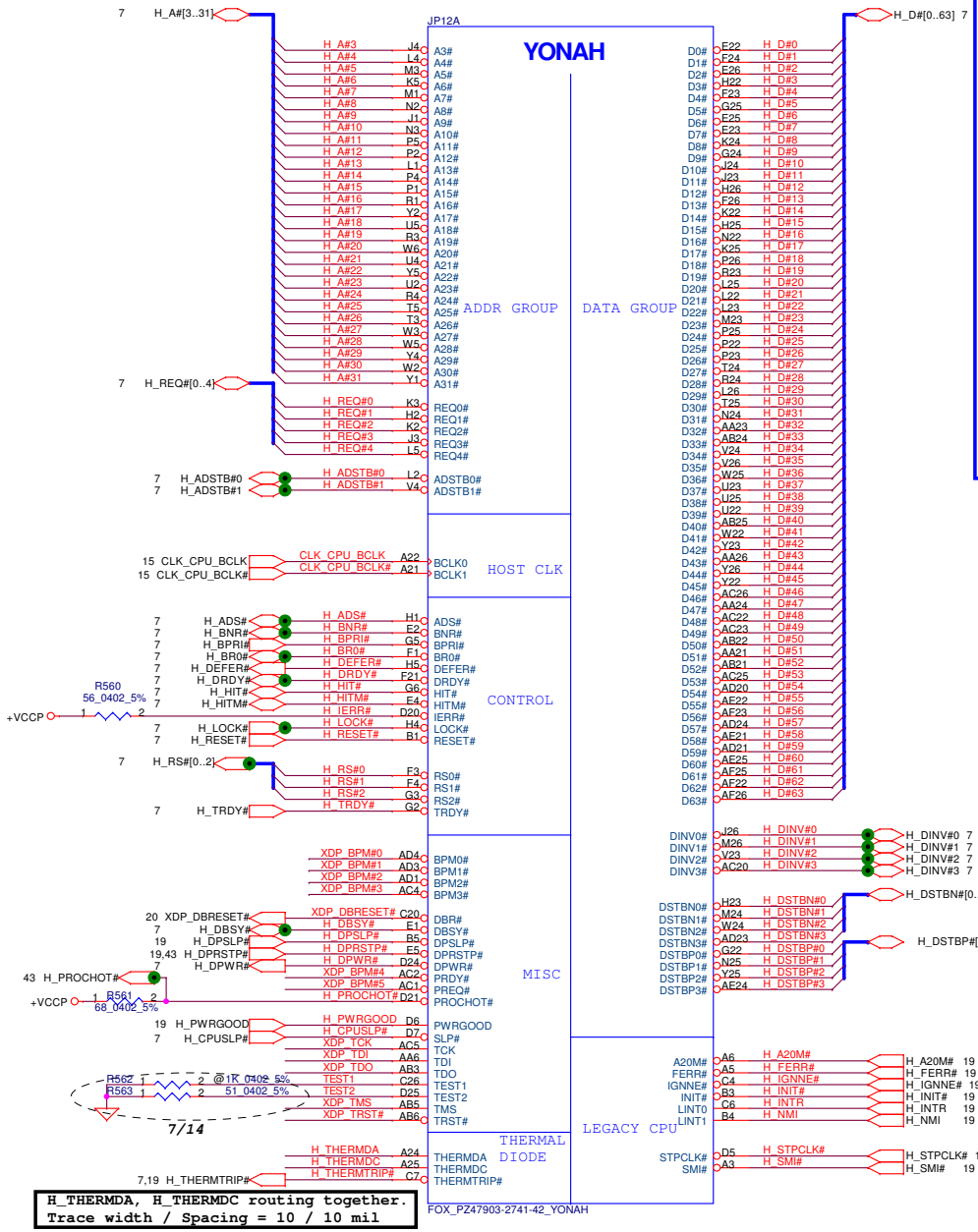
DEVICE	PCI Device ID	IDSEL #	
LAN	D8	AD24	
Azalia	D27	AD11	
PCI-E	D28	AD12	
USB1.1/2.0	D29	AD13	
PCI to PCI (DMI to PCI)	D30	AD14	
AC97 MODEM	D30	AD14	(Disabled by BIOS)
AC97 Audio	D30	AD14	(Disabled by BIOS)
PATA/SATA	D31	AD15	(PATA is Disabled by BIOS)
LPC I/F	D31	AD15	
SMBUS	D31	AD15	

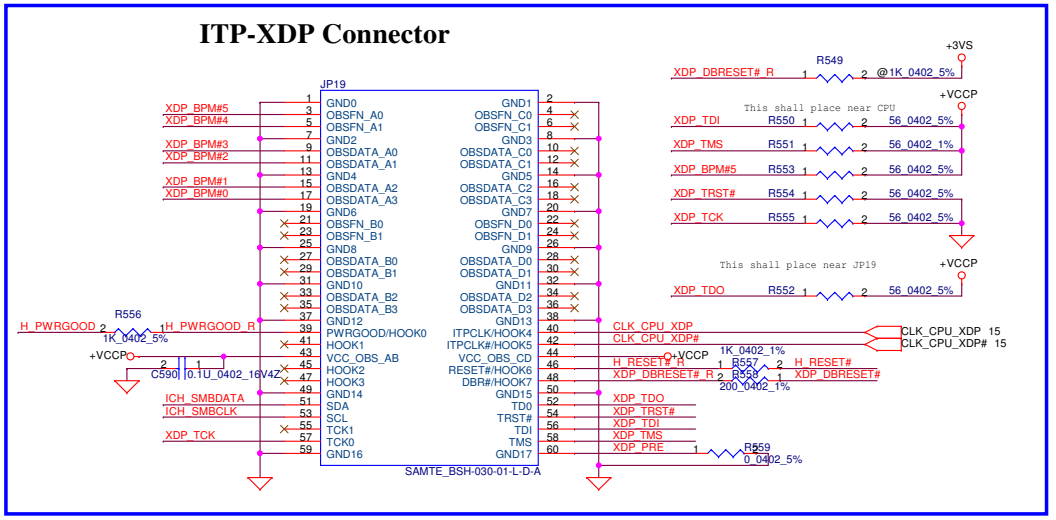
External PCI Devices

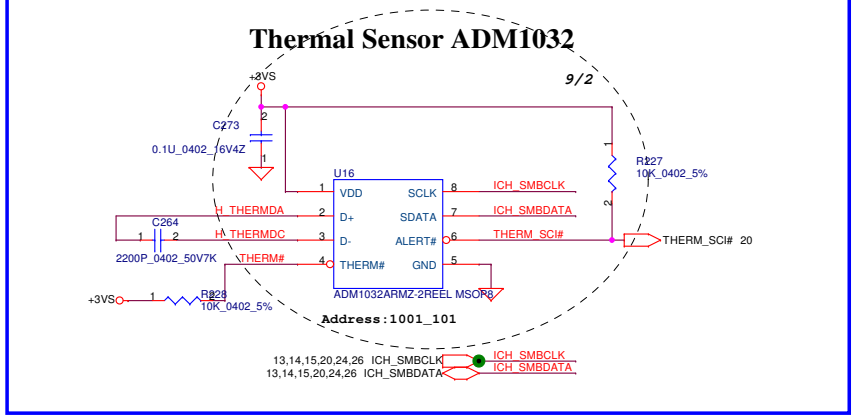
DEVICE	PCI Device ID	IDSEL #	REQ/GNT #	PIRQ
CARD BUS	D6	AD22	2	C D E G

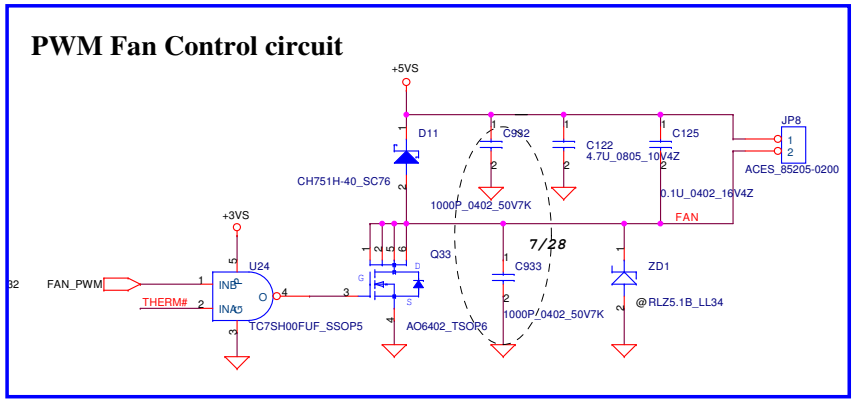
I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 0
DDR SO-DIMM 1	A4	1 0 1 0 0 1 0 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0









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Title: **Yonah CPU in mFCPGA479**

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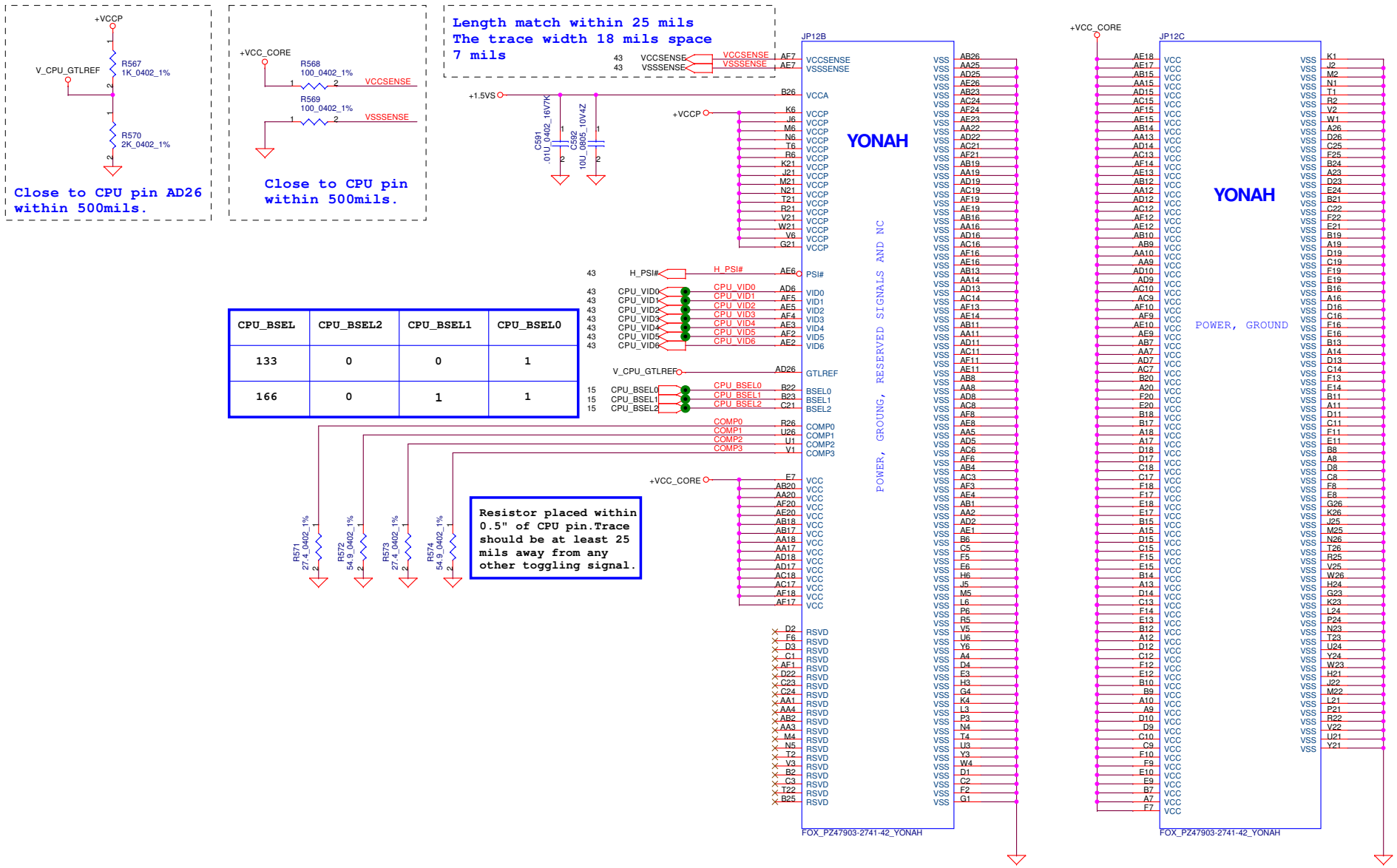

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
133	0	0	1
166	0	1	1

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Title	Yonah CPU in mFCPGA479
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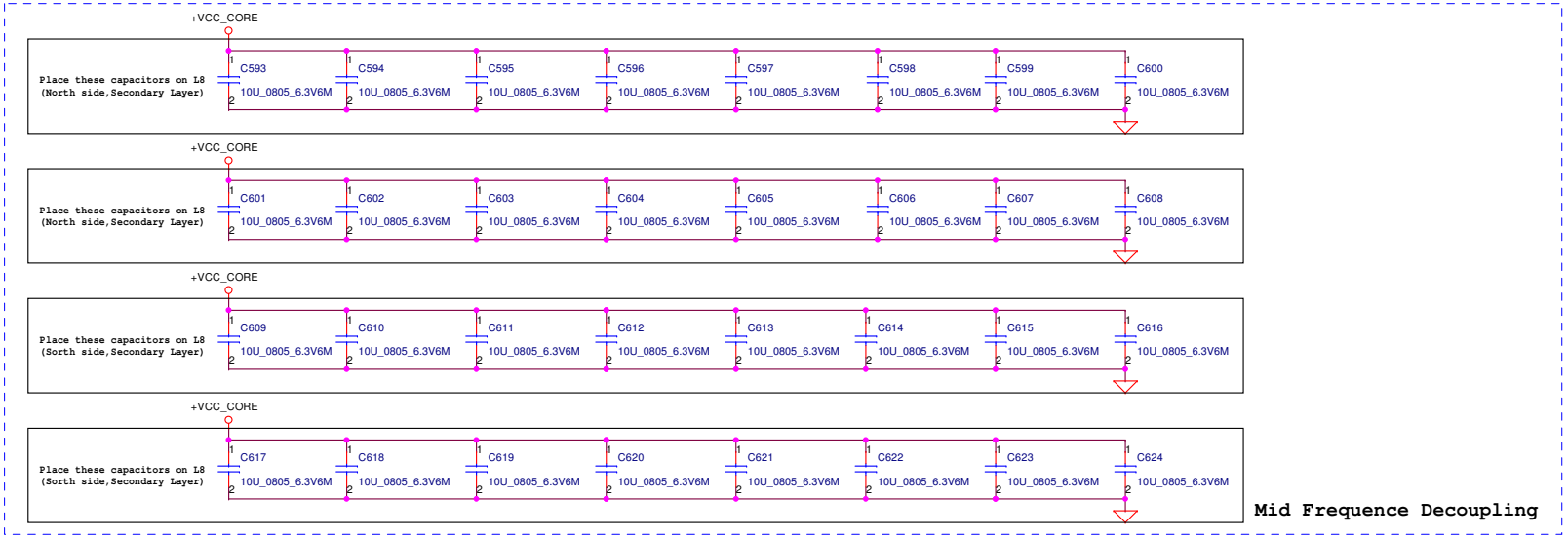
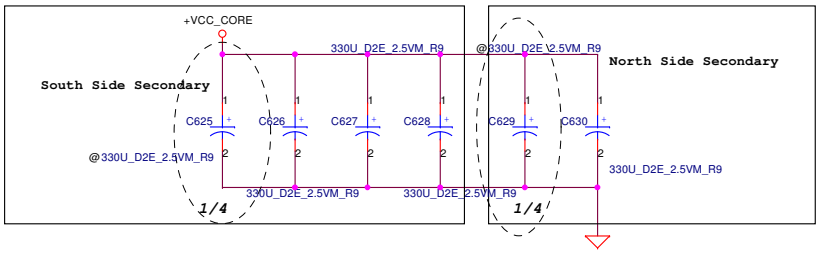
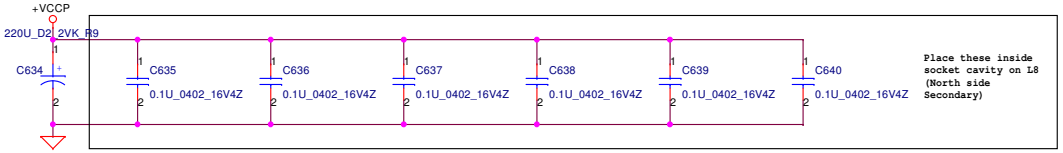




ESR = 1.5m ohm
Capacitor = 1980uF



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Compal Electronics, Inc.			
Title	CPU Bypass capacitors		
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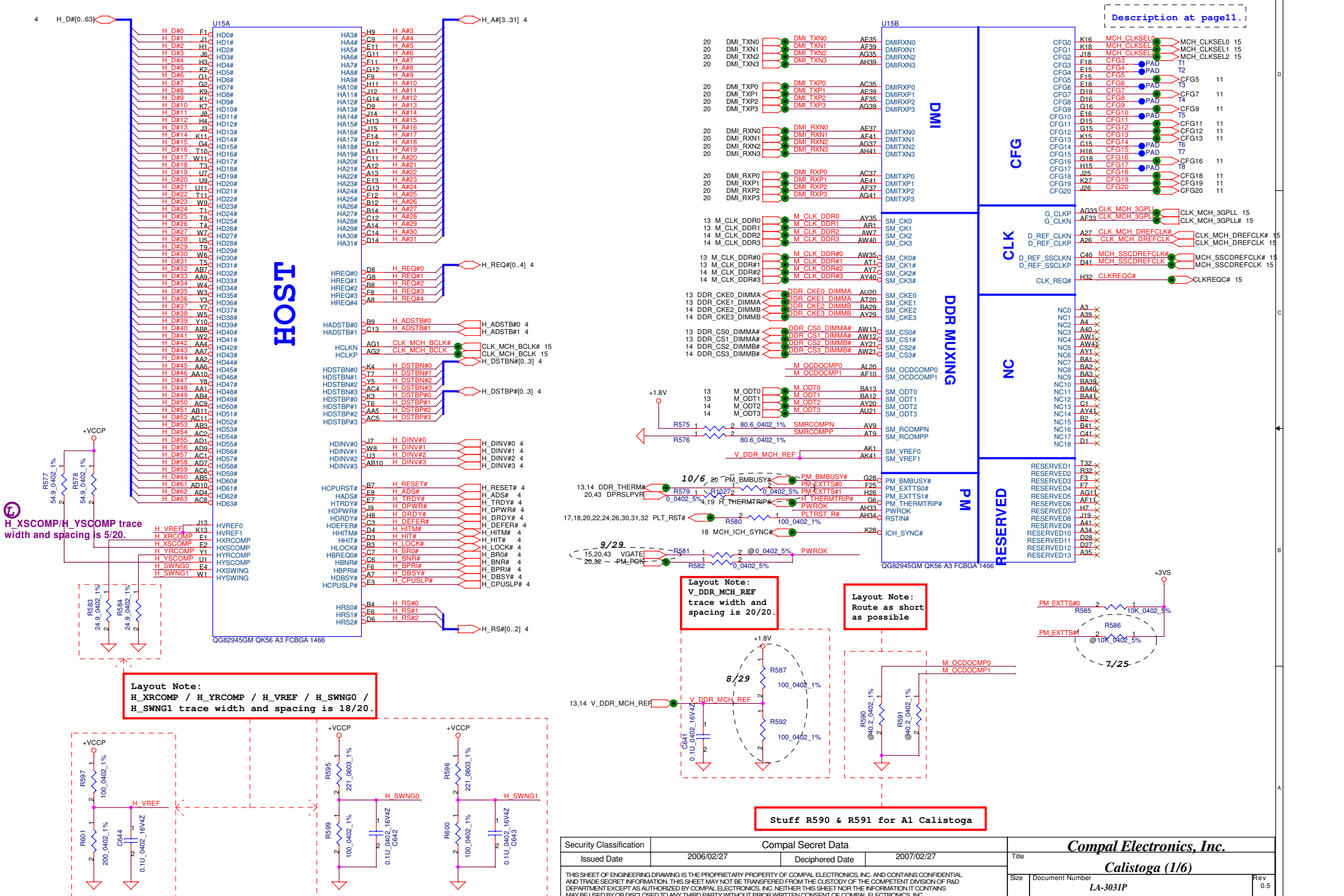
HOST
U15A
QG82945GM QK56 A3 FCBGA 1466
U15B
QG82945GM QK56 A3 FCBGA 1466
DMI
DDR MUXING
CFG
CLK
NC
PM
RESERVED
Description at page11.
H_XSCOMP/H_YSCOMP trace width and spacing is 5/20.
Layout Note:
H_XRCOMP / H_YRCOMP / H_VREF / H_SWNG0 / H_SWNG1 trace width and spacing is 18/20.
Layout Note:
V_DDR_MCH_REF trace width and spacing is 20/20.
Layout Note:
Route as short as possible
Stuff R590 & R591 for A1 Calistoga
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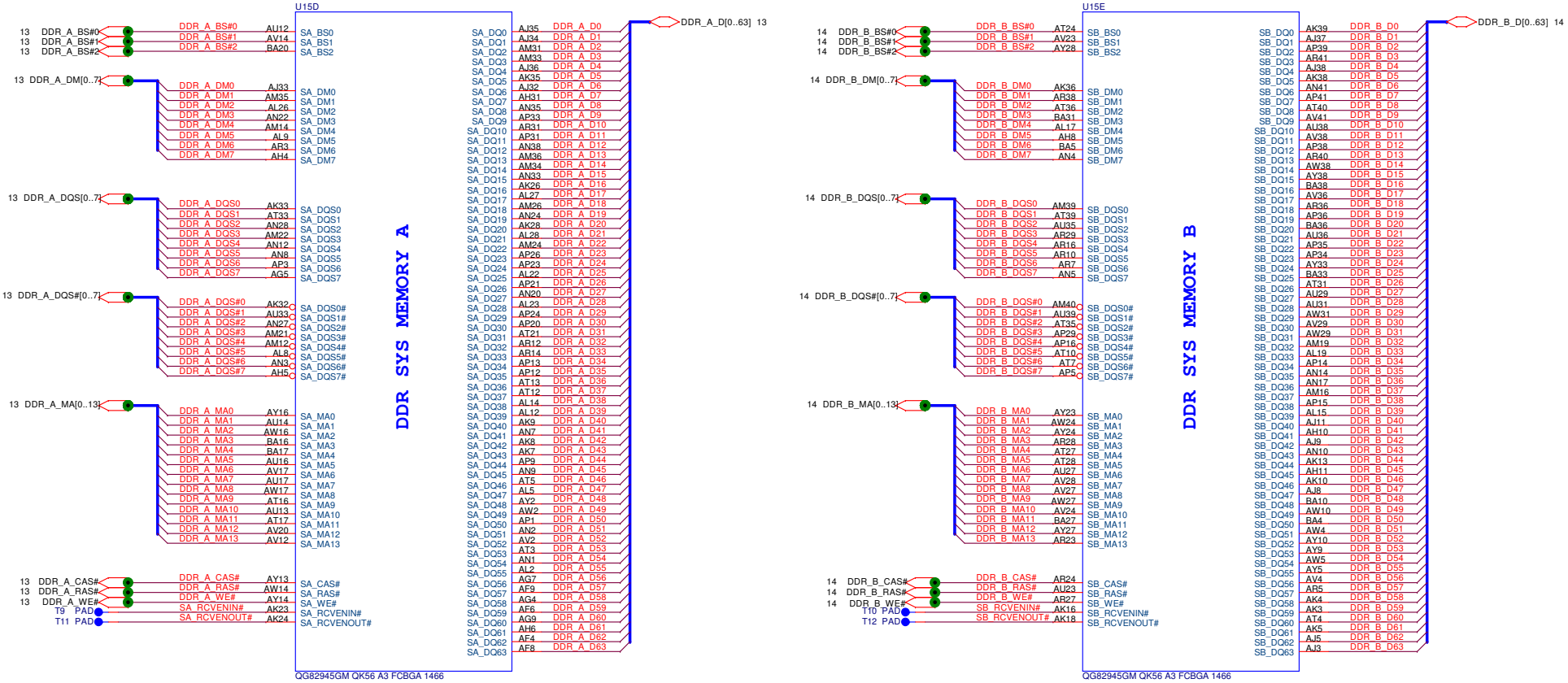

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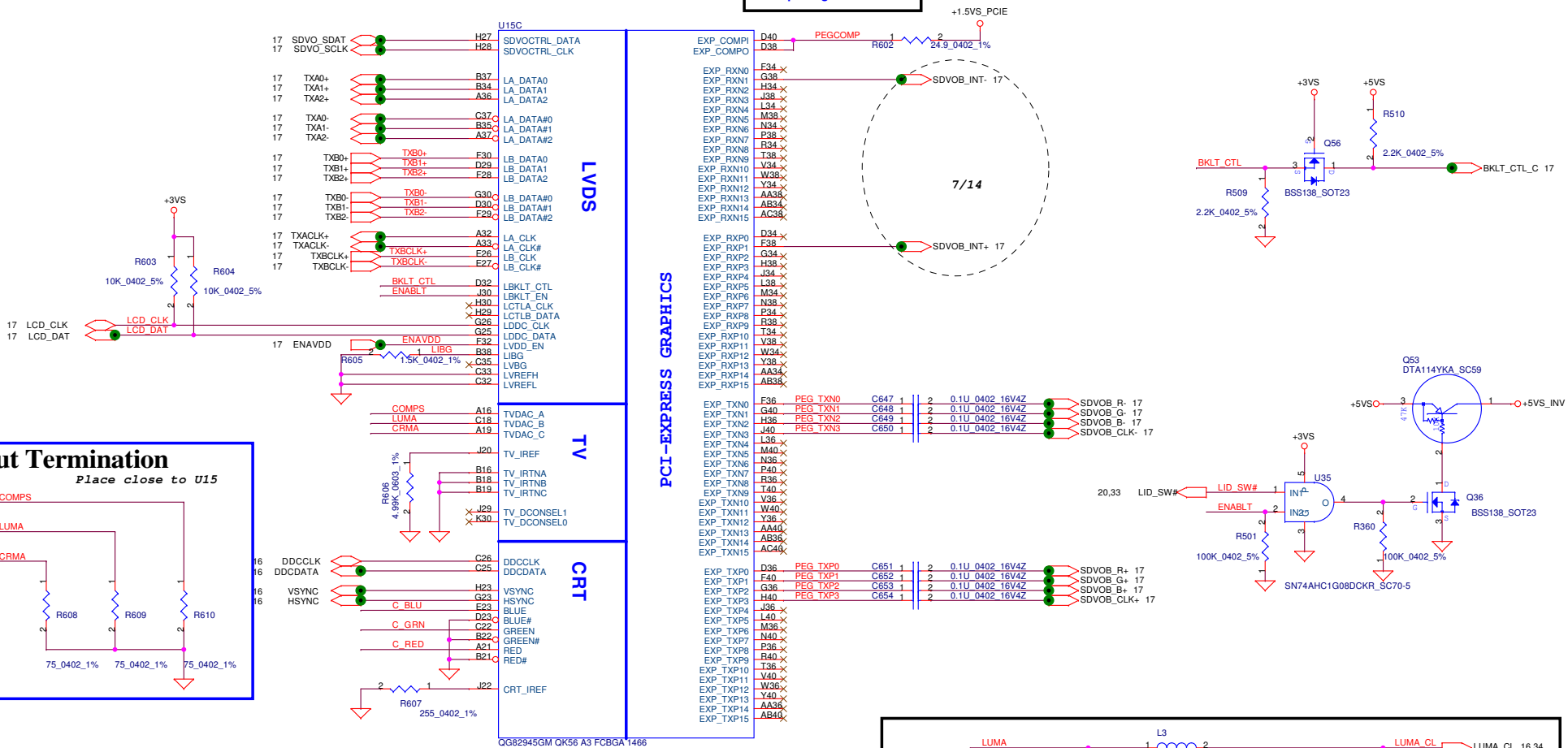
PEGCOMP trace width and spacing is 18/25 mils.

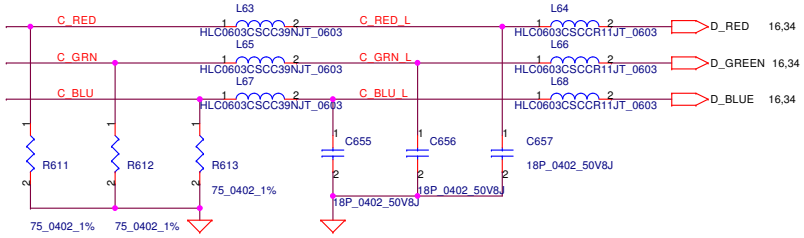


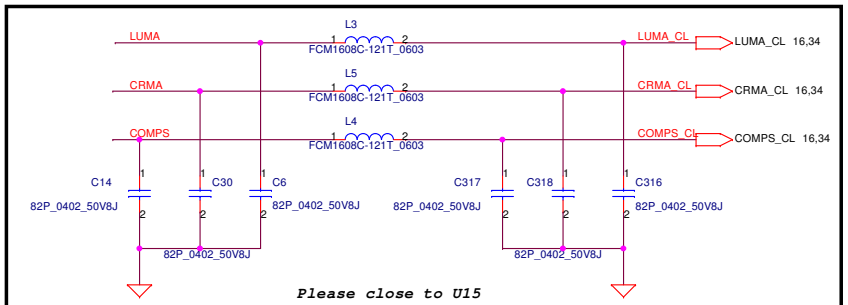
TV-Out Termination

Place close to U15

CRT Termination/EMI Filter

Place close to U15





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Title	Calistoga (3/6)		
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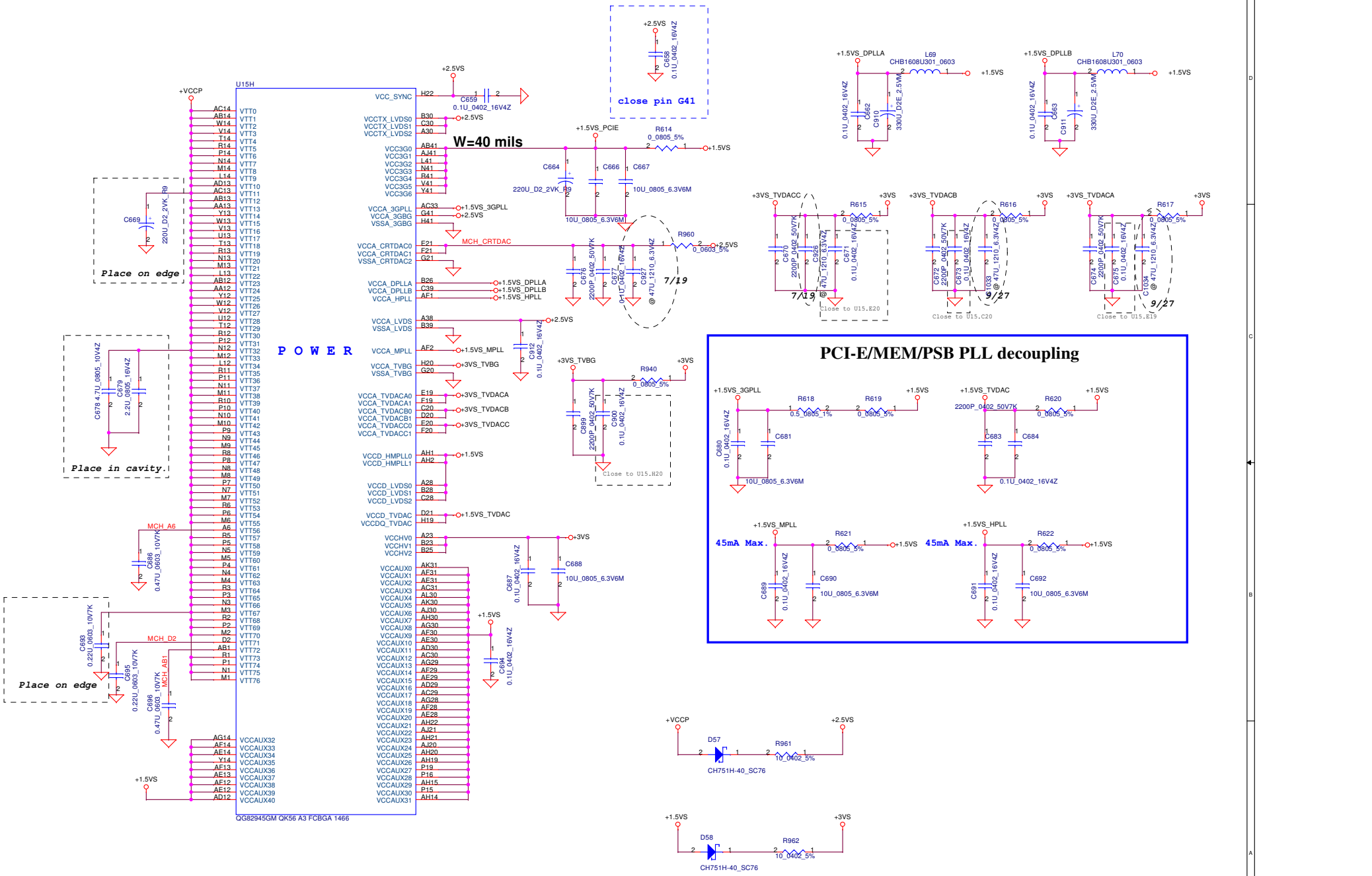

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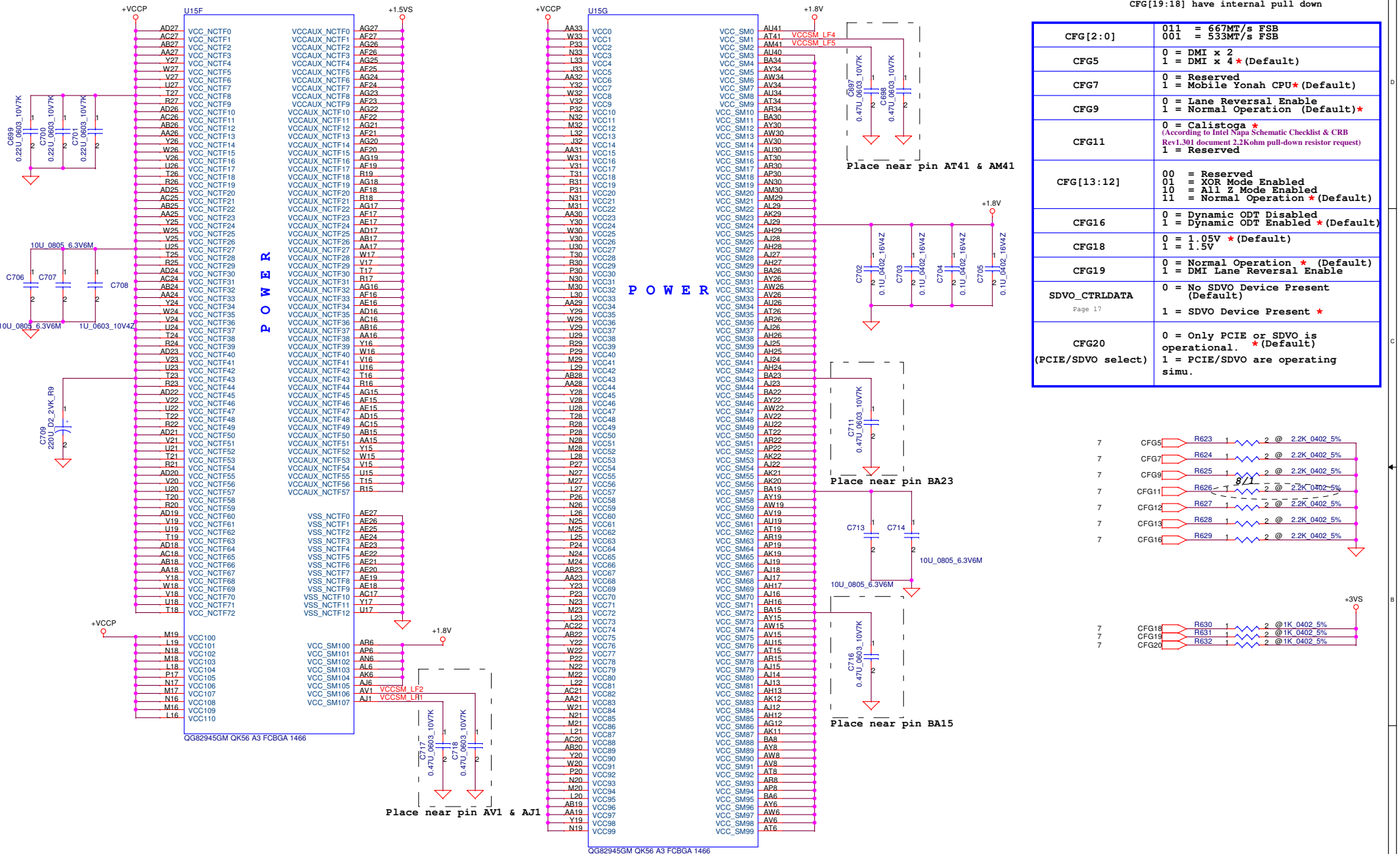
Strap Pin Table

CFG[3:17] have internal pull up

CFG[19:18] have internal pull down

CFG[2:0]	011 = 667MT/s FSB 001 = 533MT/s FSB
CFG5	0 = DMI x 2 1 = DMI x 4 ★(Default)
CFG7	0 = Reserved 1 = Mobile Yonah CPU★(Default)
CFG9	0 = Lane Reversal Enable 1 = Normal Operation (Default)★
CFG11	0 = Calistoga ★ (According to Intel Napa Schematic Checklist & CRB Rev1.301 document 2.2Kohm pull-down resistor request) 1 = Reserved
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation ★(Default)
CFG16	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled ★(Default)
CFG18	0 = 1.05V ★(Default) 1 = 1.5V
CFG19	0 = Normal Operation ★ (Default) 1 = DMI Lane Reversal Enable
SDVO_CTRLDATA Page 17	0 = No SDVO Device Present (Default) 1 = SDVO Device Present ★
CFG20 (PCIE/SDVO select)	0 = Only PCIE or SDVO is operational. ★(Default) 1 = PCIE/SDVO are operating simu.



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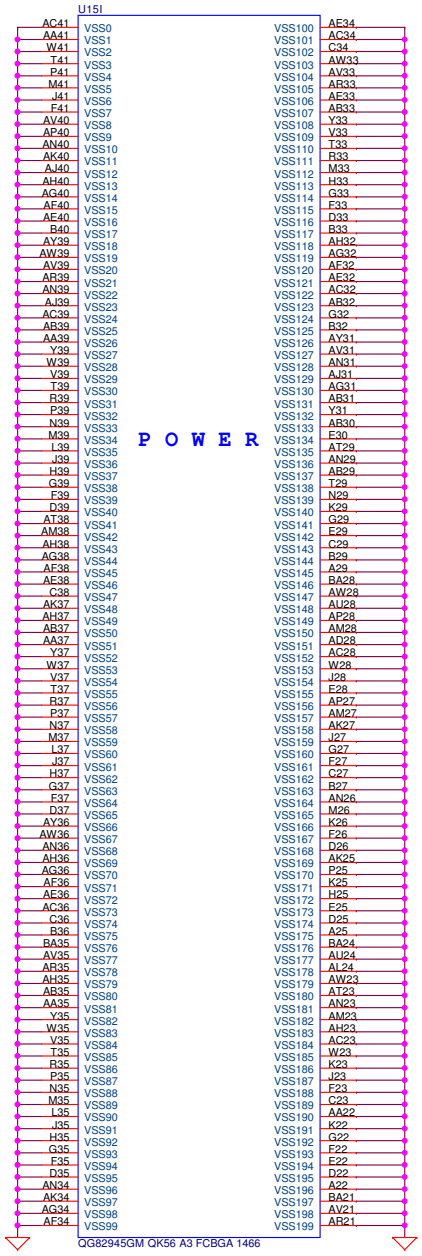

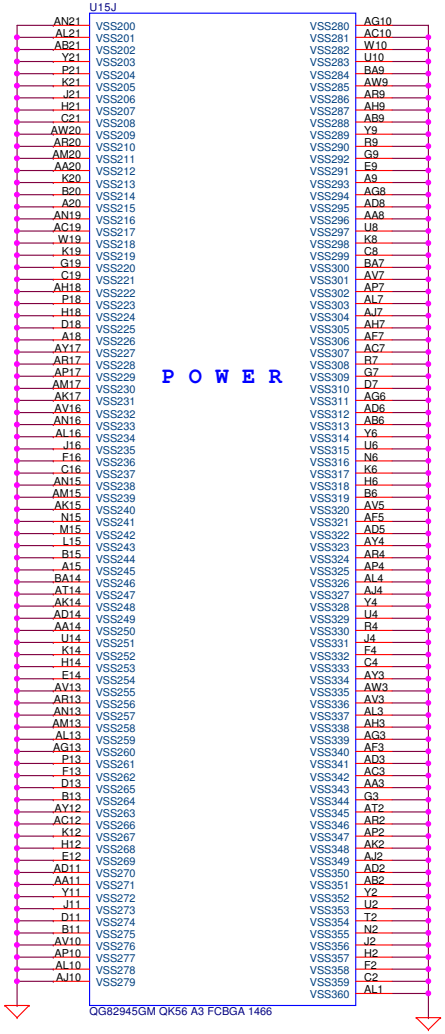

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Title: **Calistoga (6/6)**

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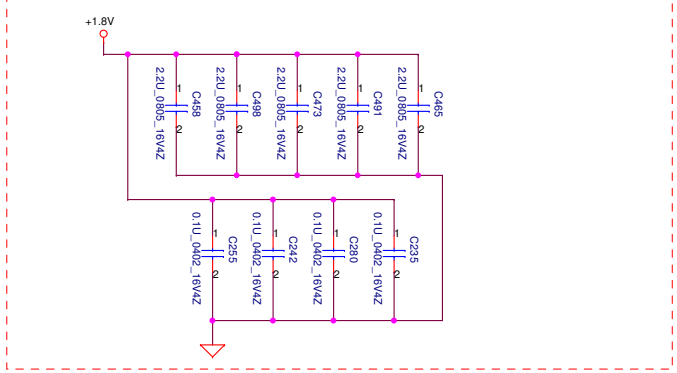
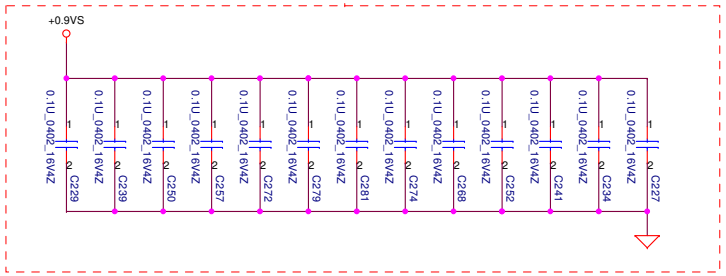
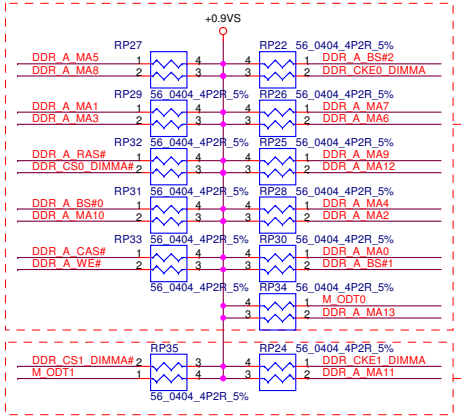
8 DDR_A_DQS#[0..7]
8 DDR_A_D[0..63]
8 DDR_A_DM[0..7]
8 DDR_A_DQS[0..7]
8 DDR_A_MA[0..13]

Layout Note:
Place near JP34



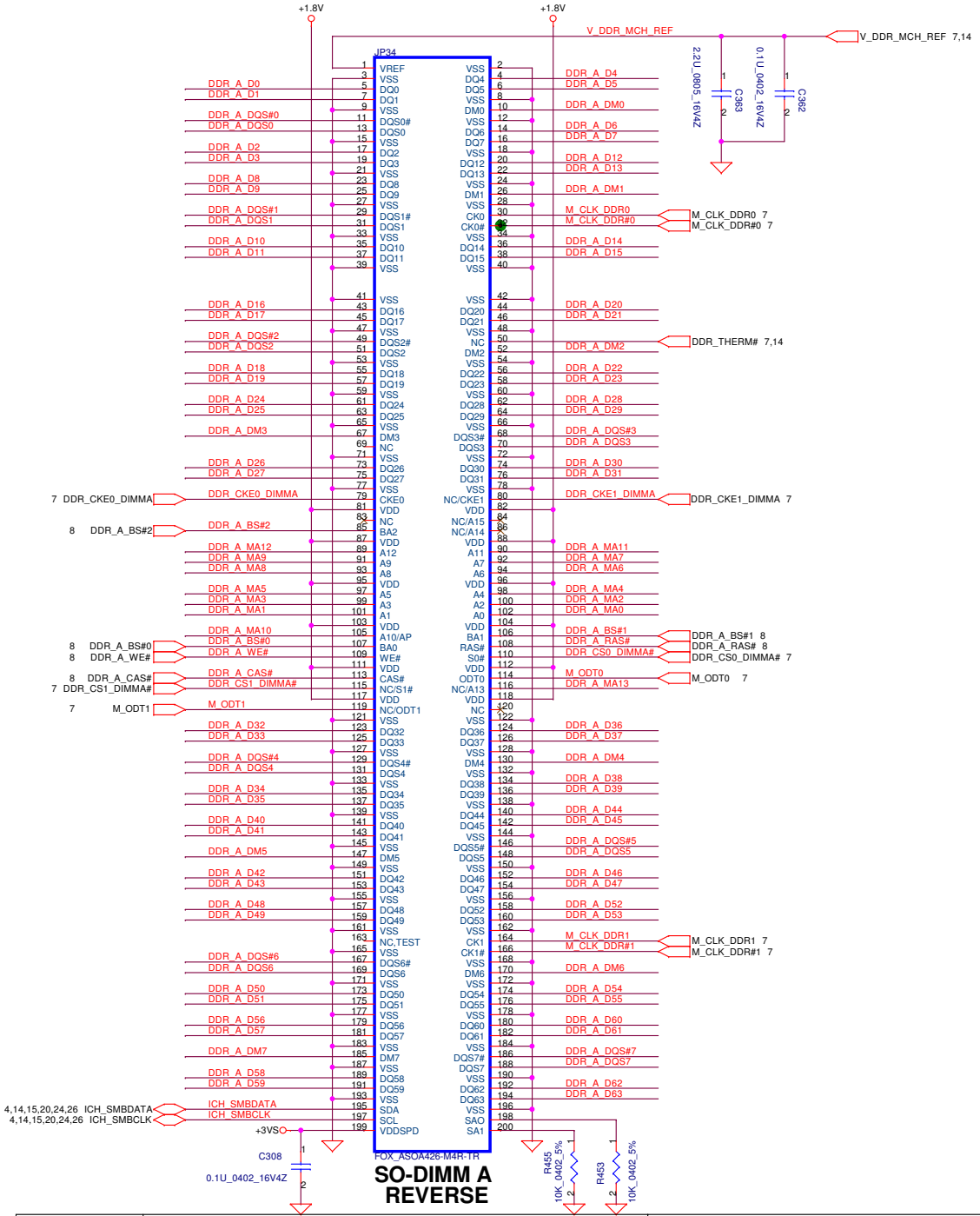
Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V_DDR_VTT





Layout Note:
Place these resistor closely JP34,all trace length<750 mil

Layout Note:
Place these resistor closely JP34,all trace length Max=1.3"



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Compal Electronics, Inc.

Title: **DDRII-SODIMM SLOT1**

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8 DDR_B_DQS#[0..7]
8 DDR_B_D[0..63]
8 DDR_B_DM[0..7]
8 DDR_B_DQS[0..7]
8 DDR_B_MA[0..13]

Layout Note:
Place near JP10

+1.8V

C236 2.2U_0805_16V4Z
C265 2.2U_0805_16V4Z
C247 2.2U_0805_16V4Z
C159 2.2U_0805_16V4Z
C164 2.2U_0805_16V4Z
C166 0.1U_0402_16V4Z
C219 0.1U_0402_16V4Z
C188 0.1U_0402_16V4Z
C161 0.1U_0402_16V4Z

Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V_DDR_VTT

+0.9VS

C176 C179 C186 C197 C213 C220 C183 C210 C199 C173 C218 C163 C177 0.1U_0402_16V4Z

+0.9VS

RP14 RP10 RP17 RP11 RP16 RP12 RP18 RP13 RP19 RP15 RP21 56_0404_4P2R_5%

DDR_B_MA1 DDR_B_MA3 DDR_B_MA9 DDR_B_MA12
DDR_B_BS#0 DDR_B_MA10 DDR_CKE3_DIMMB DDR_B_MA11
DDR_B_MA0 DDR_B_BS#1 DDR_B_MA5 DDR_B_MA8
DDR_B_RAS# DDR_CS2_DIMMB# DDR_B_MA7 DDR_B_MA6
DDR_B_CAS# DDR_B_WE# DDR_B_MA4 DDR_B_MA2
M_ODT2 DDR_B_MA13

Layout Note:
Place these resistor closely JP10,all trace length<750 mil

RP23 RP9 56_0404_4P2R_5%

DDR_CS3_DIMMB# M_ODT3 DDR_B_BS#2 DDR_CKE2_DIMMB

Layout Note:
Place these resistor closely JP10,all trace length Max=1.3"

+1.8V +1.8V V_DDR_MCH_REF

V_DDR_MCH_REF 7,13

C89 2.2U_0805_16V4Z C90 0.1U_0402_16V4Z

JP10 FOX_ASOA426-M2R-TR

DDR_B_D0	DDR_B_D1	DDR_B_D4	DDR_B_D5
DDR_B_DQS#0	DDR_B_DQS0	DDR_B_DM0	
DDR_B_D2	DDR_B_D3	DDR_B_D6	DDR_B_D7
DDR_B_D8	DDR_B_D9	DDR_B_D12	DDR_B_D13
DDR_B_DQS#1	DDR_B_DQS1	DDR_B_DM1	
DDR_B_D10	DDR_B_D11	M_CLK_DDR3	M_CLK_DDR#3
DDR_B_D16	DDR_B_D17	DDR_B_D14	DDR_B_D15
DDR_B_DQS#2	DDR_B_DQS2	DDR_B_D20	DDR_B_D21
DDR_B_D18	DDR_B_D19	DDR_B_DM2	
DDR_B_D24	DDR_B_D25	DDR_B_D22	DDR_B_D23
DDR_B_DM3		DDR_B_D28	DDR_B_D29
DDR_B_D26	DDR_B_D27	DDR_B_DQS#3	DDR_B_DQS3
DDR_CKE2_DIMMB		DDR_B_D30	DDR_B_D31
DDR_B_BS#2		DDR_CKE3_DIMMB	
DDR_B_MA12	DDR_B_MA9	DDR_B_MA11	DDR_B_MA7
DDR_B_MA8		DDR_B_MA6	
DDR_B_MA5	DDR_B_MA3	DDR_B_MA4	DDR_B_MA2
DDR_B_MA1		DDR_B_MA0	
DDR_B_MA10	DDR_B_BS#0	DDR_B_BS#1	DDR_B_RAS#
DDR_B_WE#		DDR_CS2_DIMMB#	
DDR_B_CAS#	DDR_CS3_DIMMB#	M_ODT2	DDR_B_MA13
M_ODT3		DDR_B_D32	DDR_B_D33
DDR_B_DQS#4	DDR_B_DQS4	DDR_B_D36	DDR_B_D37
DDR_B_D34	DDR_B_D35	DDR_B_DM4	
DDR_B_D40	DDR_B_D41	DDR_B_D38	DDR_B_D39
DDR_B_DM5		DDR_B_D44	DDR_B_D45
DDR_B_D42	DDR_B_D43	DDR_B_DQS#5	DDR_B_DQS5
DDR_B_D48	DDR_B_D49	DDR_B_D46	DDR_B_D47
DDR_B_DQS#6	DDR_B_DQS6	DDR_B_D52	DDR_B_D53
DDR_B_D50	DDR_B_D51	M_CLK_DDR2	M_CLK_DDR#2
DDR_B_D56	DDR_B_D57	DDR_B_DM6	
DDR_B_DM7		DDR_B_D54	DDR_B_D55
DDR_B_D58	DDR_B_D59	DDR_B_D60	DDR_B_D61
ICH_SMBDATA	ICH_SMBCLK	DDR_B_DQS#7	DDR_B_DQS7
+3VS		DDR_B_D62	DDR_B_D63

DDR_THERM# 7,13
DDR_CKE3_DIMMB 7
M_CLK_DDR3 7
M_CLK_DDR#3 7
M_CLK_DDR2 7
M_CLK_DDR#2 7
M_ODT2 7
DDR_B_BS#1 8
DDR_B_RAS# 8
DDR_CS2_DIMMB# 7

7 DDR_CKE2_DIMMB
8 DDR_B_BS#2
8 DDR_B_BS#0
8 DDR_B_WE#
8 DDR_B_CAS#
7 DDR_CS3_DIMMB#
7 M_ODT3
4,13,15,20,24,26 ICH_SMBDATA
4,13,15,20,24,26 ICH_SMBCLK

C301 0.1U_0402_16V4Z

R257 10K_0402_5% +3VS

R254 10K_0402_5%

SO-DIMM B REVERSE

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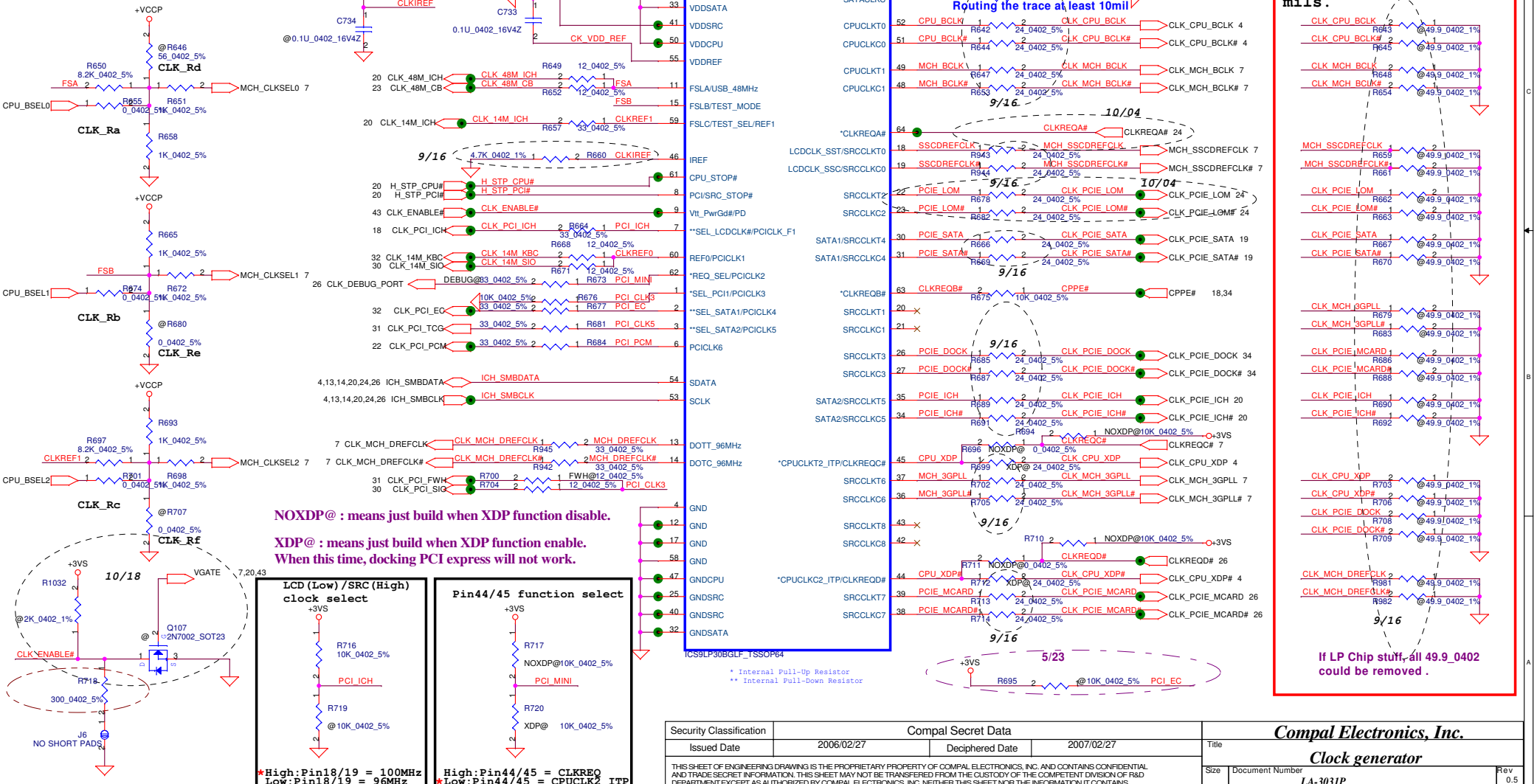
FSLC CLKSEL2	FSLB CLKSEL1	FSLA CLKSEL0	CPU MHz	SRC MHz	PCI MHz
0	0	1	133	100	33.3
0	1	1	166	100	33.3

Table : ICS954306

FSB Frequency Selet:

CPU Driven ★(Default)	Stuff	CLK_Ra CLK_Rb CLK_Rc
	No Stuff	CLK_Rd CLK_Re CLK_Rf
533MHz	Stuff	CLK_Rd CLK_Re CLK_Rf
	No Stuff	CLK_Ra CLK_Rb CLK_Rc
667MHz	Stuff	CLK_Rd CLK_Rf
	No Stuff	CLK_Ra CLK_Rb CLK_Rc CLK_Re



Security Classification	Compal Secret Data		
Issued Date	2006/02/27	Deciphered Date	2007/02/27

Compal Electronics, Inc.

Title: **Clock generator**

Size	Document Number	Rev
	LA-3031P	0.5

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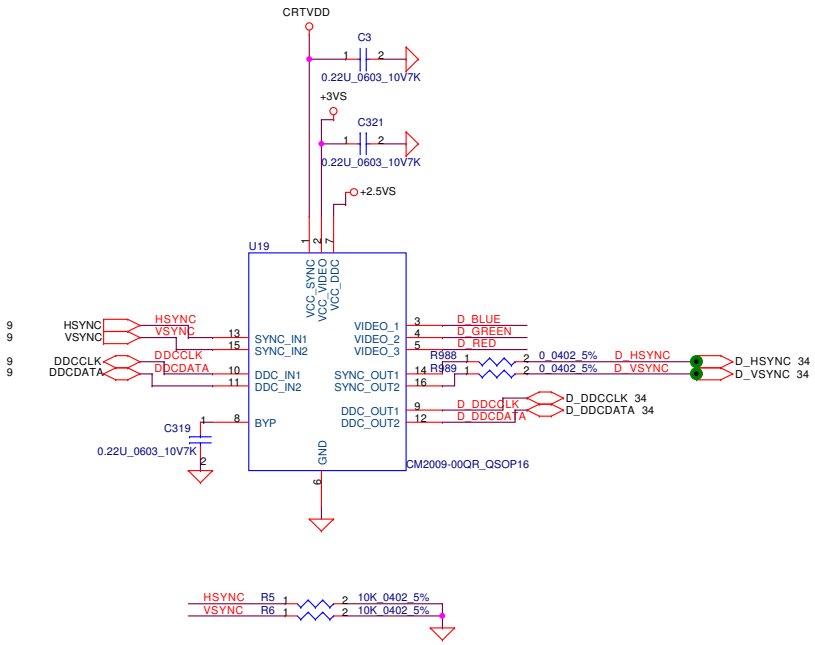
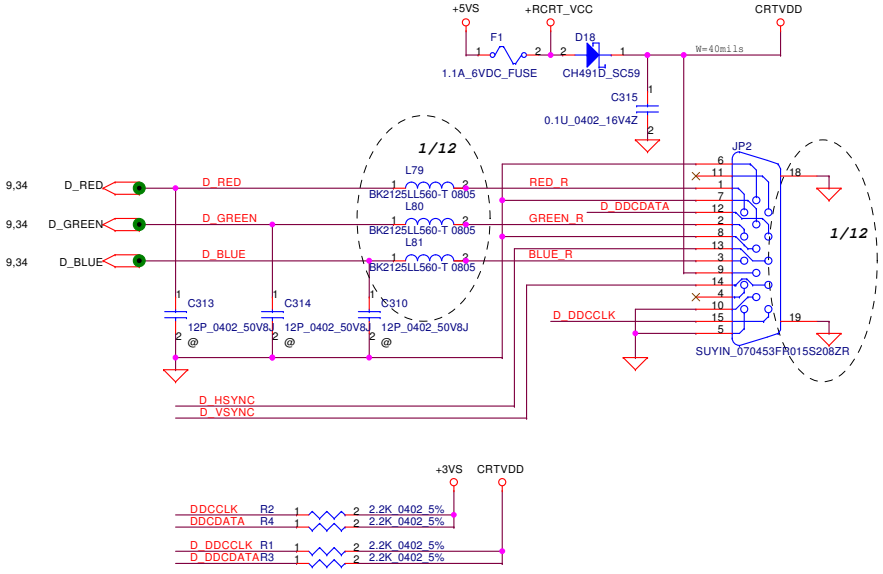
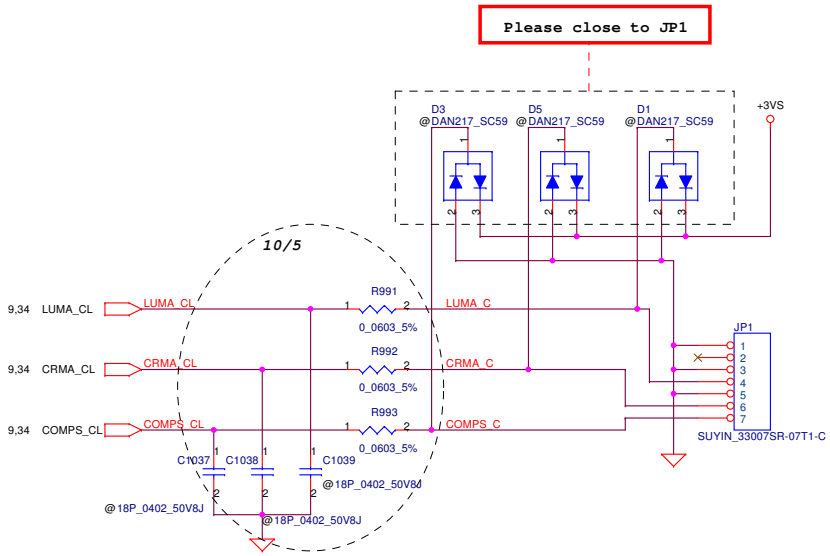
CRT Connector





TV-Out Connector



Security Classification	Compal Secret Data		
Issued Date	2006/02/27	Deciphered Date	2007/02/27

Compal Electronics, Inc.			
Title: CRT & TVout Connector			
Size	Document Number: LA-3031P		Rev: 0.5
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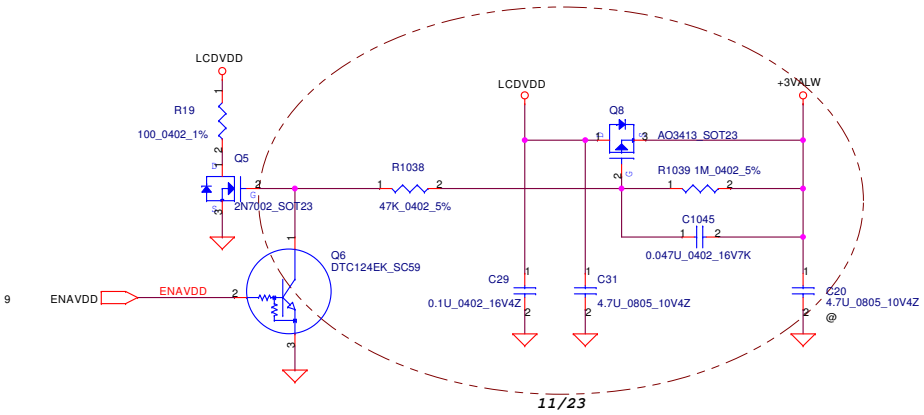
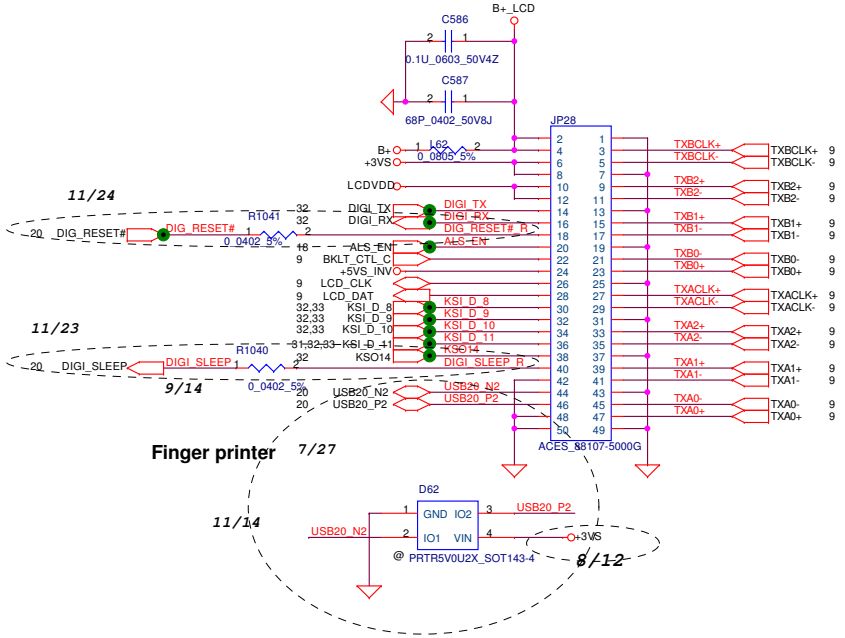
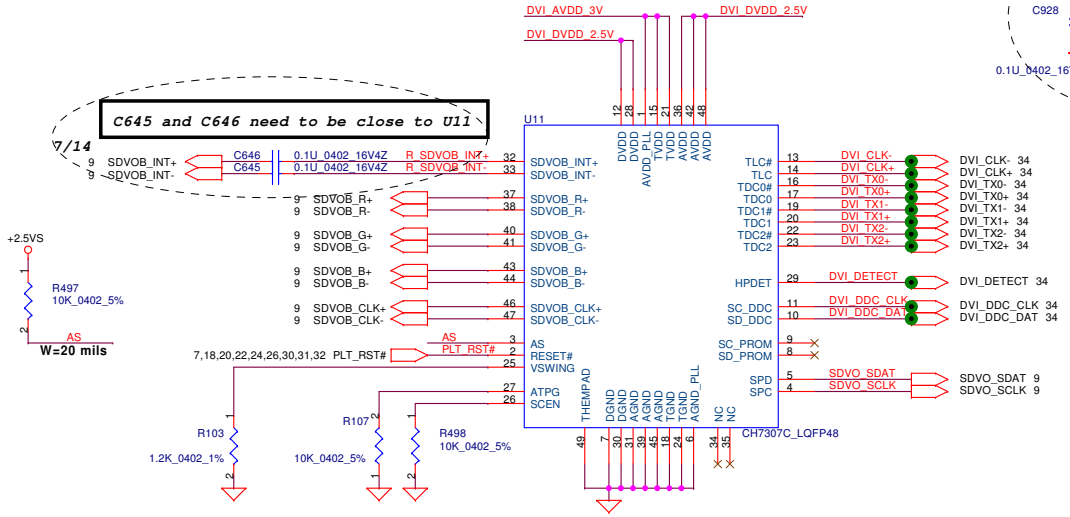
LCD POWER CIRCUIT

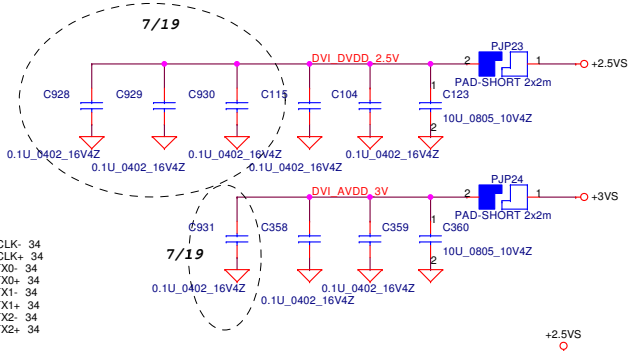


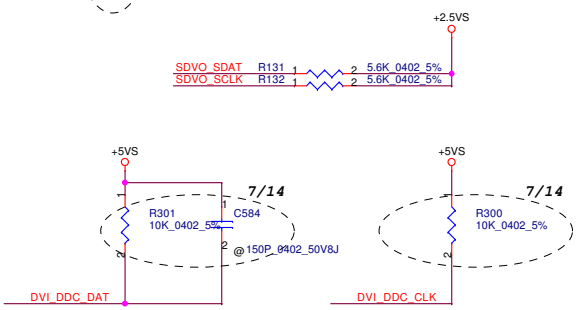
LCD/PANEL BD. CONN.



DVI CONTROLLER







Security Classification	Compal Secret Data		
Issued Date	2006/02/27	Deciphered Date	2007/02/27

Compal Electronics, Inc.			
Title	DVI (CH7307)/LCD CONN.		
Size	Document Number		Rev
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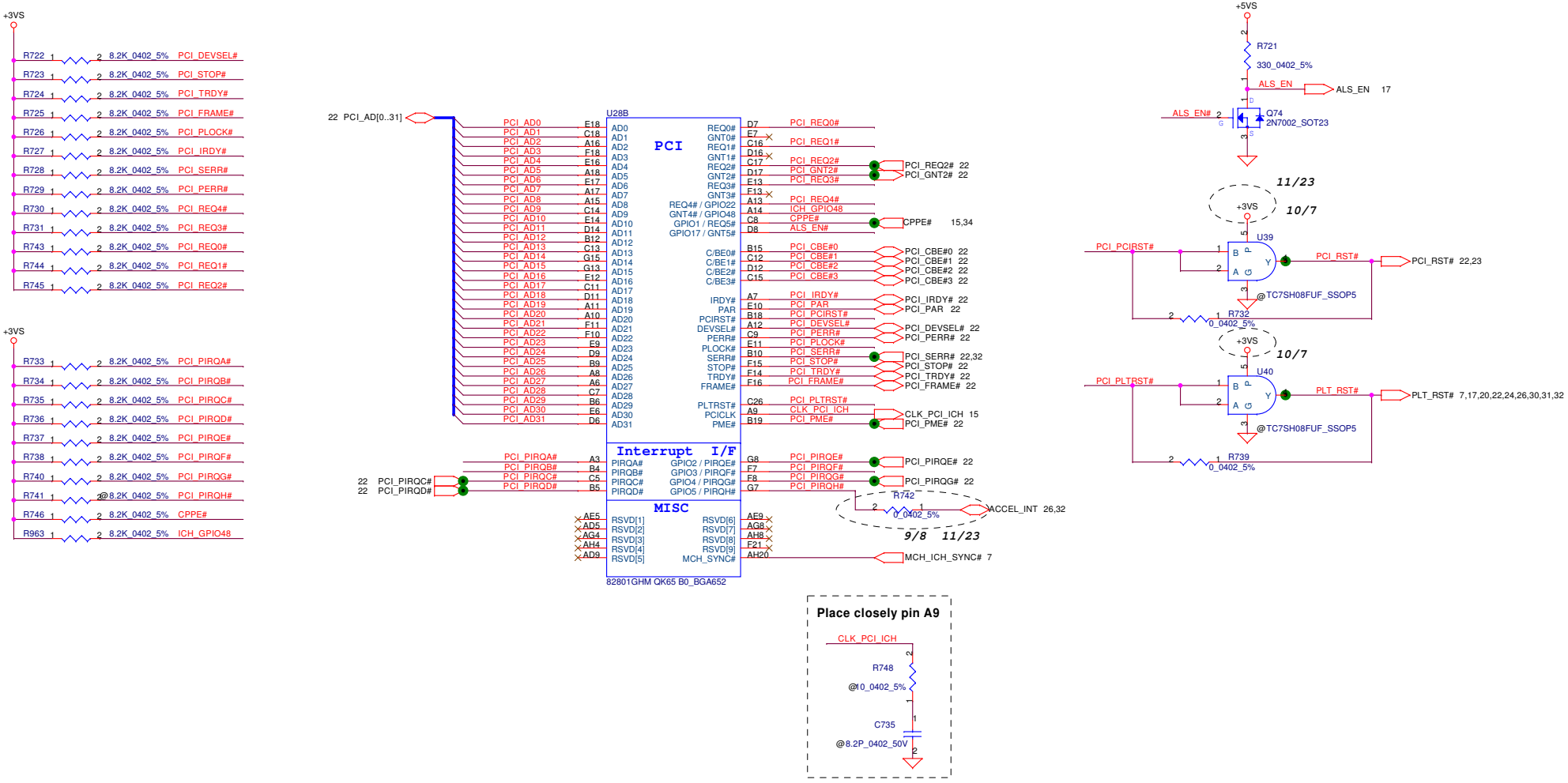


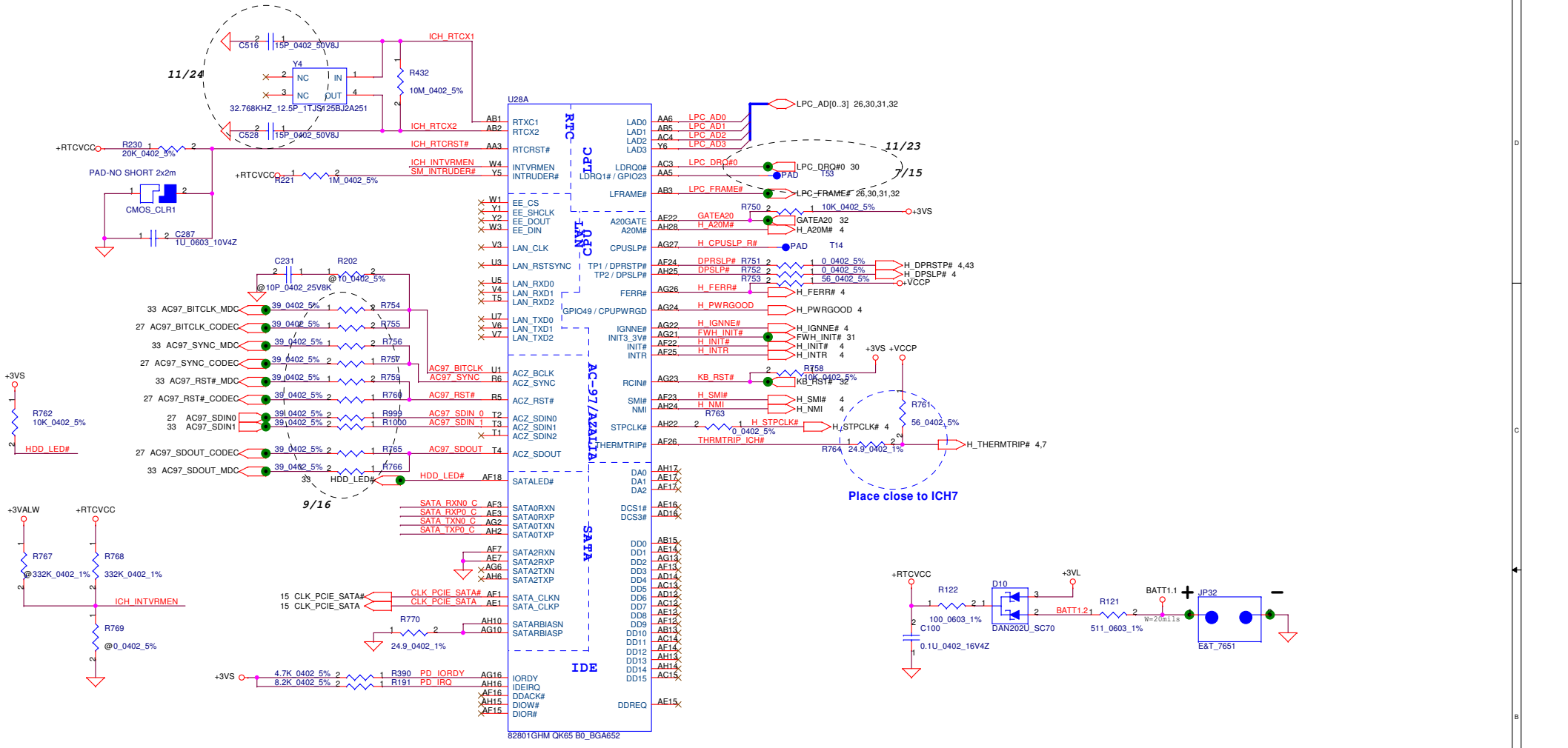
Security Classification	Compal Secret Data
Issued Date	2006/02/27
Deciphered Date	2007/02/27

Compal Electronics, Inc.

Title: **ICH7-M(1/4)**

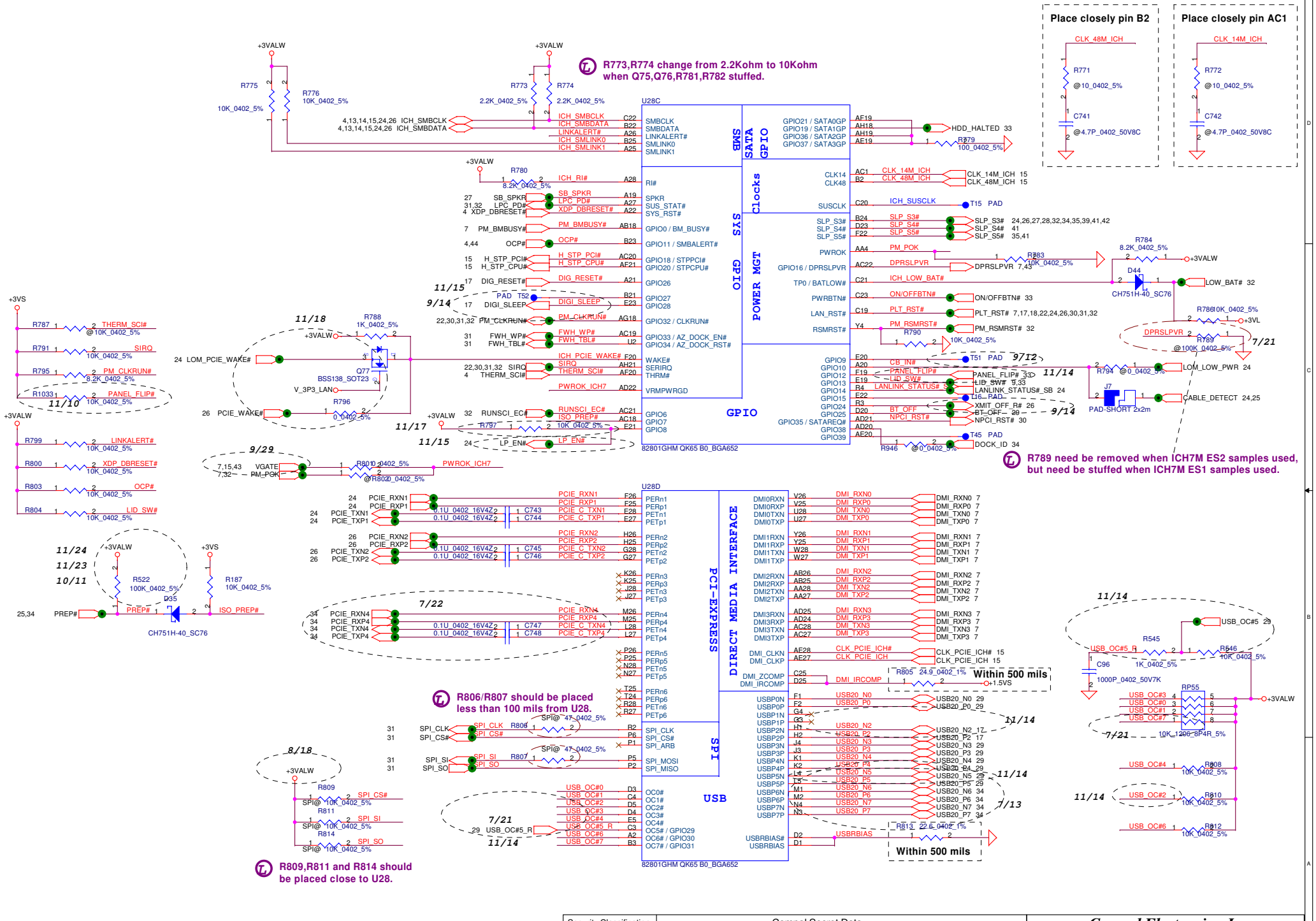
Size	Document Number	Rev
	LA-3031P	0.5

Date: Tuesday, February 28, 2006 | Sheet 18 of 49



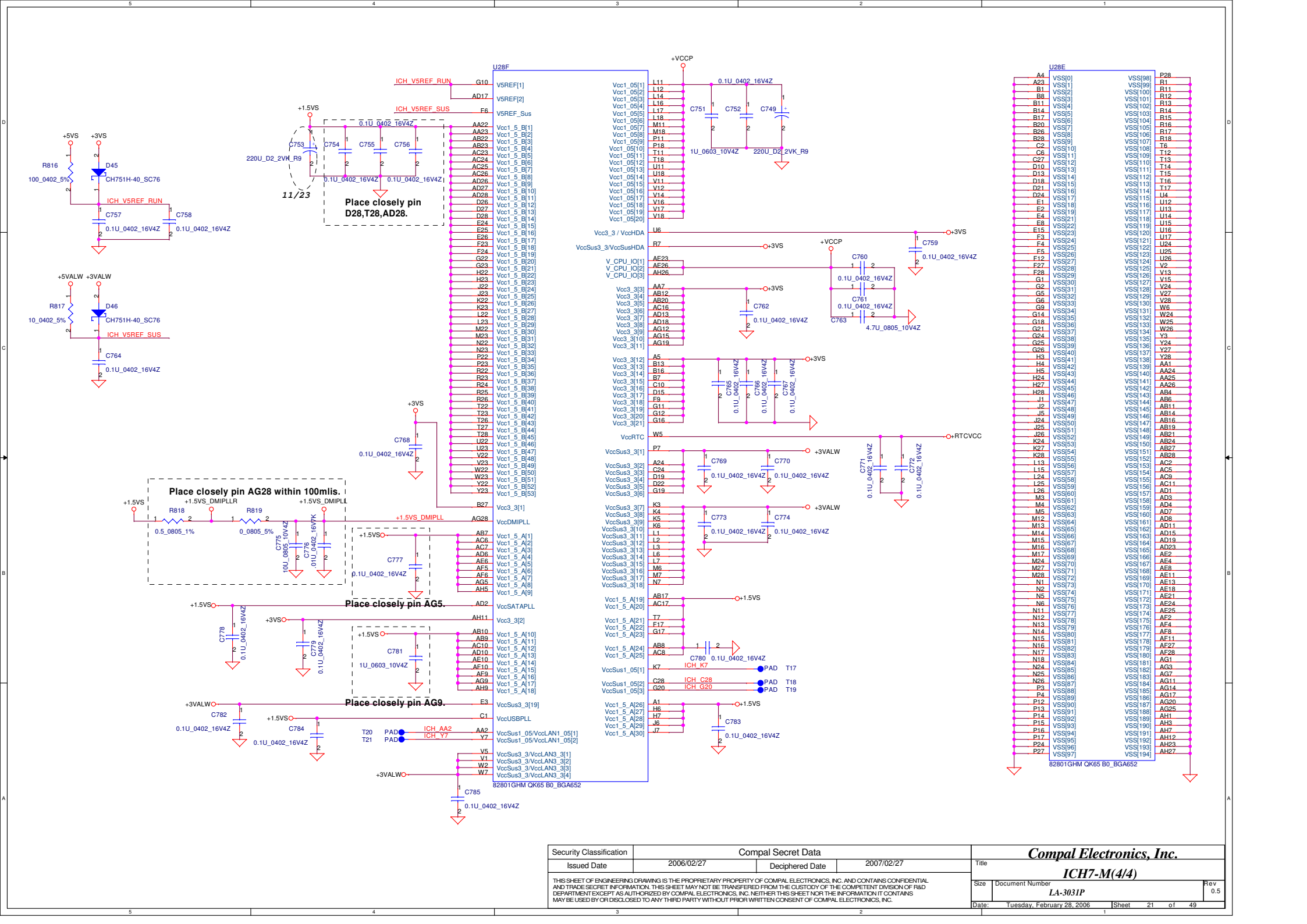
Security Classification	Compal Secret Data		
Issued Date	2006/02/27	Deciphered Date	2007/02/27

Compal Electronics, Inc.			
Title	ICH7-M(2/4)		
Size	Document Number LA-3031P		Rev 0.5
Date: Tuesday, February 28, 2006	Sheet 19 of 49		



Security Classification	Compal Secret Data		
Issued Date	2006/02/27	Deciphered Date	2007/02/27

Compal Electronics, Inc.			
Title: ICH7-M(3/4)			
Size	Document Number: LA-3031P		Rev: 0.5
Date: Tuesday, February 28, 2006	Sheet 20 of 49		



Security Classification	Compal Secret Data		
Issued Date	2006/02/27	Deciphered Date	2007/02/27

Compal Electronics, Inc.

Title: **ICH7-M(4/4)**

Size	Document Number	Rev
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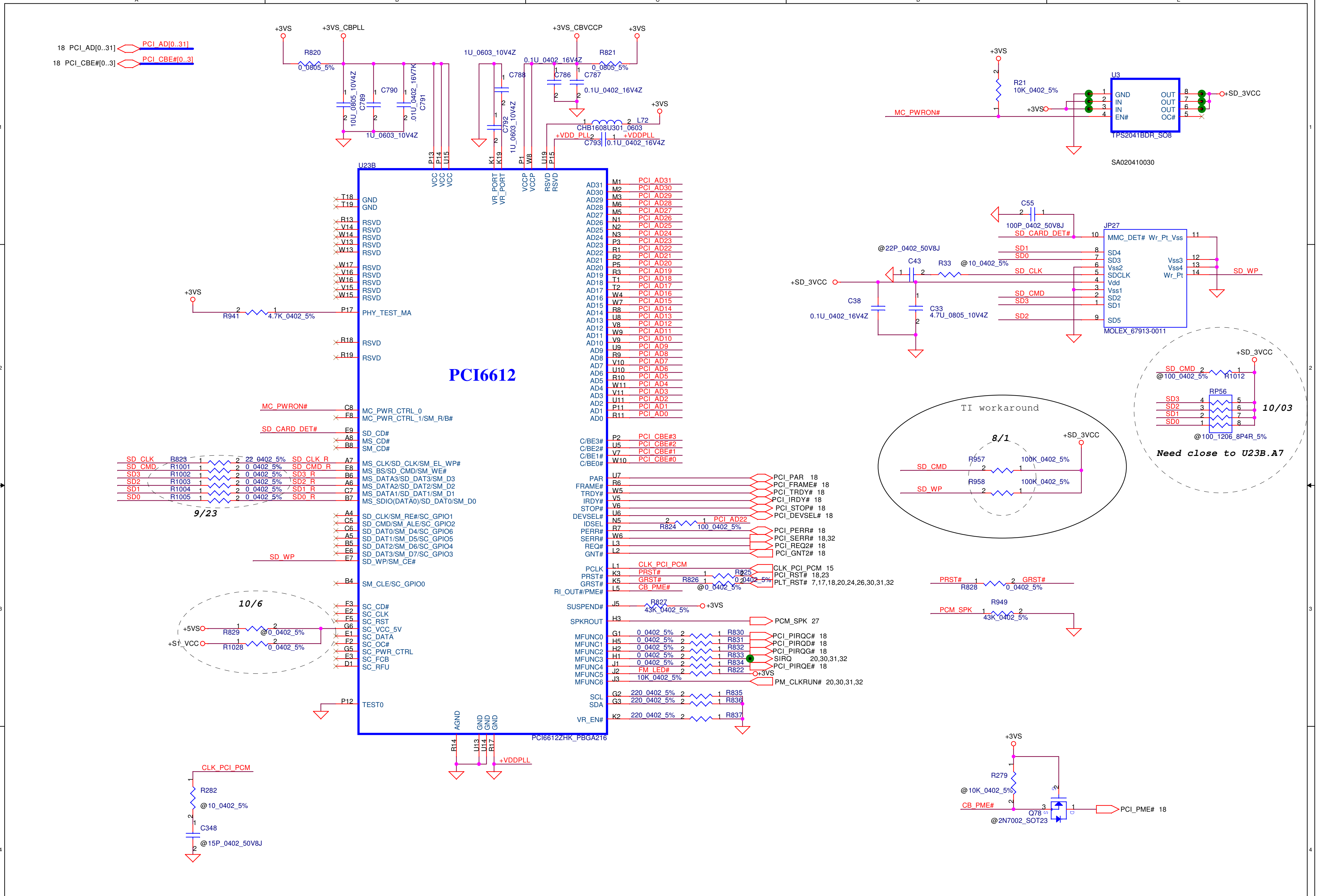
Date: Tuesday, February 28, 2006 | Sheet 21 of 49



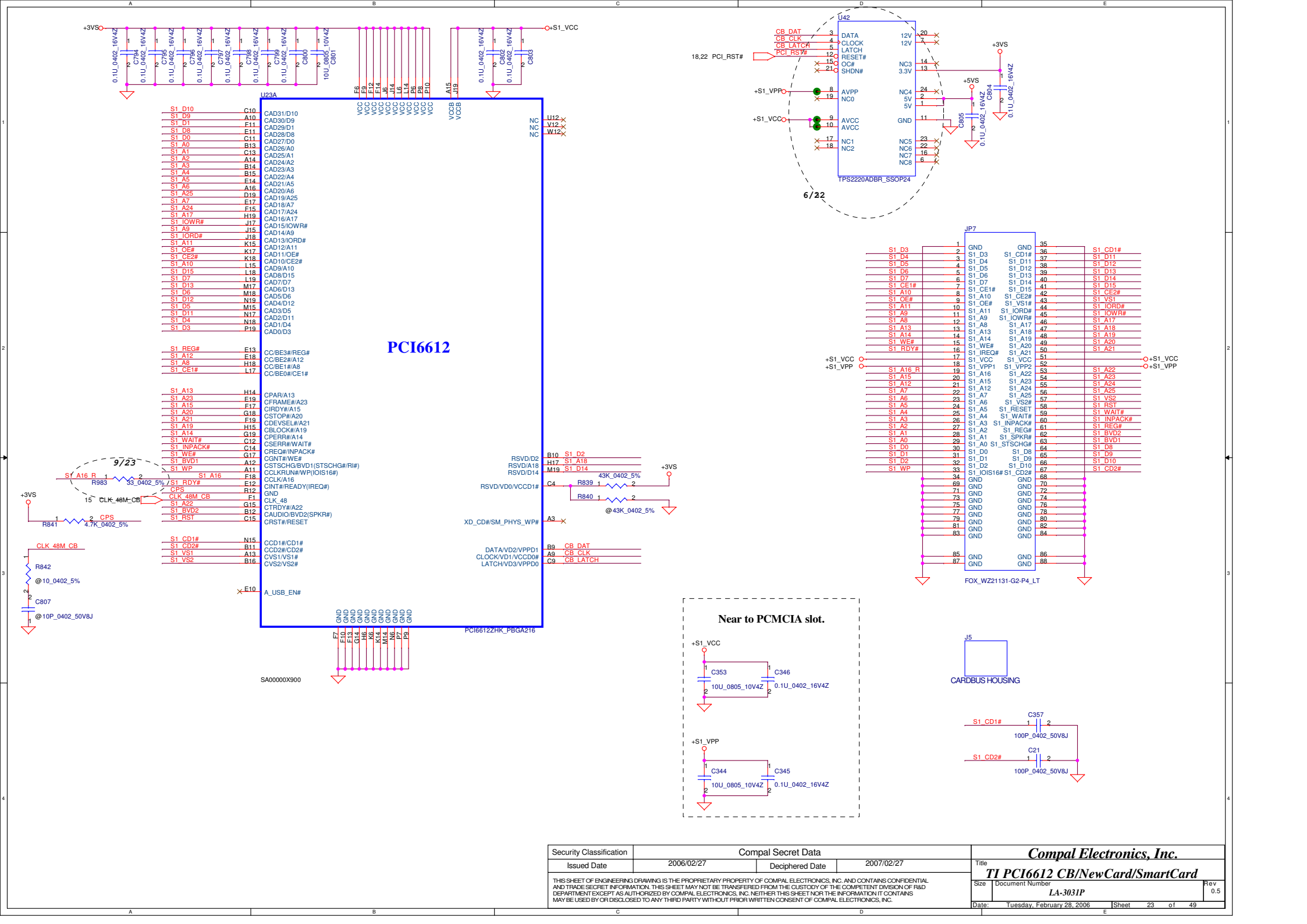
Security Classification	Compal Secret Data		
Issued Date	2006/02/27	Deciphered Date	2007/02/27

Compal Electronics, Inc.

Title: **TI PCI6612 PCI/CardReader**

Size | Document Number: LA-3031P | Rev 0.5

Date: Tuesday, February 28, 2006 |


PCI6612
U23A
PCI6612ZHK_PBGA216
SA00000X900
U42
TPS2220ADBR_SSOP24
6/22
JP7
FOX_WZ21131-G2-P4_LT
9/23
Near to PCMCIA slot.
CARDBUS HOUSING
Compal Secret Data
Issued Date 2006/02/27
Deciphered Date 2007/02/27
Compal Electronics, Inc.
TI PCI6612 CB/NewCard/SmartCard
LA-3031P
Rev 0.5
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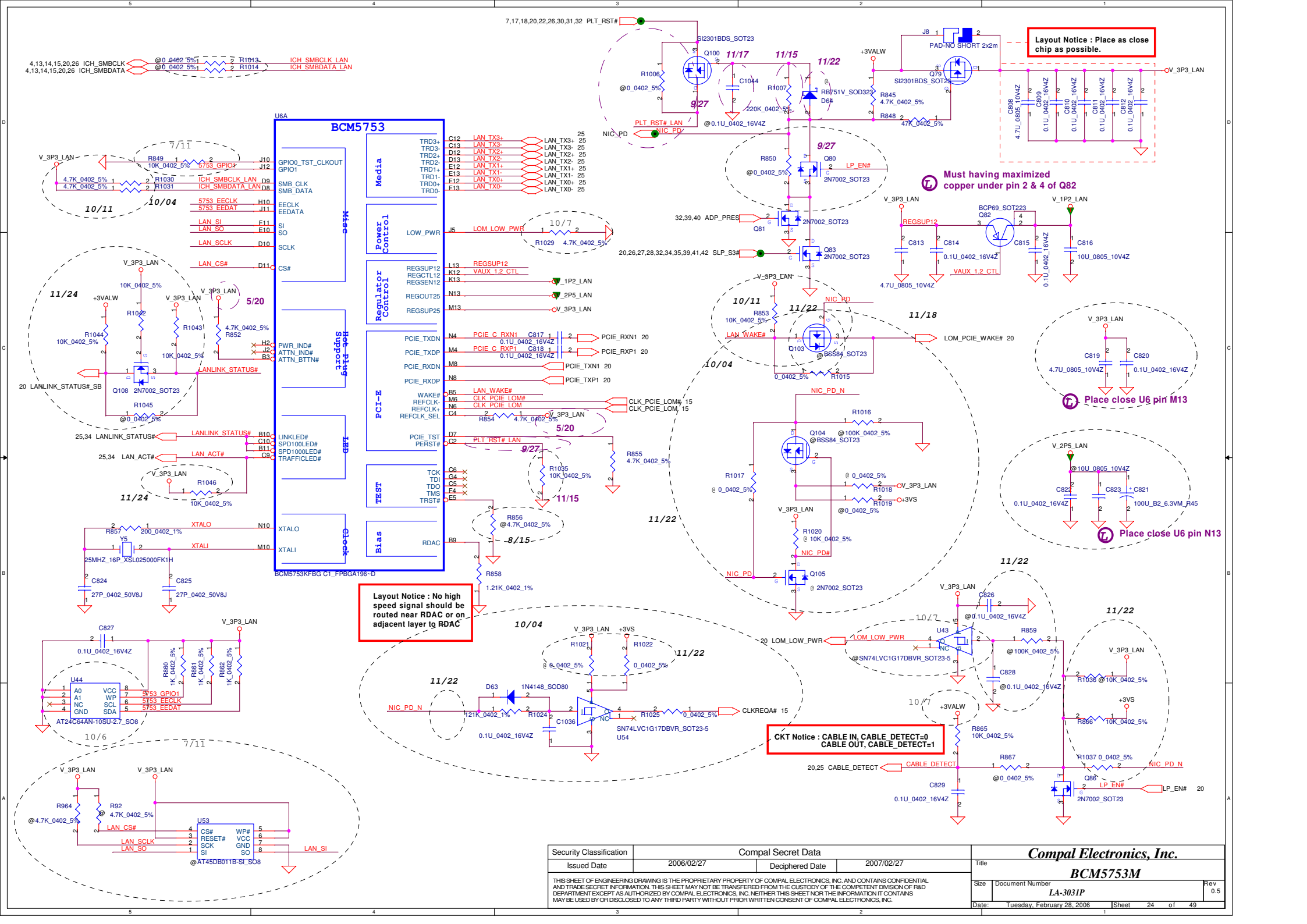
BCM5753
U6A
BCM5753KFBG C1_FPBGA196~D
Layout Notice : Place as close chip as possible.
Must having maximized copper under pin 2 & 4 of Q82
Place close U6 pin M13
Place close U6 pin N13
Layout Notice : No high speed signal should be routed near RDAC or on adjacent layer to RDAC
CKT Notice : CABLE IN, CABLE_DETECT=0
CABLE OUT, CABLE_DETECT=1
Media
Power Control
Regulator Control
PCI-E
Host Bus Support
LED
TEST
Bias
Clock
Misc
Q100 SI2301BDS_SOT23
Q79 SI2301BDS_SOT23
Q80 2N7002_SOT23
Q81 2N7002_SOT23
Q83 2N7002_SOT23
Q108 2N7002_SOT23
Q103 @BSS84_SOT23
Q104 @BSS84_SOT23
Q105 @ 2N7002_SOT23
Q86 2N7002_SOT23
D64 RB751V_SOD323
D63 1N4148_SOD80
U44 AT24C64AN-10SU-2.7_SO8
U53 @AT45DB011B-SI_SO8
U43 @SN74LVC1G17DBVR_SOT23-5
U54 SN74LVC1G17DBVR_SOT23-5
Y5 25MHZ_16P_XSL025000FK1H
J8 PAD-NO SHORT 2x2m
BCP69_SOT223 Q82
V_3P3_LAN
V_1P2_LAN
V_2P5_LAN
+3VALW
+3VS
NIC_PD
NIC_PD_N
PLT_RST#_LAN
LAN_WAKE#
LOM_PCIE_WAKE# 20
LOM_LOW_PWR 20
CABLE_DETECT 20,25
LP_EN# 20
LANLINK_STATUS# 20
CLKREQA# 15
ADP_PRES 32,39,40
SLP_S3# 20,26,27,28,32,34,35,39,41,42
PCIE_RXN1 20
PCIE_RXP1 20
PCIE_TXN1 20
PCIE_TXP1 20
CLK_PCIE_LOM# 15
CLK_PCIE_LOM 15
LAN_TX3+ 25
LAN_TX3- 25
LAN_TX2+ 25
LAN_TX2- 25
LAN_TX1+ 25
LAN_TX1- 25
LAN_TX0+ 25
LAN_TX0- 25
REGSUP12
VAUX_1.2_CTL
LOM_LOW_PWR
PLT_RST# 7,17,18,20,22,26,30,31,32
ICH_SMBCLK 4,13,14,15,20,26
ICH_SMBDATA 4,13,14,15,20,26
ICH_SMBCLK_LAN
ICH_SMBDATA_LAN
LANLINK_STATUS# 25,34
LAN_ACT# 25,34
5753_GPIO1
5753_EECLK
5753_EEDAT
LAN_SI
LAN_SO
LAN_SCLK
LAN_CS#
PWR_IND#
ATTN_IND#
ATTN_BTTN#
LINKLED#
SPD100LED#
SPD1000LED#
TRAFFICLED#
XTALO
XTALI
Security Classification
Compal Secret Data
Issued Date
2006/02/27
Deciphered Date
2007/02/27
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Compal Electronics, Inc.
Title
BCM5753M
Size
Document Number
LA-3031P
Rev
0.5
Date: Tuesday, February 28, 2006
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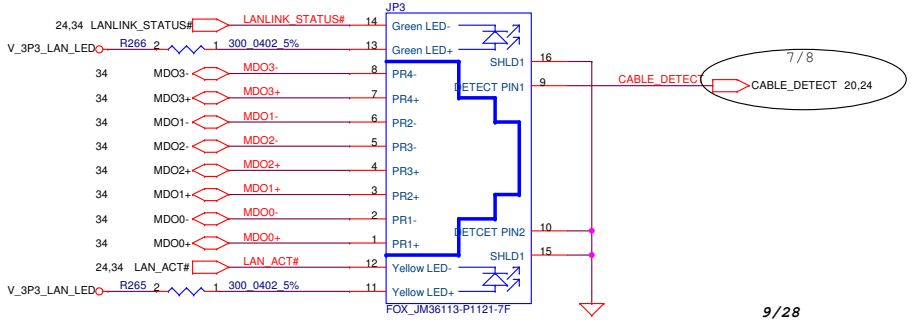
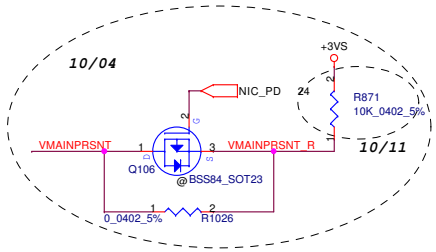
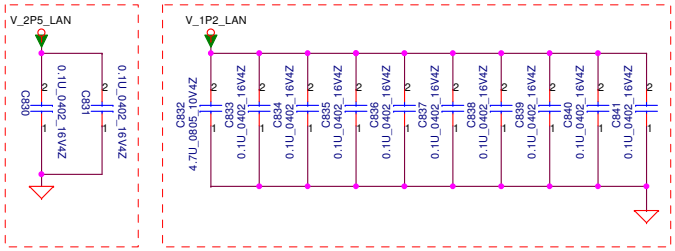
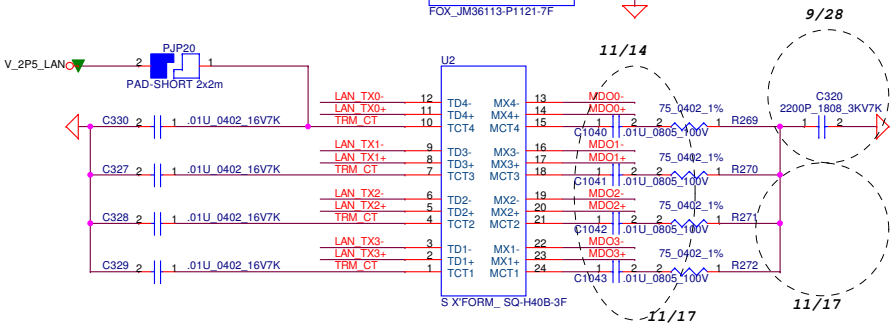
RJ-45 CONN.



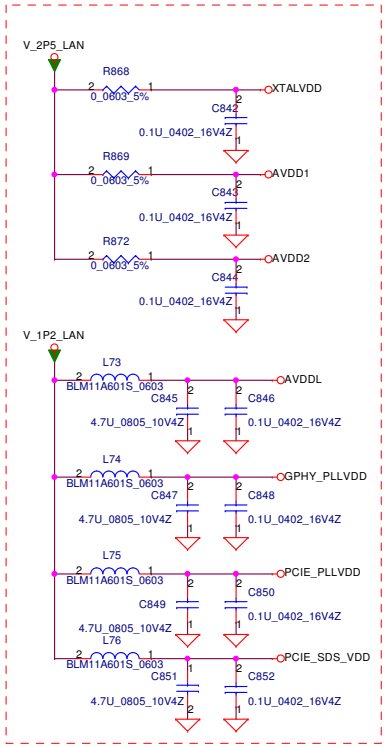


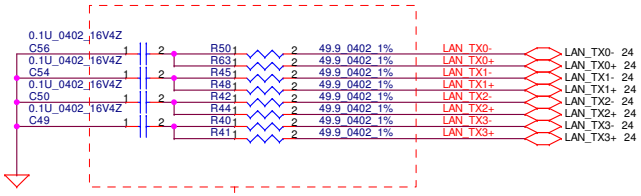
Layout Notice : 1.2V filter. Place as close chip as possible.



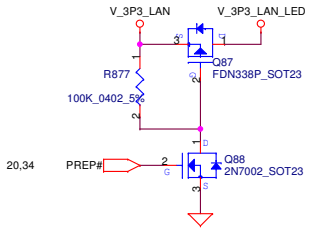


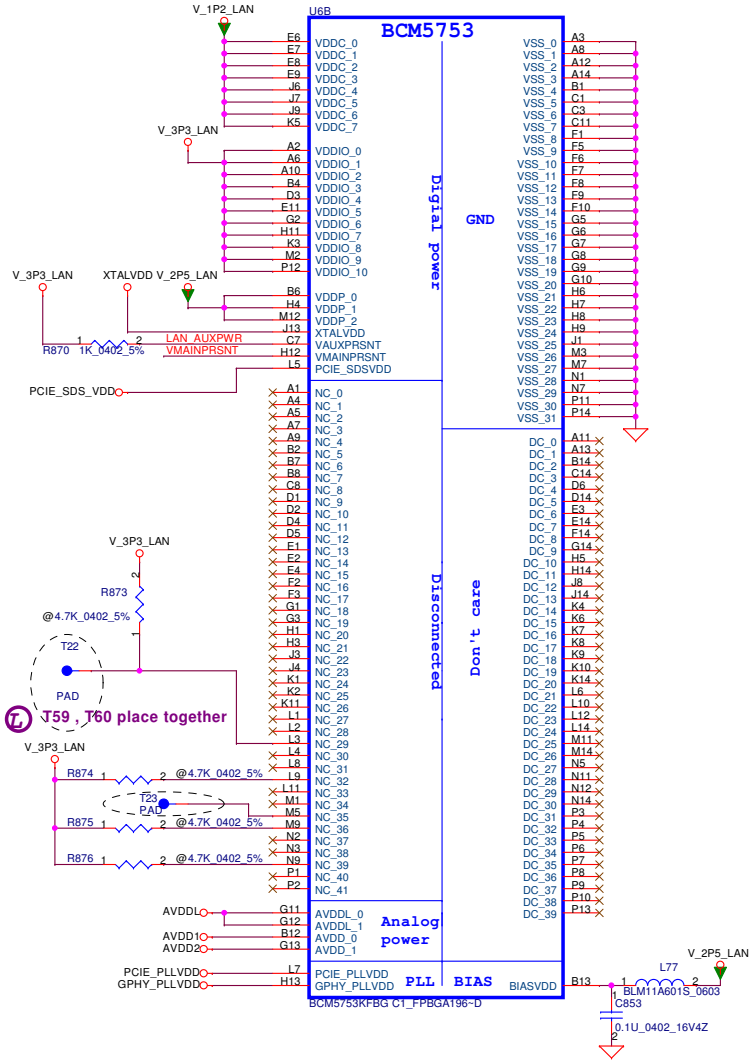
Layout Notice : Filter place as close chip as possible.





Layout Notice : Place termination as close as BCM5753M as possible





Security Classification	Compal Secret Data		
Issued Date	2006/02/27	Deciphered Date	2007/02/27

Compal Electronics, Inc.

Title: **Magnetic & RJ45/RJ11**

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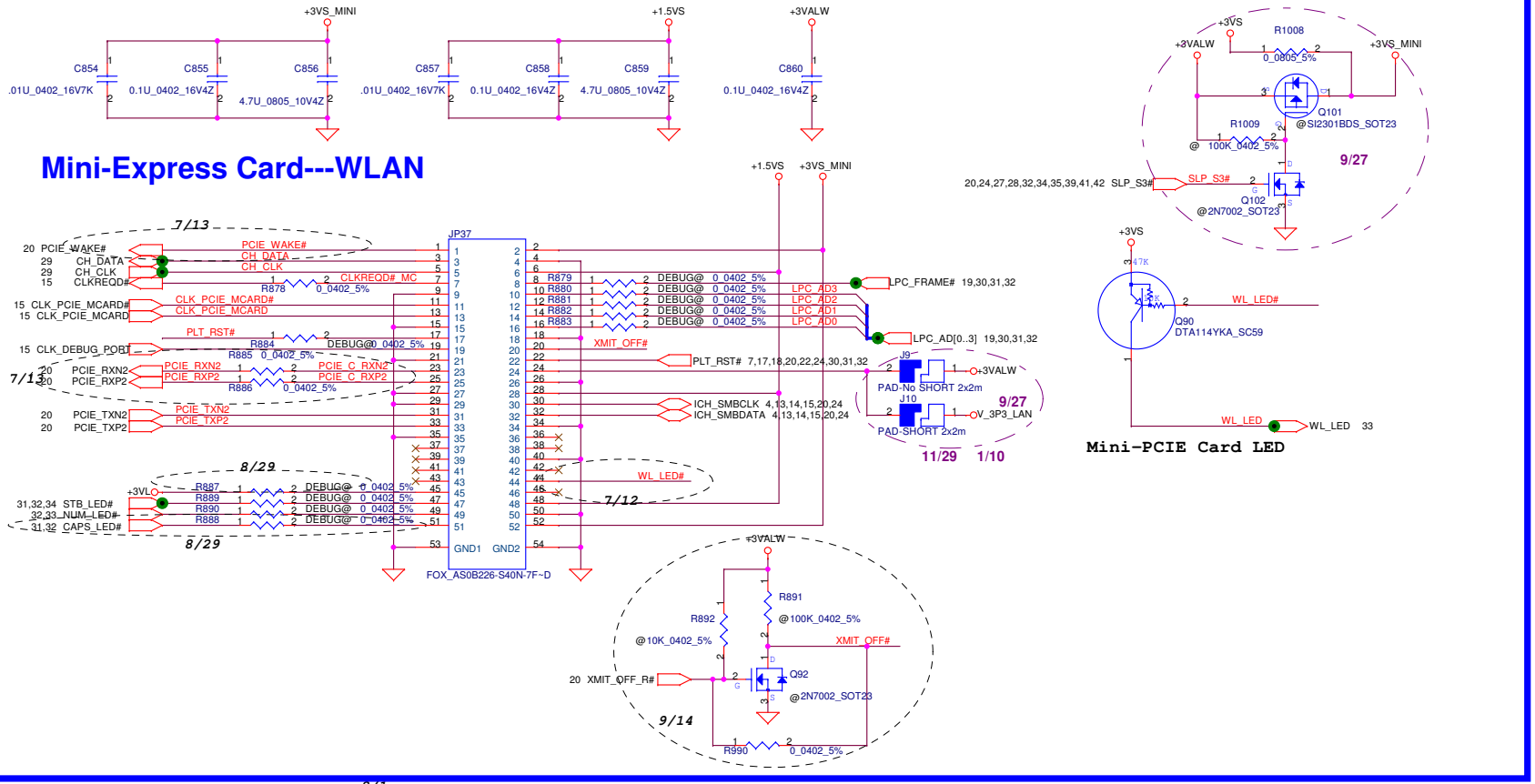
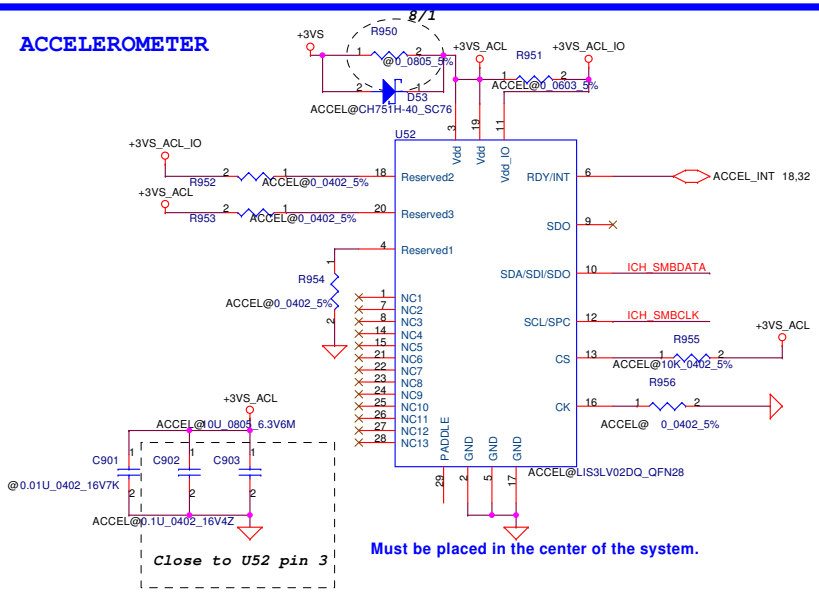


ACCELEROMETER



Security Classification	Compal Secret Data		
Issued Date	2006/02/27	Deciphered Date	2007/02/27

Compal Electronics, Inc.

Title: **Mini-Card/ACCELEROMETER**

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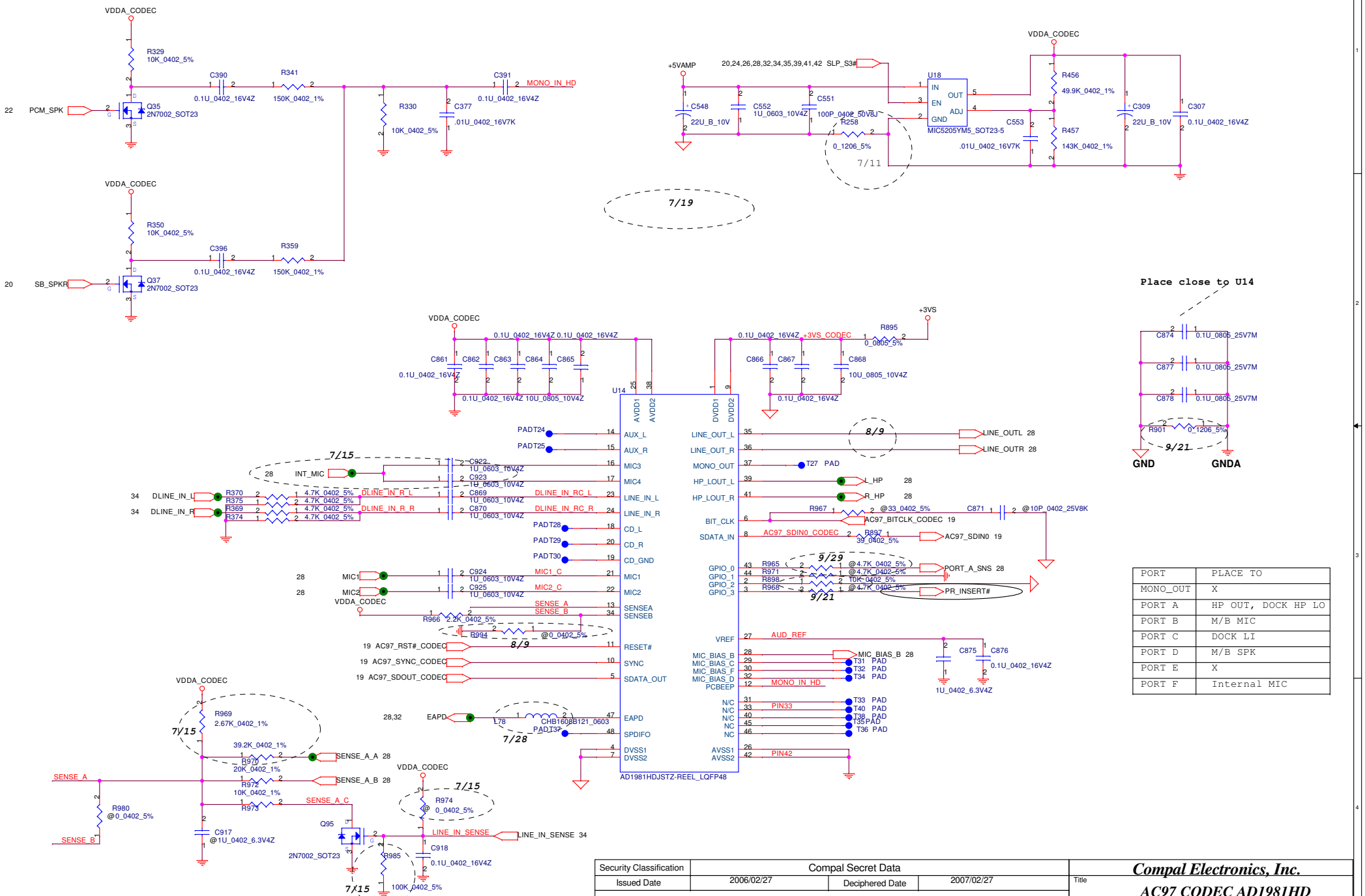

PORT	PLACE TO
MONO_OUT	X
PORT A	HP OUT, DOCK HP LO
PORT B	M/B MIC
PORT C	DOCK LI
PORT D	M/B SPK
PORT E	X
PORT F	Internal MIC

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Issued Date	2006/02/27	Deciphered Date	2007/02/27

Compal Electronics, Inc.

Title: AC97 CODEC AD1981HD

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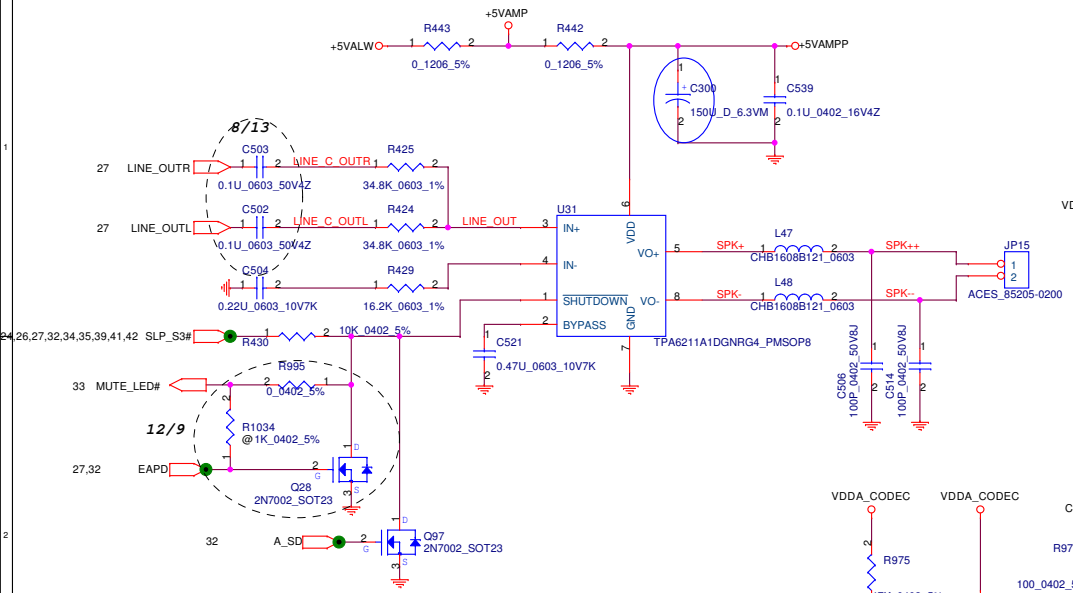
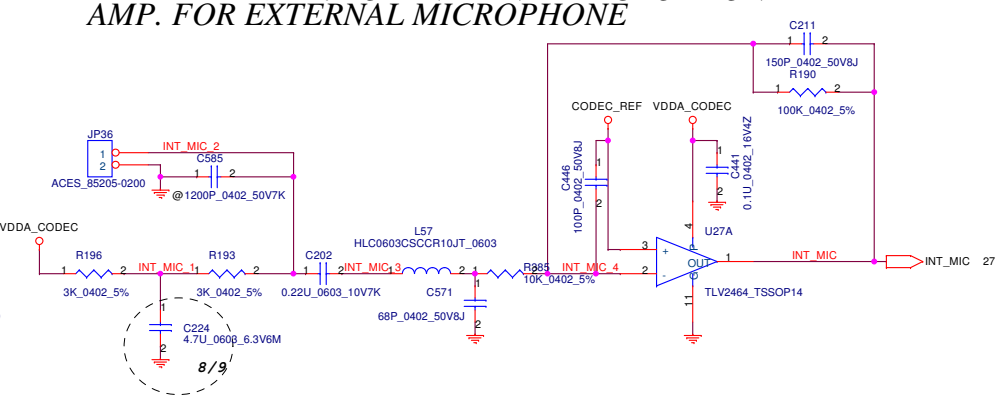
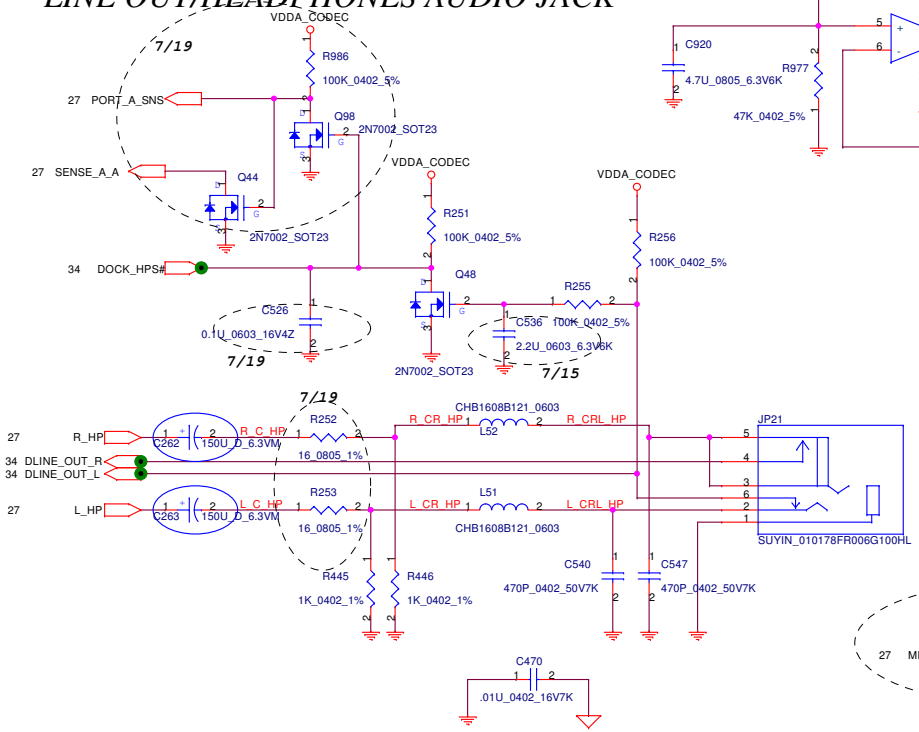
AMP. FOR INTERNAL SPEAKER

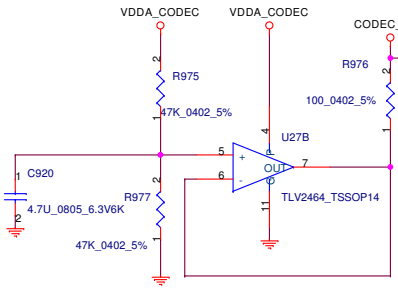


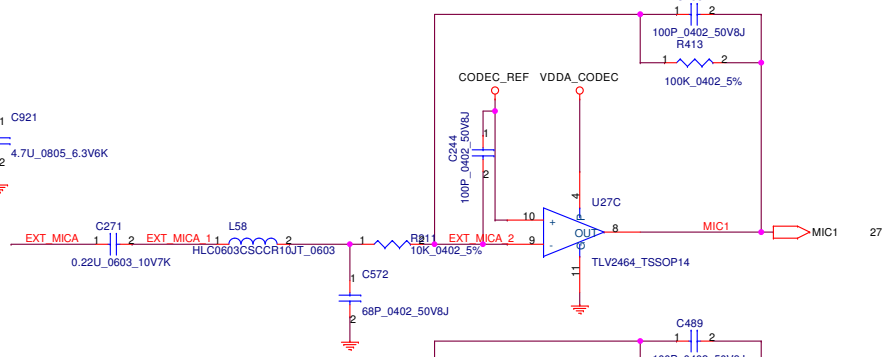
AMP. FOR INTERNAL MICROPHONE
AMP. FOR EXTERNAL MICROPHONE

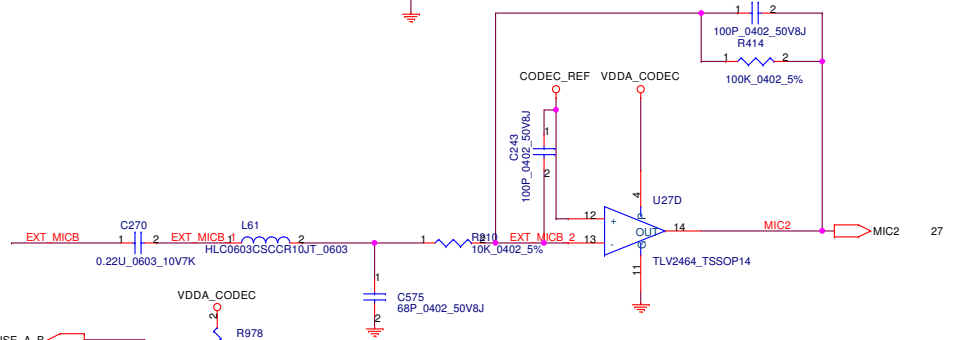


LINE OUT/HEADPHONES AUDIO JACK

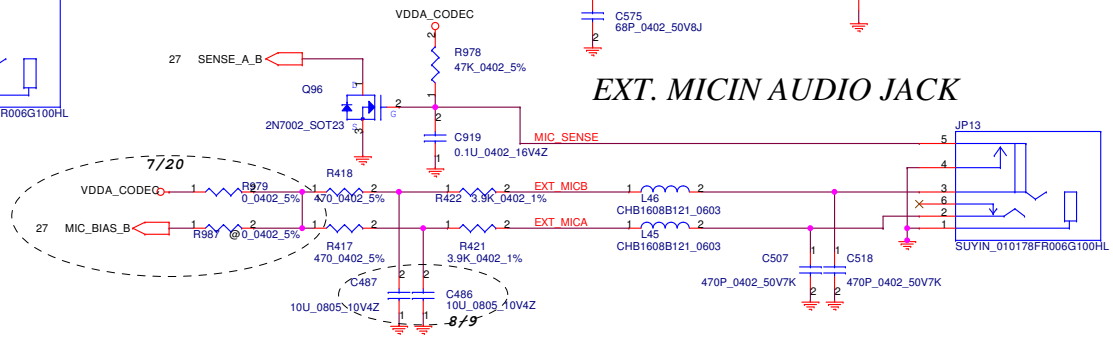








EXT. MICIN AUDIO JACK



Security Classification	Compal Secret Data		
Issued Date	2006/02/27	Deciphered Date	2007/02/27

Compal Electronics, Inc.			
Title	AMP & Audio Jack		
Size	Document Number		Rev
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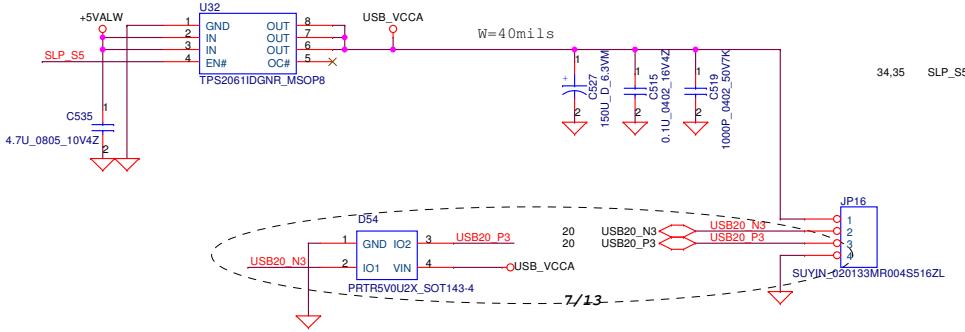
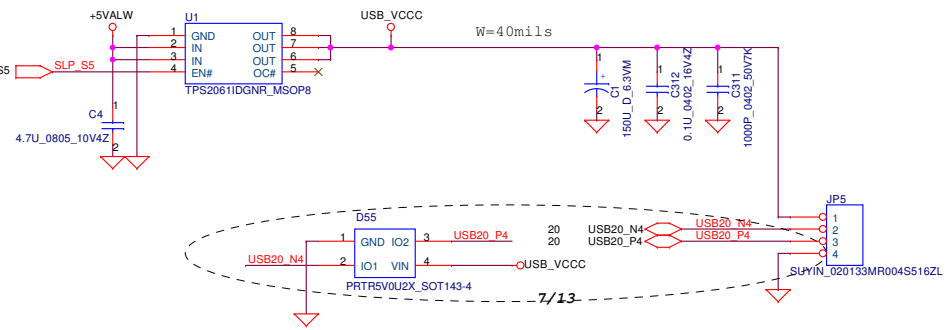
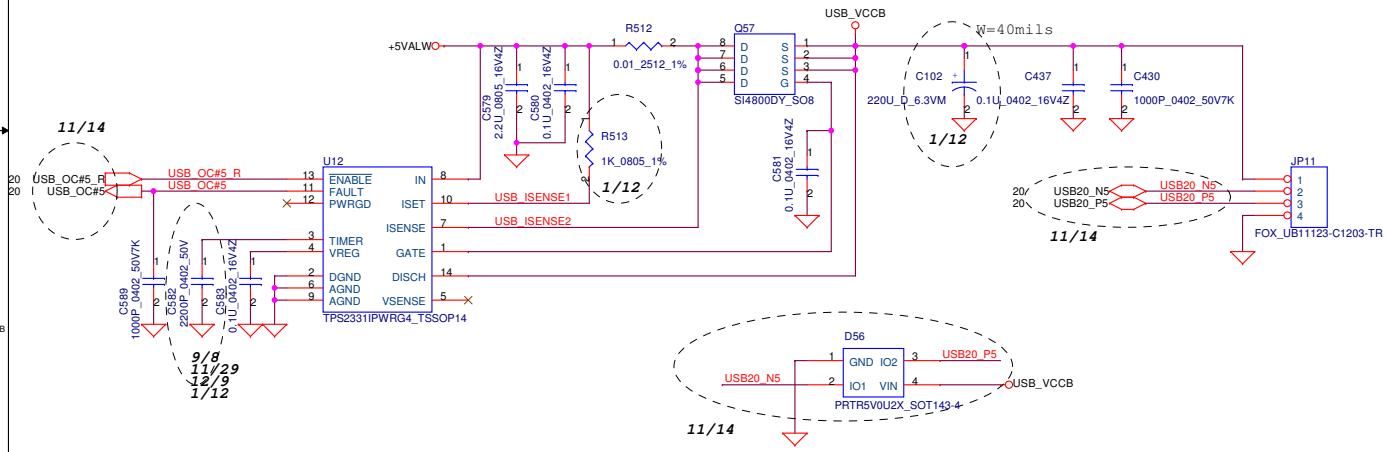
USB CONNECTOR 1



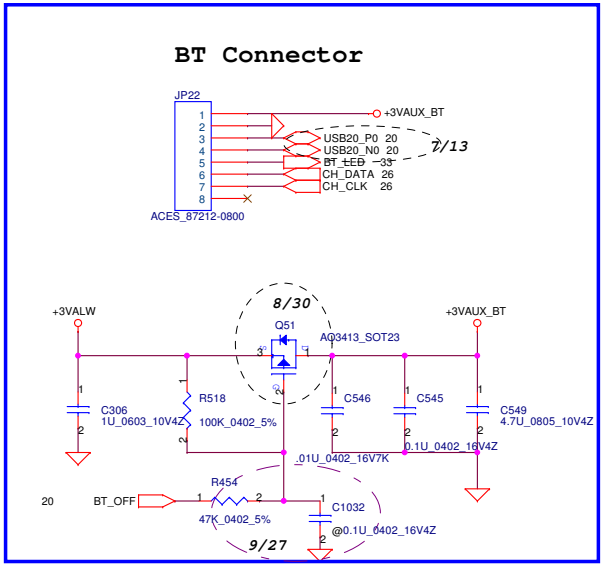
USB CONNECTOR 2



USB CONNECTOR 3



BT Connector



Security Classification	Compal Secret Data		
Issued Date	2006/02/27	Deciphered Date	2007/02/27

Compal Electronics, Inc.			
Title	USB & BT Connector		
Size	Document Number		Rev
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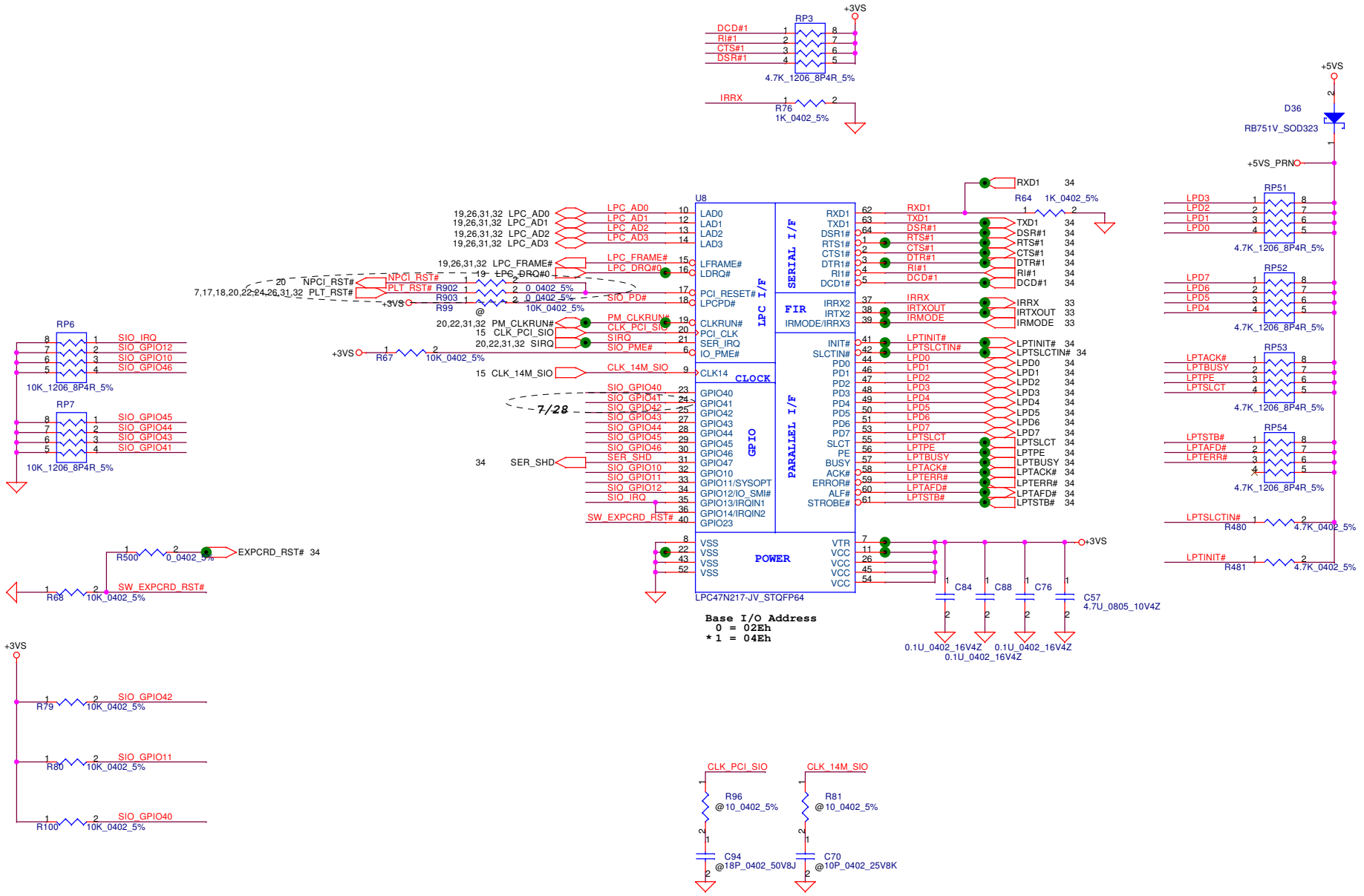

Security Classification	Compal Secret Data		
Issued Date	2006/02/27	Deciphered Date	2007/02/27

Compal Electronics, Inc.			
Title	SUPER I/O LPC47N217		
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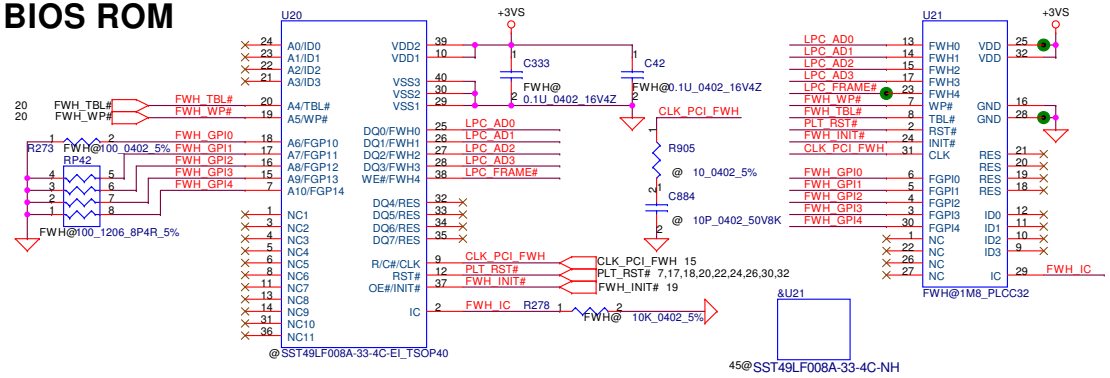
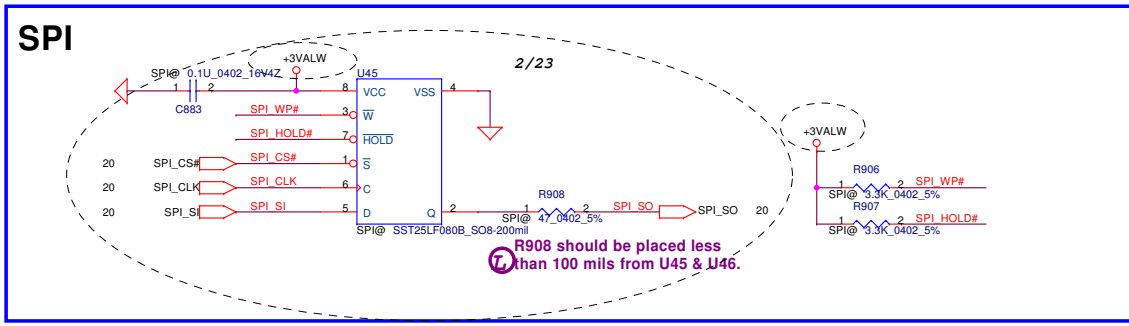
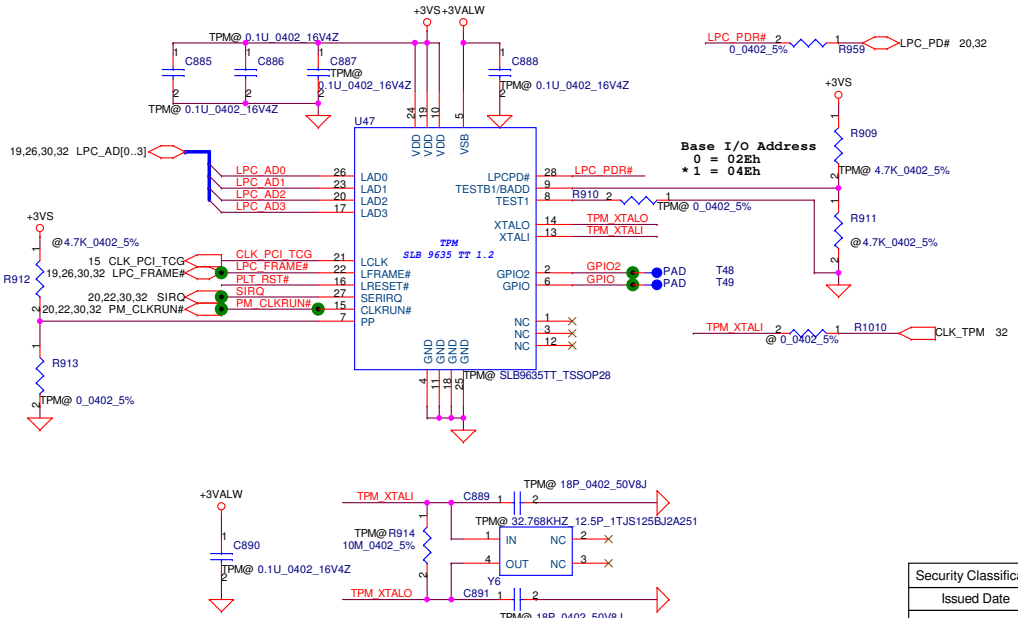
BIOS ROM



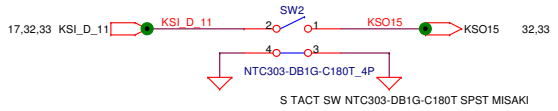
SPI



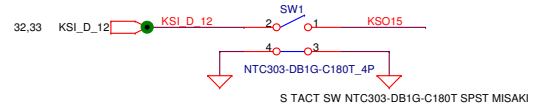
TPM1.2



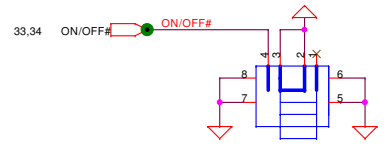
Wireless/BT ON & OFF Button

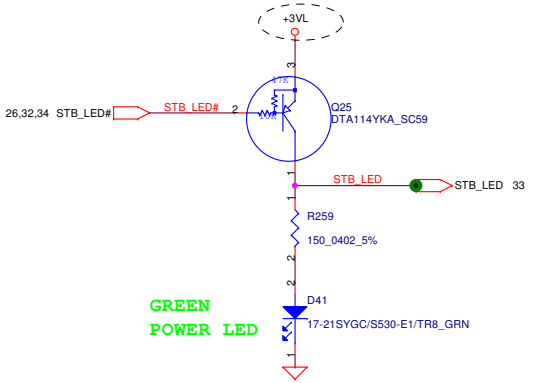


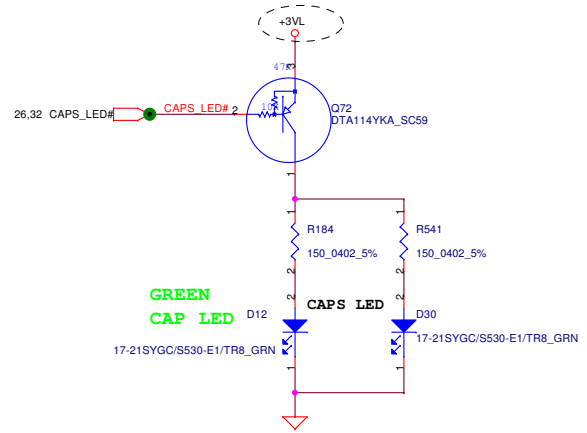
QuickLook Button



ON/OFF & SLEEP Button







Security Classification	Compal Secret Data		
Issued Date	2006/02/27	Deciphered Date	2007/02/27

Compal Electronics, Inc.			
Title: TCG/BIOS ROM/PS2/LED/SW			
Size	Document Number: LA-3031P		Rev: 0.5
Date: Tuesday, February 28, 2006	Sheet 31 of 49		

250@	1021@
R78	R930
R62	

Note: R94 must be removed when R1354 stuff and R87 remove.

AGND FILTER

BIOS debug port
Place under KB area

For KBC debugging used.

1. For normal operation:
   Un-install R29,R65
2. For KBC internal ROM flash:
   Install R29,R65

KBC1021_TQFP100

32.768KHZ_12.5P_1TJS125DJ2A073

Security Classification	Compal Secret Data		
Issued Date	2006/02/27	Deciphered Date	2007/02/27

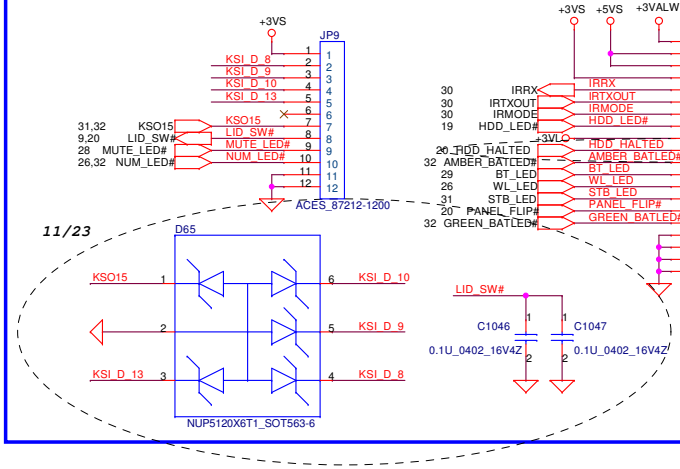
Compal Electronics, Inc.

Title: **LPC47N1021**

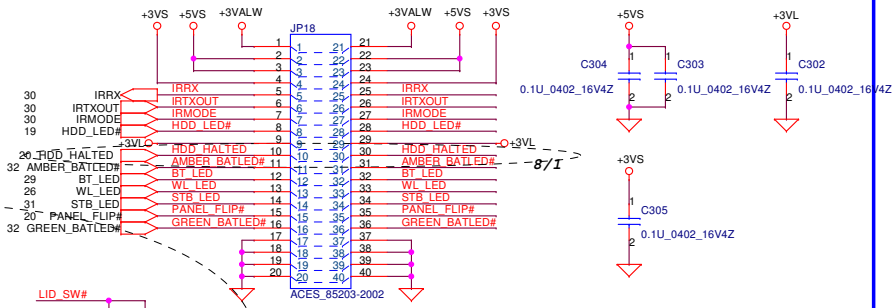
Size: | Document Number: **LA-3031P** | Rev: 0.5

Date: Tuesday, February 28, 2006 | Sheet 32 of 49

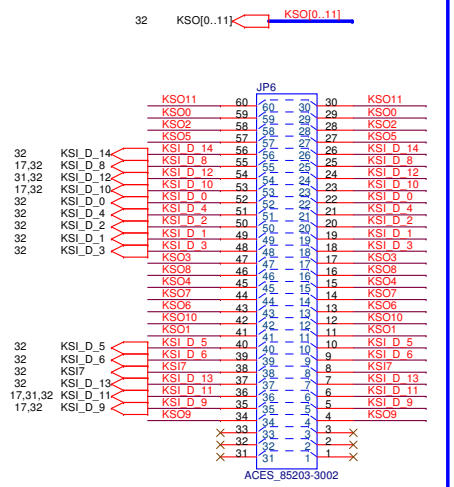
FUN BD.

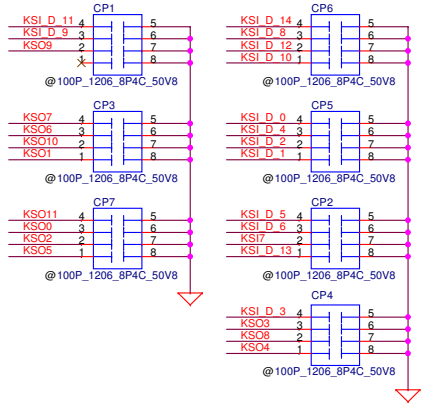


FIR & LED BD.

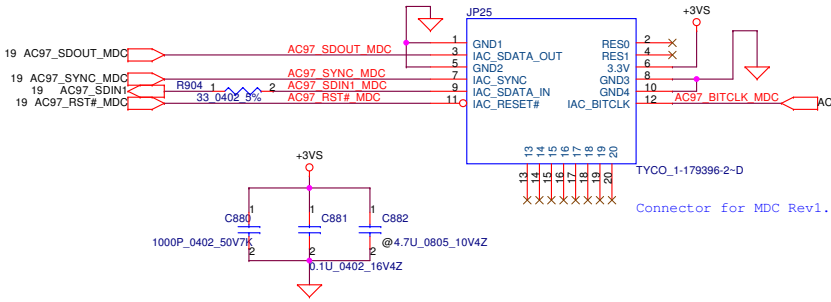


INT_KBD CONN.

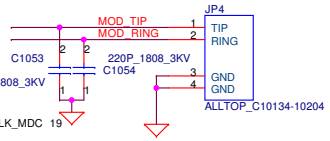




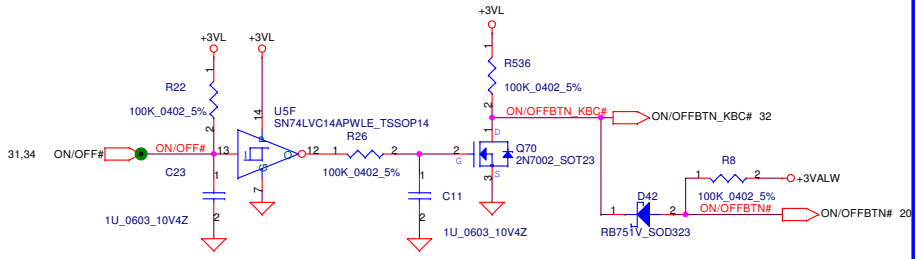
MDC 1.5 Conn.



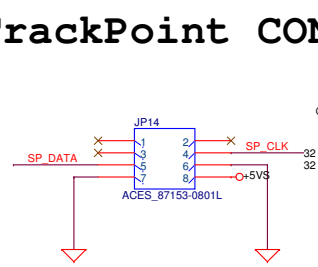
RJ-11 CONN.



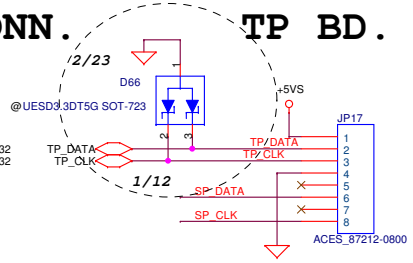
Power button



TrackPoint CONN.



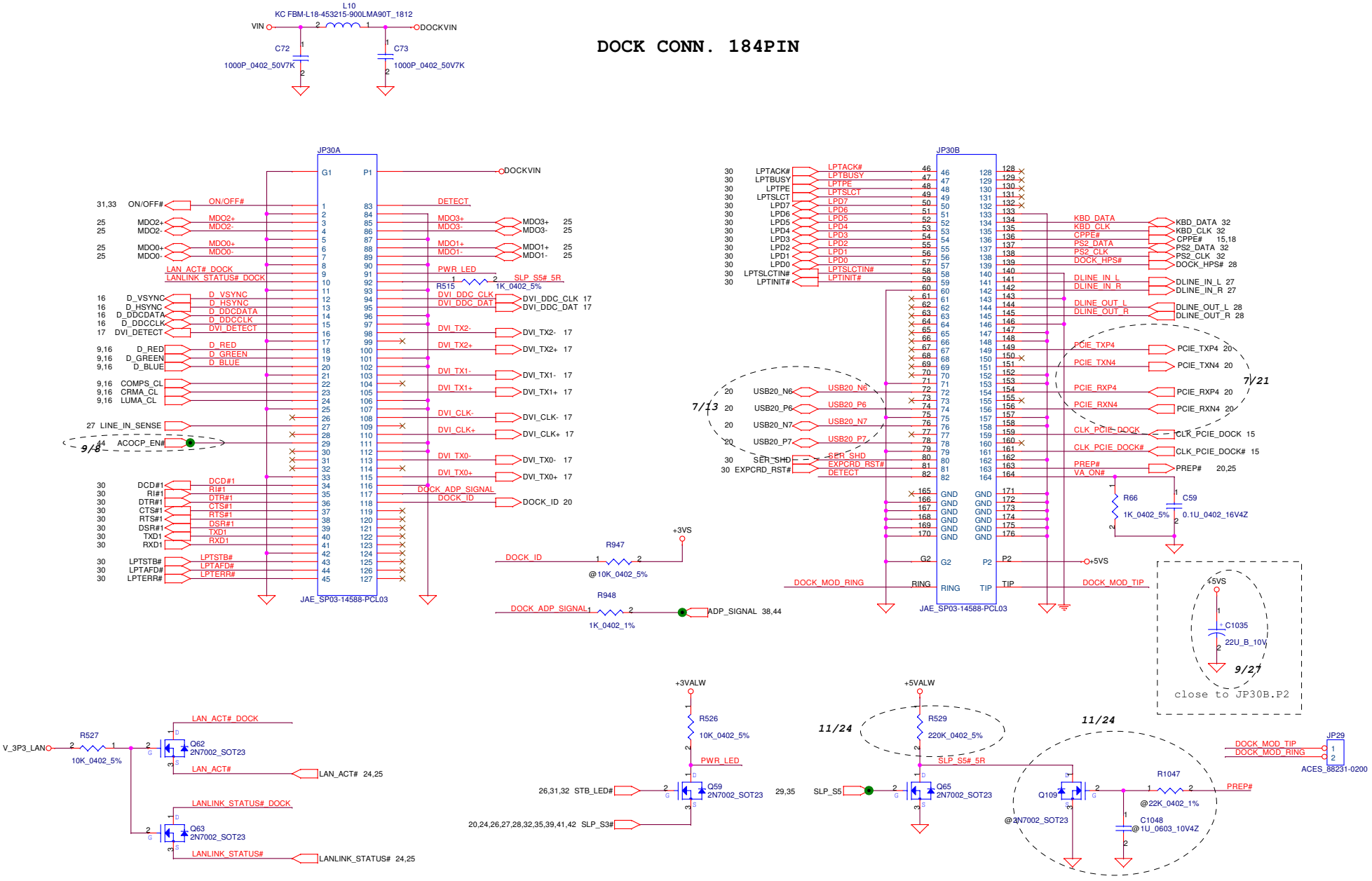
TP BD.



Security Classification	Compal Secret Data		
Issued Date	2006/02/27	Deciphered Date	2007/02/27

Compal Electronics, Inc.			
Title	MDC/KBD/ON_OFF/LID		
Size	Document Number		Rev
	LA-3031P		0.5
Date:	Tuesday, February 28, 2006	Sheet	33 of 49

DOCK CONN. 184PIN



Security Classification	Compal Secret Data		
Issued Date	2006/02/27	Deciphered Date	2007/02/27

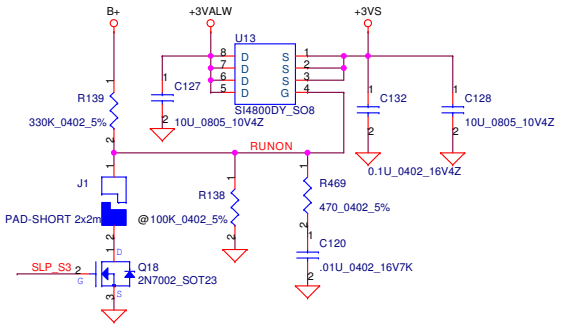
Compal Electronics, Inc.

Title: **SPR Connector**

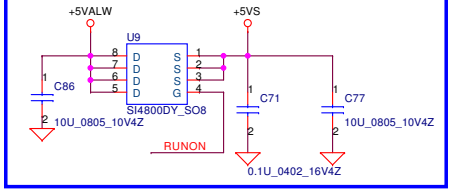
Size	Document Number	Rev
	LA-3031P	0.5

Date: Tuesday, February 28, 2006 | Sheet 34 of 49

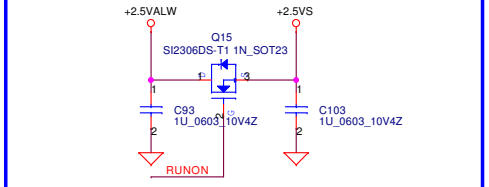
+3VALW to +3VS Transfer

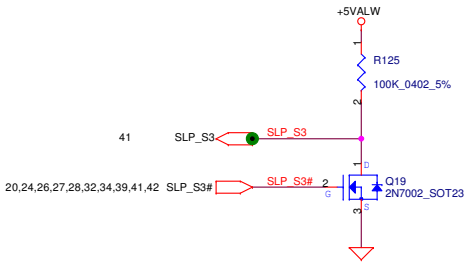


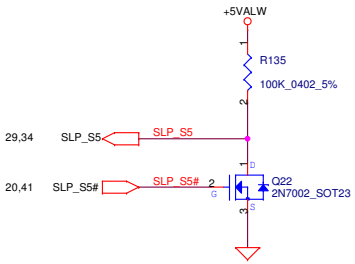
+5VALW to +5VS Transfer



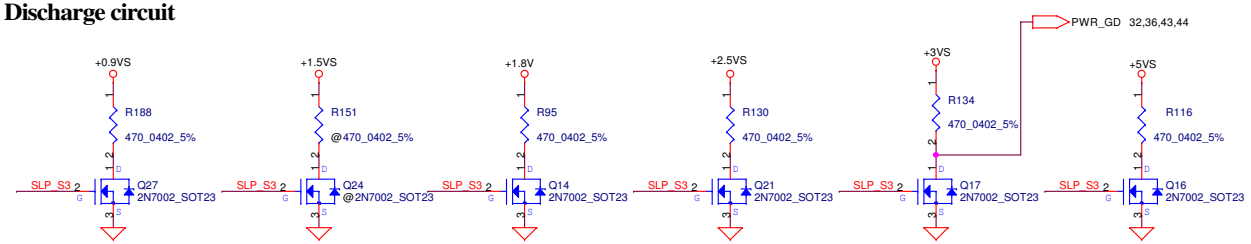
+2.5VALW to +2.5VS Transfer





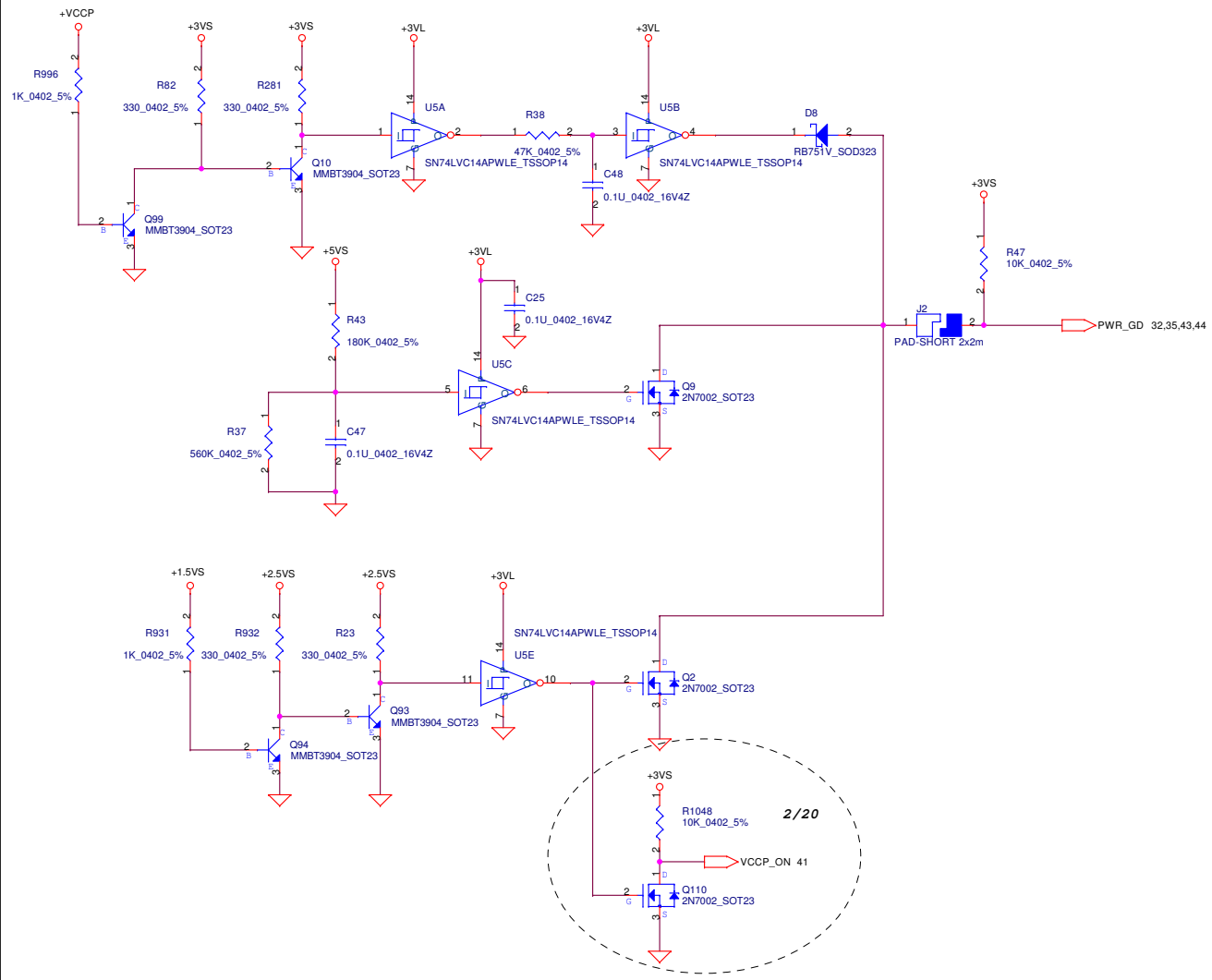


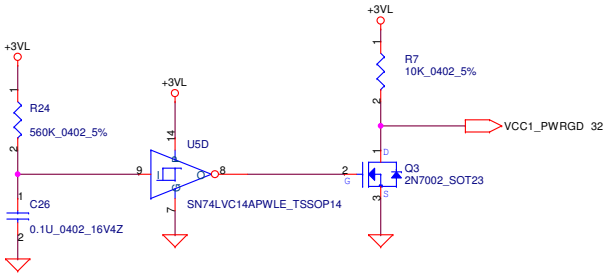
Discharge circuit

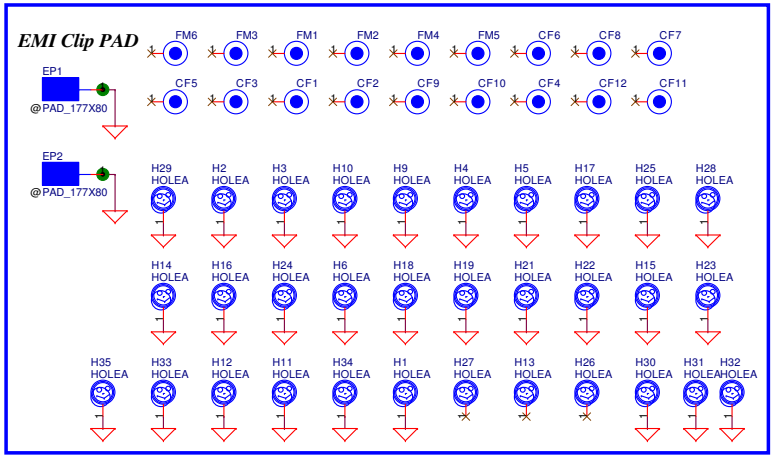


Security Classification	Compal Secret Data		
Issued Date	2006/02/27	Deciphered Date	2007/02/27

Compal Electronics, Inc.			
Title: DC/DC Circuits			
Size	Document Number: LA-3031P		Rev: 0.5
Date: Tuesday, February 28, 2006	Sheet 35 of 49		







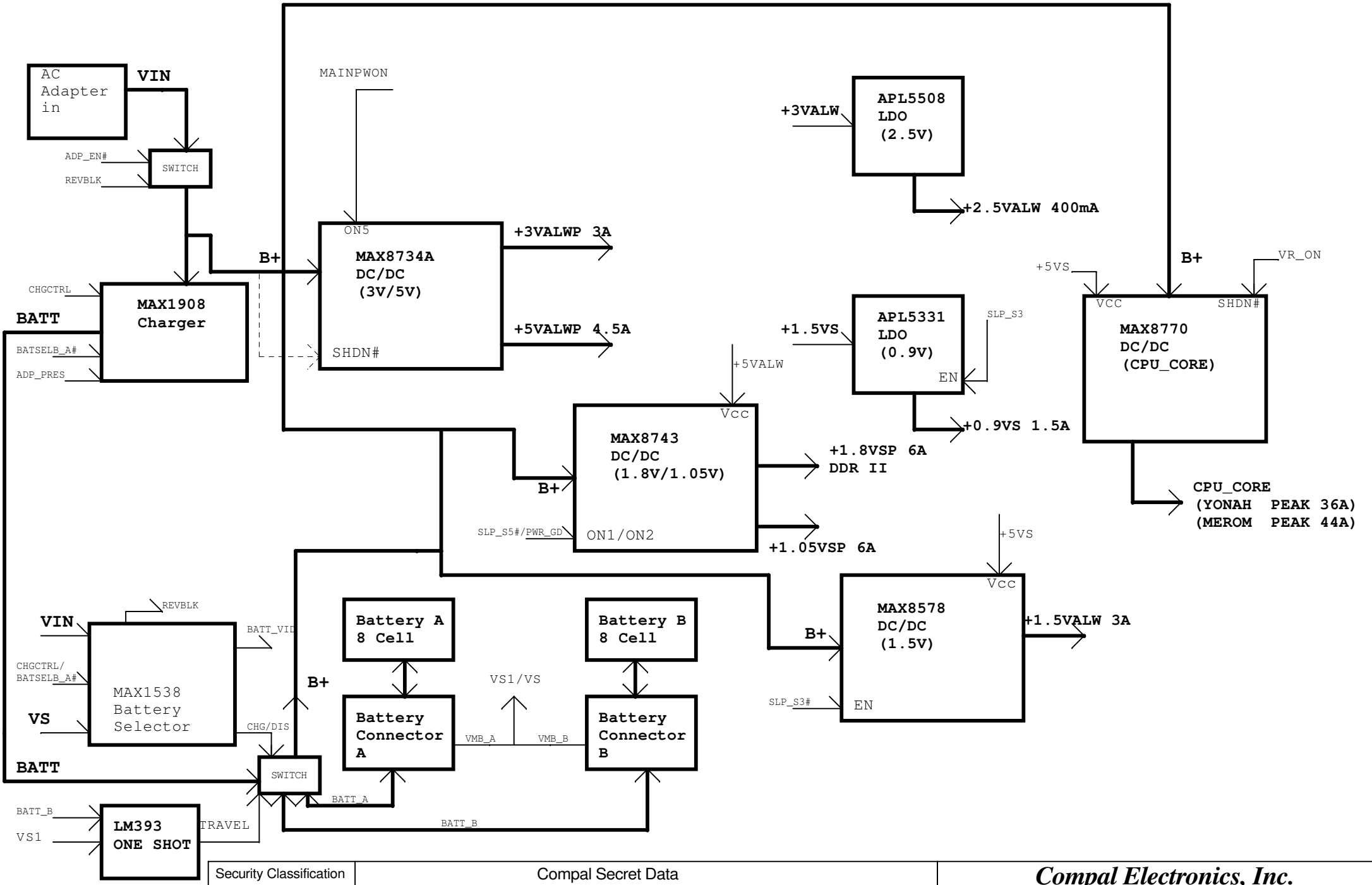
Security Classification	Compal Secret Data		
Issued Date	2006/02/27	Deciphered Date	2007/02/27

Compal Electronics, Inc.

Title: **POK CKT**

Size	Document Number	Rev
	LA-3031P	0.5

Date: Tuesday, February 28, 2006 | Sheet 36 of 49



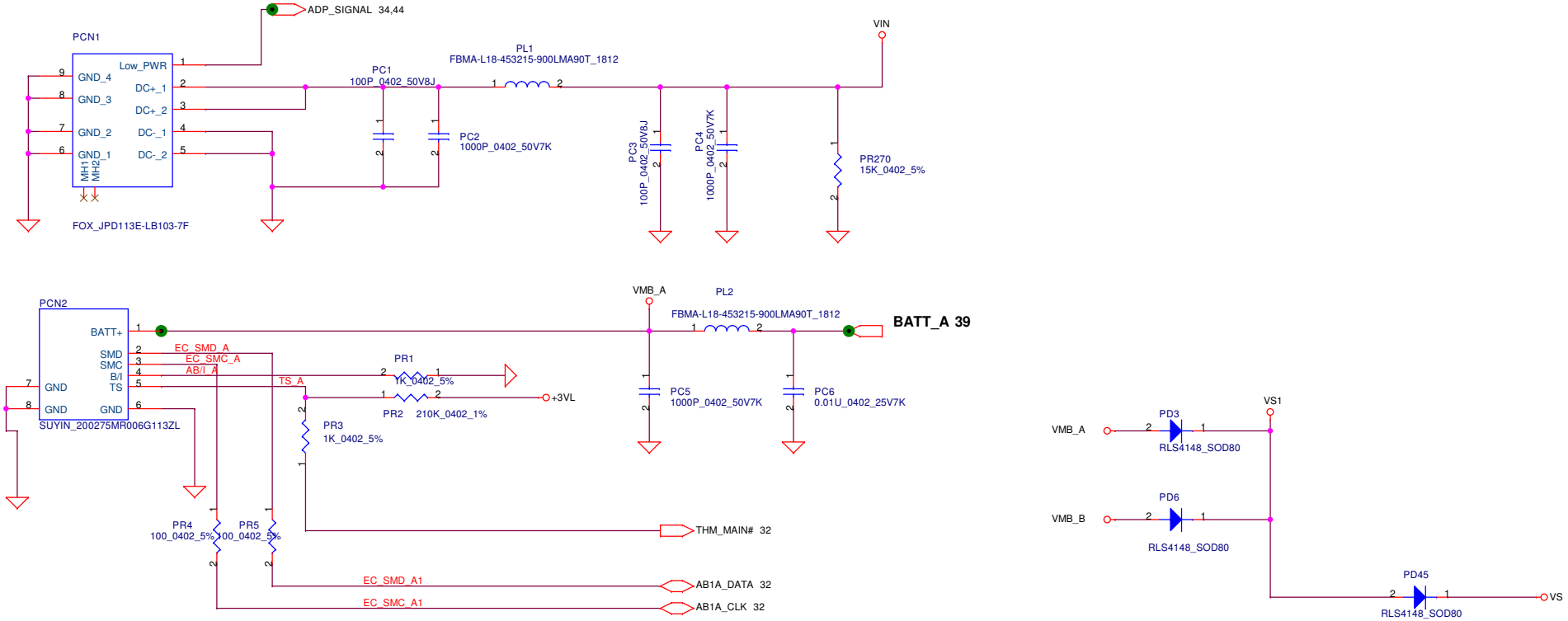
Security Classification	Compal Secret Data		
Issued Date	2006/02/27	Deciphered Date	2007/02/27

Compal Electronics, Inc.

Title: **POWER BLOCK DIAGRAM**

Size	Document Number	Rev
	LA-3031P	0.5

Date: Tuesday, February 28, 2006 | Sheet 37 of 49



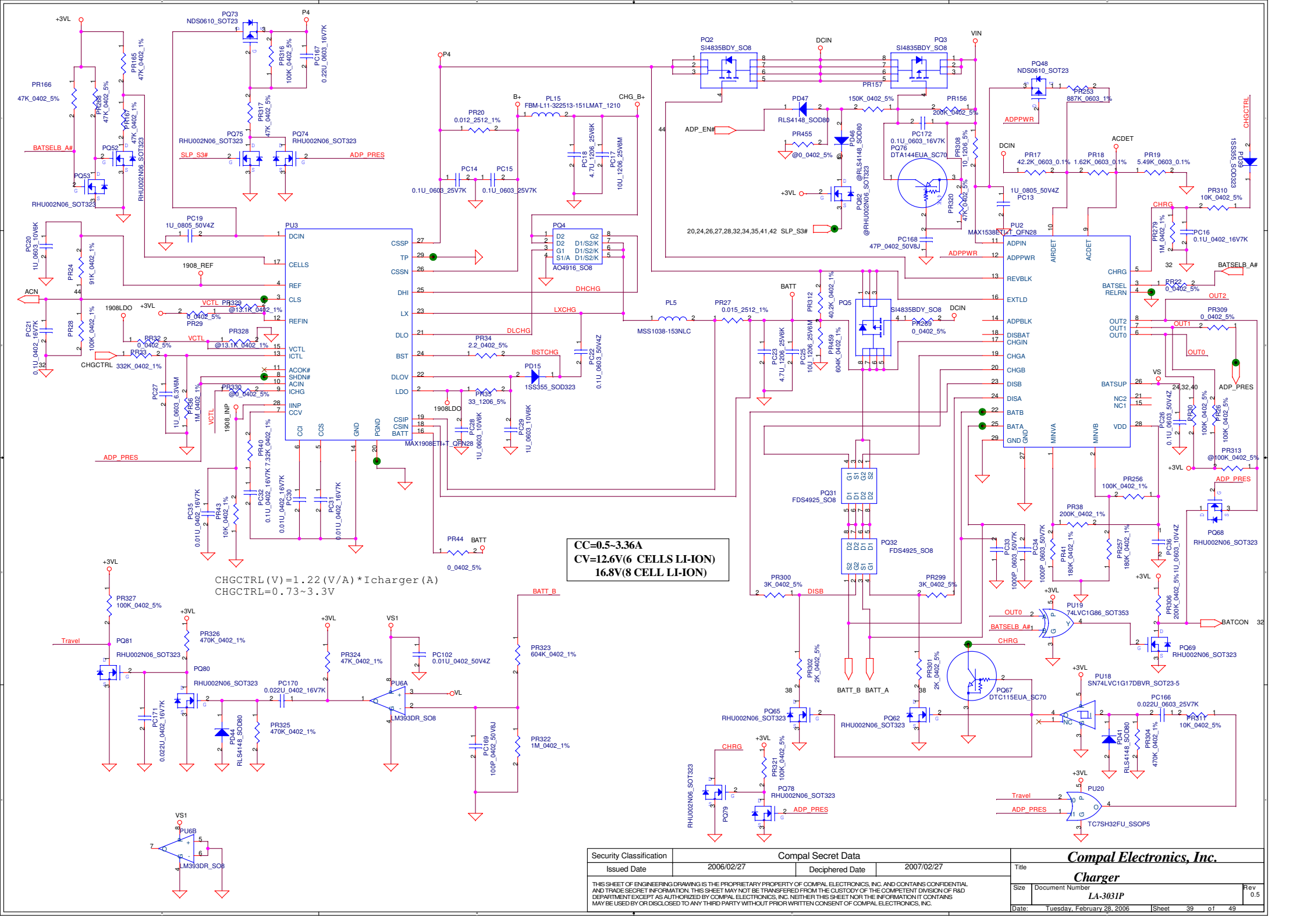
Security Classification	Compal Secret Data		
Issued Date	2006/02/27	Deciphered Date	2007/02/27

Compal Electronics, Inc.

Title: **BATTERY CONN**

Size	Document Number	Rev
	LA-3031P	0.5

Date: Tuesday, February 28, 2006 | Sheet 38 of 49



Security Classification	Compal Secret Data		
Issued Date	2006/02/27	Deciphered Date	2007/02/27

Compal Electronics, Inc.

Title: **Charger**

Size	Document Number	Rev
	LA-3031P	0.5

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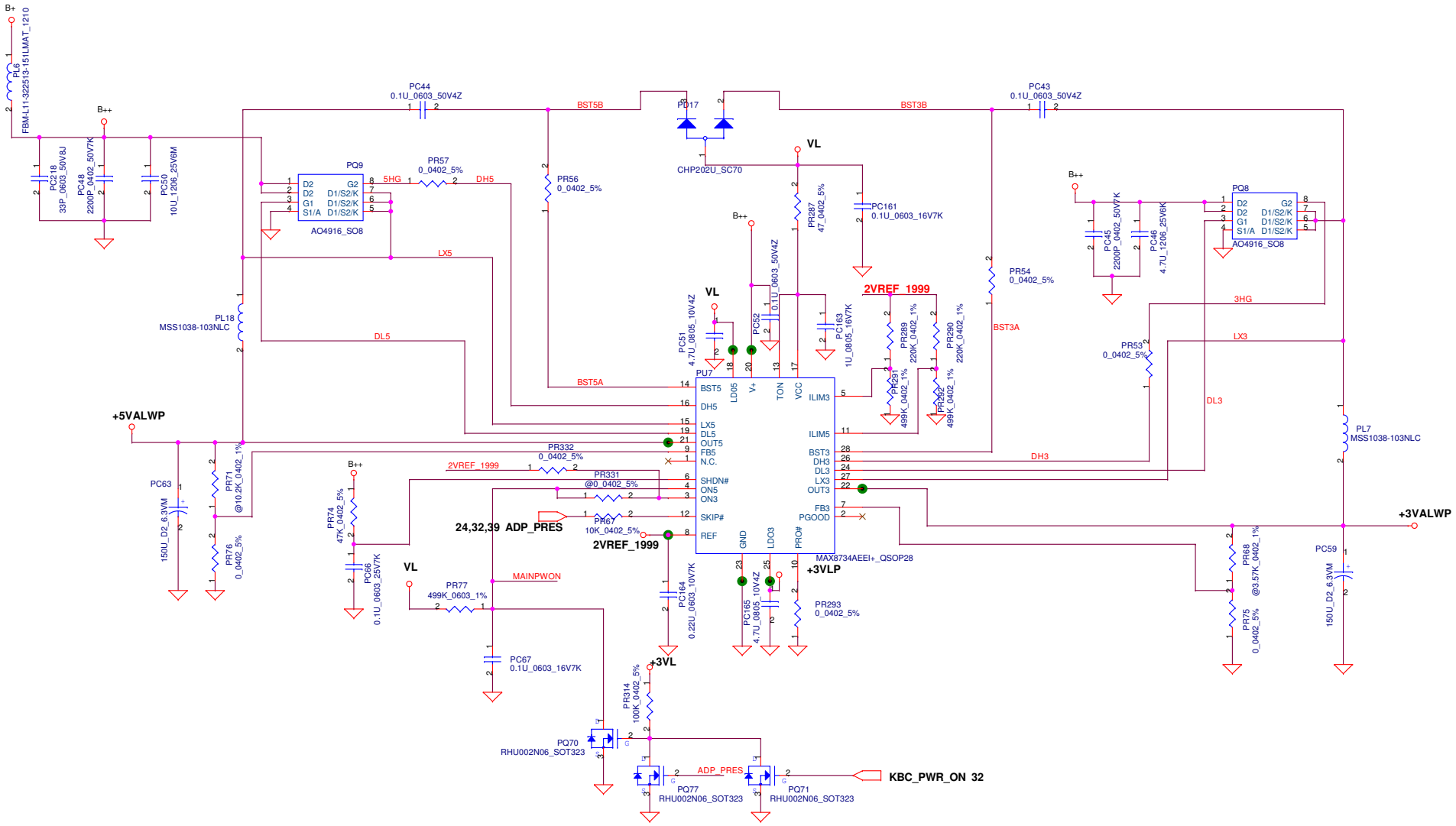
+3.3V/+5V



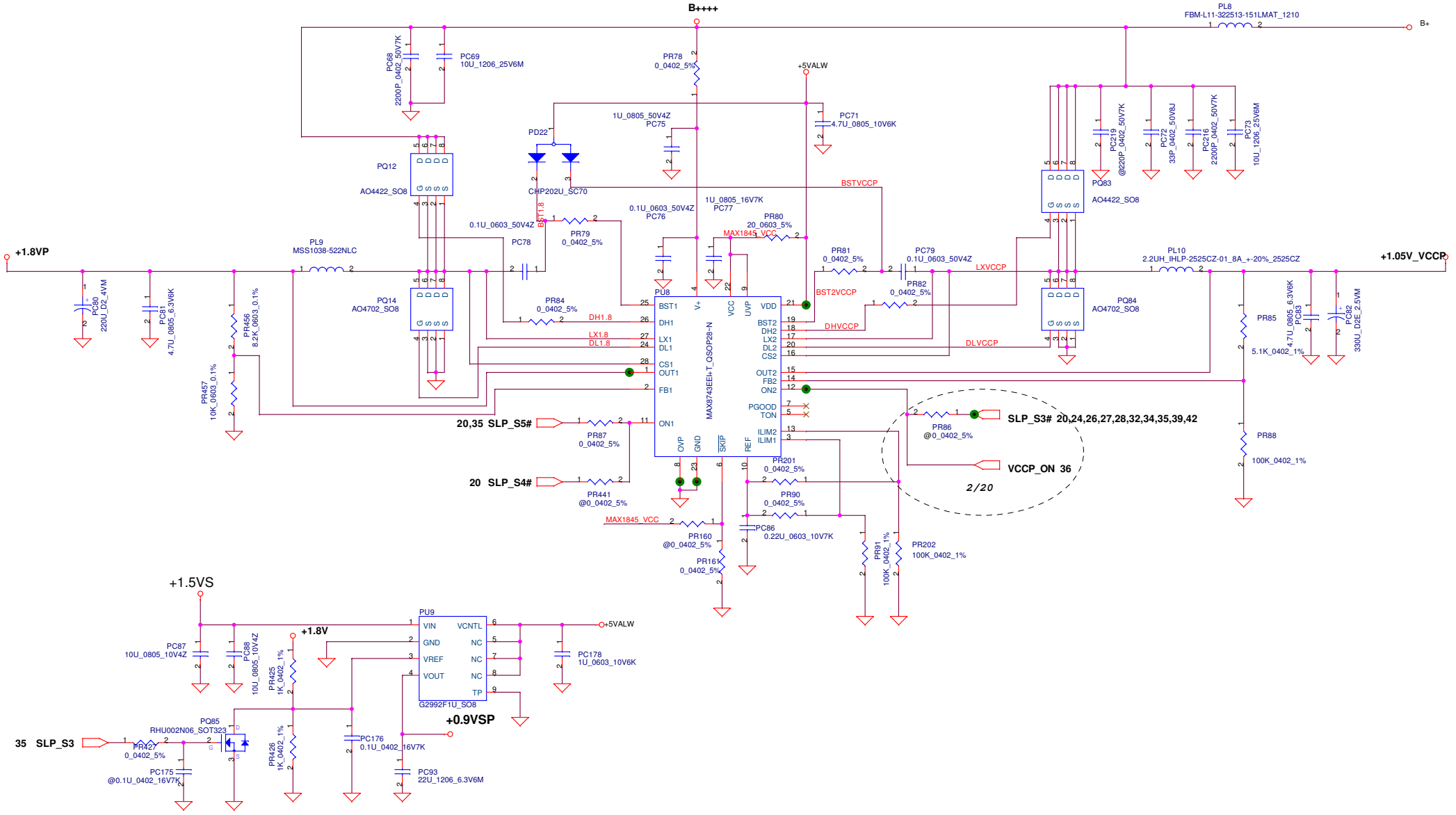
Security Classification	Compal Secret Data		
Issued Date	2006/02/27	Deciphered Date	2007/02/27

Compal Electronics, Inc.

Title: **3.3V / 5V**

Size	Document Number	Rev
	LA-3031P	0.5

Date: Tuesday, February 28, 2006 | Sheet 40 of 49



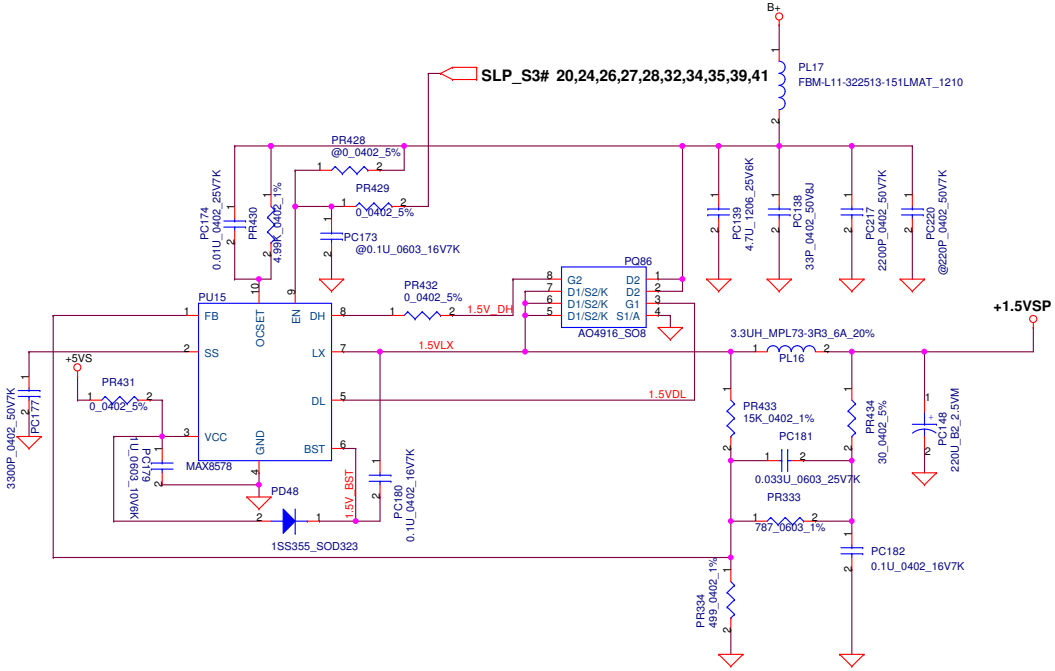
Security Classification	Compal Secret Data		
Issued Date	2006/02/27	Deciphered Date	2007/02/27

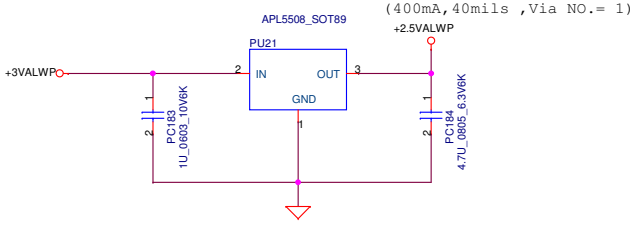
Compal Electronics, Inc.

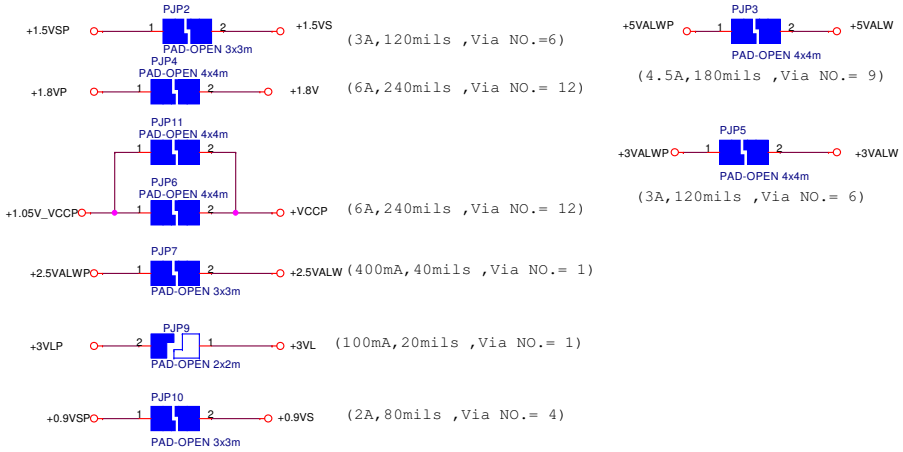
Title: **DDRII/+1.05VSP/+1.8VSP**

Size	Document Number	Rev
	LA-3031P	0.5

Date: Tuesday, February 28, 2006 | Sheet 41 of 49





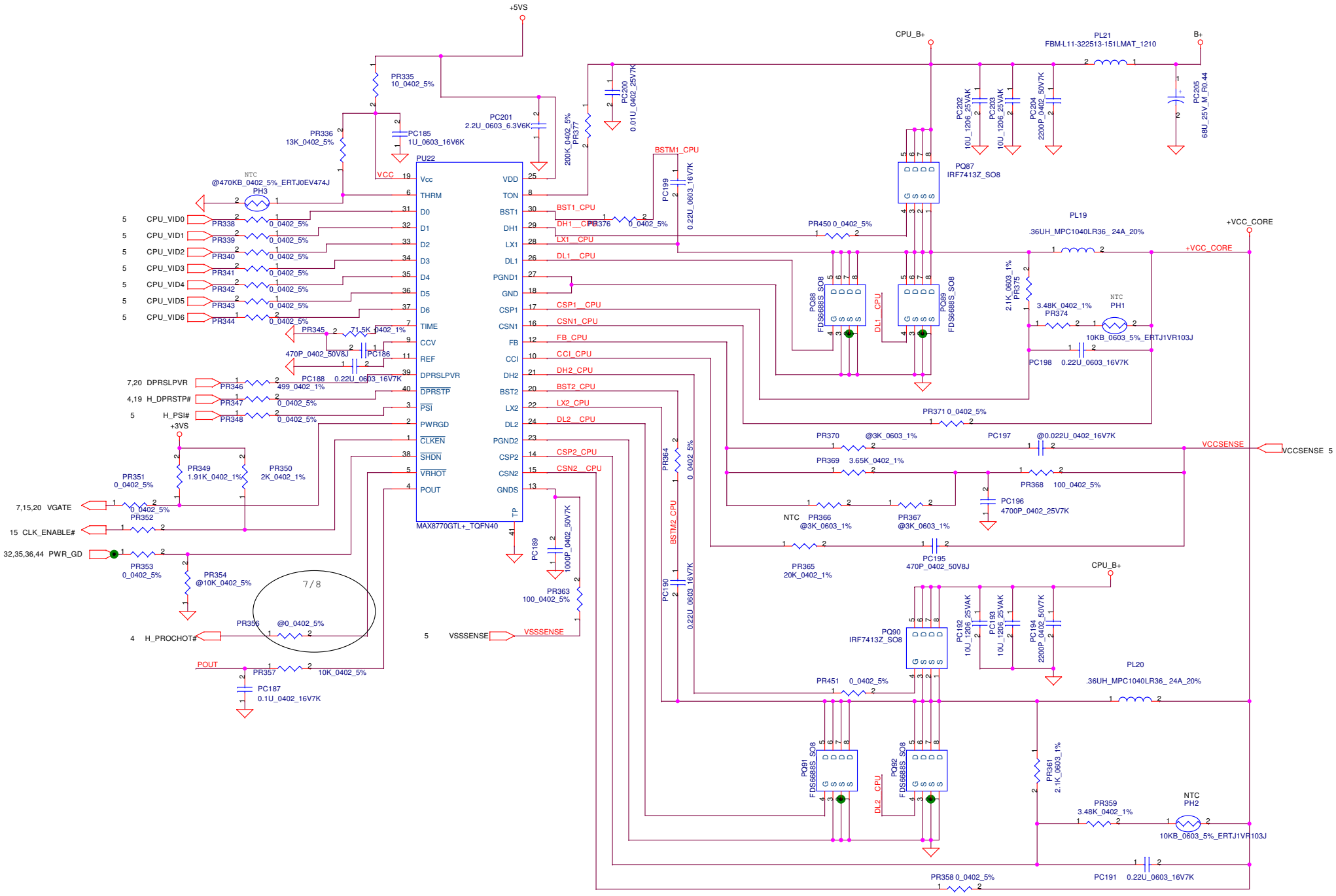


Compal Electronics, Inc.

Title: **2.5VALWP/1.5VSP**

Size	Document Number	Rev
	LA-3031P	0.5

Date: Tuesday, February 28, 2006 | Sheet 42 of 49



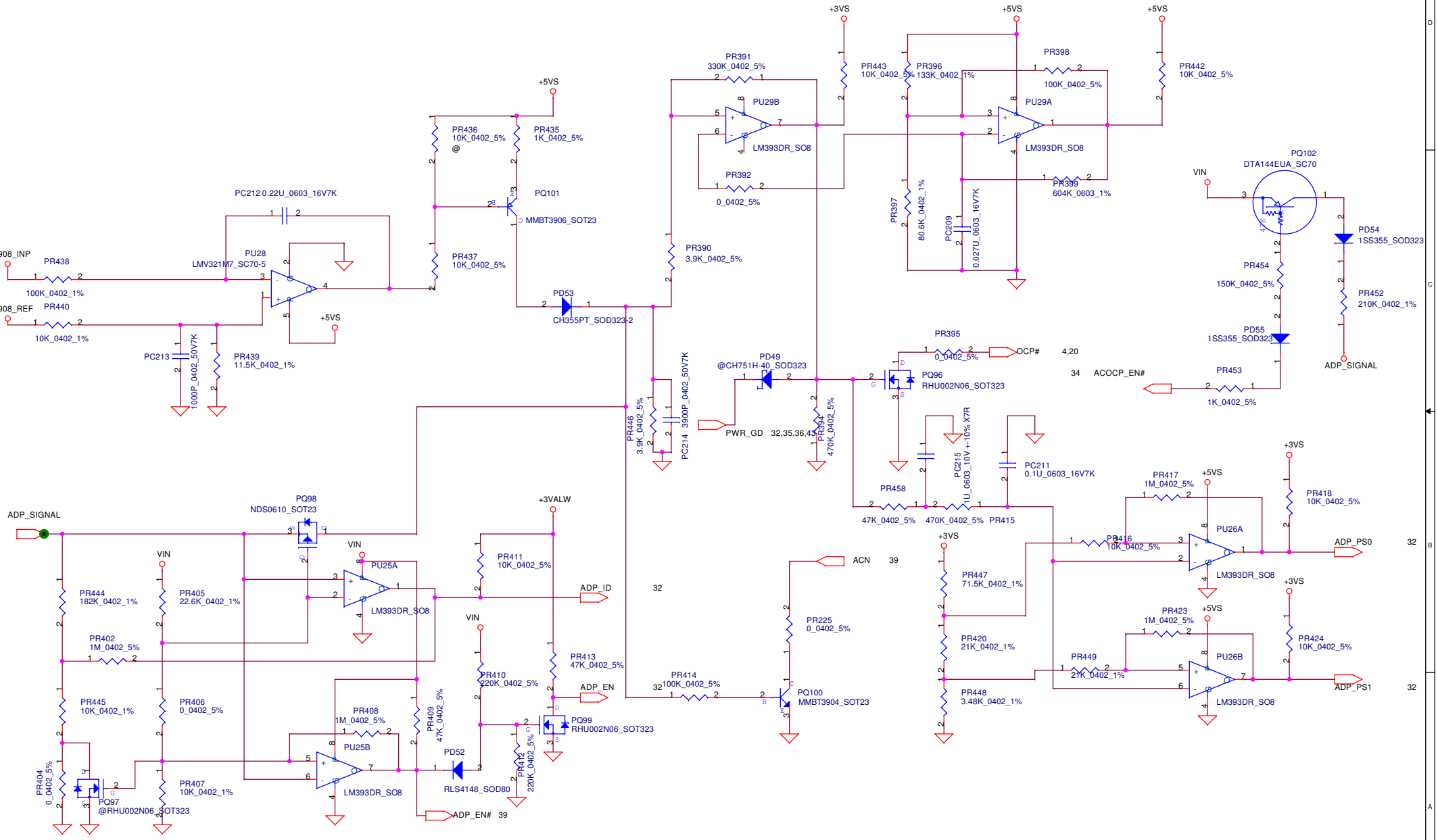
Security Classification	Compal Secret Data		
Issued Date	2006/02/27	Deciphered Date	2007/02/27

Compal Electronics, Inc.

Title: **+CPU_CORE**

Size	Document Number	Rev
	LA-3031P	0.5

Date: Tuesday, February 28, 2006 | Sheet 43 of 49



Security Classification	Compal Secret Data		
Issued Date	2006/02/27	Deciphered Date	2007/02/27

Compal Electronics, Inc.

Title: **ADP_OCP**

Size	Document Number	Rev
	LA-3031P	0.5

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EE PIR list

DB Build:

07/19/2005

Page 4 -Remove R565 and R566 and disconnect from +VCCP.

Page 10 - Add a 47uF cap on U15H.E21,F21 for resolution of possible wavy video issues..

Page 10 - Add a 47uF cap on R615-2 for resolution of possible wavy video issues.

Page 16 - Add R988 and R989 to leave the option in the future to change the values for impedance matching.

Page 20 - Make U28C.E23 a test point.

Page 27 - Change DOCK_HPS# to PORT_A_SNS at R965

Page 27 - delete R979 and jumper

Page 27 - delete R894 and jumper

Page 27 - delete R900 and jumper

Page 27 - Change CODEC_REF to MIC_BIAS_B on pin 28 of U14

Page 27 - Connect LINE_IN_SENSE to pin 27 of JP30A docking connector

Page 27 - Change R526 from 1uF to 0.1uF

Page 27 - Reserve C917.

Page 27 - Reserve R901

Page 28 - add zero ohm mic bias options to VDDA_CODEC and MIC_BIAS_B

Page 28 - add inverting fet and PORT_A_SNS sense signal

Page 28 - Change R252, R253 from 0402 to 0805 package size.

Page 32 - Remove R928

Page 32 - Remove R538 and disconnect net EC_GPIO12 from +3VL.
Remove J10 and J12. EC_GPIO12 should be directly connected to ADP_PS1

Page 32 - Remove J15 and disconnect net BATCON from OUT0.

Page 32 - Remove J11 and connect diode CH751H-40_SC76 (pin 2) to EC_GPIO13 and pin1 to ADP_PRES.

Page 34 - Connect JP30A.27 to LINE_IN_SENSE

07/20/2005

Page 28 - Connect R418 and R417 side 1 together to apply the bias voltage (VDDA_Codec or the optional MIC_BIAS_B) to both the tip and ring.

Page 32 - Remove D62

07/21/2005

Page 20 - Remove connections for USB_OC#3 and USB_OC#4 from the USB ports and USB_OC#2 net from RP55.

Page 20 - Reserve R789 for Calistoga A1.

Page 20 - Connect Net PM_EXTTS#0 (U15B.F25) to JP34.50 and JP10.50 for TS.

Page 26 - Remove Mini-Card Clip JP38.

Page 26 - Reserve 0-ohm option resistor from XMIT_OFF to XMIT_OFF# to bypass Q92

07/22/2005

Page 17 - Modify fingerprint signal.

Page 20 - Change PCIE port 5 to PCIE port 4 for the PCIE channel for the dock

07/25/2005

Page 7 - Reserve R586. because IMVP6 VR had installed a series Resistor (500-Ohm)

07/27/2005

Page 17 - add 2 pins GND by removing B+_LCD *1 and LCDVDD *1 and modify all signals except LVDS

Page 29 - Install D54, D55 and D56 for HP request.

07/28/2005

Page 4 - Add C932 and C933 for EMI request.

Page 27 - Add L78 for EMI request.

07/29/2005

Page 4 - Modify the thermal sensor from ADM1032 to ADT7461.

Page11 - Reserve R626 per the latest Intel CRB schematics v1.502

Page19 - Remove +3VS from SATA for HP request.

08/01/2005

Page22 - Modify R957 and R958 from 2.2K to 100K for TI request.

Page26 - Reserve R950.

08/03/2005

Page16 - Add R991, R992 and R993 for EMI.

08/09/2005

Page 27 - add open pull down resistor (R994) option on SENSE B for ADI request.

Page 27 - delete C915 and C916 for ADI request.

Page 28 - add resistor (R995) jumper option between pins 1 and 2 of Q97 for ADI request.

Page 28 - change C224 from 1uF to 4.7uF for ADI request.

Page 28 - change C487, C486 from 4.7uF to 10uF for ADI request.

08/12/2005

Page 17 - change D62.4 from _USB_VCCA to +3VS.

08/13/2005

Page 28 - change the option bypass R995 to bypass Q28

Page 28 - Change C502 and C503 from 0.1uF to 0.22uF

08/15/2005

Page 24 - reserve R856by Boardcom request.

08/17/2005

Page 28 - Change C502 and C503 from 0.22uF to 0.1uF

SI-1 Build:

08/19/2005

Page 7 - Install R587 and R592 for V_DDR_MCH_REF.

Page 26 - Move +3VL from JP37.39 to JP37.45 and move CAPS_LED# from jp37.41 to JP37.51.

09/08/2005

Page 4 - Change the Thermal Sensor U16 back to ADM1032.

Page 18 - Install R742 to connect ACCEL_INT to PCI_PIRQH# (U28B.G7).

Page 20 - R793 on U28C.E20 should be NC (with @ symbol NOT ACCEL@) to disconnect U28C.E20 from ACCEL_INT.

Page 25 - disconnect R270 & R271 from C320.
Add another 1000pF 2 to 3KV capacitor to ground for R270 & R271 connection

Page 29 - Change the timing capacitor C582 on U12 pin 3 from 0.1UF to 0.001UF

Page 32 - R78 should have an "250@" symbol and should not be installed for the 1021.

Page 34 - Route ACOCP_EN# from the circuit to the docking connector JP30A.29 and remove net SM_ADPTR.

09/12/2005

Page 20 - Remove R792 and R793 and disconnect nets ADP_ID and ACCEL_INT from U28C.E20. Make U28C.E20 a TP.

Page 32 - Add R998 for KBC TX issue.

09/14/2005

Page 17, 20 - Connect JP28.40 to U28.E23 for digitizer sleep pin.

Page 26 - install R990 and un-install R891, R892 and Q92 for BIOS code implement.

09/16/2005

Page 15 - Modify R660 from 475 ohm to 4.7K ohm to meet ICS spec

Page 15 - Install R639, R641 to meet ICS spec

Page 15 - Modify R642, R644, R647, R653, R943, R944, R666, R669, R678, R682, R685, R687, R689, R691, R702, R705, R713, R714 from 33 ohm to 24 ohm to meet ICS spec

Page 15 - NI R643, R645, R648, R654, R659, R661, R662, R663, R667, R670, R679, R683, R686, R688, R690, R692, R703, R706, R708, R709, R981, R982 to meet ICS spec

Page 19 - Change R754, R755, R756, R757, R759, R760, R765, R766 from 33Ohm to 39Ohm.
Add 39Ohm series resistors to AC97_SDIN0, AC97_SDIN1.

Compal Electronics, Inc.	
Title	H/W2 EE Dept. PIR SHEET
Size	Document Number: LA-3031P — Rev: 0.5
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EE PIR list (II)

9/21/2005

Page 27 - Install 10K ohm resistor in the R898 location and install R901 with 0 ohm.

Page 28 - Resistor R995 should be placed from gate of Q28 to drain pin 1

9/23/2005

Page 22 - Add damping resistor on SD_DAT/SD_CMD.

Page 23 - Modify R983 from 4.7K to 33 ohm for CARDBUS issue.

9/27/2005

Page 10 - Add placeholder for 47uF capacitor at R616.2 to GND and R617.2 to GND for bulk capacitance on +3VS_TVDACB and +3VS_TVDACA.

Page 24 - Disconnect PLT_RST from U6A.C2. Add circuit shown for PLT_RST#_LAN and connect signal PLT_RST#_LAN to U6A.C2.

Page 26 - Add circuit for +3VS_MINI. Add pads for JP37.24 to +3VS and +3VALW.

Page 29 - At R454.2 node, add placeholder NI for @0.1uF cap to GND.

Page 31 - Add CLK_TPM signal at R929.1 with NI @0Ohm option. Connect this to U47.13 with another NI @0Ohm option on this pin.

Page 34 - At JP30B.P2, add placeholder for 22uF NI @ capacitor.

9/28/2005

Page 25 - Modify C320 and C934 from 1000p 3KV to 2200p 2KV.

9/29/2005

Page 22 - Add the termination resistor for SD card overshot and undershot.

Page 27 - install R965 to fix the issue of "internal speaker no sound" that found on all DB-B M/B.

Page 36 - Remove the PGD_IN circuit

Page 36 - Remove the VGATE_INTEL circuit

10/04/2005

Page 15 - Move PCIE_LOM/PCIE_LOM# from SCRCLKT1/C1 to SRCCLKT2/C2 (U25.22, U25.23).

Page 24 - Add Circuits to prevent leakage from BCM5753M and is urgent to implement in SI-1.

Page 24 - Remove R656 and disconnect from +3VS and connect CLKREQA# to circuit

Page 24 - Add 0-Ohm NI resistors on ICH_SMBCLK and ICH_SMBDATA on U6A.D9/D8.
This is to leave I2C disconnected and reserved for ASF implementation.

10/06/2005

Page 7 - add 0-Ohm jumper Installed for DDR_THERM#.

Page 22 - At U23B.G6, add 0-Ohm jumper to +S1_VCC. Change R829 to 0-Ohm and NI R829.

Page 24 - Change U44 from AT24C512N (512kB) to AT24C64A which is a 64kbit EEPROM.

10/07/2005

Page 18 - Change U39.5 and U40.5 to +3VALW.

Page 24 - Add 4.7kOhm pulldown to GND on LOM_LOW_PWR U6A.J5 andNI U43.

Page 24 - Change R865.1 rail to +3VALW

10/11/2005

Page 20 - modify R522 from 10K to 100k and the rail from V_3P3_LAN to +3VALW

Page 24 - Install 4.7kOhm Pullup Resistors to +V_3P3_LAN at R1013.2 and R1014.2.

Page 25 - Change R871 to 10K-Ohm.

11/10/2005

Page 15 - Reserve the workaround circuit for MAXIM IC issue.

Page 20 - Swap PANEL_FLIP# from GPIO39 to GPIO12 and add a pull-up resistor.

11/14/2005

Page 17,20,29 - Change USB20_P1, N1 to No Connects. Connect USB20_P2,N2 to Fingerprint. Change JP11.2 and JP11.4 from USB20_N2/P2 to USB20_N5/P5 respectively. Swap USB_OC#5 and USB_OC#2.

Page 25 - Add 4x 12nF 100V capacitor placeholders at R269.2, R270.2, R271.2, and R272.2.

Page 28 - Add the R1034(1Kohm) and the R995(0Ohm) between EAPD and EAPD#. Change net name from EAPD# to MUTE_LED#.

11/15/2005

Page 20 - Move LP_EN# from GPIO27 (U28C.B21) to GPIO8 (U28C.E21). Make U28C.B21 a Test Point.

Page 24 - AF30 have black screen issue when AC plug-in(LP_EN# inactive).
This issue is caused by PLT_RST# dropped to 1.12V.
Change R1007 from 0 ohm to 220K ohm for solving this issue.
Add R1025 (10k ohm) in PLT_RST#_LAN.

11/17/2005

Page 24 - Add C1044 (0.1uF cap.) to GND at Q57.2.

Page 25 - Change C1040, C1041, C1042, C1043 in series with R269-2, R270-2, R271-2, and R272-2.
INSTALL C1040, C1041, C1042, and C1043. Remove C934.
Connect C320 to R269-1, R270-1, R271-1, and R272-2.

11/18/2005

Page 25 - Change C1040,C1041,C1042,C1043 value from 12nF to 10nF.

Page 24 - Change Q103.1 net name to LOM_PCIE_WAKE#.

Page 20 - Change Q77.3 net name to LOM_PCIE_WAKE# and disconnect from R796.1.
Install R796 and give R796.1 net name PCIE_WAKE#.

Page 24 - Change C1044 to no stuff.

11/22/2005

Page 24 - NI C826,R859,C828,R1017, R1016, R1018, R1020 and Q105.
Reverse Q103.1 to LAN_WAKE# and Q103.3 to LOM_PCIE_WAKE#.
NI R1021 and Install R1022. +3VS should be powering this Schmidt Trigger.
Remove R1023, we don't need this option. Connect NIC_PD_N to D63.1 directly.
At Q86.1, add 0-Ohm(R1037) Installed option and call output NIC_PD_N.
Add Option 10K ohm(R1036) Pullup at Q86.1 but NI and pull-up to V_3P3_LAN.
Add a NI Zener Diode RB751V_SOD23(D64) in parallel with R1007.

11/23/2005

Page 21 - Change C753 to 220uF 6.3V.

Page 17 - Change the LCD Power Circuit from AF and Caymus.
Delete R12,R474 and C28. Add R1038,R1039 and C1045. No install C20.
On JP28.40, add 0-Ohm jumper on DIGI_SLEEP.

Page 18 - Change U39.5 and U40.5 to +3VS. Install R742 and NI R741.

Page 19 - Remove R984 and disconnect from +3VS. Make U28A.AA5 a TP.

Page 20 - Change R522.2 to V_3P3_LAN.

Page 33 - Add function board ESD solution. Add C1046,C1047 and D65.

11/24/2005

Page 17 - Add 0-Ohm Jumper on JP28.18 also (DIG_RESET).

Page 20 - Change R522.2 to +3VALW.

Page 34 - Change R529 to 220K and at node SLP_S5#_5R add 2N7002 FET (NI) pin 1, pin 3 to GND, and Pin 2 output should have 1uF 10V Cap to GND NI, and 22KOhm series NI. Connect output of 22K to PREP#.

Page 20 - Add LANLINK_STATUS# isolation circuit.Cange U26C.R4 (GPIO14) to LANLINK_STATUS#_SB.
Add 0-Ohm option NI to bypass this circuit if necessary.

Page 19 - Change C516 and C528 from 10pf to 15pf to solve the RTC issue.

Page 24 - On DC mode without LAN cable plugged, system dose not provide power for LAN chip.
So LANLINK_STATUS# will be driven low by LAN chip.
We will add isolation CKT to solve this issue.
Add R1042,R1043,R1044,R1046,Q108.

11/29/2005

Page 29 - Change C582 from 0.001uF to 0.047uF.

Page 26 - J9 short and J10 open to solve that 3.3V Aux power is not present on Mini Card slot.

12/09/2005

Page 28 - Add Q28 and delete R1034 because audio driver not ready.

Page 29 - Change C582 from 0.047uF to 1500pF.

01/04/2006

Page 6 - Reserve C625 and C629 to solve PCA Acoustic Noise .

Page 26 - Add C1049 to solve EMI issue.

Page 26 - Short J10 and un-short J9 to fix WLAN leakage.

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.		
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EE PIR list (II)

1/10/2006

Page 26 - Change J10.1 from +3VS to V_3P3_LAN to ensure that WoWLAN is supported but no leakage on DC.

1/12/2006

Page 15 - Reserve C1050, C1051 and C1052 for EMI.

Page 16 - Add L79, L80 and L81 to fix EMI issue.

Page 24 - Change RDAC R858 from 1.24kOhm to 1.21kOhm.

Page 29 - Change R513 to 1kOhm, C582 to 2200pF and C102to 220uF.

Page 33 - Reserve D66 on TP_DATA / TP CLK for EMI.

Page 33 - Add C1053 and C1054 on MOD_TIP / MOD_RING near RJ-11.

2/20/2006

Page 36 - Add the circuit for power sequence timing between +1.5VS and VCCP.

Compal Electronics, Inc.	
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Version Change List (P. I. R. List) for Power Circuit

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	44	ADP_OCP	7/29	HP	PC212 change from 2200pF to 0.22uF	PC212 change from 2200pF to 0.22uF	
2	44	ADP_OCP	7/29	HP	PR416 change from 10K to 3.3K	PR416 change from 10K to 3.3K	
3	44	ADP_OCP	7/29	HP	PR449 change from 3.3K to 10K	PR449 change from 3.3K to 10K	
4	44	ADP_OCP	7/29	HP	PC211 change from 2.2uF to 10U_0805_6.3V6M	PC211 change from 2.2uF to 10U_0805_6.3V6M	
5	41	1.05V/1.8VP	10/3	Intel	Intel modify DDR2 spec can not less than 1.75V.	Modify 1.8VP soultion from fix mode to adjustable mode.	
6	39	Charger/OCP	11/14	HP	Remove PQ82 and PD46	Remove PQ82 and PD46	
7	39	Charger/OCP	11/14	HP	PR36 change from 560k to 1M.	PR36 change from 560k to 1M.	
8	44	ADP_OCP	11/14	HP	PR390 change from 27K to 3.9K_5%	PR390 change from 27K to 3.9K_5%	
9	44	ADP_OCP	11/14	HP	PC209 change from 0.22uF to 0.027uF	PC209 change from 0.22uF to 0.027uF	
10	44	ADP_OCP	11/14	HP	PR399 change from 649K to 604K	PR399 change from 649K to 604K	
11	44	ADP_OCP	11/14	HP	PC211 change from 10uF to 0.1uF X7R	PC211 change from 10uF to 0.1uF X7R	
12	44	ADP_OCP	11/14	HP	PR411 change from 47K to 10K_5%	PR411 change from 47K to 10K_5%	
13	44	ADP_OCP	11/14	HP	PR420 change from 10K to 21K_1%	PR420 change from 10K to 21K_1%	
14	44	ADP_OCP	11/14	HP	R448 change from 11.5K to 3.48K_1%	R448 change from 11.5K to 3.48K_1%	
15	44	ADP_OCP	11/14	HP	PR416 change from 3.3K to 10K_5%	PR416 change from 3.3K to 10K_5%	
16	44	ADP_OCP	11/14	HP	PR449 change from 10K to 21K_1%	PR449 change from 10K to 21K_1%	

Compal Electronics, Inc.	
Title	Changed-List History-1
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Version Change List (P. I. R. List) for Power Circuit

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
17	44	ADP_OCP	11/14	HP	Add new 47K_5% resistor in series with PR415-2	Add new 47K_5% resistor in series with PR415-2	
18	44	ADP_OCP	11/14	HP	Add new 1uF X7R capacitor from PR415-2 to GND	Add new 1uF X7R capacitor from PR415-2 to GND	
19	41	0.9VSP	01/10	Compal	Change PU9 from APL5331 to G2992F1U		
20	40	3.3V/5V	02/27	HP	WWAN noise issue	Add new 33pF X7R capacitor from PL6,2 to PC59 2.	
21	41	1.05V	02/27	HP	WWAN noise issue	Add new 2200pF X7R capacitor to parallel PC72	
22	41	1.05V	02/27	HP	WWAN noise issue	Change PC73 from 2200pF to 33pF X7R capacitor.	
23	41	1.5V	02/27	HP	WWAN noise issue	Add new 2200pF X7R capacitor to parallel PC138	
24	41	1.5V	02/27	HP	WWAN noise issue	Change PC138 from 2200pF to 33pF X7R capacitor.	
25	41	1.05V	02/28	HP	EMI issue	Reserve PC219 220pF X7R capacitor to parallel PC72	
26	41	1.5V	02/28	HP	EMI issue	Reserve PC220 220pF X7R capacitor to parallel PC138	