

Compal Confidential

NAWE6 Schematics Document

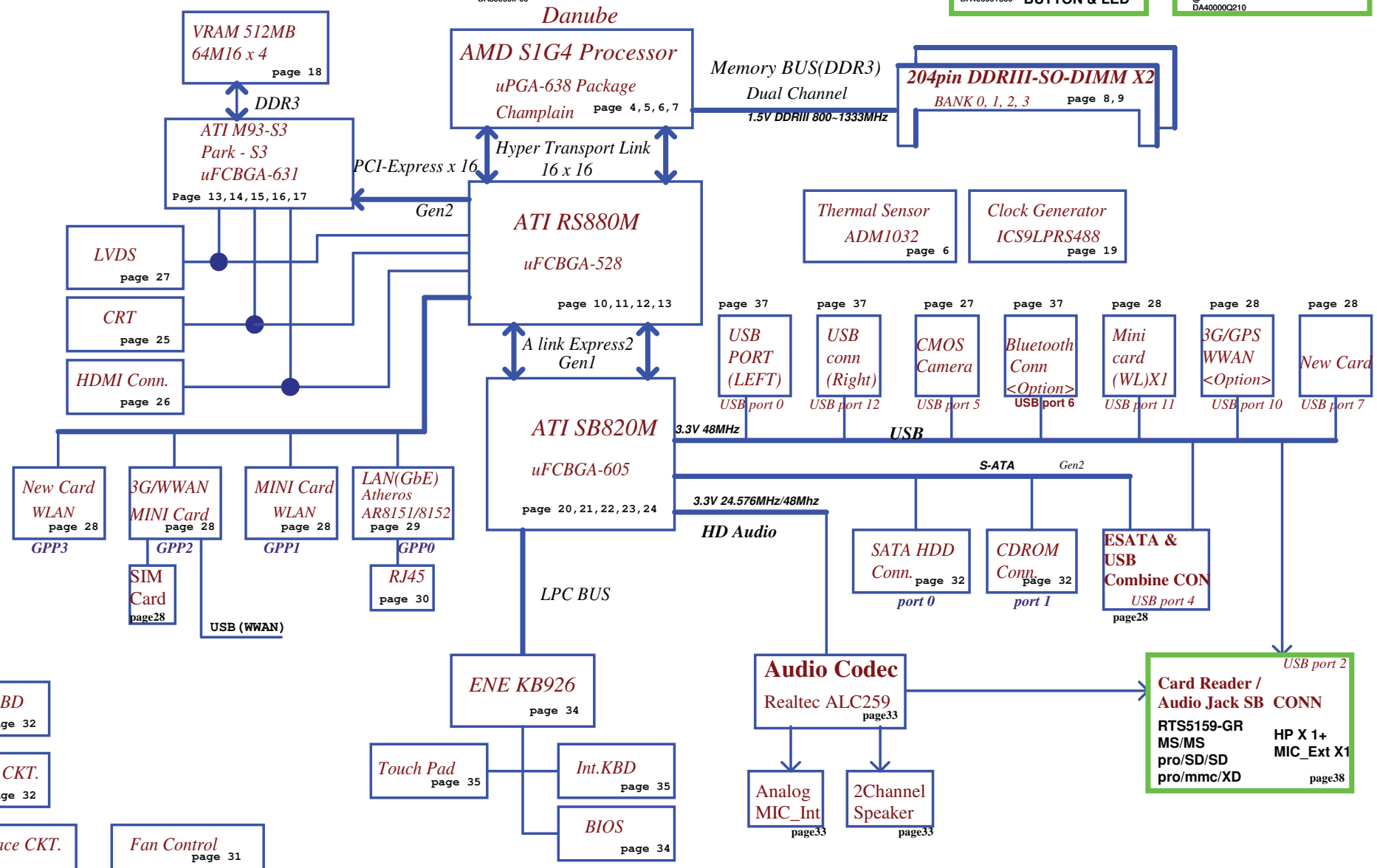
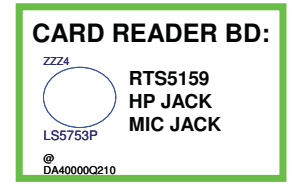
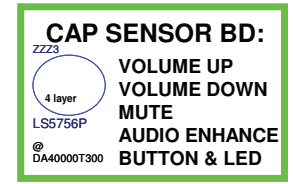
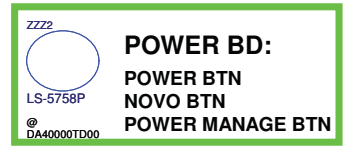
AMD Danube

Champlain Processor with RS880M/SB820/Park VGA

2010-02-24

LA5754 REV: 0.2

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Issued Date	2008/10/06	Deciphered Date	2010/03/12	Title	Cover Page
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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE_0	Core voltage for CPU (0.7-1.2V)	ON	OFF	OFF
+CPU_CORE_1	Core voltage for CPU (0.7-1.2V)	ON	OFF	OFF
+CPU_CORE_NB	Voltage for On-die Northbridge of CPU(0.8-1.1V)	ON	OFF	OFF
+0.75VS	+0.75VS LDO power rail for DDR3 VTT	ON	ON	OFF
+1.1VS	1.1V switched power rail for NB VDDC & VGA	ON	OFF	OFF
+VGA_CORE	0.95-1.2V switched power rail	ON	OFF	OFF
+1.5VS	1.5V power rail for PCIE Card	ON	OFF	OFF
+1.5V	1.5V power rail for CPU VDDIO and DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V for CPU_VDDA	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V_LAN	3.3V power rail for LAN	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	ClOCK
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts

EC SM Bus1 address

Device	Address	HEX	Device	Address	HEX
Smart Battery	0001 011X b	16H	EMC1402-1 (CPU)	100_1100b	4CH
			EMC1412-A (GPU)	111_1100b	7CH
			EMC1403-2 (DDR,WWAN)	100_1101b	4DH

EC SM Bus2 address

SB820 SM Bus 0 address

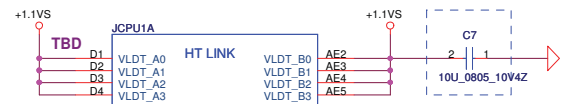
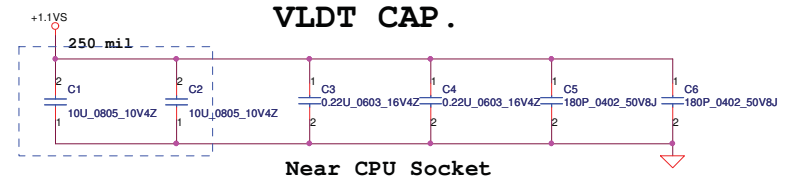
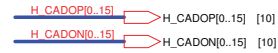
Device	Address	HEX	Device	Address
Clock Generator (SILEGO SLG8SP626)	1101 001Xb	D2		
DDR DIMM1	1001 000Xb	90		
DDR DIMM2	1001 010Xb	94		

SB820 SM Bus 1 address

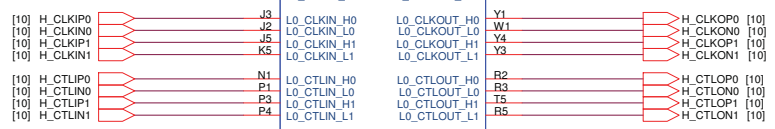
BOM Config

UMA only SKU: UMA@
DIS ONLY (Park S3): DIS@
EXT CLK Mode:EXT@
INT CLK mode:INT@
LAN GIGA: 8151@
LAN 100: 8152@
CMOS@
BT@
3G@
S@
H@

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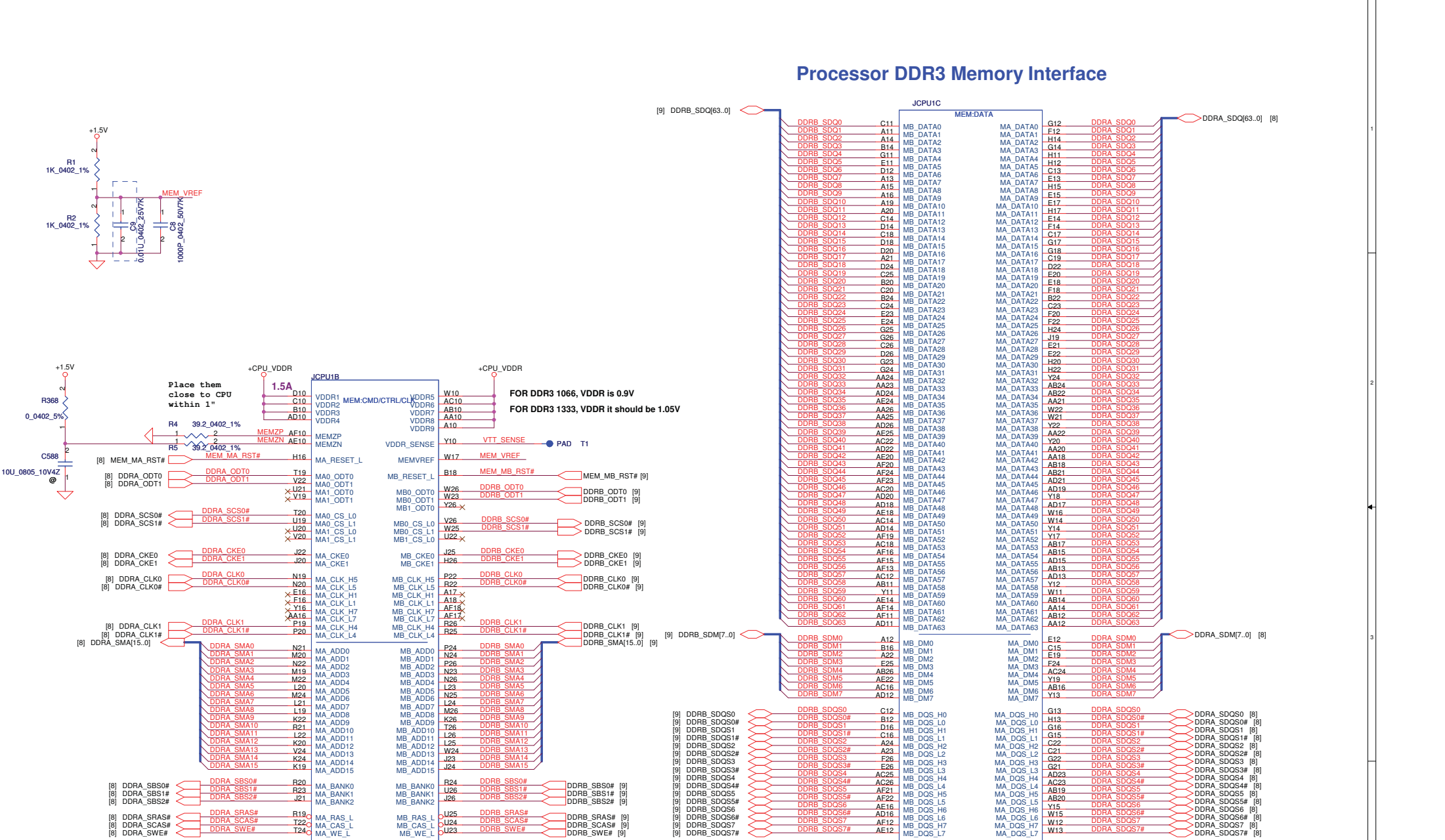
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H_CADIP1	E1	L0_CADIN_H1	L0_CADOUT_H1	AC2	H_CADOP1
H_CADIN1	F1	L0_CADIN_L1	L0_CADOUT_L1	AC3	H_CADON1
H_CADIP2	G3	L0_CADIN_H2	L0_CADOUT_H2	AB1	H_CADOP2
H_CADIN2	G2	L0_CADIN_L2	L0_CADOUT_L2	AA1	H_CADON2
H_CADIP3	G1	L0_CADIN_H3	L0_CADOUT_H3	AA2	H_CADOP3
H_CADIN3	H1	L0_CADIN_L3	L0_CADOUT_L3	AA3	H_CADON3
H_CADIP4	H1	L0_CADIN_H4	L0_CADOUT_H4	W2	H_CADOP4
H_CADIN4	K1	L0_CADIN_L4	L0_CADOUT_L4	W3	H_CADON4
H_CADIP5	L3	L0_CADIN_H5	L0_CADOUT_H5	V1	H_CADOP5
H_CADIN5	L3	L0_CADIN_L5	L0_CADOUT_L5	L1	H_CADON5
H_CADIP6	L2	L0_CADIN_H6	L0_CADOUT_H6	U2	H_CADOP6
H_CADIN6	M1	L0_CADIN_L6	L0_CADOUT_L6	U3	H_CADON6
H_CADIP7	N3	L0_CADIN_H7	L0_CADOUT_H7	T1	H_CADOP7
H_CADIN7	E5	L0_CADIN_L7	L0_CADOUT_L7	R1	H_CADON7
H_CADIP8	N2	L0_CADIN_H8	L0_CADOUT_H8	AD4	H_CADOP8
H_CADIN8	F5	L0_CADIN_L8	L0_CADOUT_L8	AD3	H_CADON8
H_CADIP9	F3	L0_CADIN_H9	L0_CADOUT_H9	AD5	H_CADOP9
H_CADIN9	F4	L0_CADIN_L9	L0_CADOUT_L9	AC5	H_CADON9
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H_CADIN10	H5	L0_CADIN_L10	L0_CADOUT_L10	AB3	H_CADON10
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H_CADIN11	H4	L0_CADIN_L11	L0_CADOUT_L11	AA5	H_CADON11
H_CADIP12	K3	L0_CADIN_H12	L0_CADOUT_H12	YS	H_CADOP12
H_CADIN12	K4	L0_CADIN_L12	L0_CADOUT_L12	W5	H_CADON12
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H_CADIN13	M5	L0_CADIN_L13	L0_CADOUT_L13	V3	H_CADON13
H_CADIP14	M3	L0_CADIN_H14	L0_CADOUT_H14	V5	H_CADOP14
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H_CADIN15	P5	L0_CADIN_L15	L0_CADOUT_L15	T3	H_CADON15



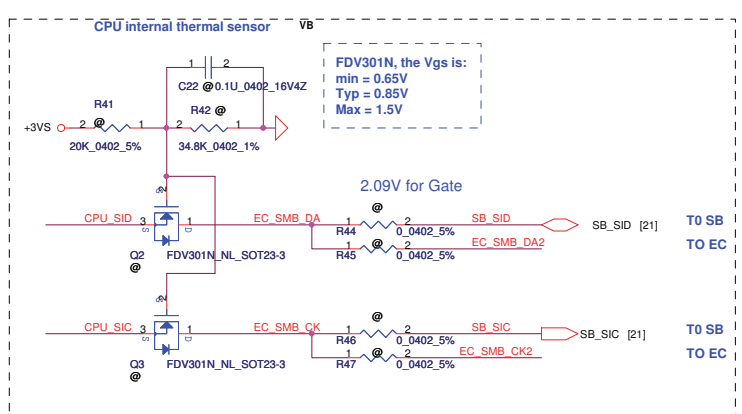
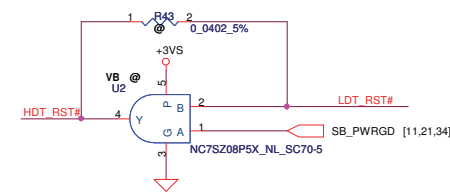
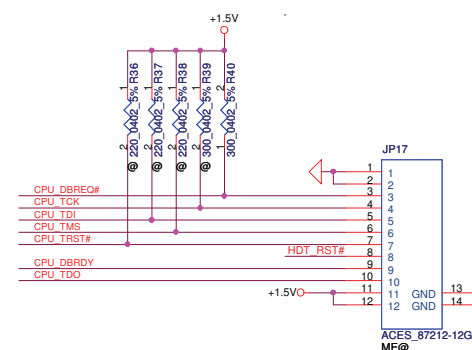
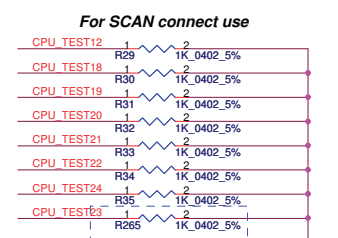
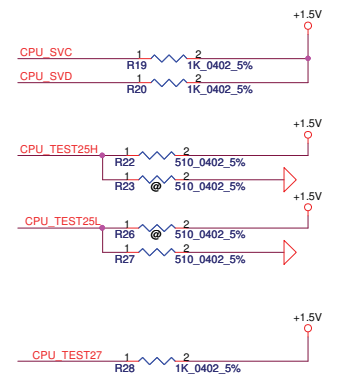
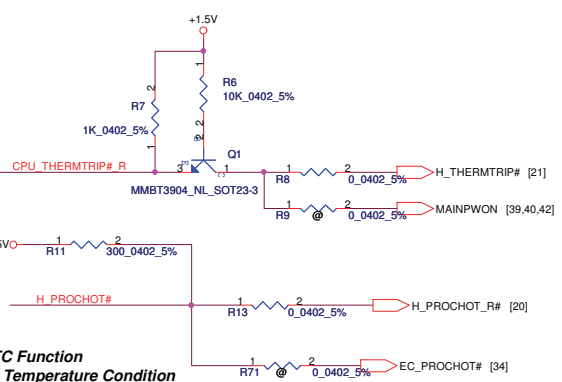
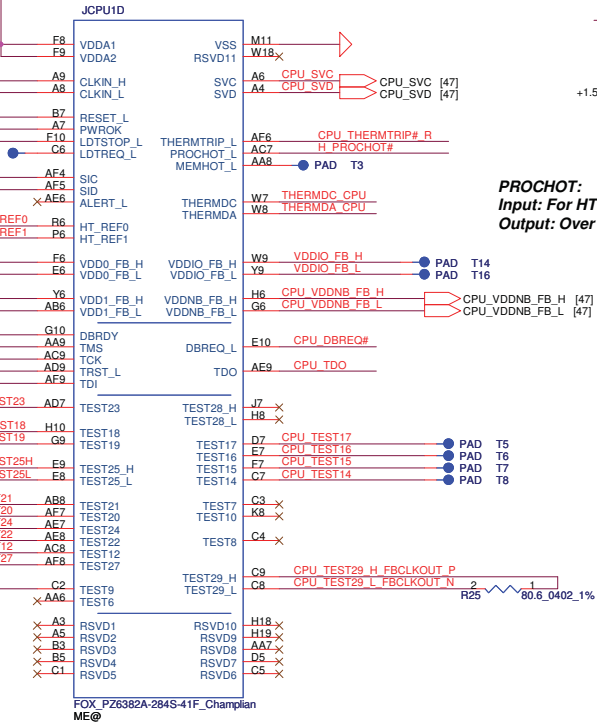
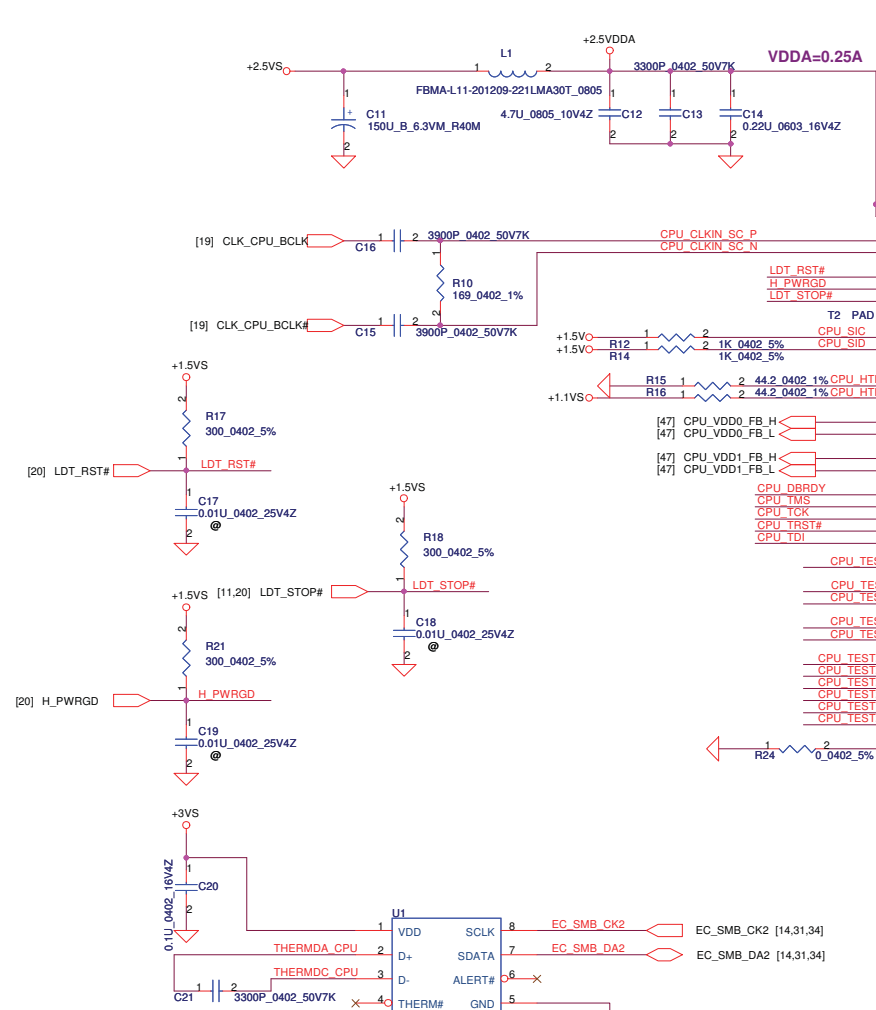
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Processor DDR3 Memory Interface



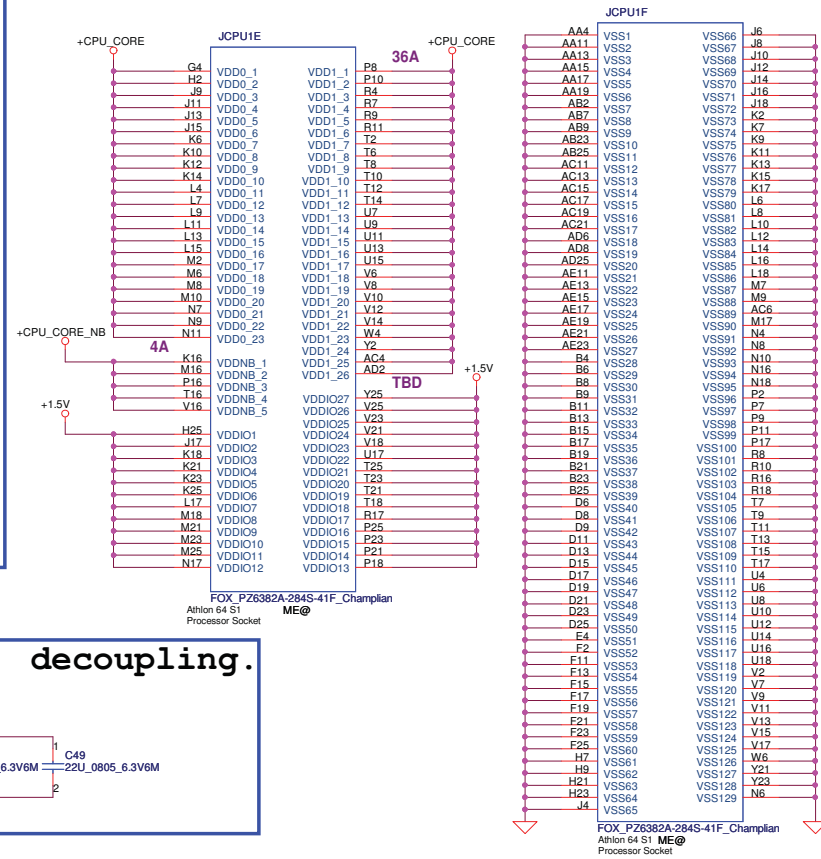
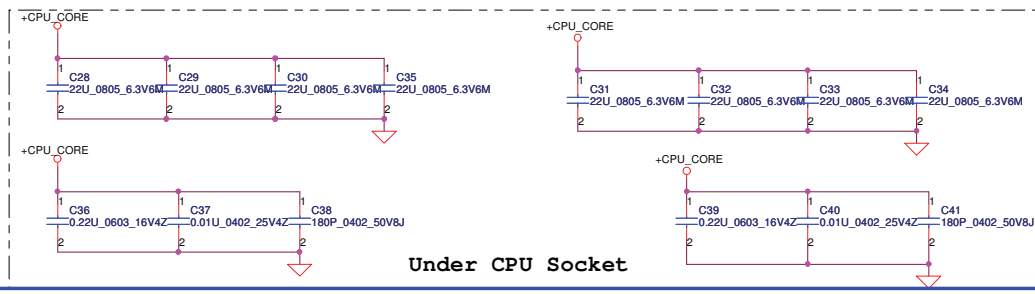
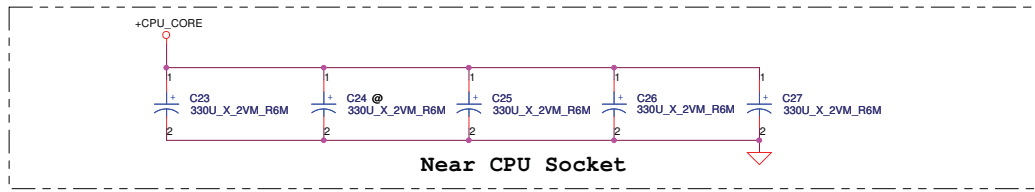
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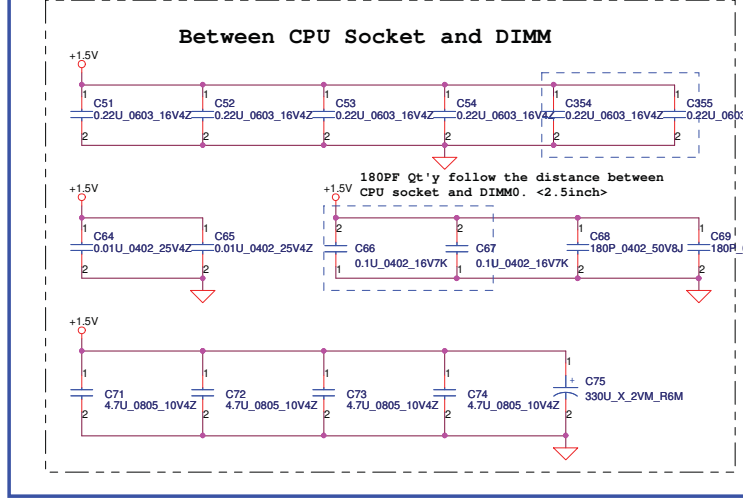
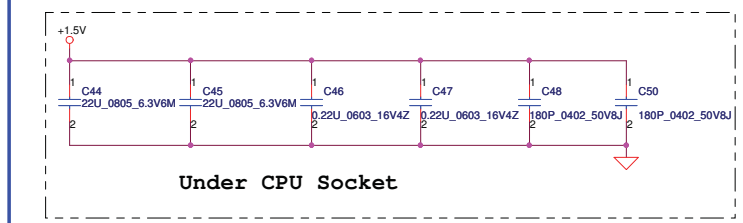
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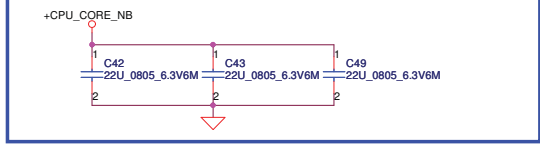
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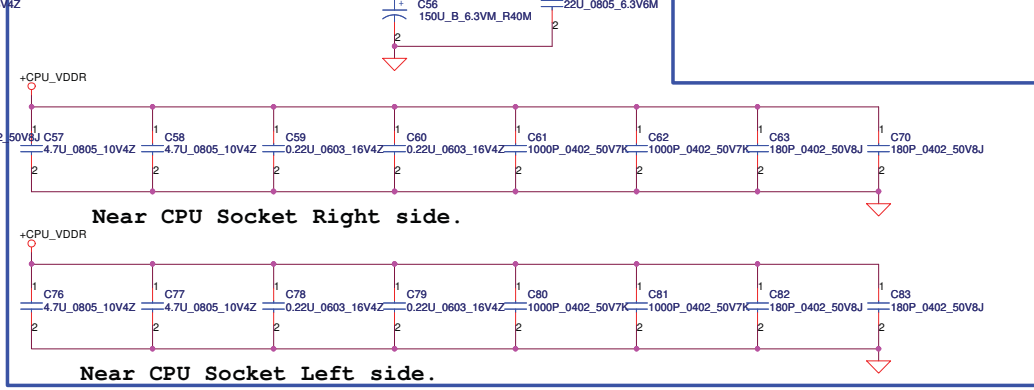
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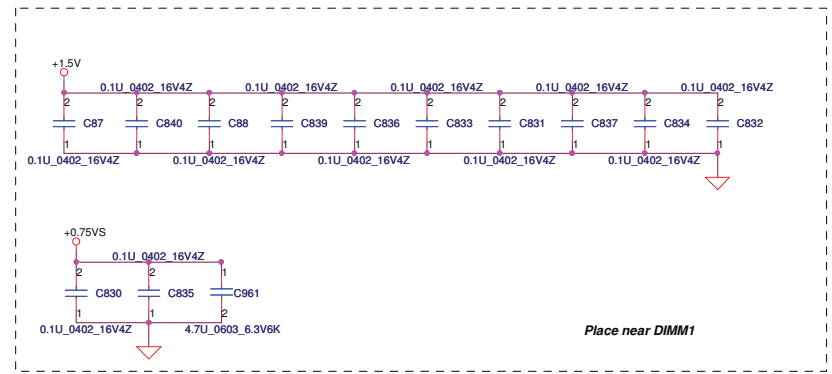
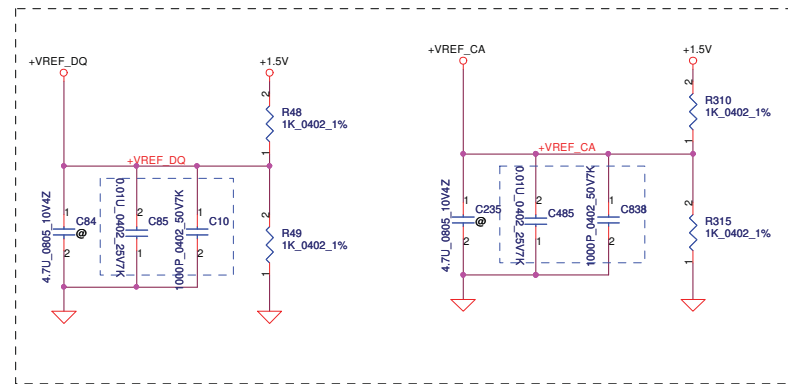
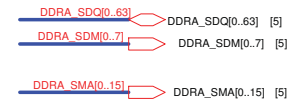
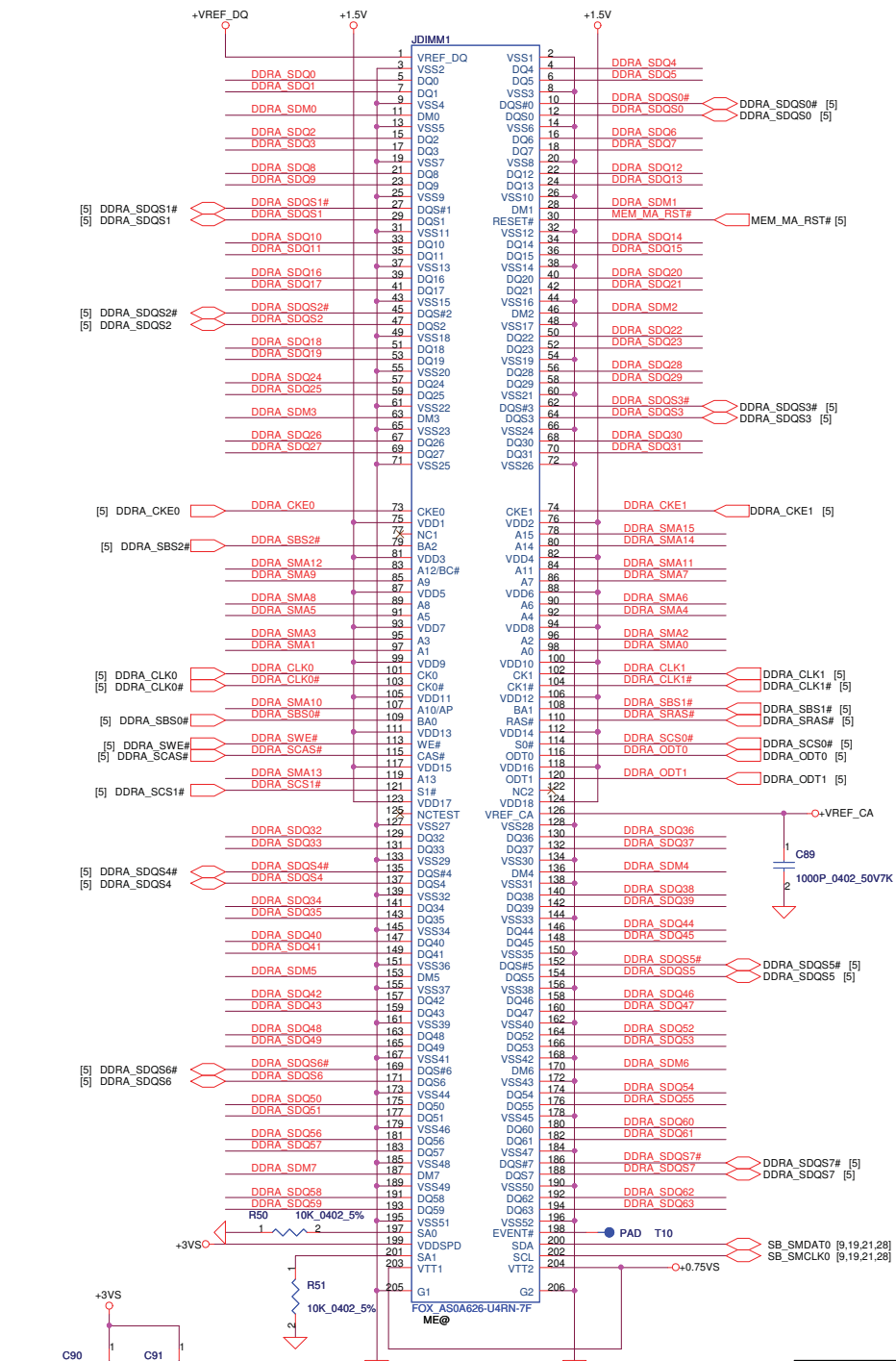
+CPU_CORE_NB decoupling.



VDDR decoupling.

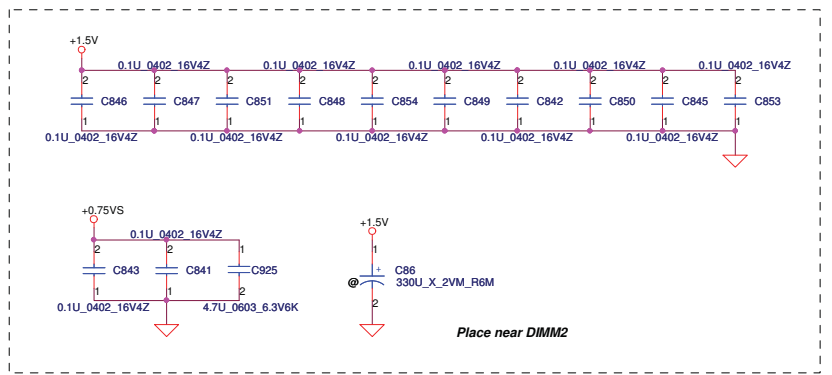
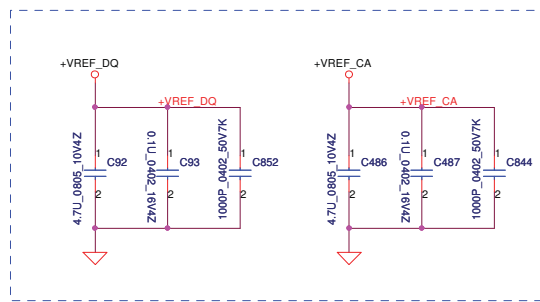
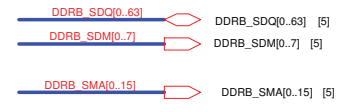
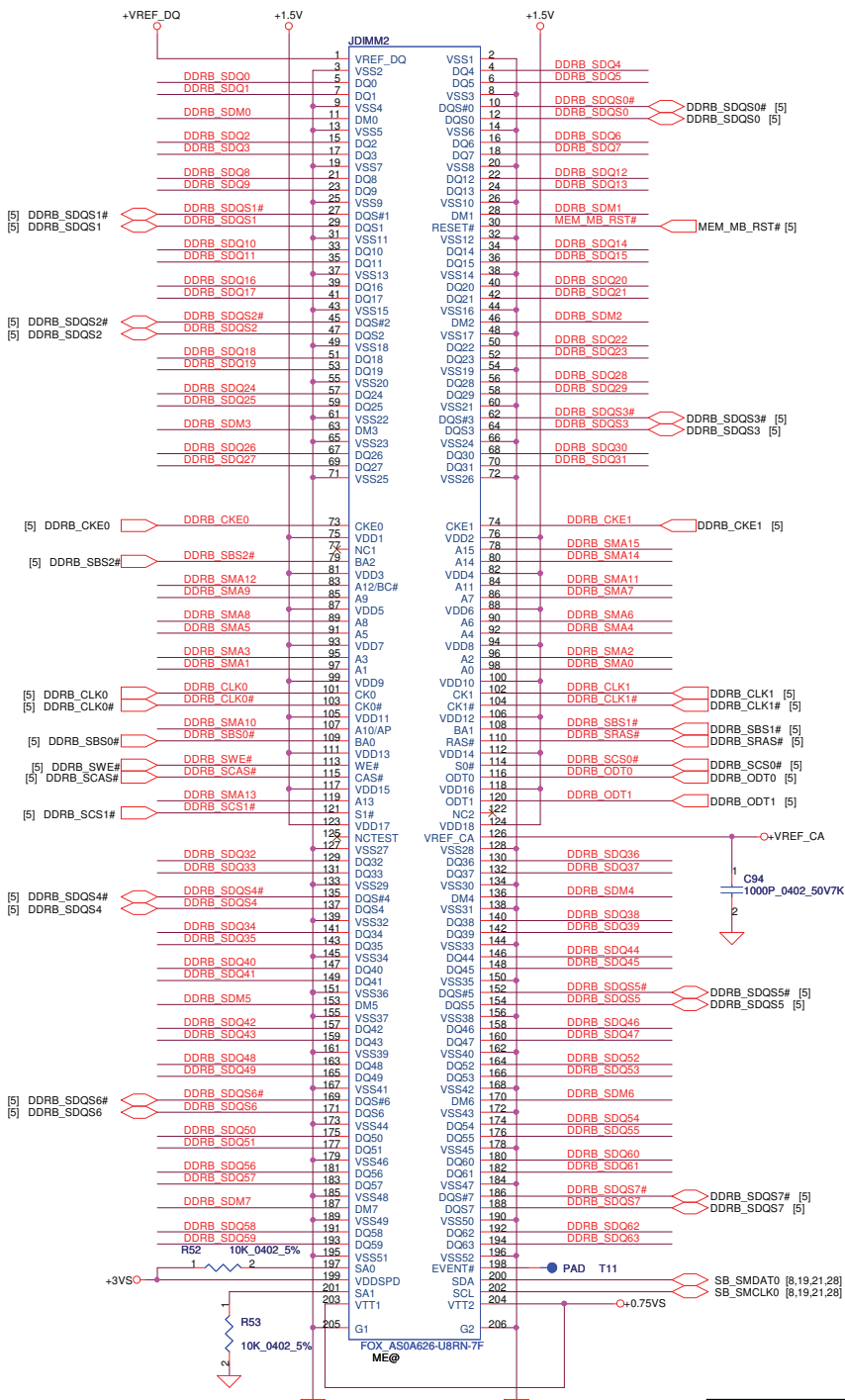


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DIMM_A Rervse H:4mm
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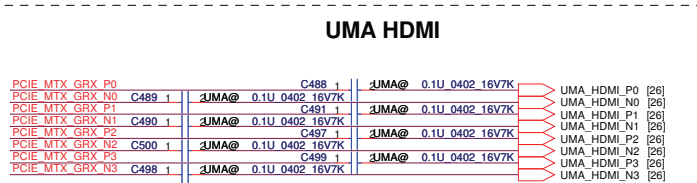


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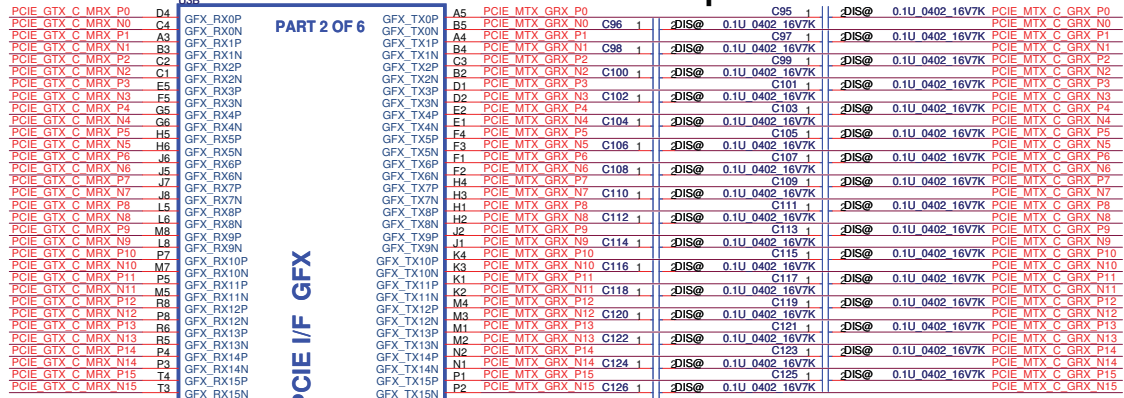
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[13] PCIE_GTX_C_MRX_P[0..15] PCIE GTX C MRX P[0..15]
 [13] PCIE_GTX_C_MRX_N[0..15] PCIE GTX C MRX N[0..15]

PCIE_MTX_C_GRX_P[0..15] PCIE_MTX_C_GRX_P[0..15] [13]
 PCIE_MTX_C_GRX_N[0..15] PCIE_MTX_C_GRX_N[0..15] [13]



Cap close NB



[28] PCIE_PTX_C_IRX_P1
 [28] PCIE_PTX_C_IRX_N1
 [29] PCIE_PTX_C_IRX_P2
 [29] PCIE_PTX_C_IRX_N2
 [28] PCIE_PTX_C_IRX_P3
 [28] PCIE_PTX_C_IRX_N3

[20] SB_RX0P
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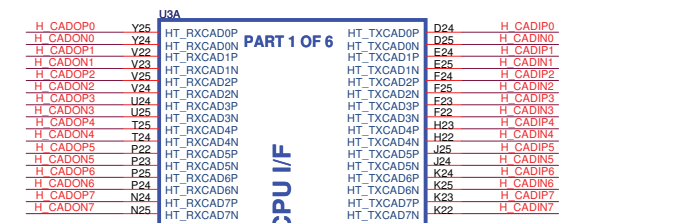
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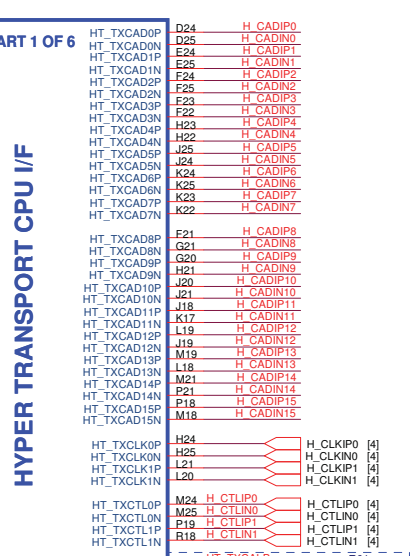
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WLAN
 GLAN
 WWAN

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 [4] H_CLKON0
 [4] H_CLKOP1
 [4] H_CLKON1

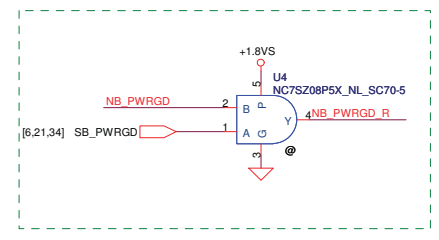
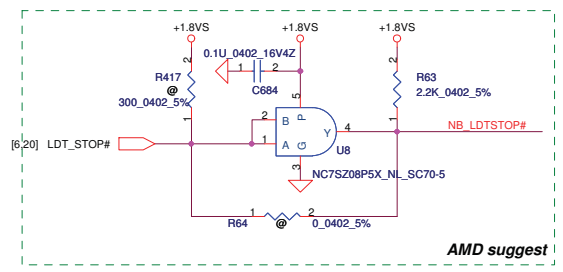
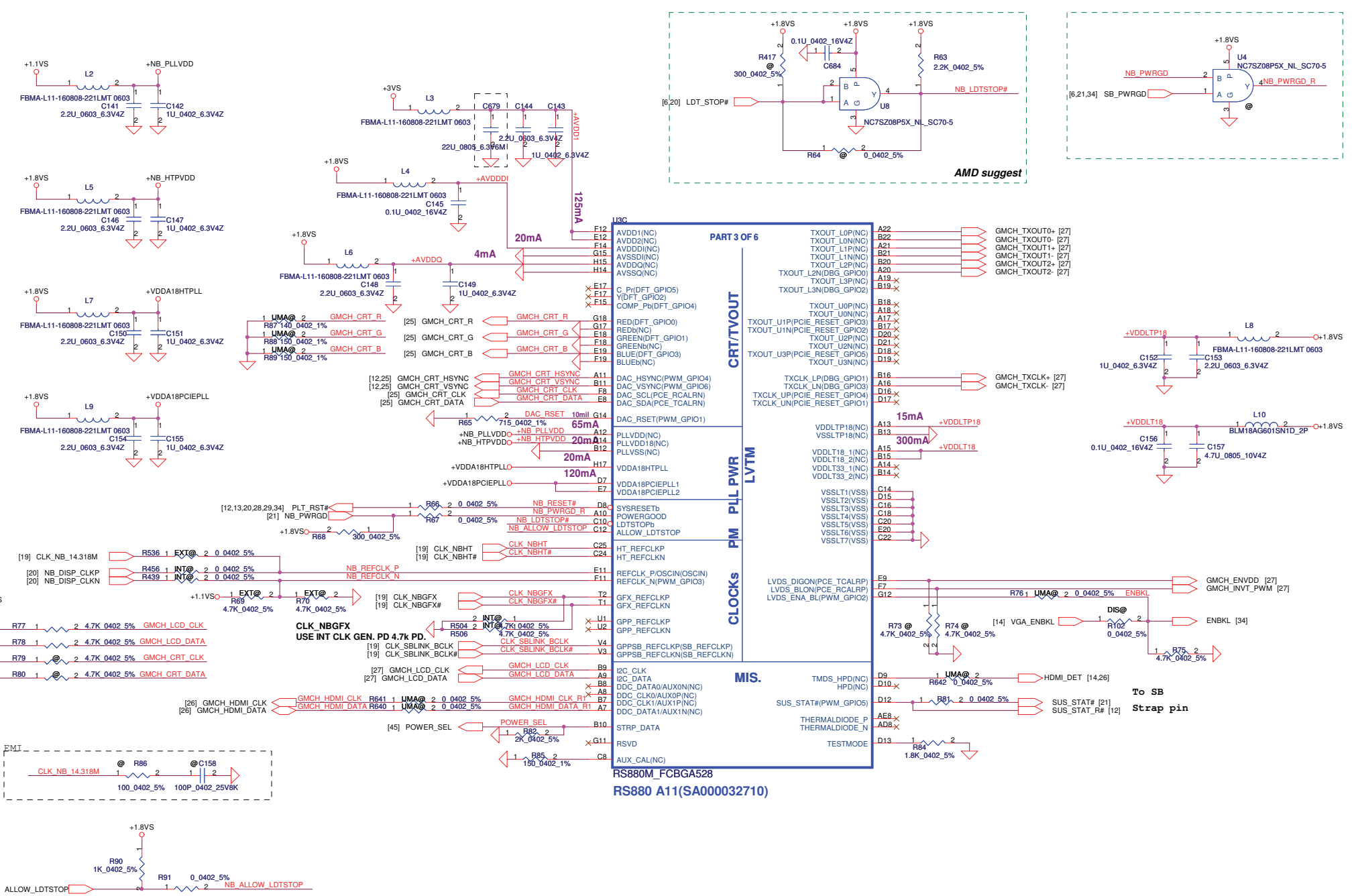
[4] H_CTLOP0
 [4] H_CTLOP1
 [4] H_CTLOP2
 [4] H_CTLOP3
 [4] H_CTLOP4
 [4] H_CTLOP5
 [4] H_CTLOP6
 [4] H_CTLOP7
 [4] H_CTLOP8
 [4] H_CTLOP9
 [4] H_CTLOP10
 [4] H_CTLOP11
 [4] H_CTLOP12
 [4] H_CTLOP13
 [4] H_CTLOP14
 [4] H_CTLOP15



HT_RXCALP
 HT_RXCALN
 HT_RXCALP
 HT_RXCALN

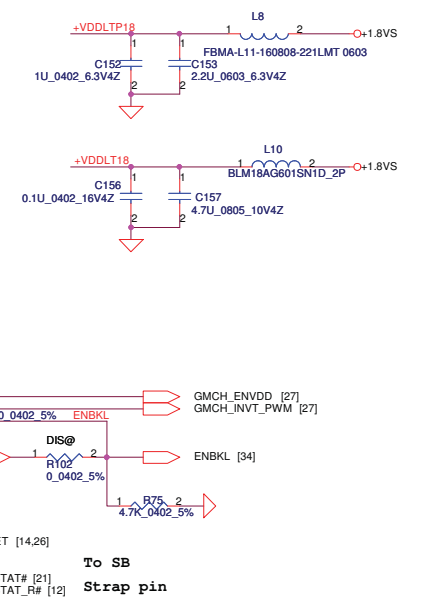
RS880 A11(SA000032710)

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RS880M_FCBGA528
RS880 A11(SA000032710)

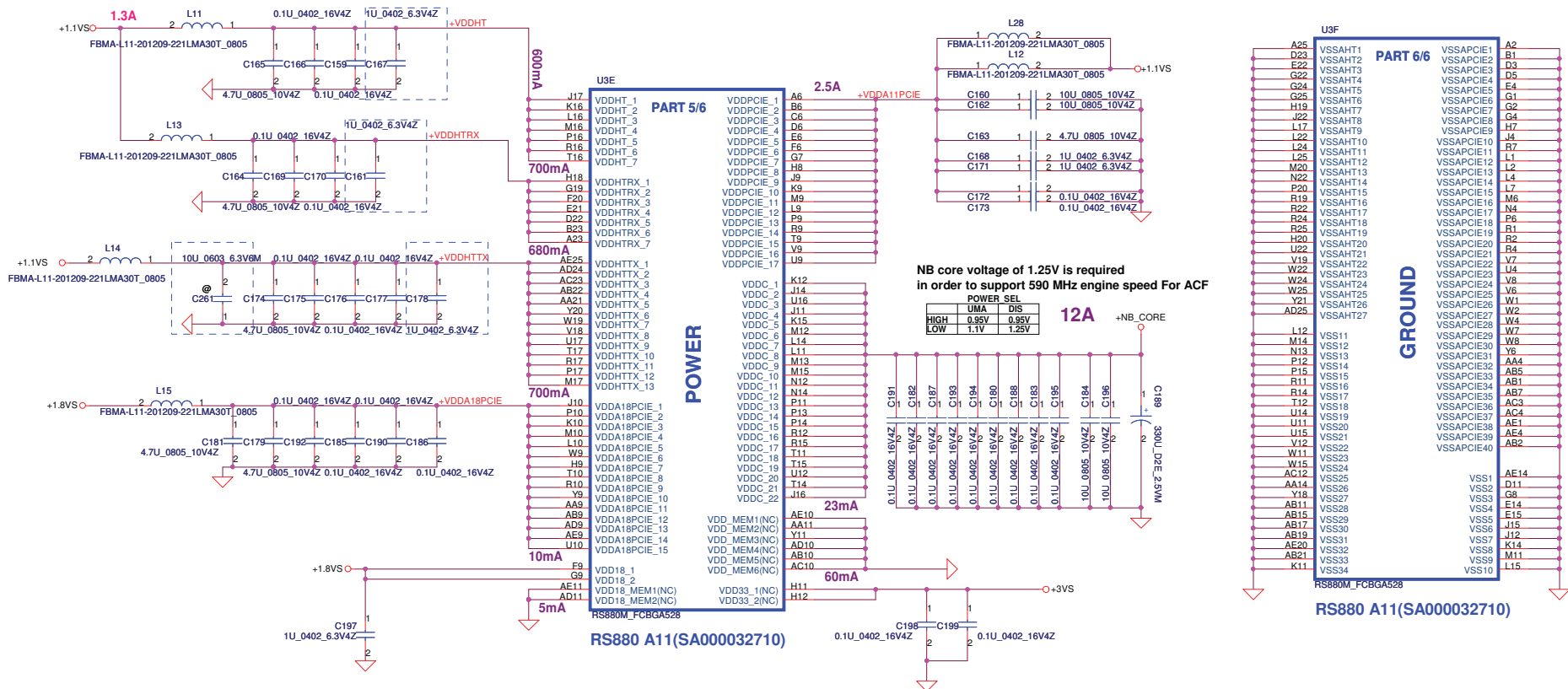
Pin	Signal Name	Notes
F12	AVDD1(NC)	
F12	AVDD2(NC)	
F14	AVDD3(NC)	
G15	AVDD4(NC)	
H15	AVDD5(NC)	
H14	AVSS3(NC)	
F17	C_P(DFT_GPIO5)	
F17	Y(DFT_GPIO2)	
F15	COMP_Pb(DFT_GPIO4)	
G18	RED(DFT_GPIO0)	
G17	RED(NC)	
F18	GREEN(DFT_GPIO1)	
F18	GREEN(NC)	
E19	BLUE(DFT_GPIO3)	
F19	BLUE(NC)	
A11	DAC_HSYNC(PWM_GPIO4)	
B11	DAC_VSYNC(PWM_GPIO6)	
F8	DAC_SCL(PCE_RCALRN)	
E8	DAC_SDA(PCE_TCALRN)	
G14	DAC_RSET(PWM_GPIO1)	
A13	VDDLTP18(NC)	
B13	VSSLT18(NC)	
A15	VDDLTP18	15mA
B15	VDDLTP18	300mA
A14	VDDLTP18	
B14	VDDLTP18	
C14	VSSLT1(VSS)	
D15	VSSLT2(VSS)	
C16	VSSLT3(VSS)	
C16	VSSLT4(VSS)	
E20	VSSLT5(VSS)	
C22	VSSLT6(VSS)	
C22	VSSLT7(VSS)	
E9	LVDS_DIGON(PCE_TCALRP)	
F7	LVDS_BLON(PCE_RCALRP)	
G12	LVDS_ENA_BL(PWM_GPIO2)	
D9	TMD5_HPD(NC)	
D10	HPD(NC)	
D12	SUS_STAT#(PWM_GPIO5)	
AE8	THERMALDIODE_P	
AD8	THERMALDIODE_N	
D13	TESTMODE	



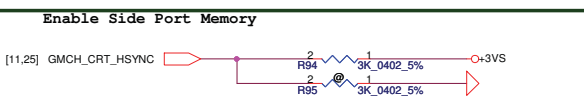
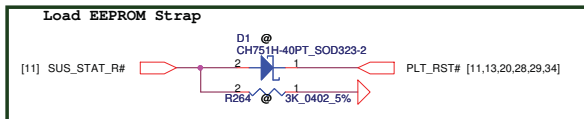
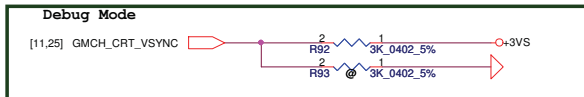
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Issued Date	2008/10/06	Deciphered Date
		2010/03/12

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Title	
RS880 VEDIO/CLK GEN	
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Side port and Strap setting



DFT_GPIO5:STRAP_DEBUG_BUS_GPIO_ENABLED

Enables the Test Debug Bus using GPIO. (VSYNC)

1 : Disable
0 : Enable

DFT_GPIO1: LOAD_EEPROM_STRAPS

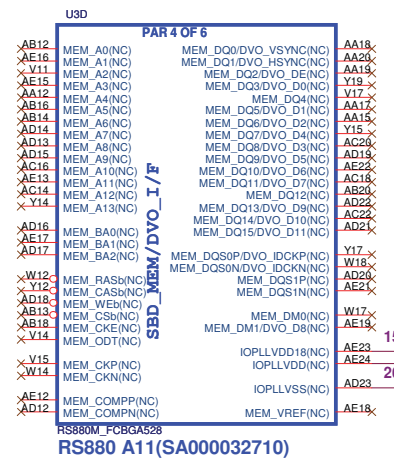
Selects Loading of STRAPS from EPROM

1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

Enable Side Port Memory

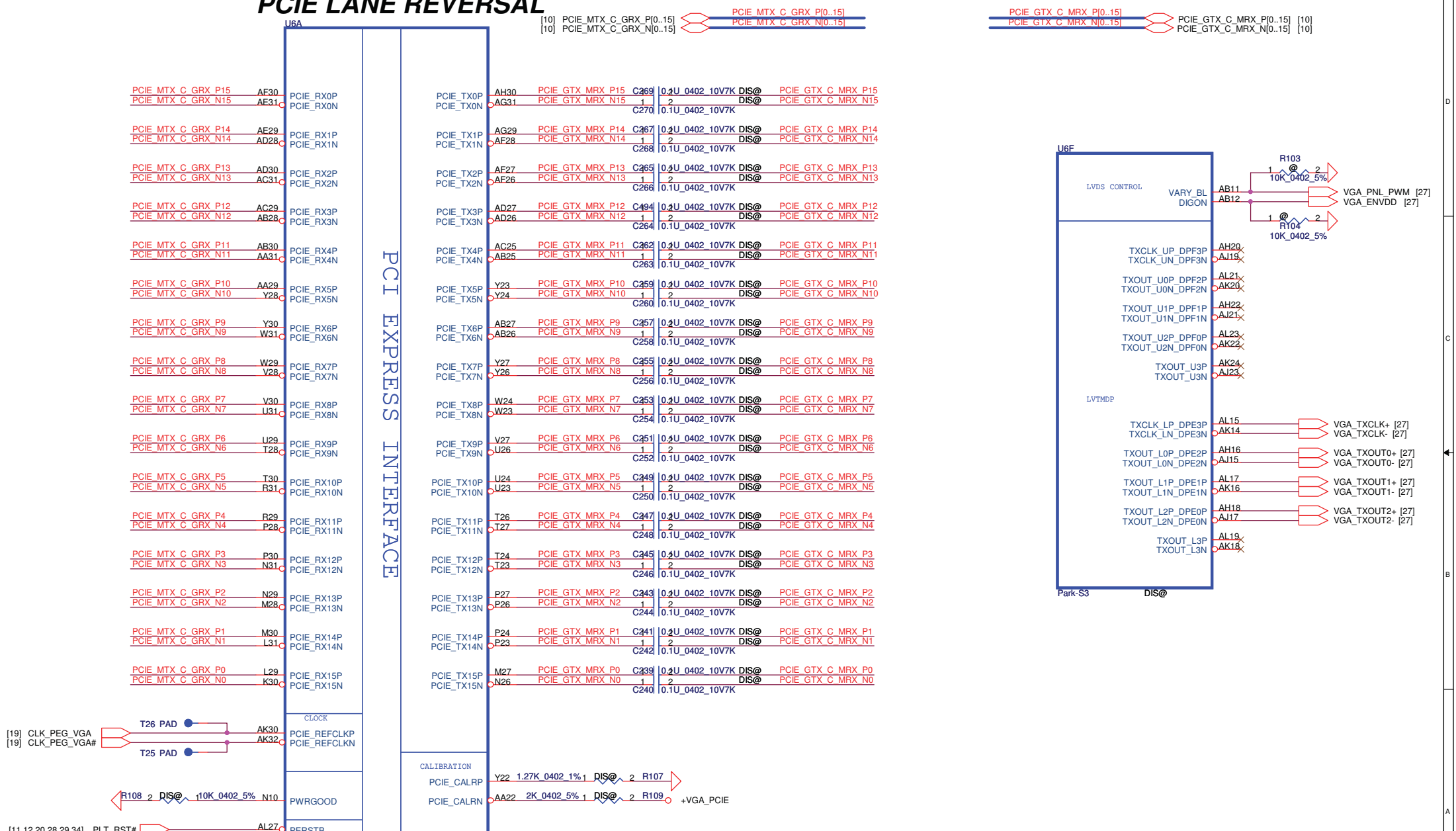
RS880: HSYNC# Register Readback of strap:
0: Enable
1: Disable

NB_CLKCFG:CLK_TOP_SPARE_D[1]

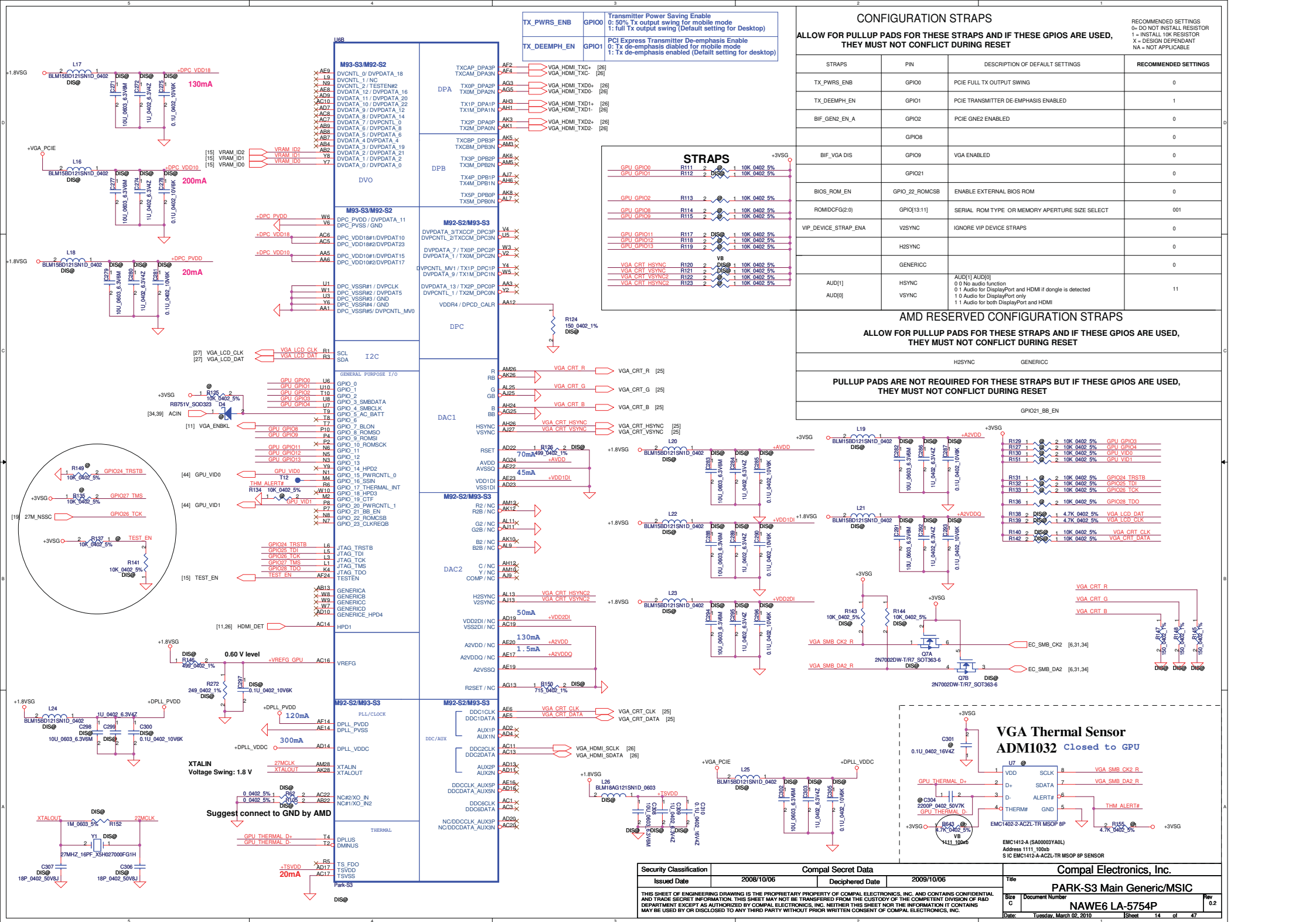


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<p>Customer</p>			<p>Document Number</p> <p>NAWE6 LA-5754P</p>	
<p>Date</p> <p>Monday, March 01, 2010</p>			<p>Rev</p> <p>0.2</p>	
<p>Sheet</p> <p>12 of 47</p>				

PCI EXPRESS REVERSAL



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TX_PWRS_ENB GPIO0 0: 50% Tx output swing for mobile mode
1: full Tx output swing (Default setting for Desktop)

TX_DEEMPH_EN GPIO1 PCI Express Transmitter De-emphasis Enable
0: Tx de-emphasis disabled for mobile mode
1: Tx de-emphasis enabled (Default setting for desktop)

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	0
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	1
BIF_GEN2_EN_A	GPIO2	PCIE GNE2 ENABLED	0
BIF_VGA_DIS	GPIO8	VGA ENABLED	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
BIOS_ROM_EN	GPIO21	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	001
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
	H2SYNC		0
	GENERICC		0
AUD[1]	HSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	11
AUD[0]	VSNC		

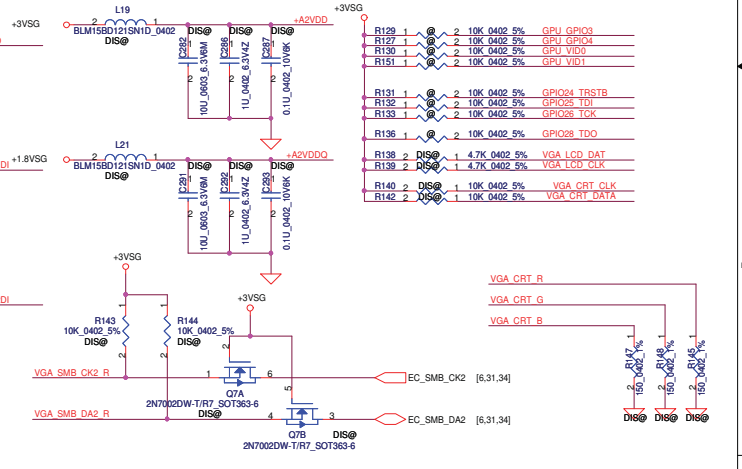
AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

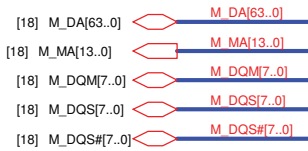
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
H2SYNC	GENERICC		

PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

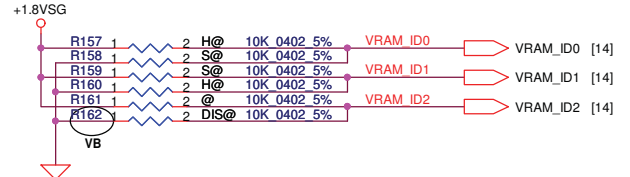
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
GPIO24_TRSTB	GPIO24		
GPIO27_TMS	GPIO27		
GPIO26_TCK	GPIO26		



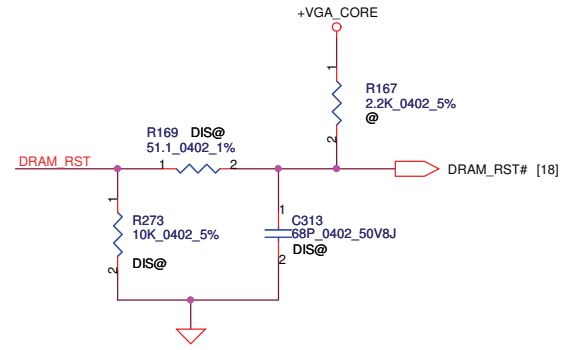
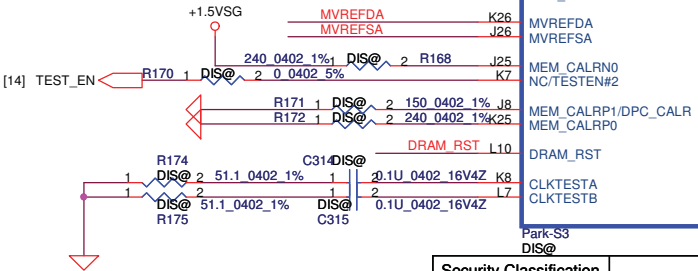
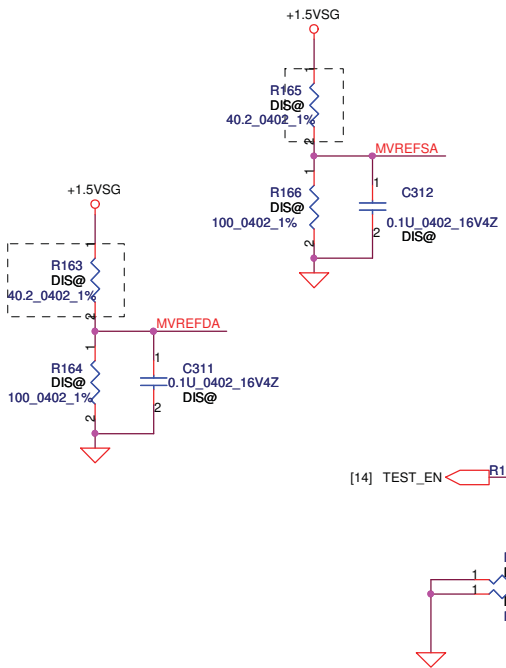
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Size C	Document Number NAWE6 LA-5754P	Rev	02
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MEMORY INTERFACE

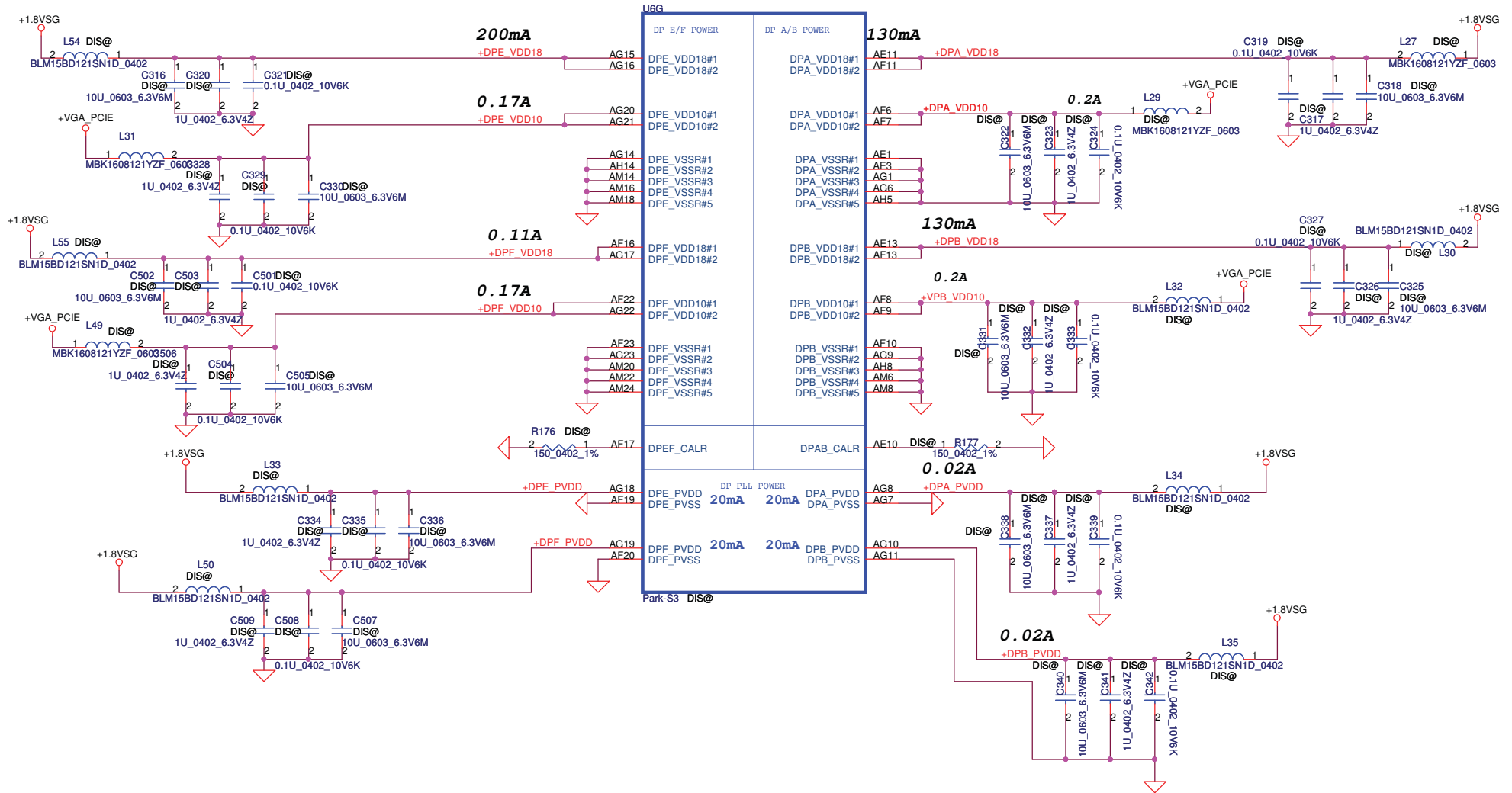


Vendor		VRAM_ID0	VRAM_ID1	VRAM_ID2
Hynix	H5TQ1G63BFR-12C	1	0	0
Samsung	K4W1G1646E-HC12	0	1	0

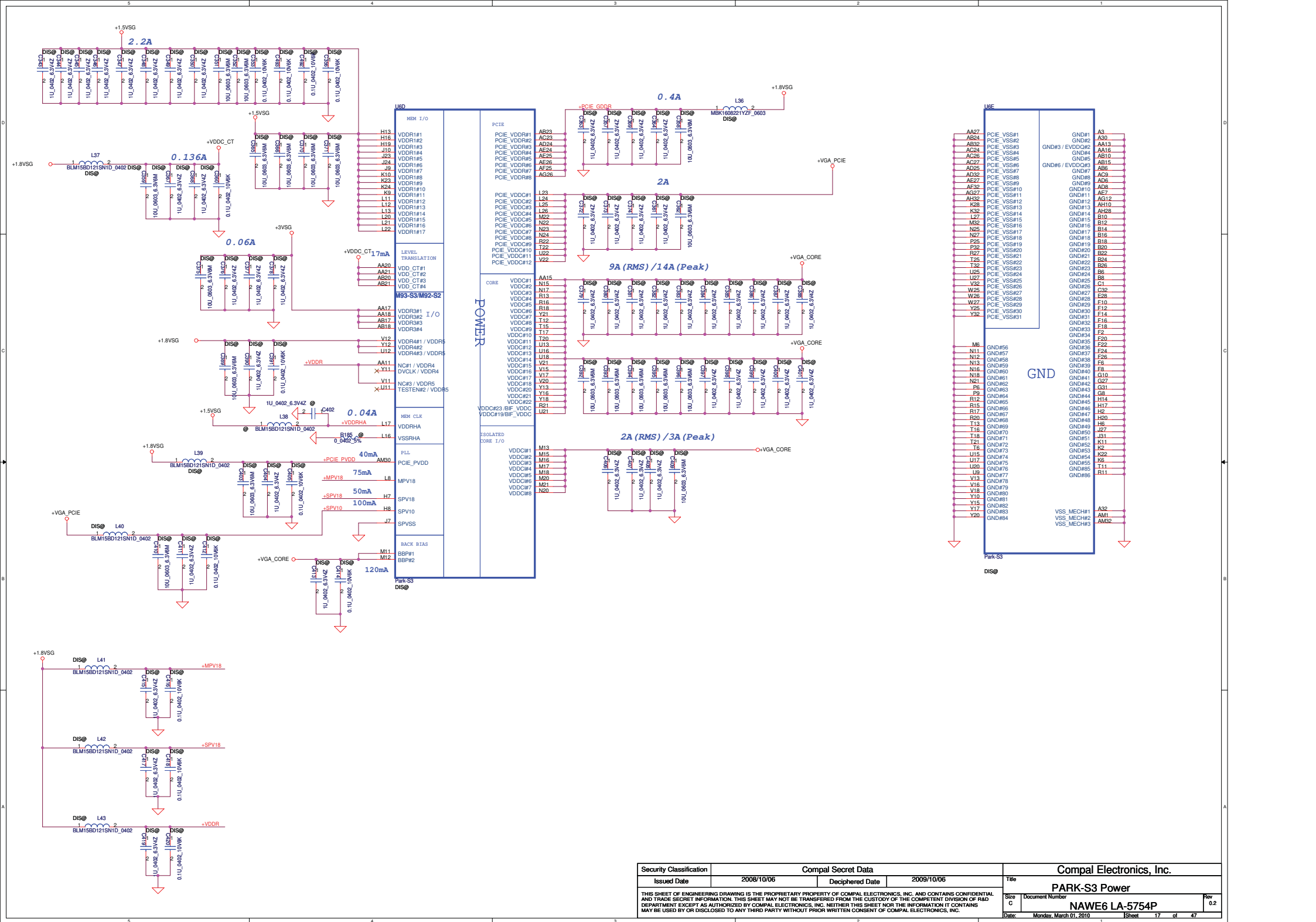


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DPE_VDD10
DFP_VDD10 Park-S3: TMD5/DP=110mA@1.0V : LVDS=120mA@1.0V

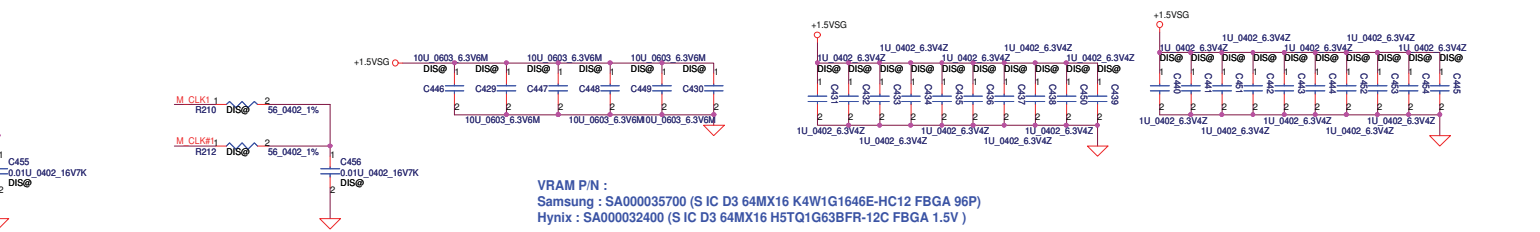
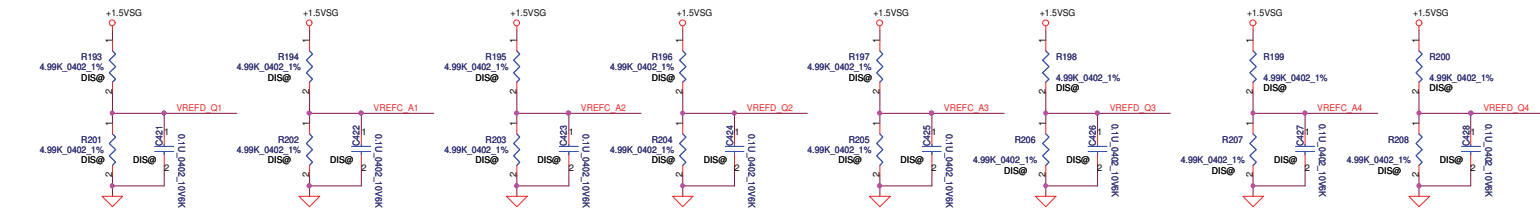
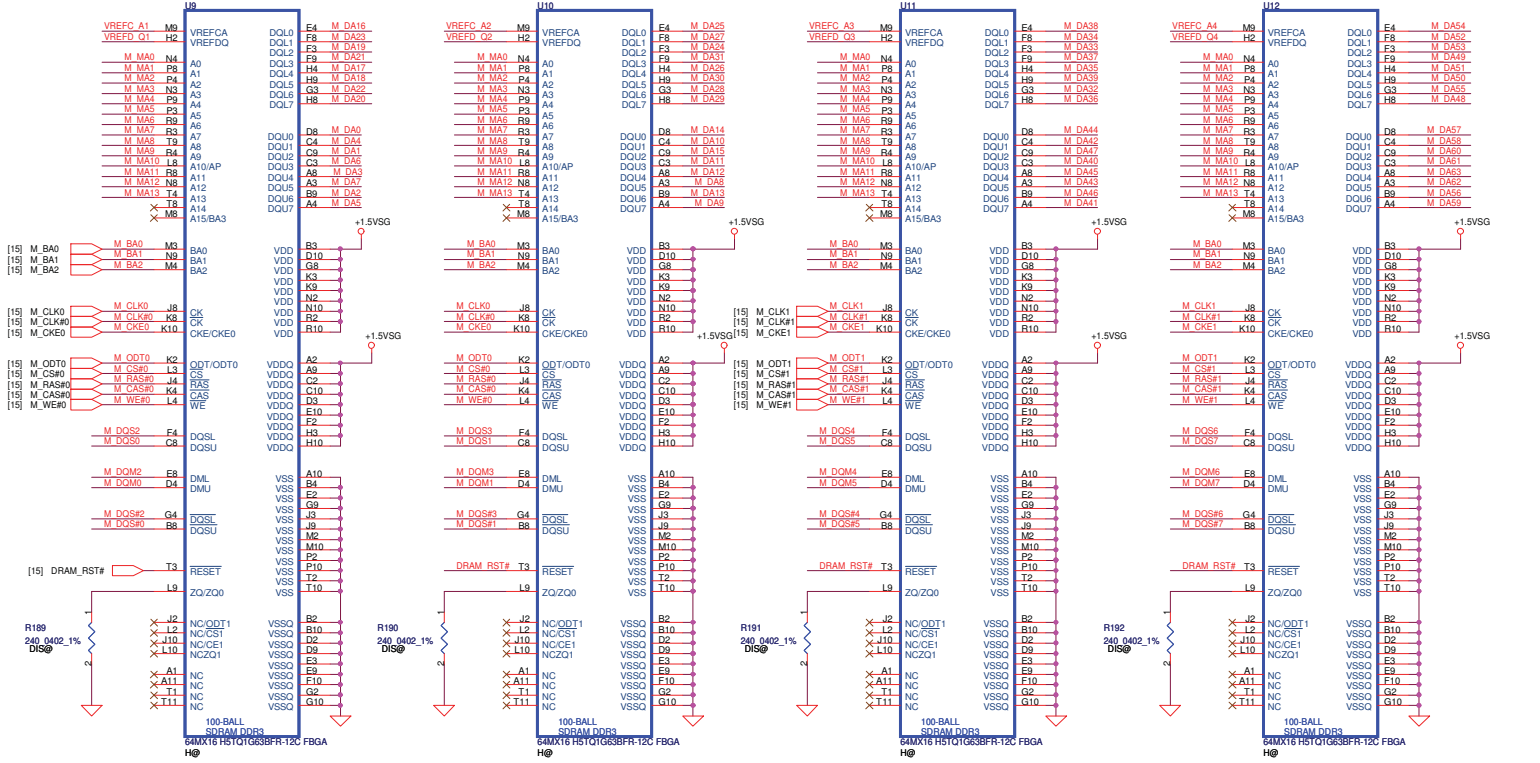


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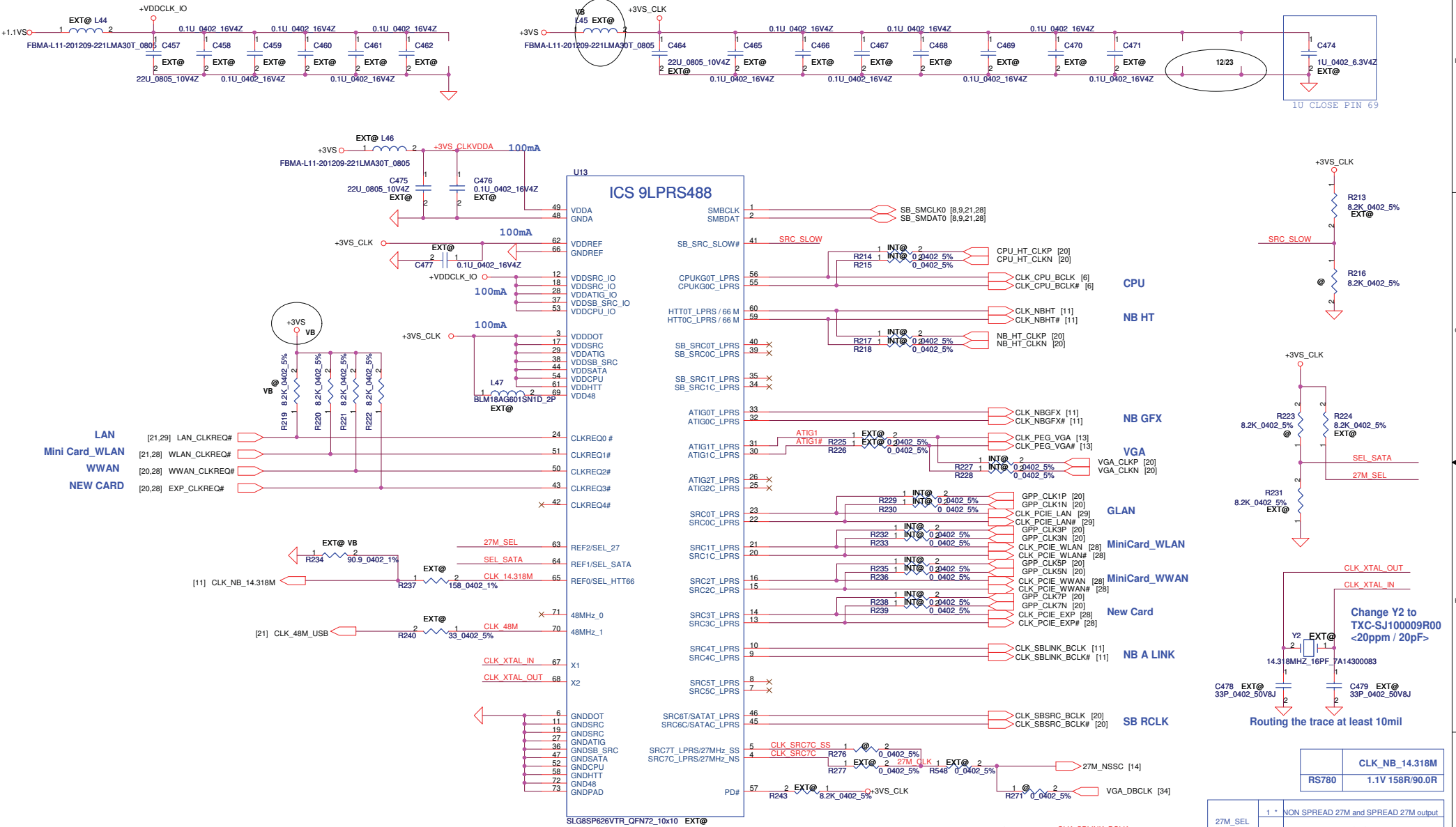
- [15] M_DA[63..0] M_DA[63..0]
- [15] M_MA[13..0] M_MA[13..0]
- [15] M_DQM[7..0] M_DQM[7..0]
- [15] M_DQS[7..0] M_DQS[7..0]
- [15] M_DQS# [7..0] M_DQS# [7..0]



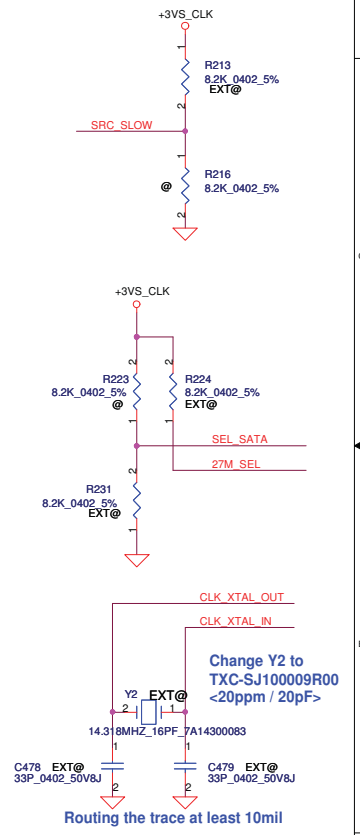
VRAM P/N :
 Samsung : SA000035700 (S IC D3 64MX16 K4W1G1646E-HC12 FBGA 96P)
 Hyunix : SA000032400 (S IC D3 64MX16 H5TQ1G63BFR-12C FBGA 1.5V)

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C		PARK-S3 DDR3 VRAM		NAWE6 LA-5754P	
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Check Timing +1.1VS <50us +3VS for EXT CLKGEN stable



1st (SILEGO) : SA00001Z310 S IC SLG8SP626VTR QFN 72P CLK GEN
 2nd (ICS) : SA000023H10 S IC ICS9LPRS488CKLFT M7F 72P CLK GEN



Change Y2 to TXC-SJ10009R00 <20ppm / 20pF>

Routing the trace at least 10mil

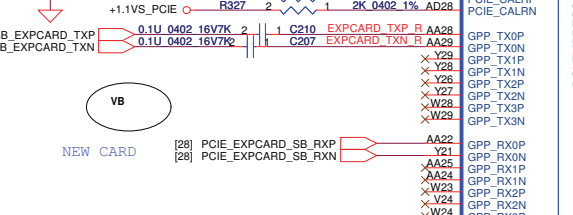
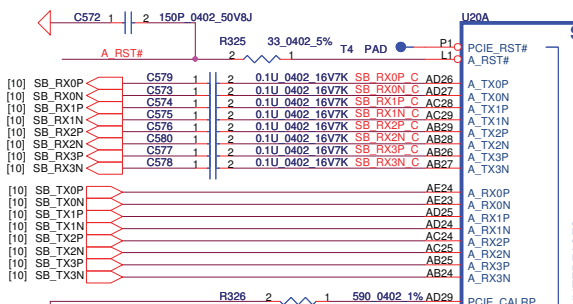
	CLK_NB_14.318M
RS780	1.1V 158R/90.0R

27M_SEL	1	NON SPREAD 27M and SPREAD 27M output
	0	differential spread SRC 7 output

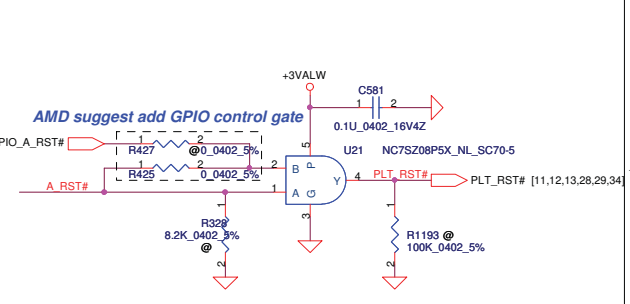
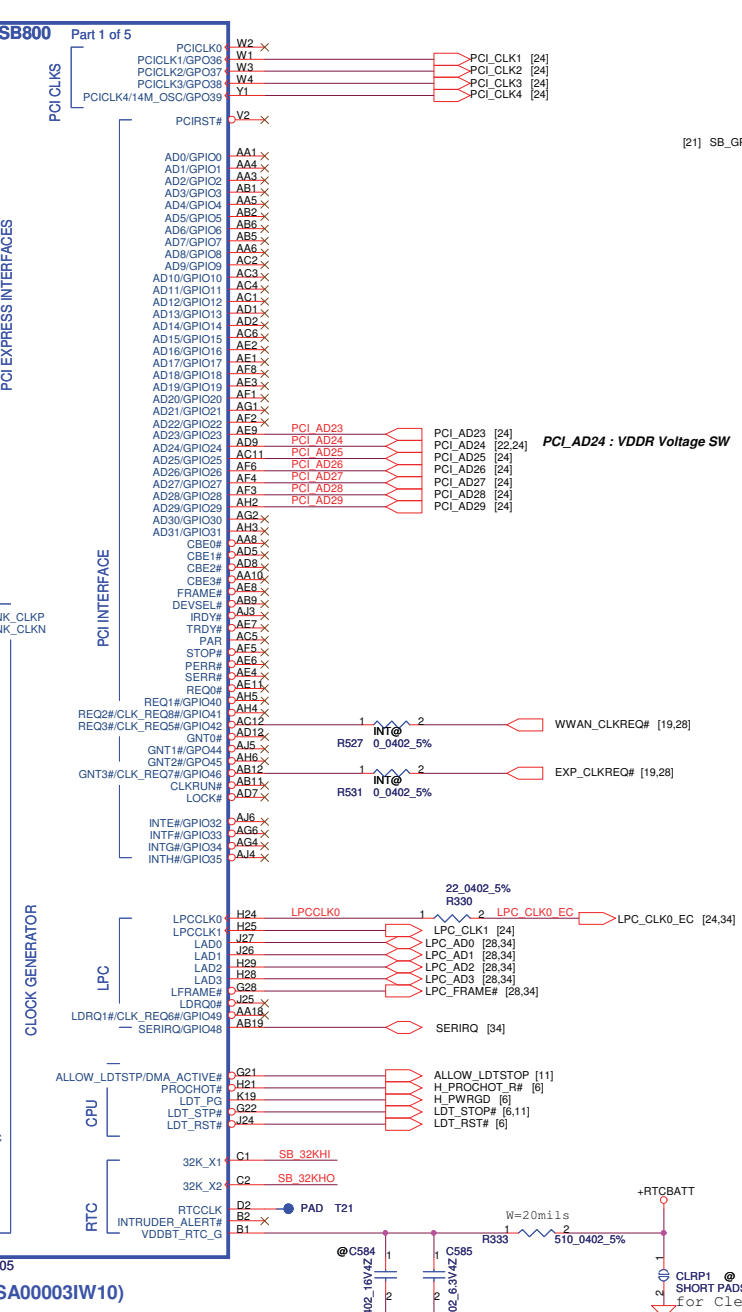
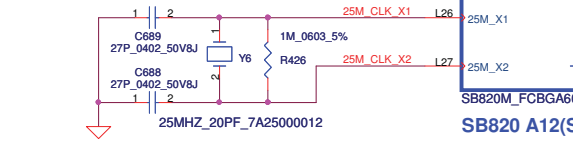
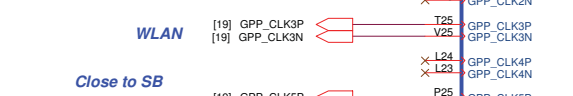
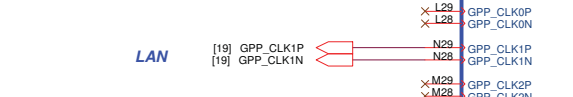
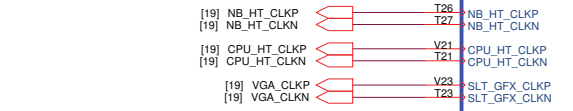
SEL_HTT66	1	single-ended 66MHz HTT output
	0	differential 100MHz HTT output

SEL_SATA	1	NON SPREAD 100M SATA SRC6 output
	0	SPREAD 100M SATA SRC6 output

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Workaround
Setting SpreadSpectrum =1
will enable spread spectrum

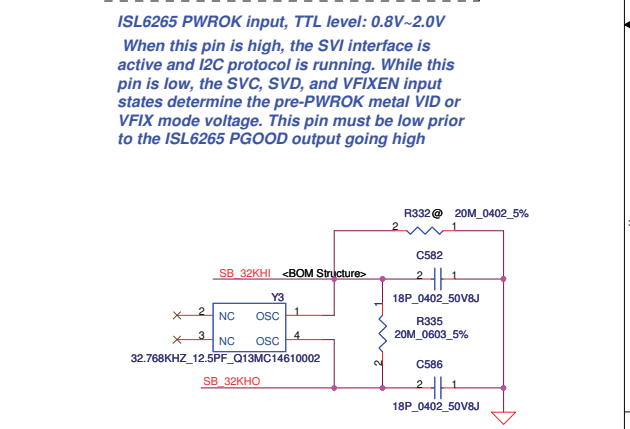


AMD suggest add GPIO control gate
Check the output status of control gate when power on!!

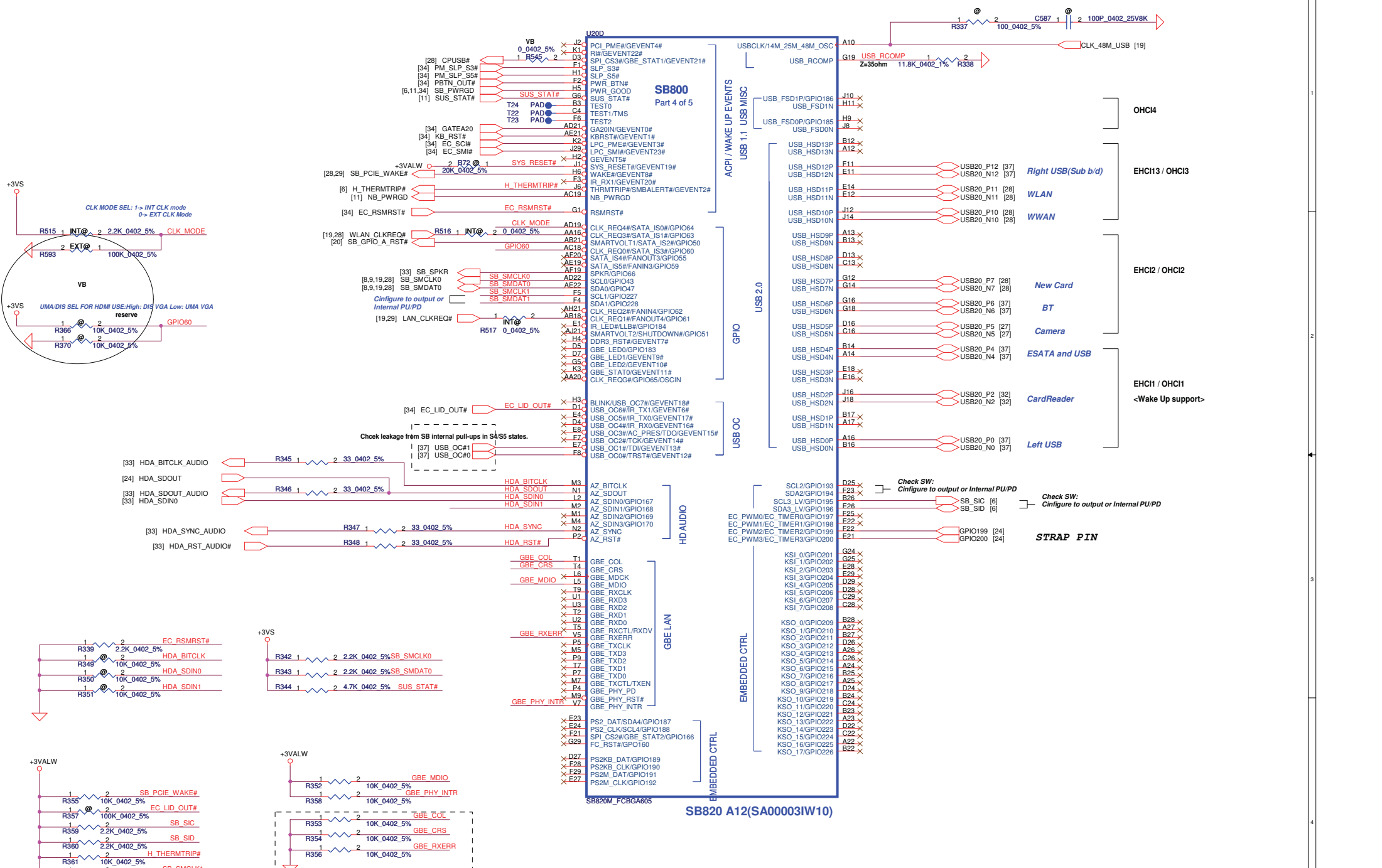


level shift to ISL6265

ISL6265 PWROK input, TTL level: 0.8V-2.0V
When this pin is high, the SVI interface is active and I2C protocol is running. While this pin is low, the SVC, SVD, and VFIXEN input states determine the pre-PWROK metal VID or VFIX mode voltage. This pin must be low prior to the ISL6265 PGOOD output going high



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SB820 USB/HD audio

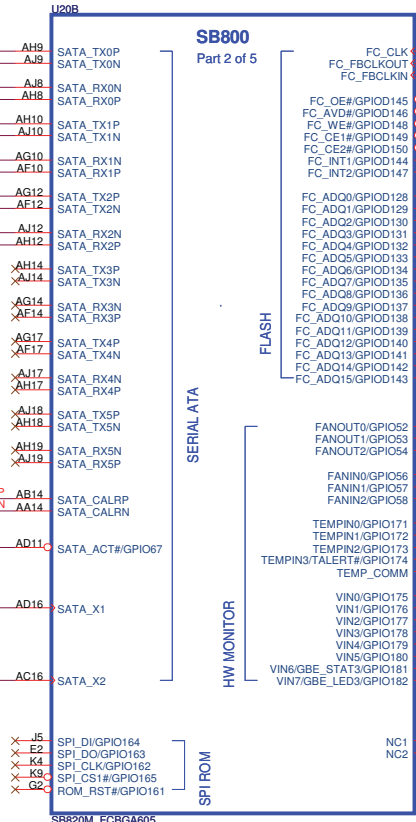
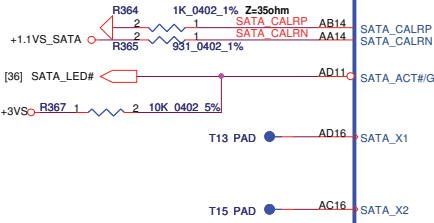
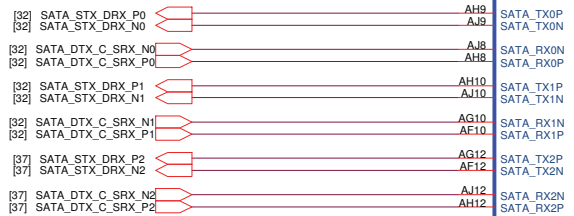
NAWE6 LA-5754P

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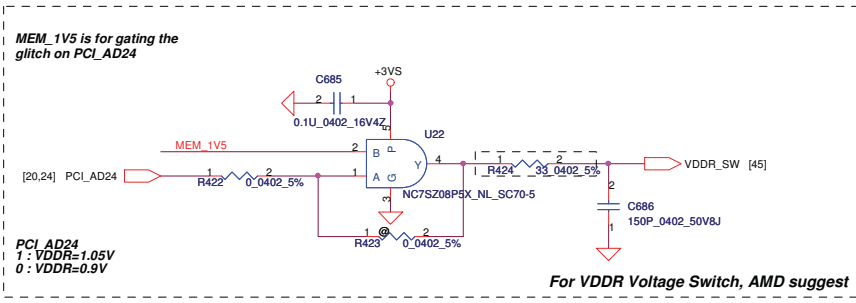
HDD

ODD

e-SATA

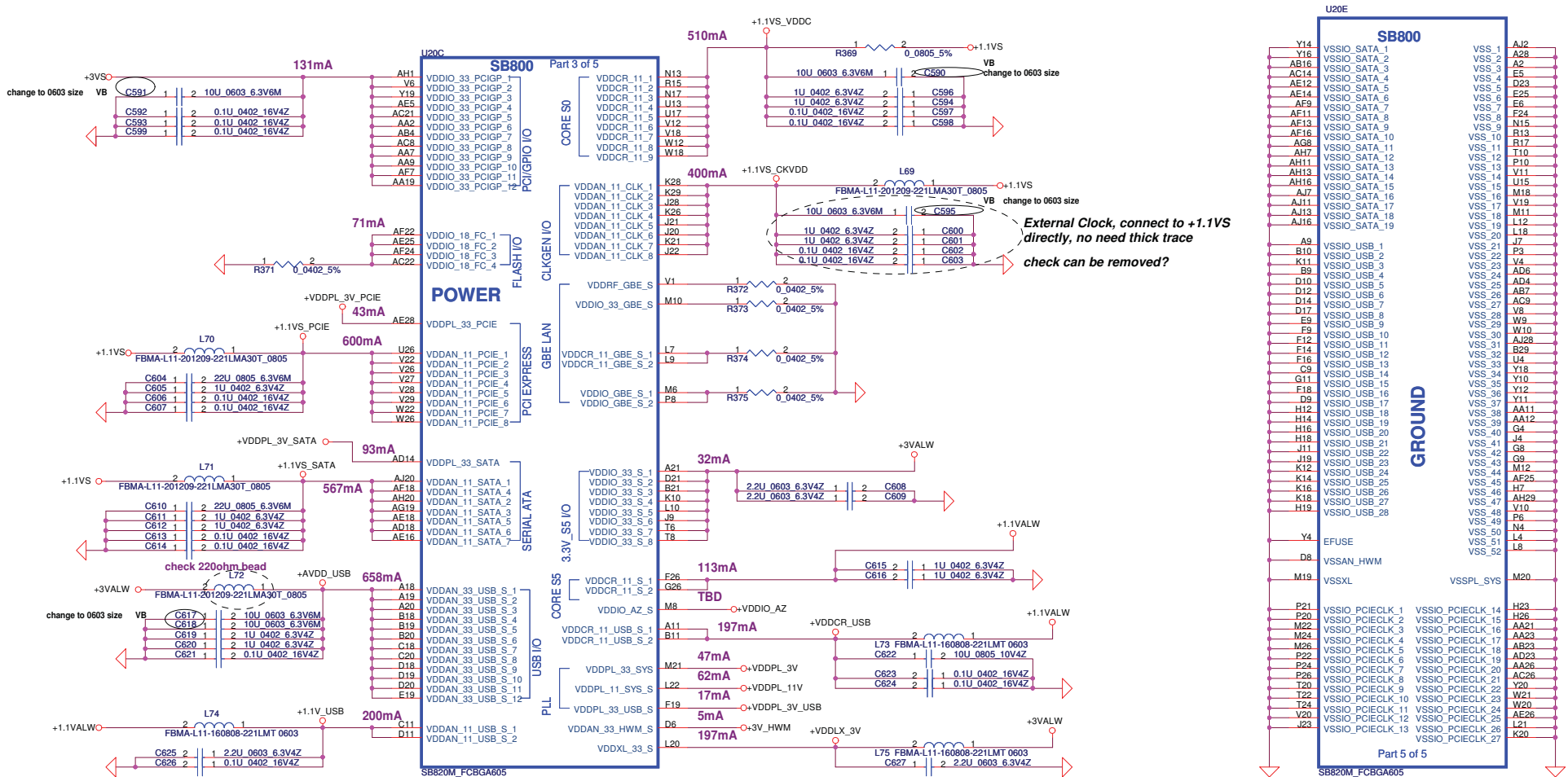


SB820 A12(SA00003IW10)



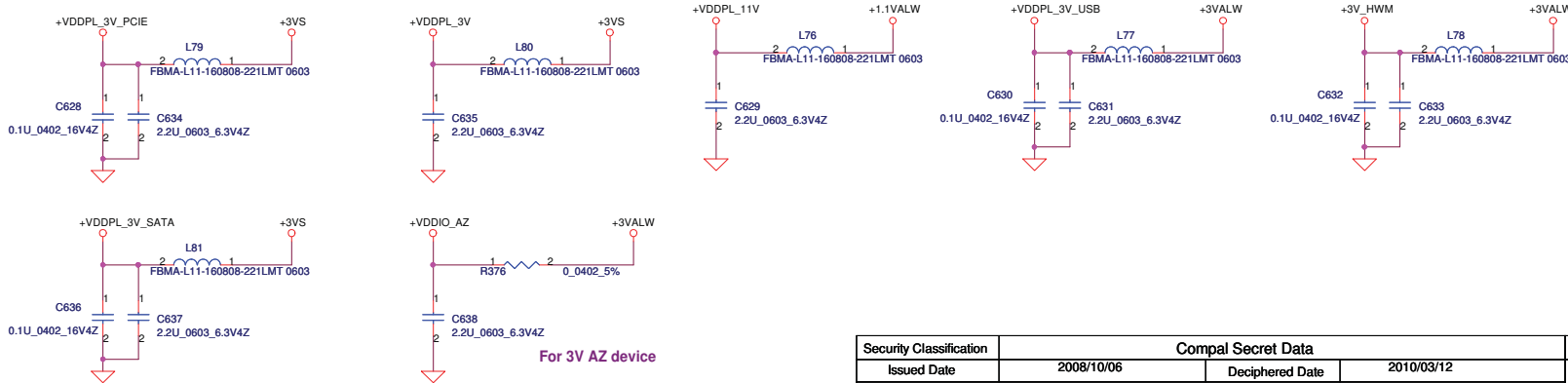
Check SW: Configure to output or Internal PUPD

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SB820 A12(SA00003IW10)

SB820 A12(SA00003IW10)



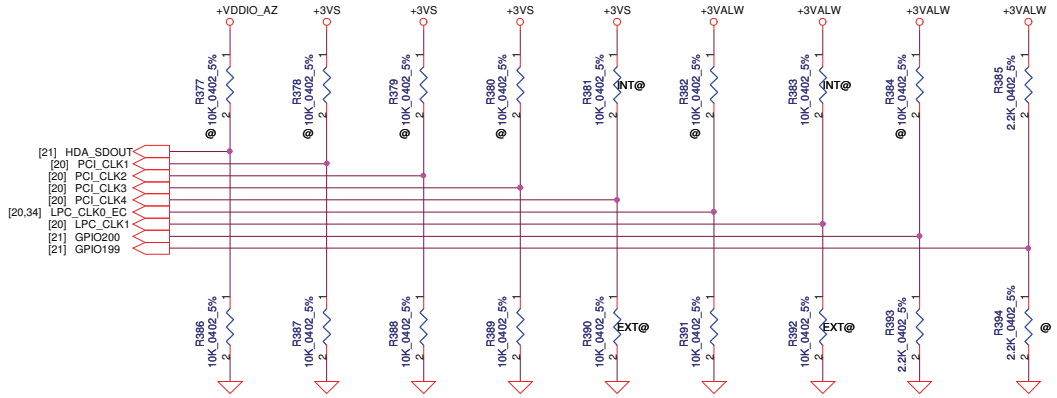
For 3V AZ device

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REQUIRED STRAPS

Check Internal PU/PD

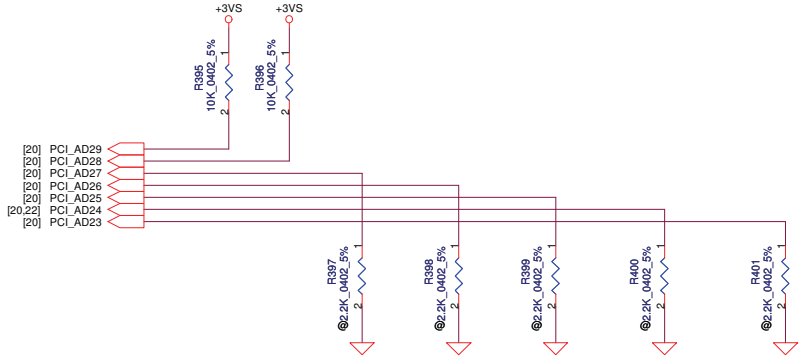
	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200	GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE GEN2	WATCHDOG TIMER ENABLE	USE DEBUG STRAP	CPU/HT CLK SEL Enable	EC ENABLE	CLOCKGEN ENABLE	H,H = Reserved H,L = SPI ROM	
PULL LOW	Performance MODE	FORCE PCIE GEN1	WATCHDOG TIMER DISABLE	IGNORE DEBUG STRAP	CPU/HT CLK SEL Disable	EC DISABLE	CLOCKGEN DISABLE	L,H = LPC ROM (Default L,NC) L,L = FWH ROM	
	DEFAULT	DEFAULT	DEFAULT	DEFAULT	DEFAULT	DEFAULT	DEFAULT		



DEBUG STRAPS

SB800 HAS 15K INTERNAL PU FOR PCI_AD[27:23]

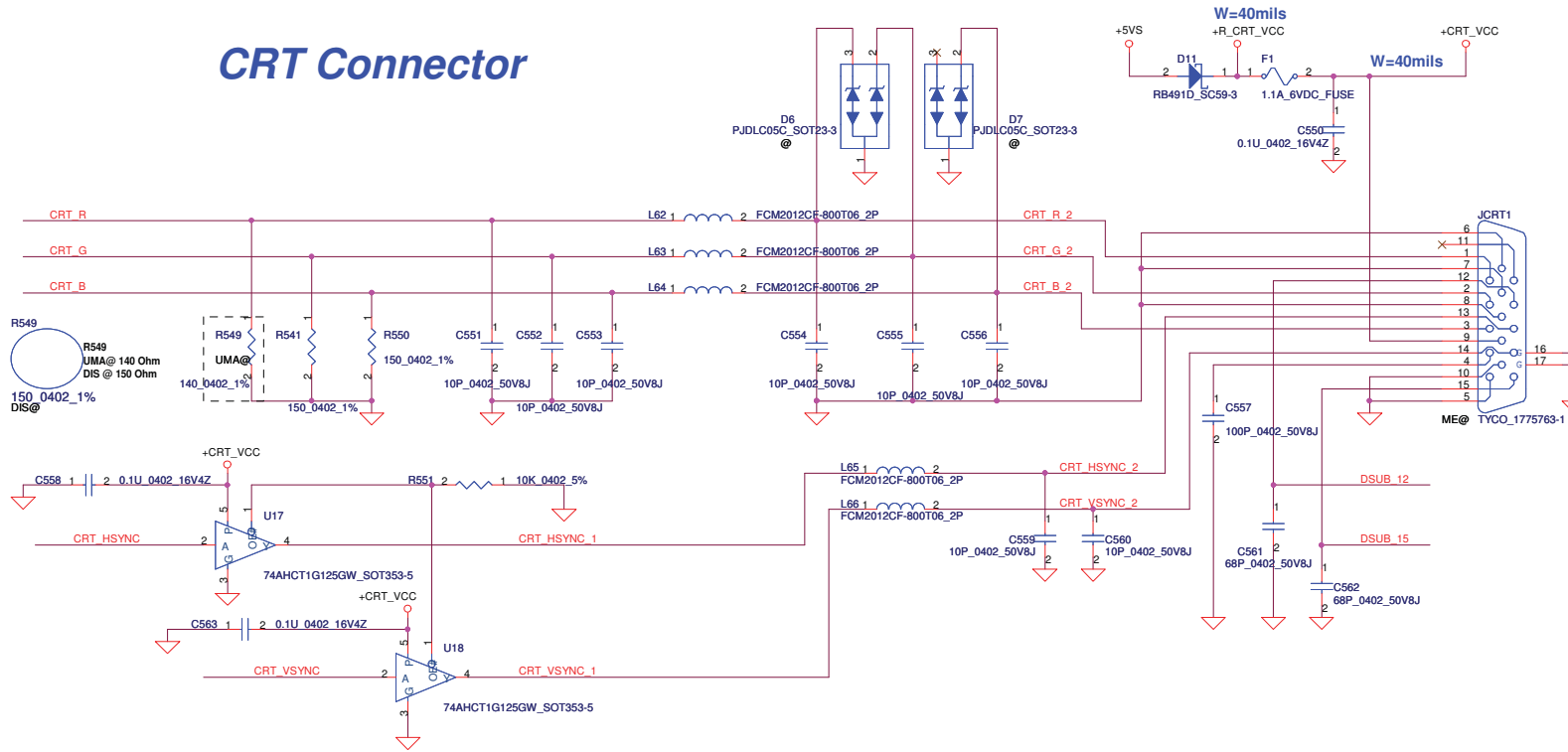
	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL	DISABLE ILA AUTORUN	USE FC PLL	USE DEFAULT PCIE STRAPS	DISABLE PCI MEM BOOT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT
	DEFAULT	DEFAULT	DEFAULT	DEFAULT	DEFAULT



Check AD29,AD28 strap function

check default

CRT Connector

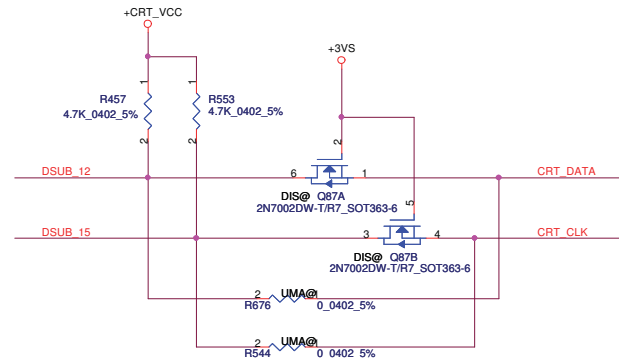


- For UMA Only**
- [11] GMCH_CRT_R → GMCH_CRT_R R677 2 UMA@ 1 0 0402 5% CRT_R
 - [11] GMCH_CRT_G → GMCH_CRT_G R542 2 UMA@ 1 0 0402 5% CRT_G
 - [11] GMCH_CRT_B → GMCH_CRT_B R679 2 UMA@ 1 0 0402 5% CRT_B
 - [11,12] GMCH_CRT_HSYNC → GMCH_CRT_HSYNC R547 2 UMA@ 1 0 0402 5% CRT_HSYNC
 - [11,12] GMCH_CRT_VSYNC → GMCH_CRT_VSYNC R543 2 UMA@ 1 0 0402 5% CRT_VSYNC
 - [11] GMCH_CRT_DATA → GMCH_CRT_DATA R546 2 UMA@ 1 0 0402 5% CRT_DATA
 - [11] GMCH_CRT_CLK → GMCH_CRT_CLK R678 2 UMA@ 1 0 0402 5% CRT_CLK

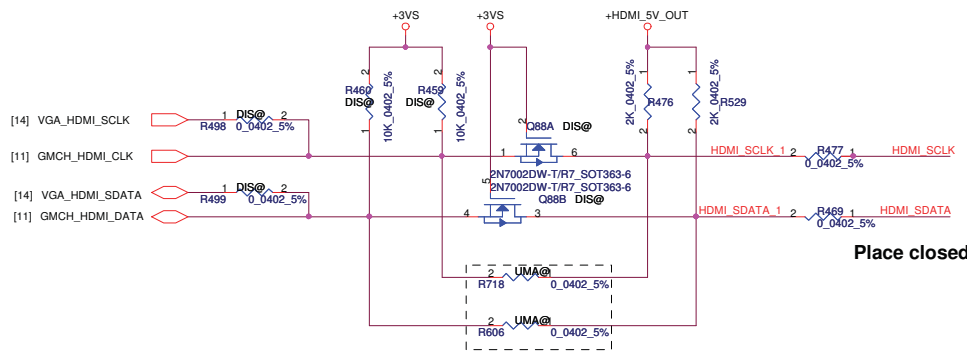
- For VGA Only**
- [14] VGA_CRT_R → VGA_CRT_R R539 2 DIS@ 1 0 0402 5% CRT_R
 - [14] VGA_CRT_G → VGA_CRT_G R552 2 DIS@ 1 0 0402 5% CRT_G
 - [14] VGA_CRT_B → VGA_CRT_B R554 2 DIS@ 1 0 0402 5% CRT_B
 - [14] VGA_CRT_HSYNC → VGA_CRT_HSYNC R535 2 DIS@ 1 0 0402 5% CRT_HSYNC
 - [14] VGA_CRT_VSYNC → VGA_CRT_VSYNC R557 2 DIS@ 1 0 0402 5% CRT_VSYNC
 - [14] VGA_CRT_DATA → VGA_CRT_DATA R538 2 DIS@ 1 0 0402 5% CRT_DATA
 - [14] VGA_CRT_CLK → VGA_CRT_CLK R556 2 DIS@ 1 0 0402 5% CRT_CLK

NOTE:
IF RS880M ONLY(NO MXM SUPPORT),
DAC_SDAT AND DAC_SCL DON'T
NEED LEVEL SHIFT, PU TO +5V DIRECTLY.
DAC_SDAT AND DAC_SCL ARE 5V TOLERANCE.

Close to Conn side

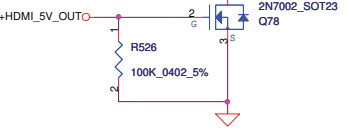
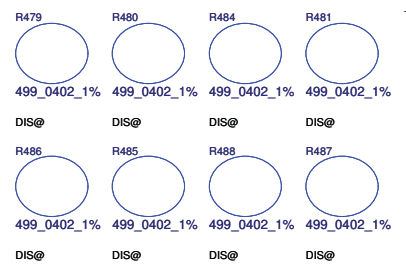


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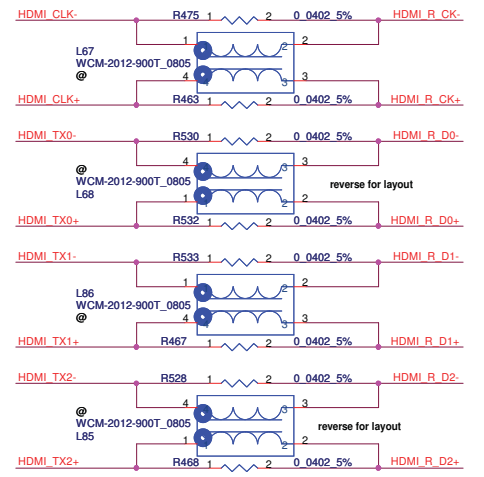
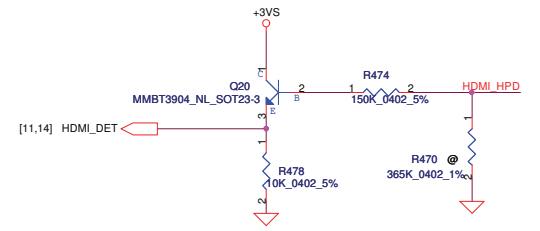
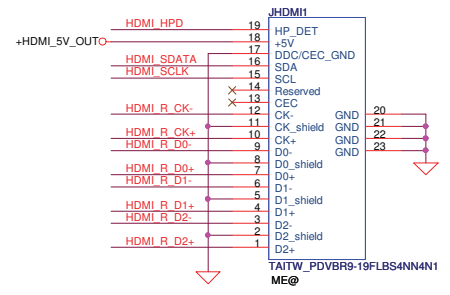
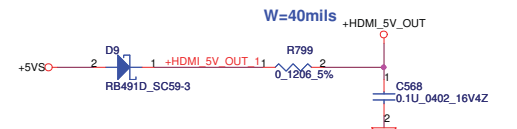


- [10] UMA_HDMI_P0 R490 1 UMA@ 0.0402 5% HDMI TX2+
- [10] UMA_HDMI_N0 R497 1 UMA@ 0.0402 5% HDMI TX2-
- [10] UMA_HDMI_P1 R491 1 UMA@ 0.0402 5% HDMI TX1+
- [10] UMA_HDMI_N1 R492 1 UMA@ 0.0402 5% HDMI TX1-
- [10] UMA_HDMI_P2 R494 1 UMA@ 0.0402 5% HDMI TX0+
- [10] UMA_HDMI_N2 R493 1 UMA@ 0.0402 5% HDMI TX0-
- [10] UMA_HDMI_P3 R495 1 UMA@ 0.0402 5% HDMI CLK+
- [10] UMA_HDMI_N3 R496 1 UMA@ 0.0402 5% HDMI CLK-

- [14] VGA_HDMI_TXD2+ C569 DIS@ 2 1 0.1U 0.402 16V7K HDMI TX2+
- [14] VGA_HDMI_TXD2- C570 DIS@ 2 1 0.1U 0.402 16V7K HDMI TX2-
- [14] VGA_HDMI_TXD1+ C571 DIS@ 2 1 0.1U 0.402 16V7K HDMI TX1+
- [14] VGA_HDMI_TXD1- C700 DIS@ 2 1 0.1U 0.402 16V7K HDMI TX1-
- [14] VGA_HDMI_TXD0+ C899 DIS@ 2 1 0.1U 0.402 16V7K HDMI TX0+
- [14] VGA_HDMI_TXD0- C702 DIS@ 2 1 0.1U 0.402 16V7K HDMI TX0-
- [14] VGA_HDMI_TXC+ C701 DIS@ 2 1 0.1U 0.402 16V7K HDMI CLK+
- [14] VGA_HDMI_TXC- C698 DIS@ 2 1 0.1U 0.402 16V7K HDMI CLK-

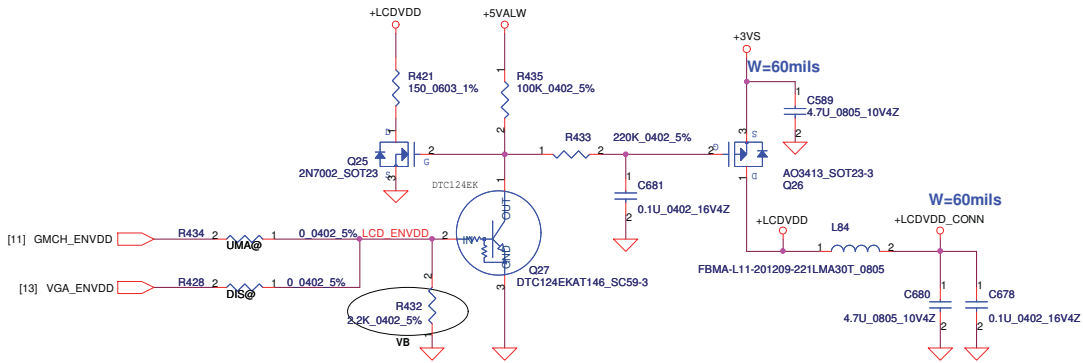


UMA use 715 ohm
VGA use 499 ohm

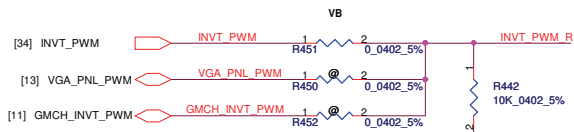
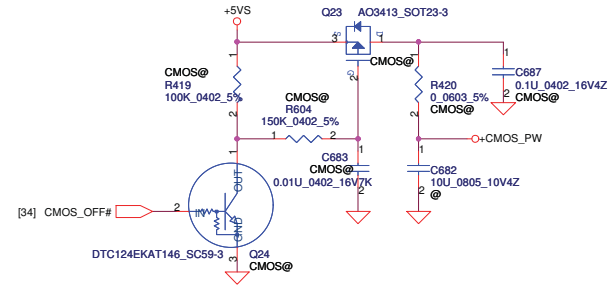


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LCD POWER CIRCUIT



CMOS Camera

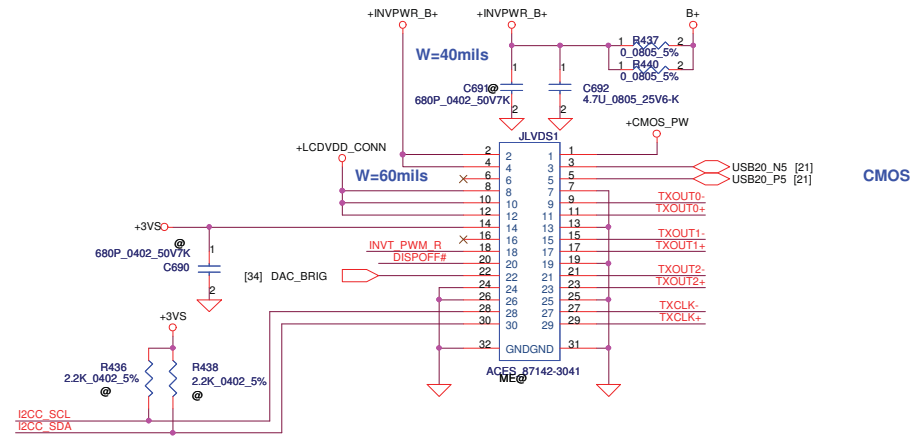


VGA ONLY

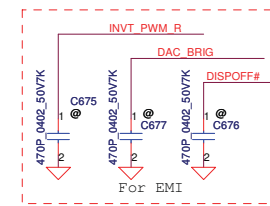
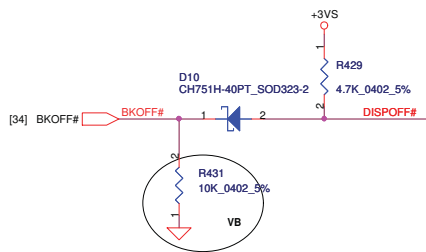
TXCLK-	DIS@ 1	R466 2	0.0402 5%	VGA_TXCLK-	[13]
TXCLK+	DIS@ 1	R505 2	0.0402 5%	VGA_TXCLK+	[13]
TXOUT2-	DIS@ 1	R508 2	0.0402 5%	VGA_TXOUT2-	[13]
TXOUT2+	DIS@ 1	R510 2	0.0402 5%	VGA_TXOUT2+	[13]
TXOUT1+	DIS@ 1	R511 2	0.0402 5%	VGA_TXOUT1+	[13]
TXOUT1-	DIS@ 1	R512 2	0.0402 5%	VGA_TXOUT1-	[13]
TXOUT0+	DIS@ 1	R513 2	0.0402 5%	VGA_TXOUT0+	[13]
TXOUT0-	DIS@ 1	R514 2	0.0402 5%	VGA_TXOUT0-	[13]
I2CC_SCL	DIS@ 2	R455 1	0.0402 5%	VGA_LCD_CLK	[14]
I2CC_SDA	DIS@ 2	R441 1	0.0402 5%	VGA_LCD_DAT	[14]

UMA ONLY

TXCLK-	UMA@1	R521 2	0.0402 5%	GMCH_TXCLK-	[11]
TXCLK+	UMA@1	R537 2	0.0402 5%	GMCH_TXCLK+	[11]
TXOUT2-	UMA@1	R555 2	0.0402 5%	GMCH_TXOUT2-	[11]
TXOUT2+	UMA@1	R540 2	0.0402 5%	GMCH_TXOUT2+	[11]
TXOUT1+	UMA@1	R603 2	0.0402 5%	GMCH_TXOUT1+	[11]
TXOUT1-	UMA@1	R600 2	0.0402 5%	GMCH_TXOUT1-	[11]
TXOUT0+	UMA@1	R602 2	0.0402 5%	GMCH_TXOUT0+	[11]
TXOUT0-	UMA@1	R601 2	0.0402 5%	GMCH_TXOUT0-	[11]
I2CC_SCL	UMA@2	R453 1	0.0402 5%	GMCH_LCD_CLK	[11]
I2CC_SDA	UMA@2	R454 1	0.0402 5%	GMCH_LCD_DATA	[11]

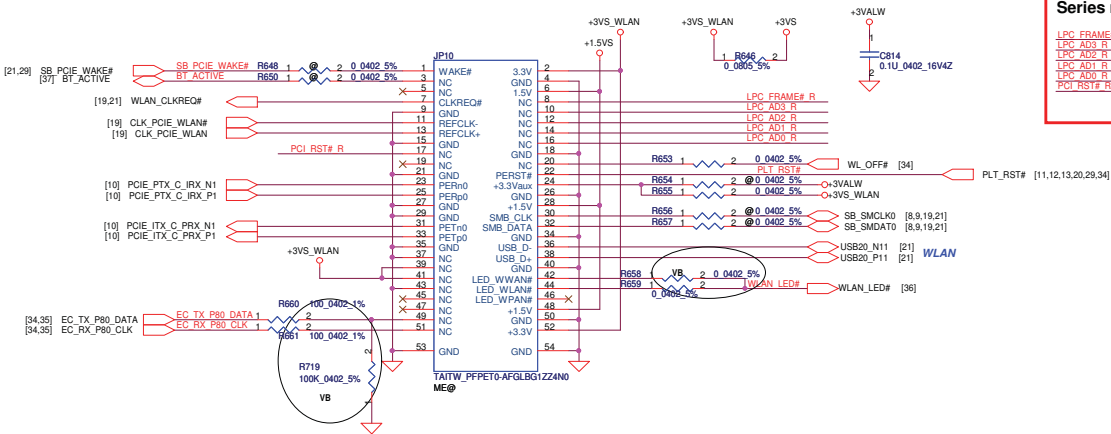


CMOS



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Mini-Express Card for WLAN/WiMAX(Half)

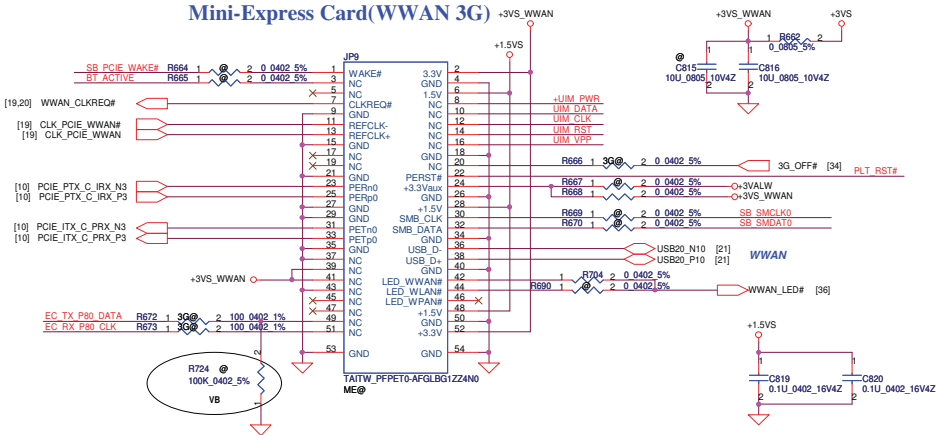


Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.

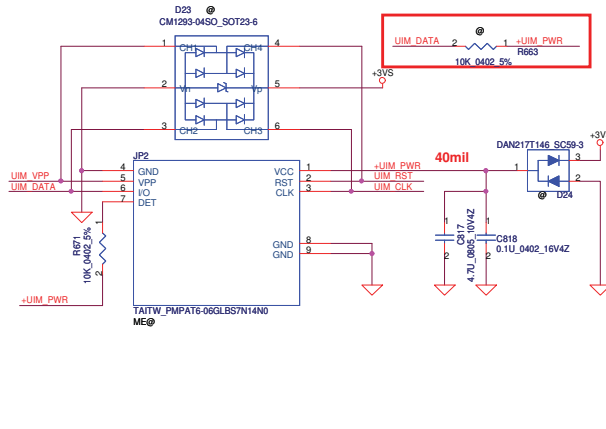
LPC_FRAME# R	R644	1	2	0	0402_5%	LPC_FRAME#	[20,34]
LPC_AD3# R	R645	1	2	0	0402_5%	LPC_AD3#	[20,34]
LPC_AD2# R	R647	1	2	0	0402_5%	LPC_AD2#	[20,34]
LPC_AD1# R	R649	1	2	0	0402_5%	LPC_AD1#	[20,34]
LPC_AD0# R	R651	1	2	0	0402_5%	LPC_AD0#	[20,34]
PLT_RST# R	R652	1	2	0	0402_5%	PLT_RST#	[11,12,13,20,29,34]

Mini-Express Card for WWAN(Full)

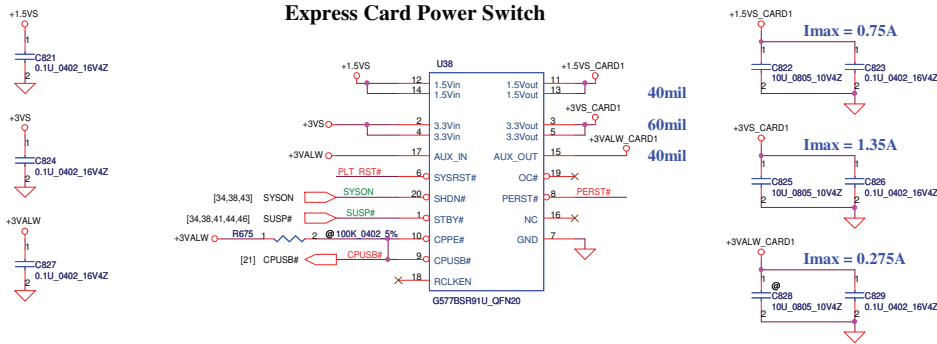
Mini-Express Card(WWAN 3G)



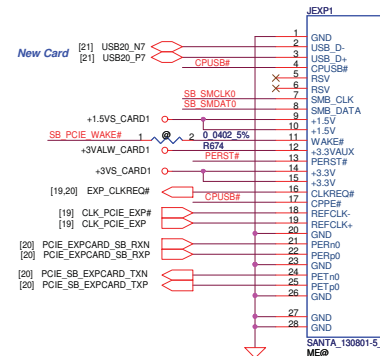
Vcc 3.3V +/- 8%
Peak Icc 2750mA
with max supply droop 50mA
Average Icc 1000mA

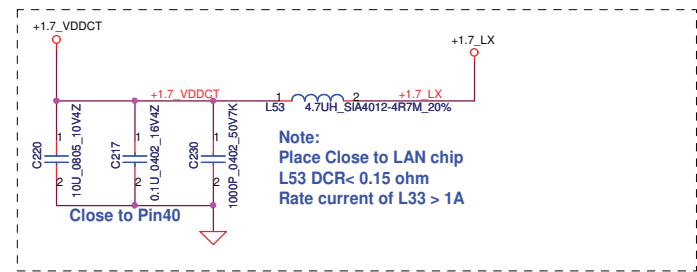
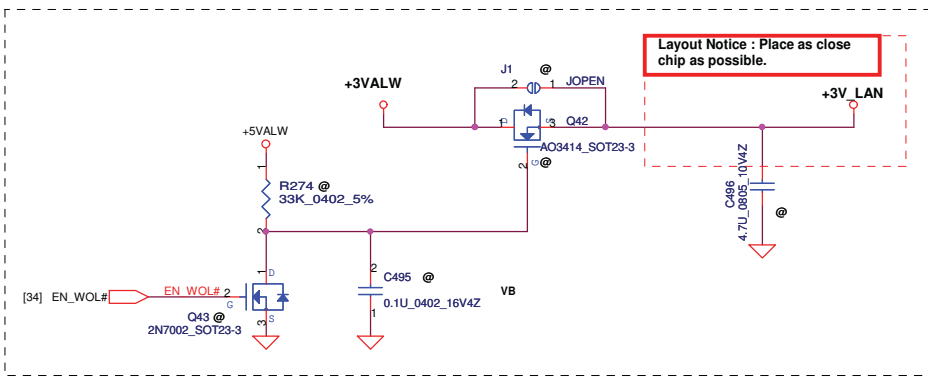


Express Card Power Switch



New Card 34mm Socket (Left/TOP)

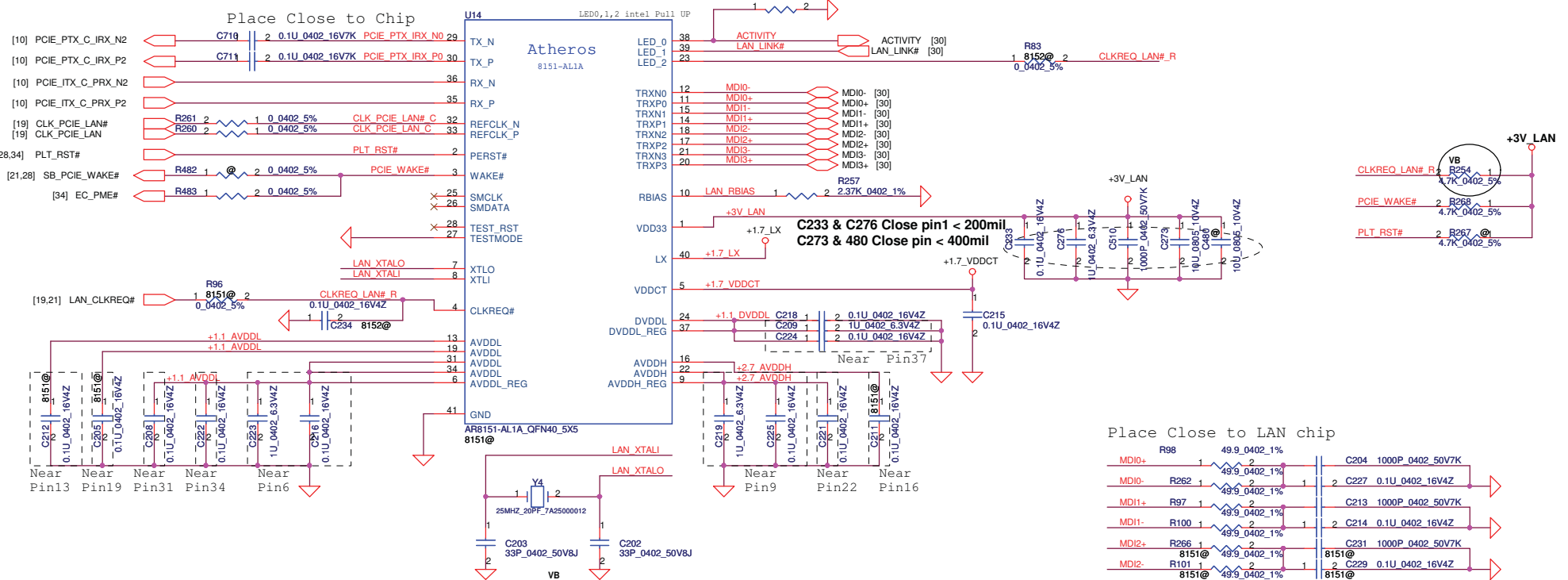




Power On strapping

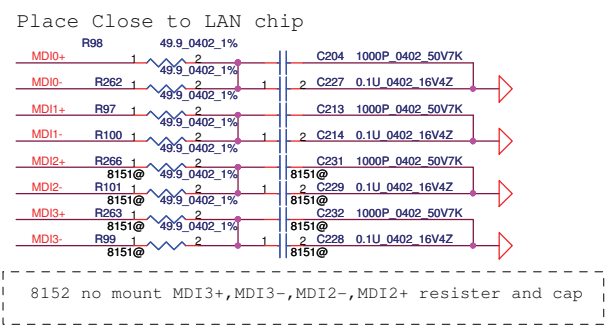
Pin	Description	Chip Default
LED0	H:Over Clock Enable L:Over Clock Disable *	H
	H:SWR Switch mode regulator Select *	
	AR8151 Pin23=LED2.	--
	AR8152, Pin23 is CLKREQ	

S IC AR8152-AL1E QFN 40P E-LAN CTRL

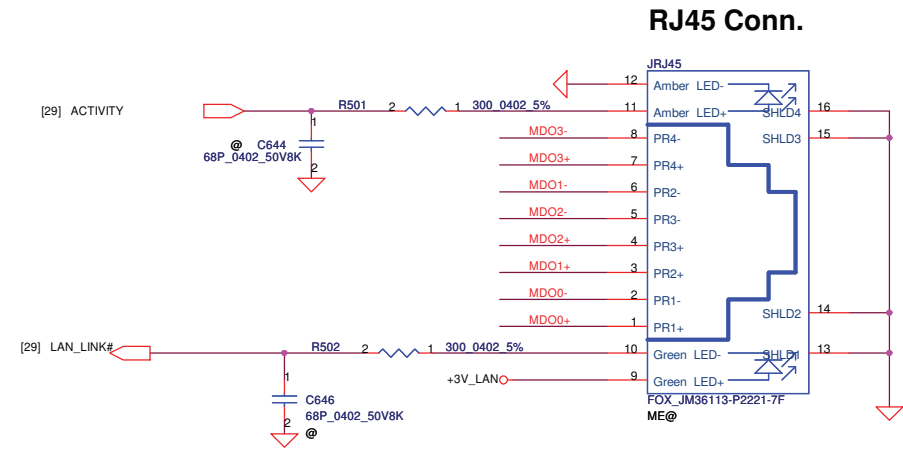
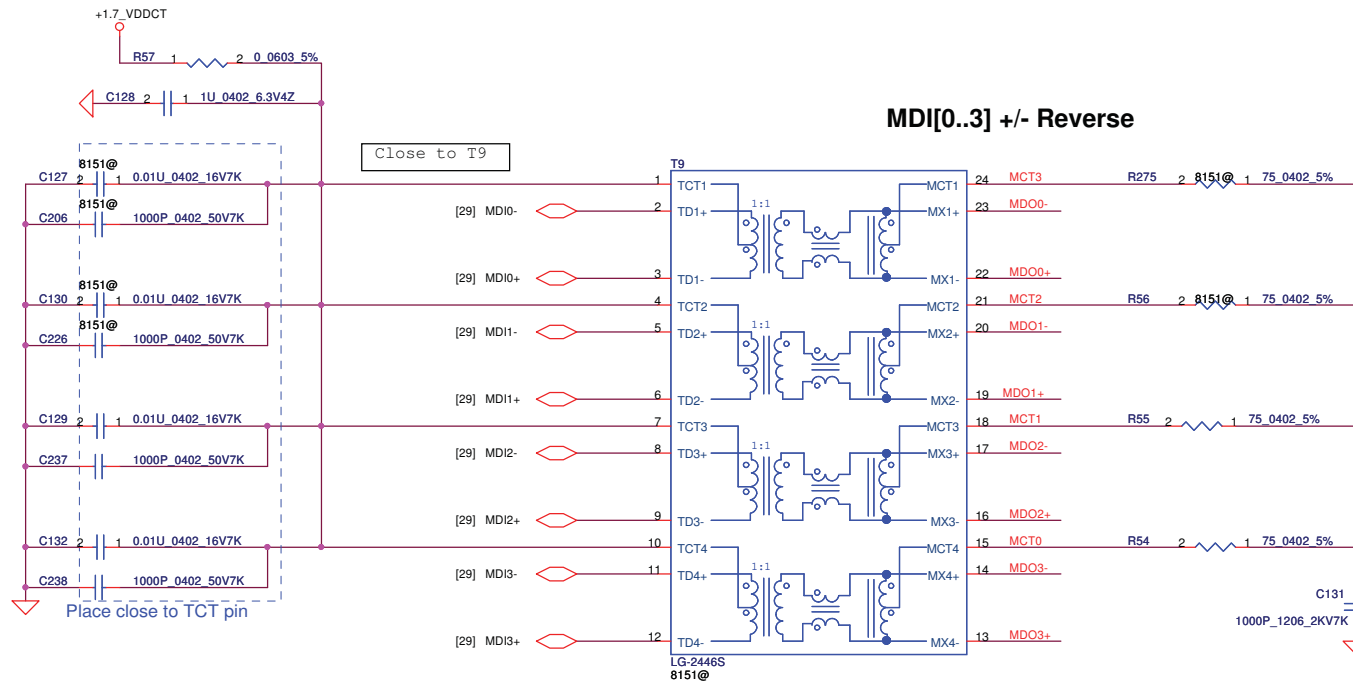


For AR8152, pin23 is the LDO output. Mount C234 and no mount R96.close to this pin4

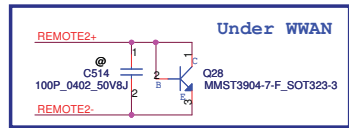
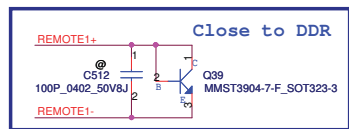
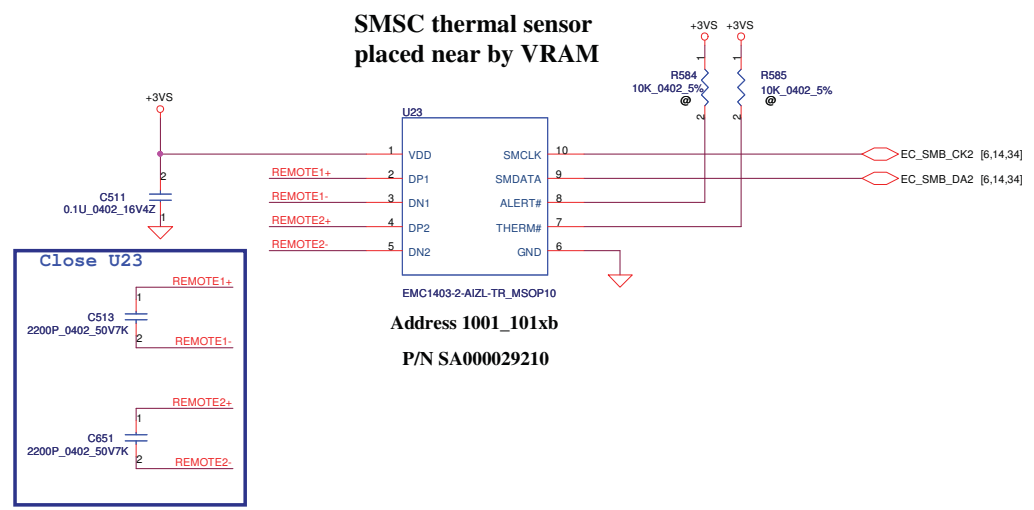
For AR8151, pin4 is the CLKREQn pin, mount R96 and no mount C234.close to this pin4



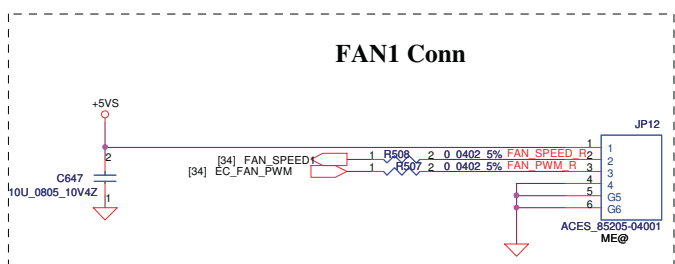
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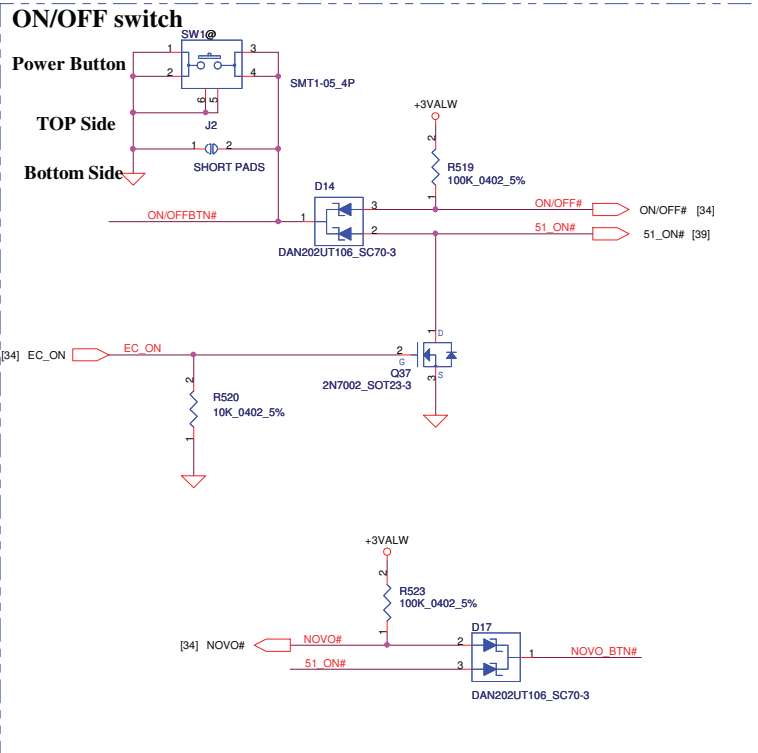
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Issued Date	2009/03/20	Deciphered Date	2010/03/20	Title	
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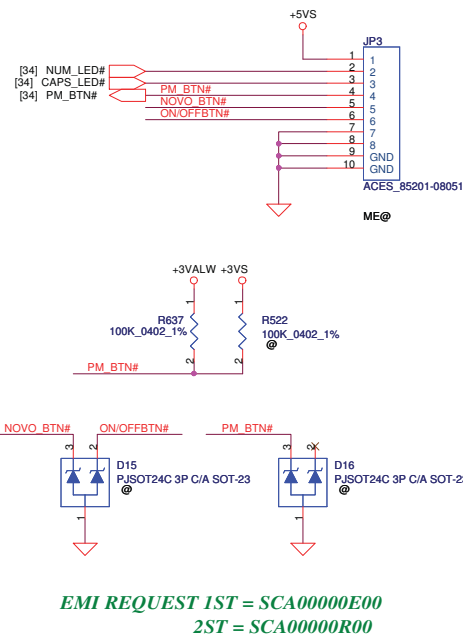
REMOTE1, 2+/-:
Trace width/space: 10/10 mil
Trace length: <8"



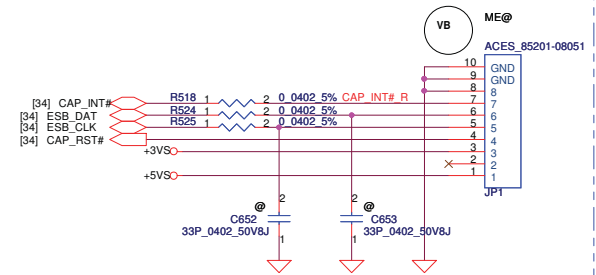
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Issued Date	2008/10/06	Deciphered Date	2010/03/12	Title	
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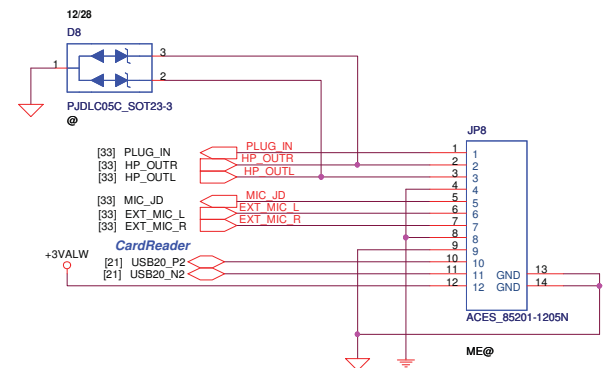
Power Bottom Board Conn. 8pin



Cap Sensor Board Conn. 8pin

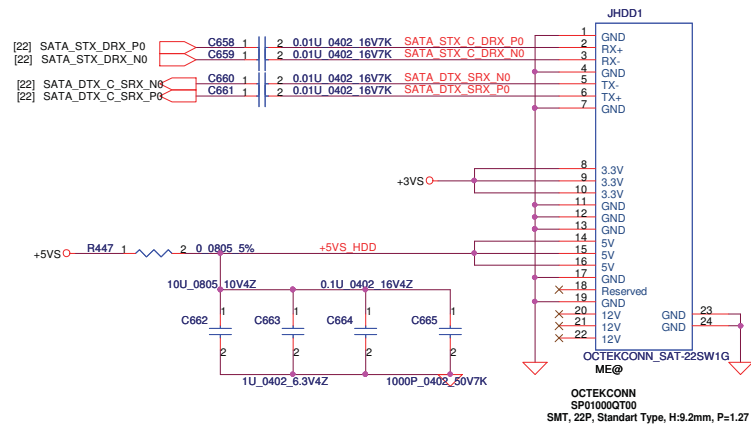
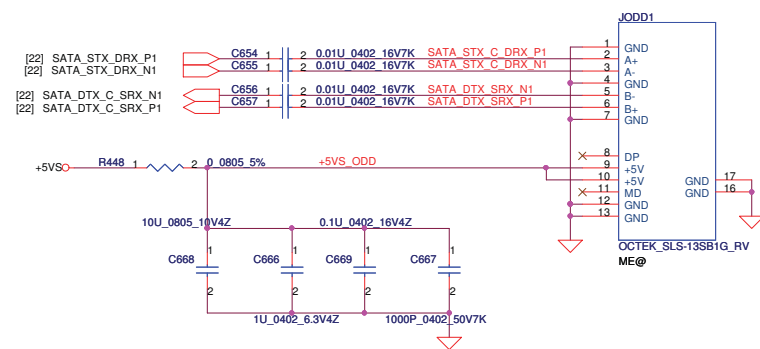


Card Reader/Audio Jack SB CONN



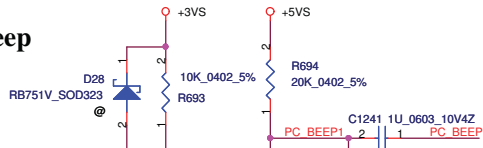
SATA HDD Conn.

SATA ODD Conn.

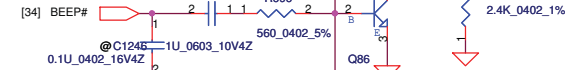


Security Classification	Compal Secret Data			Title	
Issued Date	2007/10/15	Deciphered Date	2008/10/15	HDD/ODD Connector	
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				NAWE6 LA-5754P	0.2
				Date: Tuesday, March 02, 2010	Sheet 32 of 47

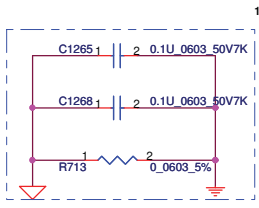
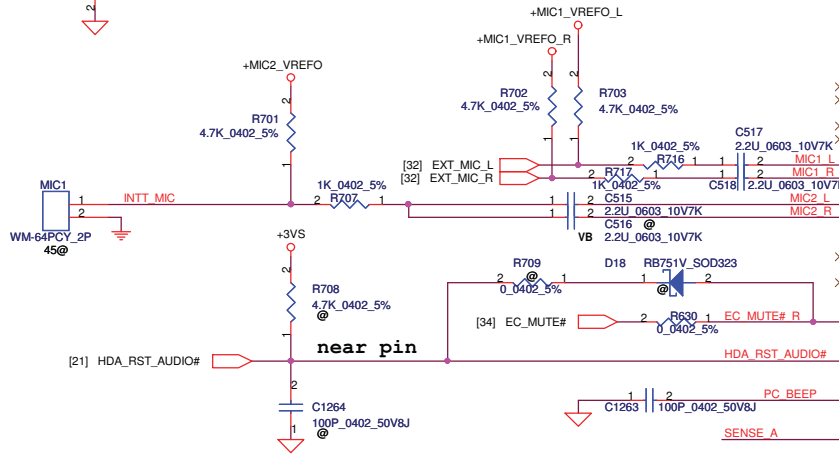
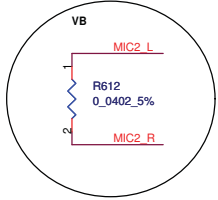
PC BEEP



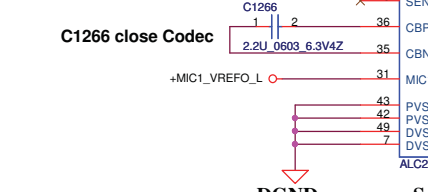
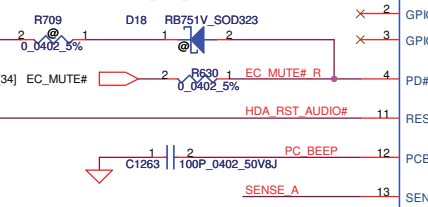
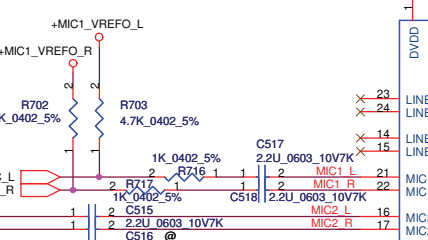
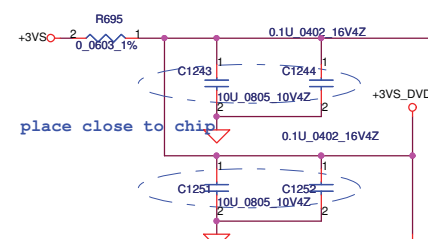
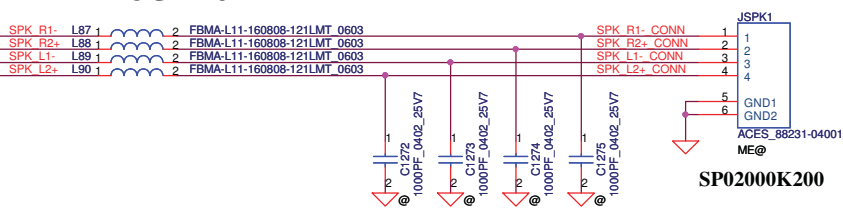
EC BEEP



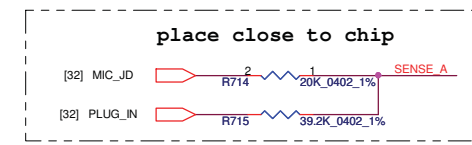
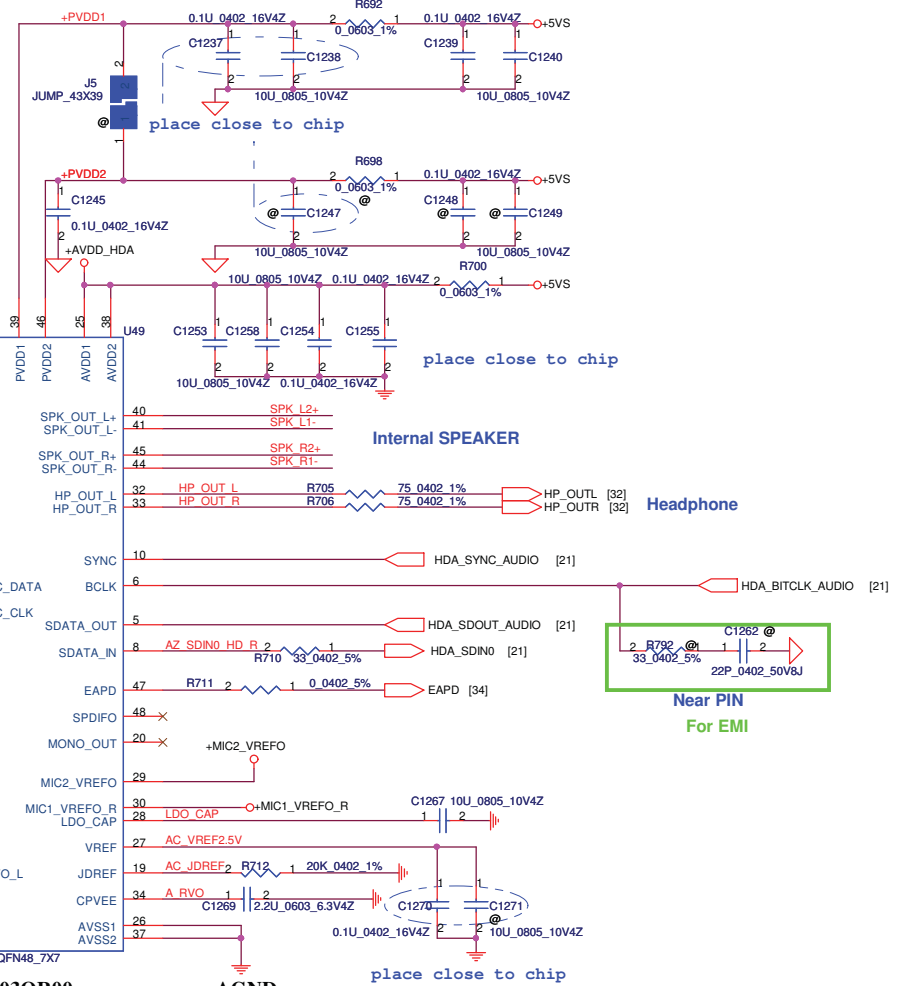
SB BEEP



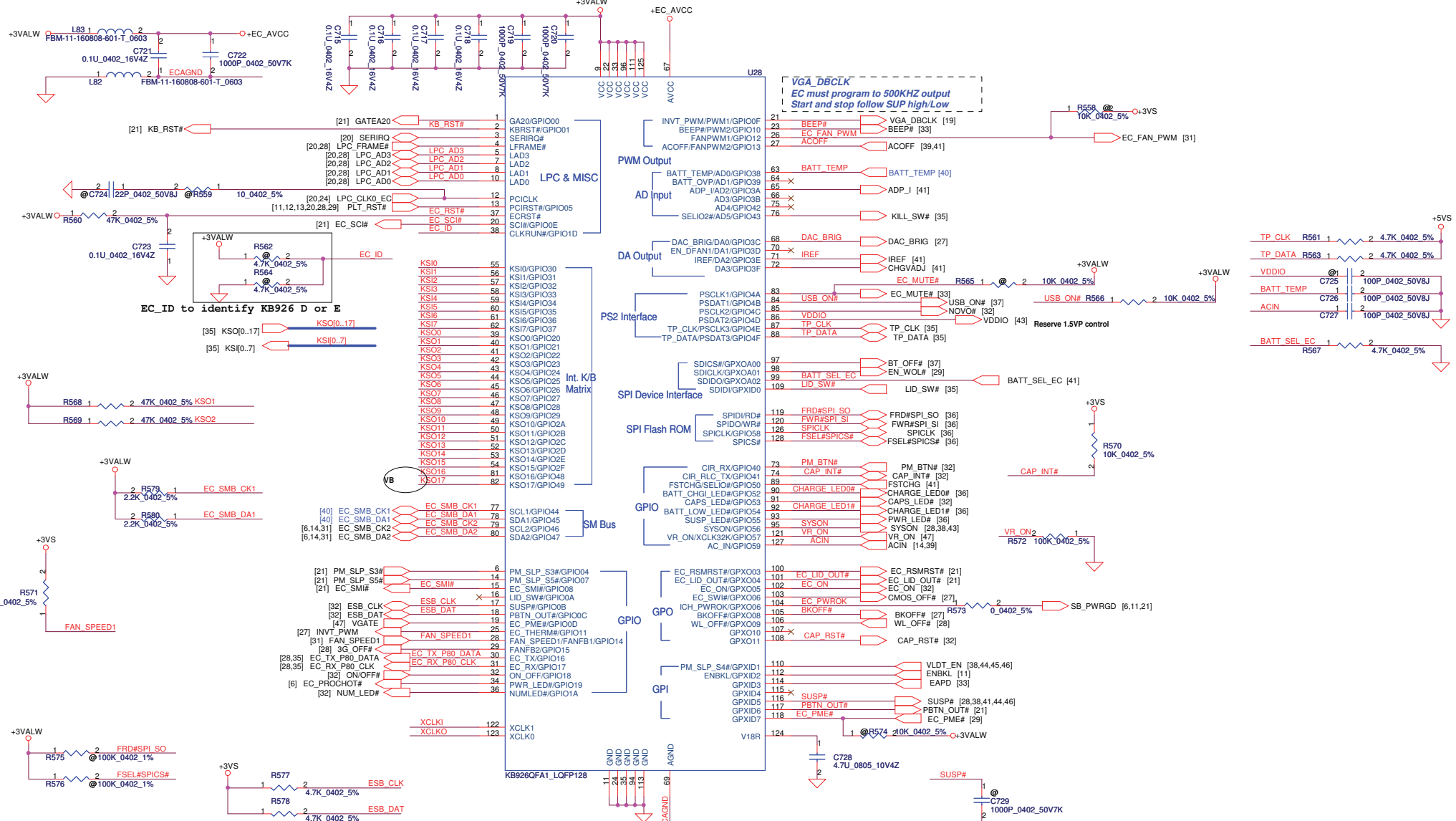
wide 20MIL



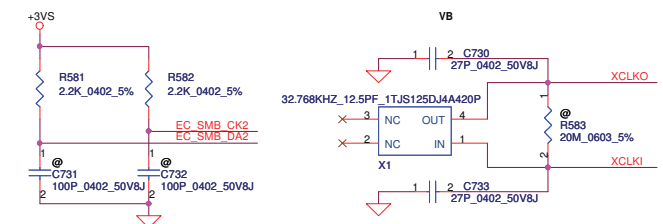
Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	(PIN 48)	



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Issued Date	2008/03/25	Deciphered Date	2008/04/	ALC259 Codec	
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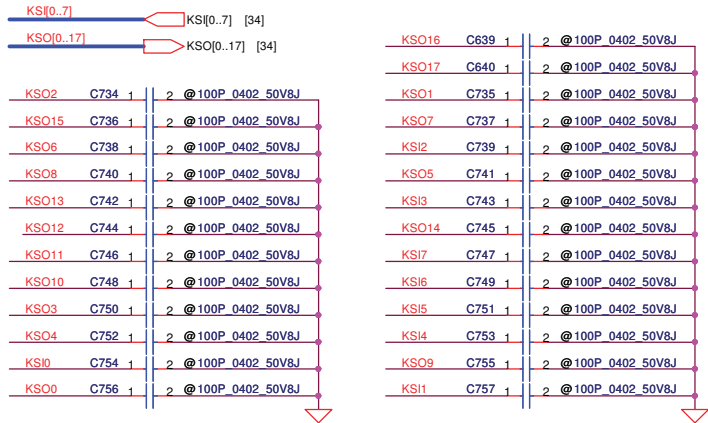
ENE926 (EO) SA0001J5A0



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Issued Date	2007/10/15	Deciphered Date	2008/10/15	Document Number
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				0.2
Date: Tuesday, March 02, 2010				Sheet 34 of 47

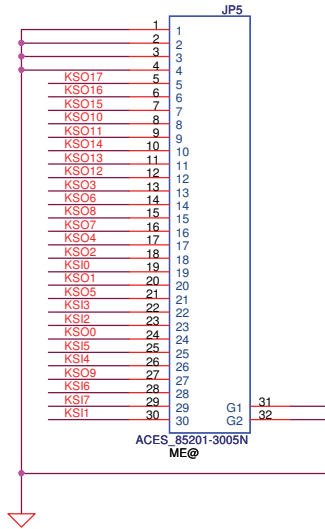
Compal Electronics, Inc.
BIOS & EC I/O Port
NAWE6 LA-5754P

INT_KBD Conn.

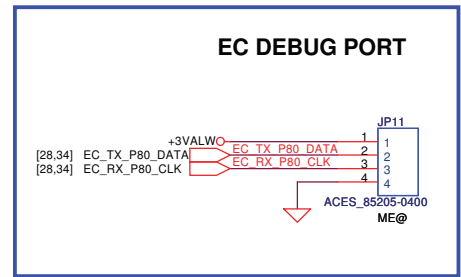


CONN PIN define need double check

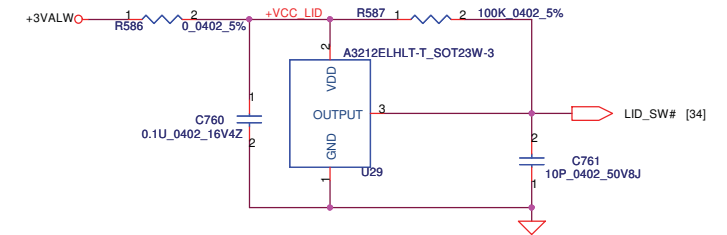
reversal of NIWE1



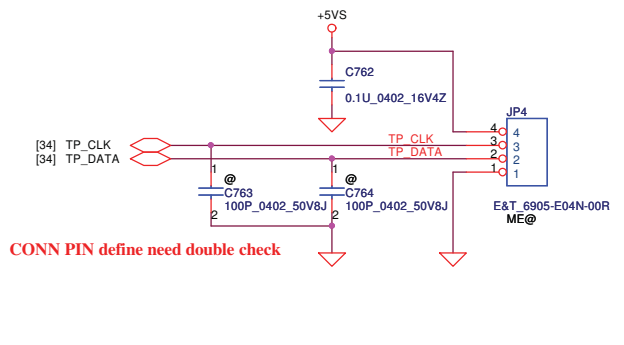
EC DEBUG PORT



Lid Switch

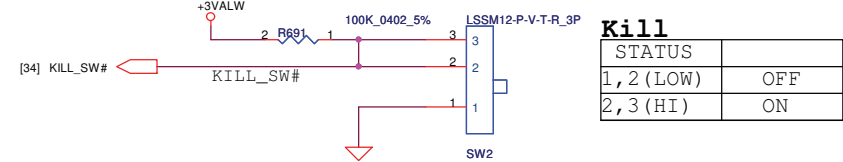


To TP/B Conn.



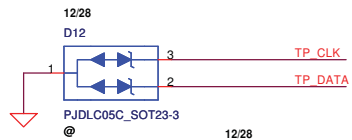
CONN PIN define need double check

Kill Switch



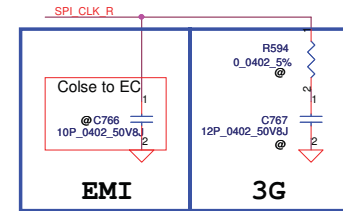
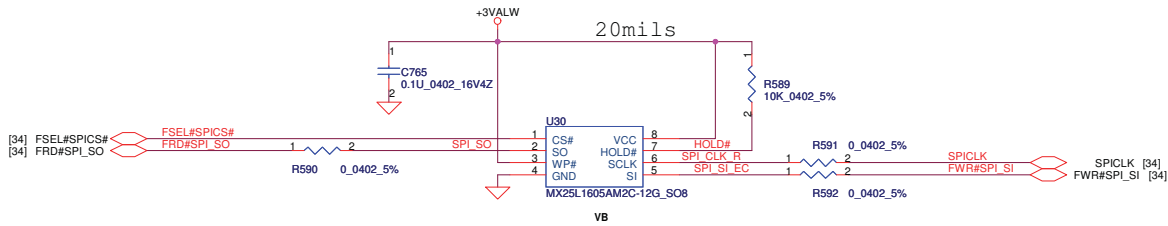
Kill

STATUS	
1, 2 (LOW)	OFF
2, 3 (HI)	ON

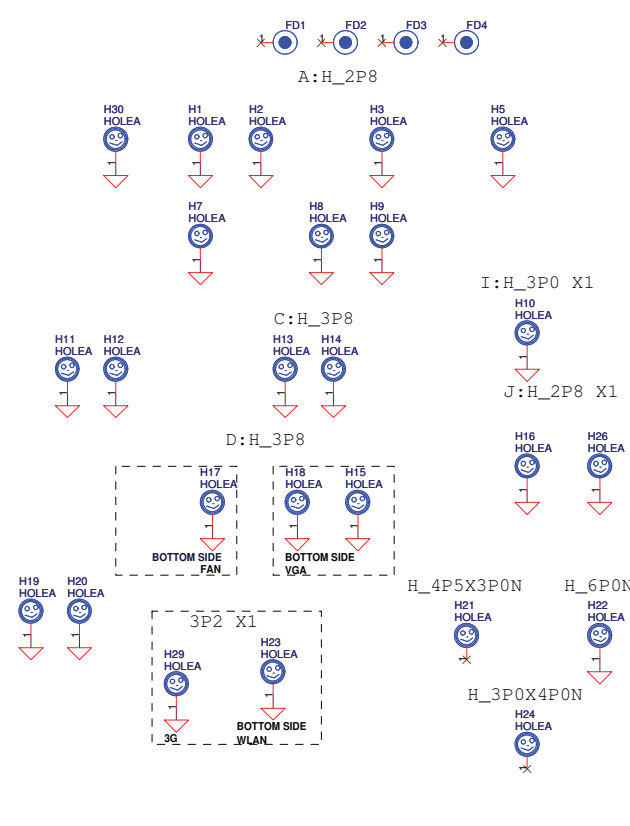
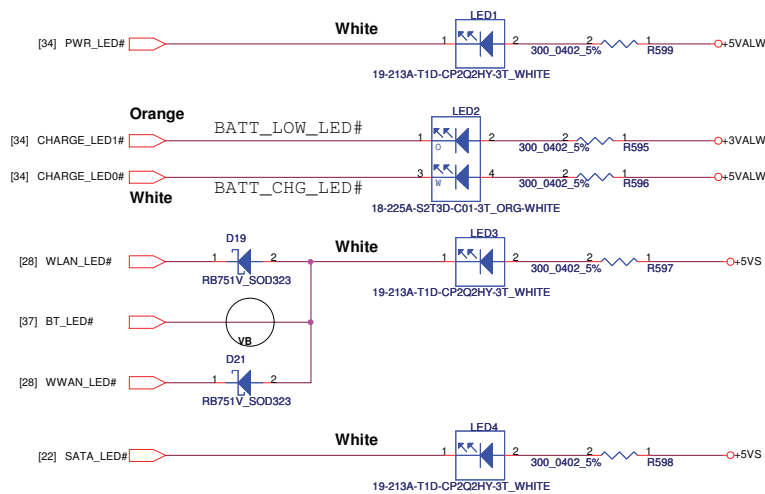


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Issued Date	2007/10/15	Deciphered Date	2008/10/15	Compal Electronics, Inc.
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Date:	Monday, March 01, 2010	Sheet	35	of 47

**SA00002T000 package 200mil
S IC FL 16MBIT MX25L1605AM2C-12G SO8 ROM**

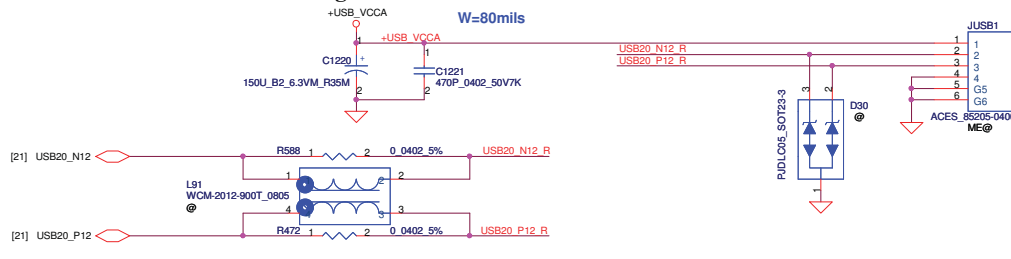


LED

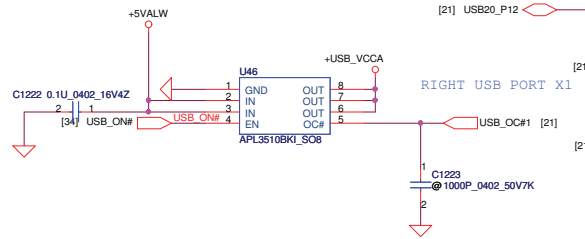


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				NAWE6 LA-5754P
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				Date: Tuesday, March 02, 2010
				Sheet 36 of 47

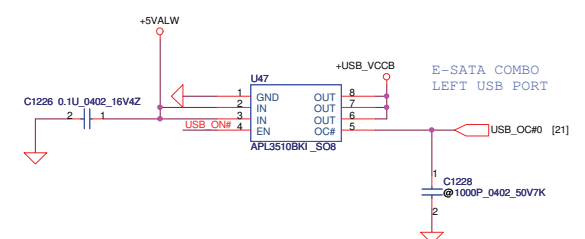
Right USB Conn.



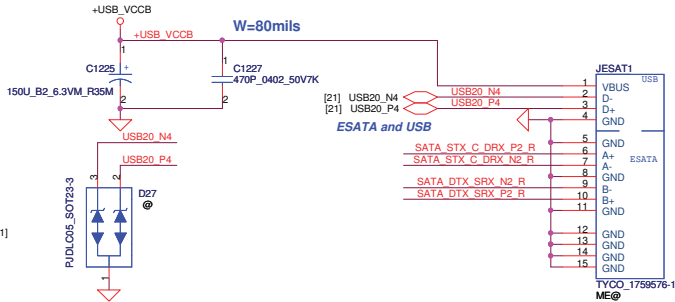
Right USB(Sub b/d)



USB power switch need update symbol to SA000039E00(Low enable)

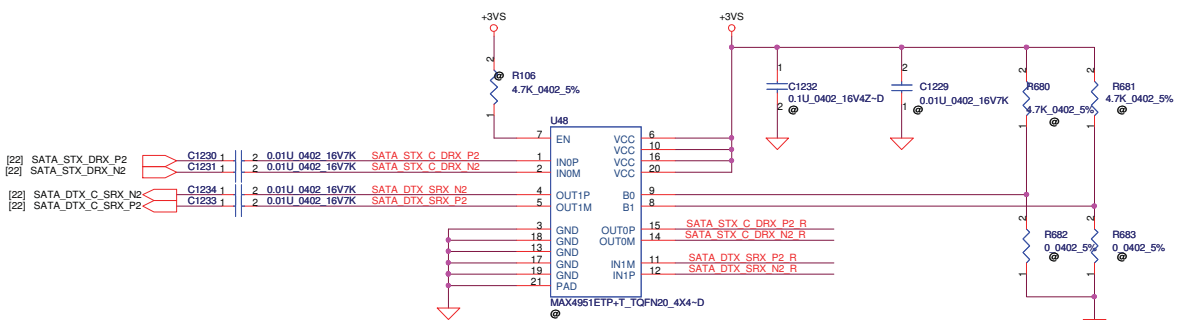
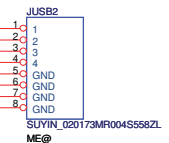
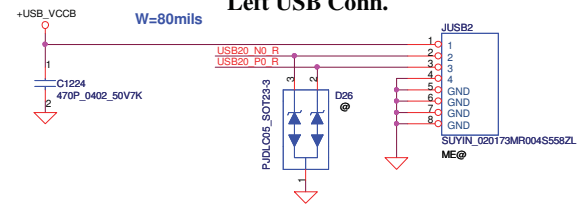


ESATA and USB Conn.

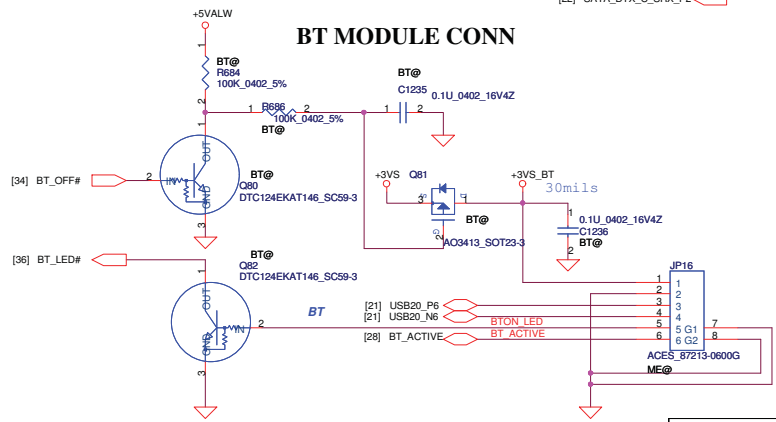


USB
A+ = RXP
A- = RXN
B- = TXN
B+ = TXP

Left USB Conn.

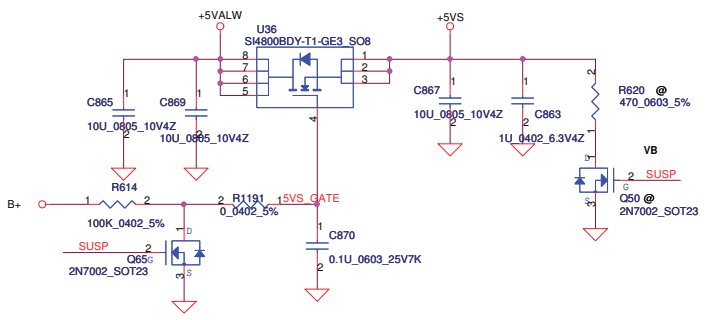


BT MODULE CONN

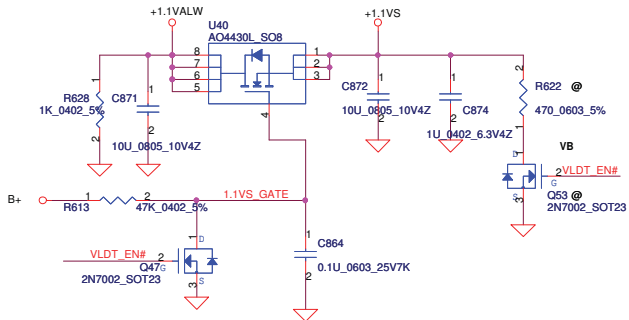


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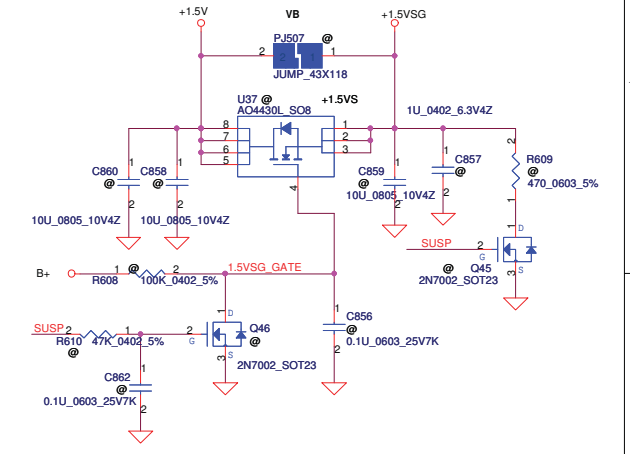
+5VALW TO +5VS



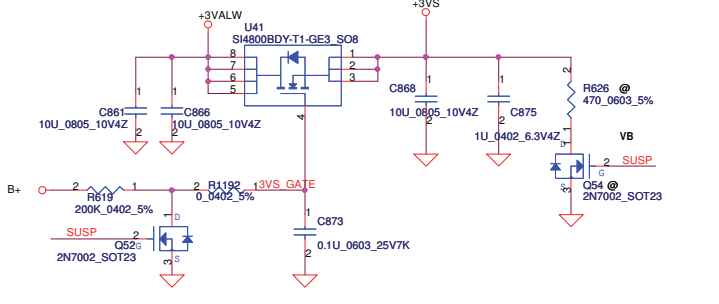
+1.1VALW TO +1.1VS (NB HT)



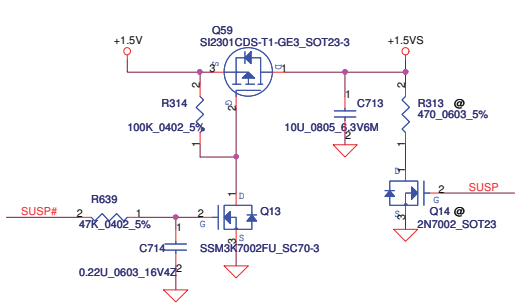
+1.5V to +1.5VSG



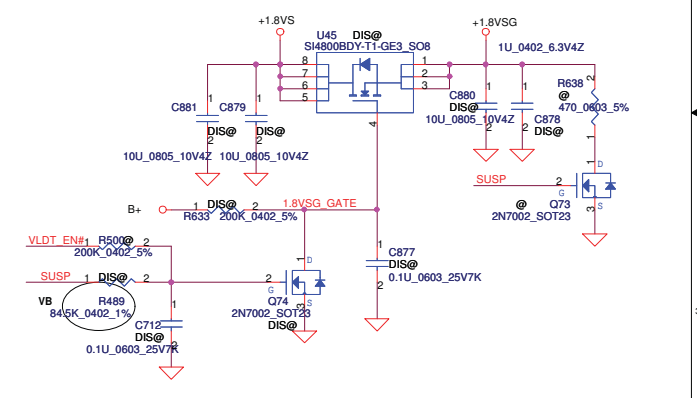
+3VALW TO +3VS



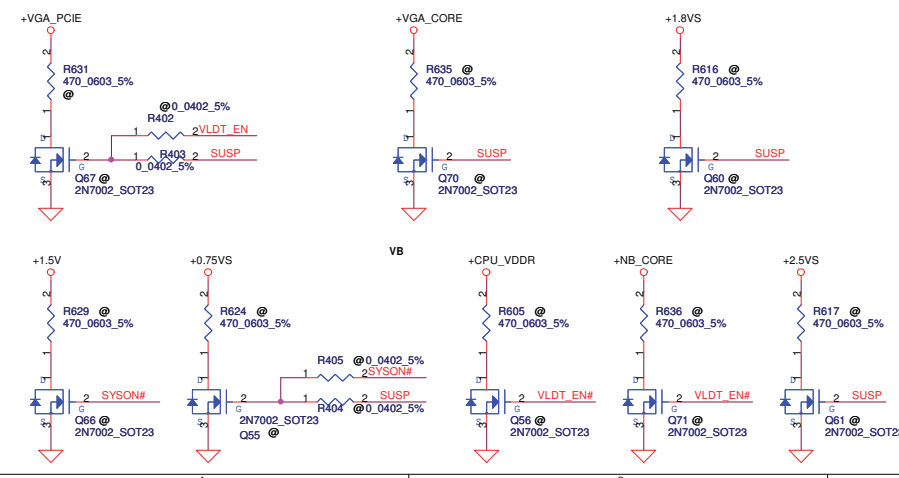
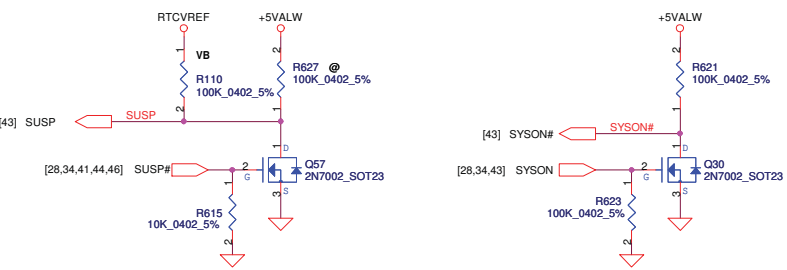
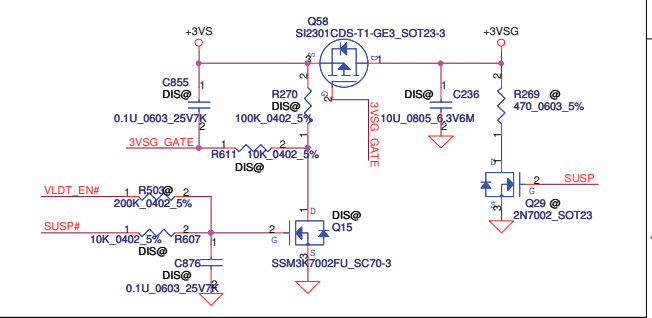
+1.5VS



+1.8VS to +1.8VSG

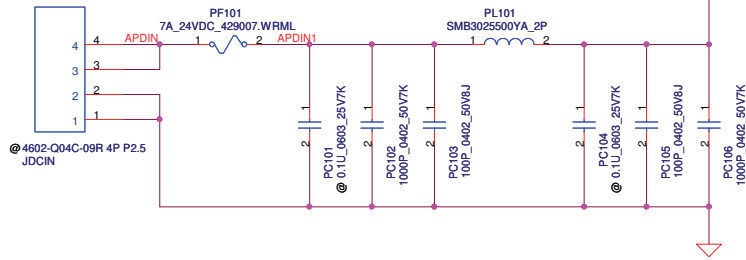


+3VSG

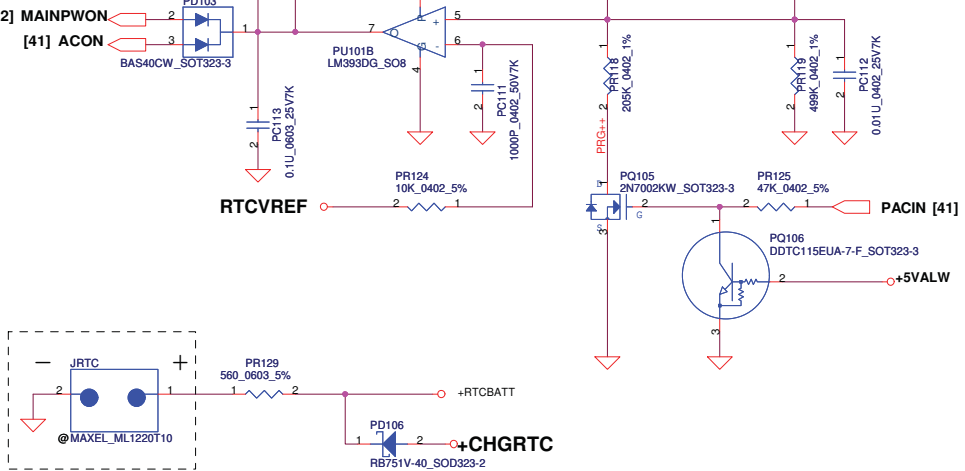
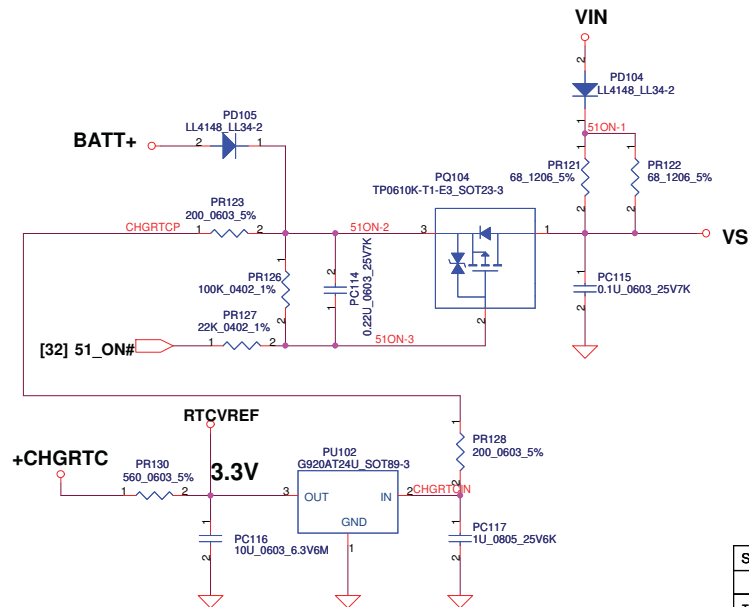
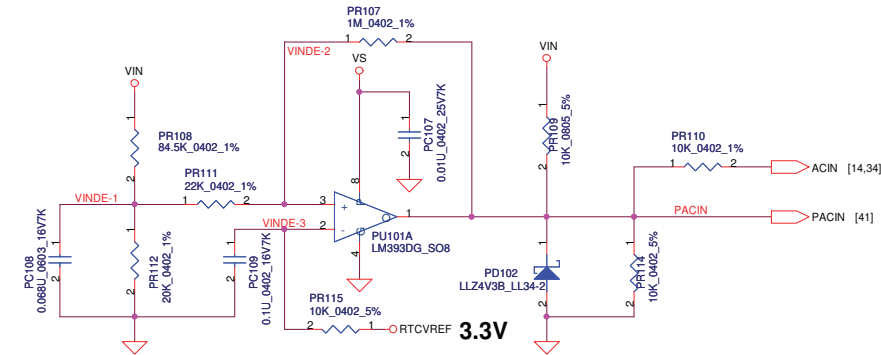


Security Classification		Compal Secret Data		Title	
Issued Date	2008/10/06	Deciphered Date	2010/03/12	DC Interface	
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				NAWE6 LA-5754P	0.2
				Date: Tuesday, March 02, 2010	Sheet 38 of 47

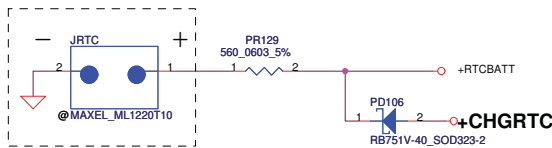
DC030006J00



Vin Detector			
	Min.	typ.	Max.
L-->H	17.430V	17.901V	18.384V
H-->L	16.976V	17.262V	17.728V

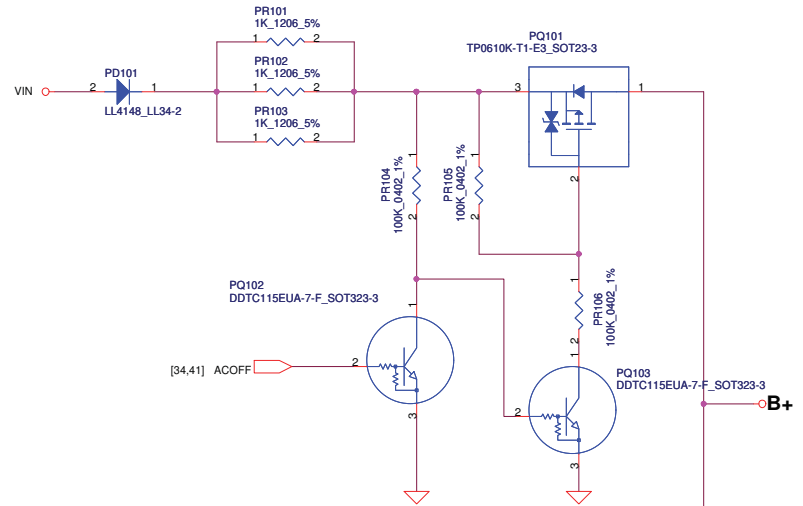


RTC Battery



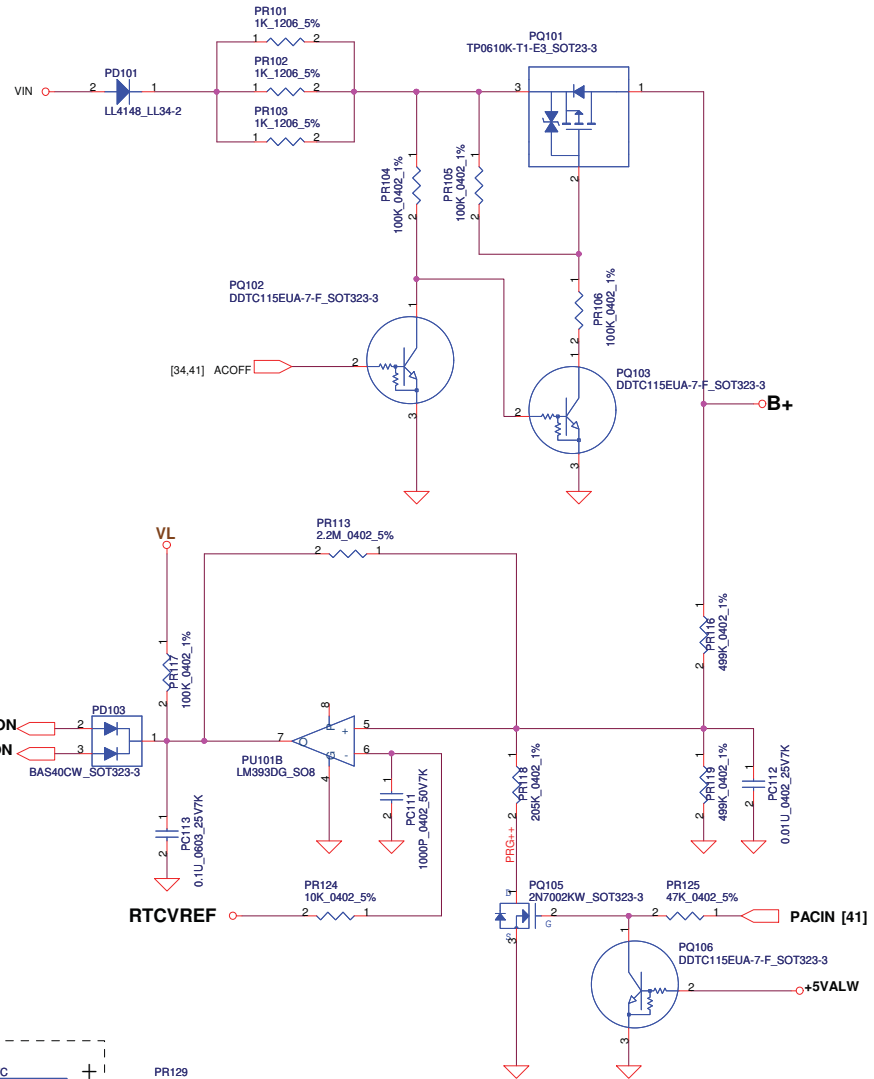
ACIN

Precharge detector			
	Min.	typ.	Max.
L-->H	14.991V	15.381V	15.782V
H-->L	13.860V	14.247V	14.621V

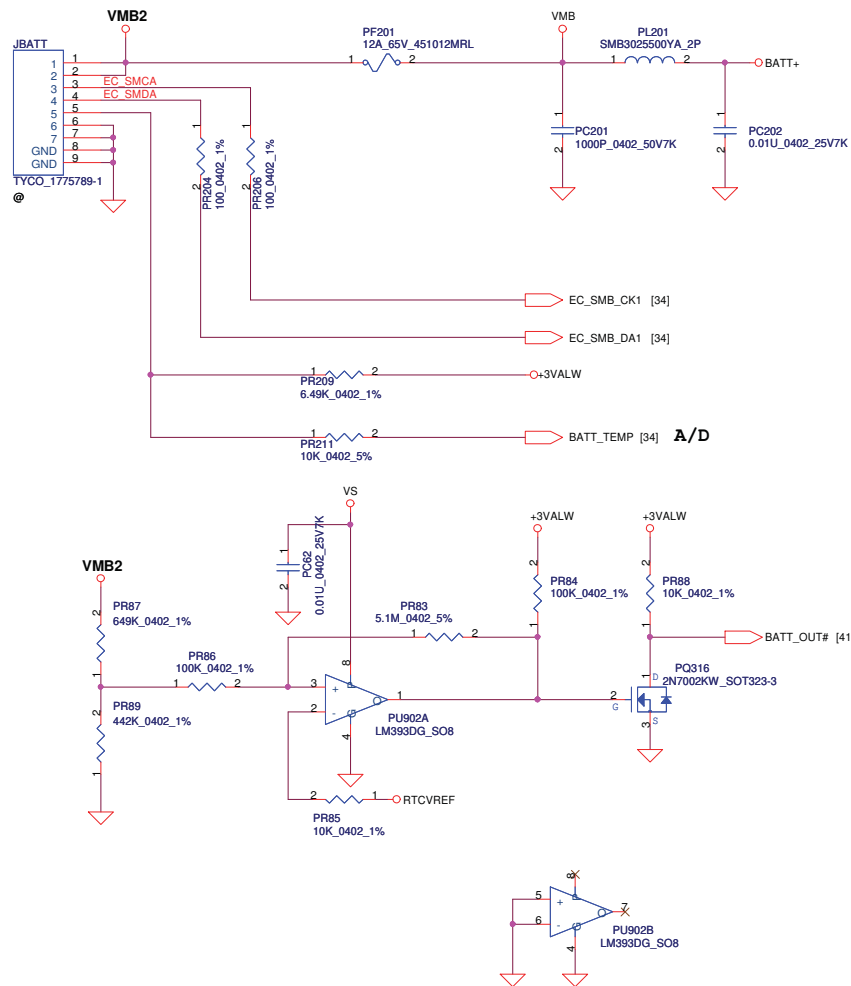


BATT ONLY

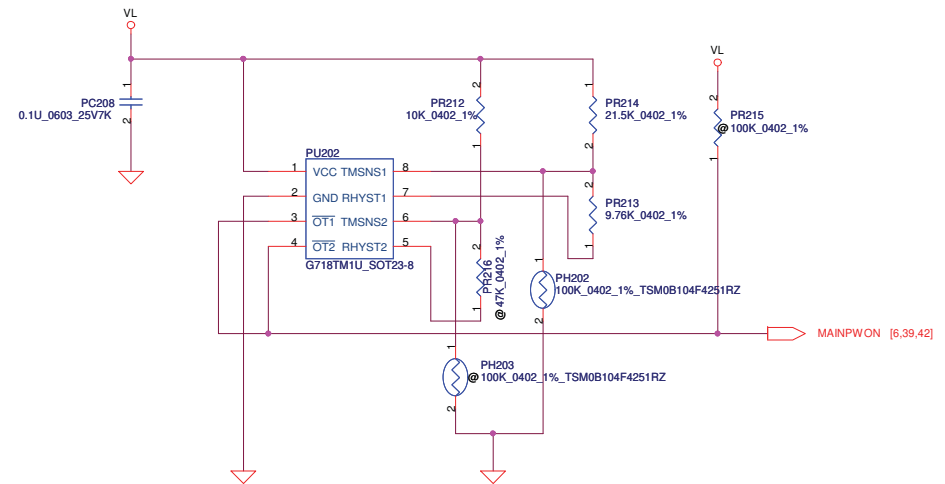
Precharge detector			
	Min.	typ.	Max.
L-->H	7.196V	7.349V	7.505V
H-->L	6.138V	6.214V	6.056V



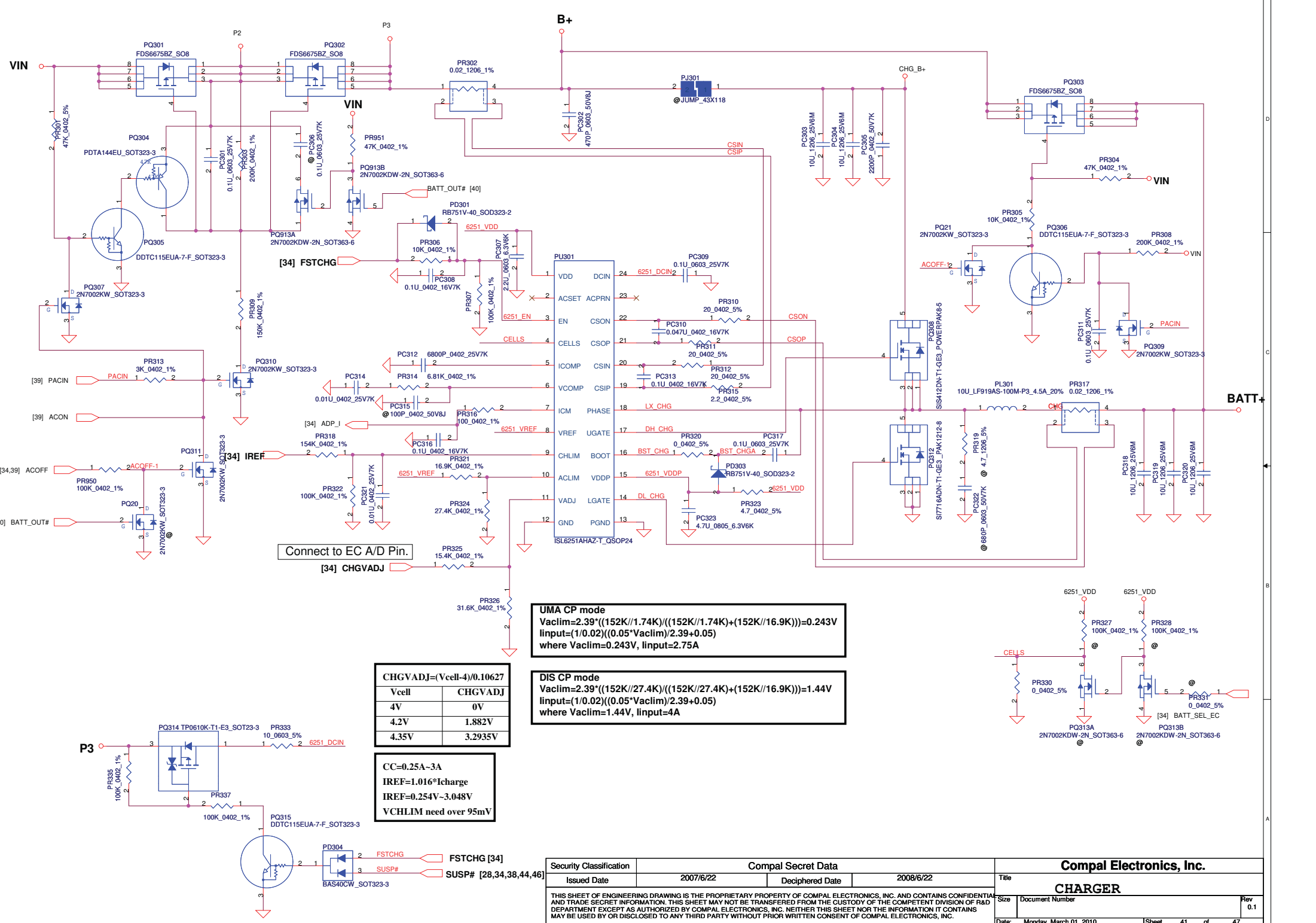
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Issued Date	2009/01/06	Deciphered Date	2010/01/06	Title		DCIN & DETECTOR		
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PH1 under CPU bottom side :
 CPU thermal protection at 92 degree C
 Recovery at 56 degree C



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Issued Date	2009/01/06	Deciphered Date	2010/01/06	Title	BATTERY CONN / OTP
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Size	Document Number				Rev
					0.1
Date:	Monday, March 01, 2010	Sheet	40	of	47



Connect to EC A/D Pin.
[34] CHGVADJ

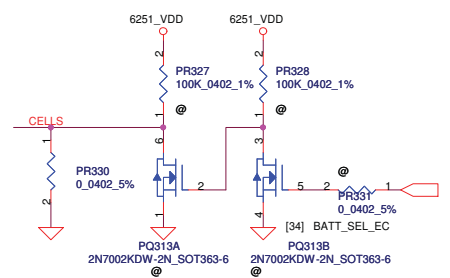
UMA CP mode
 $V_{aLim} = 2.39 * ((152K / 1.74K) / ((152K / 1.74K) + (152K / 16.9K))) = 0.243V$
 $Input = (1 / 0.02) * ((0.05 * V_{aLim}) / 2.39 + 0.05)$
 where $V_{aLim} = 0.243V$, $Input = 2.75A$

DIS CP mode
 $V_{aLim} = 2.39 * ((152K / 27.4K) / ((152K / 27.4K) + (152K / 16.9K))) = 1.44V$
 $Input = (1 / 0.02) * ((0.05 * V_{aLim}) / 2.39 + 0.05)$
 where $V_{aLim} = 1.44V$, $Input = 4A$

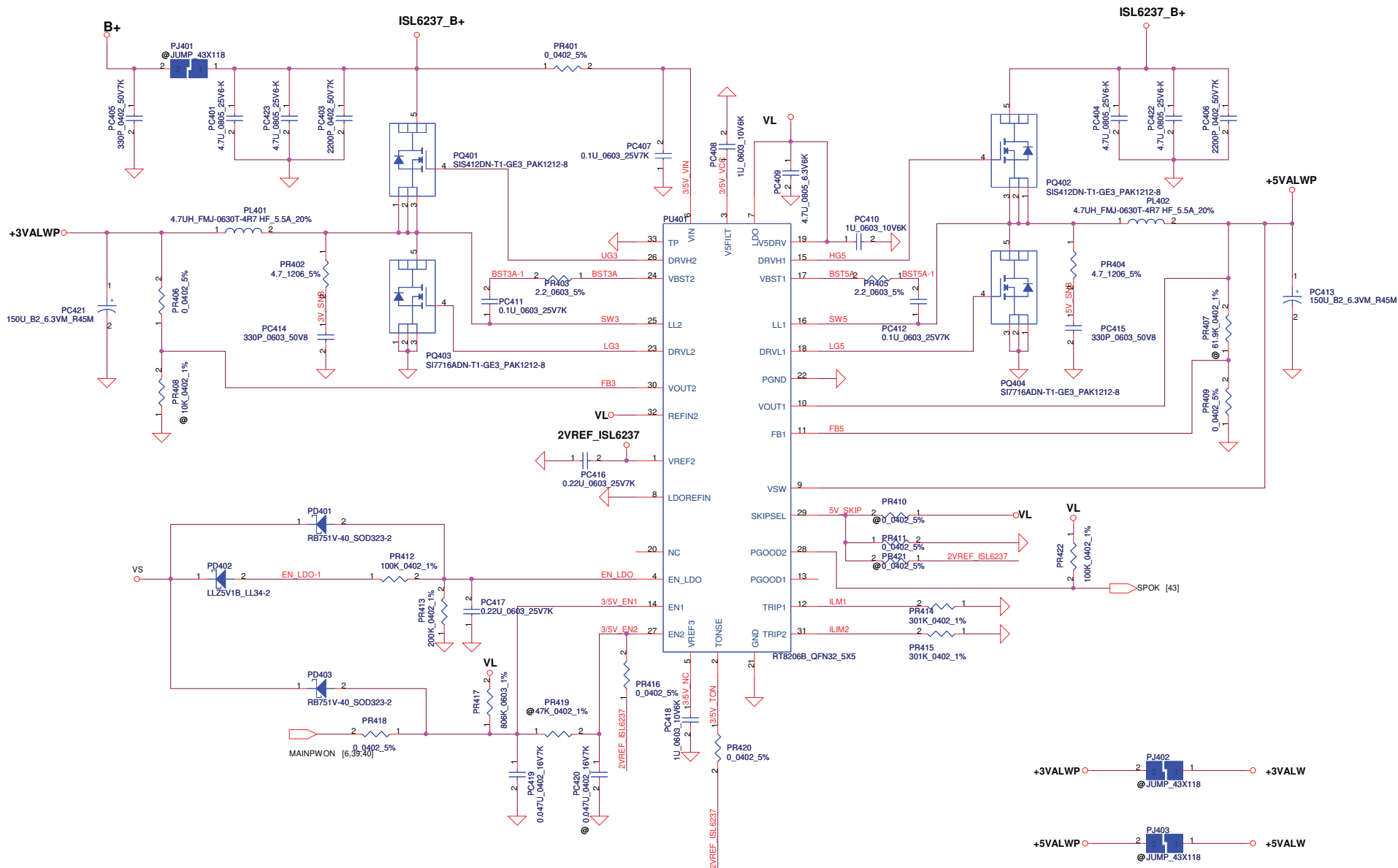
$CHGVADJ = (V_{cell} - 4) / 0.10627$

Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

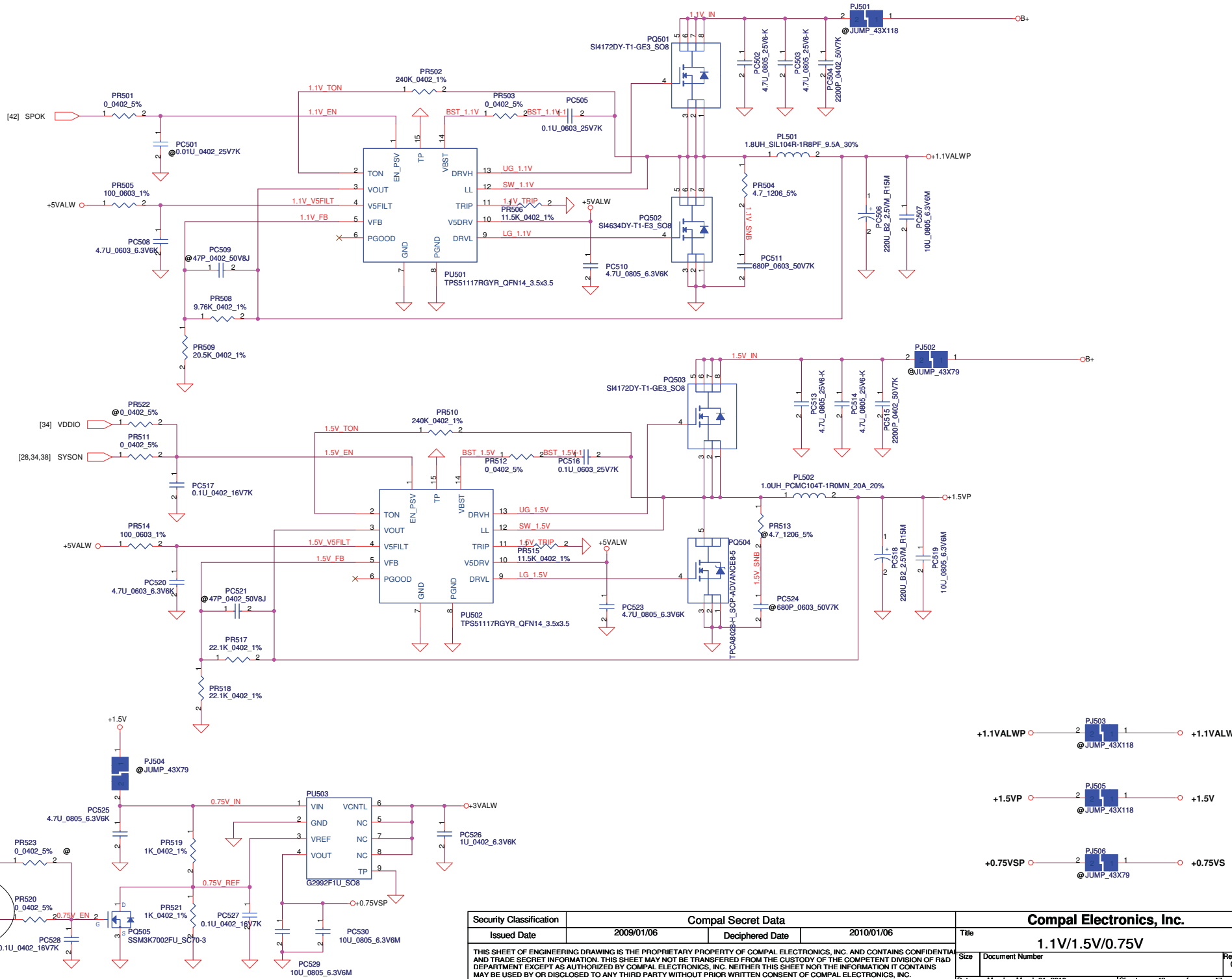
$CC = 0.25A - 3A$
 $I_{REF} = 1.016 * I_{charge}$
 $I_{REF} = 0.254V - 3.048V$
 VCHLIM need over 95mV



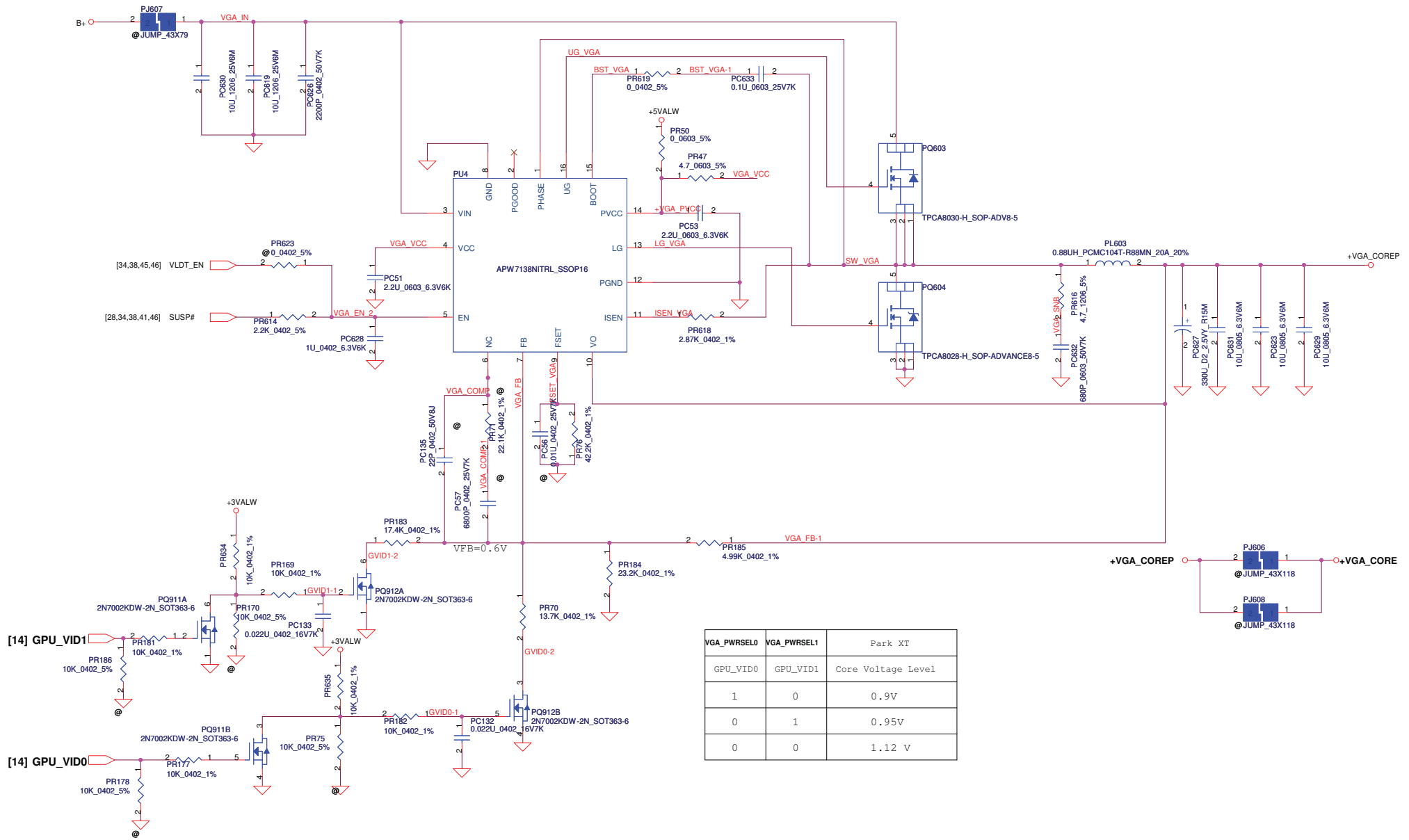
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2007/6/22	Deciphered Date	2008/6/22	Title
				CHARGER
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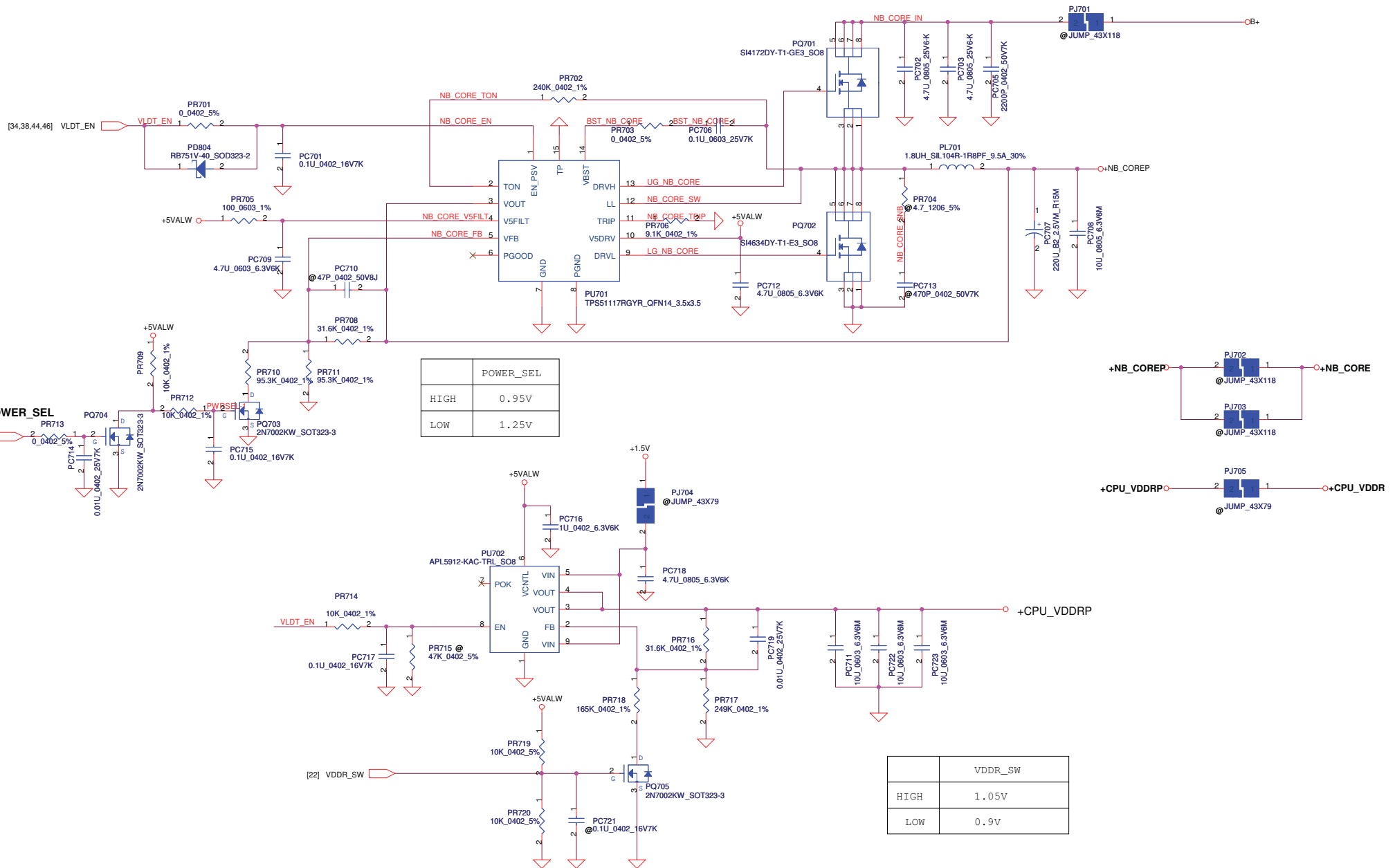


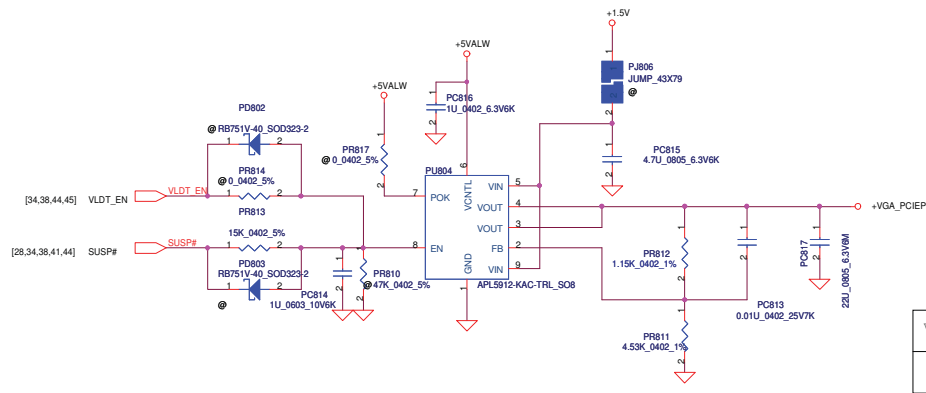
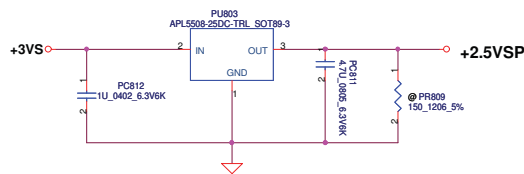
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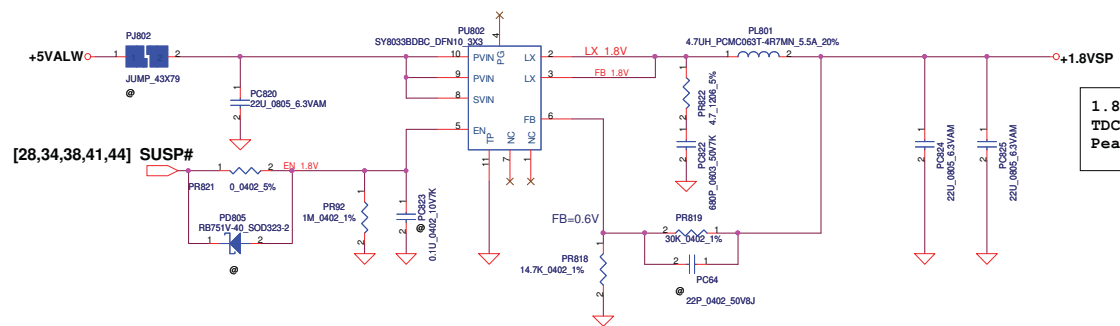
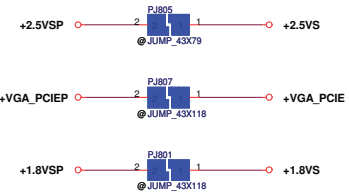
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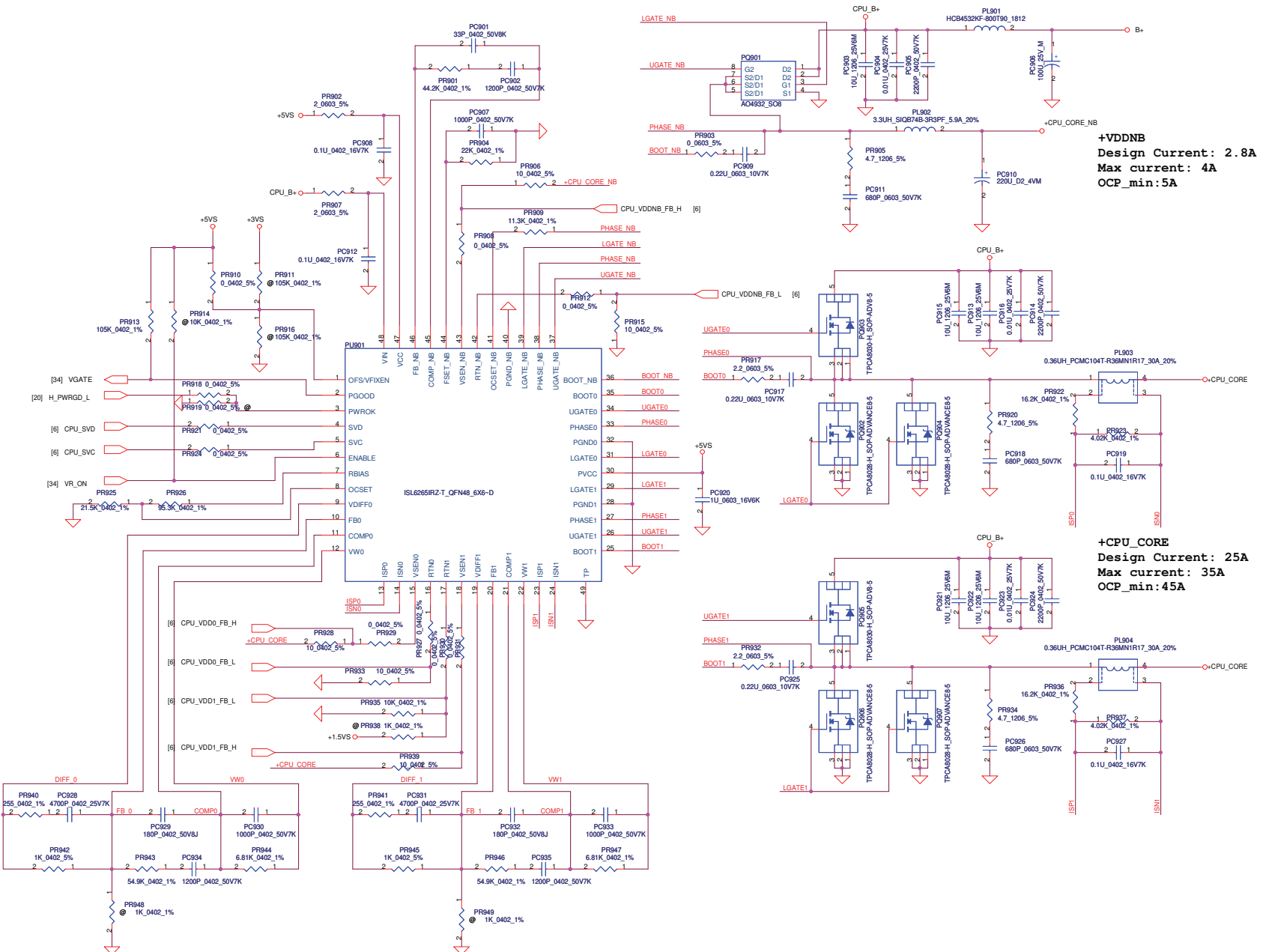




VGA_PCIE	1.0V	1.1 V
PR811	4.53K	3K



1.8VSP
TDC 2 A
Peak Current 3 A



+VDDNB
 Design Current: 2.8A
 Max current: 4A
 OCP_min:5A

+CPU_CORE
 Design Current: 25A
 Max current: 35A
 OCP_min:45A

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