

# 2010.04.07 MV Schematic

## TABLE OF CONTENTS

### MB


P02 : SYSTEM BLOCK DIAGRAM  
 P03 : CLOCK MAP  
 P04 : POWER DELIVERY CHART  
 P05 : POWER SEQUENCY DIAGRAM  
 P06 : POWER SEQUENCE CHART  
 P07 : SMBUS&I2C MAP  
 P08 : S1G4 HT I/F & PWR  
 P09 : S1G4 CTRL & DEBUG  
 P10 : S1G4 DDRIII MEMORY I/F  
 P11 : RS880M-PCIE/HT LINK/SPMEM  
 P12 : RS880M-SYSTEM I/F  
 P13 : RS880M-POWER  
 P14 : SB820M-PCIE/CPU/LPC/STRAP  
 P15 : SB820M-GPIO/USB/AZ//SATA  
 P16 : SB820M-POWER & DECOUPLING  
 P17 : DDR3(SO-DIMM\_0/1)  
 P18 : VGA\_S3 (PCI-E) 1/3  
 P19 : VGA (IO)/(STRAP) 2/3  
 P20 : VGA\_S3 (POWER) 3/3  
 P21 : VRAM (DDR3)  
 P22 : EC+KBC (IT8502E) & ROM  
 P23 : Audio (CODEC\_ALC270A)

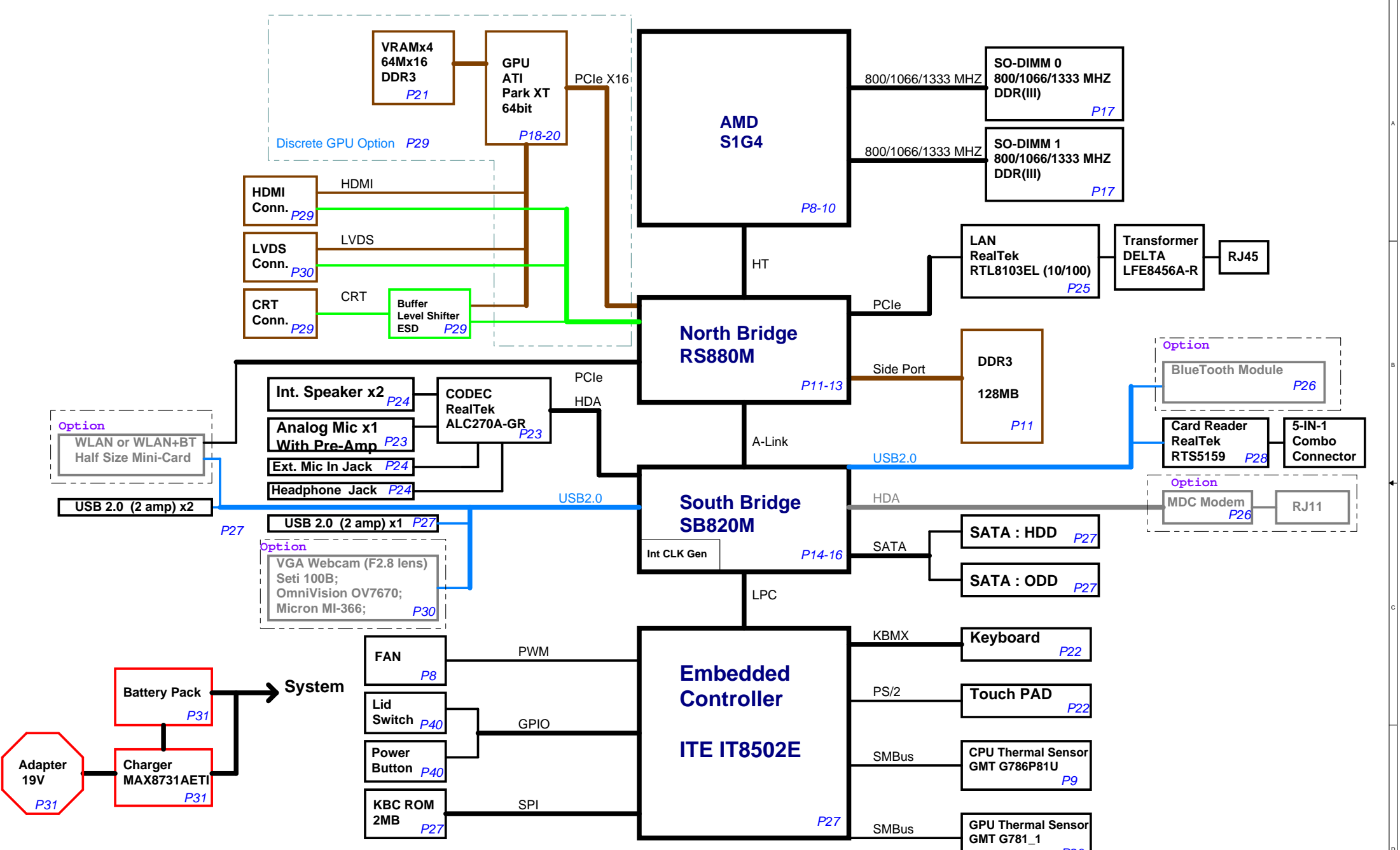
P24 : Audio (JACK+AMP+SPK+Mute)  
 P25 : LAN(RTL8103EL)  
 P26 : Mini PCIE & RJ11 & BT  
 P27 : USBX2/USB DB/SATA CONN.  
 P28 : Card Reader  
 P29 : HDMI & CRT  
 P30 : LVDS&Webcam  
 P31 : PWR\_Charger MAX8731AETI  
 P32 : 5V/3.3V SN0608098RHBT  
 P33 : Vcore MAX17480  
 P34 : +V1.1S TPS51117 & VDDR  
 P35 : +V1.8S RT8253ALGS & VDDA  
 P36 : PWR\_Others power plane  
 P37 : +VCCNB & 1.5VDDR3 +0\_75V  
 P38 : ATVDD TPS51217 & +VPCIE  
 P39 : Stitch CAP

### Daughter Board

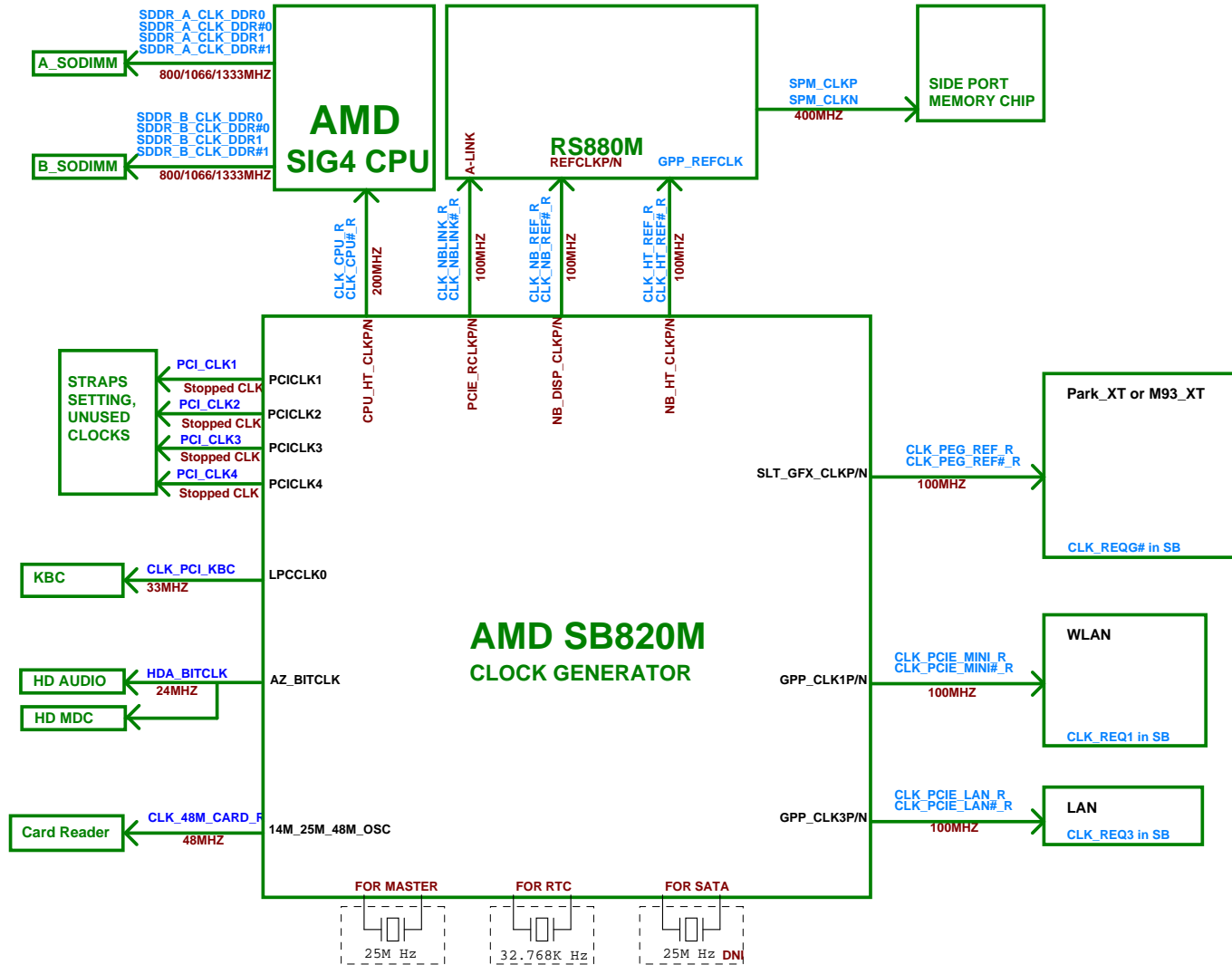
P40 -- Power Board / USB Board / SW Board

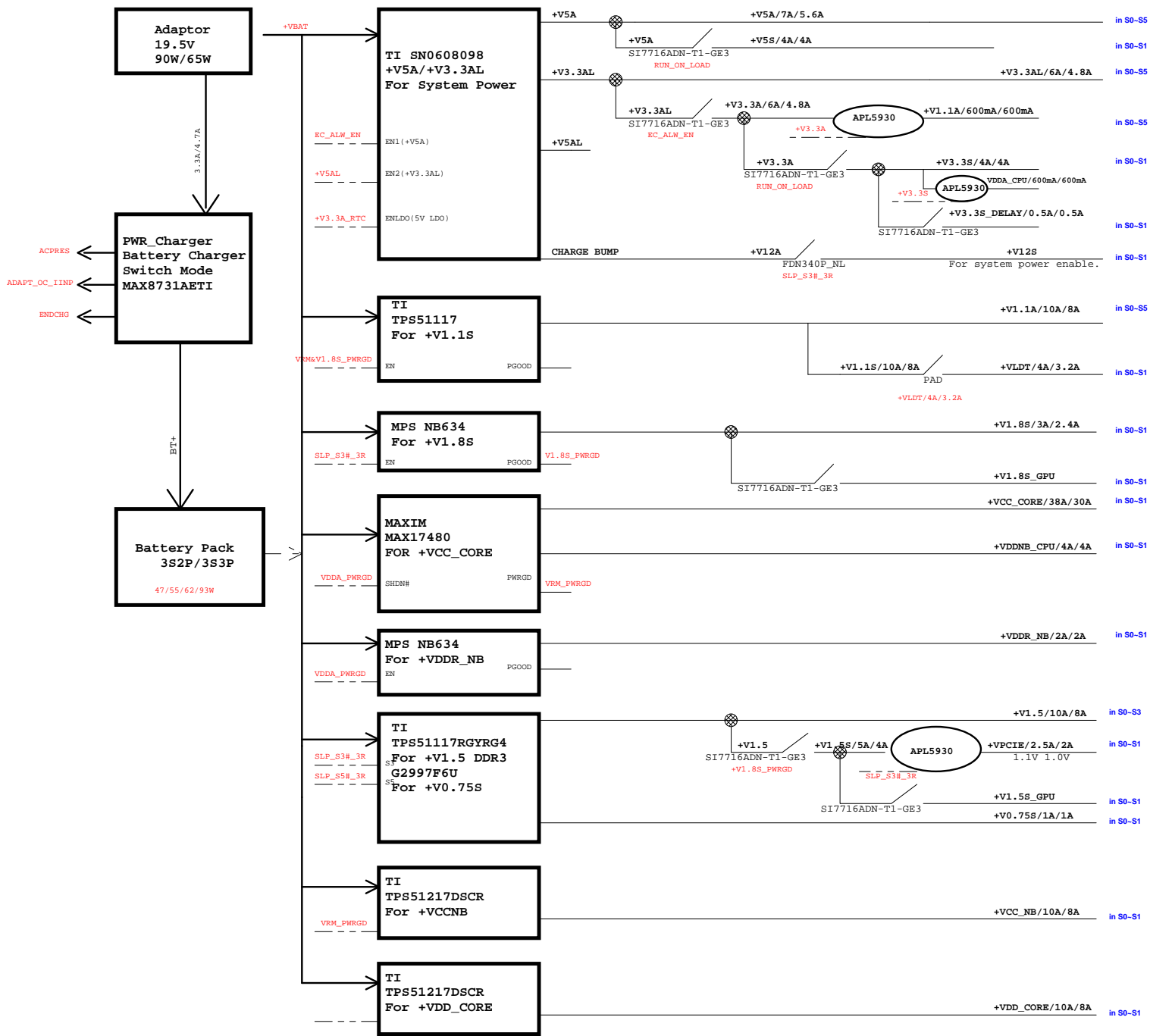
P. Leader	Check by	Design by

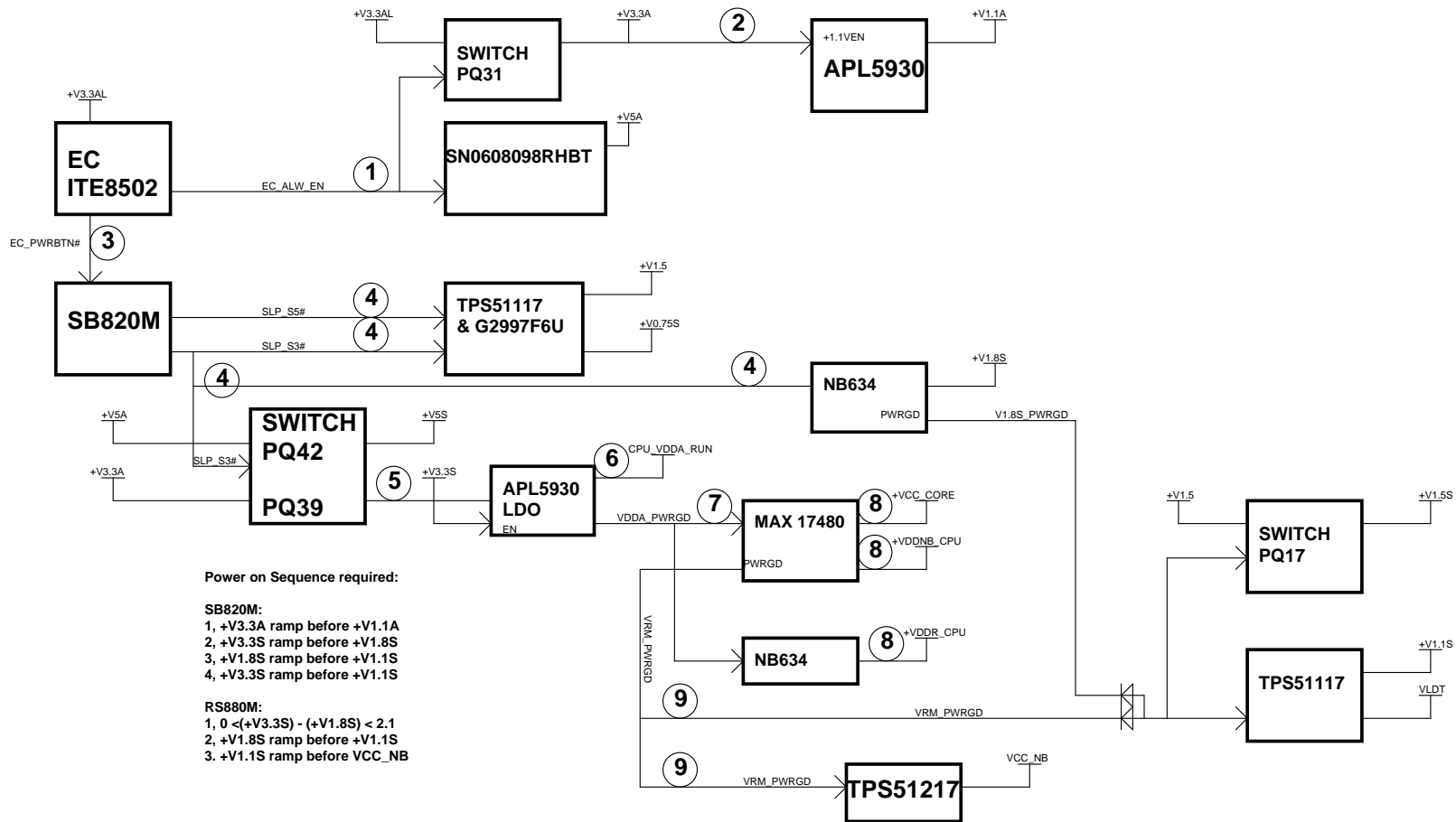
		Hon Hai Precision Industry Co. Ltd. Foxconn eMS Inc. HNBD R&D		phone: +886-2-2799-6111	
Title					
TABLE OF CONTENTS					
Size	Document Number				Rev
Custom	Safina				MV
Page Modified: Wednesday, April 07, 2010		121112 (UTC/GMT)		Sheet 1 of 39	



# INTERNAL CLOCK MODE







**Power on Sequence required:**

**SB820M:**

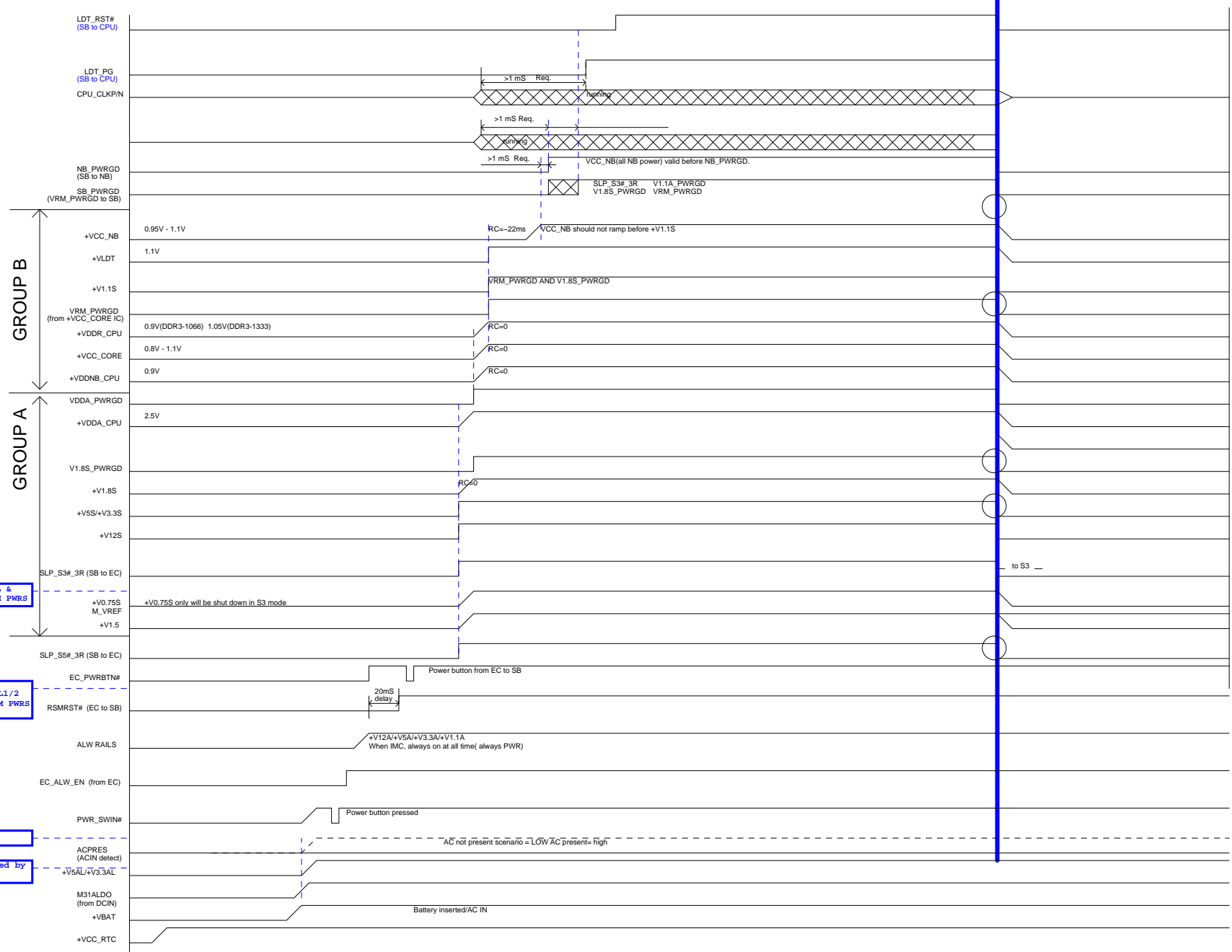
- 1, +V3.3A ramp before +V1.1A
- 2, +V3.3S ramp before +V1.8S
- 3, +V1.8S ramp before +V1.1S
- 4, +V3.3S ramp before +V1.1S

**RS880M:**

- 1,  $0 < (+V3.3S) - (+V1.8S) < 2.1$
- 2, +V1.8S ramp before +V1.1S
- 3, +V1.1S ramp before VCC\_NB

GROUP B

GROUP A



**Power on Sequence required:**

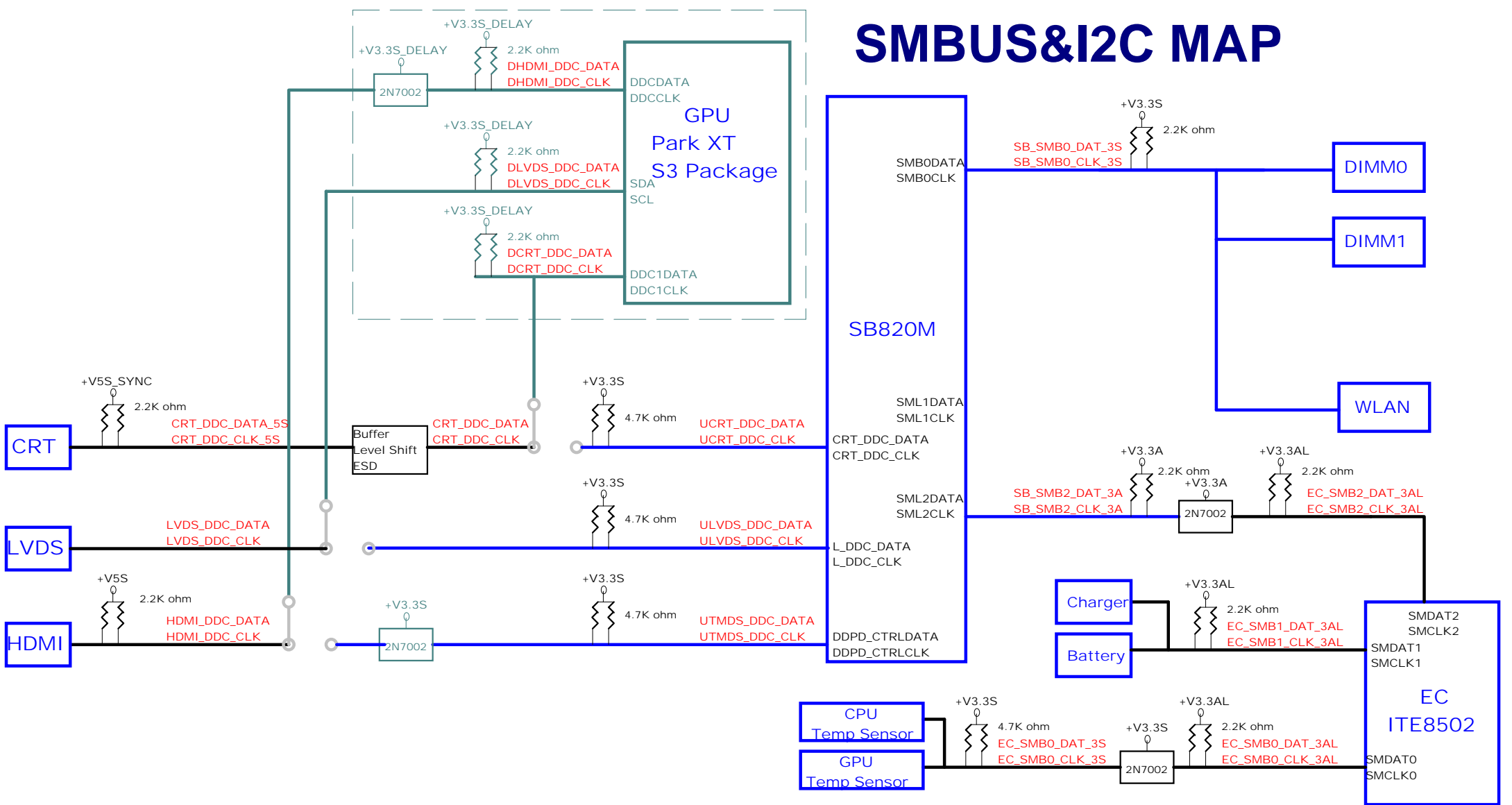
**SB820:**

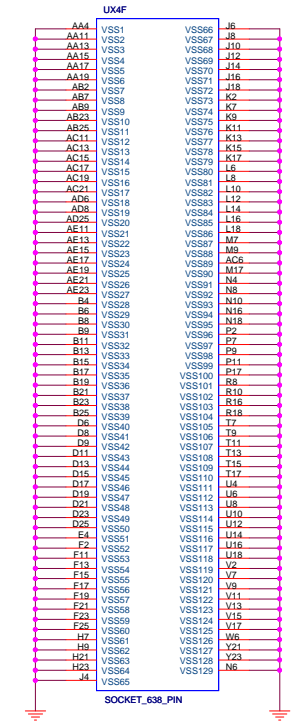
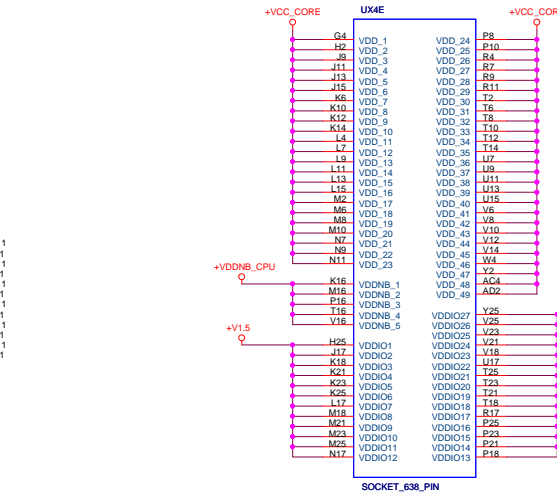
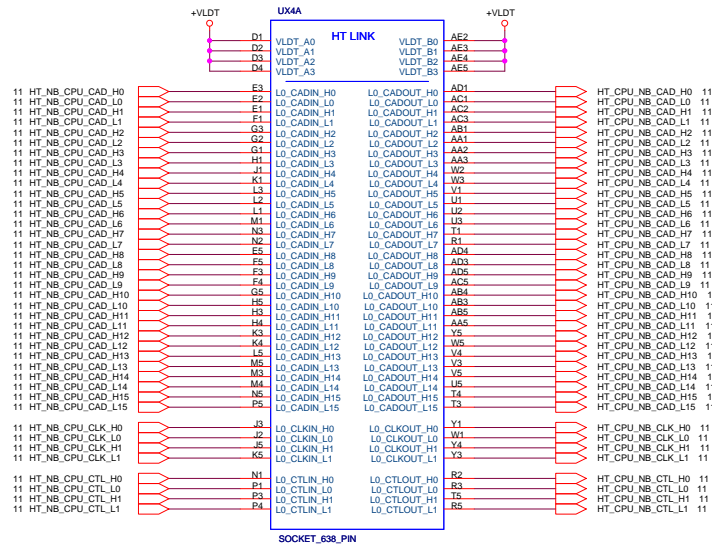
- 1, +V3.3A ramp before +V1.1A
- 2, +V3.3S ramp before +V1.8S
- 3, +V1.8S ramp before +V1.1S
- 5, +V3.3A ramping down time > 300us
- 6, 50uS <= All power rails except +V3.3A <= 40mS
- 7, 100uS <= +V3.3A <= 40mS

**RS880M:**

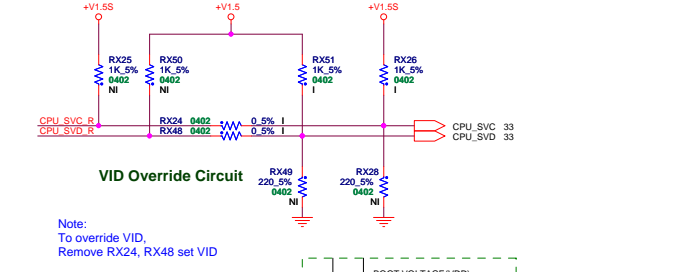
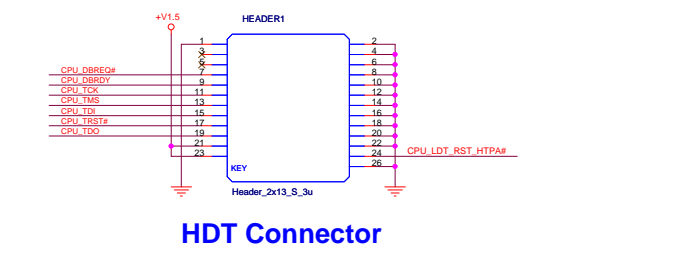
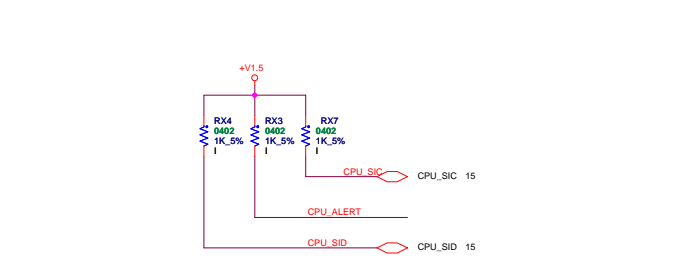
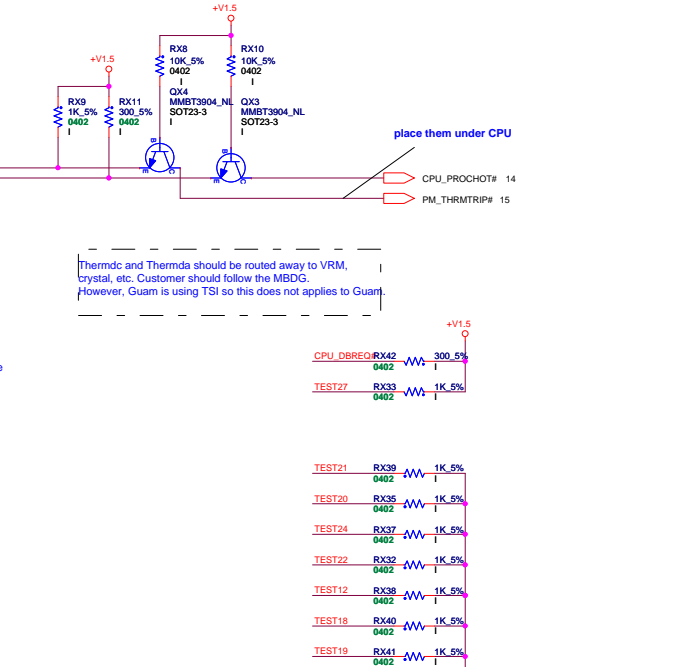
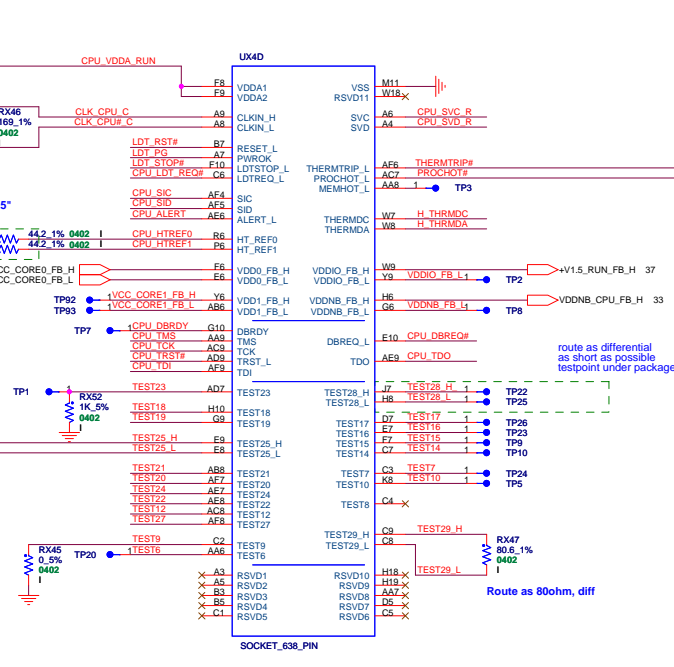
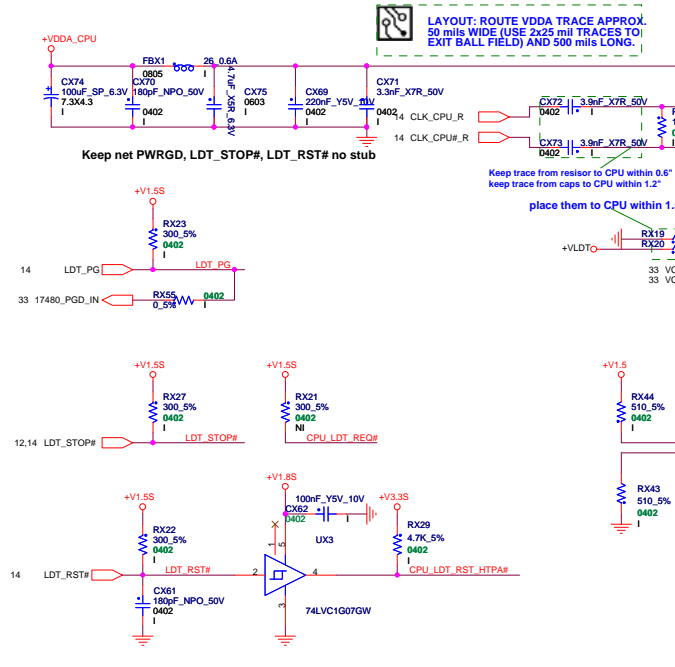
- 1, 0 <(+V3.3S) - (+V1.8S) < 2.1
- 2, +V1.8S ramp before +V1.1S
- 3, +V1.1S ramp before +VCC\_NB

# SMBUS&I2C MAP



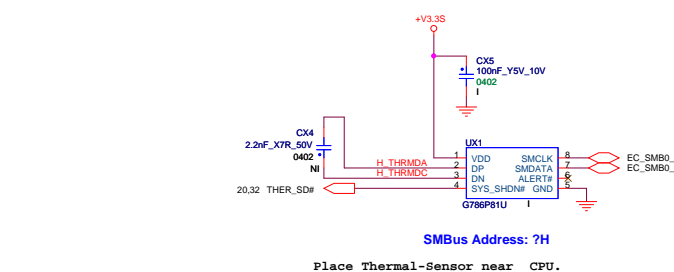
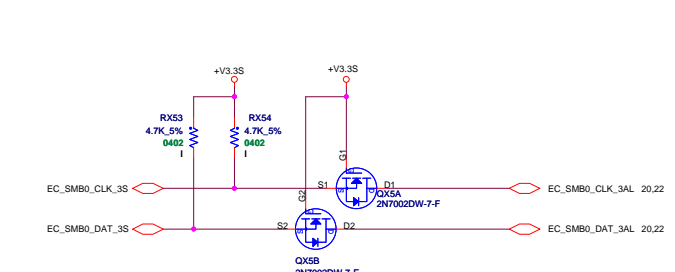






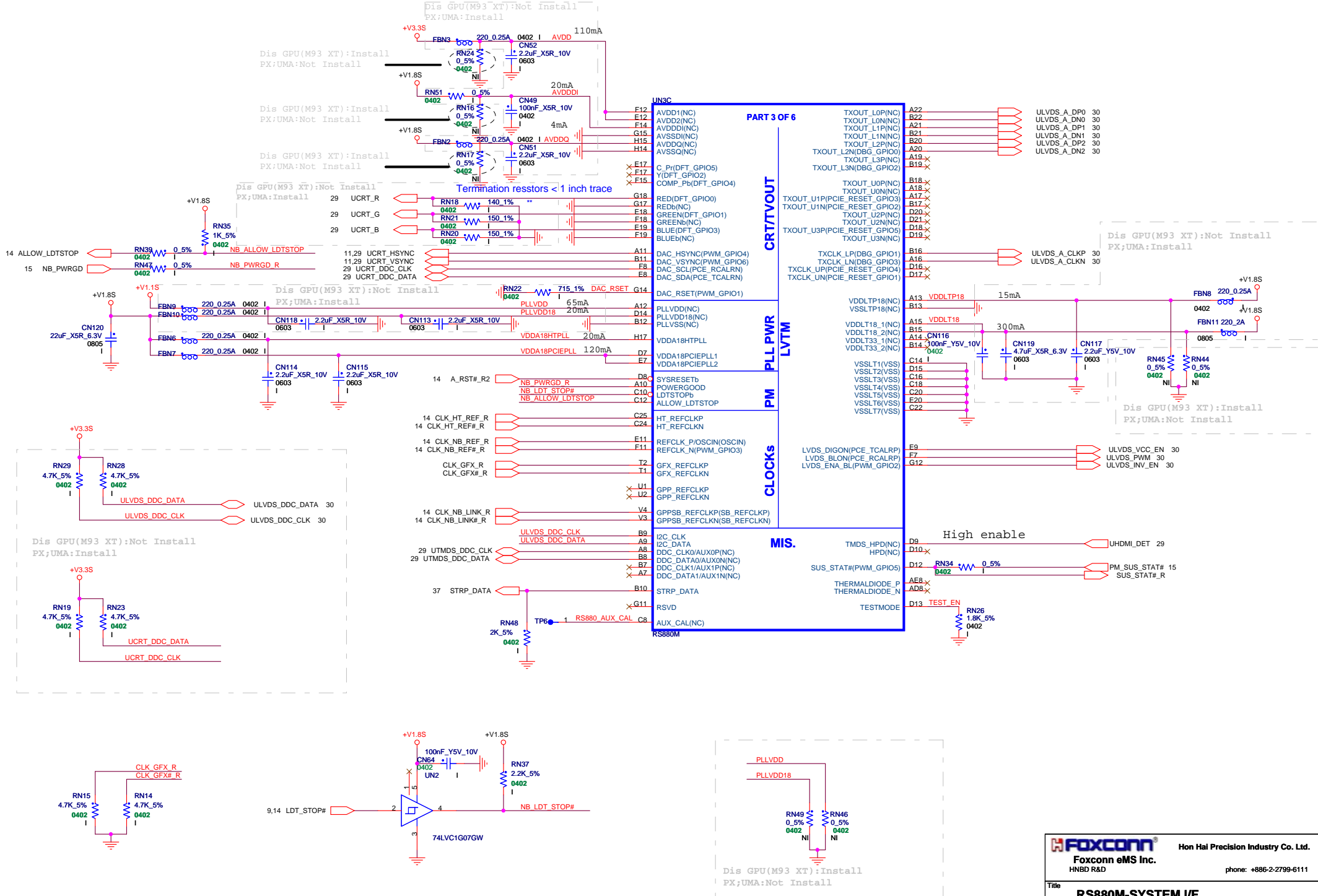
SVC		SVD		BOOT VOLTAGE(VDD)	
		(CPU/VRM PROG = +VCC/GND)		(CPU/VRM PROG = OPEN)	
0	0	1.1	1.1		
0	1	1.0	1.2		
1	0	0.9	1.0		
1	1	0.8	0.8		

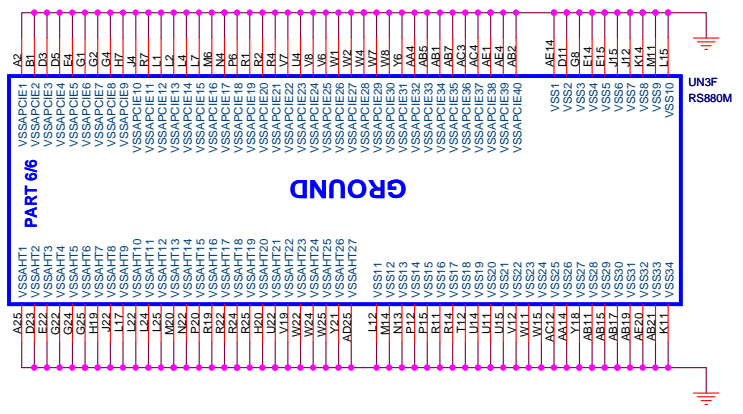
VID OVERRIDE TABLE (VDD)





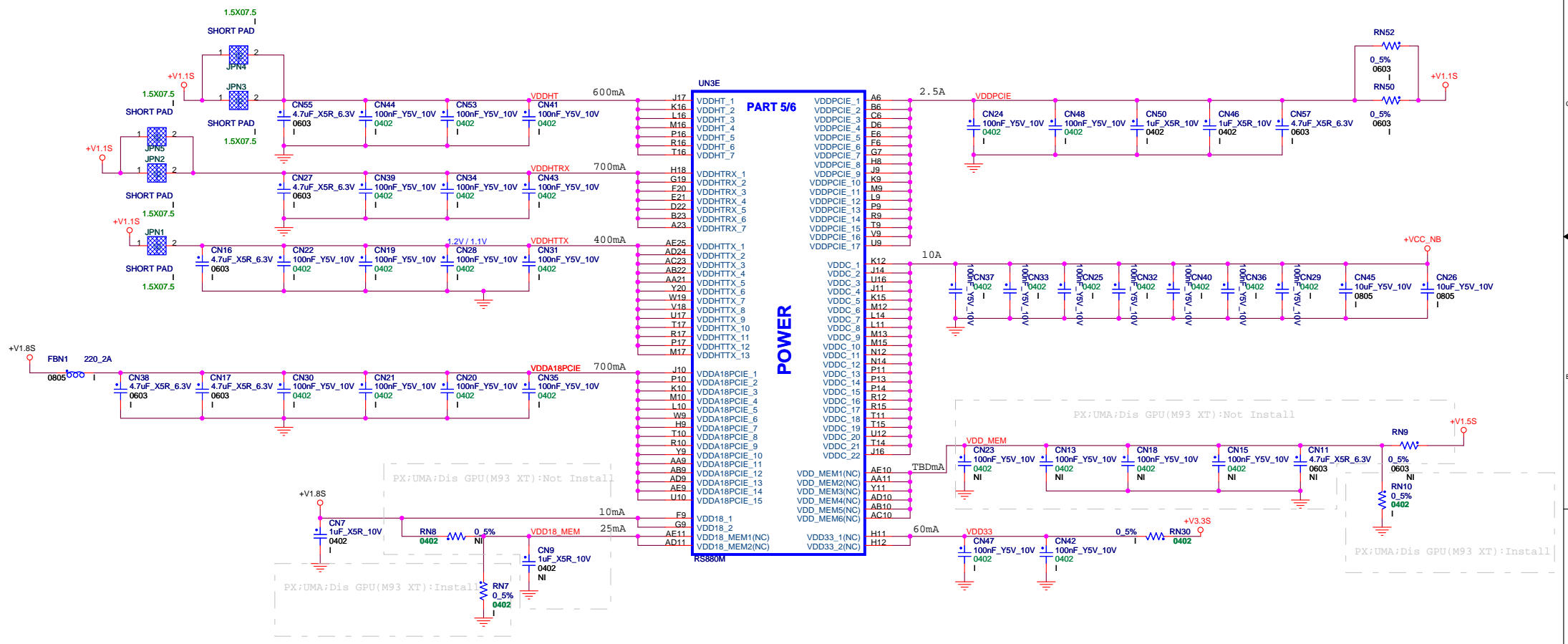






**RS880M POWER TABLE**

PIN NAME	RS880M	PIN NAME	RS880M
VDDHT	+1.1V	IOPLLVD	+1.1V
VDDHTRX	+1.1V	AVDD	+3.3V
VDDHTTX	+1.2V	AVDDI	+1.8V
VDDA18PCIE	+1.8V	AVDDQ	+1.8V
VDDG18	+1.8V	PLLVD	+1.1V
VDD18_MEM	+1.8V	PLLVD18	+1.8V
VDDPCIE	+1.1V	VDDA18PCIEPLL	+1.8V
VDDC	+1.1V	VDDA18HTPLL	+1.8V
VDD_MEM	+1.8V/1.5V	VDDLTP18	+1.8V
VDDG33	+3.3V	VDDL18	+1.8V
IOPLLVD18	+1.8V	VDDL33	NC



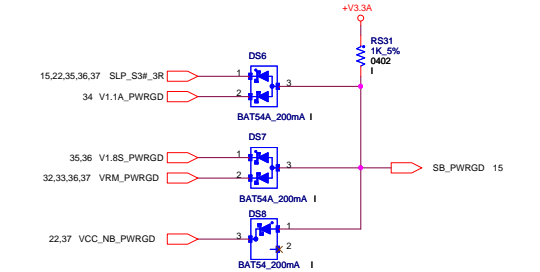
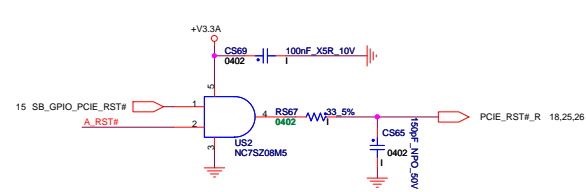
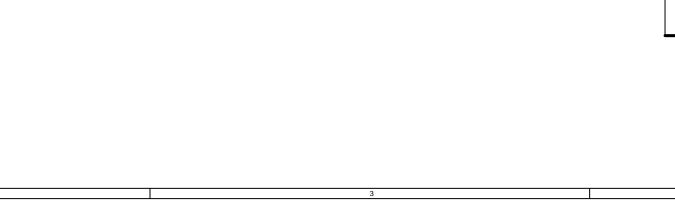
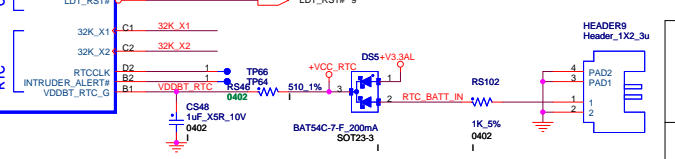
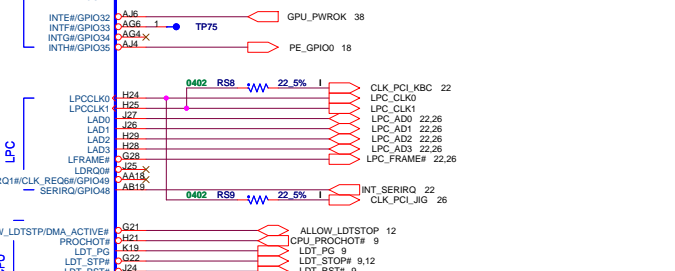
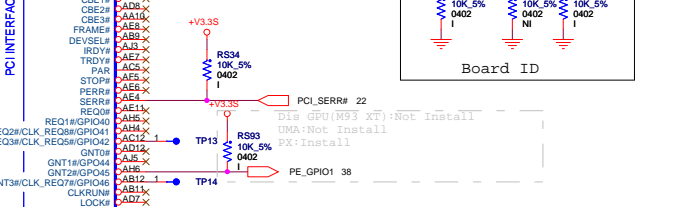
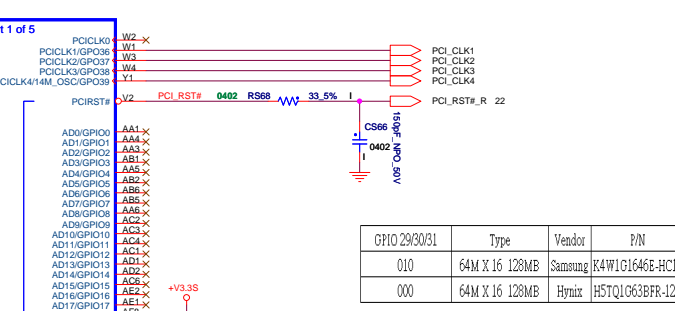
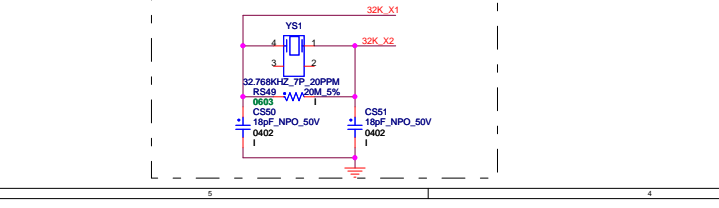
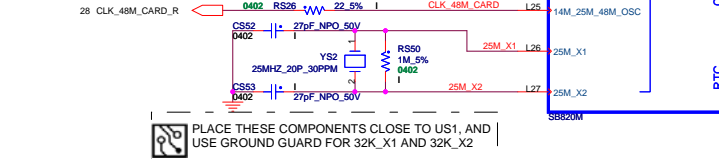
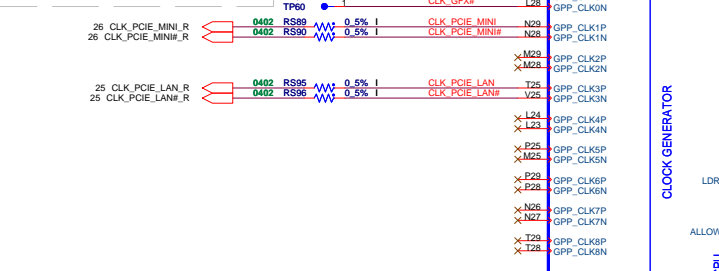
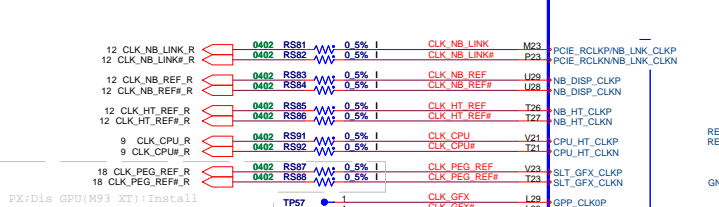
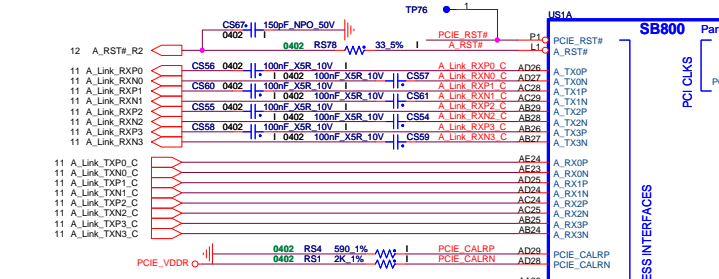
**FOXCONN** Hon Hai Precision Industry Co. Ltd.  
Foxconn eMS Inc.  
HNBD R&D phone: +886-2-2799-6111

Title: **RS880M-POWER**

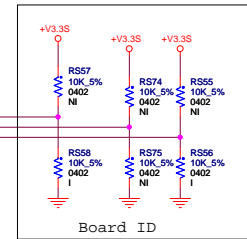
Size	Document Number	Rev
Custom	Safina	MV

Page Modified: Wednesday, April 07, 2010 18:48:16 (UTC+08MT) Sheet 13 of 39

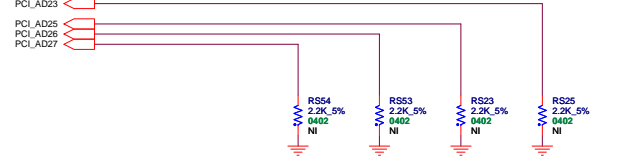
**PLACE THESE PCIE AC COUPLING CAPS CLOSE TO US1**



GPIO 29/30/31	Type	Vendor	P/N
010	64M X 16 128MB	Samsung	K4W1G1646E-HC12
000	64M X 16 128MB	Hynix	H5TQ1G63BFR-12C

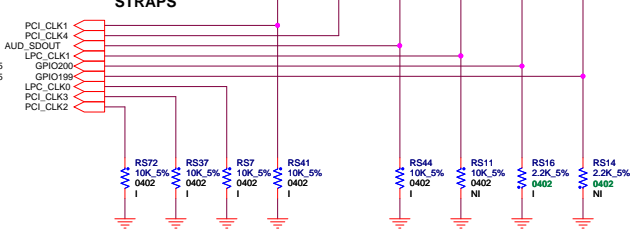


**DEBUG STRAPS**



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD23
<b>PULL HIGH</b>	USE PCI PLL	DISABLE ILA AUTORUN	USE FC PLL	DISABLE PCI MEM BOOT
	DEFAULT	DEFAULT	DEFAULT	DEFAULT
<b>PULL LOW</b>	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	ENABLE PCI MEM BOOT

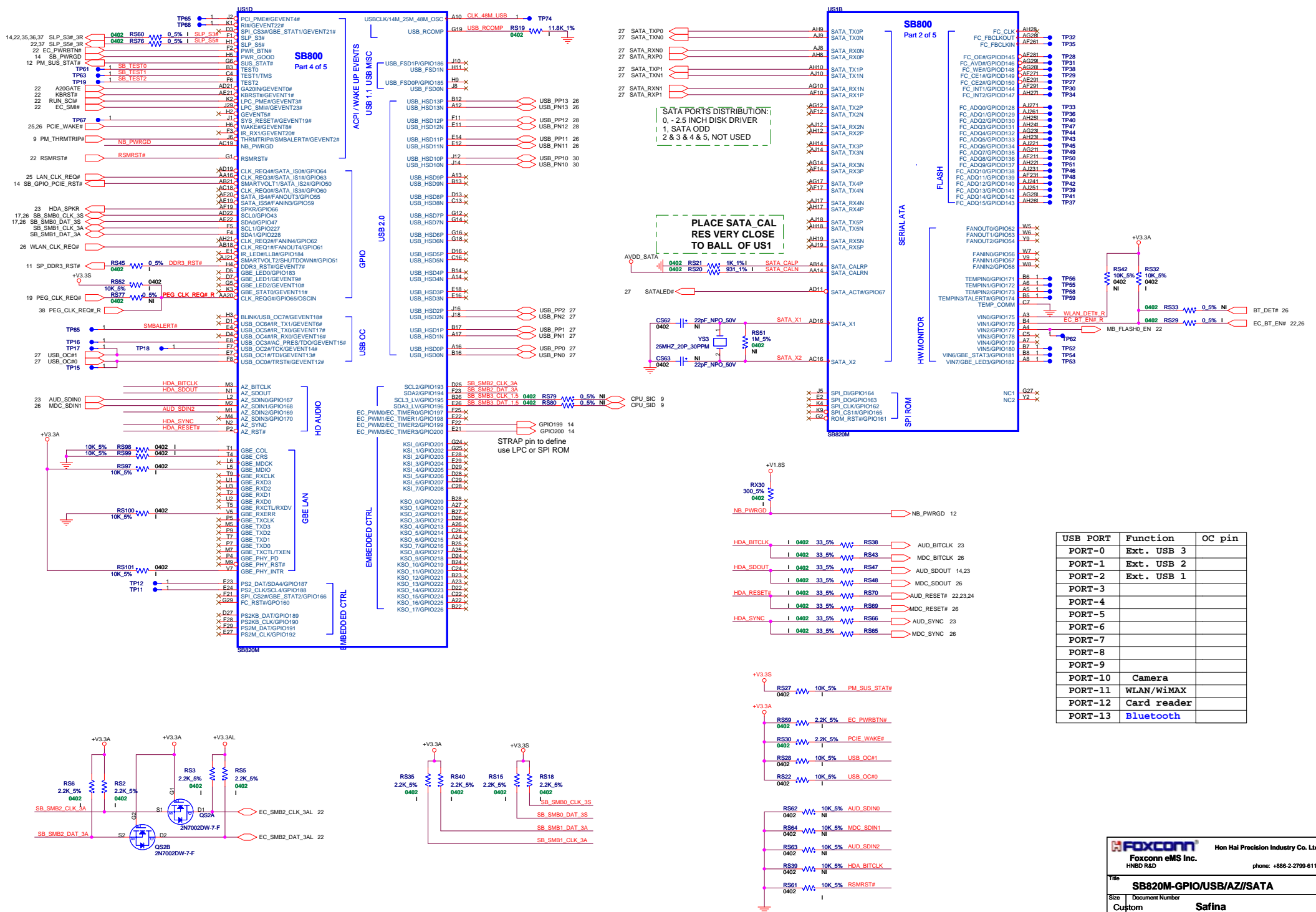
**REQUIRED STRAPS**



	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200	GPIO199
<b>PULL HIGH</b>	LOW POWER MODE	ALLOW PCIE Gen2	Watchdog Timer Enabled	USE DEBUG STRAP	non Fusion CLOCK MODE	EC ENABLED	CLKGEN ENABLED	H,H = Reserved H,L = SPI ROM	
	DEFAULT	DEFAULT	DEFAULT	DEFAULT	DEFAULT	DEFAULT	DEFAULT		
<b>PULL LOW</b>	PERFORMANCE MODE	FORCE PCIE Gen1	Watchdog Timer Disabled	IGNORE DEBUG STRAP	FUSION CLOCK MODE	EC DISABLED	CLKGEN DISABLED	L,H = LPC ROM (Default) L,L = FWH ROM	

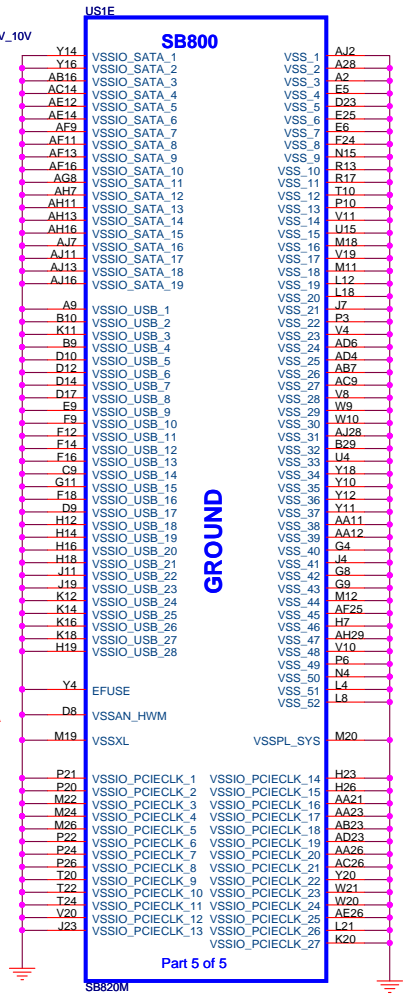
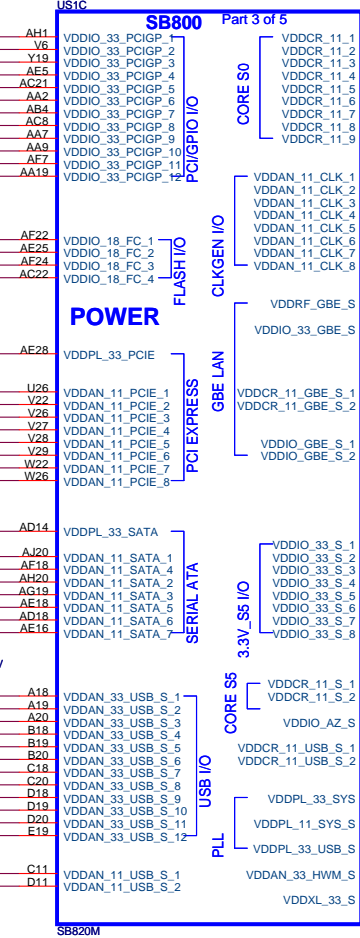
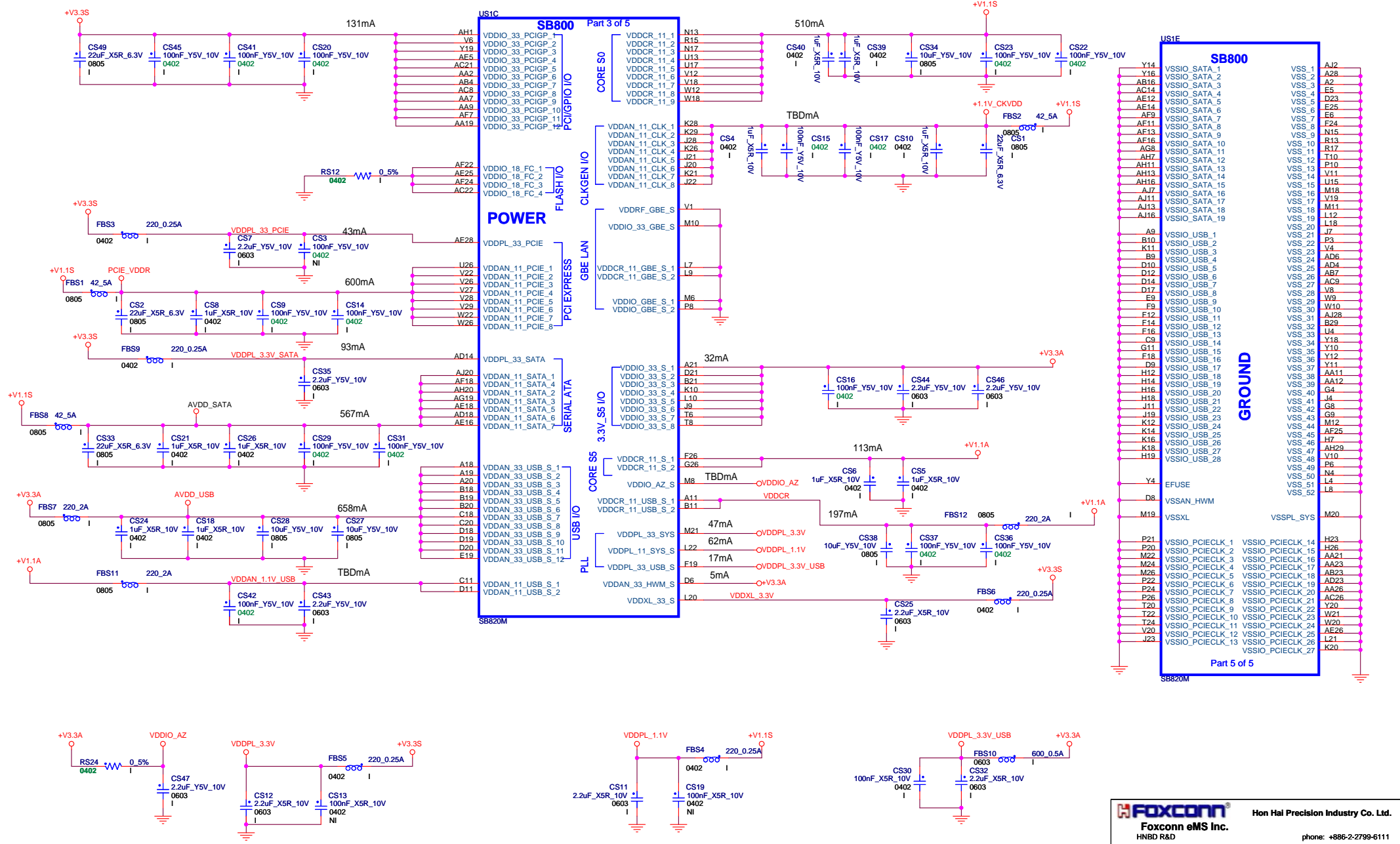
**FOXCONN** Hon Hai Precision Industry Co. Ltd.  
Foxconn eMS Inc.  
HNB0 R&D phone: +886-2-2799-6111

Title: **SB820M-PCIE/CPU/LPC/STRAP**  
Size: Document Number  
Customer: **Safina** Rev: MW  
Page Modified: Wednesday, April 27, 2011 18:48:18 (UTC+08) Sheet 14 of 39





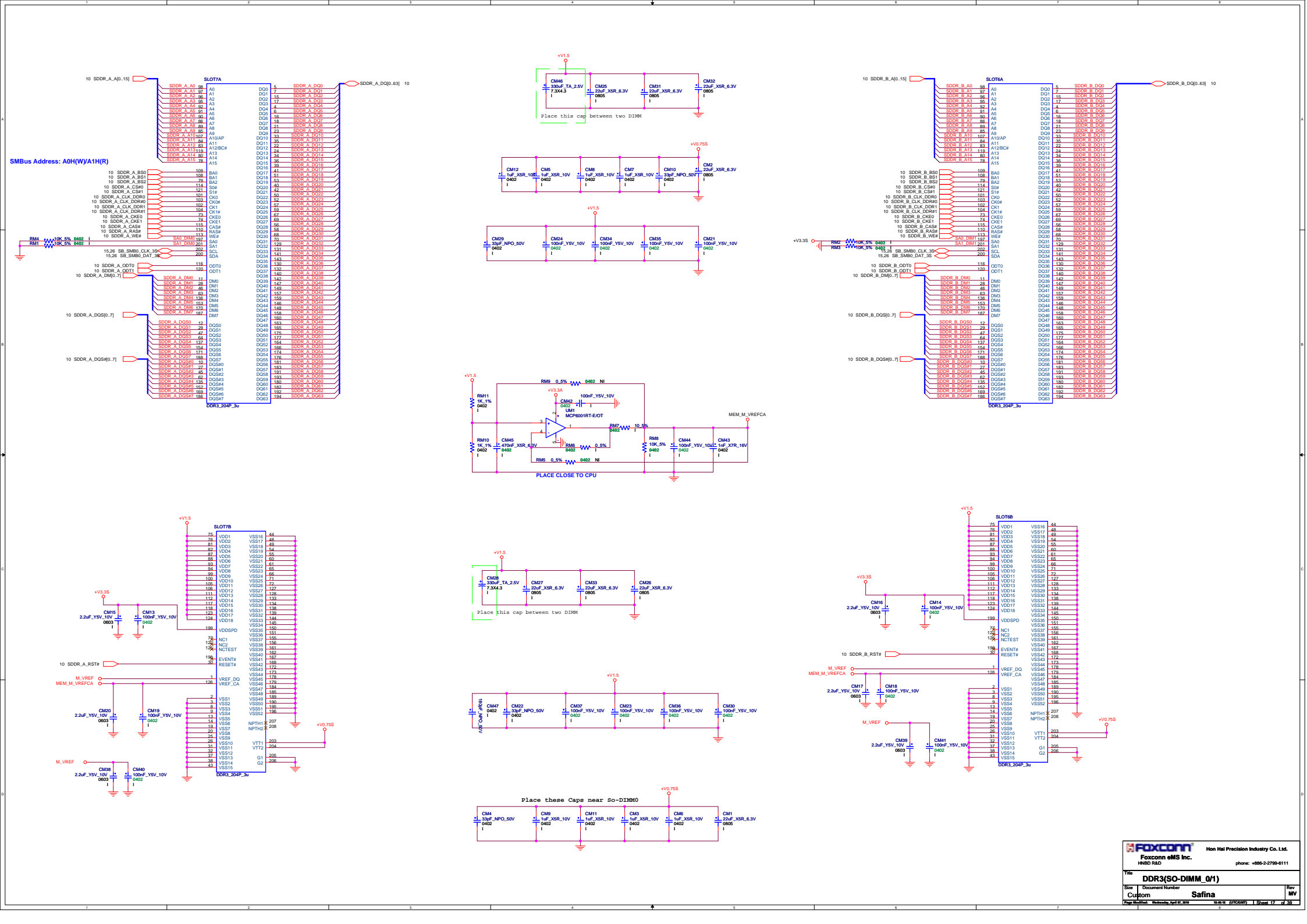
PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.

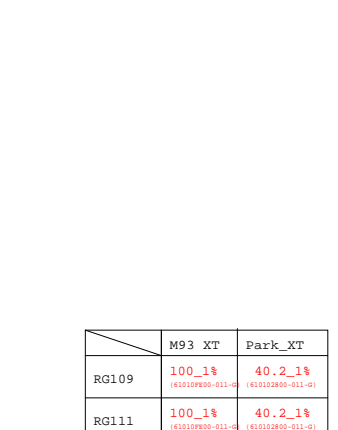
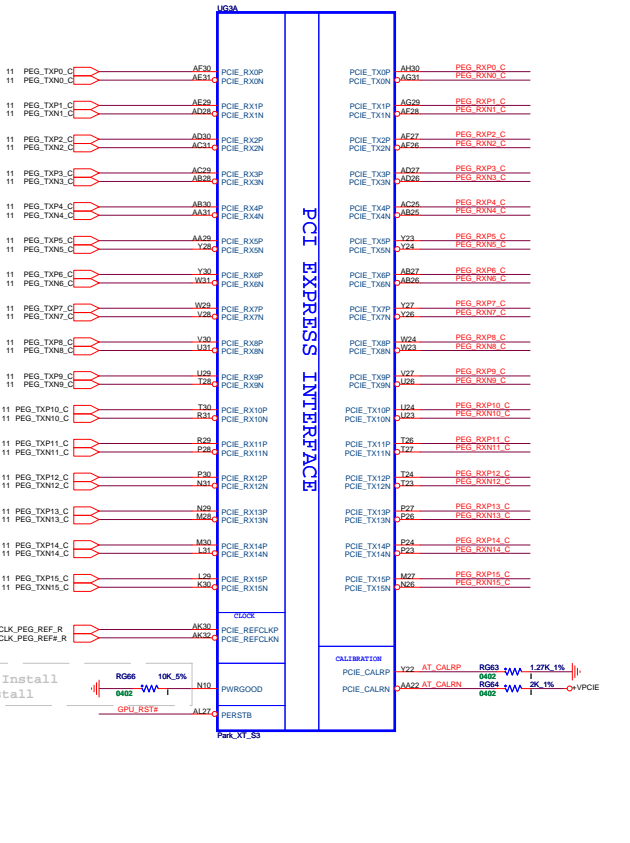


**FOXCONN** Hon Hai Precision Industry Co. Ltd.  
 Foxconn eMS Inc. HNBDR&D phone: +886-2-2799-6111

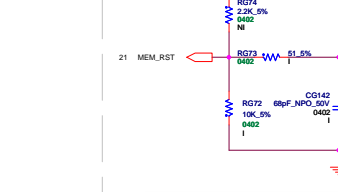
Title <b>SB820-POWER &amp; DECOUPLING</b>		
Size	Document Number	Rev
Custom	<b>Safina</b>	MV
Page Modified: Wednesday, April 07, 2010 18:49:17 (UTC+0800)		Sheet 16 of 39



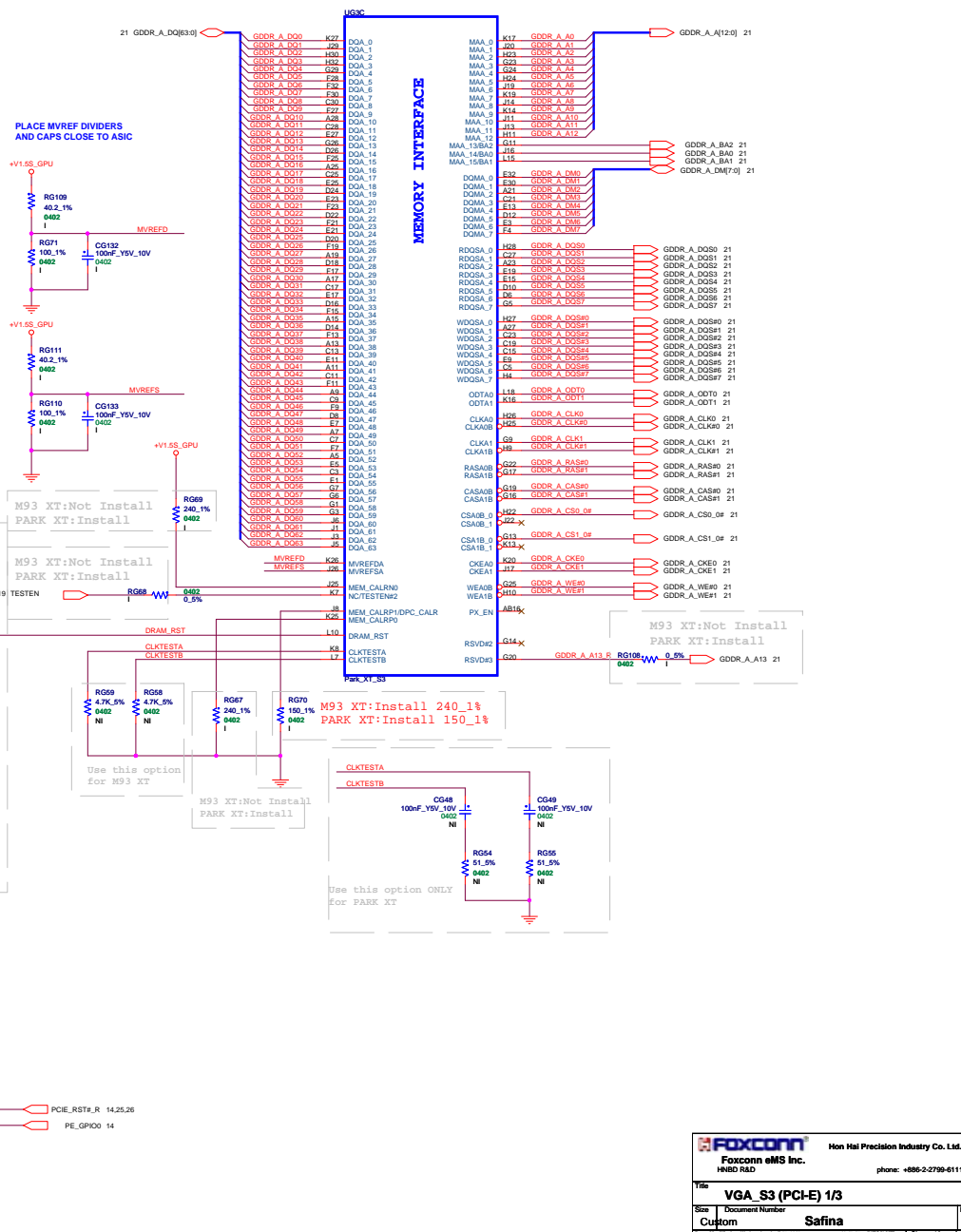
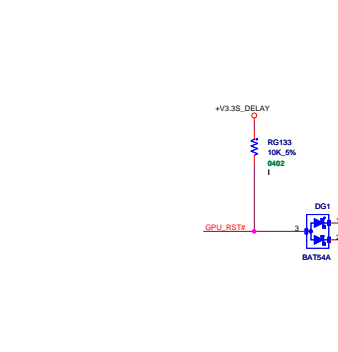


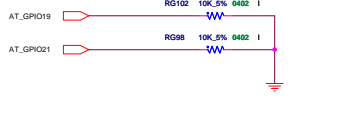
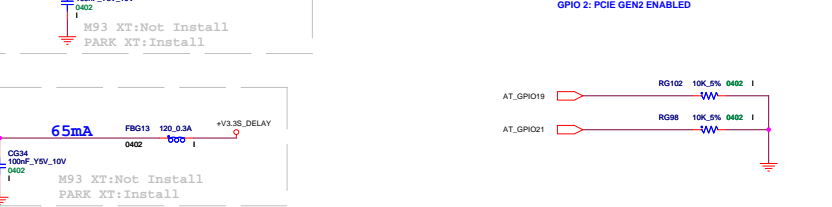
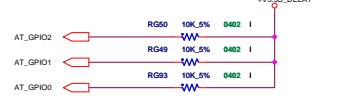
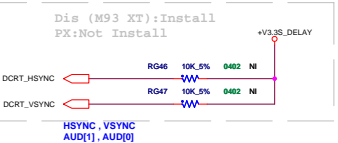
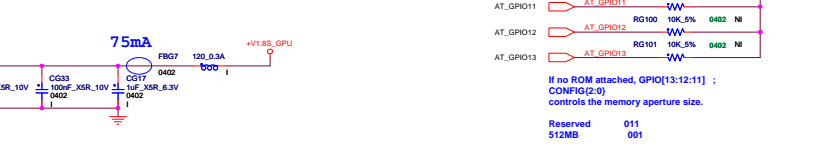
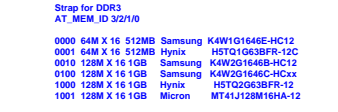
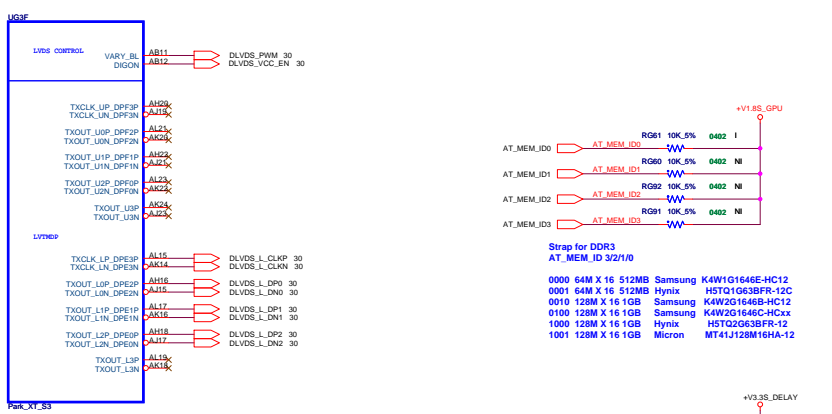
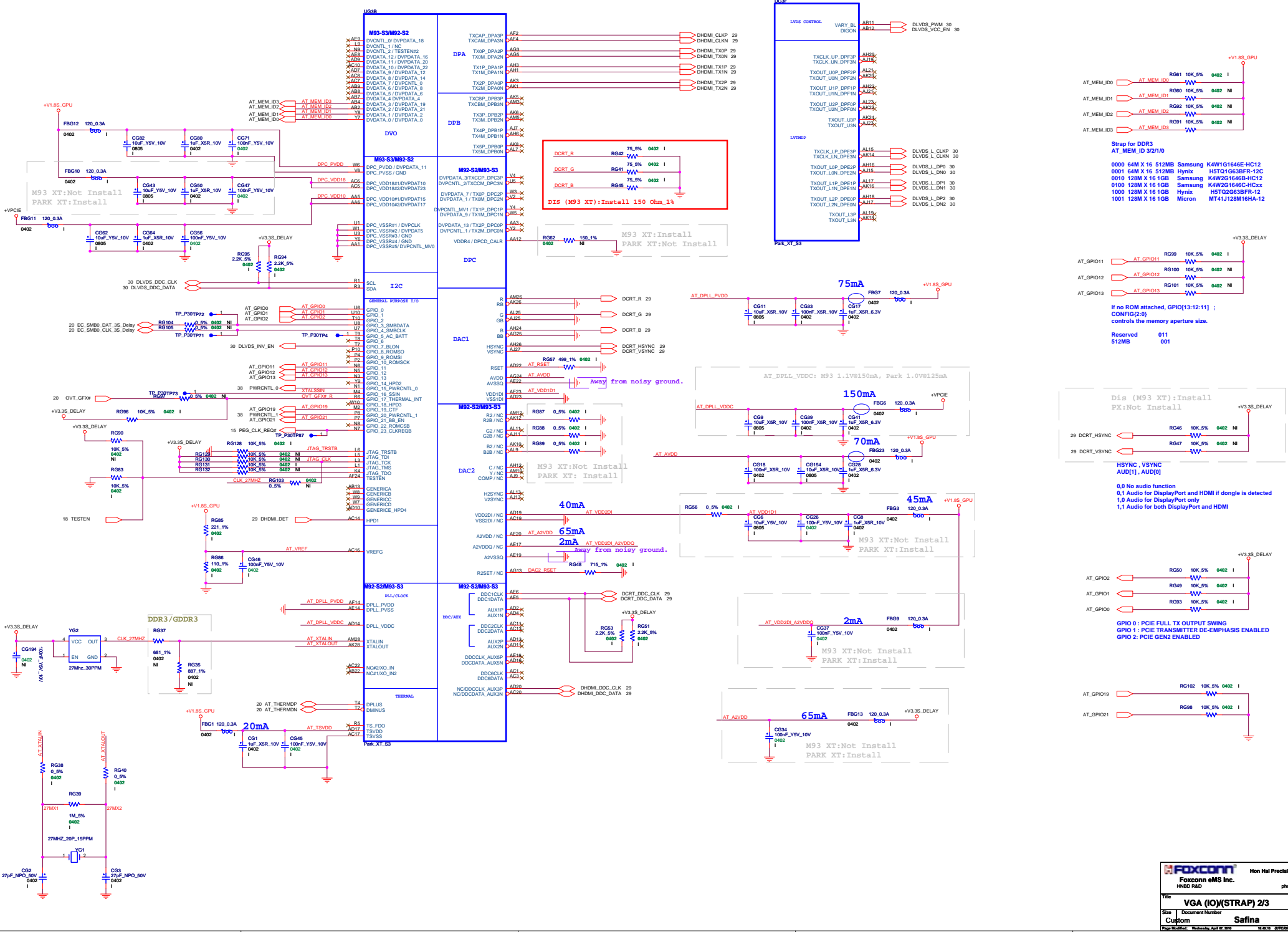


	M93_XT	Park_XT
RG109	100_1% (R1010P90-011-0)	40.2_1% (R1010280-011-0)
RG111	100.1% (R1010P90-011-0)	40.2_1% (R1010280-011-0)

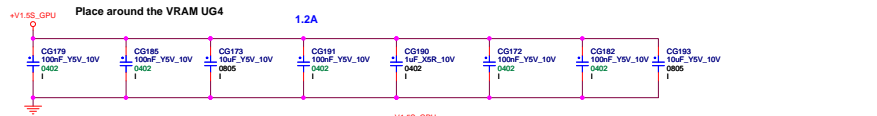
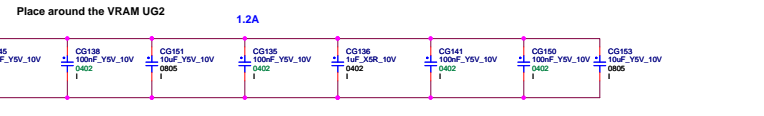
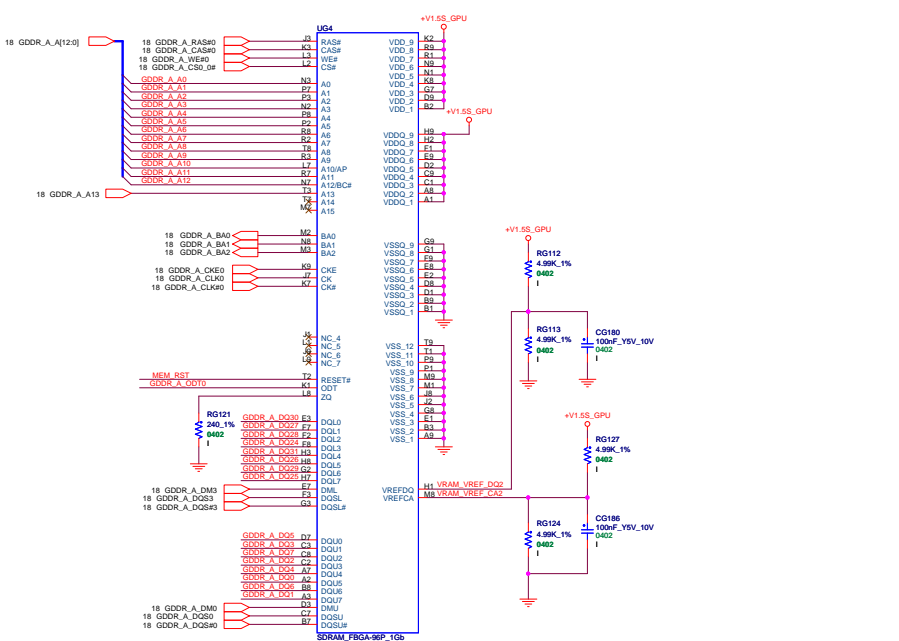
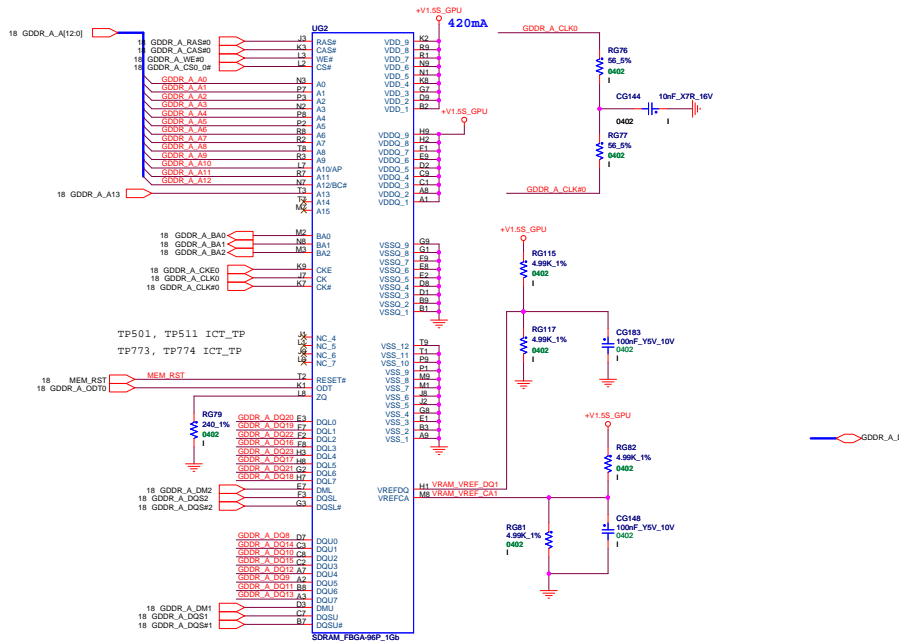


	M93_XT	PARK_XT
RG72	DNI	10K
RG73	OR	51R
RG74	2.2K	DNI
CG142	2.2nF	68pF

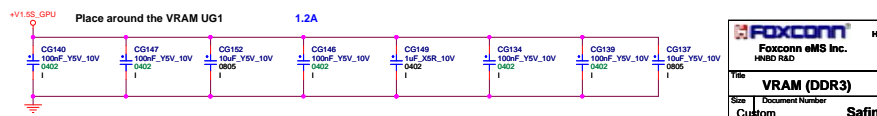
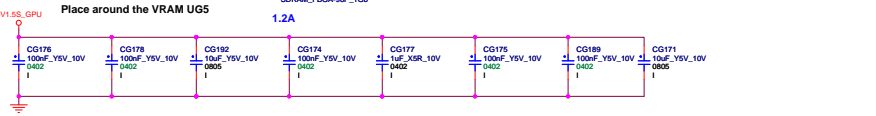
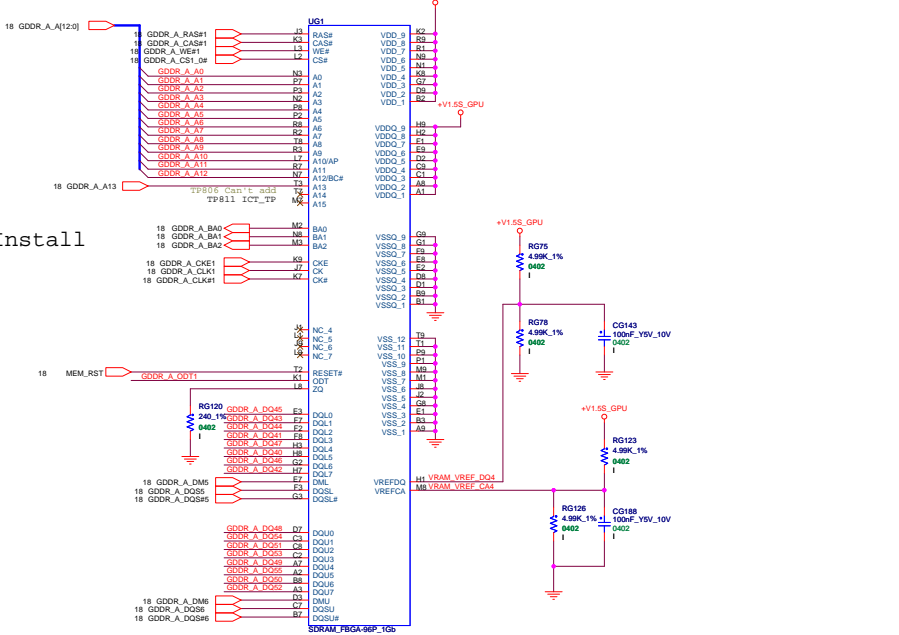
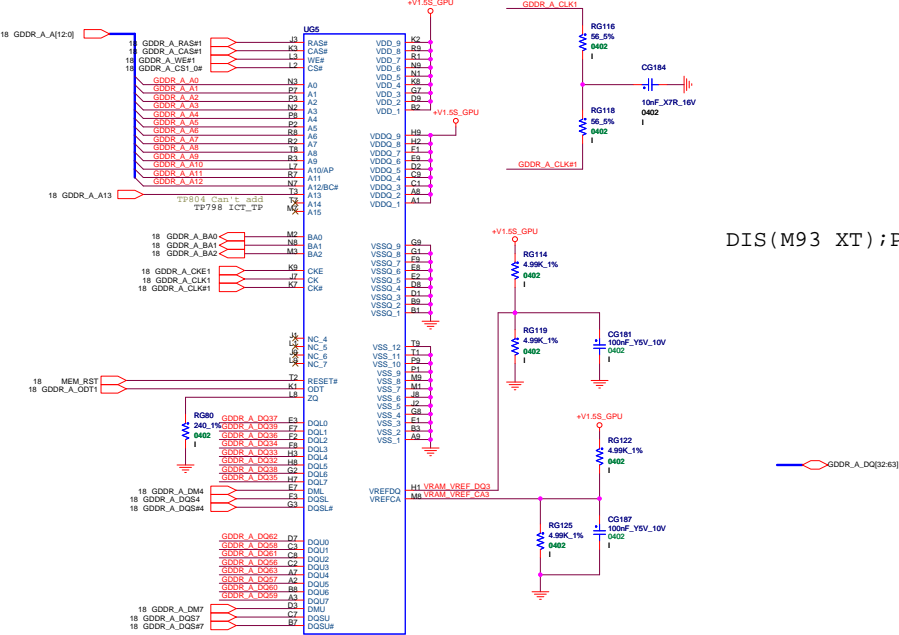


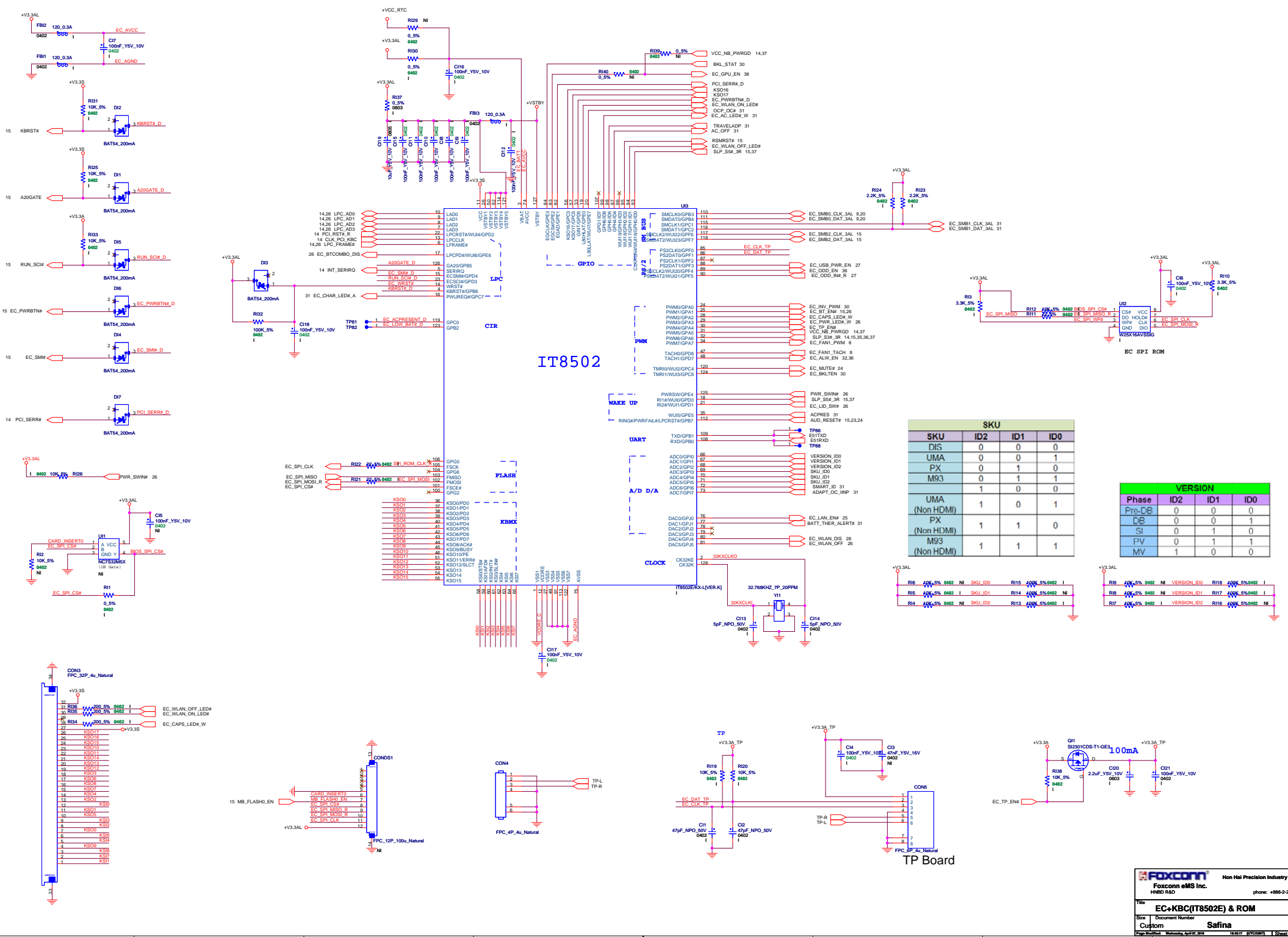






DIS(M93 XT);PX : Install

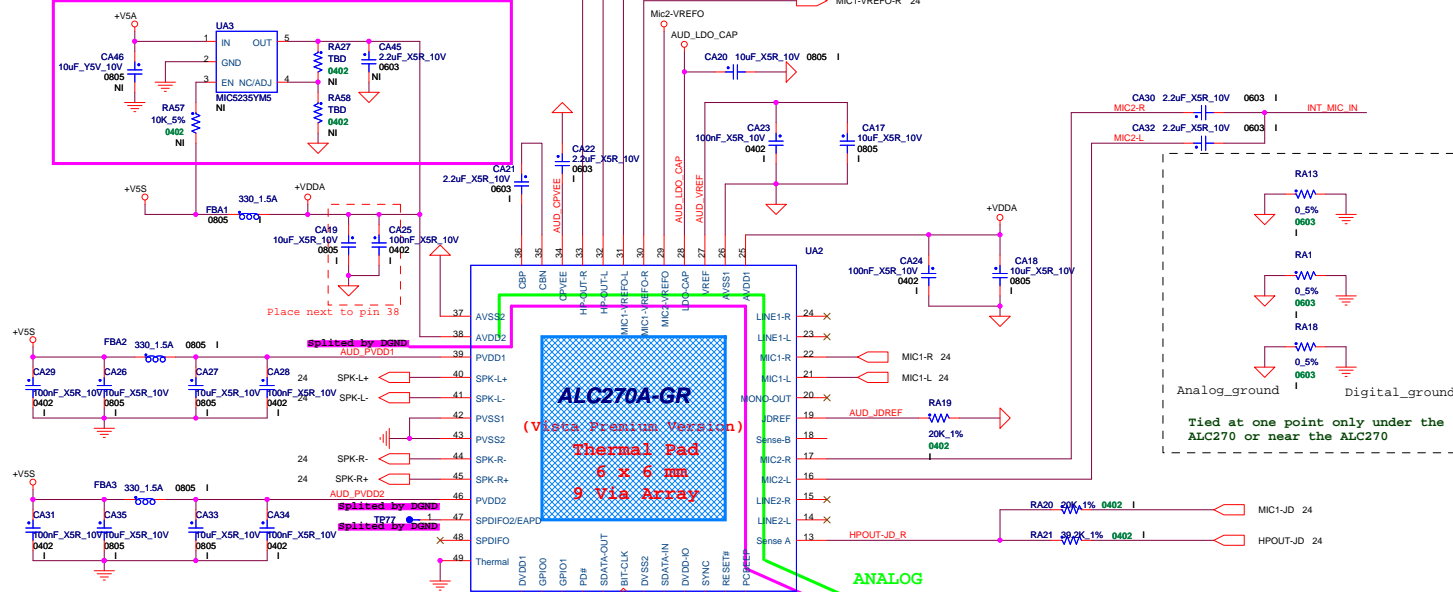




SKU			
SKU	ID2	ID1	ID0
DIS	0	0	0
UMA	0	0	1
PX	0	1	0
M93	0	1	1
UMA (Non HDMI)	1	0	1
PX (Non HDMI)	1	1	0
M93 (Non HDMI)	1	1	1

VERSION			
Phase	ID2	ID1	ID0
Pre-DB	0	0	0
DB	0	0	1
SI	0	1	0
PV	0	1	1
MV	1	0	0

Reserved LDO circuitry for +VDDA power source



Place next to pin 38

Splitted by GND

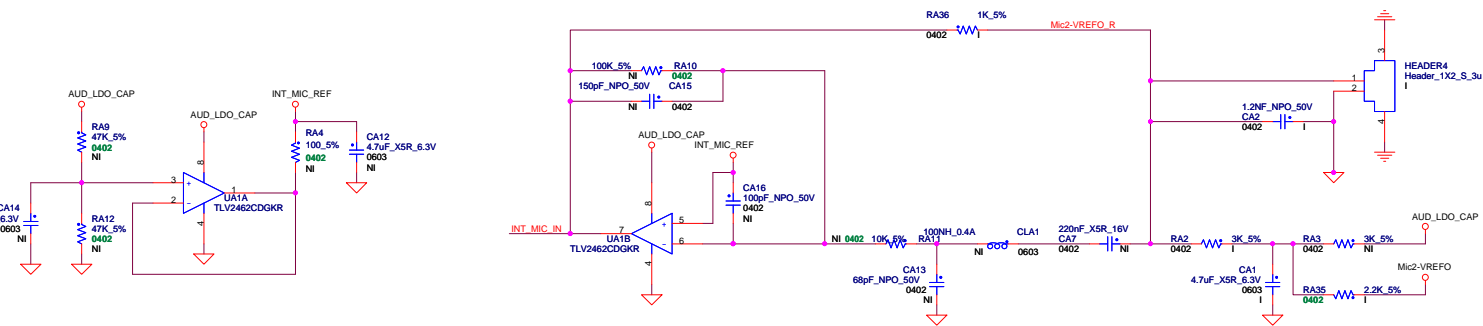
Splitted by GND

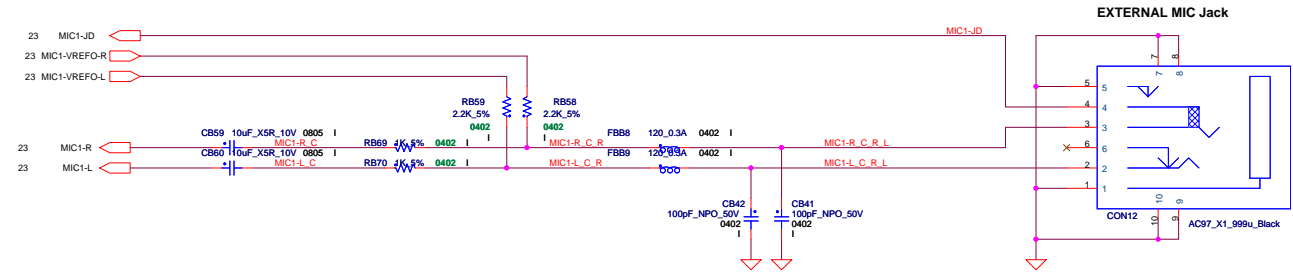
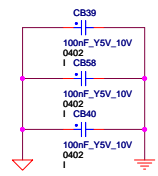
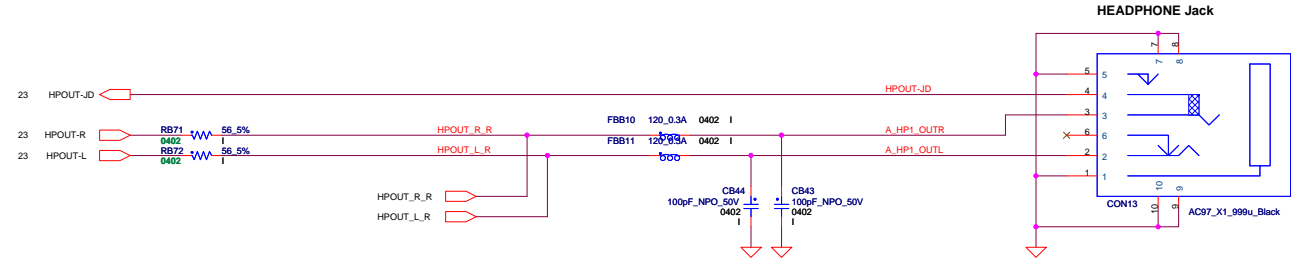
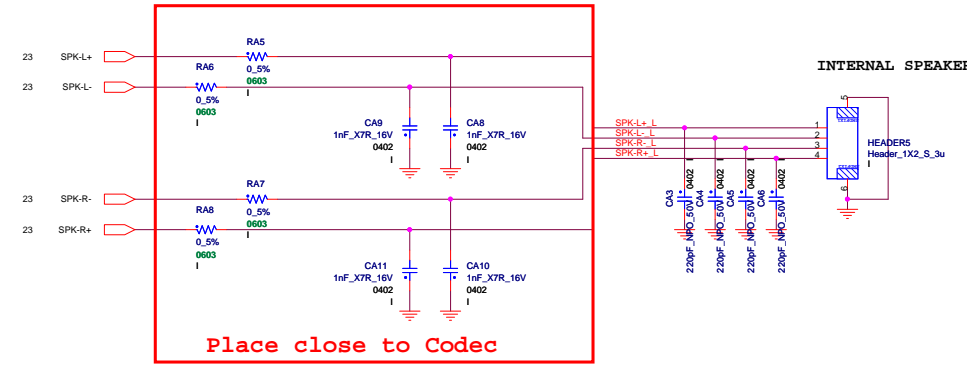
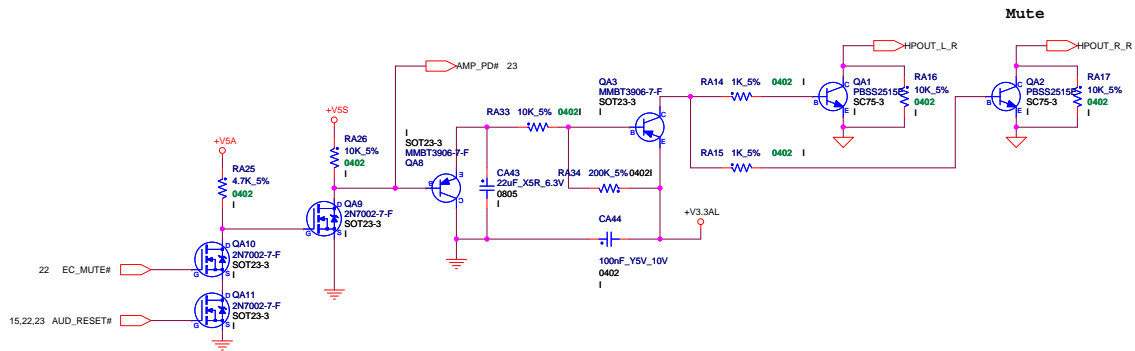
Splitted by GND

<<Attention>>  
Surges of PVDD >7V duration 0.1ms when class D amplifier is working may damage the amplifier, 10uF tantalum capacitors are required at PVDD1 and PVDD2 to suppress the surge.

PD# = 0V : Power down Class D SPK amplifier  
PD# = 3.3V : Power up Class D SPK amplifier

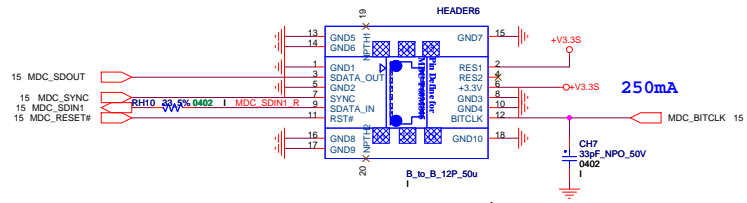
<<Attention>>  
For power\_on/off de-pop circuit and system booting warning signal: Please System BIOS Engineer Note :  
1. If you want the system make warning signal after power on , please let EC\_MUTE# High first.  
2. When you want to exit your Bios Programming Code, please let the EC\_MUTE# Low. (The programming is different from before .)



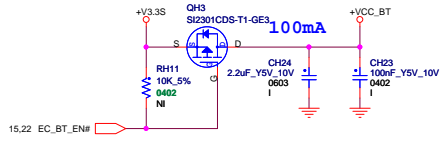
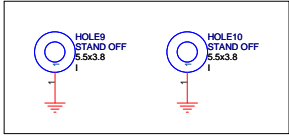




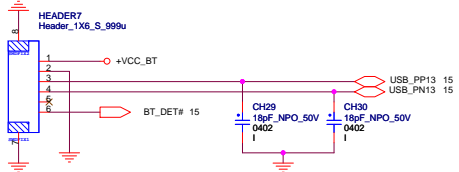




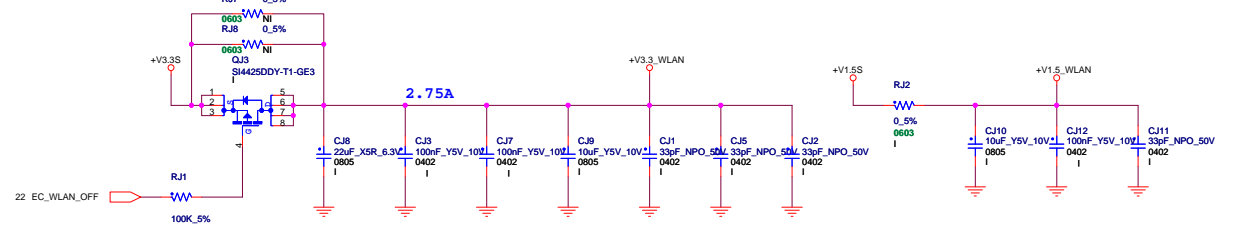
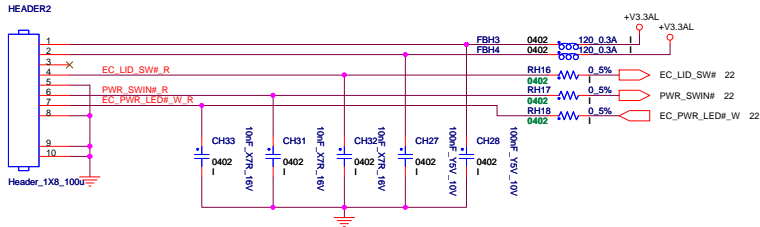
MDC CONN. Option



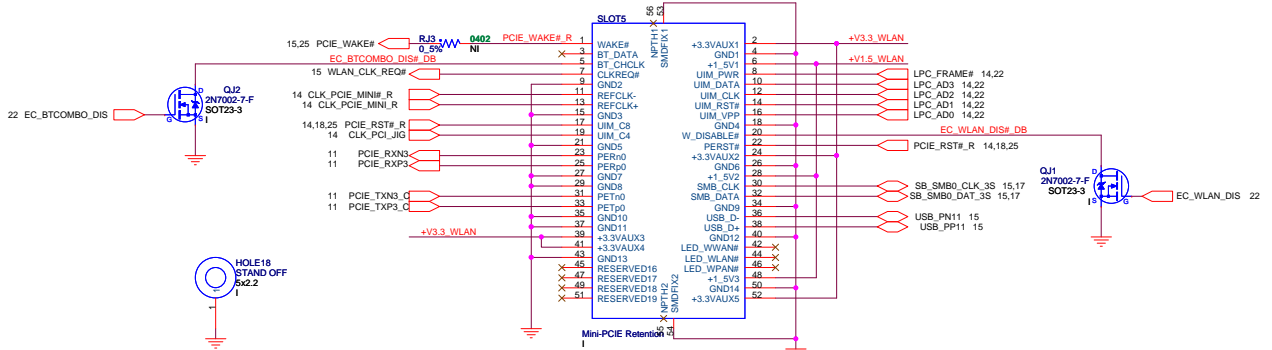
Bluetooth CONN.



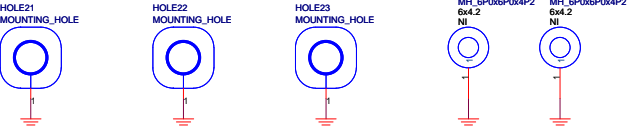
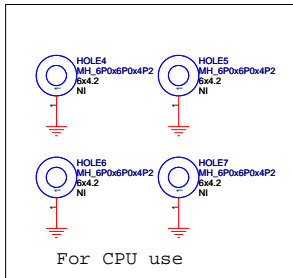
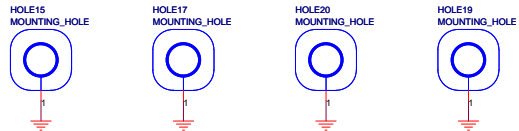
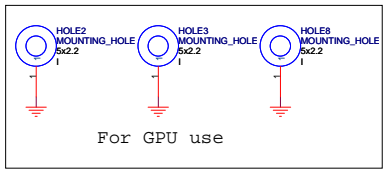
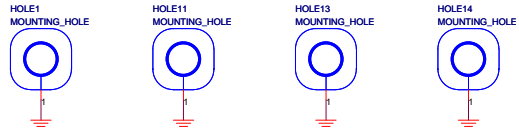
PWR Board CONN.



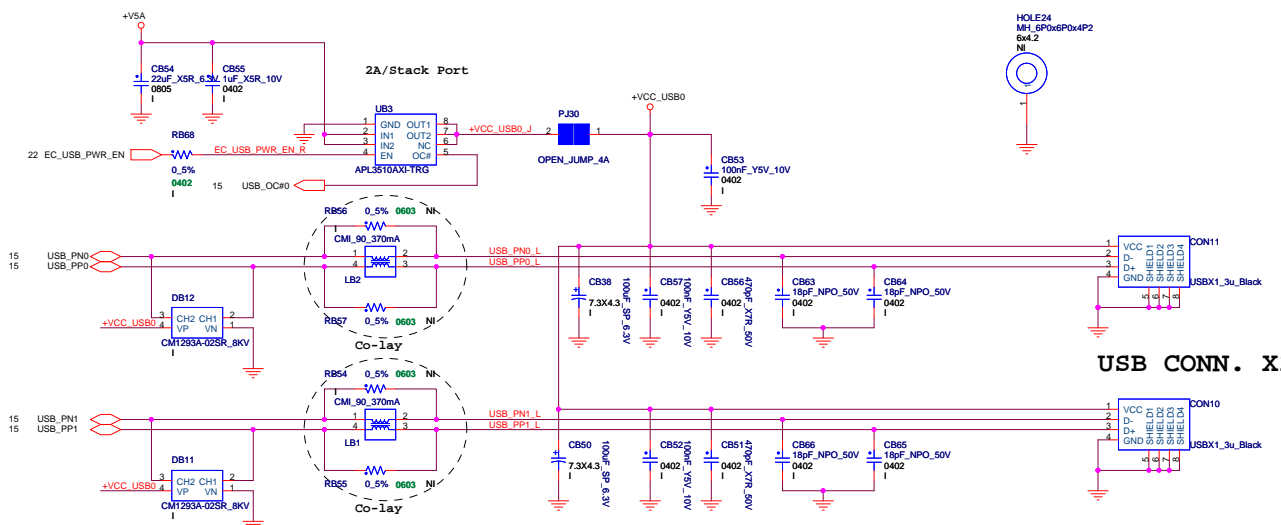
+1.5V=>0.5A Peak/0.375A Normal  
+3.3Vaux=>2.75A Peak/1.1A Normal



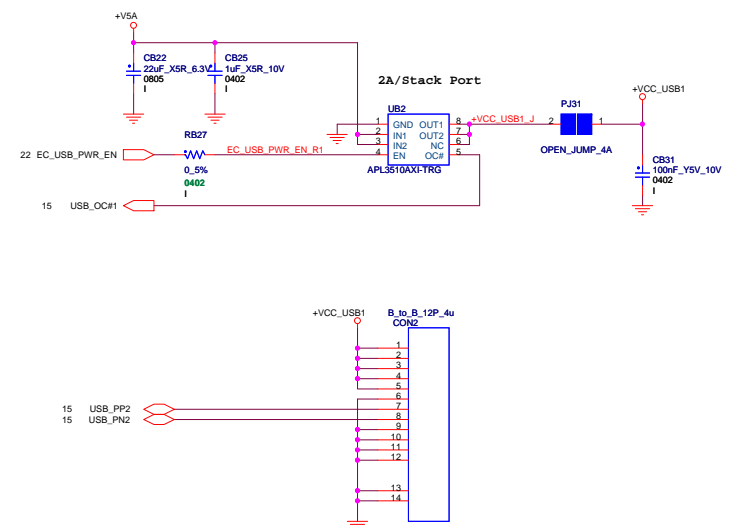
Half Mini Card for WLAN



Mounting HOLE

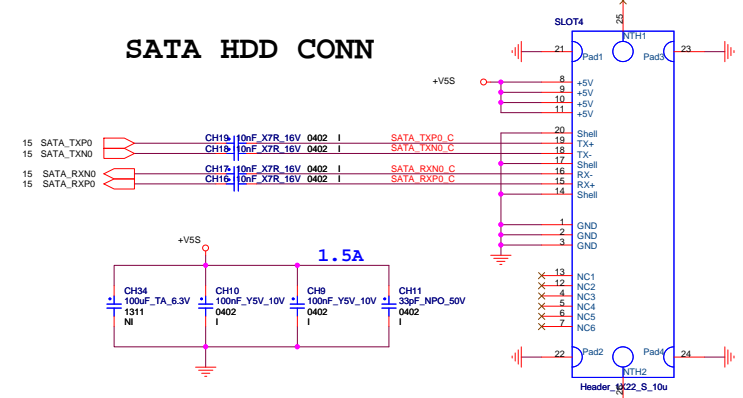


USB CONN. X2

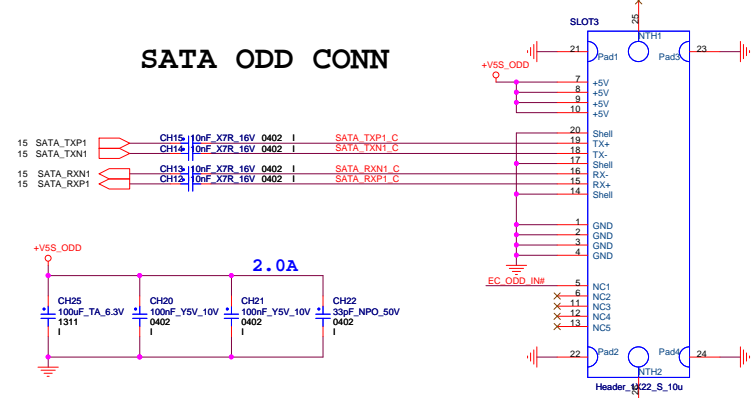


USB Board CONN.

SATA HDD CONN

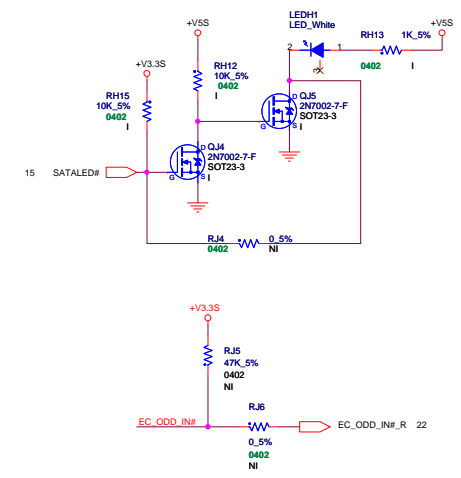


SATA ODD CONN



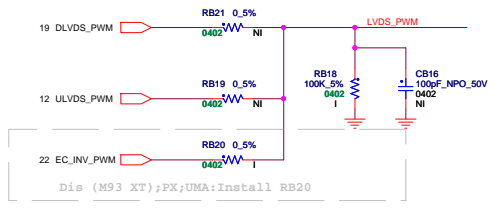
Power pin current  
max. 1300 mA (less 2ms)

HDD/ODD Status LED

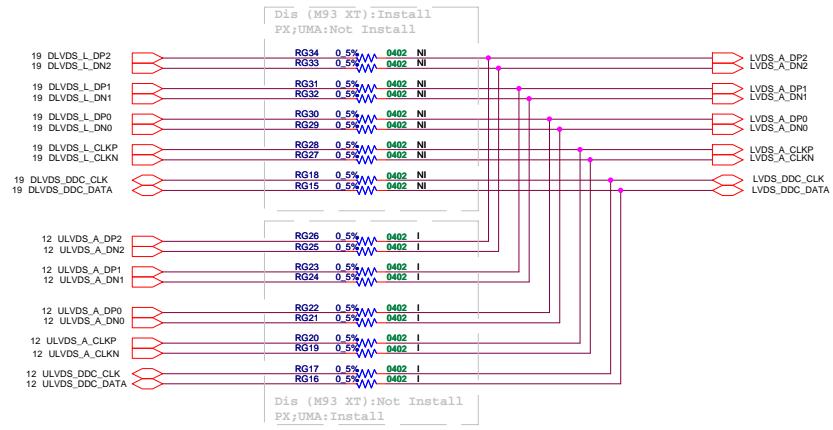




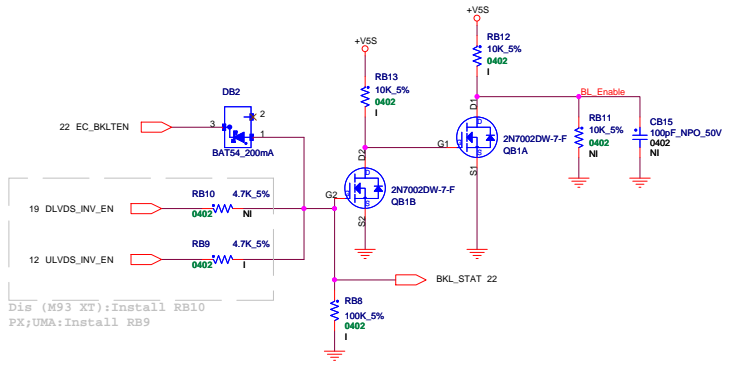




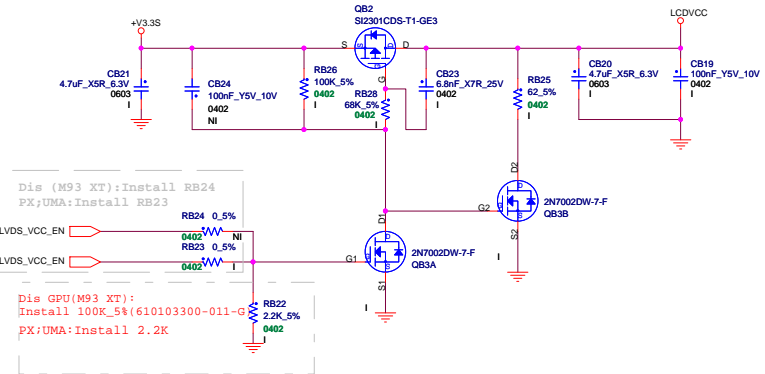
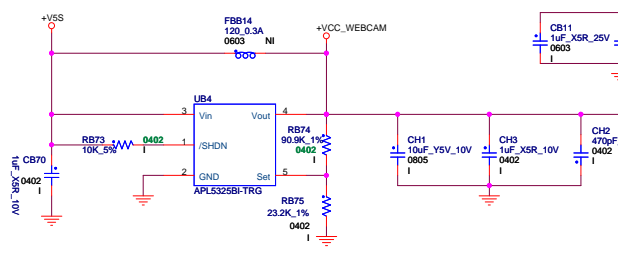
Dis (M93 XT):PX;UMA:Install RB20



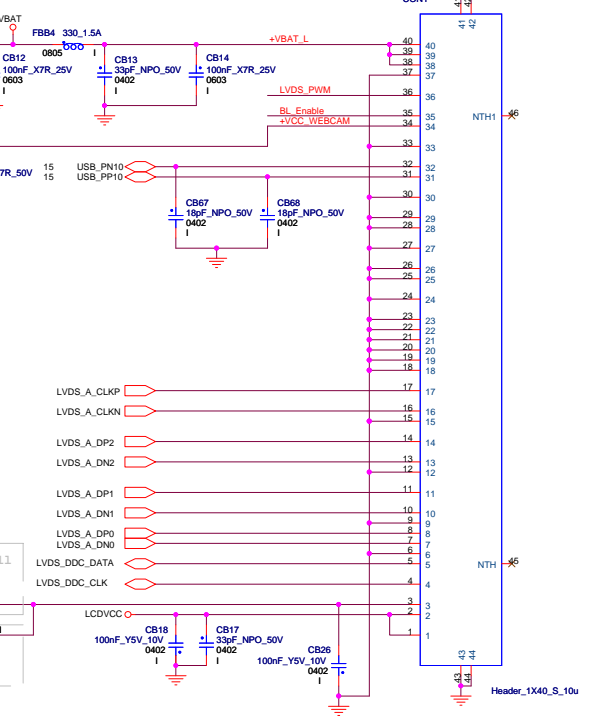
Dis (M93 XT):Not Install  
PX;UMA:Install



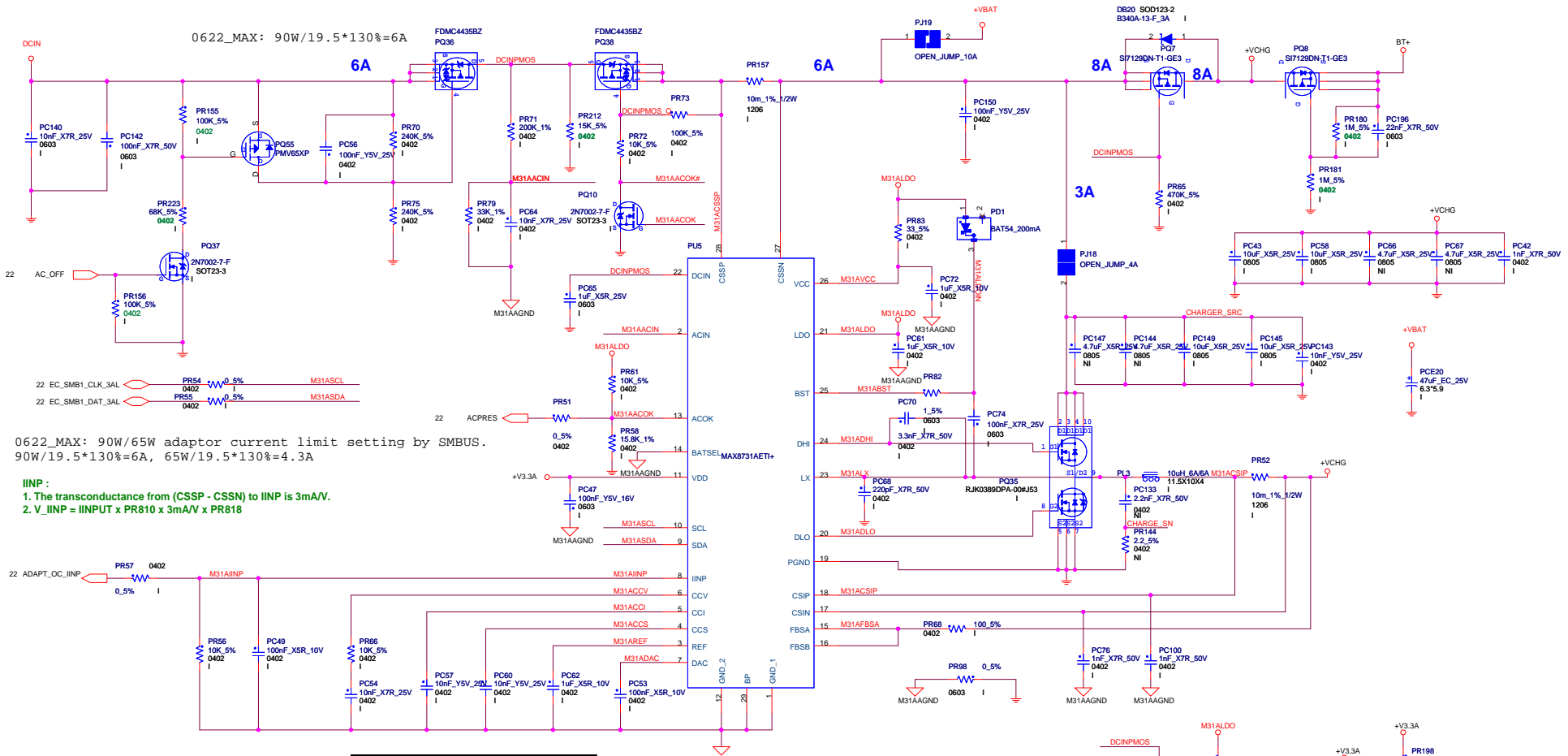
Dis (M93 XT):Install RB10  
PX;UMA:Install RB9



Dis GPU(M93 XT):  
Install 100K\_5%(610103300-011-G)  
PX;UMA:Install 2.2K



M93 XT:Not Install  
PX;UMA:Install  
M93 XT:Install  
PX;UMA:Not Install

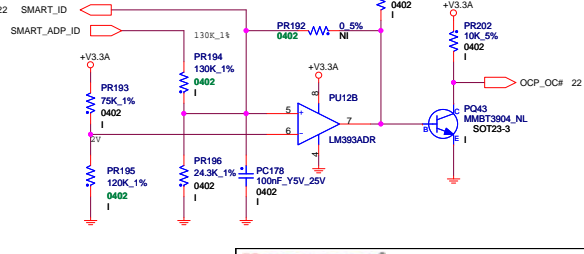
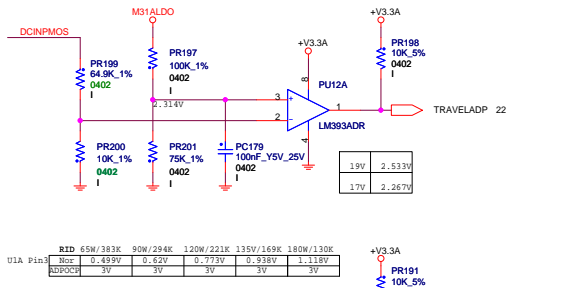
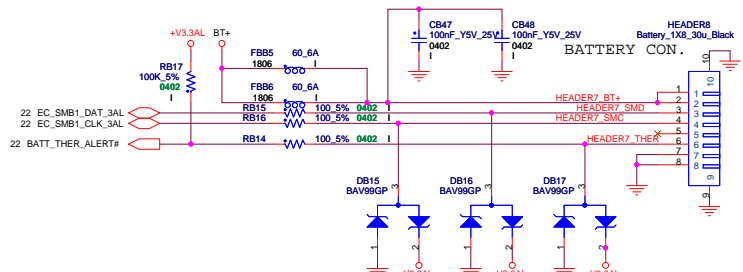
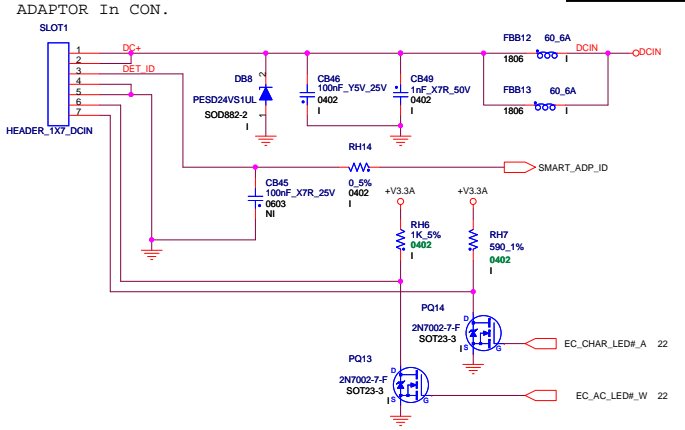


0622\_MAX: 90W/65W adaptor current limit setting by SMBUS.  
 $90W/19.5 \times 130\% = 6A$ ,  $65W/19.5 \times 130\% = 4.3A$

- IINP :**
- The transconductance from (CSSP - CSSN) to IINP is 3mA/V.
  - $V_{IINP} = IINP \times PR810 \times 3mA/V \times PR818$

Pin No	Pin Define	AWG	Color
1	DC+	22	Red
2	DC+	22	Red
3	Detect (ID)	28	White
4	DC-	22	Black
5	DC-	22	Black
6	LED-	28	Black
7	LED+	28	yellow

Pin No.	Symbol	Comments
1	BATT+	Batt+, Battery Positive Terminal.
2	BATT+	Batt+, Battery Positive Terminal.
3	SMD	SMBus data interface I/O pin..
4	SMC	SMBus clock interface I/O pin
5	ID	Open
6	B/I	Connect to thermistor (103AT2 equivalent)
7	GND	Batt-, Battery Negative Terminal
8	GND	Batt-, Battery Negative Terminal



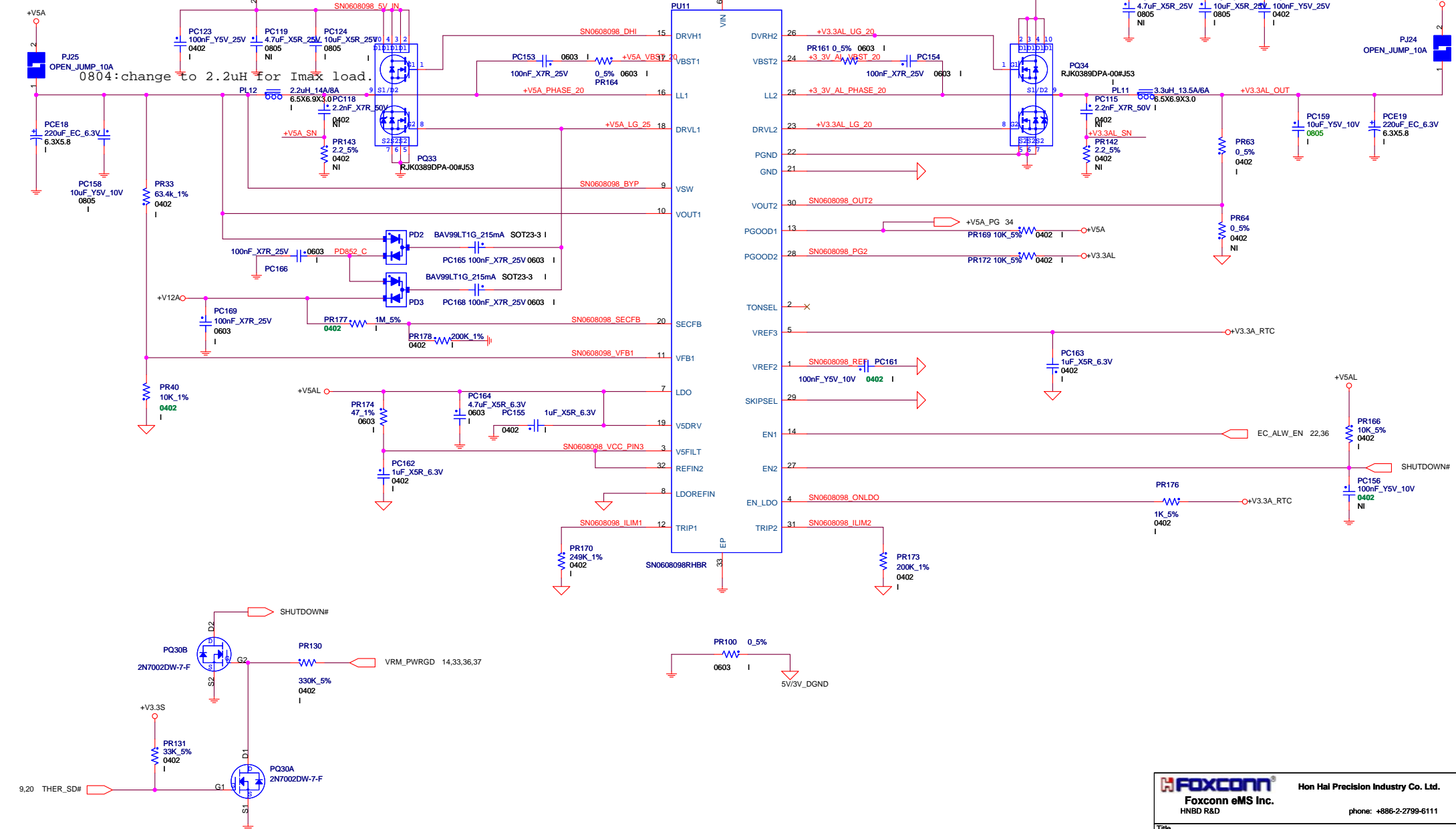
**FOXCONN** Hon Hai Precision Industry Co. Ltd.  
 Foxconn eMS Inc.  
 HNBD RAD phone: +886-2-2799-6111

Title: **PWR\_Charger MAX8731AETI**

Size: Document Number  
 Custom Safina Rvw  
 Page Modified: Wednesday, April 07, 2010 16:16:16 (UTC+8) Sheet 31 of 39

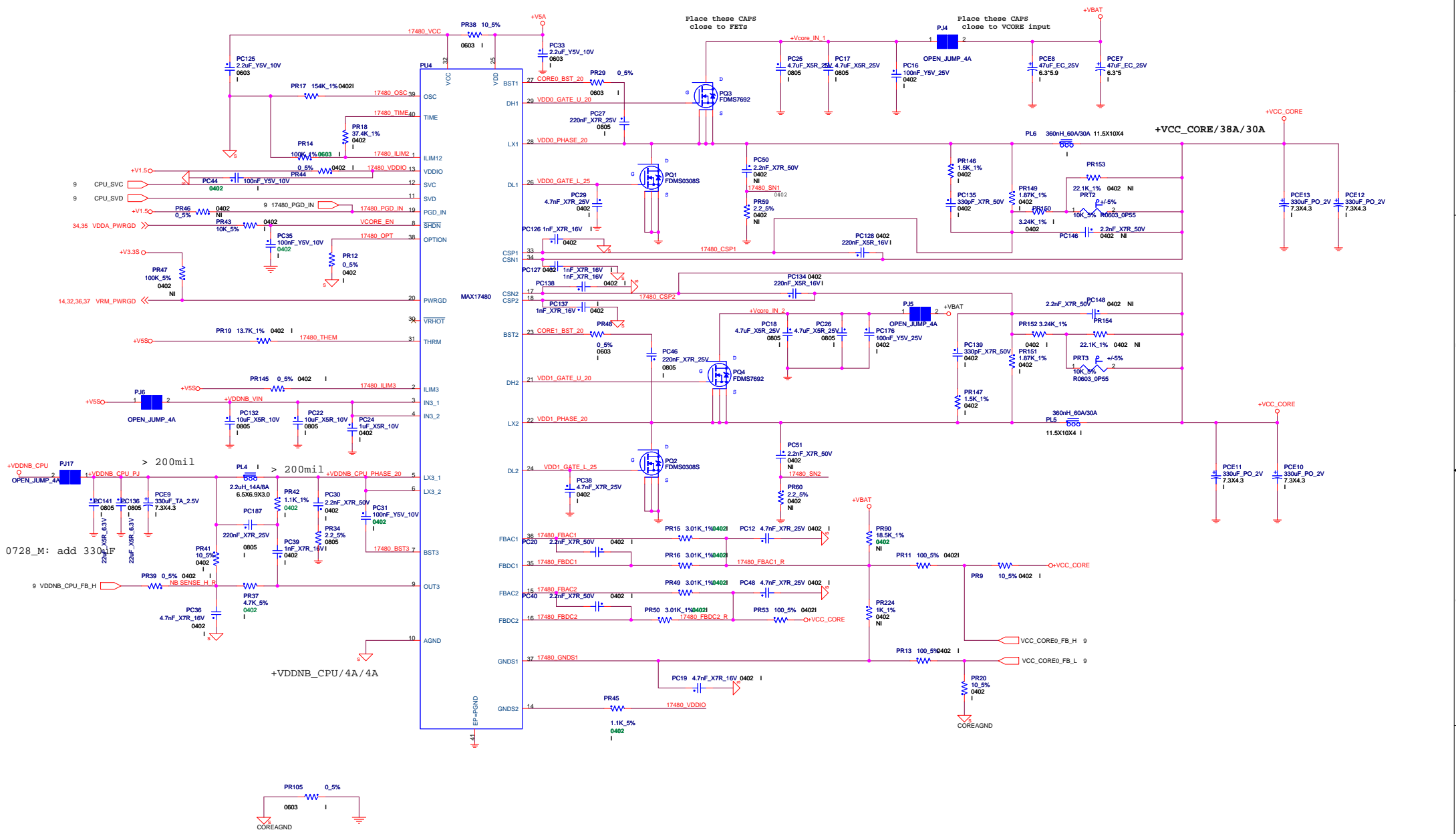
+V5A/7A/5.6A

+V3.3A/6/4.8A



		Hon Hai Precision Industry Co. Ltd.	
Foxconn eMS Inc.		HNBDR&D	
		phone: +886-2-2799-6111	
Title: <b>5V/3.3V SN0608098RHBT</b>			
Size	Document Number	Rev	MV
Custom	Safina		
Page Modified: Wednesday, April 07, 2010		18:49:16 (UTC+08:00) Sheet 32 of 39	

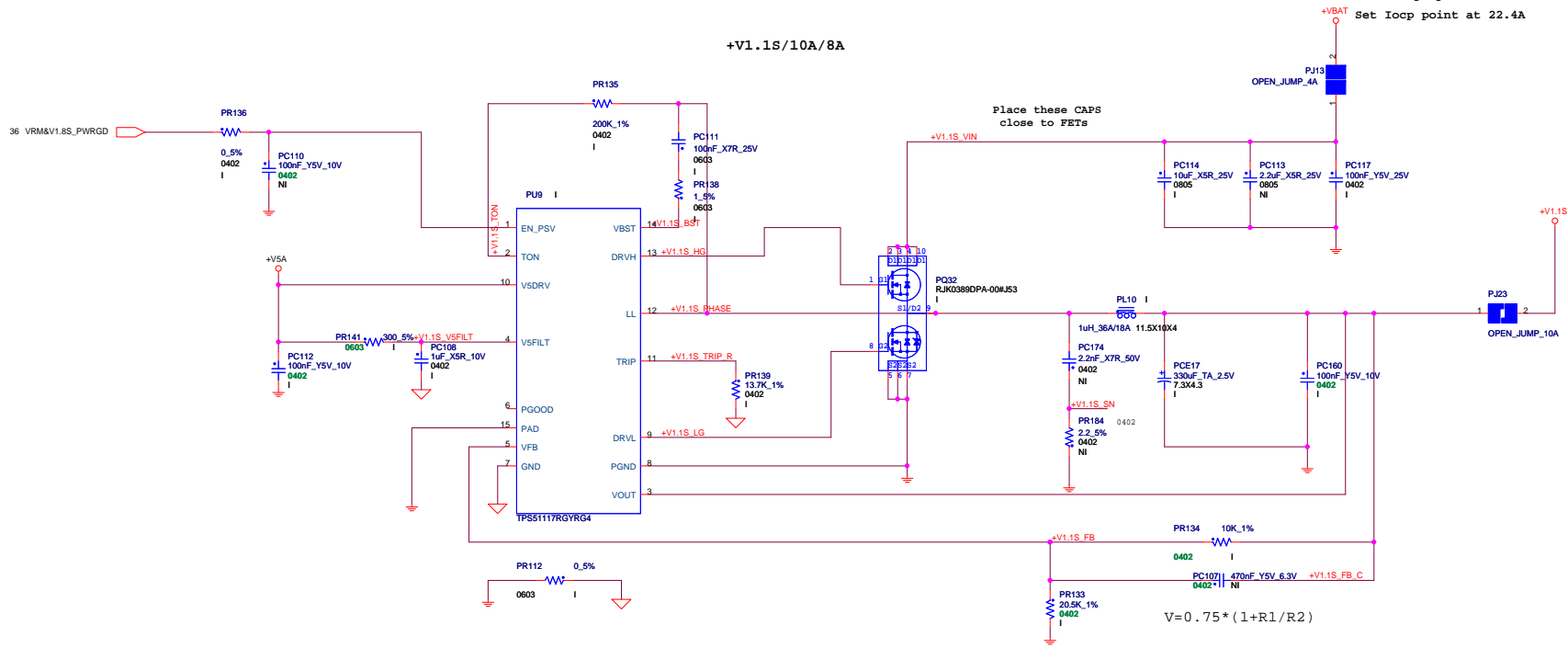




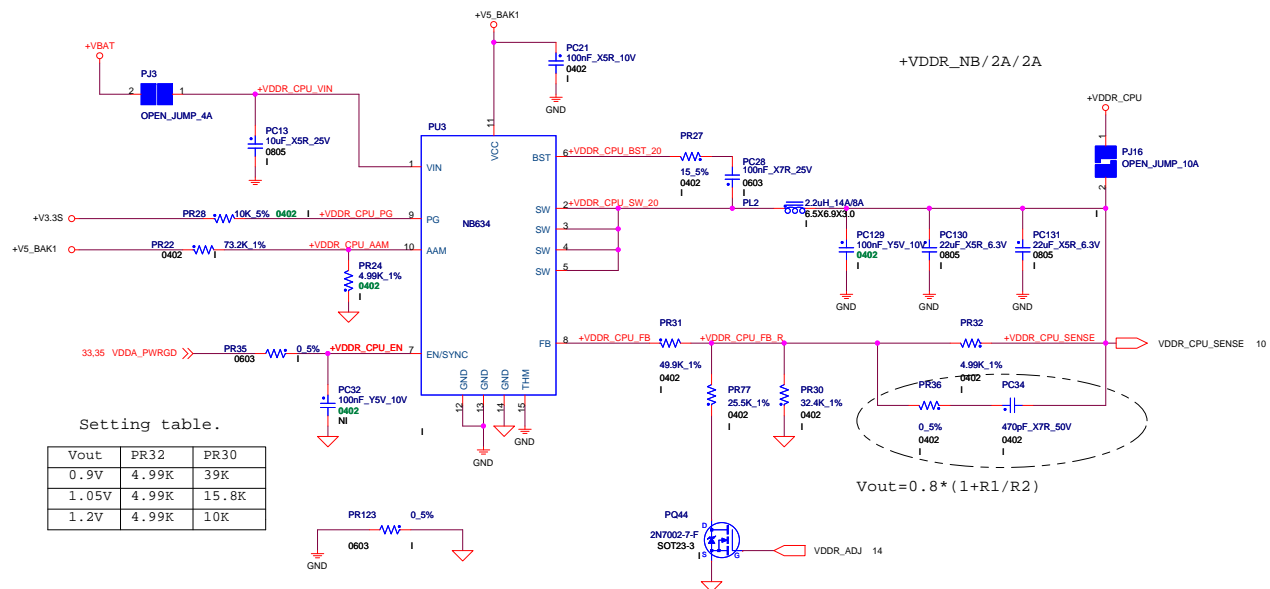
0728\_M: add 330uF

Frequency is 300K HZ  
 auto-skip operation mode  
 Set Iocp point at 22.4A

+V1.1S/10A/8A



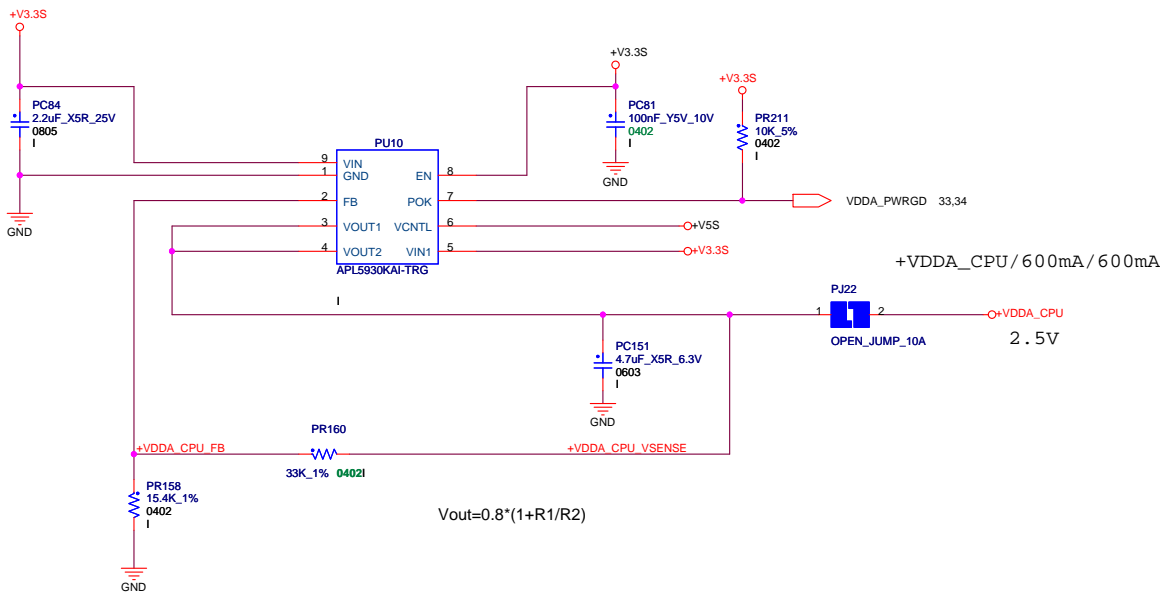
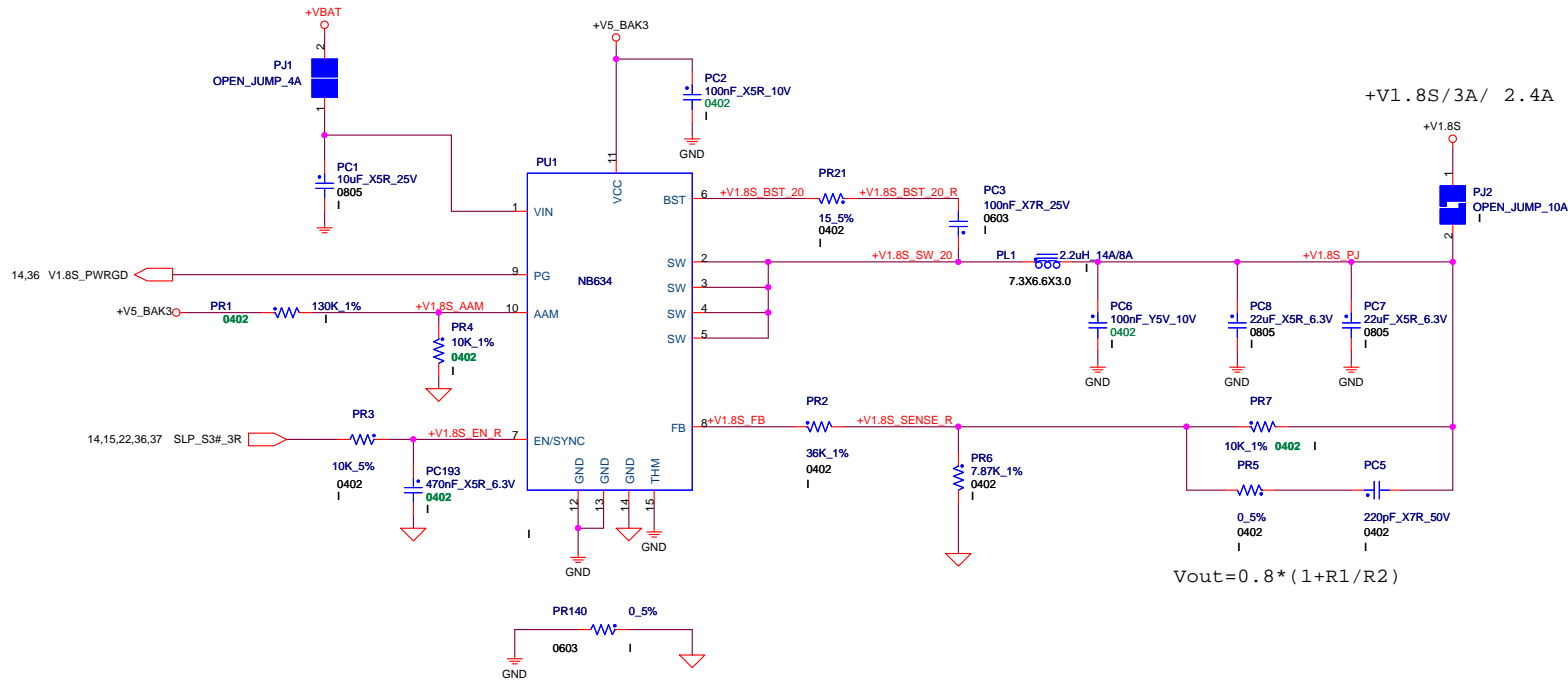
$$V = 0.75 * (1 + R1/R2)$$

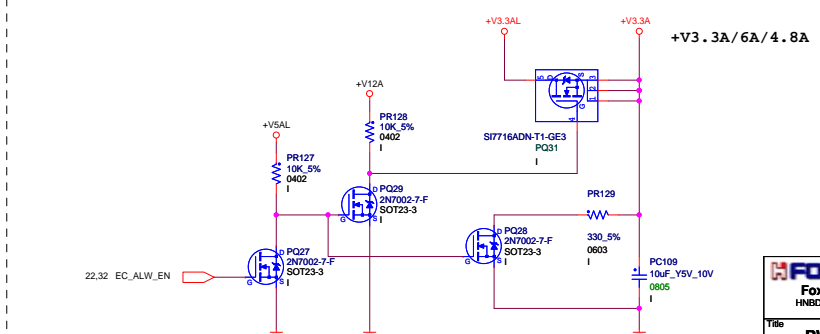
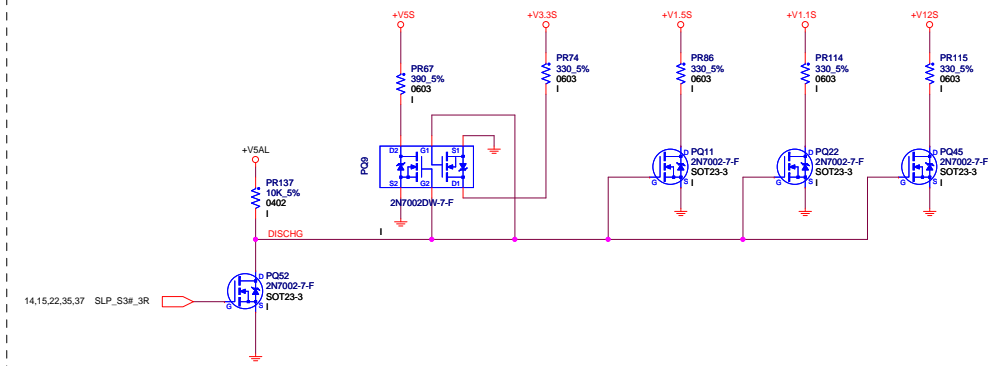
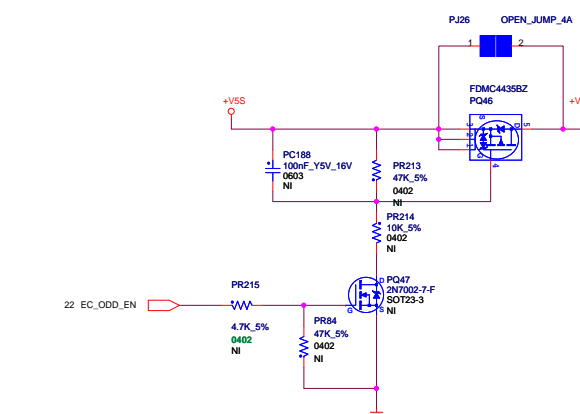
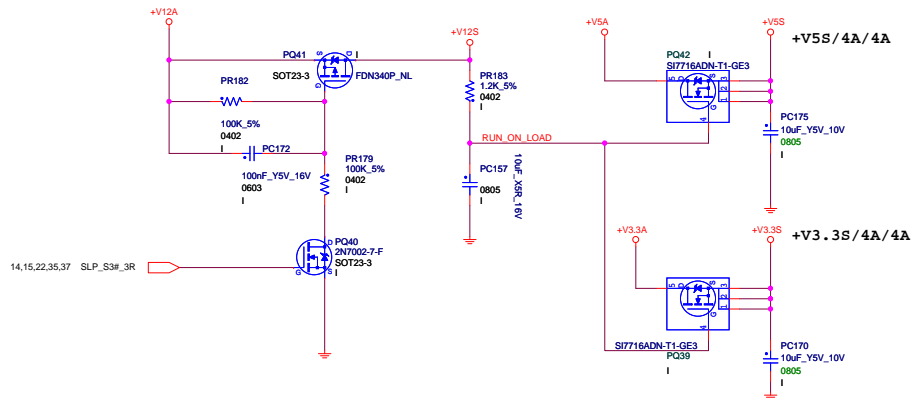
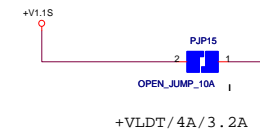
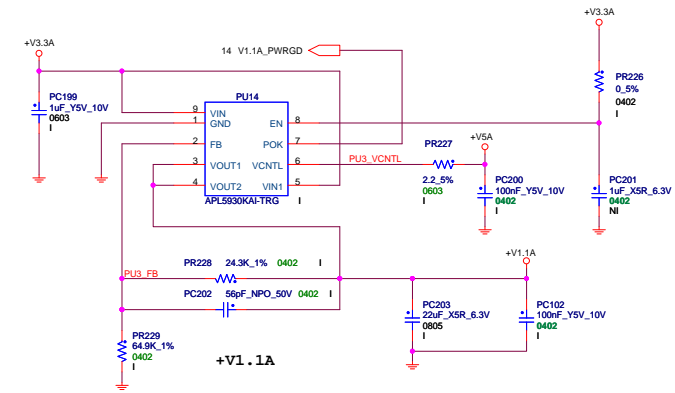
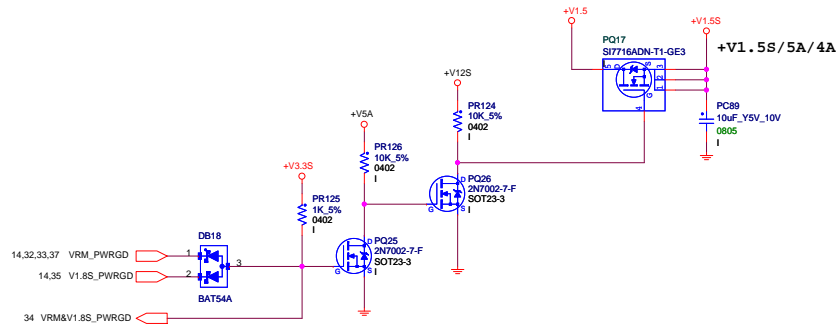


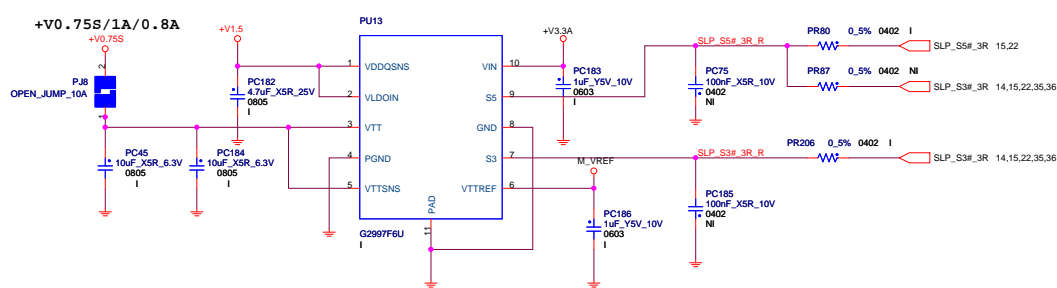
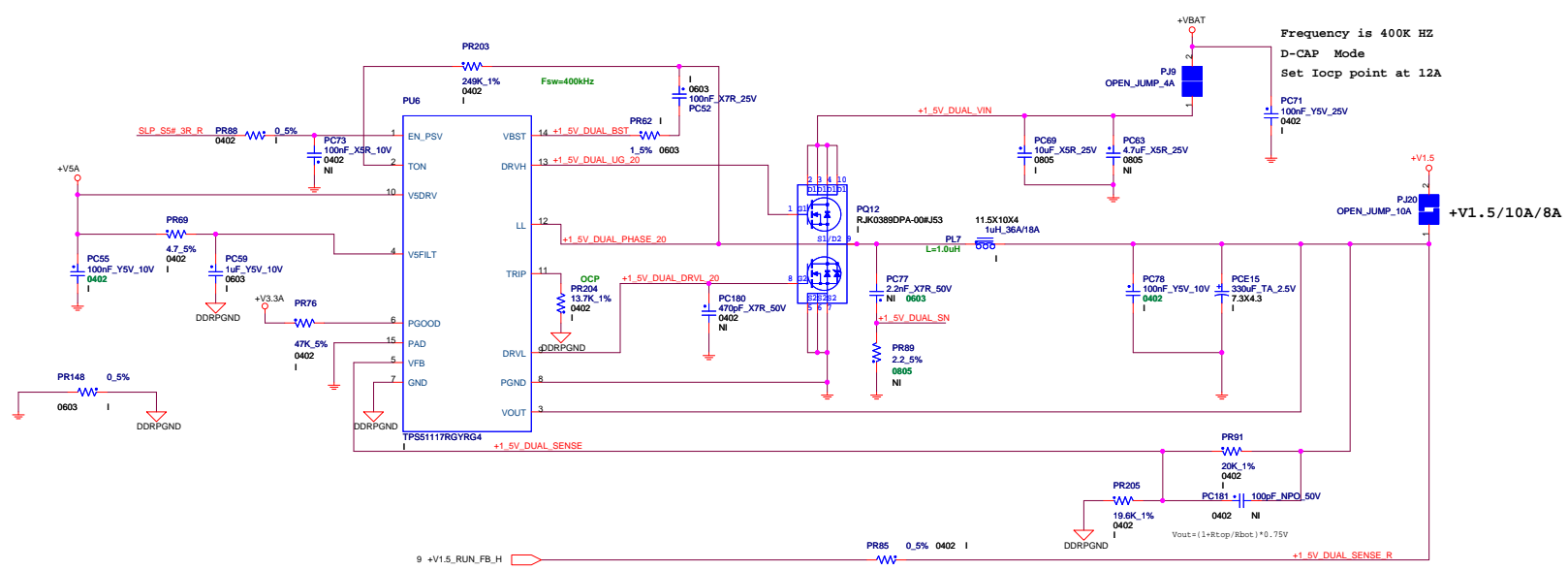
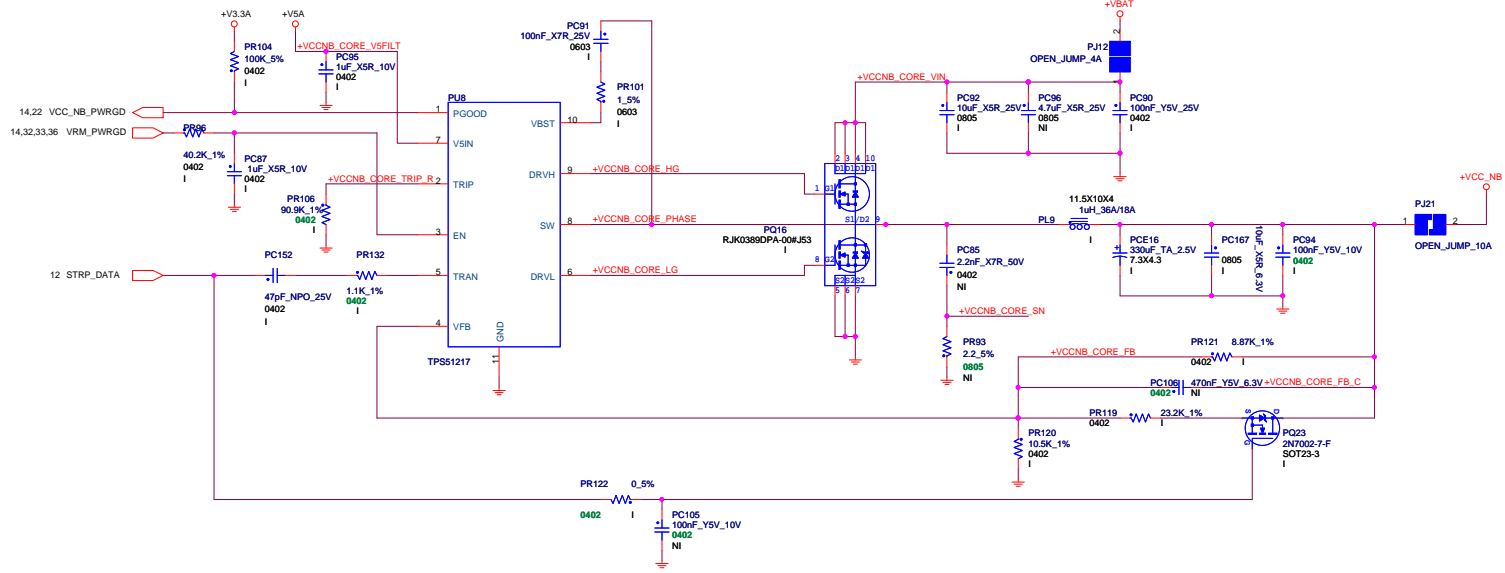
$$V_{out} = 0.8 * (1 + R1/R2)$$

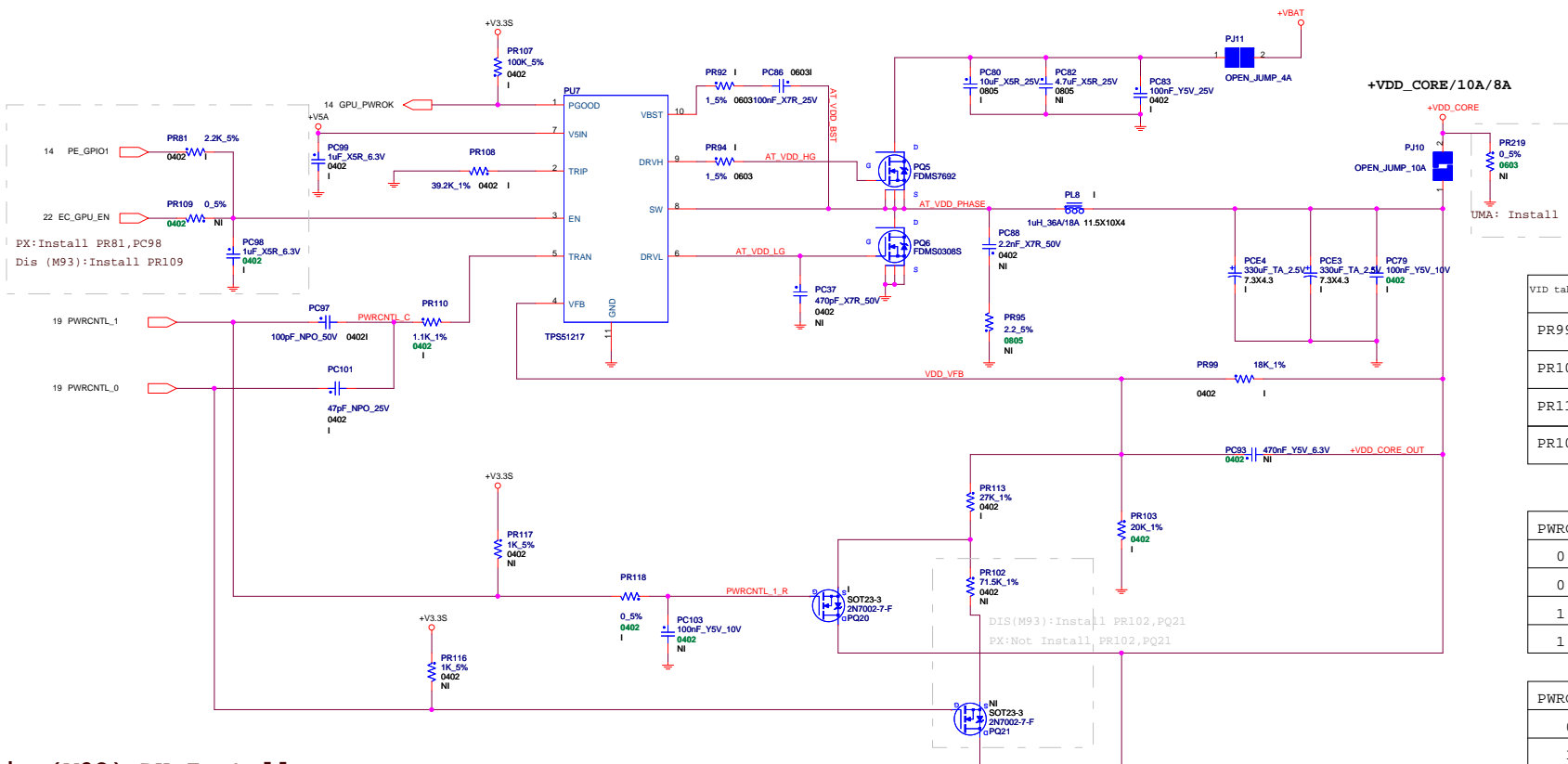
Setting table.

Vout	PR32	PR30
0.9V	4.99K	39K
1.05V	4.99K	15.8K
1.2V	4.99K	10K









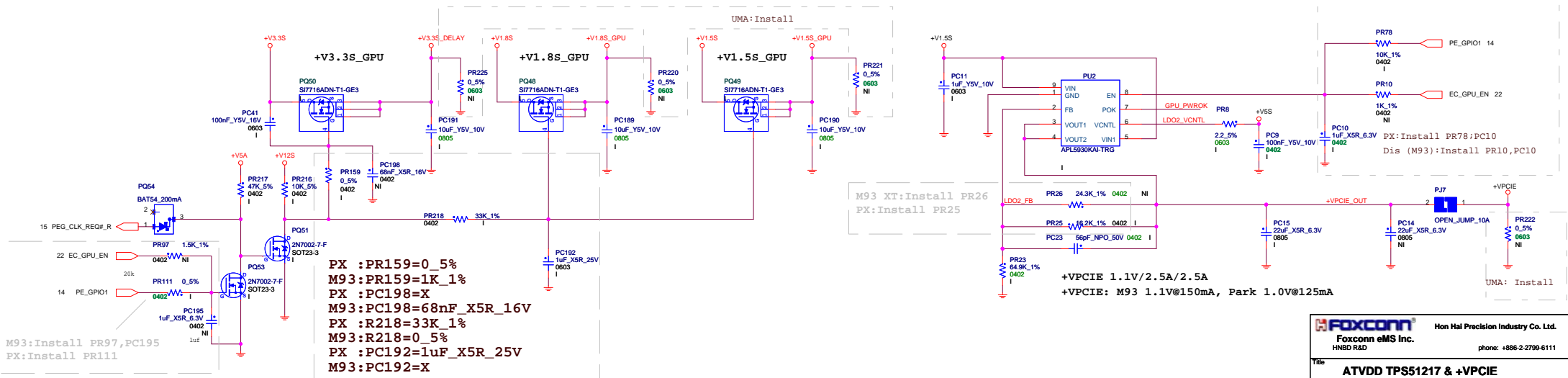
VID table	M93_XT_S3	Park_XT_S3
PR99	20.5K_1% (61011JW00-012-G)	18K_1% (610115W00-012-G)
PR103	20K_1% (610114H00-011-G)	20K_1% (610114H00-011-G)
PR113	28.7K_1% (61011B400-012-G)	27K_1% (610117200-012-G)
PR102	71.5K_1% (611008700-011-G)	N/A

PWRCNTL_1	PWRCNTL_0	M93_XT_S3
0	0	1.2V
0	1	1.1V
1	0	0.95V
1	1	0.9V

PWRCNTL_1	Park_XT_S3
0	1.12V
1	0.9V

Dis (M93);PX:Install  
UMA:Not Install

$$V = 0.6 * (1 + R1/R2)$$

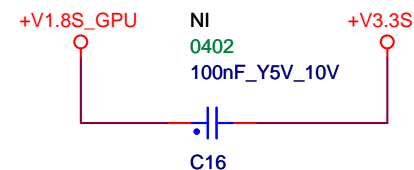
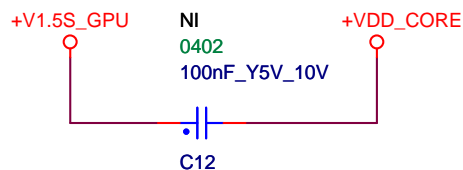
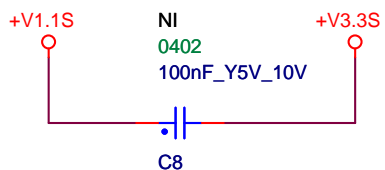
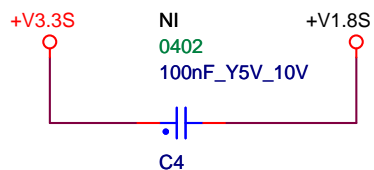
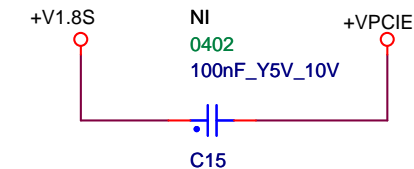
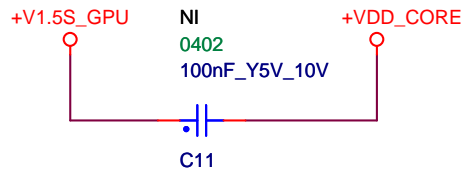
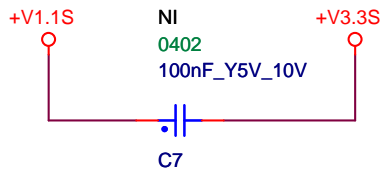
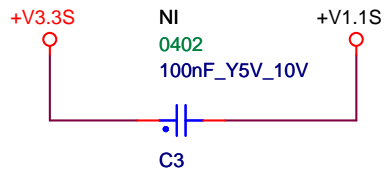
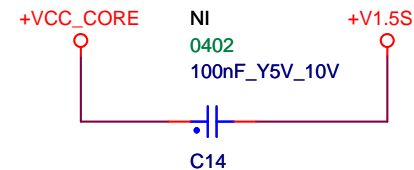
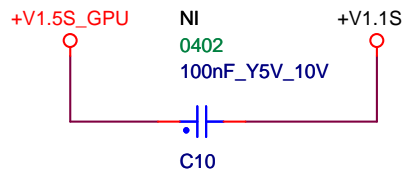
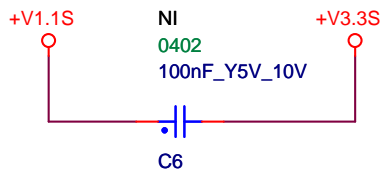
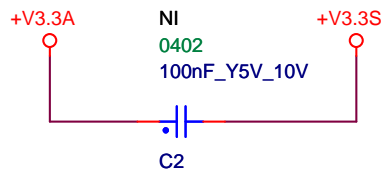
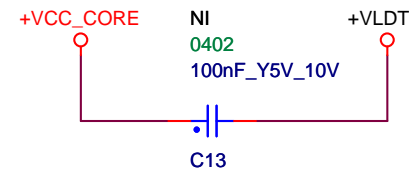
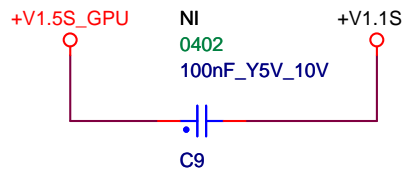
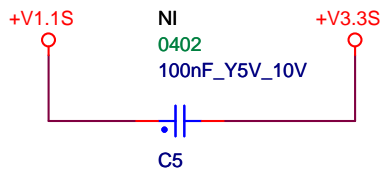
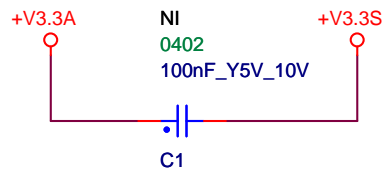


PX : PR159=0.5%  
M93: PR159=1K\_1%  
PX : PC198=X  
M93: PC198=68nF\_X5R\_16V  
PX : R218=33K\_1%  
M93: R218=0.5%  
PX : PC192=1uF\_X5R\_25V  
M93: PC192=X

M93 XT: Install PR26  
PX: Install PR25

+VPCIE 1.1V/2.5A/2.5A  
+VPCIE: M93 1.1V@150mA, Park 1.0V@125mA

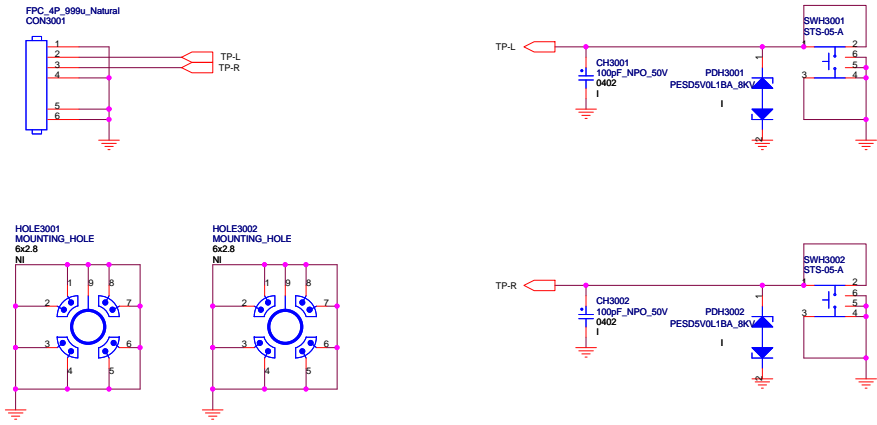
M93: Install PR97, PC195  
PX: Install PR111



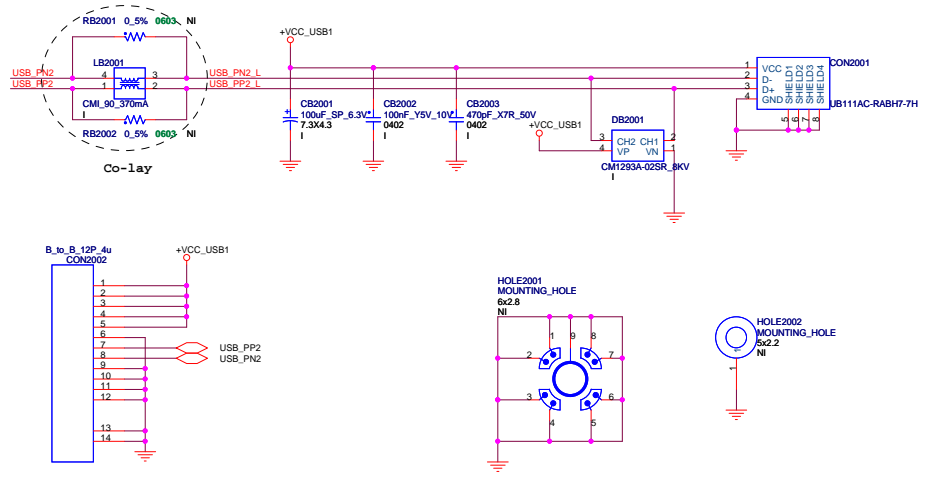
Only for 6 layer M/B use

**FOXCONN**<sup>®</sup> Hon Hai Precision Industry Co. Ltd.  
 Foxconn eMS Inc.  
 HNBD R&D phone: +886-2-2799-6111

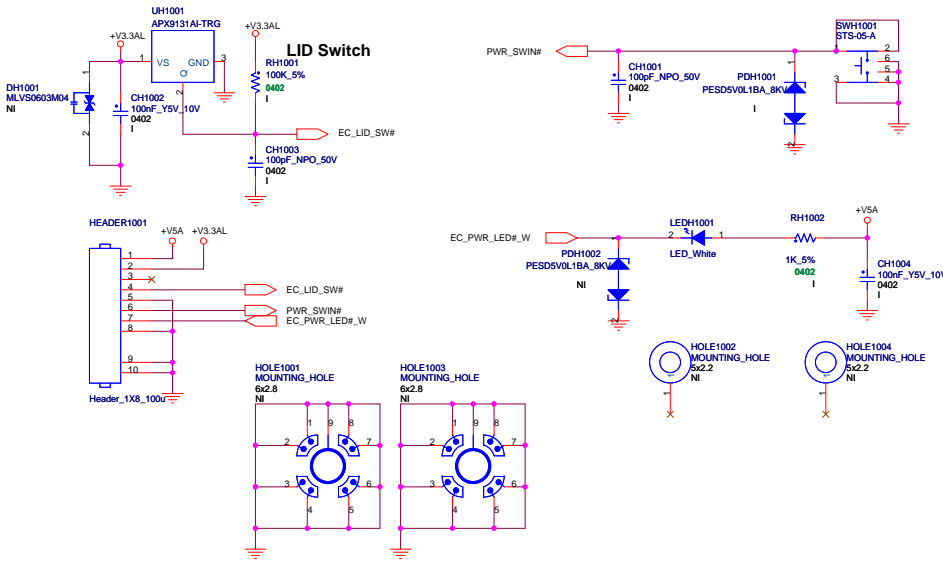
Title		
<b>SYSTEM BLOCK DIAGRAM</b>		
Size	Document Number	Rev
A	<b>Safina</b>	MV
Page Modified: Wednesday, April 07, 2010		18:49:16 (UTC/GMT) Sheet 39 of 39



SW Board



USB Board



Power Board