SiGma Micro
IC Solution Designing

SPECIFICATION

SG8UP5393

8-Bit OTP Microcontroller

Version 1.3

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1.INTRODUCTION

The SG8UP5393 is a series of Universal Serial Bus 8-bit RISC One-Time Programming (OTP) microcontrollers. It is specifically designed for USB low speed device application and to support legacy device such as PS/2 and USB Keyboard. The SG8UP5393 also support one device address and three endpoints.

The SG8UP5393 is implemented on a RISC architecture. It has 8-level stack and 8 interrupt sources. Each device has 144bytes of general purpose SRAM and 4K*14bits of OTP ROM.

2. FEATURE

- Operating voltage 4.5V~5.5V
- USB Specification Compliance
  - Universal Serial Bus Specification Version 1.0
  - USB Device Class Definition for Human Interface Device (HID).
  - Support 1 device address and 3 endpoints
- USB Application
  - DM has an internal pull-high resistor (1.5K ohm)
  - USB protocol handling
  - USB device state handling
- PS/2 Application Support
  - MCU handle detects PS/2 or USB port
  - Build-in PS/2 port interface for keyboard
- Built-in 8-bit RISC MCU
  - 8 level stacks for subroutine and interruption
  - 8 available interruptions
  - an 8-bit TCC Timer with overflow interruption

- a watch dog timer with its own on-chip RC oscillator to prevent system stand still
- Power-down mode (SLEEP mode)
- Three clocks per instruction cycle
- Built-in power on reset (POR)
- Power-up timer (PWRT)
- Oscillator Startup timer (OST)

- I/O Ports
  - Up to 13 LED sink pins (P20~P22、P26~P27、P4)
  - Each GPIO pin of P0, P1, P3,P4, has an internal programmable pull-high resistor
  - Each GPIO pin of P1, P24~P27,and P4 can wakeup the MCU from sleep mode by input state change
- Internal Memory
  - Built-in 4K*14bits OTP ROM.
  - Built-in 144 bytes general purpose registers(SRAM)
  - Built-in USB Application FIFOs
- Operation Frequency
  - MCU can run at the internal RC oscillator frequency, 6MHz
- Built-in 3.3V Voltage Regulator.
  - For USB PHY power supply
  - Pull-up source for the external USB resistor on DM pin

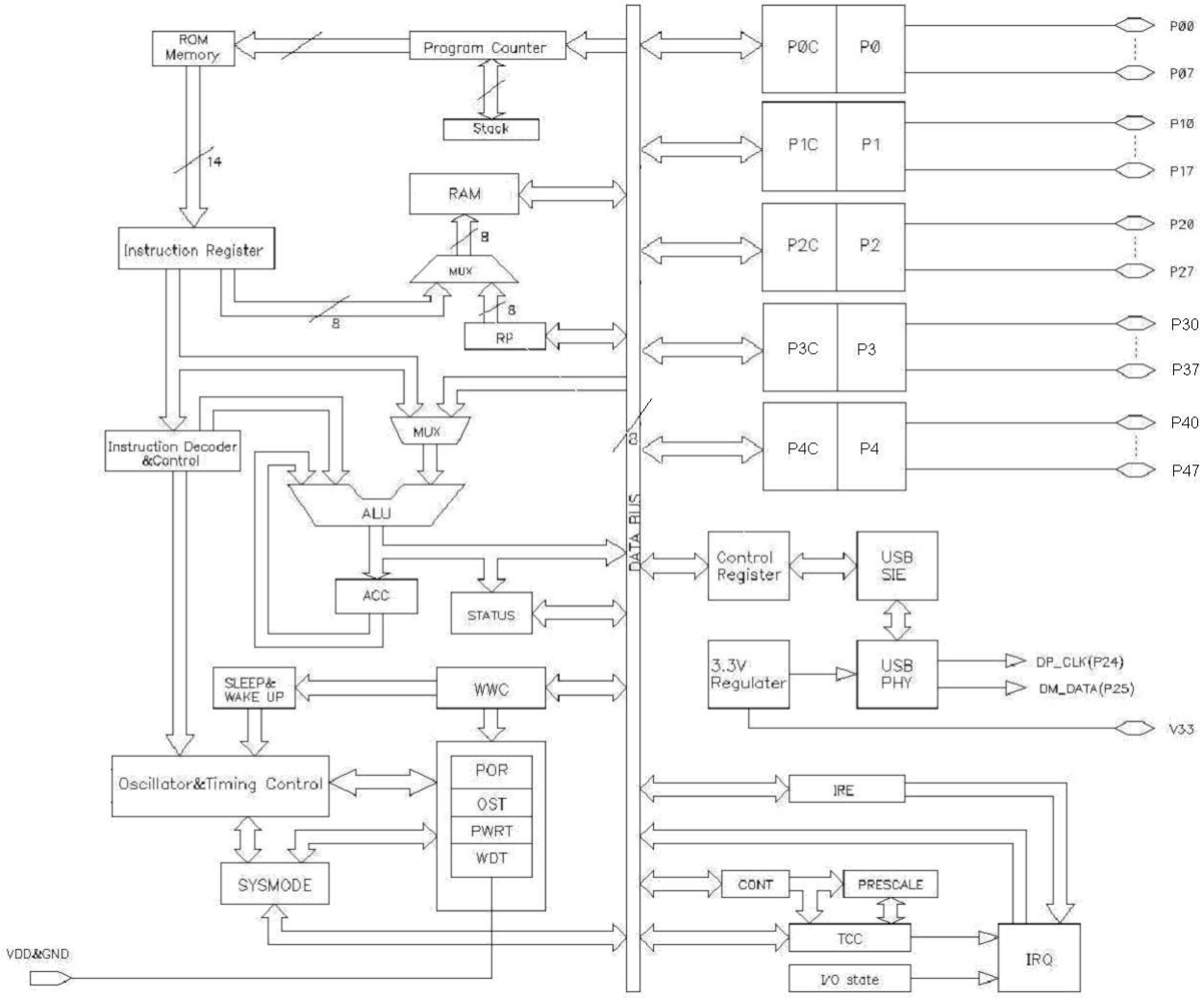
3. APPLICATIONS

- USB and PS/2 both compatible with Keyboard.

4.PIN ASSIGNMENT

Symbol	I/O	Function Description
P27~P26	I/O	LED sink pins
VDD	PWR	Power supply pin.
TEST	I/O	Test pin
VDDA	PWR	Power supply pin.
V33	PWR	3.3V Power supply pin..
VOUT	PWR	3.3V regulator output.
GND	PWR	Ground pin.
DM_DATA (P25)	I/O	USB minus data line interface or DATA for PS/2 keyboard. When the SG8UP5393 is running under PS/2 mode, this pin will have an internal pulled-high resistor, with V_{dd}=5.0V When the SG8UP5393 is running under USB mode, this pin will have an internal pulled-high resistor, 1.5k Ohm, with $V_{3.3}$=3.3V
DP_CLK (P24)	I/O	USB plus data line interface or CLK for PS/2 keyboard When the SG8UP5393 is running under PS/2 mode, this pin will have an internal pulled-high resistor, with V_{dd} =5.0V
P46~P47	I/O	GPIO pins. These pins can be pulled-high internally through software control or LED sink pins.
P40~P45	I/O	GPIO pins. These pins can be pulled-high internally through software control or LED sink pins.
P00~P07	I/O	GPIO pins. These pins can be pulled-high internally through software control.
P30~P37	I/O	GPIO pins. These pins can be pulled-high internally through software control.
P10~P17	I/O	GPIO pins. These pins can be pulled-high internally through software control.
P22~P20	I/O	LED sink pins
VPP/RESETb	PWR	OTP burn supply. And ext reset, low active .

5.LOGIC BLOCK DIAGRAM



6. FUNCTION DESCRIPTION

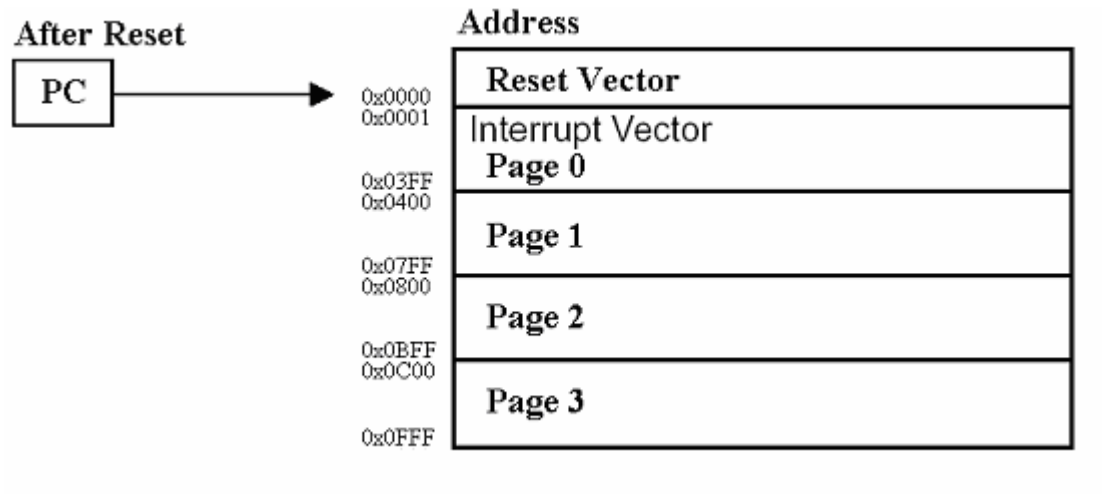
The SG8UP5393 memory is organized into three spaces, namely: User Program memory in 4Kx14bits OTP ROM space, Data Memory in 144bytes SRAM space, and USB Application FIFOs for EndPoint0, EndPoint1, and EndPoint2. Furthermore, several registers are used for special purposes.

6.1 PROGRAM MEMORY

The program space of the SG8UP5393 is 4Kx14bits, and is divided into 4 pages. Each page is 1K long. After Reset, the 12-bit Program Counter (PC) points to location zero of the program space.

The Interrupt Vector is at 0x0001 and accommodates TCC interrupt, EndPoint0 interrupt, Endpoint1 interrupt, Endpoint2 interrupt, USB Reset interrupt and Port2 status change interrupt.

After an interrupt, the MCU will fetch the next instruction from the corresponding address as illustrated in the following diagram.



6.2 DATA MEMORY

The Data Memory has 144 bytes SRAM and 3x8bytes USB Application FIFO.

6.2.1 SPECIAL PURPOSE REGISTER

There are 2 types of register in SG8UP5393, data register and control register. Control registers are accessed only by instruction by CTLR [m] or CTLW [m].

ADDRESS	REGISTER	CONTROL REGISTER
00	IAR	-
01	TCC	-
02	PC	-
03	STATUS	-
04	RP	-
05	P0	P0C
06	P1	P1C
07	P2	P2C
08	P3	P3C
09	P4	P4C
0A	OMCR	PCR
0B	UCR	PECR
0C	UDR	
0D	WCR	LCR

0E	WECR	LECR
0F	IRQ	IMR
10 … 1F	16 × 8 Common Register	
20 … 3F	4 BANK 32 × 8 RAM	

6.2.1.1 Operation Registers

IAR (Indirect Addressing Register)

The IAR is not a physical register. Any read/write operation of IAR accesses the RAM pointed to by RP register.

Initial value on reset: 00000000(Bin)

TCC

An 8-bit real time timer /counter advanced by each instruction cycle clock

Access mode: read/write.

Initial value on reset: 00000000(Bin).

PC (Program Counter)

PC is a 12-bit program counter provides address for PROM.

When execute JMP or CALL, Bit11 ~ bit10 are determined by register OMCR. The register OMCR does not affect the PC if JMP and CALL are not executed.

Instruction JMP, CALL, RET, RETL, RETI, MOV PC A, ADD PC A, TBL may affect PC.

JMP – load the low 10 bits of program counter.

CALL – current PC + 1 and push it into the stack, load low 10 bits of destination address.

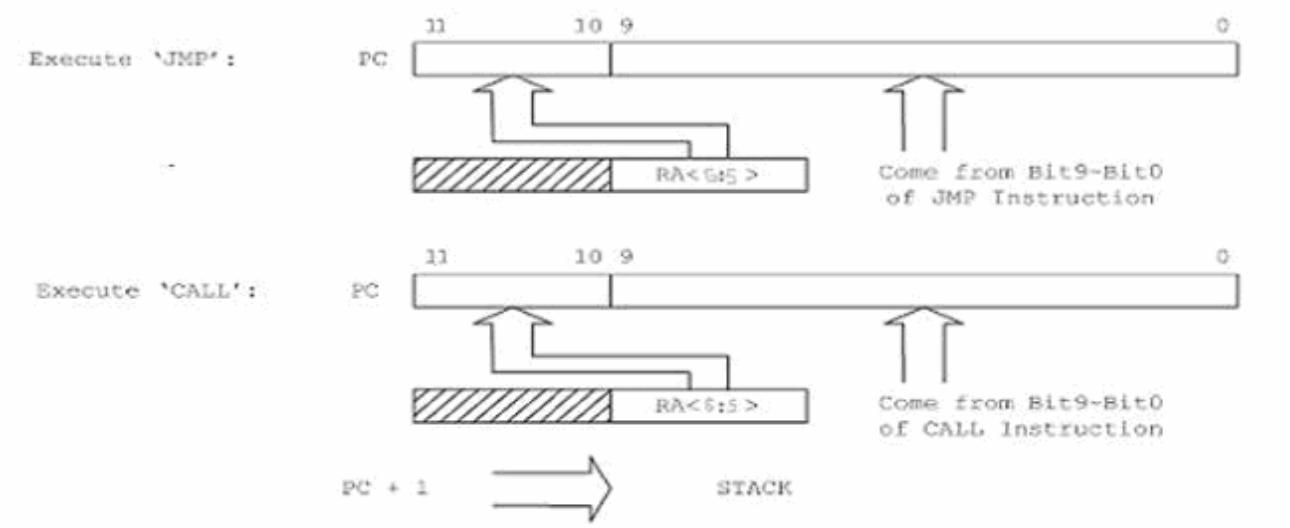
RET, RETL, RETI – load the content of stack1 into program counter.

MOV PC A – load the content of accumulator to program counter, and bit9 and bit10 are cleared to 0.

ADD PC A – Add a relative address to the current PC, and bit9 and bit10 are cleared to 0.

TBL – Add a relative address to the current PC, and do not change the content of bit9 and bit10.

Initial value on reset: 0000 0000 0000(Bin)



STATUS (Status register)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
1	EFT_MD	EFT_STA	TO	PD	Z	DC	C

C Carry flag./borrow flag

0— No carry out from the Most Significant Bit of the result occurred.

1— A carry out from the Most Significant Bit of the result occurred

DC Auxiliary carry flag./borrow flag

0— No carry out from the 4 th low order bit of the result occurred

1— A carry out from the 4 th low order bit of the result occurred

Z Zero flag

0— The result of an arithmetic or logic operation is not zero.

1— The result of an arithmetic or logic operation is zero

PD Power down flag

0 – By execution of the SLP instruction

1 – After power up or by the WDTC instruction

TO Time-out flag

0 – A WDT time out occured

1 – After power up, WDTC instruction, or SLP instruction

EFT_STA EFT flag

0 – EFT not occured

1 – EFT occured

EFT_MD EFT mode

0 – normal mode

1 – EFT mode

Access mode: read only

TO	PD	Condition
1	1	Power-on reset
1	1	WDTC instruction
0	P	WDT time-out
1	0	Power down mode

P: Previous status before WDT reset

Initial value on reset:1001 1uuu (Bin).

RP(RAM Pointer)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
B1	B0	A5	A4	A3	A2	A1	A0

A5~A0 are used to select the registers in the indirect addressing mode.

The address 0x00~0x1F is common space. In 0x20h~0x3F are divided into four banks. Use Bank Select Register.

B1, B0 to select the bank for the RAM address from 0x20~0x3F.

The following are two examples:

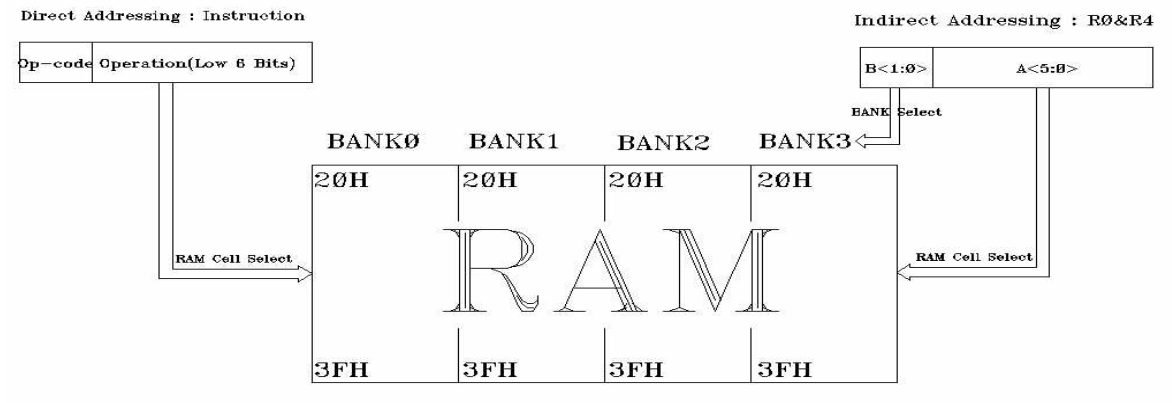
(1) RP=00001100 and RP=01001100 point to the same register 0xCh. Since 0x0Ch is in the common space. Bit6 and Bit7 are meaningless.

(2) RP=100111100 point to the register 0x3C in Back2

B1	B0	RAM Bank
0	0	Bank0
0	1	Bank1
1	0	Bank2
1	1	Bank3

Access mode: read/write.

Initial value on reset: 00uuuuuu(Bin).



P0

I/O Port0 data register.

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P07	P06	P05	P04	P03	P02	P01	P00

Access mode: read/write.

Initial value on reset: uuuu uuuu(Bin).

P1

I/O Port1 data register.

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P17	P16	P15	P14	P13	P12	P11	P10

Access mode: read/write.

Initial value on reset: uuuu uuuu(Bin).

P2

I/O Port2 data register.

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P27	P26	P25	P24	-	P22	P21	P20

Access mode: read/write.

Initial value on reset: uuuu-uuu(Bin).

P3

I/O Port3 data register.

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P37	P36	P35	P34	P33	P32	P31	P30

Access mode: read/write.

Initial value on reset: uuuu uuuu(Bin).

P4

I/O Port4 data register.

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P47	P46	P45	P44	P43	P42	P41	P40

Access mode: read/write.

Initial value on reset: uuuu uuuu(Bin).

OMCR

Operation Mode Control Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	PG1	PG0	-	-	-	-	WDTE

WDTE: Used to set watchdog timer

0 – Disable Watchdog

1 – Enable Watchdog

PG1~0:

Program Rom Selection bits. These three bits are the used to select the page of program memory

PG1	PG0	Program Memory Page [Address]
0	0	Page0 [0000-03FF]
0	1	Page1 [0400-07FF]
1	0	Page2 [0800-0BFF]
1	1	Page3 [0C00-0FFF]

Access mode: read/write

Initial value on reset: 000----1(Bin).

UCR

UDC Control Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SUSPD	-	-	-	-	MA2	MA1	MA0

MA2~0:

USB Indirect Address Bus

SUSPD:

USB PHY Suspend.

0: USB PHY Enable

1: USB PHY Disable

Access mode: read/write

Initial value on reset: 0----000 (Bin).

UDR

UDC Data Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
MD7	MD6	MD5	MD4	MD3	MD2	MD1	MD0

MD7~0

USB Indirect Data Bus

Access mode: read/write

Initial value on reset: 00000000 (Bin).

WCR

Wake-up Control Register

Bit7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WP17	WP16	WP15	WP14	WP13	WP12	WP11	WP10

WP17~10

These bits are used to select which of the Port1 pins is to be assigned to wakeup the MCU while in Power down mode.

1: Enable the function.

0: Disable the function.

Access mode: read/write.

Initial value on reset: 0000 0000(Bin)

WECR

Wake-up Ext Control Register

Bit7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WUE	WP46	WP45	WP44	WP43	WP42	WP41	WP40

WUE

Enable the P24~P27 wake-up function as trigger by port-changed.

1: Enable the wake-up function.

0: Disable the wake-up function.

WP45~P40

These bits are used to select which of the P45~P40 is to be assigned to wakeup the MCU while in Power down mode.

1: Enable the function.

0: Disable the function.

WP46

This bit is used to select P47&P46 is to be assigned to wakeup the MCU while in Power down mode.

1: Enable the function.

0: Disable the function.

Access mode: read/write.

Initial value on reset: 00000000(Bin)

IRQ

Interrupt Status Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Port2_IF	EFT_IF	URST_IF	UTO_IF	EPT0_IF	EPT1_IF	EPT2_IF	TCC_IF

TCC_IF TCC timer overflow interrupt flag, Set when TCC overflow and cleared by software.

EPT2_IF USB Endpoint2 interrupt flag, Set when USB endpoint2 transmission succeed.

EPT1_IF USB Endpoint1 interrupt flag, Set when USB endpoint1 transmission succeed.

EPT0_IF USB Endpoint0 interrupt flag, Set when USB endpoint0 transmission succeed.

UTO_IF USB data line 3ms timer overflow interrupt flag.

URST_IF USB reset interrupt flag, Set when USB host send reset signal.

EFT_IF EFT interrupt flag, Set when EFT occured.

Port2_IF Port2 state change interrupt flag, It will be set at P.24~P.27 State Change

Access mode: read only.

Initial value on reset: 0000 0000(Bin).

A (Accumulator)

Accumulator is for internal data transferring.

CONT

CR (Control register)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
-	INTEN	TSR2	TSR1	TSR0	PSR2	PSR1	PSR0

INTEN

A global interrupt enable flag cannot be written by the CNTW instruction.

0: interrupt masked by the DI instruction.

1: interrupt enabled by the EI or RETI instruction.

Access mode: read only.

TSR2~0

TCC timer prescaler bits.

PSR2~0

Watchdog Timer prescaler bits. These three bits are used as the prescaler of WatchDog Timer. The relationship between the prescaler value and these bits are shown below.

PSR2/TSR2	PSR1/TSR1	PSR0/TSR0	TCC Rate	WDT Rate
0	0	0	1:2	1:1
0	0	1	1:4	1:2
0	1	0	1:8	1:4
0	1	1	1:16	1:8
1	0	0	1:32	1:16
1	0	1	1:64	1:32
1	1	0	1:128	1:64
1	1	1	1:256	1:128

Access mode: read/write.

Initial value on reset: -0111111(Bin).

P0C~P4C

I/O direction control register.

1: I/O high impedance.

0: configure I/O pin as output.

Access mode: read/write.

Initial value on reset: 111111111(Bin).

PCR Pull-up Control Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PS/2	USB	-	-	-	PU3	PU1	PU0

PS/2: PS/2 mode register

1: Enable PS/2 pull-up resistor.

0: Disable PS/2 pull-up resistor.

USB: USB mode register

1: Enable USB pull-up resistor.

0: Disable USB pull-up resistor.

PU3, PU1 and PU0

Port0, Port1, and Port3 pull-high control bits.

1: Enable

0: Disable

Access mode: read/write.

Initial value on reset: 00---000(Bin)

PECR

Pull-up Ext Control Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PP47	PP46	PP45	PP44	PP43	PP42	PP41	PP40

PP47~40

These bits control the pull-high resistor of individual pins in Port4.

1: Enable the function of pull-high

0: Disable the function of pull-high.

Access mode: read/write.

Initial value on reset: 00000000 (Bin)

LCR

LED Control Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LP47	LP46	LP45	LP44	LP43	LP42	LP41	LP40

LP47~40

These bits control the LED sink capacity of individual pins in port4

1: Enable the LED sink capacity.

0: Disable the LED sink capacity.

Access mode: read/write.

Initial value on reset: 00000000 (Bin)

LECR

LED Ext Control Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LP27	LP26	-	-	-	LP22	LP21	LP20

LP27~26, LP22~20

These bits control the LED sink capacity of individual pins in port2.

1: Enable the LED sink capacity.

0: Disable the LED sink capacity.

Access mode: read/write.

Initial value on reset: 00---000 (Bin)

IMR

Interrupt Mask Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
POR2_IE	EFT_IE	URST_IE	UTO_IE	EPT0_IE	EPT1_IE	EPT2_IE	TCC_IE

Interrupt enable bits. Individual interrupt is enabled by setting its associated control bit in the IMR to “1”

1: Enable Interrupt.

0: Disable Interrupt

When USB data timeout overflow interrupt (UTO_IF) occurred, UTO_IE must be cleared in order to clear the UTO timer.

Only when the global interrupt is enabled by the EI instruction that the individual interrupt will work. After DI instruction, any interrupt will not work even if the respective control bits of IMR are set to 1.

Access mode: read/write.

Initial value on reset: 0000 0000 (Bin)

CODE OPTION REGISTER

SG8UP5393 has a code option word that is not a part of normal program memory. The option bits can't be accessed during normal program execution.

Code option register arrangement distribution:

WORD0							
-	-	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
-	-	-	-	-	-	-	-
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
OPT_LED	OPT_C	SP_MD	EFT_MD1	EFT_MD0	UTC1	UTC0	CS

CS：

0: Enable protect function

1: Disable protect function

UTC1, UTC0：

00: 2.5ms

01: 3ms

10: 3.5ms

11: 4ms

EFT_MD1，EFT_MD0：

00: disable EFT module

01: never hold mcu

10: hold mcu when EFT

11: auto hold mcu when EFT

SP_MD：

0: USB mode, Enable USB pull-up resistor by hardware.

1: USB+PS2 mode, Enable USB/PS2 pull-up resistor by software.

OPT_C：

0: AG wire application

1: Carbon wire application

OPT_LED：

0: The current of LED driver (P2) is 15mA .

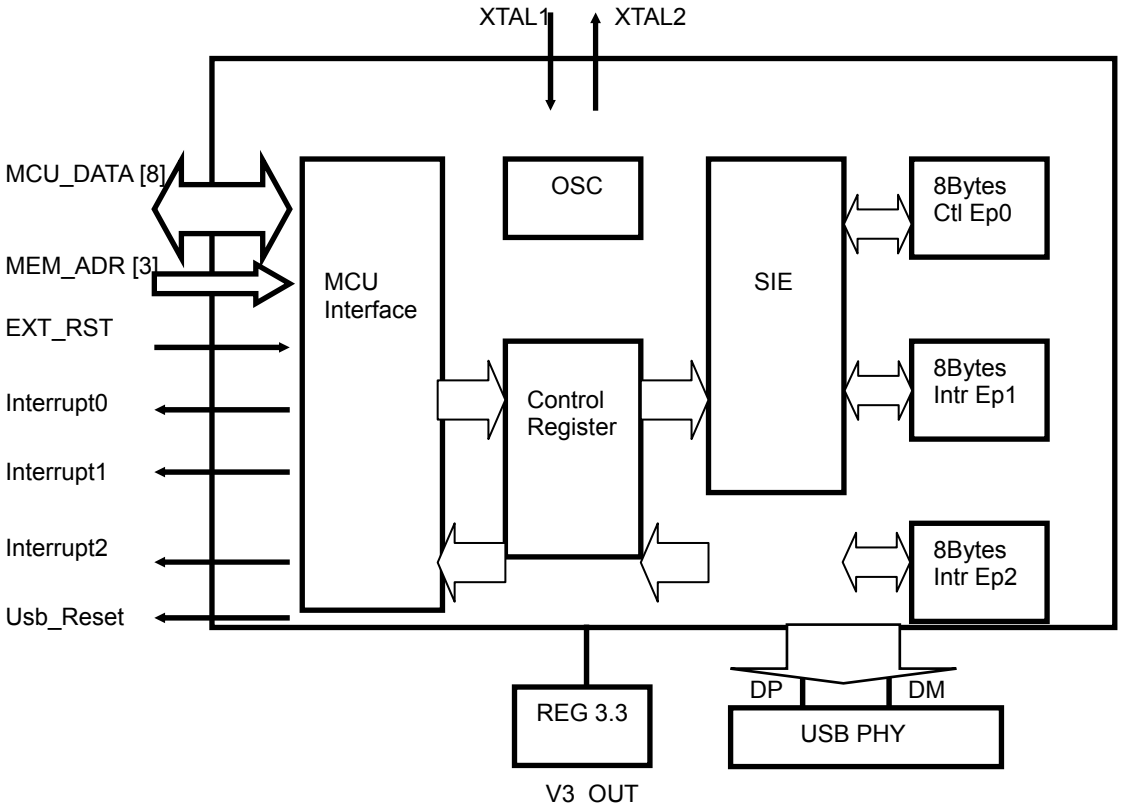
1: The current of LED driver (P2) is 10mA .

Customer ID register arrangement distribution:

WORD1													
Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Customer ID													

6.2.2 USB DEVICE CONTROLLER

6.2.2.1 Block Diagram



6.2.2.2 UDC Indirect Register Table

Index	Description	Access	Bit Position							
			7	6	5	4	3	2	1	0
0	EPT0 CTL Register	R/W	0BSY	0STL	CMD	0DIR	0CLR	SR CNT [3]		
1	EPT1 CTL Register	R/W	1BSY	1STL			1CLR	SR CNT [3]		
2	EPT2 CTL Register	R/W	2BSY	2STL			2CLR	SR CNT [3]		
3	Address Register	R/W	Flag	DEVICE ADDRESS REGISTER [7]						
4	ZPACK FLAG	R/W	0	0	-	-	-	ZPAC K2	ZPAC K1	ZPAC K0
5	EPT0 FIFO	R/W	FIFO SETUP REGISTER [8]							
6	EPT1 FIFO	R/W	FIFO INOUT REGISTER [8]							
7	EPT2 FIFO	R/W	FIFO INOUT REGISTER [8]							

6.2.2.3 UDC Indirect Register Description

EPT0 CTL Register

Bit Number	Bit Mnemonic	Access	Function	Default
7	0BSY	R/W	Endpoint0 Busy, 0BSY = 1 SETUP (h) => ACK (d) OUT (h) => NACK (d) IN (h) => NACK (d) 0BSY = 0 SETUP (h) => ACK (d) OUT (h) = > DATA (h) = > ACK (d) IN (h) => DATA (d) => ACK (h)	1'b1
6	0STL	R/W	Stall Host Command	1'b0
5	CMD	R/W	Setup Package flag	1'b0
4	0DIR	R/W	Bus Direction flag Host => Device, 0DIR is 0 Device => Host, 0DIR is 1	
3	0CLR	R/W	Clear Endpoint0 FIFO pointer to 3'h0	1'b0
2:0	SR CNT	R/W	Endpoint0 Receive and Send Counter SR CNT Number 000: 8bytes 001: 1bytes 010: 2bytes …….. 111: 7bytes	3'h0

EPT1 CTL Register

Bit Number	Bit Mnemonic	Access	Function	Default
7	1BSY	R/W	Endpoint1 Busy 1BSY = 1 IN (h) => NACK (d) 1BSY = 0 IN (h) => DATA (d) => ACK (h)	1'b1
6	1STL	R/W	Endpoint1 Stall	1'b0
3	1CLR	R/W	Clear Endpoint1 FIFO pointer to 3'h0	1'b0

2:0	SR CNT	R/W	Endpoint1 Receive and Send Counter SEND CNT Number 000: 8bytes 001: 1bytes 010: 2bytes …… 111: 7bytes	3'h0

EPT2 CTL Register

Bit Number	Bit Mnemonic	Access	Function	Default
7	2BSY	R/W	Endpoint2 Busy 2BSY = 1 OUT (h) => NACK (d) 2BSY = 0 OUT (h) => DATA (h) => ACK (d)	1'b1
6	2STL	R/W	Endpoint2 Stall	1'b0
3	2CLR	R/W	Clear Endpoint2 FIFO pointer to 3'h0	1'b0
2:0	SR CNT	R/W	Endpoint2 Receive and Send Counter SEND CNT Number 000: 8bytes 001: 1bytes 010: 2bytes …… 111: 7bytes	3'h0

ADDRESS Register

Bit Number	Bit Mnemonic	Access	Function	Default
7	Flag	R/W	This bit set 1,when device send last control in package in endpoint0.	1'b0
6:0	Device Address Register	R/W	Device address, when SetAddress Cmd complete, set this register.	7'h00

ZPACK FLAG

Bit Number	Bit Mnemonic	Access	Function	Default
7		R	This bit must be zero	1'b0

6		R	This bit mus be zero	1'b0
2	ZPACK2	RW	UDC send a zero packet(data packet) when it is 1'b1.	1'b0
1	ZPACK1	RW	UDC send a zero packet(data packet) when it is 1'b1.	1'b0
0	ZPACK0	RW	UDC send a zero packet(data packet) when it is 1'b1.	1'b0

EPT0 FIFO

Bit Number	Bit Mnemonic	Access	Function	Default
7:0	EPT0_FIFO	R/W	Endpoint0 FIFO Register	8'h0

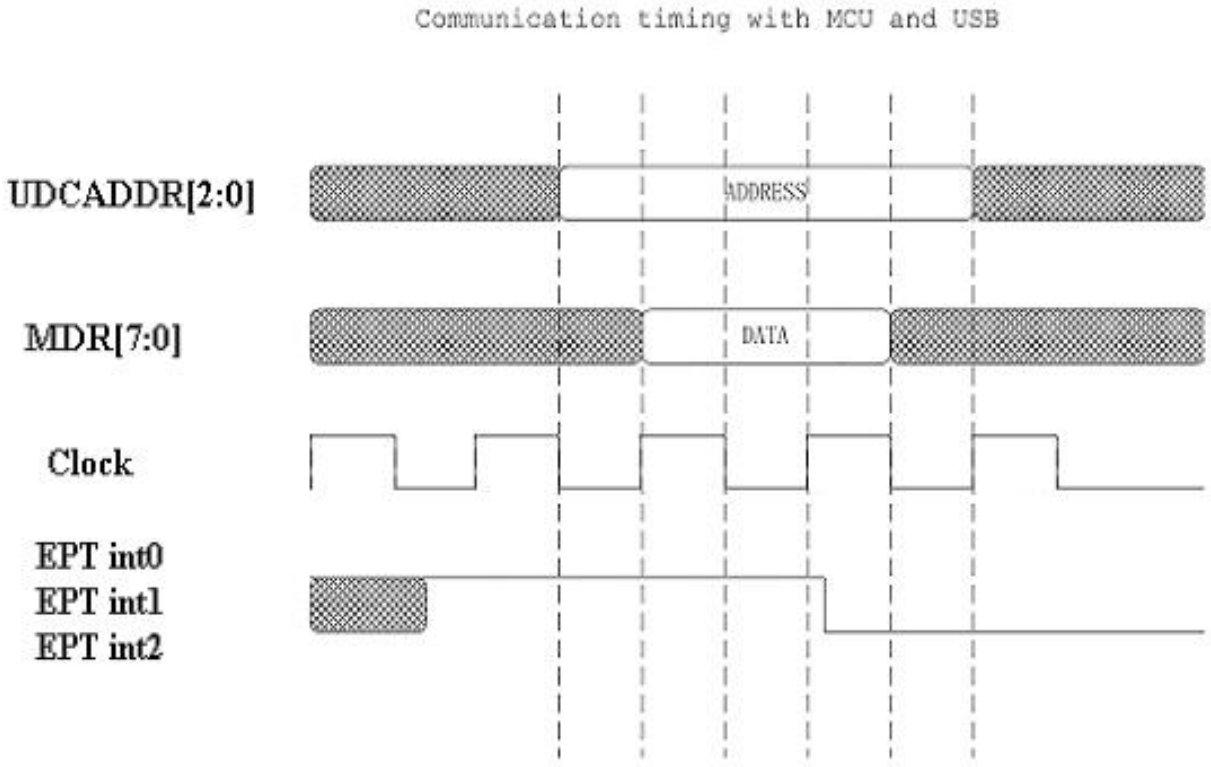
EPT1 FIFO

Bit Number	Bit Mnemonic	Access	Function	Default
7:0	EPT1_FIFO	R/W	Endpoint1 FIFO Register	8'h0

EPT2 FIFO

Bit Number	Bit Mnemonic	Access	Function	Default
7:0	EPT2_FIFO	R/W	Endpoint2 FIFO Register	8'h0

6.2.2.4 UDC Indirect Register Access Timing



6.3 TIMER & WDT

TCC is an 8-bit timer/counter. TCC is also an interrupt source.

The watchdog timer is a free running on-chip RC oscillator. The WDT can be enabled or disabled any time during the normal mode by software. During normal operation or sleep mode, a WDT time-out (if enabled) will cause the device to reset. With 1x prescaler, The WDT time-out period is approximate to 7.6ms.

WDT can't reset the following register:

Address	Name	Remark
0B	UCR	Hold when WDT reset ；
0D	WCR	Hold when WDT reset ；
0E	WECR	Hold when WDT reset ；
CON 05	P0C	Hold when WDT reset ；
CON 06	P1C	Hold when WDT reset ；
CON 07	P2C	Hold when WDT reset ；
CON 08	P3C	Hold when WDT reset ；

CON 09	P4C	Hold when WDT reset ；
CON 0A	PCR	Hold when WDT reset ；
CON 0B	PECR	Hold when WDT reset ；
CON 0F	IMR	Hold when WDT reset ： EFT_ IE、URST_IE、EPT0_IE、EPT1_IE、EPT2_IE；

6.4 I/O PORTS

The I/O P0 is 8bit bi-directional tri-state I/O port. P0 have internal weakly pull-high resistor.

The I/O P1 is 8bit bi-directional tri-state I/O port. P1 have internal weakly pull-high resistor and port input status change wake-up function.

The I/O pin P24 and P25 is the bi-directional tri-state I/O ports with the programmable pull-high resistor (5Kohm). And P25 have a programmable pull-high resistor (1.5K ohm, V33).

The I/O pin P24~P27 can wakeup the MCU from sleep mode.

The I/O pin P20~P22, P26~P27 have the programmable LED sink function.

The I/O P3 is 8bit bi-directional tri-state I/O port. P3 have internal weakly pull-high resistor.

The I/O P4 is 8bit bi-directional tri-state I/O port. P4 have internal weakly pull-high resistor and port input status change wake-up function. P4 can also be used for LED sink function through software.

When the I/O port work as input port, The input signal is shaped by schmitt trigger. The signal is regarded as ‘1’ if the input voltage is higher than 2.0V , and it regarded as ‘0’ if the input voltage is lower than 1.0V.

Then I/O registers and I/O control registers are both readable and writable.

6.5 RESET

A RESET is initiated by

1) Power on reset
2) Watch dog reset
3) USB Reset
4) LVR Reset

6.5.1 POWER-ON RESET

Power-on reset occurs when the device is attached to power and a reset signal is initiated. The signal

will last until the MCU becomes stable. After a Power-on Reset, the MCU enters into following predetermined states, and then, it is ready to execute the program.

a. The program counter is cleared.

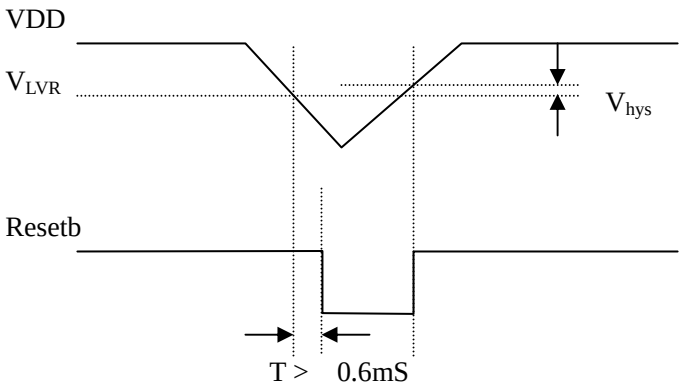
b. The TCC timer and Watchdog timer are cleared.

c. Special registers and special control registers are all set to initial value.

6.5.2 LOW VOLTAGE RESET (LVR)

The MCU also has a low voltage detector that detects low output power condition.

Whenever the voltage of the VDD decreases to below 3.2V, a reset signal is set off. The device produces an internal reset for both rising and fast falling edge of VDD.



6.5.3 WATCH DOG RESET

When the Watchdog timer overflows, it causes the Watchdog to reset. After it resets, the program is executed from the beginning and some registers will be reset. The UDC remains unaffected.

6.5.4 USB RESET

When UDC detects a USB reset signal on USB bus, it interrupts the MCU, then proceed to perform the specified process. After a USB device is attached to the USB port, it cannot respond to any bus transactions until it receives a USB Reset signal from the bus.

6.5.5 POWER-UP TIMER (PWRT)

The Power-up timer provides a fixed 40ms time-out on power-on reset or low voltage reset. The power up timer operates on an internal RC oscillator from the rising edge of internal POR.

6.5.6 OSCILLATOR START-UP TIMER (OST)

The oscillator start-up timer (OST) provides a 1024 oscillator cycle (system clock) delay whenever the PWRT is invoked, or a wake-up from SLEEP state. The delay allows the crystal osciilator or resonator to stabilize before the device exits reset state.

If system wakes up from ‘sleep mode’ ,there is also an OST before Next instruction is executed.

6.5.7 RESET SEQUENCE

On power-up, the reset sequence is as follows.

1) The internal POR signal goes high when the POR trip point is reached.
2) Both the PWRT and OST timers start. In general, PWRT time-out is longer.

6.6 INTERRUPT

The SG8UP5393 has an interrupt vectors in 0x0001. When an interrupt occurs during the MCU running program, it will jump to the interrupt vector (0x0001) and execute the instructions sequentially from interrupt vector.

IRQ is the interrupt status register recording the interrupt request and every interrupt flag bit has a corresponding interrupt mask bit which is defined in the interrupt mask register IMR.

Interrupt is enabled by EI instruction and disabled by DI instruction. When one of the interrupts (enabled) occurs, the next instruction will be fetched from address 001H. Once in the interrupt service routine, the source of an interrupt can be determined by polling the flag bits in IRQ. The interrupt flag bit must be cleared by instructions before leaving the interrupt service routine and before interrupts are enabled to avoid recursive interrupts.

The interrupt condition could be one of the following:

1. TCC Overflow: When the Timer Clock / Counter Register (TCC) overflows, the status flag IRQ[0] will be set to 1. Its interrupt vector is 0x0001.
2. Port2 State Change: When the input signals in P24~P27 changes, the status flag IRQ[7] will be set to 1. it’s interrupt vector is 0x0001.
3. USB Reset When the UDC detects a USB Reset signal on USB bus, the status flag IRQ[5] is set to 1. Its interrupt vector is 0x0001
4. UTO_IF When the UDC detects USB data line 3ms timer overflow, the status flag IRQ[4] is

set to 1. Its interrupt vector is 0x0001

5. EPT0 Interrupt When USB Endpoint0 Package transfer successed, the status flag IRQ[3] is set to 1. Its interrupt vector is 0x0001

6. EPT1 Interrupt When USB Endpoint1 Package transfer successed, the status flag IRQ[2] is set to 1. Its interrupt vector is 0x0001

7. EPT2 Interrupt When USB Endpoint2 Package transfer successed, the status flag IRQ[1] is set to 1. Its Interrupt vector is 0x0001

8. EFT_IF EFT interrupt flag, the status flag IRQ[6] is set to 1. Its Interrupt vector is 0x0001

When an interrupt is generated by 'INT' instruction, the interrupt subroutine entry is address 0002H

6.7 TIMING & CONTROL

The chip has a internal RC oscillator (6MHz) for the whole chip.

6.8 SLEEP & WAKEUP

The SG8UP5393 can enter sleep mode to decrease the power consumption and waken up by port1, port4 and P24~P27.

The sleep mode is entered by executing an instruction 'SLP'. When the MCU is waken up from sleep mode, the MCU starts to execute instructions after OST timeout.

The micro controller can be awakened by

1) WDT timeout if WDT is enabled,
2) Port1 input status changes (if enabled).
3) Port4 input status changes (if enabled)
4) Pin P24~ P27 input status changes (if enabled)

Case 1) will cause the system reset.

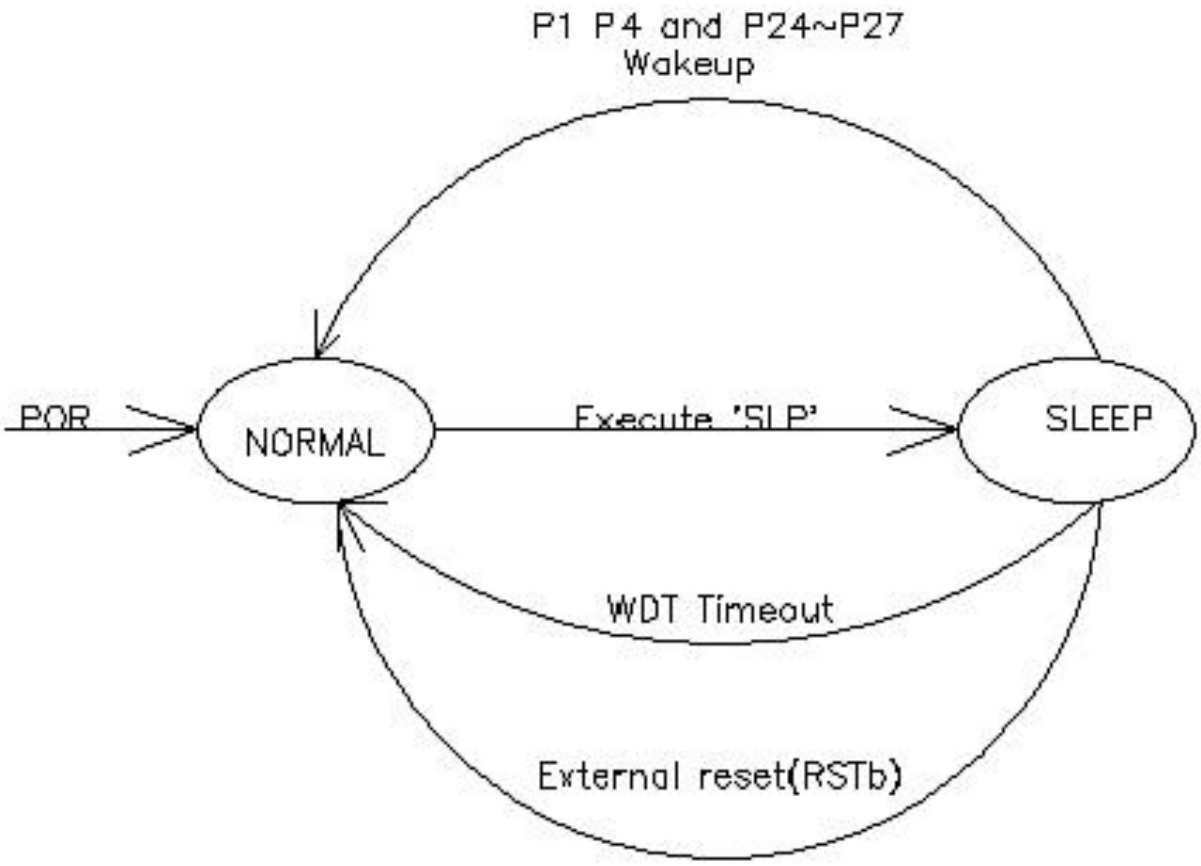
Case 4) will cause the system branch to the interrupt vector or execute next instruction. Please refer to 6.3.1I/O port.

If Port 1 ,Port4 and Pin P24~P27 Input Status Change is used to wake-up the SG8UP5393, the following instructions must be executed before 'SLP' :

```
MOV P1, P1                  ; Read Port 1
MOV A, 11111111b            ; Enable the wakeup function on Port1
MOV WCR, A
SLP                         ; Sleep
NOP
```

When wake up from sleep:

1) Oscillator starts to work.
2) OST time out.
3) MCU begins to execute next instruction or branch to interrupt vector.



6.9 REGISTER STATE

1) Register state on reset or wakeup

Register Name	POR	WDT	Wake up
IAR	uuuuuuuu	pppppppp	pppppppp
TCC	00000000	00000000	Pppppppp
PC	0000 0000 0000	0000 0000 0000	0000 0000 0001 or pppp pppp pppp
STATUS	10011uuu	p00ttppp	Pppttppp
RP	00uuuuuu	00pppppp	pppppppp
P0	Uuuuuuuu	Pppppppp	Pppppppp
P1	Uuuuuuuu	Pppppppp	Pppppppp
P2	Uuuu-uuu	Pppp-ppp	Pppp-ppp
P3	Uuuuuuuu	Pppppppp	Pppppppp
P4	Uuuuuuuu	Pppppppp	Pppppppp
OMCR	000—0-1	000—0-1	Ppp—p-p
UCR	0----000	pppppppp	p----ppp
UDR	uuuuuuuu	pppppppp	Pppppppp
WCR	00000000	pppppppp	Pppppppp
WECR	00000000	pppppppp	Pppppppp
IRQ	000-0000	000-0000	Ppp-pppp
P0C	11111111	pppppppp	Pppppppp
P1C	11111111	pppppppp	Pppppppp
P2C	1111-111	pppppppp	Pppp-ppp
P3C	11111111	pppppppp	Pppppppp
P4C	11111111	pppppppp	pppppppp
PCR	00---000	pppppppp	pp---ppp
PECR	0000000	pppppppp	pppppppp
LCR	0000000	0000000	pppppppp
LECR	00---000	00---000	pp---ppp
IMR	00000000	0pp0ppp0	Pppppppp

Note: -:not existence

u: unkown or don't care

p: previous value before reset

t: check status register state

2) Status register state

Even	TO	PD	P:previous value before reset
Power on reset	1	1	
WDT time out during operating mode	0	P	
WDT wake up during sleep mode	0	0	
Wakeup on pin status change during sleep mode	1	0	
WDTC instruction	1	1	
SLP instruction	1	0	

6.10 INSTRUCTION SET

Each SG8UP5393 instruction is a 12-bit word. An instruction cycle equals to 2 oscillator periods. All instructions are executed within a single instruction cycle, unless a conditional test is true or the PC is changed as a result of an instruction. In this case, the execution takes 2 instruction cycles. The I/O register can be regarded as general register.

MNEMONIC	DESCRIPTION	OPERATION	STATUS AFFECTED	CYCLES
ALU & Memory Category				
DAA	Adjust Hex A to Decimal	Decimal Adjust A	C	1
MOV A, n	Move n to A	n→A	-	1
OR A, n	Logical OR A and n	A∨n→A	Z	1
AND A, n	Logical AND A and n	A&n→A	Z	1
XOR A, n	Logical Exclusive-OR A and n	A⊕n→A	Z	1
SUB A, n	Subtract A from n	n-A→A	Z, C, D, C	1
ADD A, n	Increment A by n	n+A→A	Z, C, D, C	1
MOV [m],A	Move A to Memory	A→[m]	-	1
CLRA	Clear Accumulator	0→A	Z	1
CLR [m]	Clear Memory	0→[m]	Z	1
BCLR [m], b	Bit Clear [m].b	0→[m].b	-	1
BST [m], b	Bit Set [m].b	1→[m].b	-	1
SUB A, [m]	Subtract A from Memory and Store the Result to A	[m]-A→A	Z, C, D, C	1
SUB [m],A	Subtract A from Memory	[m]-A→[m]	Z, C, D, C	
DECA [m]	Decrement Memory by 1 and	[m]-1→A	Z	

	Store the Result to A			1
DEC [m]	Decrement Memory by 1	[m]-1→[m]	Z	
OR A, [m]	Logical OR A and [m], and Store the Result to A	A∨[m]→A	Z	1
OR [m],A	Logical OR A and [m], and Store the Result to [m]	A∨[m]→[m]	Z	1
AND A, [m]	Logical AND A and [m], and Store the Result to A	A&[m]→A	Z	1
AND [m],A	Logical AND A and [m], and Store the Result to [m]	A&[m]→[m]	Z	1
XOR A, [m]	Logical Exclusive-OR A and [m], and Store the Result to A	A⊕[m]→A	Z	1
XOR [m],A	Logical Exclusive-OR A and [m], and Store the Result to [m]	A⊕[m]→[m]	Z	1
ADD A, [m]	Add Memory to A	A+[m]→A	Z, C, D, C	1
ADD [m],A	Add A to Memory	A+[m]→[m]	Z, C, D, C	1
MOV A, [m]	Move Memory to A	[m]→A	Z	1
MOV [m], [m]	Move from Memory to Memory	[m]→[m]	Z	1
NOTA [m]	Logical NOT [m] and Store the Result to A	/[m]→A	Z	1
NOT [m]	Logical NOT [m]	/[m]→[m]	Z	1
INCA [m]	Increment [m] by 1 and Store the Result to A	[m]+1→A	Z	1
INC [m]	Increment [m] by 1	[m]+1→[m]	Z	1
SRCA [m]	Right Shift [m] with Carry and Store the Result to A	[m].b→A.(b-1) [m].0→C,C→A.7	C	1
SRC [m]	Right Shift [m] with Carry	[m].b→[m].(b-1) [m].0→C,C→[m].7	C	1
SLCA [m]	Left Shift [m] with Carry and Store the Result to A	[m].b→A.(b+1) [m].7→C,C→A.0	C	1
SLC [m]	Left Shift [m] with Carry	[m].b→[m].(b+1) [m].7→C,C→[m].0	C	1
SWPA [m]	Swap the high 4 bits and low 4bits of [m] and Move [m] to A	[m].(0-3)→A.(4-7) [m].(4-7)→A.(0-3)	-	1

SWP [m]	Swap the high 4 bits and low 4bits of [m]	[m].(0-3)←→[m].(4-7)	-	1
Control Register Category				
CNTR	Move CONT to A	CONT→A	-	1
CTLR [m]	Move Control Register to A	Control Register→A	-	1
CNTW	Move A to CONT register	A→CONT	-	1
CTLW [m]	Move A to Control Register	A→Control Register	-	1
Program Branch Category				
SDZA [m]	Decrement [m] by 1 and Store the Result to A, Skip if Zero Flag is Set	[m]-1→A, skip if zero	-	False 1 True 2
SDZ [m]	Decrement [m] by 1, Skip if Zero Flag is Set	[m]-1→[m], skip if zero	-	False 1 True 2
SIZA [m]	Increment [m] by 1 and store the result to A, Skip if Zero flag is Set	[m]+1→A, skip if zero	-	False 1 True 2
SIZ [m]	Increment [m] by 1, Skip if Zero Flag is Set	[m]+1→[m], skip if zero	-	False 1 True 2
SBZ [m], b	Skip if [m] .b = 0	If [m].b=0,skip	-	F/T 1/2
SBNZ [m], b	Skip if [m].b = 1	If [m] .b=1,skip	-	F/T 1/2
CALL addr	Subroutine call	PC+1→stack, (PG1,PG0, addr)→PC	-	2
JMP addr	Non-conditional Jump	(PG1,PG0, addr)→PC	-	2
RETL n	Subroutine return	n→A, pop stack to PC	-	2
INT	Interrupt	PC+1→stack, 002H→PC	-	1
RET	Return from Subroutine	Pop stack to PC	-	2
RETI	Return from Interrupt	Pop stack to PC, Enable Interrupt	-	2
TBL	JMP	[02H]+A→[02H], Bits 8-9 of [02H] unchanged	Z, C, D, C	2
Other Instructions				
NOP	No Operation	NOP	-	1
SLP	Go to Sleep Mode	0→WDT, Stop oscillator	TO, PD	1
WDTC	Clear WDT	0→WDT	TO, PD	1

EI	Enable Interrupt	Enable Interrupt	-	1
DI	Disable Interrupt	Disable Interrupt	-	1

Note: Any instructions that write to PC need two instruction cycles to complete the execution.

n: 8-bit immediate data

m: 00H~3FH hex data memory address

A: Accumulator

b: 0~7 number of bits

addr: program memory address label

7.ABSOLUTE MAXIMUM RATINGS

Symbol	Min	Max	Unit
Temperature under bias	0	70	℃
Storage temperature	-65	150	℃
Input voltage	-0.5	6.0	V
Output voltage	-0.5	6.0	V

8.DC ELECTRICAL CHARACTERISTIC

(T=25℃, Vdd=5V, Vss=0V)

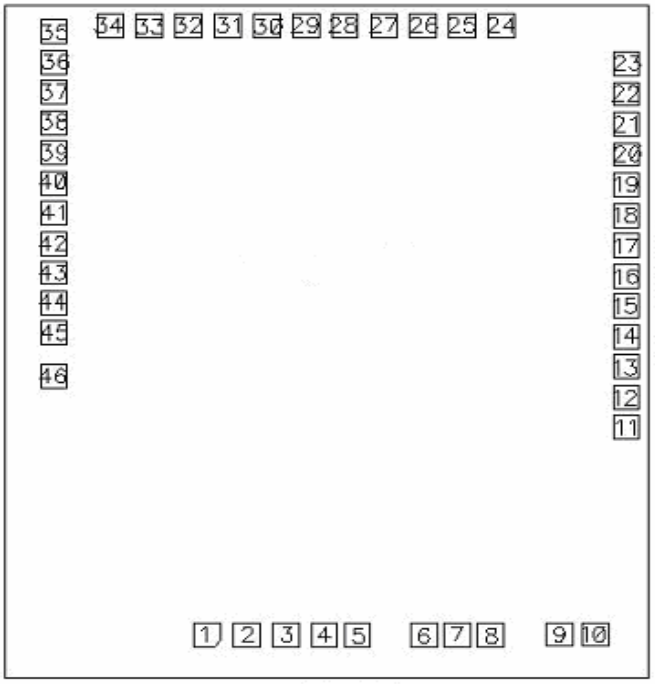
Symbol	Parameter	Condition	Min	Type	Max	Unit
3.3V Regulator						
Vreg	Output voltage of 3.3v Regulator	Vdd=4.4V~5.5V	3.0	3.3	3.6	V
Vreset	Low Power Reset detecting the Voltage		-	3.2	-	V
MCU operation						
Iil	Input Leakage Current for input pins	VIN=VDD, VSS	-	-	±1	uA
Vihx	Clock Input High Voltage	OSCI	5	-	-	V
Vilx	Clock Input Low Voltage	OSCI	-	-	0	V
Icc	VDD operating supply current Normal frequency operation mode	Crystal type Freq = 6MHz Output pins floating	-	-	10	mA

Isb1	Operating supply current 1-Power down mode	All input and I/O pins at VDD Output pins floating WDT disabled	-	-	80	uA
Isb2	Operating supply current 2-Power down mode	All input and I/O pins at VDD Output pins floating WDT enable	-	-	100	uA
GPIO Pins						
Vih	Input High Voltage	Port0&Port1 &Port3&Port4	3.0	-	-	V
		Port2	2.5	-	-	V
Vil	Input Low Voltage	Port0&Port1 &Port3&Port4	-	-	2.3	V
		Port2	-	-	1.0	V
Voh1	Output High Voltage (P20~P22, P26 and P27)	Isink = 10mA Vdd = 5V	-	2.4	-	V
Voh2	Output High Voltage (P24, P25)	Isink = 5mA Vdd = 5V	-	2.4	-	V
Voh3	Output High Voltage (Port5&Port6 & Port8 and P40~P43, P45~P47)	Isink = 10mA Vdd = 5V	-	2.4	-	V
Vol1	Output Low Voltage (P26 and P27 normal mode)	Isink = 10mA Vdd = 5V	-	0.4	-	V
Vol2	Output Low Voltage (P24, P25)	Isink = 5mA Vdd = 5V	-	0.4	-	V
Vol3	Output Low Voltage (P20~P22, P26 and P27 sink LED)	Isink = 10mA Vdd = 5V	-	3	-	V
Vol4	Output Low Voltage (P40~P47 normal mode)	Isink = 10mA Vdd = 5V	-	0.4	-	V
Vol5	Output Low Voltage (P40~P47 sink LED)	Isink = 10mA Vdd = 5V	-	1	-	V
R_{PH1}	pull-high resister (Port0, 3, P40~P43, P45~P47)	Input pin with pull-high resistor	-	10	-	KΩ
R_{PH2}	pull-high resister (Port1)	AG wire application	-	20	-	KΩ
		Carbon wire application	-	1.8	-	MΩ

Iph1	Input current with pull-high resister (P24~P27)	Input pin with pull-high Vin=Vss	-	2.27	-	mA
USB Interface						
Voh	Static Output High	USB operation Mode	2.8	-	3.6	V
Vol	Static Output Low		-	-	0.3	V
Vdi	Differential Input Sensitivity		0.2	-	-	V
Vcm	Differential Input Command Mode Range		0.8	-	2.5	V
Vse	Single Ended Receiver Threshold		0.8	-	2.0	V
Cin	Transceiver Capacitance		-	-	20	PF
Vrg	Output Voltage of internal Regulator		3.0	-	3.6	V

9. DICE INFORMATION

9.1 PAD LOCATION & BONDING DIAGRAM

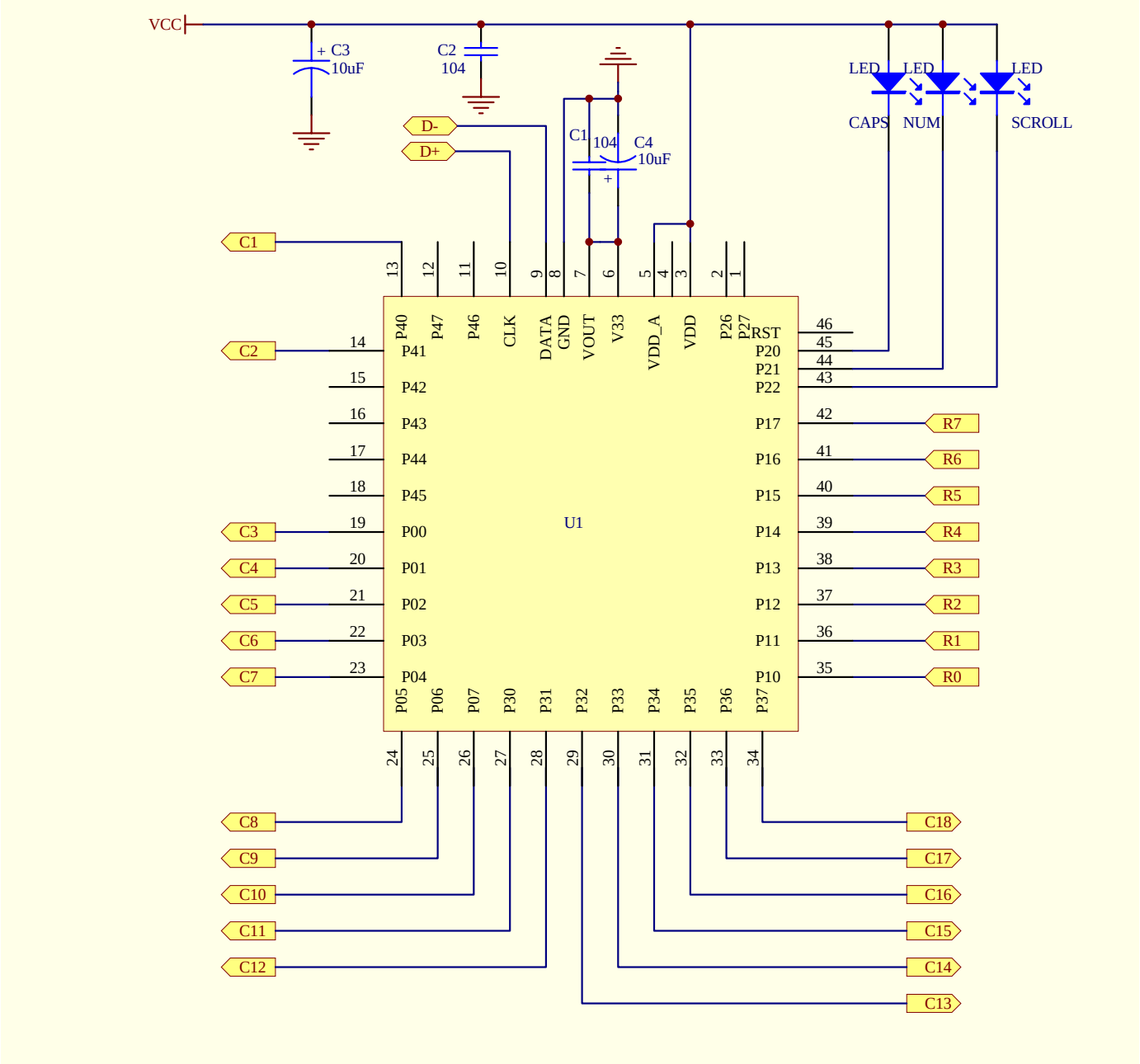


PAD diagram of SG8UP5393
Substrate Size:X=2500um;Y=2800um
Substrate Connect GND

BONDING DIAGRAM:

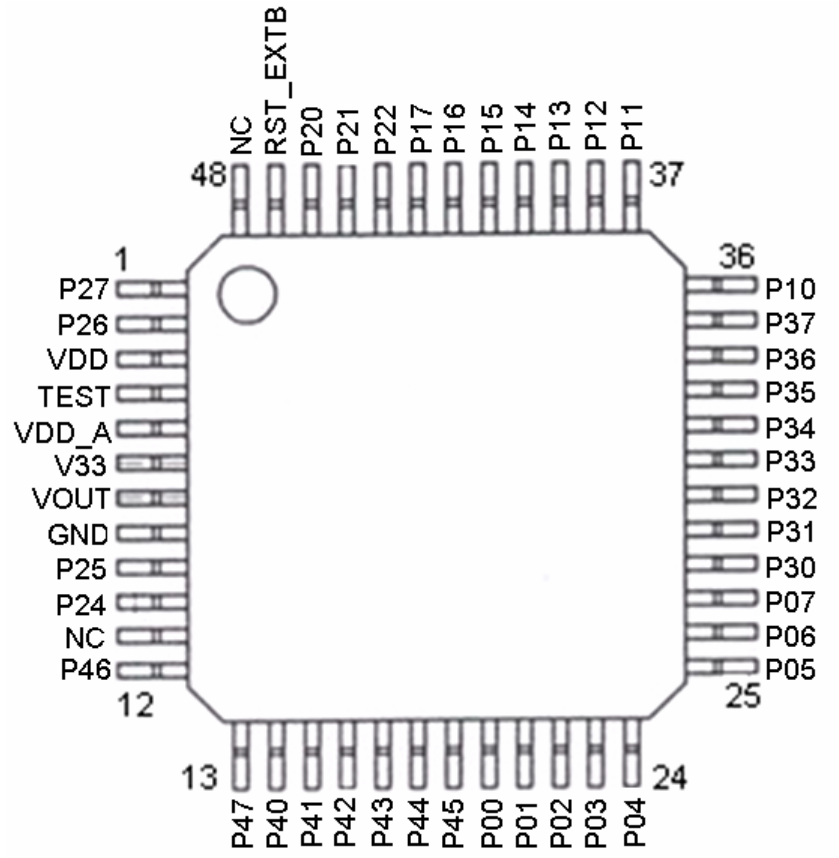
PIN NO	NAME	SG8UP5393 X	SG8UP5393 Y	PIN NO	NAME	SG8UP5393 X	SG8UP5393 Y
1	P27	615.09	148.06	24	P05	1512.21	2222.96
2	P26	735.09	148.06	25	P06	1392.99	2222.96
3	VDD	855.09	148.06	26	P07	1273.77	2222.96
4	TEST	973.09	148.06	27	P30	1154.55	2222.96
5	VDD_A	1073.10	148.06	28	P31	1035.33	2222.96
6	V33	1277.73	148.06	29	P32	916.11	2222.96
7	VOUT	1377.73	148.06	30	P33	796.89	2222.96
8	GND	1477.73	148.06	31	P34	677.67	2222.96
9	P25	1690.23	149.21	32	P35	558.45	2222.96
10	P24	1800.23	149.21	33	P36	439.23	2222.96
11	P46	1892.96	855.15	34	P37	320.01	2222.96
12	P47	1892.96	958.37	35	P10	148.06	2203.79
13	P40	1892.96	1061.59	36	P11	148.06	2100.57
14	P41	1892.96	1164.81	37	P12	148.06	1997.35
15	P42	1892.96	1268.03	38	P13	148.06	1894.13
16	P43	1892.96	1371.25	39	P14	148.06	1790.91
17	P44	1892.96	1474.47	40	P15	148.06	1687.69
18	P45	1892.96	1577.69	41	P16	148.06	1584.47
19	P00	1892.96	1680.91	42	P17	148.06	1481.25
20	P01	1892.96	1784.13	43	P22	148.06	1381.25
21	P02	1892.96	1887.35	44	P21	148.06	1279.00
22	P03	1892.96	1990.57	45	P20	148.06	1176.75
23	P04	1892.96	2093.79	46	RST_EXTb	147.02	1027.85

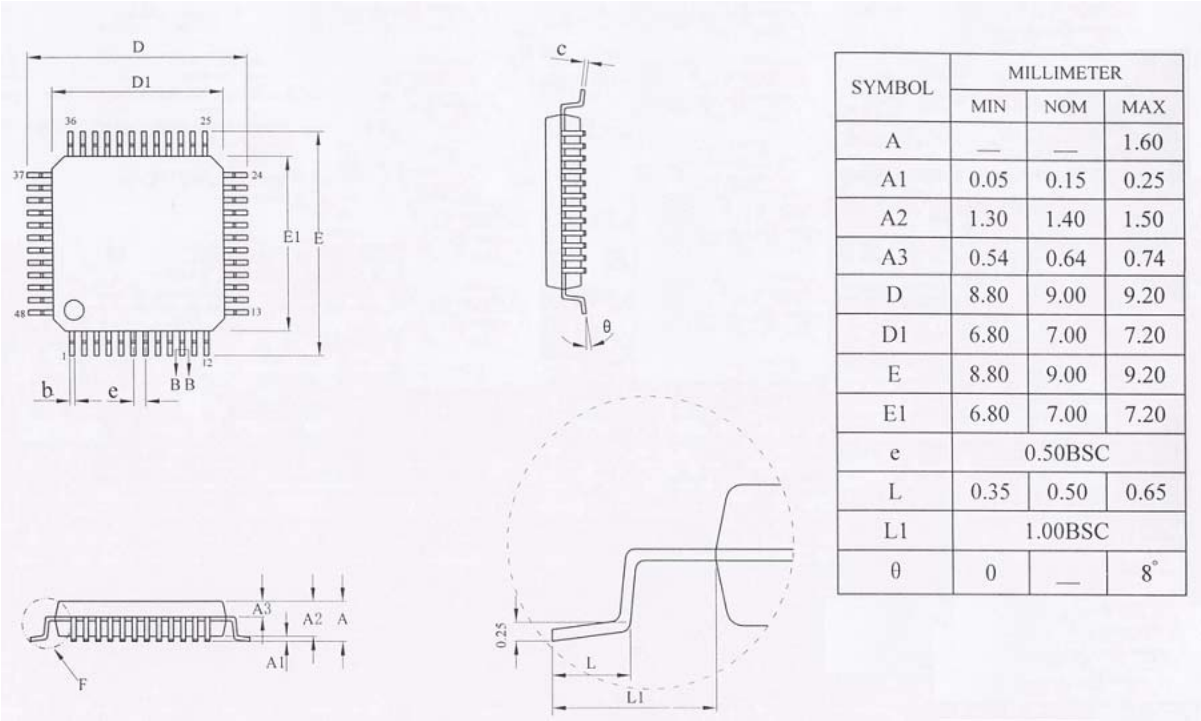
9.2 Dice Application Circuit



10 PACKAGE (LQFP48L)

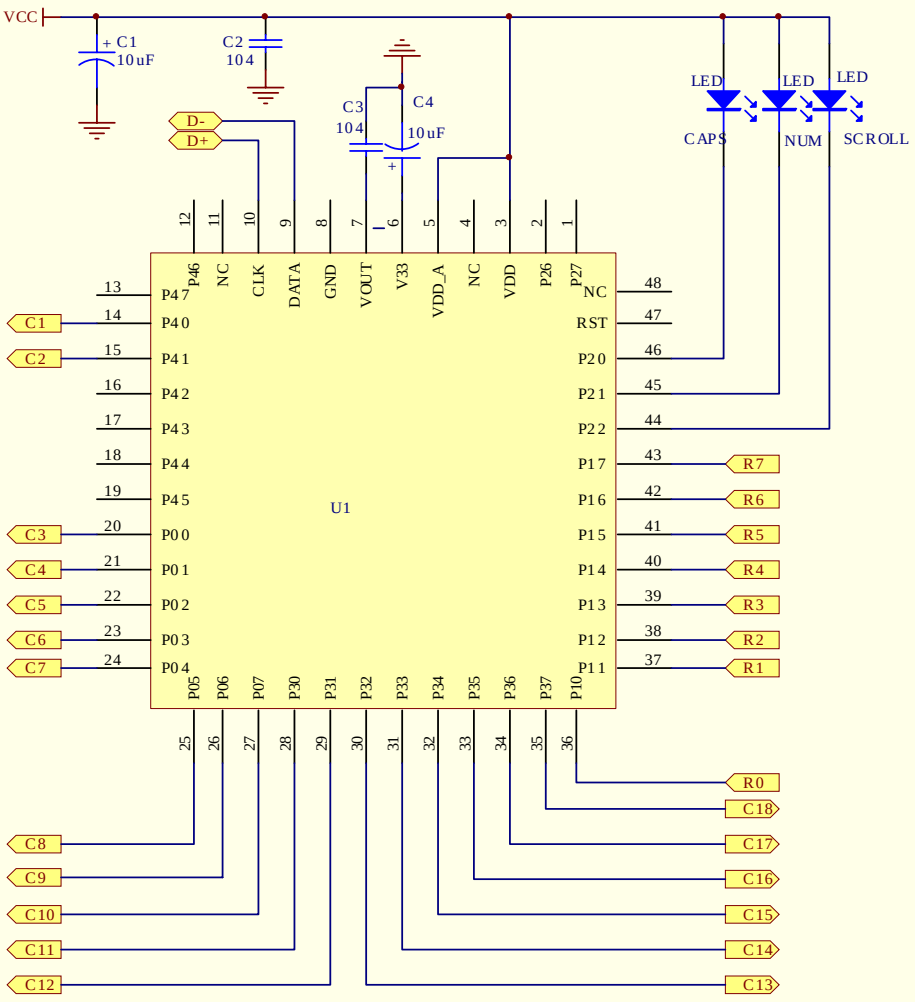
10.1 Package Information





SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	0.15	0.25
A2	1.30	1.40	1.50
A3	0.54	0.64	0.74
D	8.80	9.00	9.20
D1	6.80	7.00	7.20
E	8.80	9.00	9.20
E1	6.80	7.00	7.20
e	0.50BSC		
L	0.35	0.50	0.65
L1	1.00BSC		
θ	0	—	8°

10.2 Application Circuit



11. REVISION HISTORY

Version	Update date	Revised Content	Version by	Confirmed by
V1.0	2011-4-7	Orignal	LiuXing	
V1.1	2011-4-28	Update DC Characteristics	LiuXing	
V1.2	2013-3-25	Add Package information	LiuXing	
V1.3	2014-9-22	Add IC package Application SCH	LiuXing	