X51RL Serier Block Diagram

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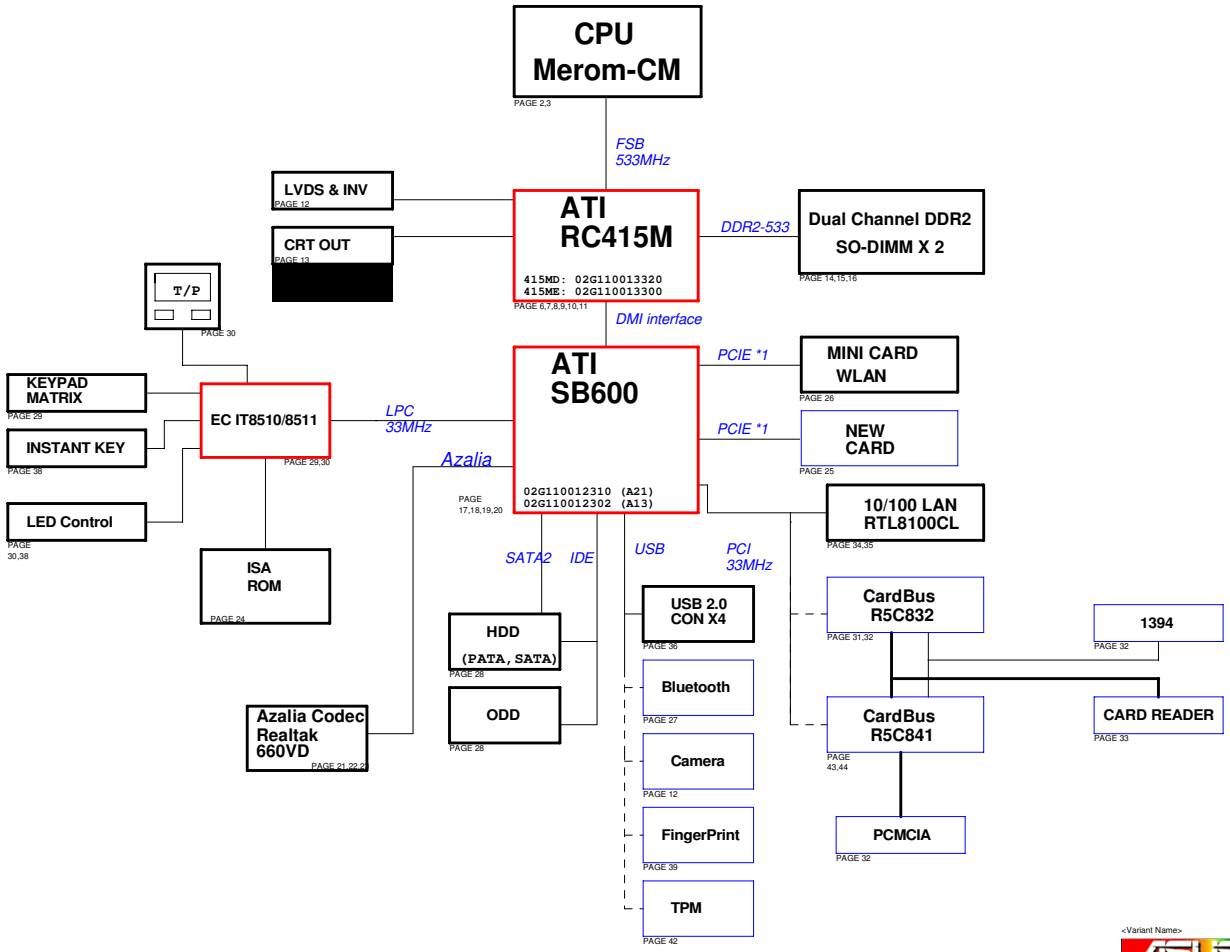

<Variant Name>

Title : BLOCK DIAGRAM

ASUSTeK COMPUTER INC

Engineer: Pommy Lu

Size	Project Name	Rev
Custom	X51RL	2.0

Date: Monday, August 06, 2007 Sheet 1 of 63

<< Kennedy_Zhang >>

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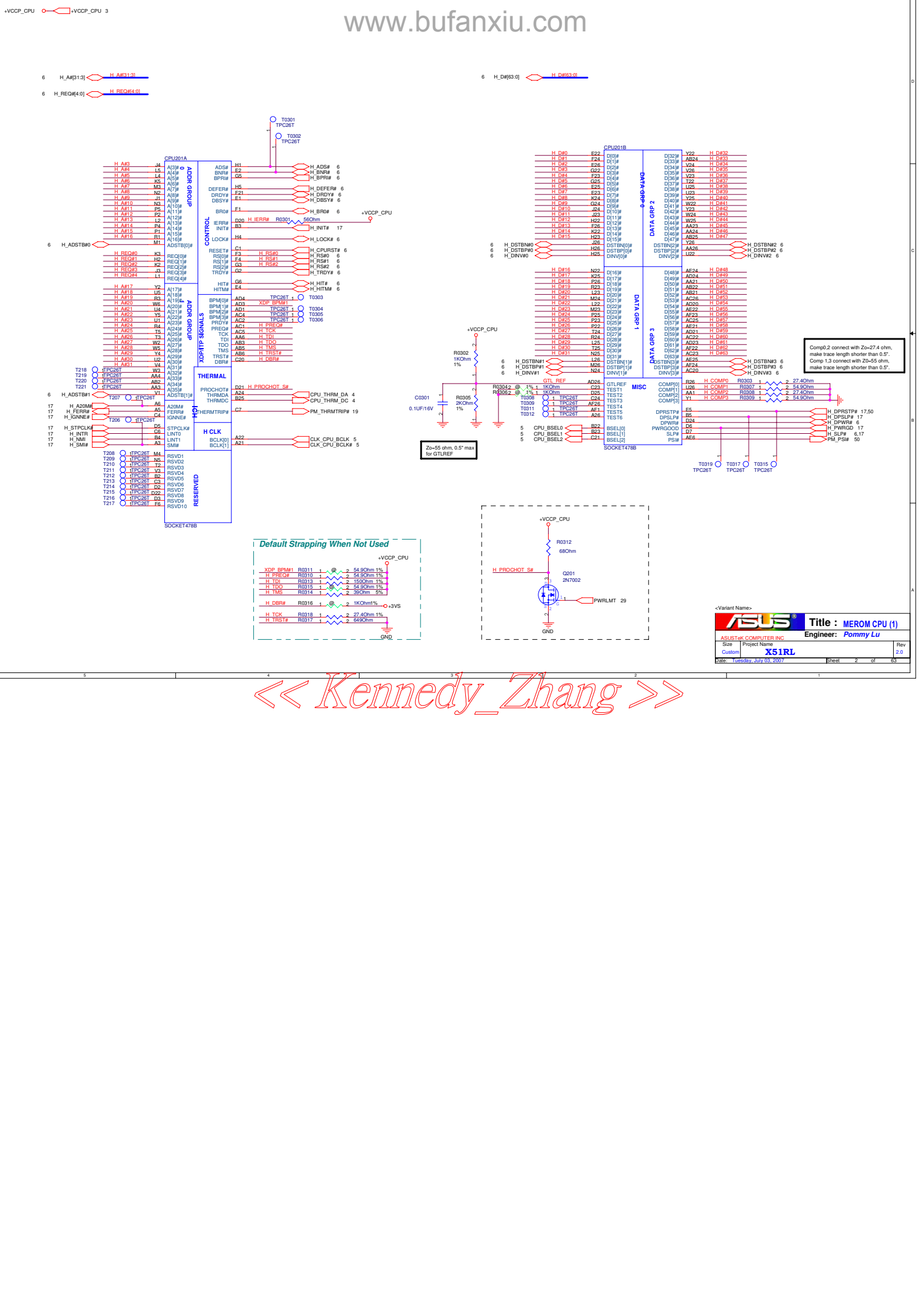

<< Kennedy_Zhang >>

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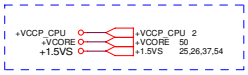
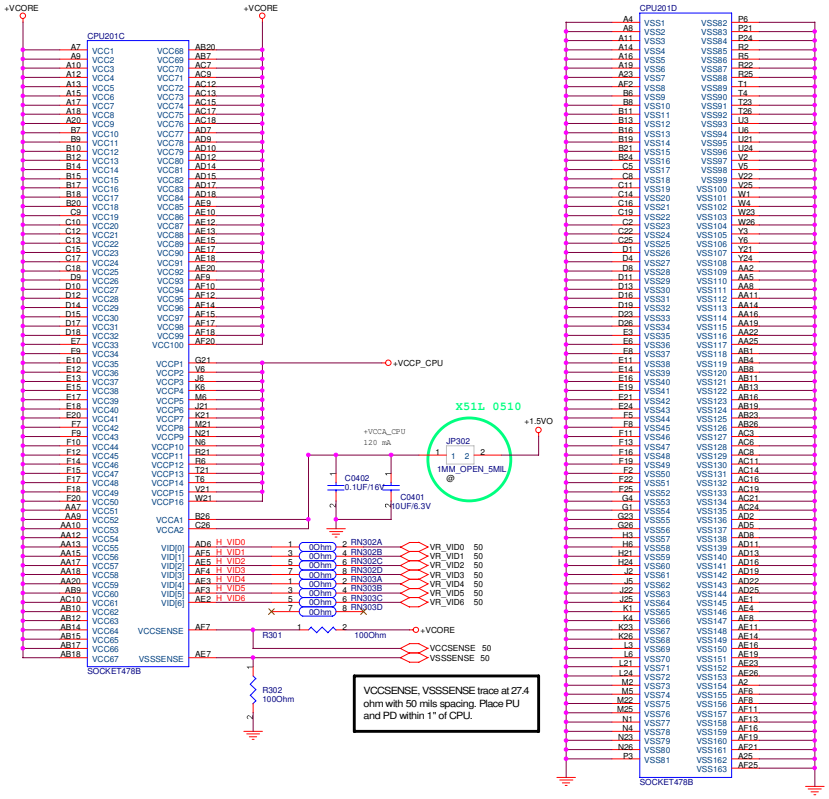
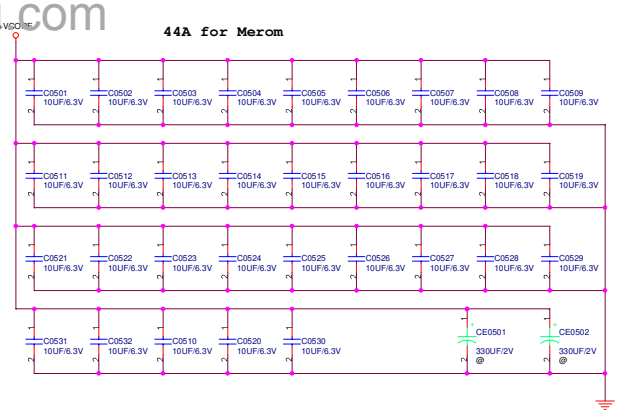




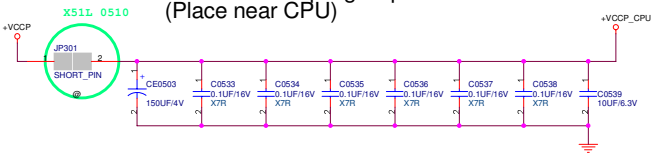


Decoupling guide from INTEL

VCORE	22uF/10V	* 32pcs
	330uF/2V	* 6pcs
VCCP	0.1uF	* 6pcs for CPU
	150uF	* 1pcs for CPU

VCORE	10uF/10V	* 32pcs
	330uF/2V	* 0pcs
VCCP	0.1uF	* 6pcs for CPU
	150uF	* 1pcs for CPU
	10uF/10V	* 1pcs

+VCCP Decoupling Capacitor (Place near CPU)



ASUSTeK COMPUTER INC

Title : MEROM CPU (2)

Engineer: Pommy Lu

Size	Project Name	Rev
Custom	X51RL	2.0

Date: Tuesday, July 03, 2007 Sheet 3 of 63

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+5VS
+3VS

+5VS 13,20,22,23,28,29,30,37,38,50,61
+3VS 2,5,9,12,13,14,15,17,18,19,20,21,22,23,25,26,28,29,31,32,33,34,37,39,40,42,43,50,52,60,61

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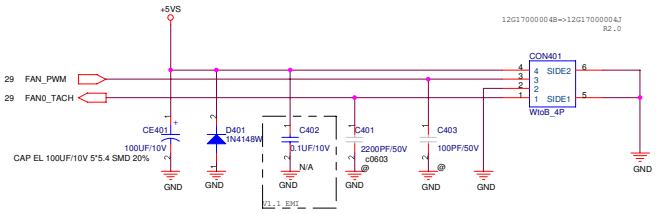
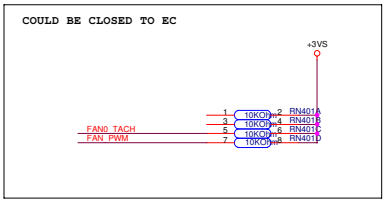
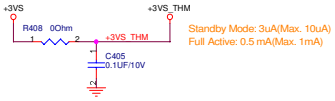
Fan Speed Control

KBC will issue a analog (a voltage level) signal.

SW: FAN_DA1 must be low during S3



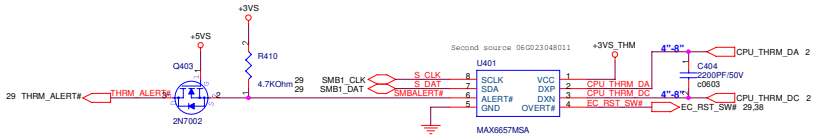




Route H_THERMDA and H_THERMDC on the same layer

----------OTHER SIGNALS
12 mils
==========GND
10 mils
=========H_THERMDA(10 mils)
10 mils
=========H_THERMDC(10 mils)
10 mils
=========GND
12 mils
----------OTHER SIGNALS

Avoid BPSB,Power



<Variant Name>

Title : THER-SENSOR,FAN
Engineer: MICHAEL WANG
ASUSTeK COMPUTER INC
Size: Custom | Project Name: X51RL | Rev: 2.0
Date: Tuesday, July 03, 2007 | Sheet 4 of 63

<< Kennedy_Zhang >>

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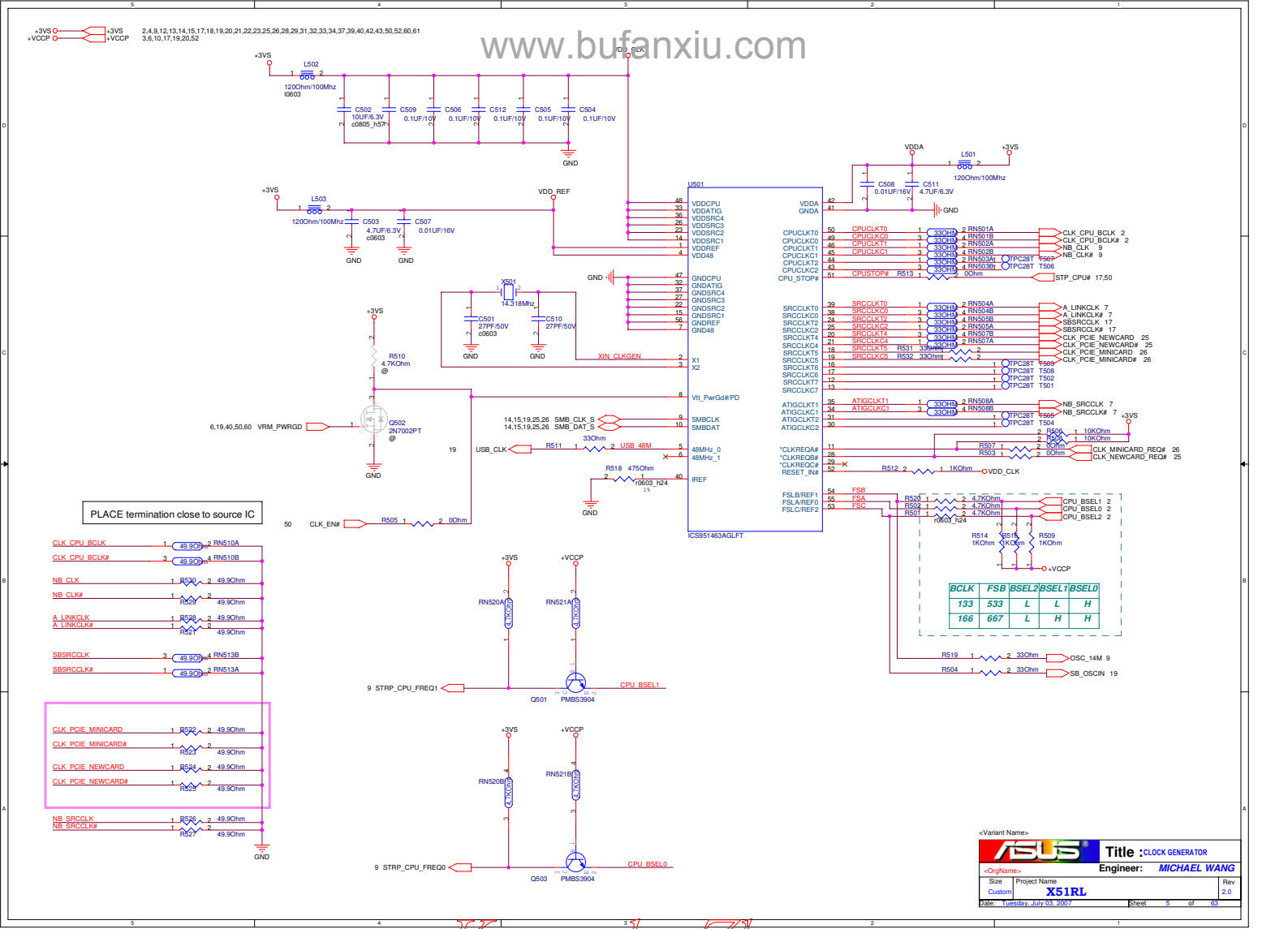

<Variant Name>

Title : CLOCK GENERATOR

<OrgName>

Engineer: MICHAEL WANG

Size	Project Name	Rev
Custom	X51RL	2.0

Date: Tuesday, July 03, 2007 Sheet 5 of 63

<< Kennedy_Zhang >>

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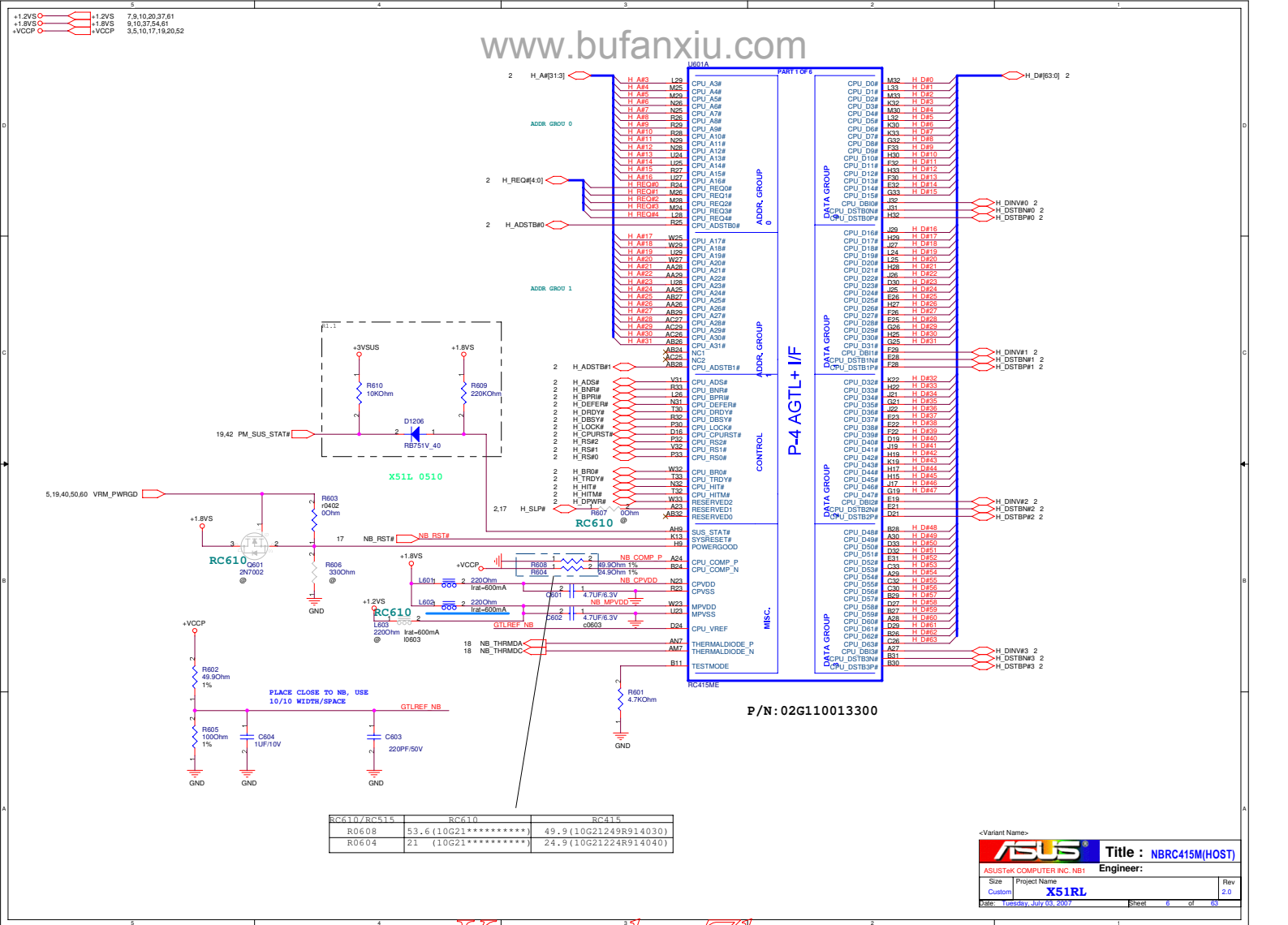

RC610/RC515	RC610	RC415
R0608	53.6(10G21**********)	49.9(10G21249R914030)
R0604	21 (10G21**********)	24.9(10G21224R914040)

<Variant Name>

ASUSTeK COMPUTER INC. NB1

Title : NBRC415M(HOST)

Engineer:

Size	Project Name	Rev
Custom	X51RL	2.0

Date: Tuesday, July 03, 2007 Sheet 6 of 63

<< Kennedy_Zhang >>

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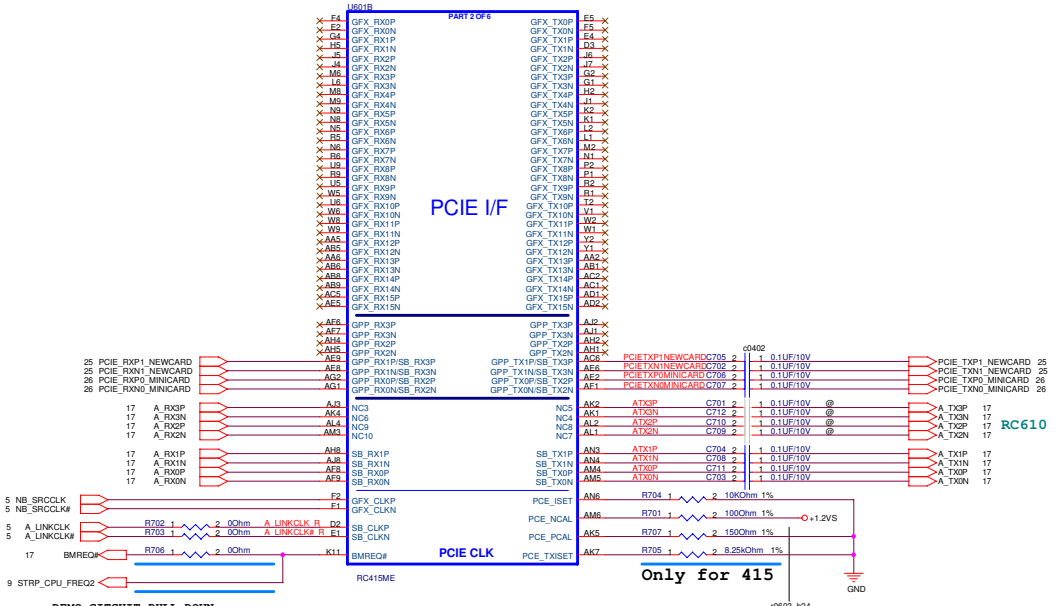
+1.2VS +1.2VS 6,9,10,20,37,61



r0603_h24

RC610/RC515	RC610	RC415
R0704	1.47K(10G21**********)	10K(10G213100213030)
R0701	2K (10G21**********)	100(10G213100013010)
R0707	562 (10G21**********)	150(10G213150013030)

<Variant Name>

ASUSTeK COMPUTER INC. NB1

Title : NB-945PM(DMI & CFG)

Engineer: MICHAEL WANG

Size	Project Name	Rev
Custom	X51RL	2.0

Date: Tuesday, July 03, 2007 Sheet 7 of 63

<< Kennedy_Zhang >>

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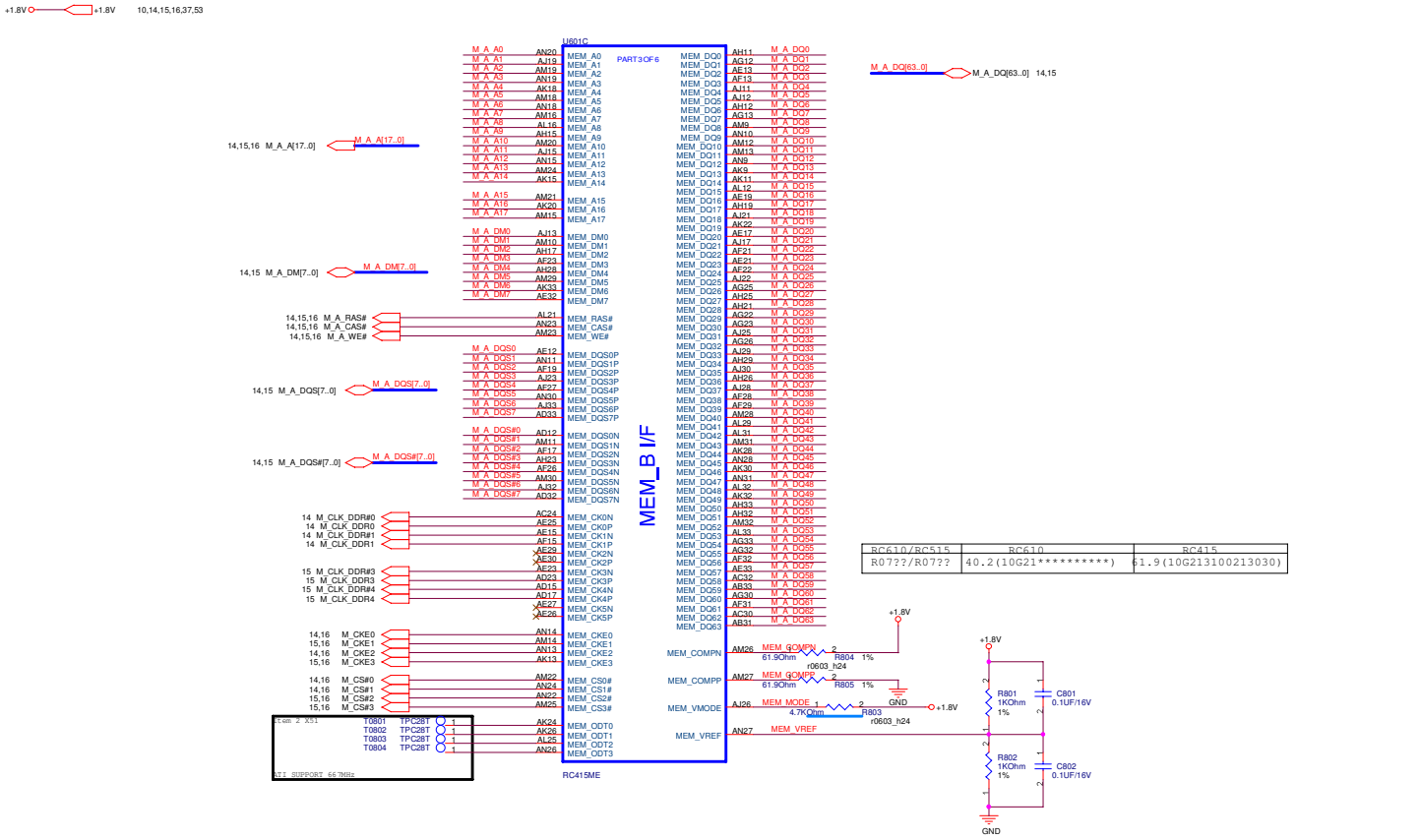

RC610/RC515	RC610	RC415
R07??/R07??	40.2(10G21*********)	61.9(10G213100213030)

<Variant Name>

Title : NB_945PM(PCI-E)

ASUSTeK COMPUTER INC. NB1 Engineer: MICHAEL WANG

Size	Project Name	Rev
Custom	X51RL	2.0

Date: Tuesday, July 03, 2007 Sheet 8 of 63

<< Kennedy_Zhang >>

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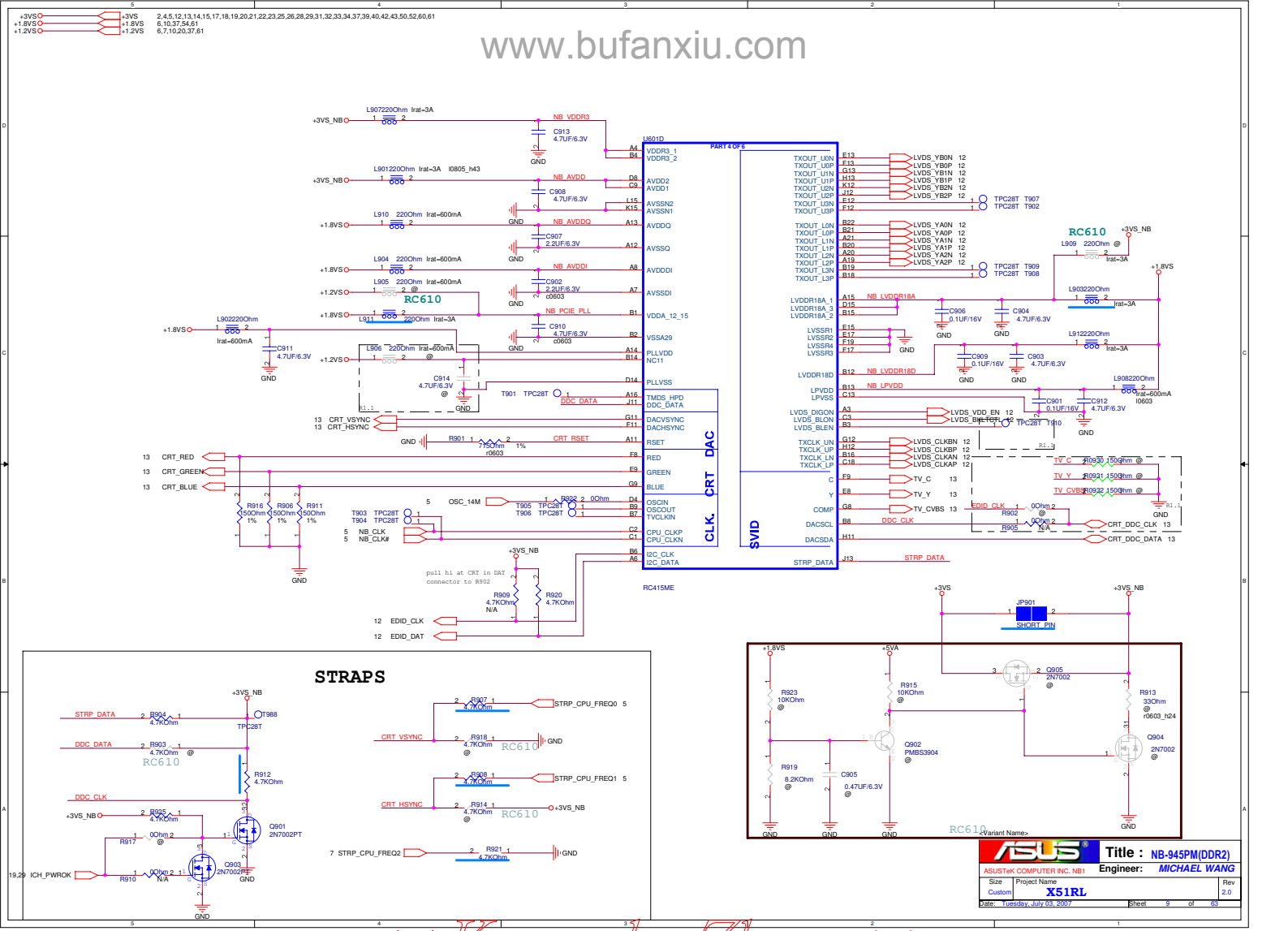

ASUSTeK COMPUTER INC. NB1

Title : NB-945PM(DDR2)

Engineer: MICHAEL WANG

Size	Project Name	Rev
Custom	X51RL	2.0

Date: Tuesday, July 03, 2007 Sheet 9 of 63

<< Kennedy_Zhang >>

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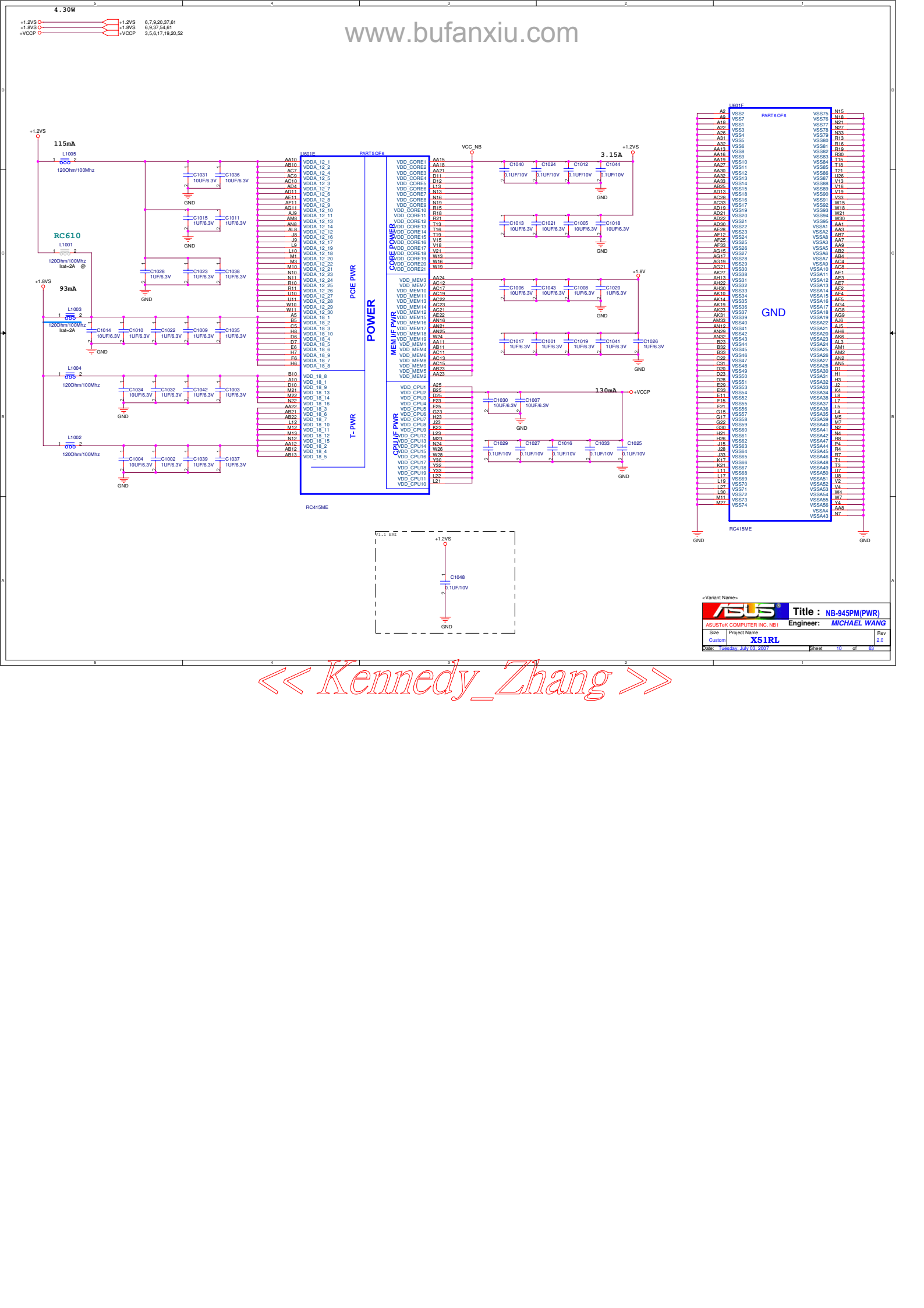

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<Variant Name>

Title : HISTORY

ASUSTeK COMPUTER INC

Engineer: MICHAEL WANG

Size	Project Name	Rev
Custom	X51RL	2.0

Date: Wednesday, May 16, 2007 Sheet 11 of 63

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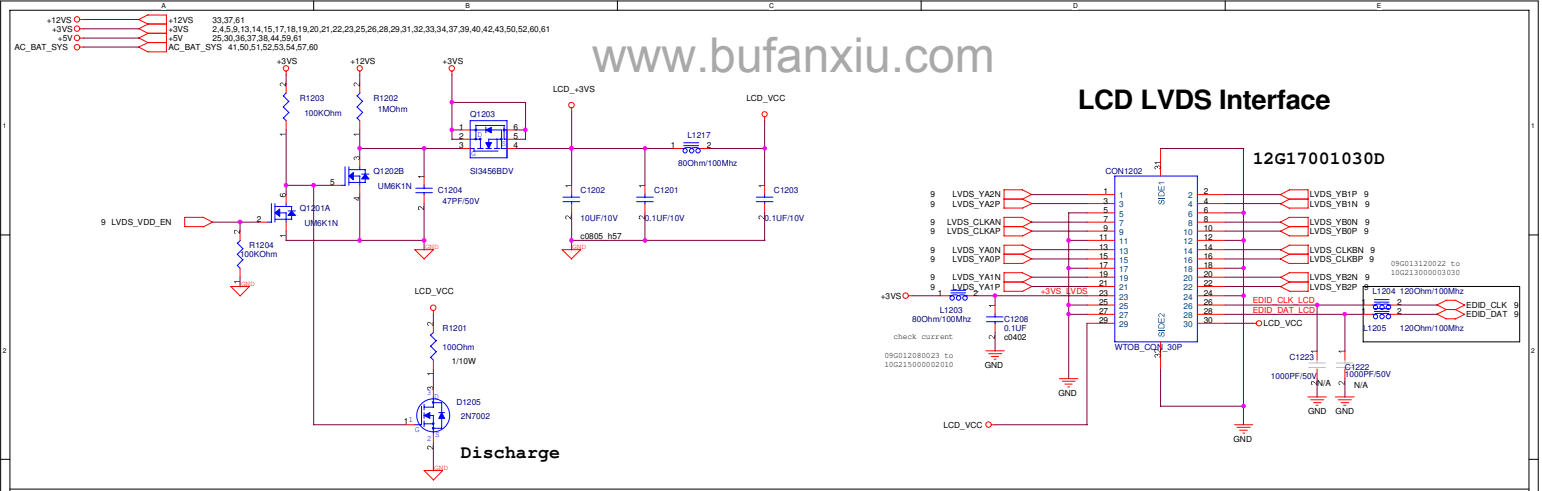
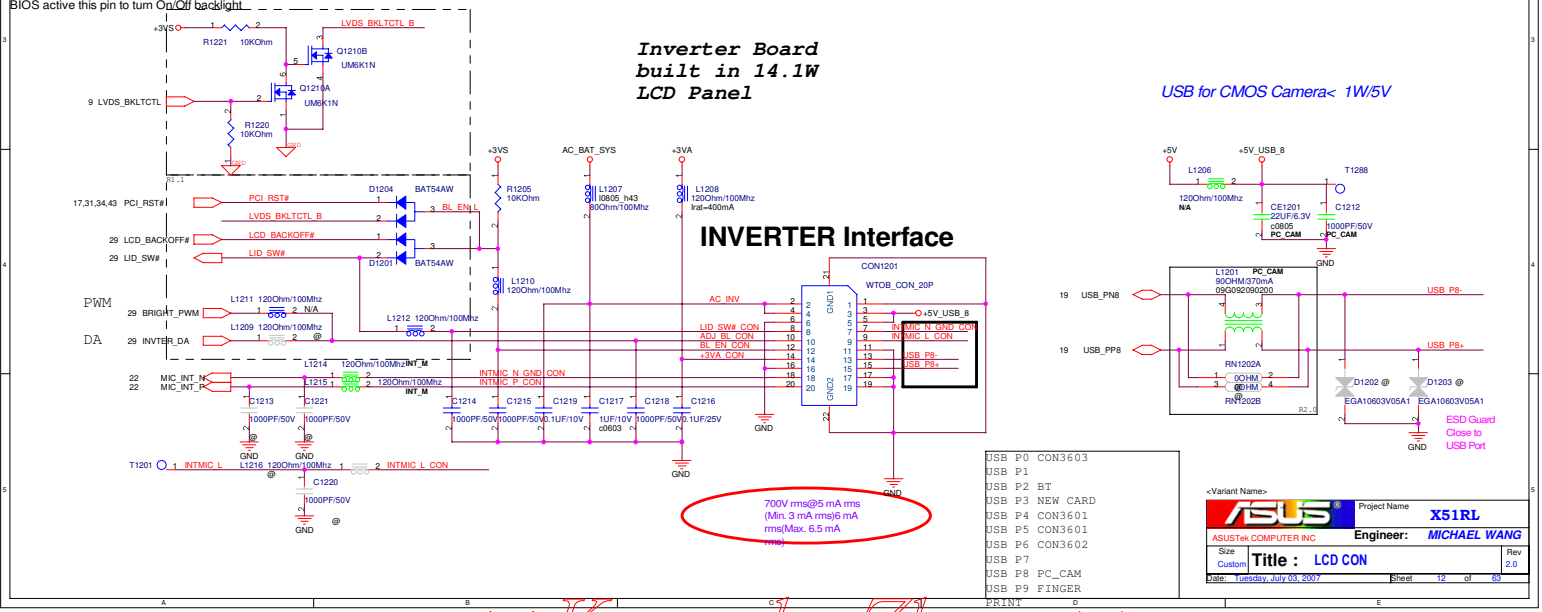


BIOS
LCD_BACKOFF#
When user push "Fn+F7" button
BIOS active this pin to turn On/Off backlight

LCD Backlight Control




```
USB P0 CON3603
USB P1
USB P2 BT
USB P3 NEW CARD
USB P4 CON3601
USB P5 CON3601
USB P6 CON3602
USB P7
USB P8 PC_CAM
USB P9 FINGER
PRINT
```

<Variant Name>

ASUSTek COMPUTER INC	Project Name	X51RL
	Engineer:	MICHAEL WANG
Size: Custom	Title : LCD CON	Rev: 2.0
Date: Tuesday, July 03, 2007	Sheet 12 of 63	

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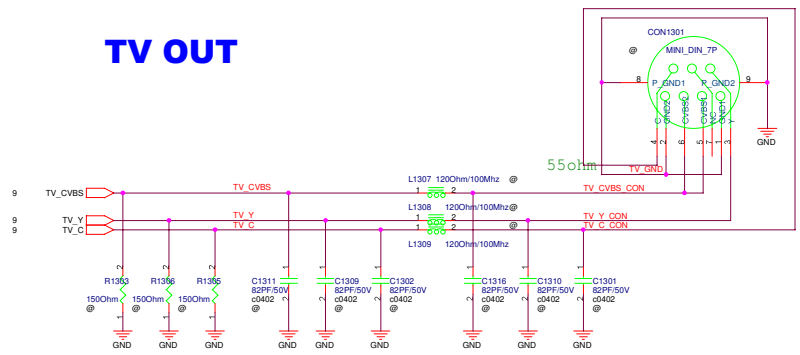
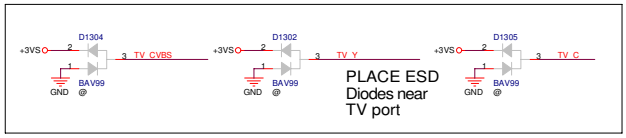
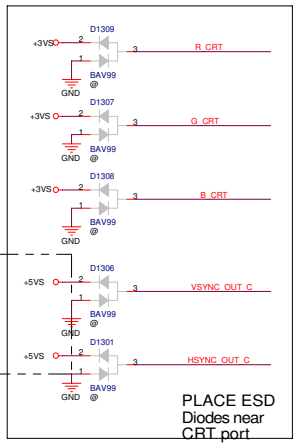
12G101102152
=>12G10110215A
R2.0

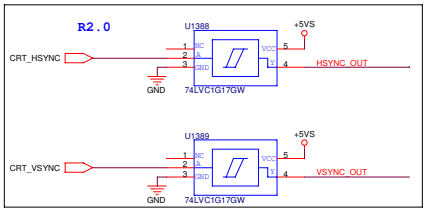
12G141011076

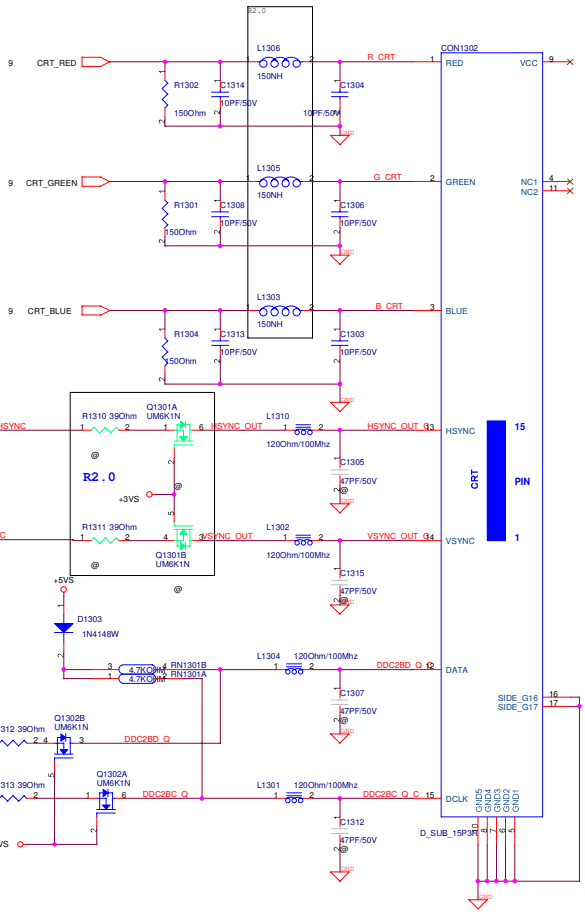
TV OUT











<Variant Name>

ASUSTek COMPUTER INC	Project Name	X51RL
	Engineer:	MICHAEL WANG
Size: Custom	Title : CRT PORT	Rev: 2.0
Date: Tuesday, July 03, 2007	Sheet 13 of 63	

<< Kennedy_Zhang >>

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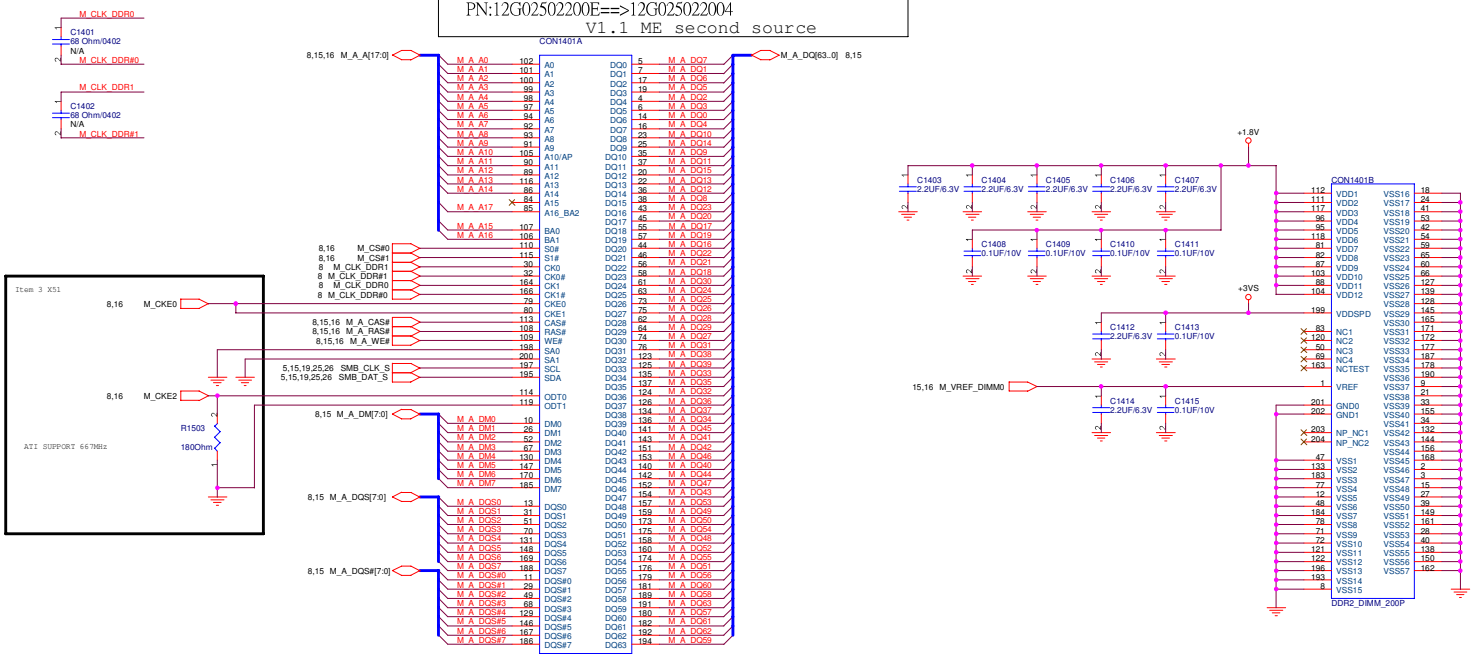
+3VS +1.8V → +3VS +1.8V 2,4,5,9,12,13,15,17,18,19,20,21,22,23,25,26,28,29,31,32,33,34,37,39,40,42,43,50,52,60,61 8,10,15,16,37,53

FRON

PN:12G02502200E==>12G025022004
V1.1 ME second source



<Variant Name>

ASUSTeK COMPUTER INC. NB1	Title : DDR2 SO-DIMM1		
	Engineer: MICHAEL WANG		
Size: Custom	Project Name: X51RL		Rev: 2.0
Date: Tuesday, July 03, 2007	Sheet 14 of 63		

<< Kennedy_Zhang >>

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+3VS
+1.8V
+3VS
+1.8V
2,4,5,9,12,13,14,17,18,19,20,21,22,23,25,26,28,29,31,32,33,34,37,39,40,42,43,50,52,60,61
8,10,14,16,37,53

PN:12G025C22000=>12G025C22004
V2.0 ME

M_CLK_DDR4
C1501
68Ohm/0402
N/A
M_CLK_DDR#4
M_CLK_DDR3
C1502
68Ohm/0402
N/A
M_CLK_DDR#3

CON1501A
DDR_DIMM_200P

8,14,16 M_A_A[17:0]
M_A_A0 102
M_A_A1 101
M_A_A2 100
M_A_A3 99
M_A_A4 98
M_A_A5 97
M_A_A6 94
M_A_A7 92
M_A_A8 93
M_A_A9 91
M_A_A10 105
M_A_A11 90
M_A_A12 89
M_A_A13 116
M_A_A14 86
M_A_A15 85
M_A_A16 107
M_A_A17 84
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10/AP A11 A12 A13 A14 A15 A16_BA2 BA0 BA1 S0# S1# CK0 CK0# CK1 CK1# CKE0 CKE1 CAS# RAS# WE# SA0 SA1 SCL SDA ODT0 ODT1

8,16 M_CS#2
8,16 M_CS#3
8 M_CLK_DDR3
8 M_CLK_DDR#3
8 M_CLK_DDR4
8 M_CLK_DDR#4
8,14,16 M_A_CAS#
8,14,16 M_A_RAS#
8,14,16 M_A_WE#
5,14,19,25,26 SMB_CLK_S
5,14,19,25,26 SMB_DAT_S

8,14 M_A_DM[7:0]
M_A_DM0 10
M_A_DM1 26
M_A_DM2 52
M_A_DM3 67
M_A_DM4 130
M_A_DM5 147
M_A_DM6 170
M_A_DM7 185
DM0 DM1 DM2 DM3 DM4 DM5 DM6 DM7

8,14 M_A_DQS[7:0]
M_A_DQS0 13
M_A_DQS1 31
M_A_DQS2 51
M_A_DQS3 70
M_A_DQS4 131
M_A_DQS5 148
M_A_DQS6 169
M_A_DQS7 188
DQS0 DQS1 DQS2 DQS3 DQS4 DQS5 DQS6 DQS7

8,14 M_A_DQS#[7:0]
M_A_DQS#0 11
M_A_DQS#1 29
M_A_DQS#2 49
M_A_DQS#3 68
M_A_DQS#4 129
M_A_DQS#5 146
M_A_DQS#6 167
M_A_DQS#7 186
DQS#0 DQS#1 DQS#2 DQS#3 DQS#4 DQS#5 DQS#6 DQS#7

M_A_DQ[63..0] 8,14
M_A_DQ0 5
M_A_DQ1 7
M_A_DQ2 17
M_A_DQ3 19
M_A_DQ4 4
M_A_DQ5 6
M_A_DQ6 14
M_A_DQ7 16
M_A_DQ8 23
M_A_DQ9 25
M_A_DQ10 35
M_A_DQ11 37
M_A_DQ12 20
M_A_DQ13 22
M_A_DQ14 36
M_A_DQ15 38
M_A_DQ16 43
M_A_DQ17 45
M_A_DQ18 55
M_A_DQ19 57
M_A_DQ20 44
M_A_DQ21 46
M_A_DQ22 56
M_A_DQ23 58
M_A_DQ24 61
M_A_DQ25 63
M_A_DQ26 73
M_A_DQ27 75
M_A_DQ28 62
M_A_DQ29 64
M_A_DQ30 74
M_A_DQ31 76
M_A_DQ32 123
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M_A_DQ58 189
M_A_DQ59 191
M_A_DQ60 180
M_A_DQ61 182
M_A_DQ62 192
M_A_DQ63 194

+3VS
R1501 10KOhm
8,16 M_CKE1
8,16 M_CKE3
R1502 180Ohm
ATI SUPPORT 667MHz

+1.8V
C1503 2.2UF/6.3V
C1504 2.2UF/6.3V
C1505 2.2UF/6.3V
C1506 2.2UF/6.3V
C1507 2.2UF/6.3V
C1508 0.1UF/10V
C1509 0.1UF/10V
C1510 0.1UF/10V
C1511 0.1UF/10V
+3VS
C1512 2.2UF/6.3V
C1513 0.1UF/10V
14,16 M_VREF_DIMM1
C1514 2.2UF/6.3V
C1515 0.1UF/10V

CON1501B
DDR_DIMM_200P
VDD1 VDD2 VDD3 VDD4 VDD5 VDD6 VDD7 VDD8 VDD9 VDD10 VDD11 VDD12 VDDSPD
NC1 NC2 NC3 NC4 NCTEST
VREF
GND0 GND1
NP_NC1 NP_NC2
VSS1 VSS2 VSS3 VSS4 VSS5 VSS6 VSS7 VSS8 VSS9 VSS10 VSS11 VSS12 VSS13 VSS14 VSS15 VSS16 VSS17 VSS18 VSS19 VSS20 VSS21 VSS22 VSS23 VSS24 VSS25 VSS26 VSS27 VSS28 VSS29 VSS30 VSS31 VSS32 VSS33 VSS34 VSS35 VSS36 VSS37 VSS38 VSS39 VSS40 VSS41 VSS42 VSS43 VSS44 VSS45 VSS46 VSS47 VSS48 VSS49 VSS50 VSS51 VSS52 VSS53 VSS54 VSS55 VSS56 VSS57

<Variant Name>

ASUSTeK COMPUTER INC. NB1	Title : DDR2 SO-DIMM1		
	Engineer: MICHAEL WANG		
Size: Custom	Project Name: X51RL		Rev: 2.0
Date: Tuesday, July 03, 2007	Sheet 15 of 63		

<< Kennedy_Zhang >>

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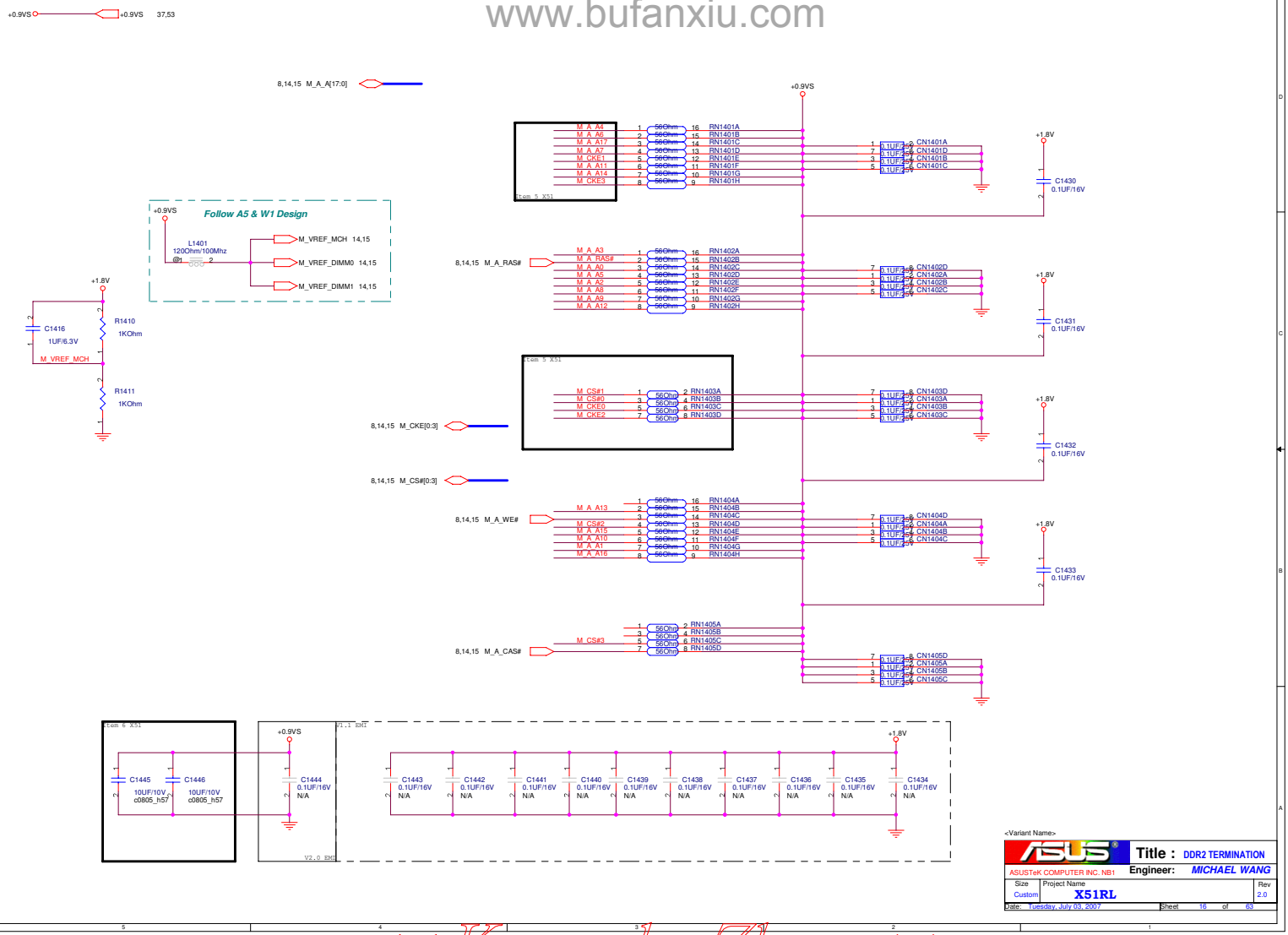

<Variant Name>

ASUSTeK COMPUTER INC. NB1	Title : DDR2 TERMINATION	
	Engineer: MICHAEL WANG	
Size: Custom	Project Name: X51RL	Rev: 2.0
Date: Tuesday, July 03, 2007	Sheet 16 of 63	

<< Kennedy_Zhang >>

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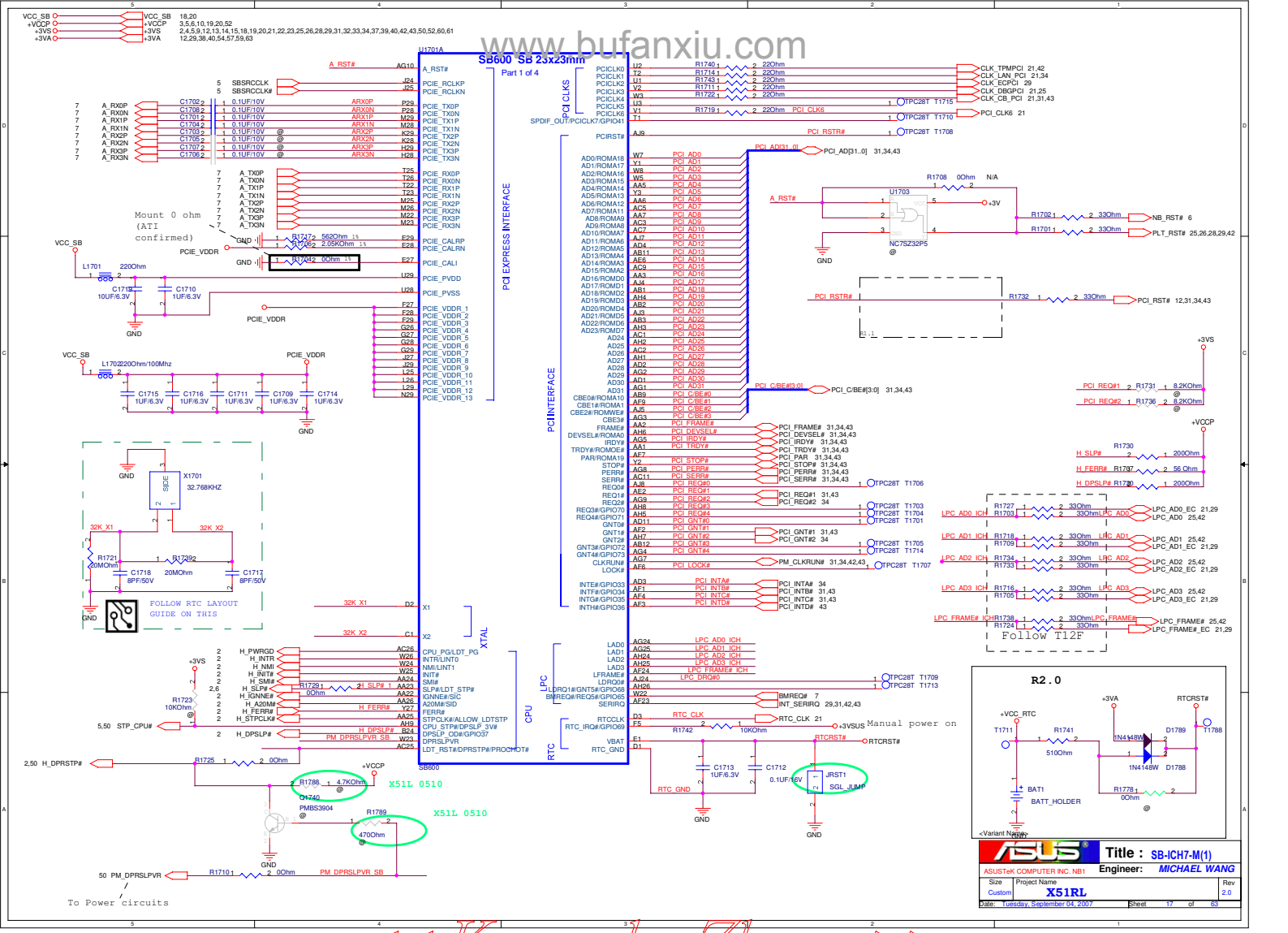

Title :	SB-ICH7-M(1)
ASUSTeK COMPUTER INC. NB1	Engineer: MICHAEL WANG
Size: Custom	Project Name: X51RL
Rev: 2.0	
Date: Tuesday, September 04, 2007	Sheet 17 of 63

<< Kennedy_Zhang >>

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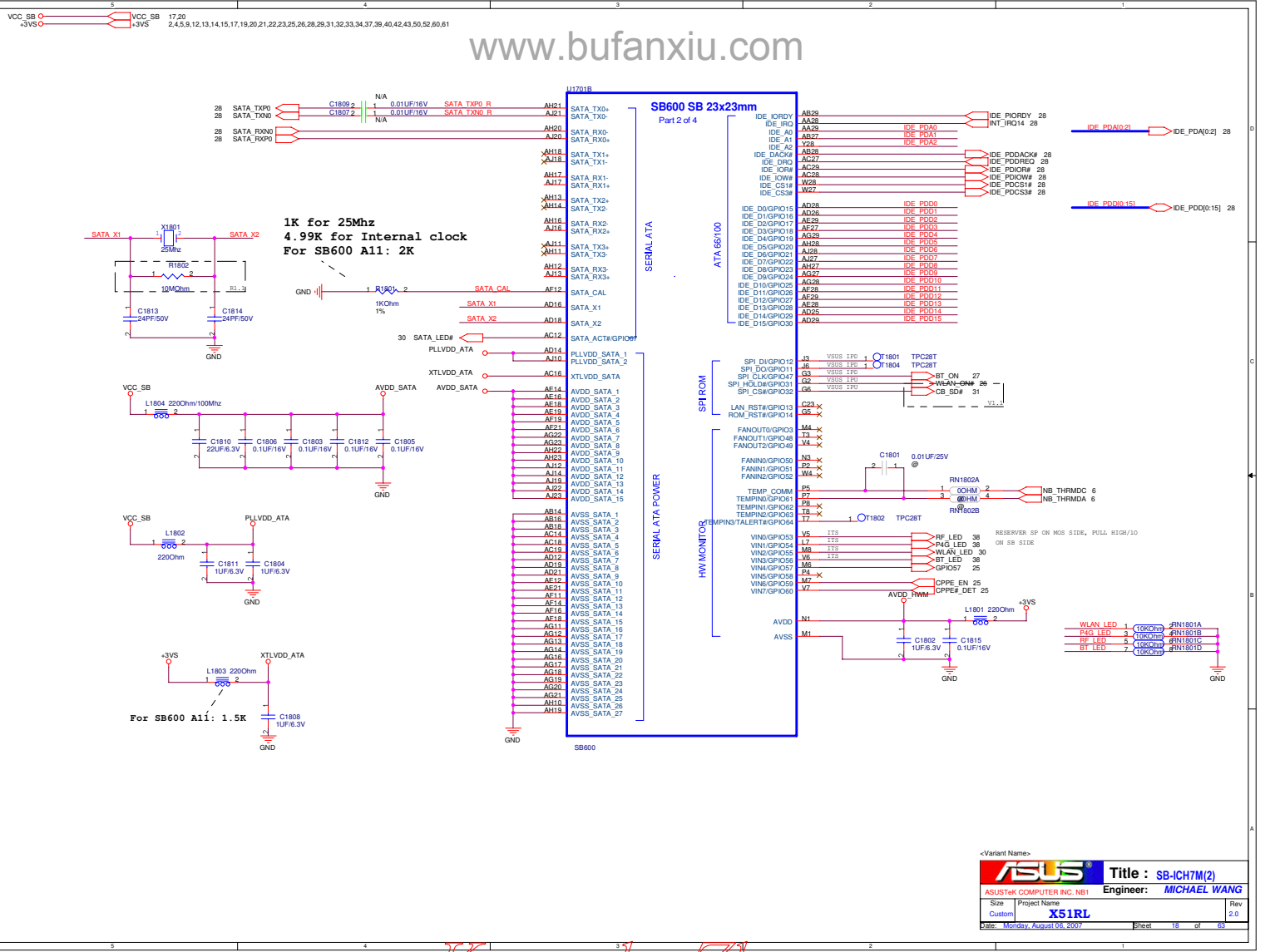

<< Kennedy_Zhang >>

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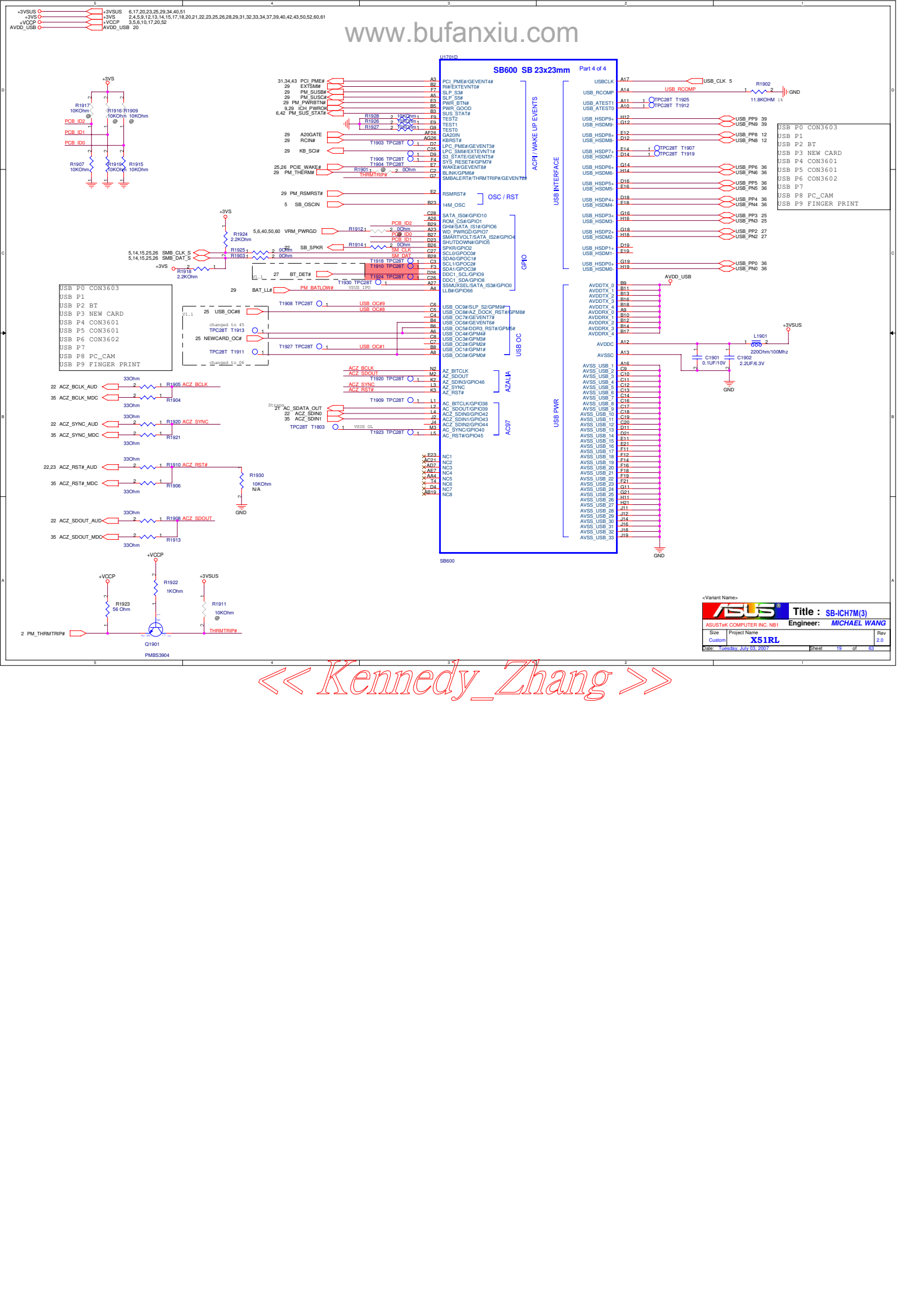

<< Kennedy_Zhang >>

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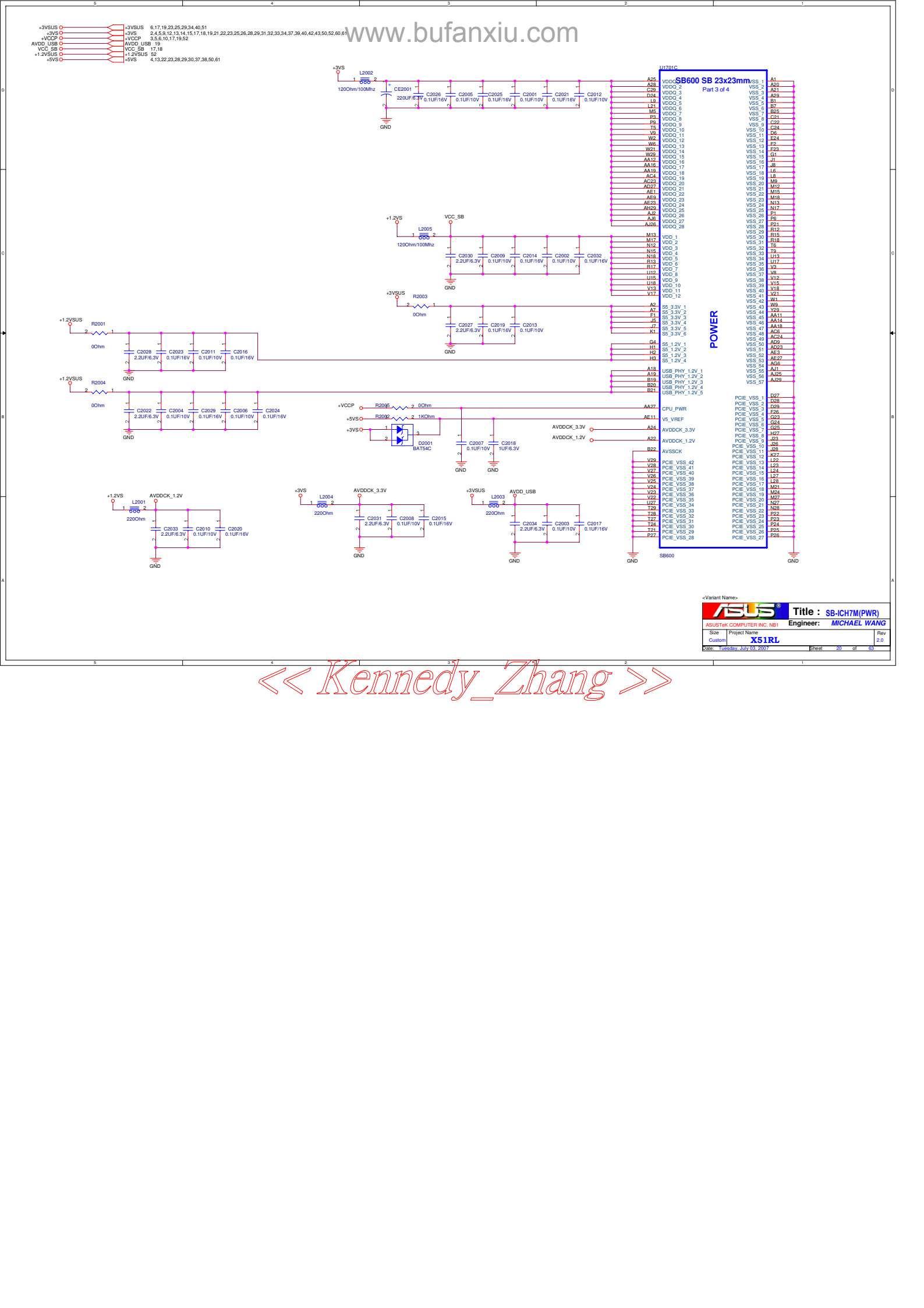

<Variant Name>

Title : SB-ICH7M(PWR)		
ASUSTeK COMPUTER INC. NB1	Engineer: MICHAEL WANG	
Size: Custom	Project Name: X51RL	Rev: 2.0
Date: Tuesday, July 03, 2007	Sheet 20 of 63	

<< Kennedy_Zhang >>

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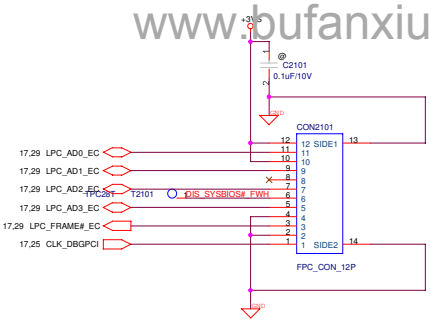
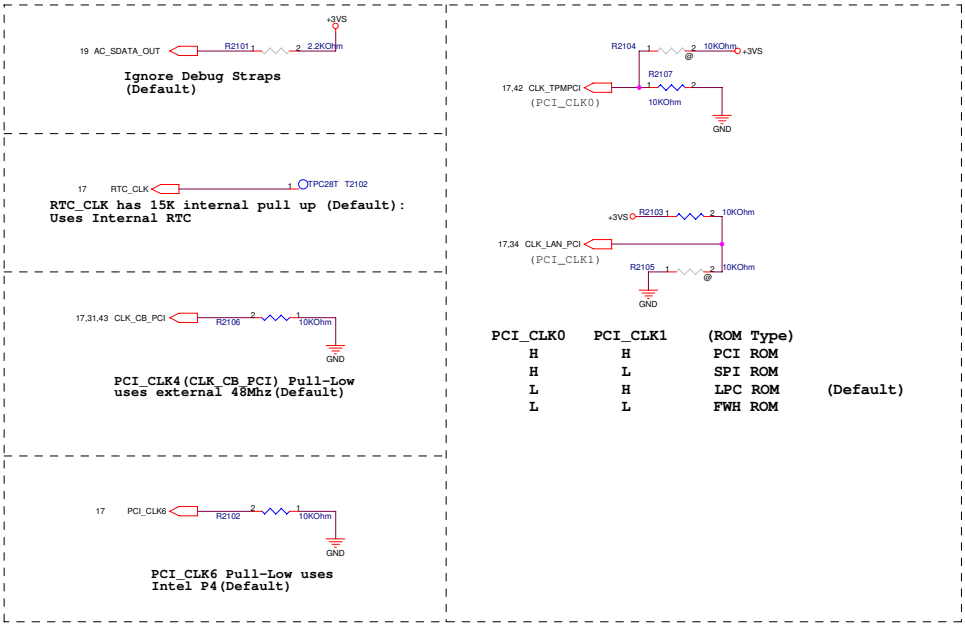




PCI_CLK0	PCI_CLK1	(ROM Type)	
H	H	PCI ROM	
H	L	SPI ROM	
L	H	LPC ROM	(Default)
L	L	FWH ROM	

<Variant Name>

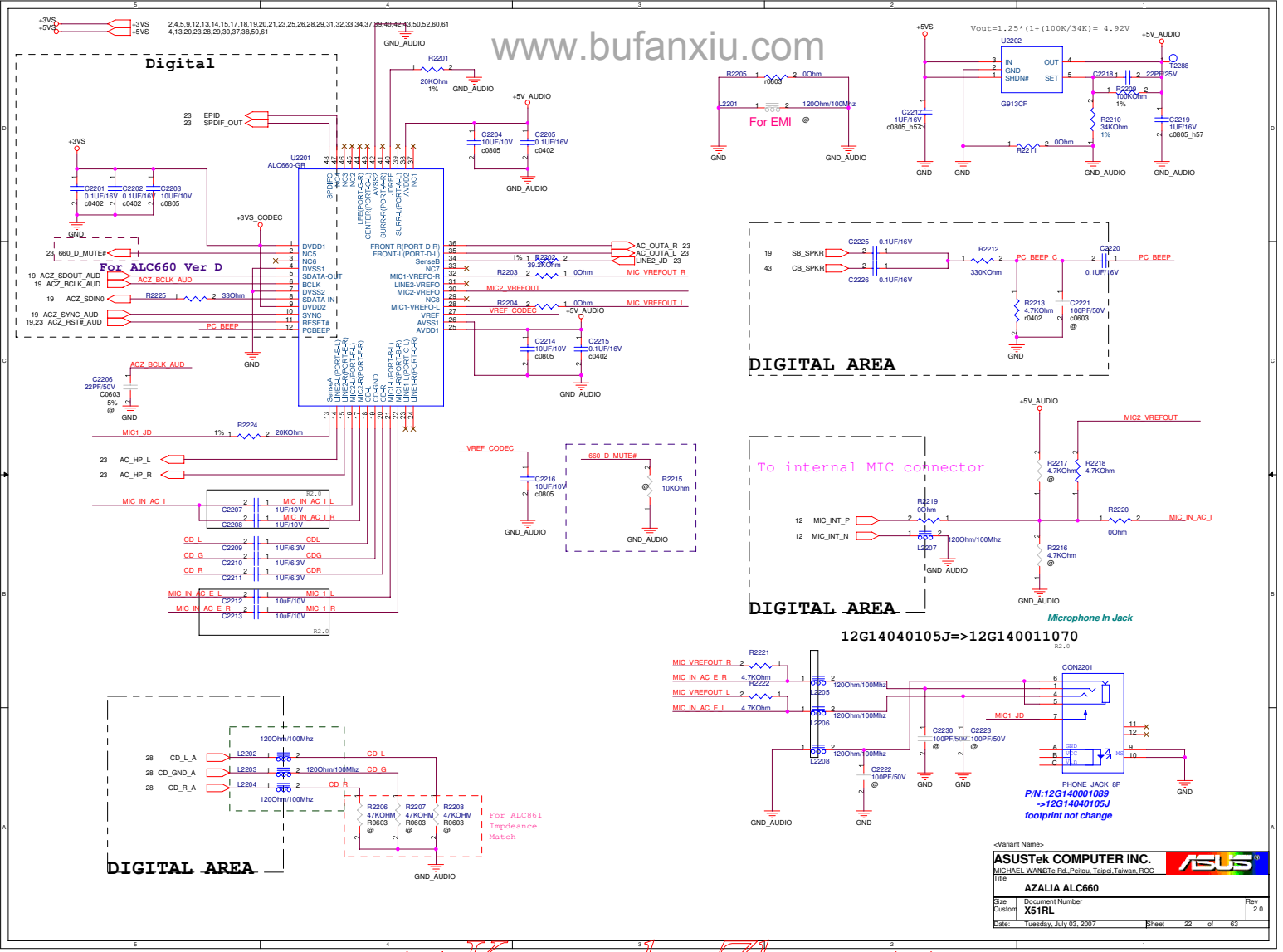
Title : BLOCK DIAGRAM

<OrgName> Engineer:

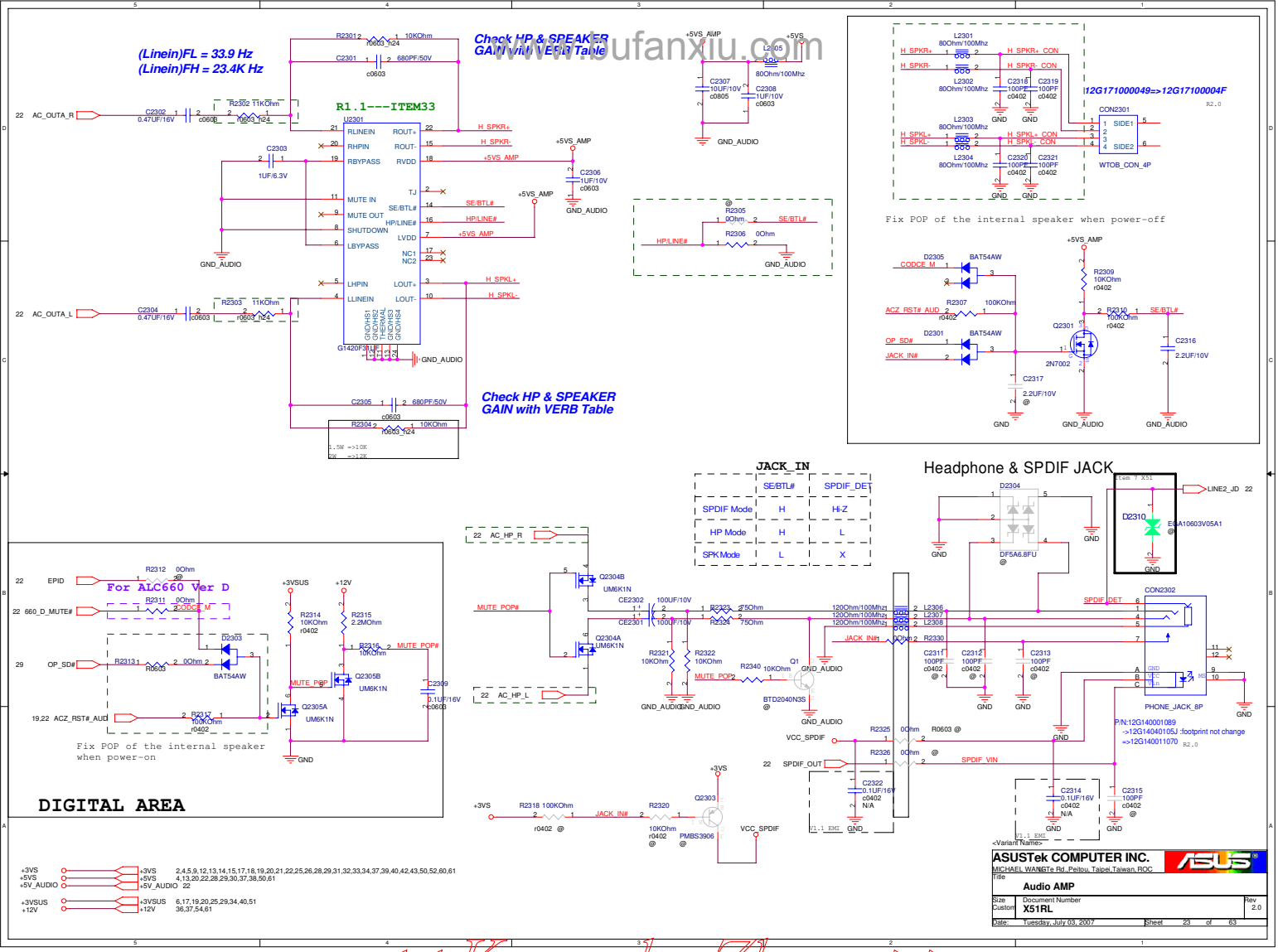
Size	Project Name	Rev
Custom	X51RL	2.0

Date: Tuesday, July 03, 2007 Sheet 21 of 63

<< Kennedy_Zhang >>



<< Kennedy_Zhang >>



<< Kennedy_Zhang >>

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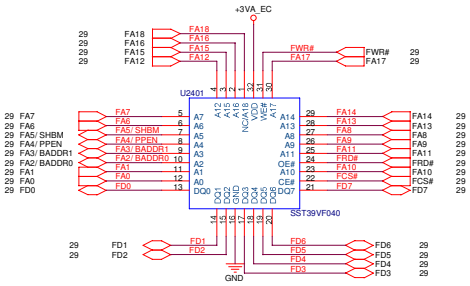
+3VA_EC +3VA_EC 26,29

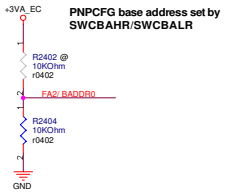
ISA ROM

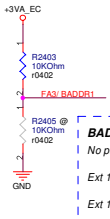
0.01A



EC Hardware Strap

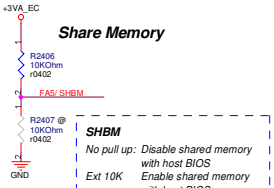
Strap value sampled after VSTBY power up reset





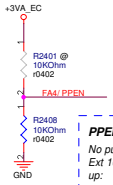
BADDR[1:0]

No pull up:	*The register pair to access PNPCFG is 002Eh and 002Fh.*
Ext 10K up on BADDR0:	*The register pair to access PNPCFG is 004Eh and 004Fh.*
Ext 10K up on BADDR1:	*The register pair to access PNPCFG is determined by EC domain registers SWCBALR and SWCBAHR.*



SHBM

No pull up:	*Disable shared memory with host BIOS*
Ext 10K up:	*Enable shared memory with host BIOS*



PPEN

No pull up:	*Normal*
Ext 10K up:	*KBS interface pins are switched to parallel port interface for in-system programming.*

<Variant Name>

ASUSTeK COMPUTER INC

Title : ISA ROM

Engineer: MICHAEL WANG

Size	Project Name	Rev
Custom	X51RL	2.0

Date: Tuesday, July 03, 2007 Sheet 24 of 63

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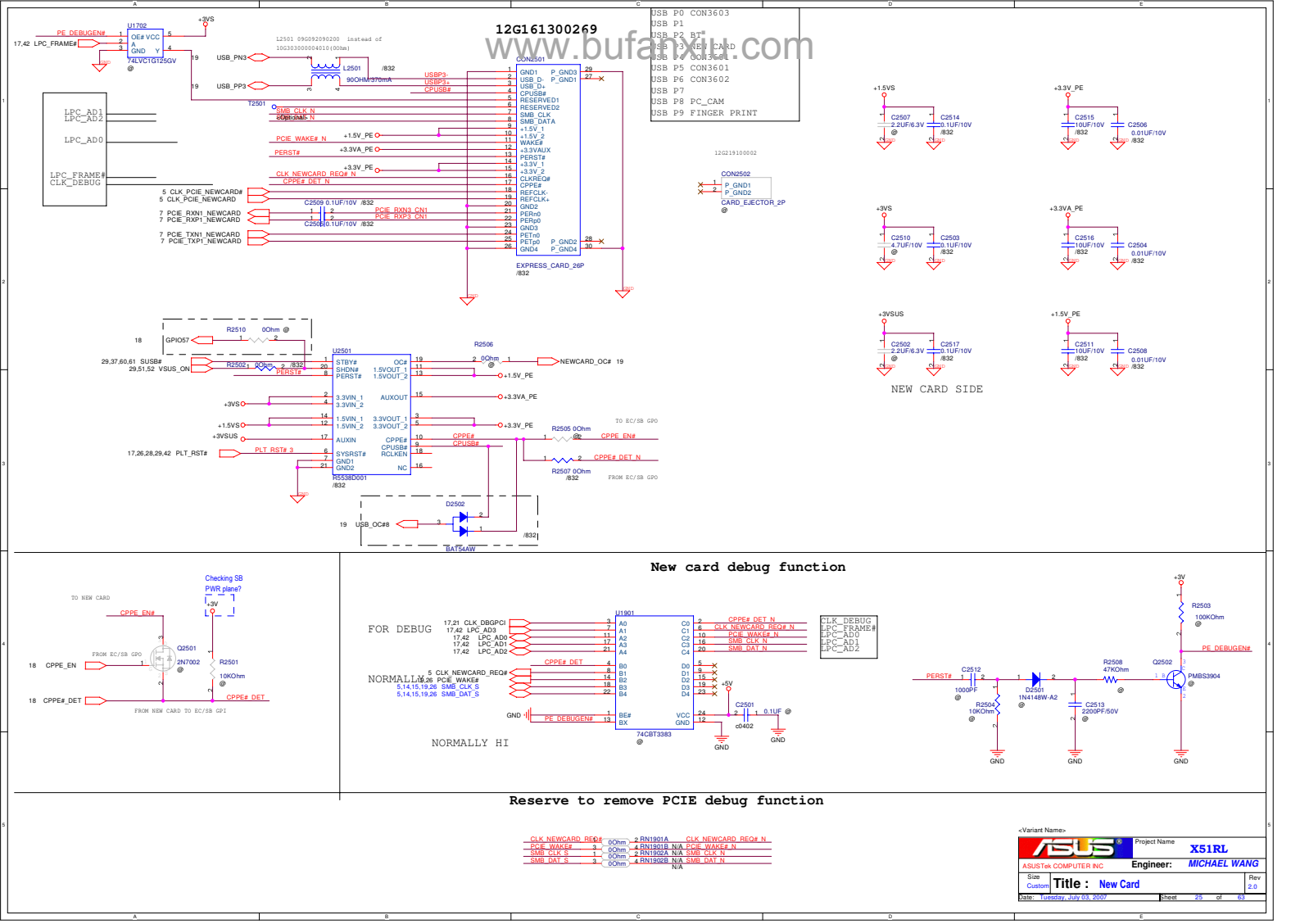

New card debug function

Reserve to remove PCIE debug function

<Variant Name>

Project Name	X51RL
ASUSTek COMPUTER INC	Engineer: MICHAEL WANG
Size: Custom	Title : New Card
Rev	2.0
Date: Tuesday, July 03, 2007	Sheet 25 of 63

<< Kennedy_Zhang >>

+3V +3V 17,25,27,31,35,37,42,43,44,61
+3VS +3VS 2,4,5,9,12,13,14,15,17,18,19,20,21,22,23,25,28,29,31,32,33,34,37,39,40,42,43,50,52,60,61
+1.5VS +1.5VS 25,37,54
+3VA_EC +3VA_EC 24,29

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12G030000526

CLKREQ#(output) CLOCK REQUEST could be pull low

CON2602
MINI_CARD_LATCH_52P

19,25 PCIE_WAKE#	1	WAKE#	3.3V_1 2
27 CH_DATA	3	Reserved1	GND7 4
27 CH_CLK	5	Reserved2	1.5V_1 6
5 CLK_MINICARD_REQ#	7	CLKREQ#	UIM_PWR 8
	9	GND1	UIM_DATA 10
5 CLK_PCIE_MINICARD#	11	REFCLK-	UIM_CLK 12
5 CLK_PCIE_MINICARD	13	REFCLK+	UIM_RESET 14
	15	GND2	UIM_VPP 16
	17	Reserved/UIM_C8	GND8 18
	19	Reserved/UIM_C4/W_DISABLE#	20
	21	GND3	PERST# 22
7 PCIE_RXN0_MINICARD	23	PERn0	+3.3Vaux 24
7 PCIE_RXP0_MINICARD	25	PERp0	GND9 26
	27	GND4	1.5V_2 28
	29	GND5	SMB_CLK 30
7 PCIE_TXN0_MINICARD	31	PETn0	SMB_DATA 32
7 PCIE_TXP0_MINICARD	33	PETp0	GND10 34
	35	GND6	USB_D- 36
	37	Reserved3	USB_D+ 38
	39	Reserved4	GND11 40
	41	Reserved5	LED_WWAN# 42
	43	Reserved6	LED_WLAN# 44
	45	Reserved7	LED_WPAN# 46
	47	Reserved8	1.5V_3 48
	49	Reserved9	GND12 50
	51	Reserved10	3.3V_2 52
	53	GND13	NP_NC2 56
	54	GND14	NP_NC1 55

+3VS
C2602 0.1UF/10V GND
C2605 0.1UF/10V GND
C2606 10UF/6.3V GND
3.003V~3.597V
Max= 750 mA

+1.5VS
C2608 0.1UF/10V GND
C2601 0.1UF/10V GND
C2603 10UF/6.3V GND
1.425V~1.575V
Max= 375 mA

+3V
C2607 0.1UF/10V GND
C2604 1UF/6.3V GND
3.003V~3.597V
Max= 250 mA

WIRELESS_LAN_ON/OFF# → PLT_RST# 17,25,28,29,42

R2603 0Ohm @ SMB_CLK_S 5,14,15,19,25
R2601 0Ohm @ SMB_DAT_S 5,14,15,19,25

WL_LED# → T260TPC28t

CON2601
MINI_PCI_LATCH_5P
MINI_PCI-E LATCH 5P
GND

12G162210052

+3VA_EC
PULL HIGH ON SB SIDE AND IT INTERNAL PULL HIGH
INTERNAL PU
R2602 47KOhm @
WIRELESS_LAN_ON/OFF#
18 WLAN_ON#
Q2601 2N7002
GND

<Variant Name>

Project Name	X51RL
ASUSTek COMPUTER INC	Engineer: MICHAEL WANG
Size: Custom	Title : MINI PCI
Rev	2.0
Date: Tuesday, July 03, 2007	Sheet 26 of 63

<< Kennedy_Zhang >>

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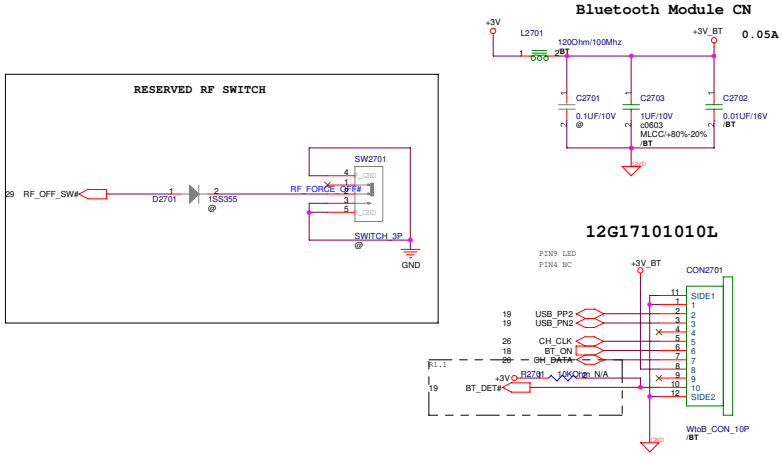
+3V +3V 17,25,26,31,35,37,42,43,44,61

For Bluetooth

Bluetooth Module CN




```
USB P0 CON3603
USB P1
USB P2 BT
USB P3 NEW CARD
USB P4 CON3601
USB P5 CON3601
USB P6 CON3602
USB P7
USB P8 PC_CAM
USB P9 FINGER
PRINT
```

<Variant Name>

ASUSTeK COMPUTER INC	Title : Blue Tooth	
	Engineer: MICHAEL WANG	
Size: Custom	Project Name: X51RL	Rev: 2.0
Date: Tuesday, July 03, 2007	Sheet 27 of 63	

<< Kennedy_Zhang >>

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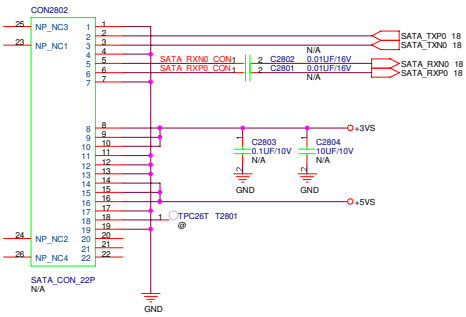
+3VS
+5VS

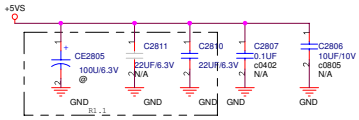
+3VS
+5VS

2,4,5,9,12,13,14,15,17,18,19,20,21,22,23,25,26,29,31,32,33,34,37,39,40,42,43,50,52,60,61
4,13,20,22,23,29,30,37,38,50,61

SATA HDD

12G15100022F



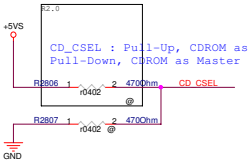


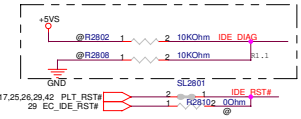
Item 8 X51

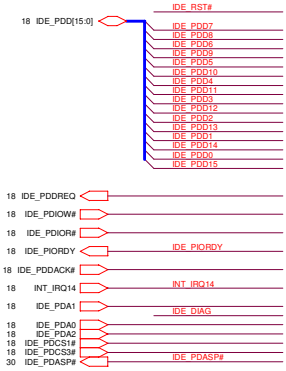
Dtlete PATA HDD

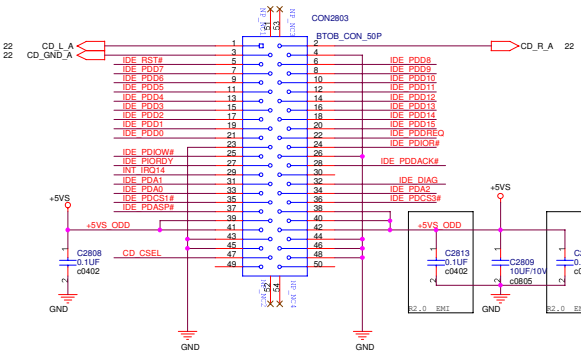
CD-ROM

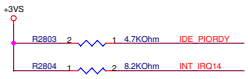
12G161210504











<Variant Name>

ASUSTeK COMPUTER INC. NB1	Title : PATA-SATA & ODD	
	Engineer:	
Size: Custom	Project Name: X51RL	Rev: 2.0
Date: Monday, August 06, 2007	Sheet 28 of 63	

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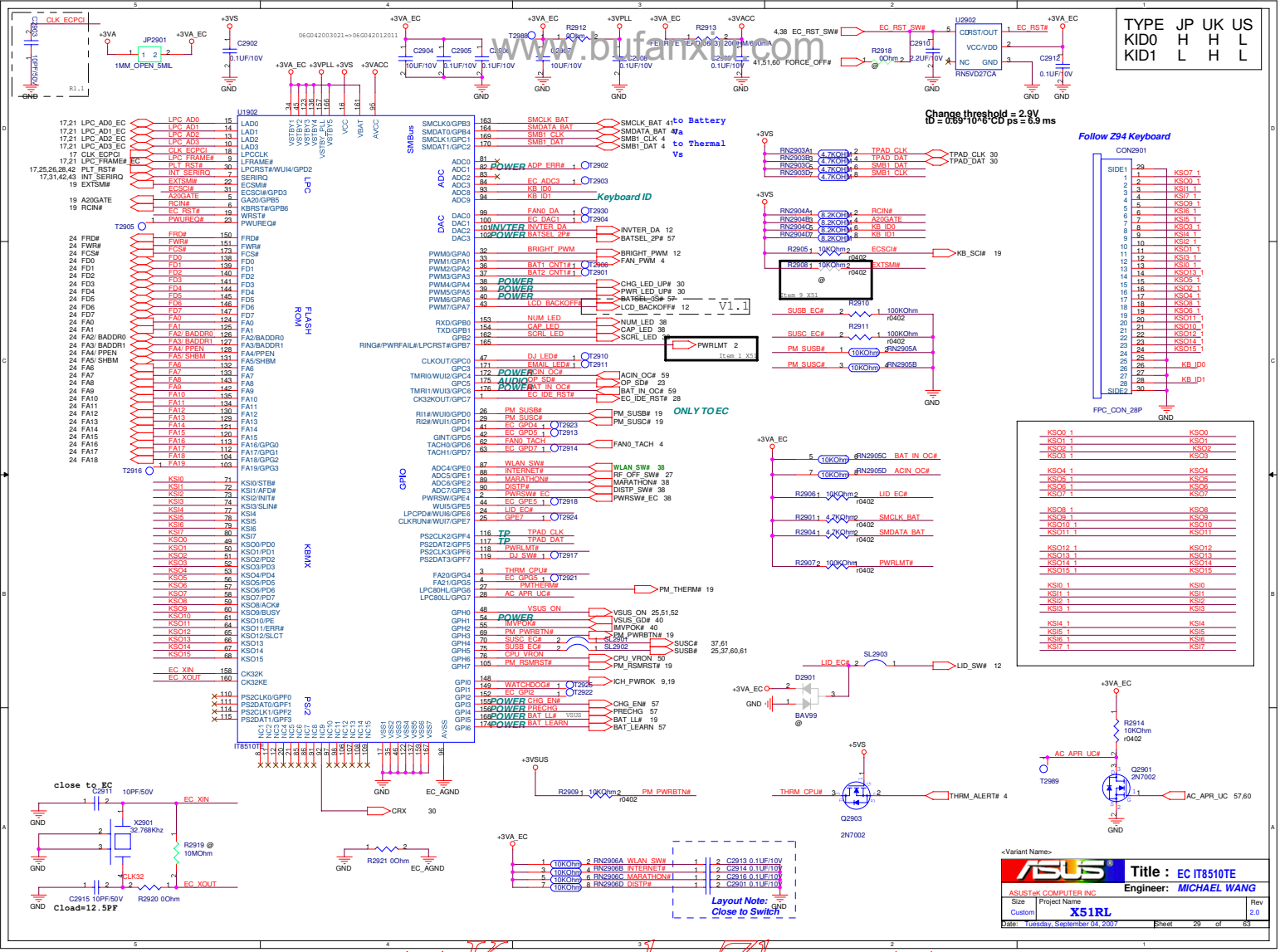

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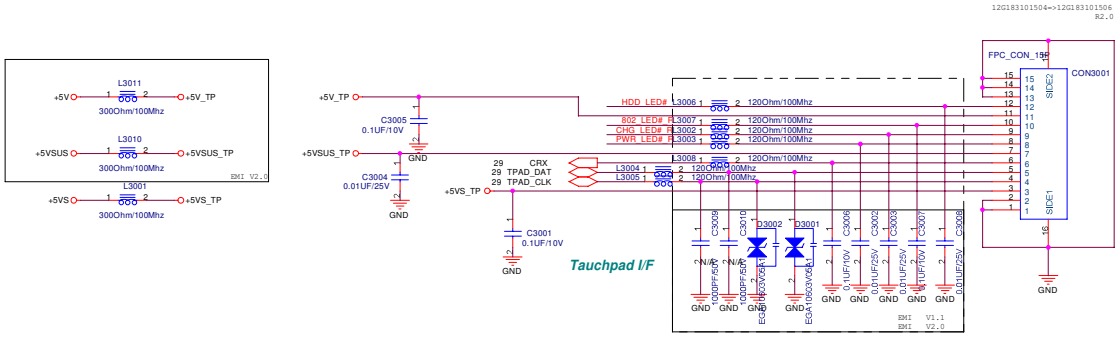
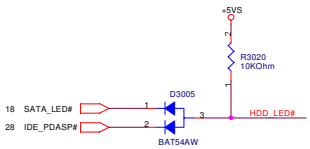
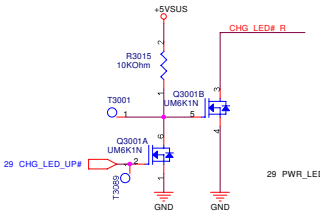


Touchpad

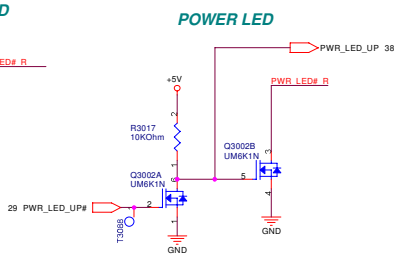
HDD LED



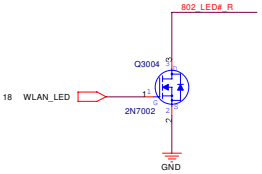
CHARGE LED



POWER LED



WLAN LED



<Variant Name>

ASUSTeK COMPUTER INC

Title : EC IT8510TE(2/2)

Engineer: MICHAEL WANG

Size	Project Name	Rev
A3	X51RL	2.0

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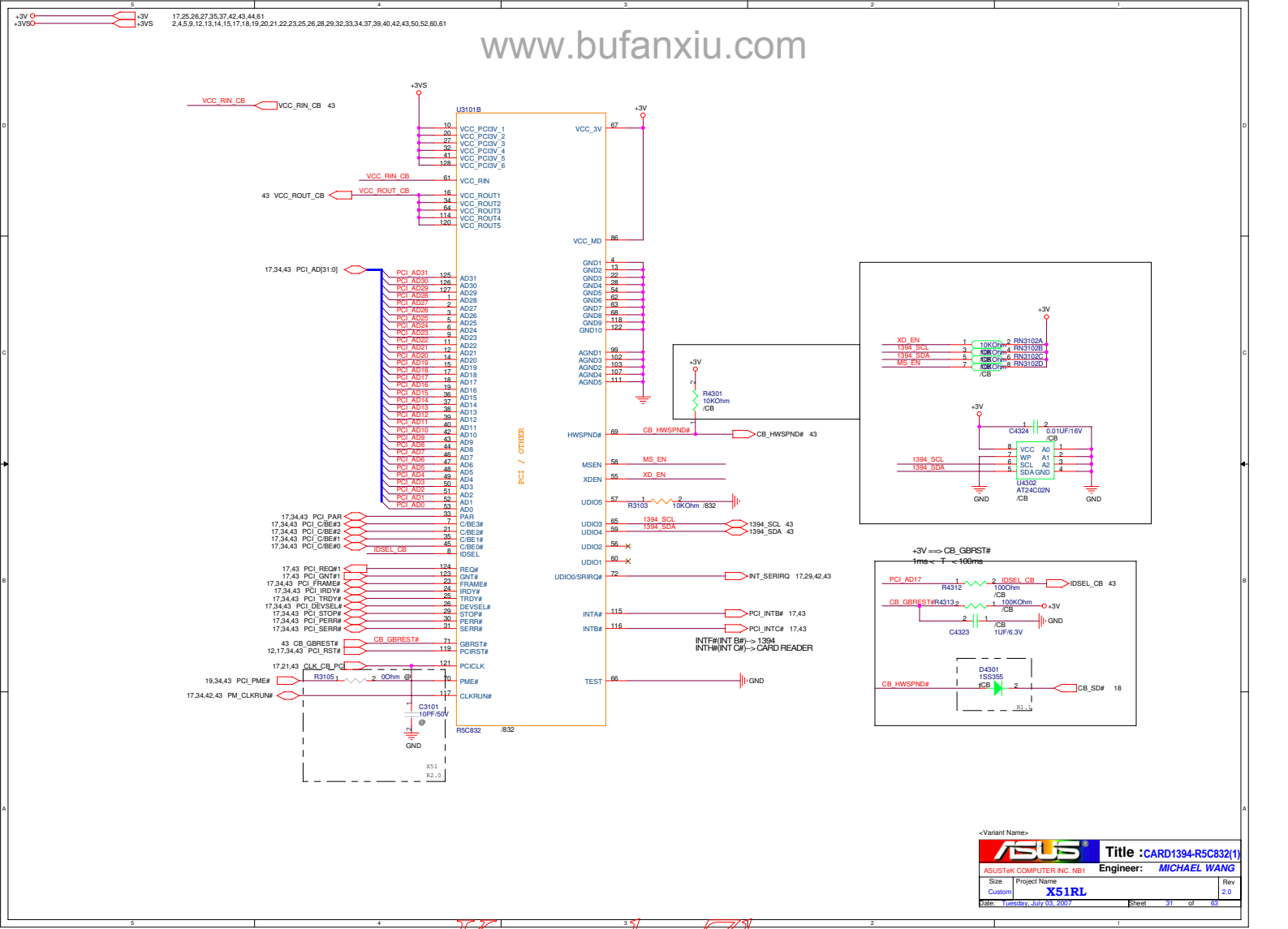

<Variant Name>

Title :	CARD1394-R5C832(1)
ASUSTeK COMPUTER INC. NB1	Engineer: MICHAEL WANG
Size: Custom	Project Name: X51RL
Rev: 2.0	
Date: Tuesday, July 03, 2007	Sheet 31 of 63

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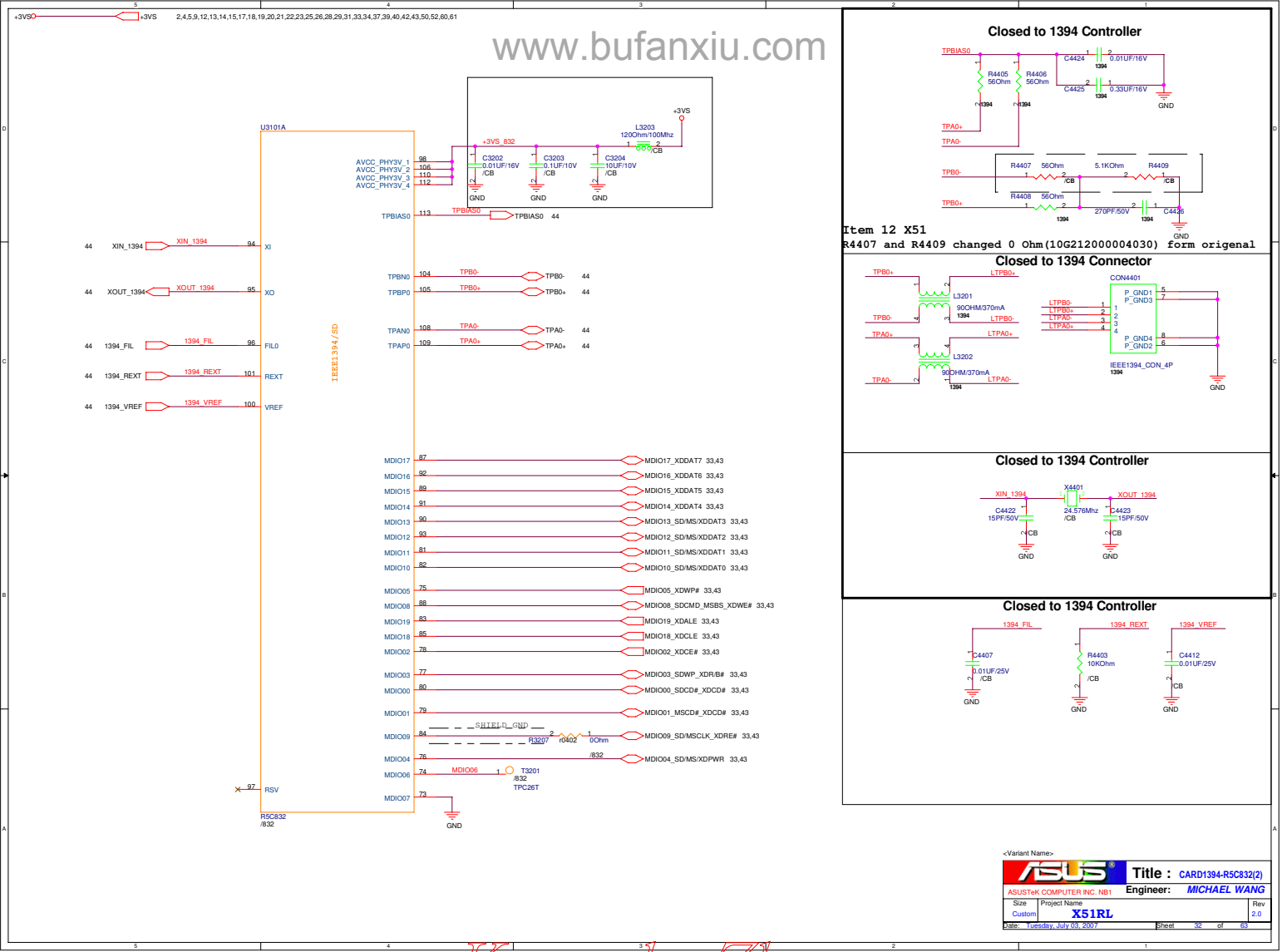

Closed to 1394 Controller

Item 12 X51
R4407 and R4409 changed 0 Ohm(10G212000004030) form origenal

Closed to 1394 Connector

Closed to 1394 Controller

Closed to 1394 Controller

<Variant Name>

ASUSTeK COMPUTER INC. NB1	Title : CARD1394-R5C832(2)	
	Engineer: MICHAEL WANG	
Size: Custom	Project Name: X51RL	Rev: 2.0
Date: Tuesday, July 03, 2007	Sheet 32 of 63	

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Name	Drive	Name	Drive
MDIO00	I - PU	MDIO10	I/O - PU
MDIO01	I - PU	MDIO11	I/O - PU
MDIO02	O - PU	MDIO12	I/O - PU
MDIO03	I - PU	MDIO13	I/O - PU
MDIO04	O - 3V	MDIO14	I/O - PU
MDIO05	O - 3V	MDIO15	I/O - PU
MDIO06	O - 3V	MDIO16	I/O - PU
MDIO07	I - 3V	MDIO17	I/O - PU
MDIO08	I/O - PU	MDIO18	I/O - PU
MDIO09	I/O - PU	MDIO19	I/O - PU

MDIO000--> SD Card Detect
MDIO001--> MS Card Detect
MDIO003--> SD Write Protect
MDIO004--> SD Card Power0 Control/ MS Power Control
MDIO008--> SD Command/MS Bus State
MDIO009--> SD Clock/MS Clock
MDIO010--> SD Data 0/MS Data 0
MDIO011--> SD Data 1/MS Data 1
MDIO012--> SD Data 2/MS Data 2
MDIO013--> SD Data 3/MS Data 3

MDIO002--> xDCE#
MDIO005--> SD Power Control 1 (xDWP
MDIO006--> xD/MS/MD Ctrl Contro
MDIO014--> xD Data
MDIO015--> xD Data
MDIO016--> xD Data
MDIO017--> xD Data
MDIO018--> xD CLE
MDIO019--> xD ALE

SD/MMC/MS/MS-PRO Card Reader Socket

32,43 MDIO17_XDDAT7 — MDIO17_XDDAT7
32,43 MDIO16_XDDAT6 — MDIO16_XDDAT6
32,43 MDIO15_XDDAT5 — MDIO15_XDDAT5
32,43 MDIO14_XDDAT4 — MDIO14_XDDAT4
32,43 MDIO13_SD/MS/XDDAT3 — MDIO13_SD/MS/XDDAT3
32,43 MDIO12_SD/MS/XDDAT2 — MDIO12_SD/MS/XDDAT2
32,43 MDIO11_SD/MS/XDDAT1 — MDIO11_SD/MS/XDDAT1
32,43 MDIO10_SD/MS/XDDAT0 — MDIO10_SD/MS/XDDAT0

32,43 MDIO05_XDWP# — MDIO05_XDWP#
32,43 MDIO08_SDCMD_MSBS_XDWE# — MDIO08_SDCMD_MSBS_XDWE#
32,43 MDIO19_XDALE — MDIO19_XDALE
32,43 MDIO18_XDCLE — MDIO18_XDCLE
32,43 MDIO02_XDCE# — MDIO02_XDCE#

32,43 MDIO03_SDWP_XDR/B# — MDIO03_SDWP_XDR/B#
32,43 MDIO00_SDCD#_XDCD# — MDIO00_SDCD#_XDCD#
32,43 MDIO01_MSCD#_XDCD# — MDIO01_MSCD#_XDCD#
32,43 MDIO09_SD/MSCLK_XDRE# — MDIO09_SD/MSCLK_XDRE#

12G340004402

+VCCCA
C3304 270P @
CON3301
MDIO08_SDCMD_MSBS_XDWE#
MDIO11_SD/MS/XDDAT1
MDIO10_SD/MS/XDDAT0
MDIO12_SD/MS/XDDAT2
MSCD#
MDIO13_SD/MS/XDDAT3
MDIO09_SD/MSCLK_XDRE#
SD_DAT2
MDIO13_SD/MS/XDDAT3
MDIO08_SDCMD_MSBS_XDWE#
MDIO09_SD/MSCLK_XDRE#
MDIO10_SD/MS/XDDAT0
SD_DAT1
SDCD#
C3305 270P @

1	MS_GND1	XD_CD	23
2	MS_BS	XD_GND1	24
3	MS_DATA1	XD_R/B	25
4	MS_DATA0	XD_RE	26
5	MS_DATA2	XD_CE	27
6	MS_INS	XD_CLE	28
7	MS_DATA3	XD_ALE	29
8	MS_SCLK	XD_WE	30
9	MS_VCC	XD_WP	31
10	MS_GND2	XD_GND2	32
11	SD_DAT2	XD_D0	33
12	SD_DAT3	XD_D1	34
13	SD_CMD	XD_D2	35
14	SD_GND1	XD_D3	36
15	SD_VCC	XD_D4	37
16	SD_CLK	XD_D5	38
17	SD_GND2	XD_D6	39
18	NC1	XD_D7	40
19	SD_DAT0	XD_VCC	41
20	SD_DAT1	NC2	42
21	SD_CD_SW	SD_WP_SW	43
22	SD_CD_COM	SD_WP_COM	44
45	NP_NC1	NP_NC2	46
47	GND1	GND2	48

CARD_READER_44P
N/A

XD_CD#
MDIO03_SDWP_XDR/B#
MDIO09_SD/MSCLK_XDRE#
MDIO02_XDCE#
MDIO18_XDCLE
MDIO19_XDALE
MDIO08_SDCMD_MSBS_XDWE#
MDIO05_XDWP#
MDIO10_SD/MS/XDDAT0
MDIO11_SD/MS/XDDAT1
MDIO12_SD/MS/XDDAT2
MDIO13_SD/MS/XDDAT3
MDIO14_XDDAT4
MDIO15_XDDAT5
MDIO16_XDDAT6
MDIO17_XDDAT7
MDIO03_SDWP_XDR/B#
C3306 270P @
+VCCCA

+12VS
+3VS

+3VS
Q3306 IRLML5103PBF /CB
+VCCCA
R3305 100KOhm /CB
C3308 0.1UF/10V /CB
Place as close to card reader socket as possible
32,43 MDIO04_SD/MS/XDPWR

+VCCCA
C3307 0.01UF/10V @
C3309 0.01UF/10V /CB
C3310 0.01UF/10V /CB
R3306 150K /CB
C3311 2.2UF/6.3V /CB
Place as close to card reader socket as possible

To coorect the problem when MS Duo adaptor is in use.

+12VS
SDCD#
R3301 10KOhm /CB
Q3301A UM6K1N /CB
GND
MDIO11_SD/MS/XDDAT1
Q3301B UM6K1N /CB
SD_DAT1
MDIO12_SD/MS/XDDAT2
Q3302A UM6K1N /CB
SD_DAT2

Card Detect Table		
	MDIO00	MDIO01
XD	Low	Low
SD	Low	High
MS	High	Low

+3VS
R3302 10KOhm /CB
XD_CD#
SDCD#
D3301 DAP202K /CB
/CB
Q3302B UM6K1N
R3208 0Ohm r0402 @
MDIO00_SDCD#_XDCD#
MDIO01_MSCD#_XDCD#
D3302 DAP202K /CB
+3VS
R3304 10KOhm /CB
MSCD#
For Memory Stick Duo Adaptor shielding ground issue

<Variant Name>

ASUSTek COMPUTER INC
Project Name: X51RL
Engineer: MICHAEL WANG
Size: Custom
Title : CardReader
Rev: 2.0
Date: Tuesday, July 03, 2007
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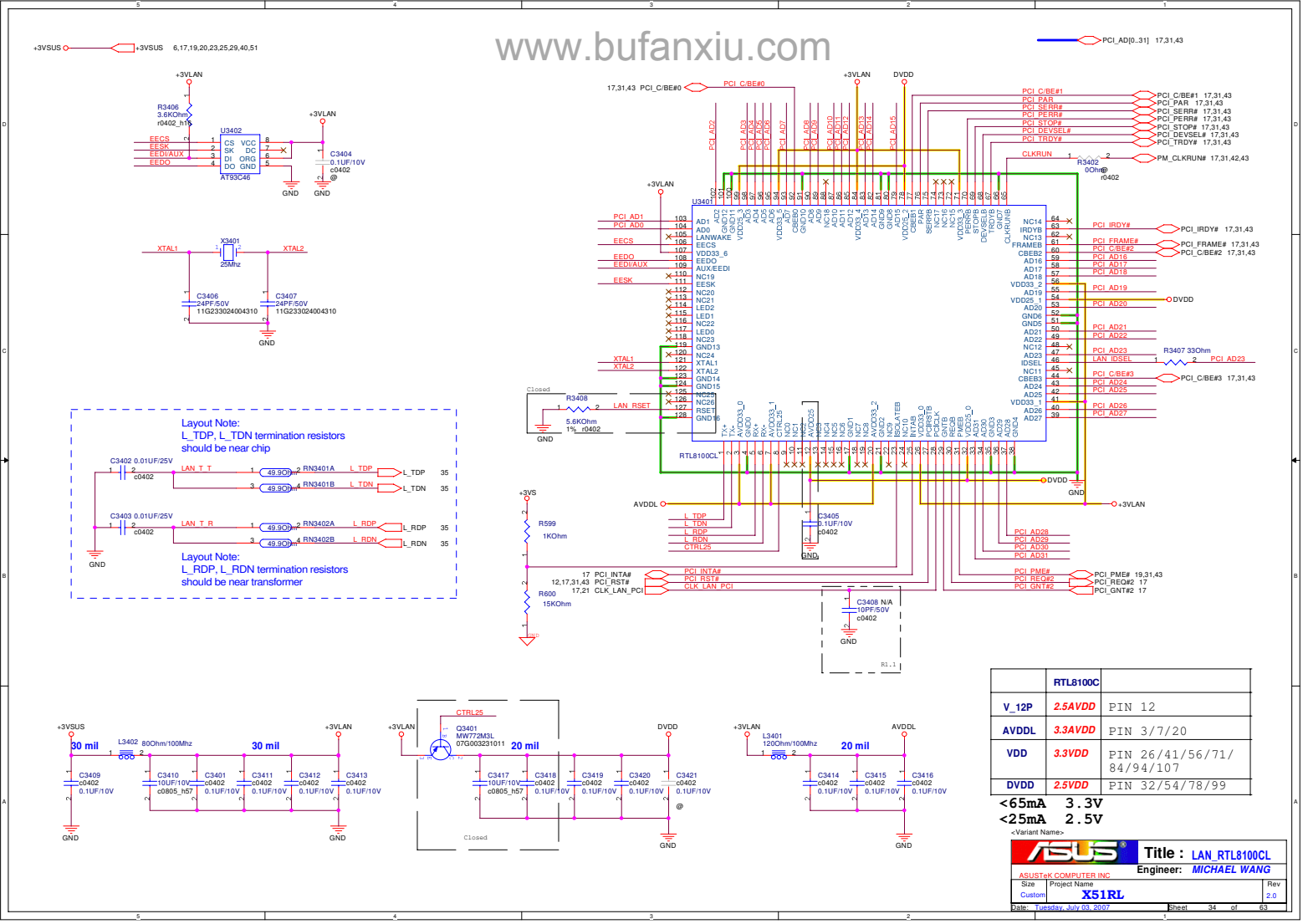
+12VS — +12VS 12,37,61
+3VS — +3VS 2,4,5,9,12,13,14,15,17,18,19,20,21,22,23,25,26,28,29,31,32,34,37,39,40,42,43,50,52,60,61

<< Kennedy_Zhang >>

www.bufanxiu.com



	RTL8100C	
V_12P	2.5AVDD	PIN 12
AVDDL	3.3AVDD	PIN 3/7/20
VDD	3.3VDD	PIN 26/41/56/71/84/94/107
DVDD	2.5VDD	PIN 32/54/78/99

<65mA 3.3V
<25mA 2.5V
<Variant Name>

ASUSTeK COMPUTER INC
Title : LAN_RTL8100CL
Engineer: MICHAEL WANG
Size: Custom
Project Name: X51RL
Rev: 2.0
Date: Tuesday, July 03, 2007
Sheet 34 of 63

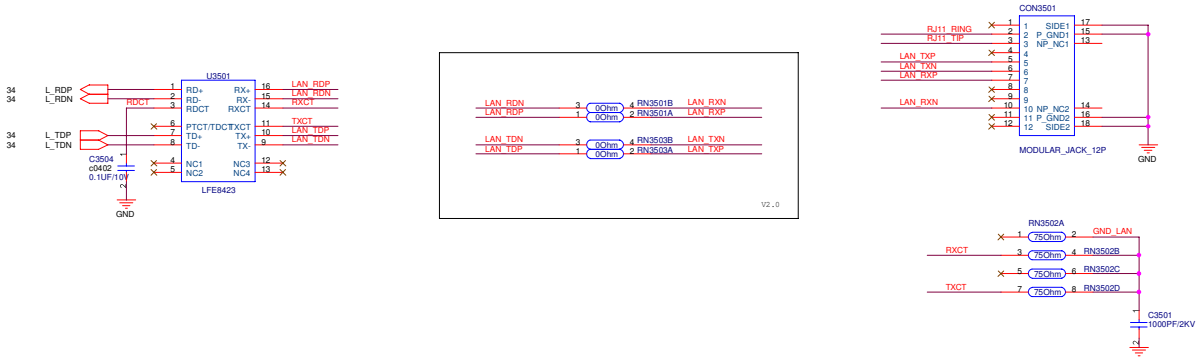
<< Kennedy_Zhang >>

+3V +3V 17,25,26,27,31,37,42,43,44,61

LAN PORT

www.bulanxiu.com

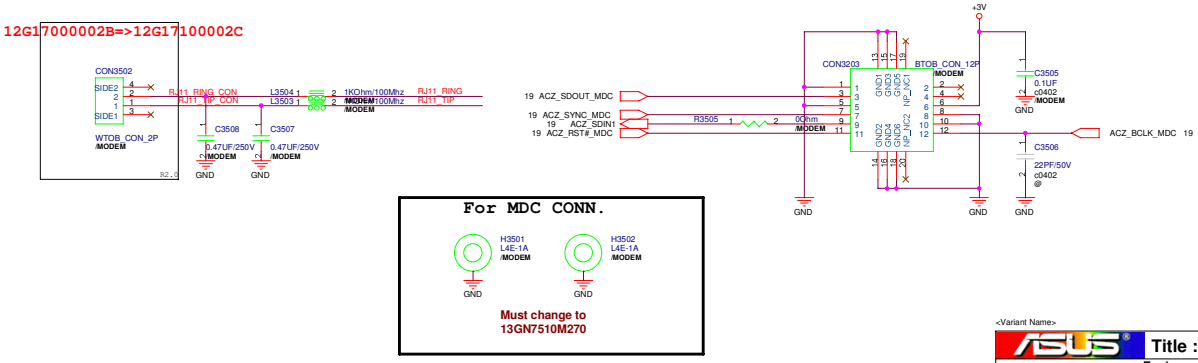
12G142111120



MDC CONNECTOR

12G161200124

12G17000002B=>12G17100002C



For MDC CONN.

H3501 L4E-1A /MODEM

H3502 L4E-1A /MODEM

GND

Must change to 13GN7510M270

<Variant Name>

ASUSTeK COMPUTER INC

Title : RJ11/45 & MDC

Engineer: MICHAEL WANG

Size	Project Name	Rev
Custom	X51RL	2.0

Date: Tuesday, July 03, 2007 Sheet 35 of 63

<< Kennedy_Zhang >>

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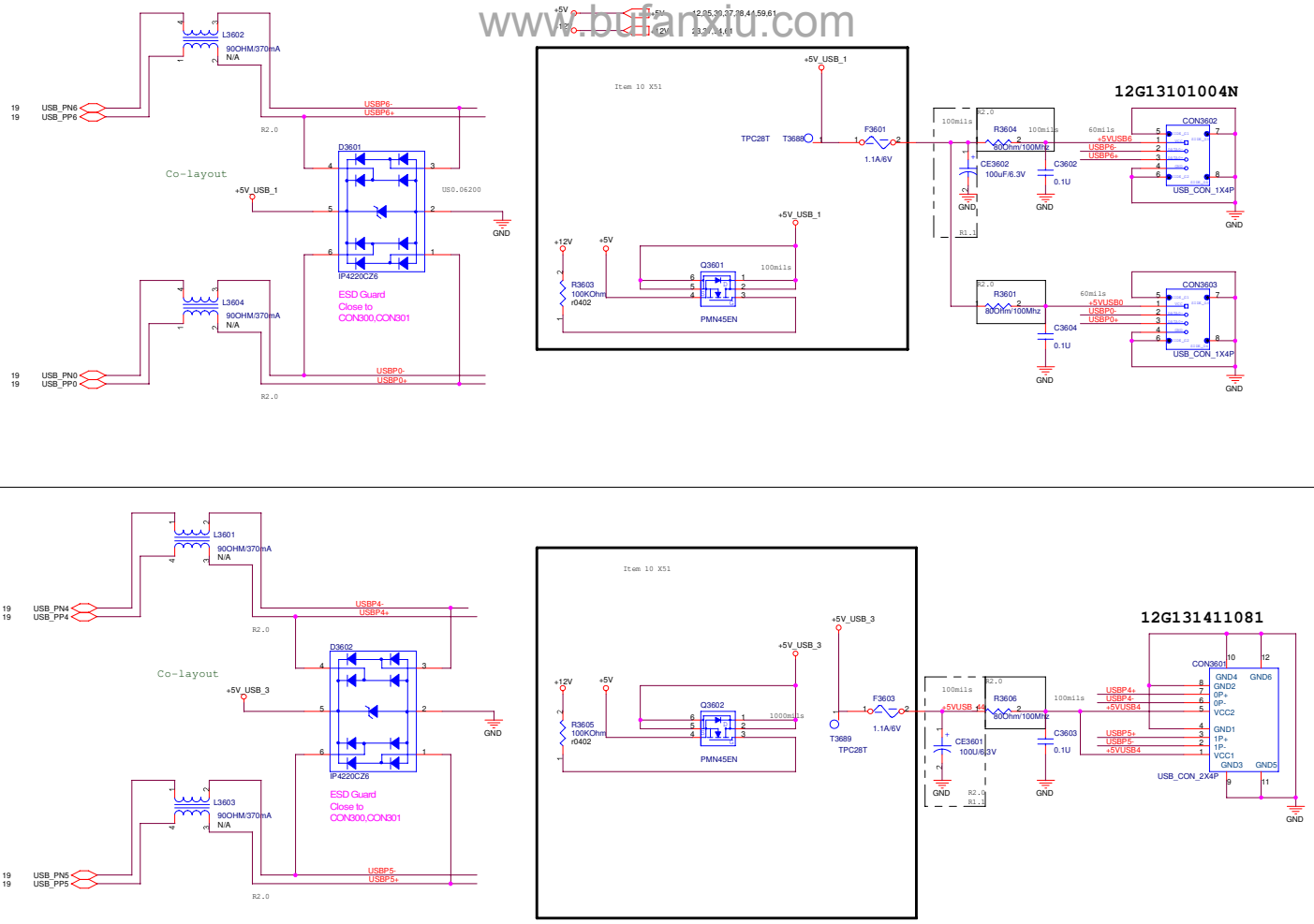

<Variant Name>

ASUSTek COMPUTER INC	Project Name	X51RL
	Engineer:	MICHAEL WANG
Size: Custom	Title :	USB CONN & +5V DC JACK
Rev: 2.0		
Date: Tuesday, July 03, 2007	Sheet	36 of 63

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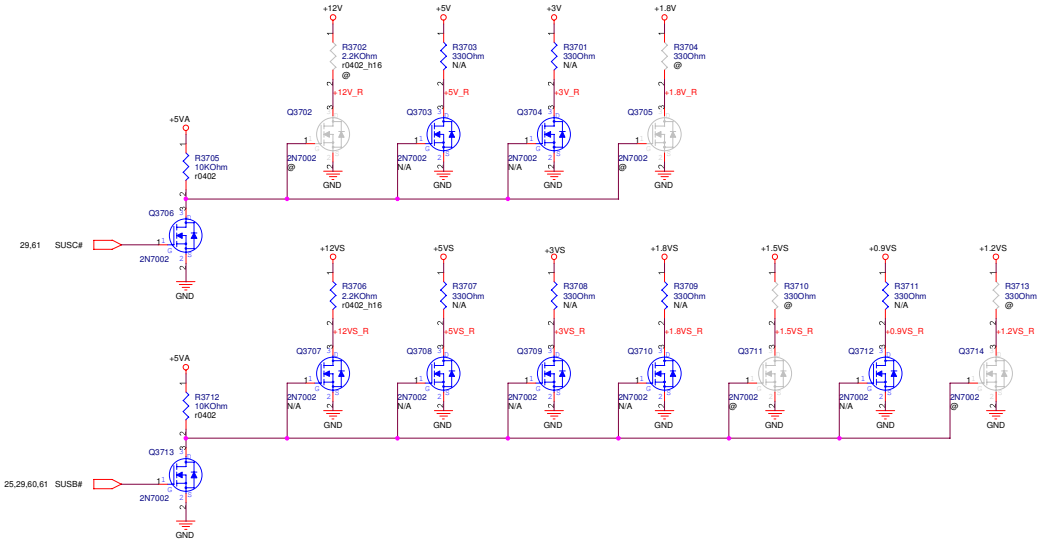

Check all power plan

<Variant Name>

ASUSTeK COMPUTER INC	Title : Discharge Circuit	
	Engineer: MICHAEL WANG	
Size: Custom	Project Name: X51RL	Rev: 2.0
Date: Tuesday, July 03, 2007	Sheet 37 of 63	

<< Kennedy_Zhang >>

Main Board SW & LED

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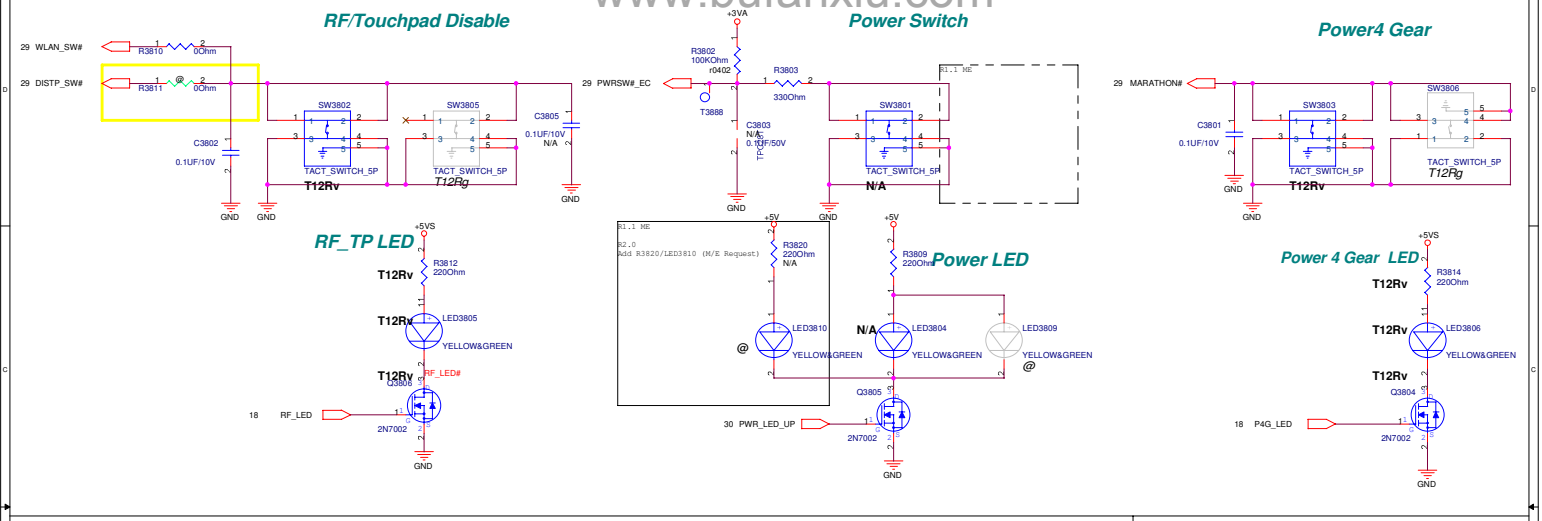

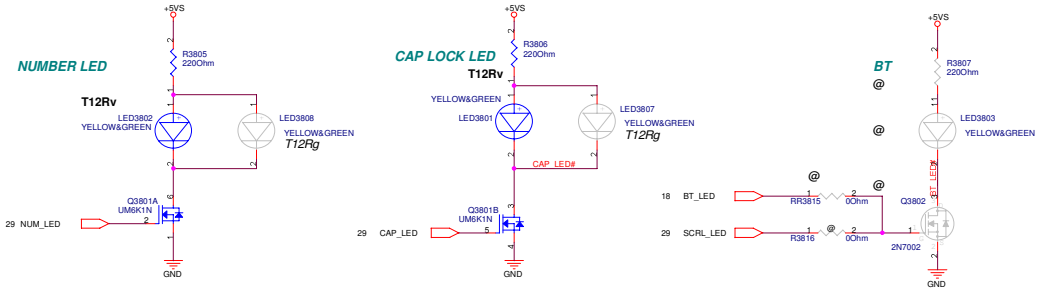

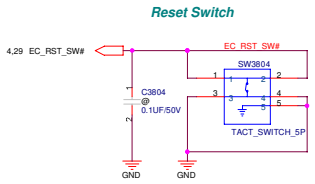

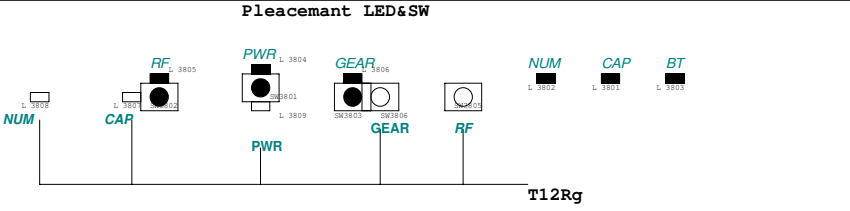

<Variant Name>
Title : SW/LED
ASUSTeK COMPUTER INC
Engineer: MICHAEL WANG
Size: Custom
Project Name: X51RL
Rev: 2.0
Date: Tuesday, July 03, 2007
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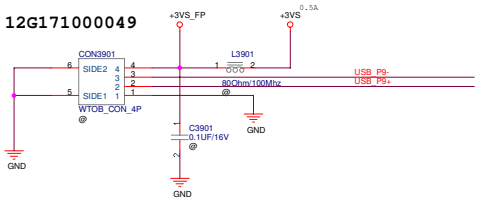
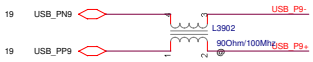
+3VS +3VS 2,4,5,9,12,13,14,15,17,18,19,20,21,22,23,25,26,28,29,31,32,33,34,37,40,42,43,50,52,60,61

FINGER PRINT
Reserved

USB P0 CON3603
USB P1
USB P2 BT
USB P3 NEW CARD
USB P4 CON3601
USB P5 CON3601
USB P6 CON3602
USB P7
USB P8 PC_CAM
USB P9 FINGER PRINT





<Variant Name>

Title : FINGER PRINT
ASUSTeK COMPUTER INC
Engineer: MICHAEL WANG
Size: Custom
Project Name: X51RL
Rev: 2.0
Date: Tuesday, July 03, 2007
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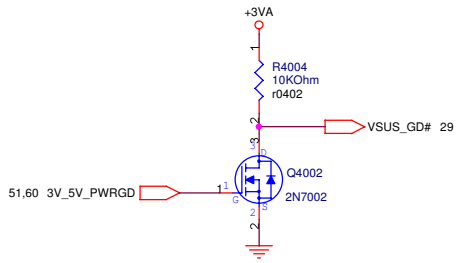
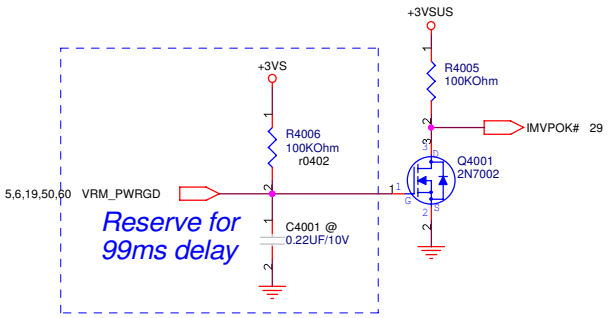
+3VA
+3VS
+3VSUS

+3VA
+3VS
+3VSUS

12,17,29,38,54,57,59,63
2,4,5,9,12,13,14,15,17,18,19,20,21,22,23,25,26,28,29,31,32,33,34,37,39,42,43,50,51,60,61
6,17,19,20,23,25,29,34,51





<Variant Name>

Title : POWER-ON SEQ.

Engineer: MICHAEL WANG

ASUSTeK COMPUTER INC

Size	Project Name	Rev
A4	X51RL	2.0

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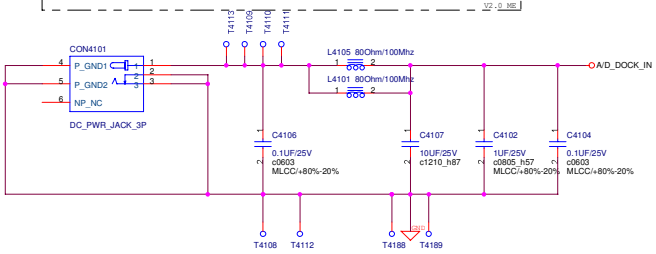
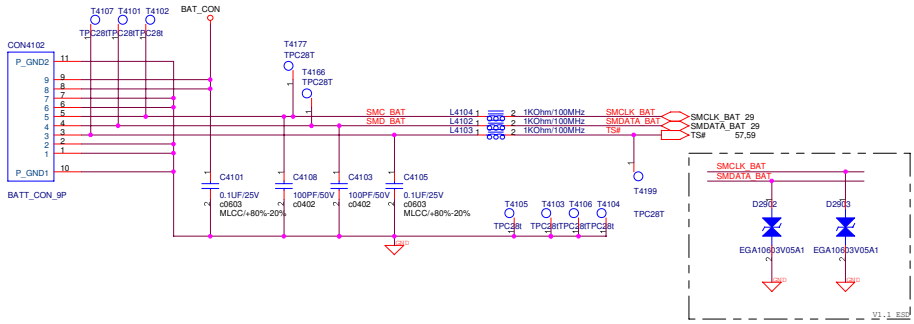
A/D_DOCK_IN — A/D_DOCK_IN 57,59
BAT_CON — BAT_CON 57
AC_BAT_SYS — AC_BAT_SYS 12,50,51,52,53,54,57,60

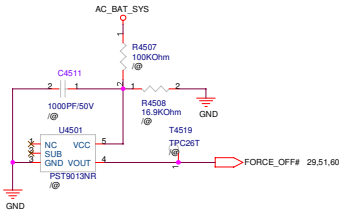
12G145002034=>12G145301031=>12G145301031



12G20001090G



Without Battery & Pull out Adapter
RESERVED



<Variant Name>

ASUSTek COMPUTER INC	Project Name	X51RL
	Engineer:	MICHAEL WANG
Size: Custom	Title : DC IN	Rev: 2.0
Date: Tuesday, July 03, 2007	Sheet 41 of 63	

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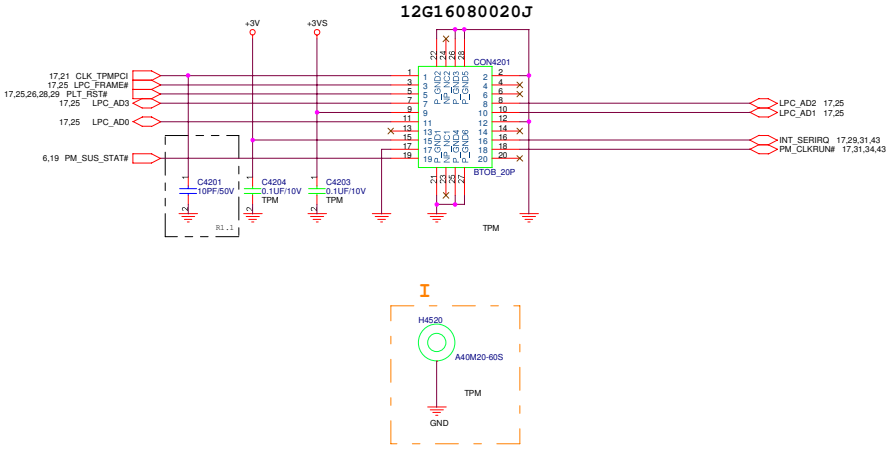
+3VS +3VS 2,4,5,9,12,13,14,15,17,18,19,20,21,22,23,25,26,28,29,31,32,33,34,37,39,40,43,50,52,60,61

+3V +3V 17,25,26,27,31,35,37,43,44,61

www.bufanxiu.com

TPM Module CON
RESERVED



For TPM CONN.

<Variant Name>

ASUSTek COMPUTER INC	Project Name: X51RL	
	Engineer: MICHAEL WANG	
Size: Custom	Title : TPM 1.2	Rev: 2.0
Date: Tuesday, July 03, 2007	Sheet 42 of 63	

<< Kennedy_Zhang >>

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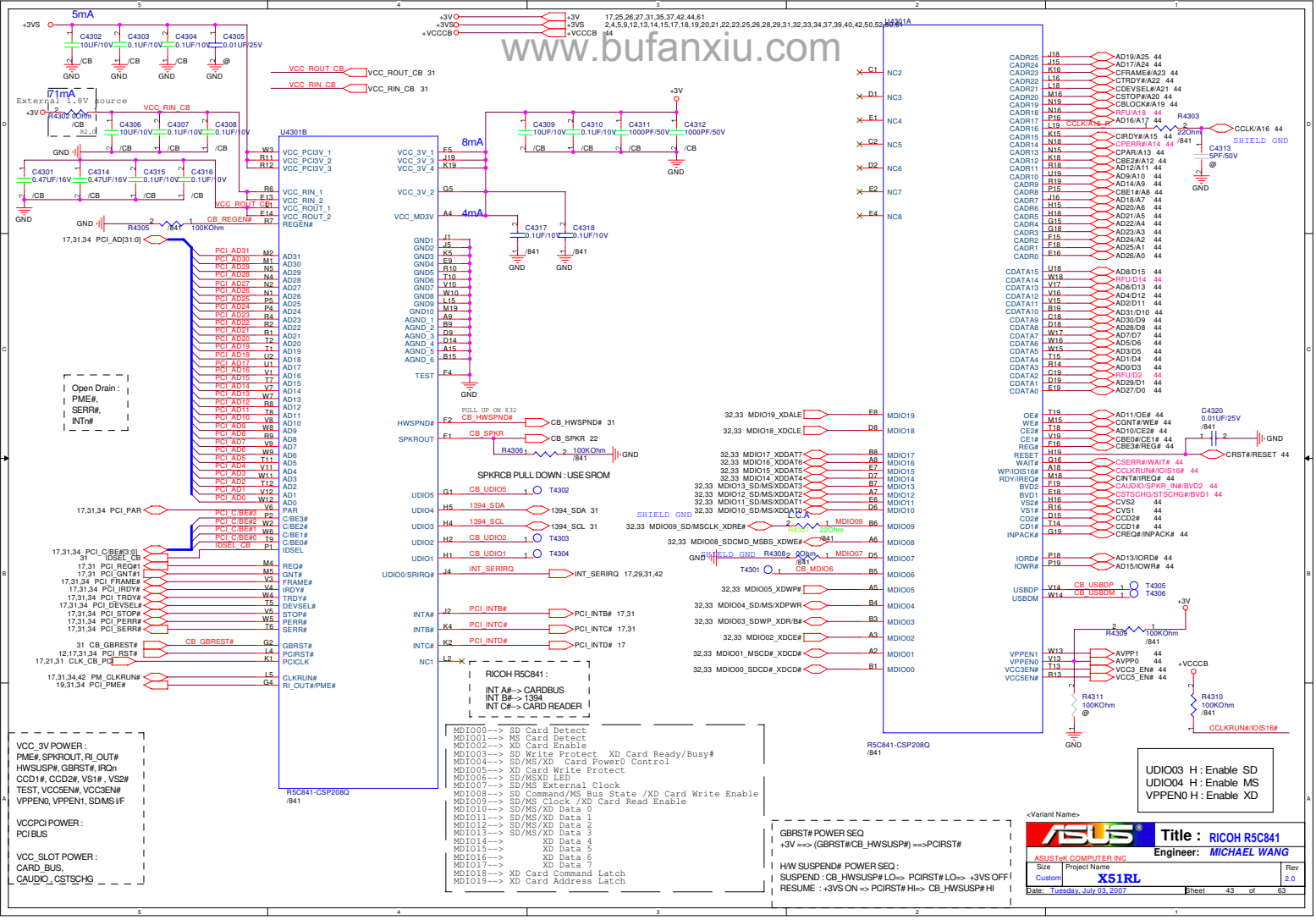
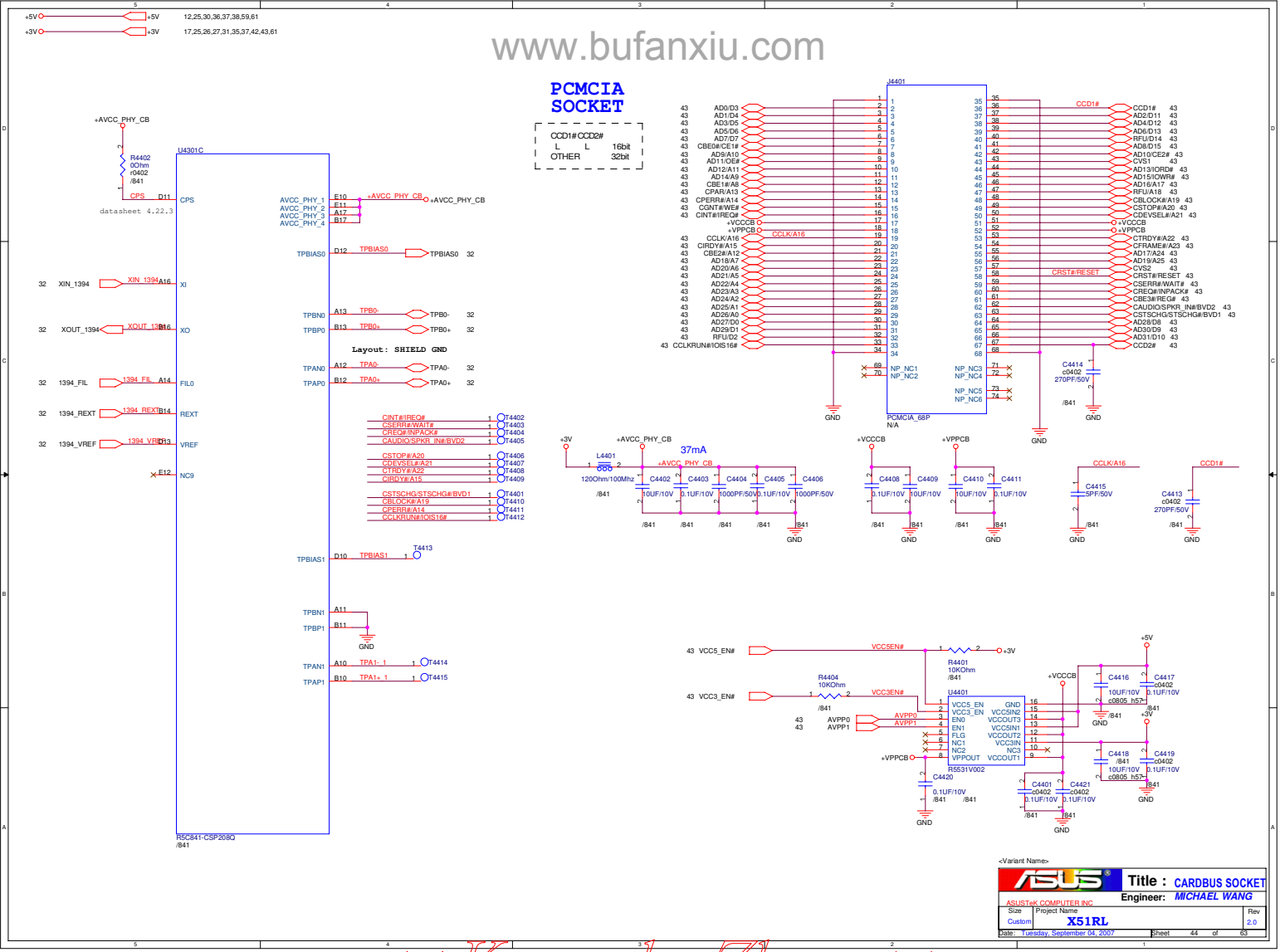


<< Kennedy_Zhang >>

www.bufanxiu.com



<< Kennedy_Zhang >>

<Variant Name>

ASUSTeK COMPUTER INC

Title : CARDBUS SOCKET		
Engineer: MICHAEL WANG		
Size: Custom	Project Name: X51RL	Rev: 2.0
Date: Tuesday, September 04, 2007	Sheet 44 of 63	

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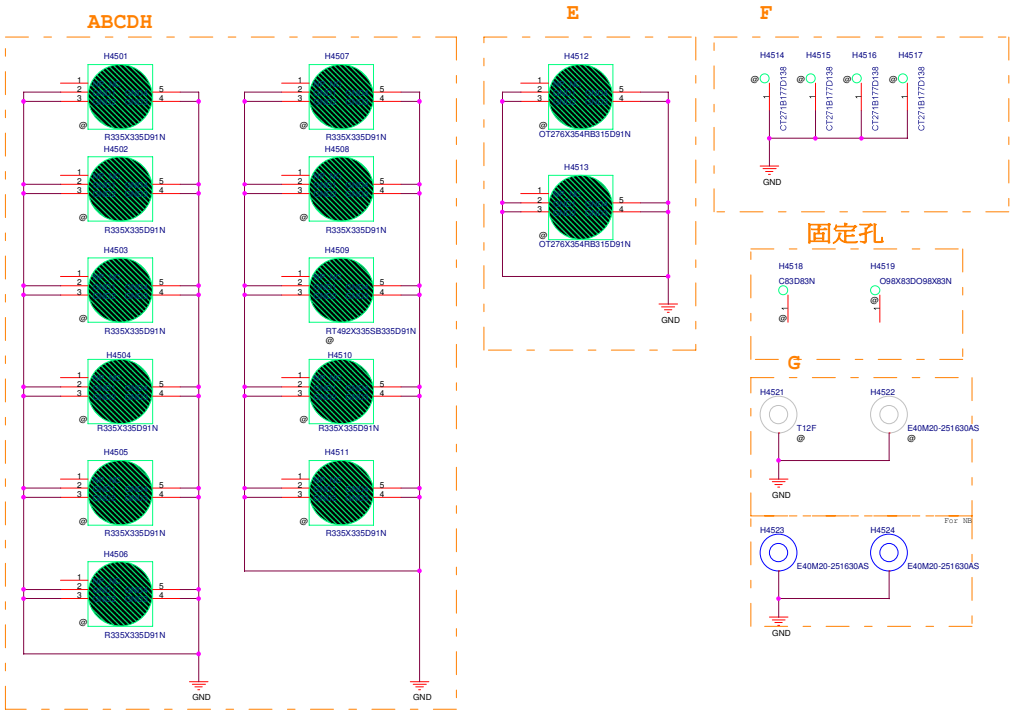

<Variant Name>

ASUSTeK COMPUTER INC

Title : SCREW HOLE

Engineer: MICHAEL WANG

Size	Project Name	Rev
Custom	X51RL	2.0

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www.bufanxiu.com

<Variant Name>

Title : HISTORY

ASUSTeK COMPUTER INC

Engineer: MICHAEL WANG

Size	Project Name	Rev
Custom	X51RL	2.0

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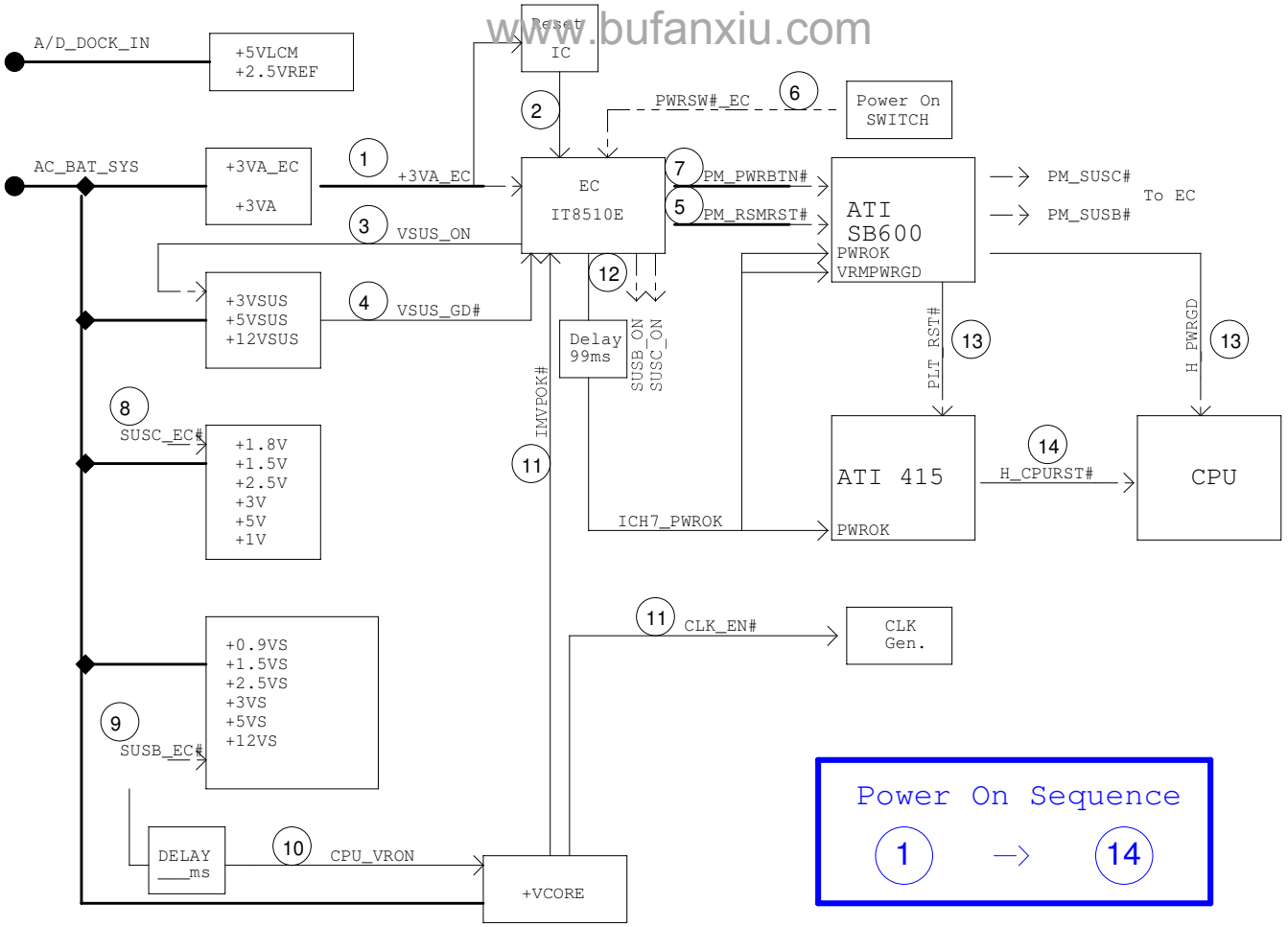

<Variant Name>

ASUSTeK COMPUTER INC

Title : FLOWCHART

Engineer: MICHAEL WANG

Size	Project Name	Rev
Custom	X51RL	2.0

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www.laoyu.com

EC GPIO SETTING

Pin	Pin Name	Signal Name	Type
32	PWM0/GPA0	BRIGHT_PWM	
33	PWM1/GPA1	FAN_PWM	O
36	PWM2/GPA2	/	
37	PWM3/GPA3	/	
38	PWM4/GPA4	CHG_LED_UP#	O
39	PWM5/GPA5	PWR_LED_UP#	O
40	PWM6/GPA6	BATSEL_3S#	
43	PWM7/GPA7	LCD_BACKOFF#	O
153	RXD/GPB0	NUM_LED	O
154	TXD/GPB1	CAP_LED	O
162	GPB2	SCRL_LED	O
163	SMCLK0/GPB3	SMCLK_BAT	I/0
164	SMDAT0GPB4	SMDATA_BAT	I/0
5	GA20/GPB5	A20GATE	O
6	KBRST#/GPB6	RC_IN#	O
165	GPB7	THRO_CPU	O
169	SMCLK1/GPC1	SMB1_CLK	I/0
170	SMDAT1/GPC2	SMB1_DAT	I/0
171	GPC3	/	
172	TMRI0/WUI2/GPC4	ACIN_OC#	I
175	GPC5	OP_SD#	O
176	TMRI1/WUI3/GPC6	BAT_IN_OC#	I
1	CK32KOUT/GPC7	/	O
26	RI1#/WUI0/GPD0	PM_SUSB#	I
29	RI2#/WUI1/GPD1	PM_SUSC#	I
30	LPCRST#/WUI4//GPD2	PLT_RST#	I
31	ECSCI#/GPD3	EXT_SCI#	O
41	GPD4		I
42	GINT/GPD5	/	
62	TACH0/GPD6	FAN0_TACH	I
63	TACH1/GPD7	/	O
87	ADC4/GPE0	WLAN_SW#	I
88	ADC5/GPE1	/	I
89	ADC6/GPE2	MARATHON#	I
90	ADC7/GPE3	DISTP_SW#	I
2	PWRSW/GPE4	PWRSW#_EC	I
44	WUI5/GPE5	/	
24	LPCPD#/WUI6/GPE6	LID_EC#	I
25	CLKRUN#/WUI7/GPE7		O
110	PS2CLK0/GPF0	/	
111	PS2DAT0/GPF1	/	
114	PS2CLK1/GPF2	/	I/0
115	PS2DAT1/GPF3	/	I/0
116	PS2CLK2/GPF4	TP_CLK	
117	PS2DAT2/GPF5	TP_DAT	
118	PS2CLK3/GPF6	PWRLMT#	
119	PS2DAT3/GPF7	/	I
113	FA16/GPG0	FA16	
112	FA17/GPG1	FA17	
104	FA18/GPG2	FA18	
103	FA19/GPG3	/	
3	FA20/GPG4	THRM_CPU#	I
4	FA21/GPG5	/	
27	LPC80HL/GPG6	PMTHERM#	O
28	LPC80LL/GPG7	AC_APR_UC#	I

Pin	Pin Name	Signal Name	Type
48	GPH0	VSUS_ON	O
54	GPH1	VSUS_GD#	I
55	GPH2	IMVPOK#	I
69	GPH3	PM_PWRBTN#	O
70	GPH4	SUSC_EC#	O
75	GPH5	SUSB_EC#	O
76	GPH6	CPU_VRON	O
105	GPH7	PM_RSMRST#	O
148	GPI0	ICH7_PWROK	O
149	GPI1	WATCH_DOG#	O
152	GPI2	/	
155	GPI3	CHG_EN#	O
156	GPI4	PRECHG	O
168	GPI5	BAT_LL#	O
174	GPI6	BAT_LEARN	O
8	GPL0	WLAN_ON#	O
11	GPL1	BT_ON#	O
12	GPL2	RF_OFF_SW#	I
20	GPL3	RF_LED	O
92	CRX	CRX	I/0

ICH7-M GPIO SETTING

Pin	Pin Name	Signal Name	Type
AG18	GPIO00/TM_BUS_7	CPU_BMBUSY#	I
C8	GPIO01/REQ5#	PCI_REQ#5	I
G8	GPIO02/PIRQE#	PCI_INTE#	I
F7	GPIO03/PIRQF#	PCI_INTF#	I
F8	GPIO04/PIRQG#	PCI_INTG#	I
G7	GPIO05/PIRQH#	PCI_INTH#	I
AC21	GPIO06	BT_LED	I/O
AC18	GPIO07	/	I
E21	GPIO08	EXTSMI#	I
E20	GPIO09	SATA_DET#0	I
A20	GPIO10	/	O
B23	SMBALERT#/GPIO11	SMB_ALERT#	I
F19	GPIO12	KBC_SCI#	I
E19	GPIO13	/	
R4	GPIO14	/	
E22	GPIO15	WLAN_LED#	I/O
AC22	GPIO16	PM_DPRSLPVR	O
D8	GPIO17/GNT5#	PCI_GNT#5	O
AC20	GPIO18/STP_PCI#	STP_PCI#	O
AH18	GPIO19/SATA1GP	/	I
AF21	GPIO20/STP_CPU#	STP_CPU#	O
AE19	GPIO21/SATA0GP	/	I
A13	GPIO22/REQ4#	PCI_REQ#4	I
AA5	LDRQ1#/GPIO23	LPC_DRQ#1	I/O
R3	GPIO24	P4G_LED#	
D20	GPIO25	CB_SD#	
A21	GPIO26/EL_RSVD	BT_DET#	
B21	GPIO27/EL_STATE0		I
E23	GPIO28/EL_STATE1		
C3	GPIO29/OC#5	USB_OC_5#	I
A2	GPIO30/OC#6	NEWCARD_OC#	I
B3	GPIO31/OC#7	USB_OC_7#	I
AG18	GPIO32/CLKRUN#	PM_CLKRUN#	O
AC19	GPIO33/AZ_DOCK_EN#	/	O
U2	GPIO34/AZ_DOCK_RST#	/	
AD21	GPIO35	ICH_GPIO35	O
AH19	GPIO36/SATA2GP	/	
AE19	GPIO37/SATA3GP	PCB_ID0	I/O
AD20	GPIO38	PCB_ID1	I
AE20	GPIO39	PCB_ID2	I
A14	GNT4#/GPIO48	PCI_GNT#4	O
AG24	GPIO49/CPUPWRGD	H_PWRGD	O

PCI Device	IDSEL#	REQ/GNT#	Interrupts
10/100 RTL8100CL	AD23	2	A
CARDBUS	AD17	1	B
1394	AD17	1	C
CARD READER	AD17	1	D

PCIE Device	Bus		
MINI_CARD	PE(T/R)(p/n)2		
NEWCARD	PE(T/R)(p/n)3		

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
Thermal Sensor	1001100x (98)

<Variant Name>

ASUSTeK COMPUTER INC

Title : GPIO Setting

Engineer: MICHAEL WANG

Size	Project Name	Rev
Custom	X51RL	2.0

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<< Kennedy_Zhang >>

T12R V1.1 History

1. Page 17, del U1702 and R1726 delete PCI_RST# Buffer.
3. Page 18, added R1802
4. Page 43&12, D4301 and L1201改footprint
5. Page 6, delete D1204 and added R601 R609 to avoid can not boot.
6 Page 17, Mount R1708, U1703 option changed reset path
7. Page 43, Mount R4302 for R5C841 internal LDO input
8. Page 9, un-mount L906 C914 , these for 610 only

9. All PCI clock added 6.8 pF to decrease skew.
10. PWM connected to EC and back-light connected to NB
11. D1306 D1301 connected to +5VS, let these signal have the same PWR plan. For ESD
12. page 19, added BT_DET# to detect BT.
13. Page 19, adjust USB OC ping to correspond USB port
14. Page 25, modification NEW CARD debug circuit to correspond new debug card
15. page 28, we used correctly capacity for customer request.
16. page 36, we used LDO with over current protect IC
17. page 41, DC in connector add 2nd source.

ME modify
1.ODD往板外移0.4mm
2
3.BATT 往板內移0.23mm
4.增加螺絲鎖付記號

6.DDR2 added 2nd source
  P/N :12G025022004
  DDR2 DIMM 200P,1.8V,H:4mm,STD
  FOXCONN/AS0A426-N4SN-1
7.add led 1 pcs LED3810 and del. SW3807(option)
8.遮版圖修改

T12R V2.0 Modify History

1. Page 6, R609 repleacement 220K by 10K
2. Page 12, RN1203 repleacement C.M chock by 0Ohm for EMI.
3. For DDRII connector(H=4mm) repleacement 12G025022004 by original.
4. For DDRII connector(H=9mm) repleacement 12G025C22004 by original.
5. For DC IN jack repleacement 12G14530103E by original(long core).
6. Page 22, for audio micro phone low quility issue, it need to changed larger cappator 10U (replace 100 with 1U).
7. Page 29, we changed new EC 8511.
8. Page 38, to increase LED brightness, we replace 07G015200485 by original
9. page 30, for EMI request, we added L3010 and L3011 and mount C3002 C3003 and C3006~3010
10 Page 35, for EMI requestion, we added 0Ohm before LAN jack for option CM chock.

T12Rg V1.0 modify from T12R V2.0

1. To modify BOM include LED(color placement), SW(placement), HDD_PATA(T SATA), PCCAM(unmount), internal MIC(unmount, and R5C841(del 1394, card reader and PCMCIA).

T12Rg V2.0

1. Page 12, L1203 0 Ohm to bead, EMI request.
2. Page 12, L1204 and L1205 0 Ohm to bead and mount C1222 C1223, EMI request.
3. Page 12, mount L1214 L1215 Ohm for added internal speaker.
4. Page 12, mount L1206, EMI request.
5. Page 6, R2301 and R2304 10K to 12K for 2W speaker..
6. Page 6, modify BOM, unmount R2908.

T12R V2.1/ X51 V1.0 modify from T12R V2.0

1. Page 6, support DDRII 667, modify DDR sechematic(CKE OTD)
1. Page 6, replacment SB A20 form A13
1. Page 6, modify BOM, delete R2908.
1. Page 6, added D2910 for EMI.
1. Page 6, to support 3S1P, added some circuit EC to H_PROCHOT_S#.

1. Page 6,modify BOM include LED, SW, HDD(DEL PATA), PCCAM and R5C841(added).

	X51	T12RG	T12R
NB	415ME	415ME	415MD
SB	SB600 A21	SB600 A21	SB600 A13
AUDIO	660VD	660VD	660VD
SPDIF	N/A	N/A	N/A
R5C832	N/A	N/A	N/A
R5C841	OK	OK	N/A
1394	N/A	OK	N/A
CARD READER	OK	OK	N/A
PCMCIA	OK	OK	N/A
NEW CARD	N/A	N/A	N/A
TPM	N/A	OK	N/A
BT	OK	N/A	N/A
PC_CAM	N/A	N/A	OK
INT. MIC.	N/A	OK	OK
MODEN	OK	N/A	N/A
TV	N/A	N/A	N/A
SPEAKER	1.5W	2W	1.5W

Title : HISTORY
Engineer:
Size: B
Project Name: X51RL
Rev: 1.0
Date: Wednesday, May 16, 2007
Sheet 38 of 38

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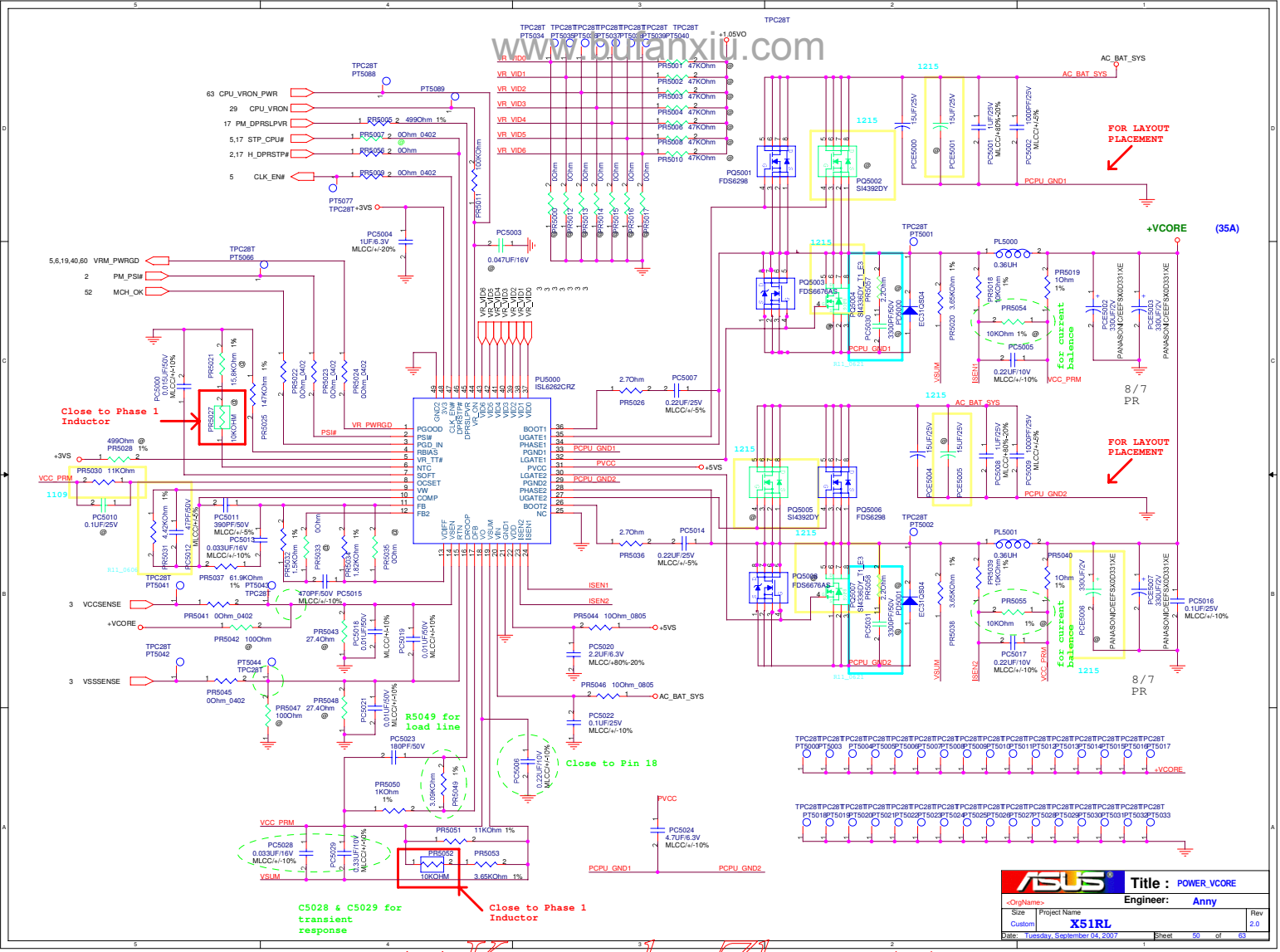
<< Kennedy_Zhang >>



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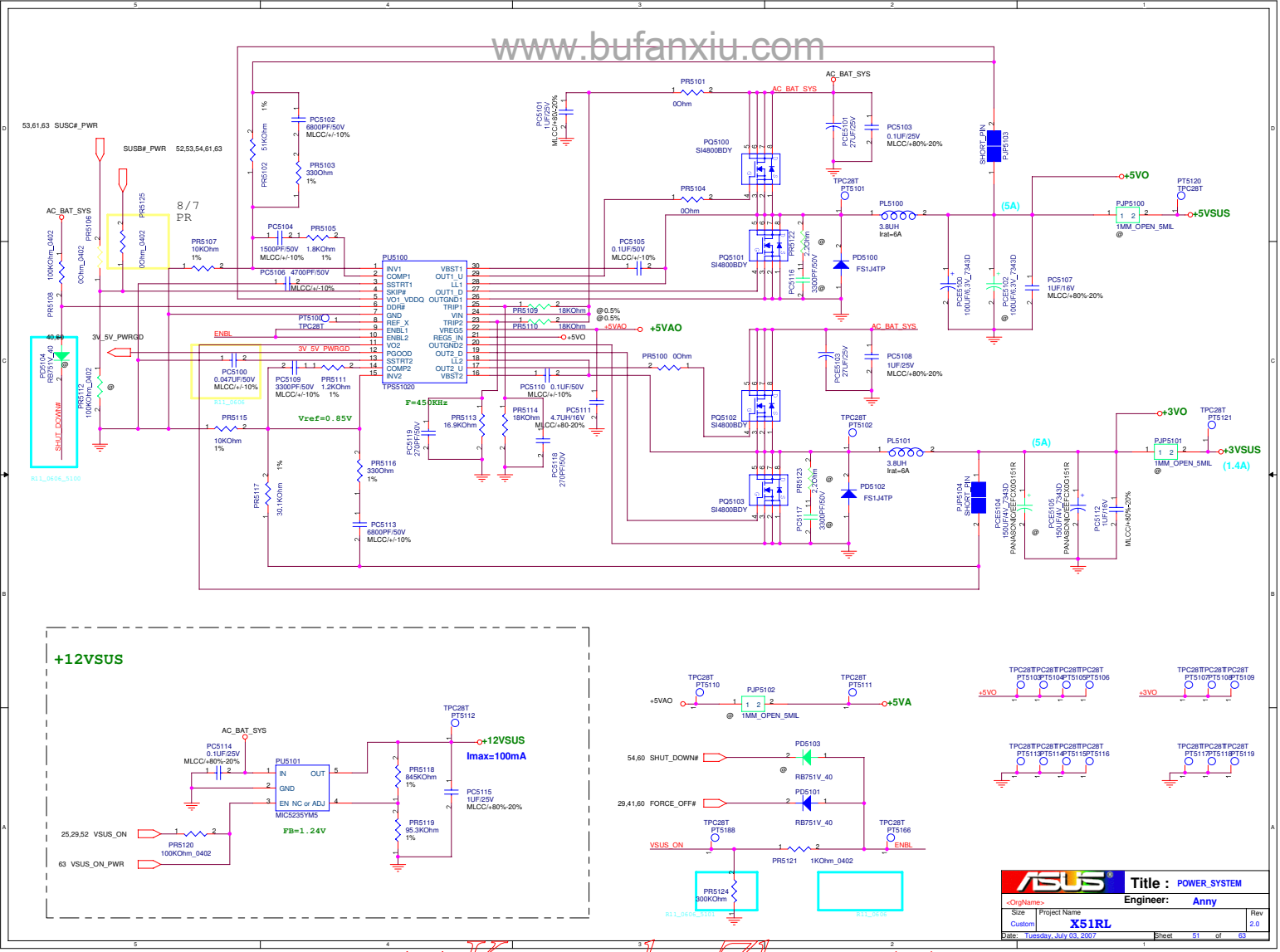

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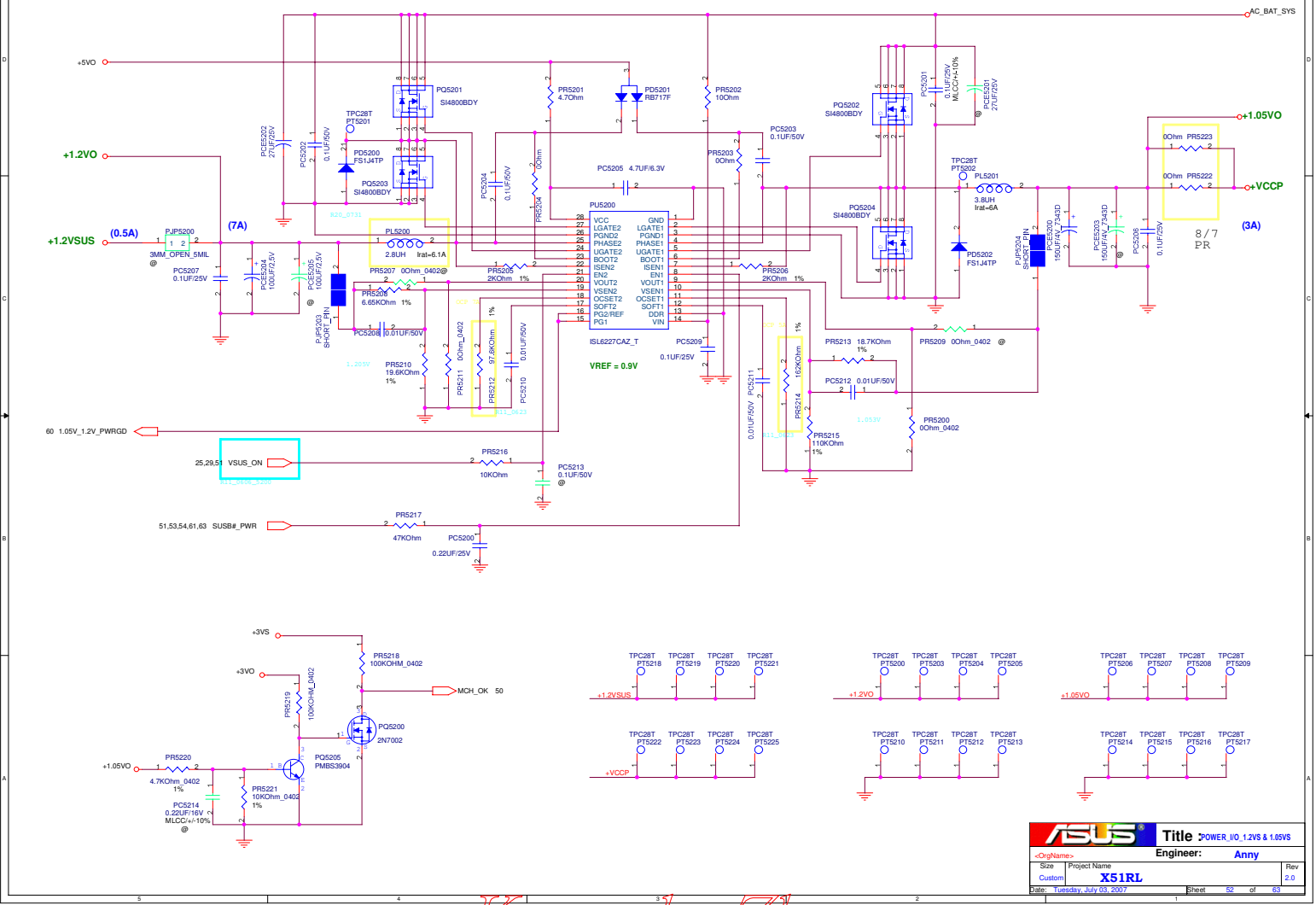

Title: POWER_I/O_1.2VS & 1.05VS
<OrgName> Engineer: Anny
Size: Custom | Project Name: X51RL | Rev: 2.0
Date: Tuesday, July 03, 2007 | Sheet 52 of 63

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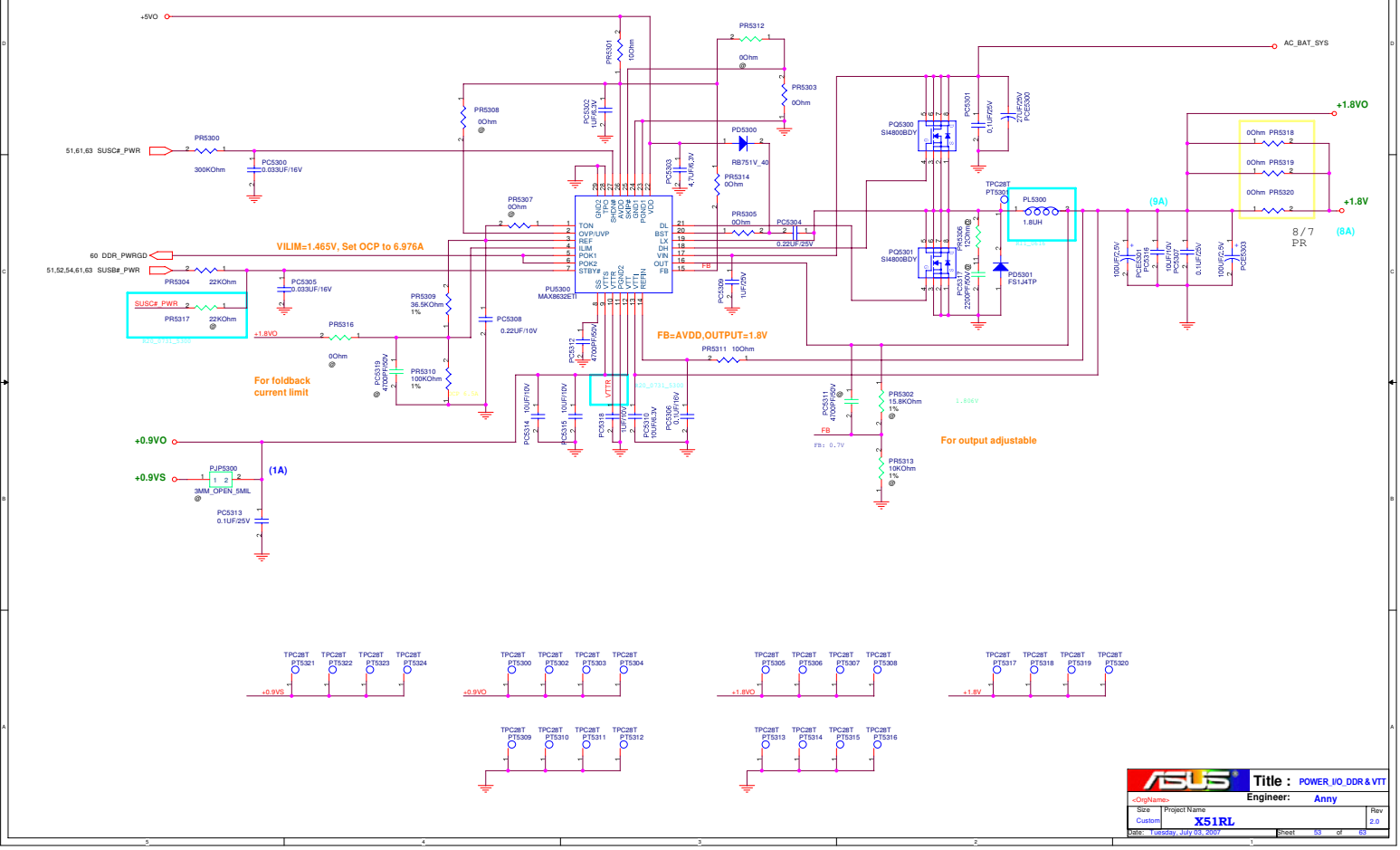

ASUS Title : POWER_I/O_DDR & VTT
<OrgName> Engineer: Anny
Size: Custom | Project Name: X51RL | Rev: 2.0
Date: Tuesday, July 03, 2007 | Sheet 53 of 63

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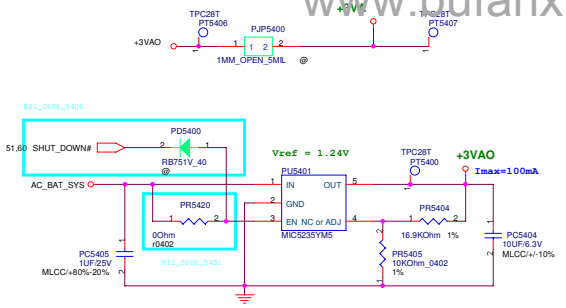
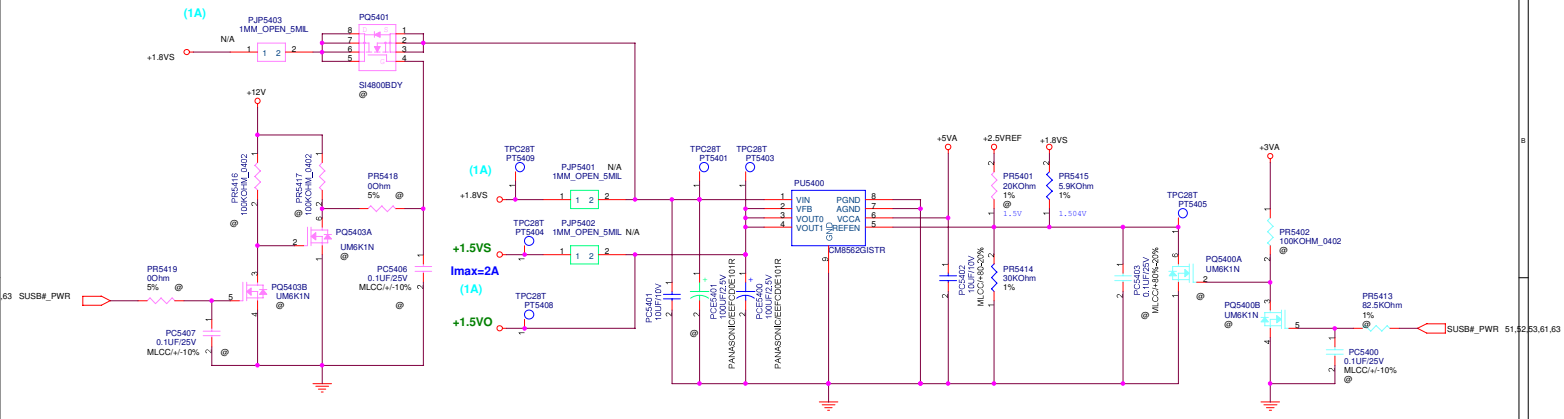
+3VAO



+2.5VS



Title : POWER_I/O_+3VA & +2.5V		
<OrgName>	Engineer: Anny	
Size: Custom	Project Name: X51RL	Rev: 2.0
Date: Tuesday, July 03, 2007	Sheet 54 of 63	

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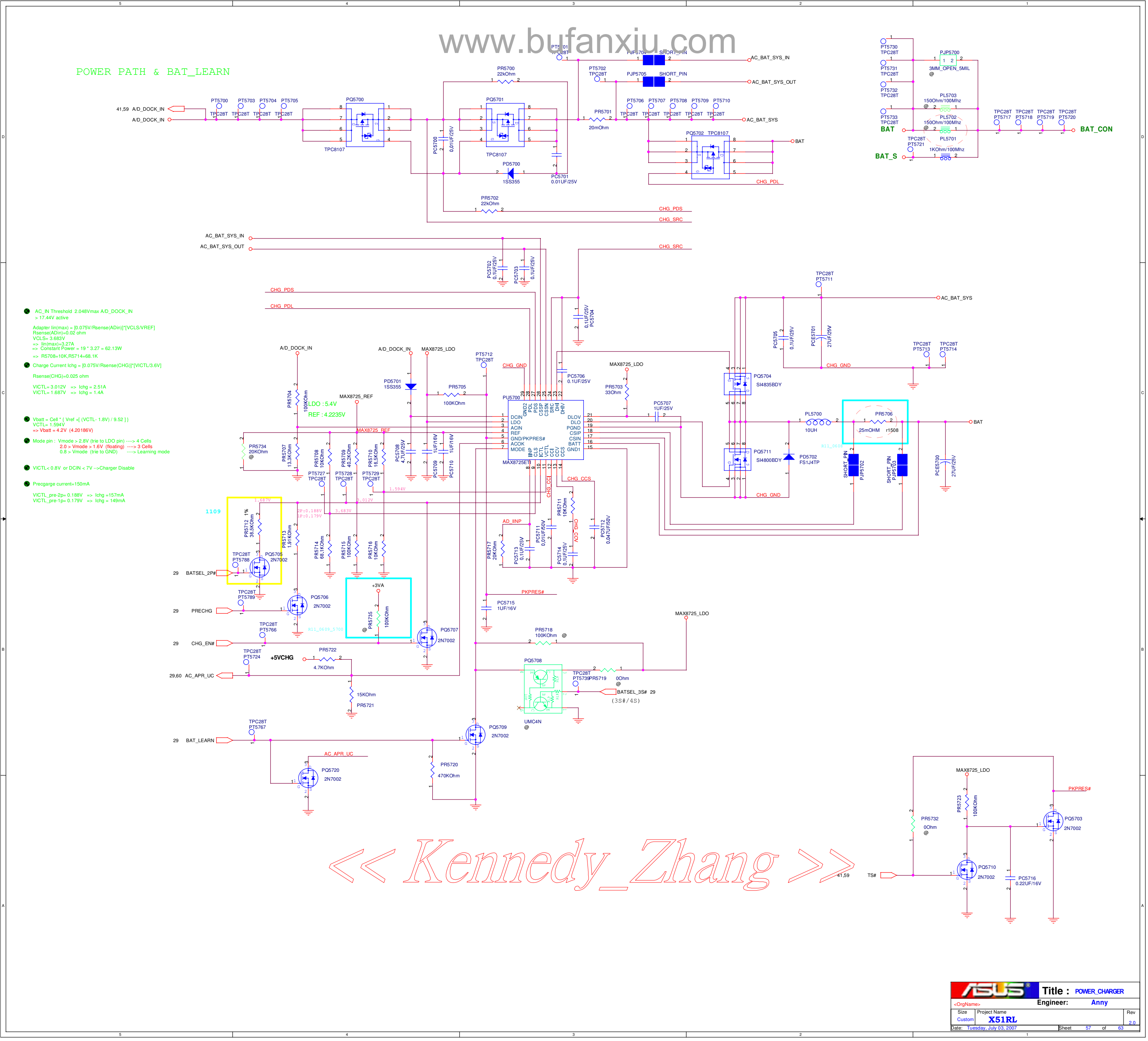

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POWER PATH & BAT_LEARN
A/D_DOCK_IN
AC_BAT_SYS_IN
AC_BAT_SYS_OUT
AC_BAT_SYS
CHG_PDS
CHG_PDL
CHG_SRC
CHG_GND
BAT
BAT_S
BAT_CON
PQ5700 TPC8107
PQ5701 TPC8107
PQ5702 TPC8107
PR5700 22kOhm
PR5701 20mOhm
PR5702 22kOhm
PD5700 1SS355
PC5700 0.01UF/25V
PC5701 0.01UF/25V
PJP5704 SHORT_PIN
PJP5705 SHORT_PIN
PJP5700 3MM_OPEN_5MIL
PL5703 150Ohm/100Mhz
PL5702 150Ohm/100Mhz
PL5701 1KOhm/100Mhz
PU5700 MAX8725ETI
DCIN LDO ACIN REF GND/PKPRES# ACOK MODE
DLOV DLO PGND CSIP CSIN BATT GND1
PQ5704 SI4835BDY
PQ5711 SI4800BDY
PD5702 FS1J4TP
PL5700 10UH
PR5706 25mOhm r1508
PC5700 27UF/25V
AC_IN Threshold: 2.048Vmax A/D_DOCK_IN = 17.44V active
Adapter Iin(max) = [0.075V/Rsense(ADin)]*[VCLS/VREF]
Rsense(ADin)=0.02 ohm
VCLS= 3.683V
=> Iin(max)=3.27A
=> Constant Power = 19 * 3.27 = 62.13W
=> R5708=10K,R5714=68.1K
Charge Current Ichg = [0.075V/Rsense(CHG)]*[VICTL/3.6V]
Rsense(CHG)=0.025 ohm
VICTL = 3.612V => Ichg = 2.51A
VICTL = 1.687V => Ichg = 1.4A
Vbatt = Cell * (Vref +[(VCTL-1.6V) / 9.52])
VCTL= 1.594V
=> Vbatt = 4.2V (4.20186V)
Mode pin : Vmode > 2.8V (tie to LDO pin) ----> 4 Cells
2.0 > Vmode > 1.6V (floating) ---> 3 Cells
0.8 > Vmode (tie to GND) ----> Learning mode
VICTL < 0.8V or DCIN < 7V -->Charger Disable
Precharge current=150mA
VICTL_pre-2p= 0.188V => Ichg =157mA
VICTL_pre-1p= 0.179V => Ichg = 149mA
LDO : 5.4V
REF : 4.2235V
MAX8725_LDO
MAX8725_REF
BATSEL_2P#
PRECHG
CHG_EN#
AC_APR_UC
BAT_LEARN
+5VCHG
+3VA
PKPRES#
AD_IINP
CHG_CCS
BATSEL_3S#
(3S#/4S)
PQ5705 2N7002
PQ5706 2N7002
PQ5707 2N7002
PQ5708 UMC4N
PQ5709 2N7002
PQ5710 2N7002
PQ5703 2N7002
PQ5720 2N7002
PR5720 470KOhm
PR5721 15KOhm
PR5722 4.7KOhm
PR5718 100KOhm
PR5719 0Ohm
PR5732 0Ohm
PC5716 0.22UF/16V
TS#
<< Kennedy_Zhang >>
Title : POWER_CHARGER
Engineer: Anny
Project Name X51RL
Size Custom
Rev 2.0
Date: Tuesday, July 03, 2007
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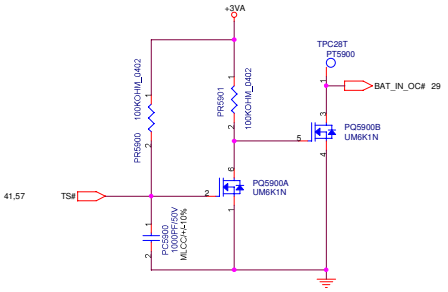
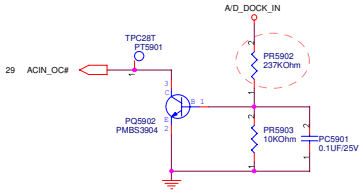
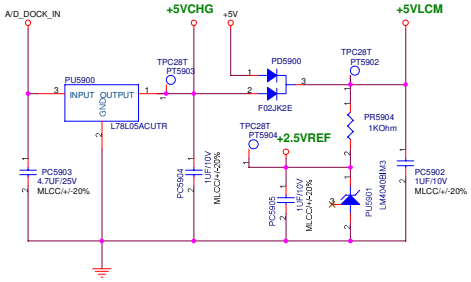
BATTERY IN DETECT



ADAPTER IN DETECT



+5VLCM, +5VCHG & +2.5VREF



Title : POWER_DETECT		
<OrgName>	Engineer: Anny	
Size: Custom	Project Name: X51RL	Rev: 2.0
Date: Tuesday, July 03, 2007	Sheet 59 of 63	

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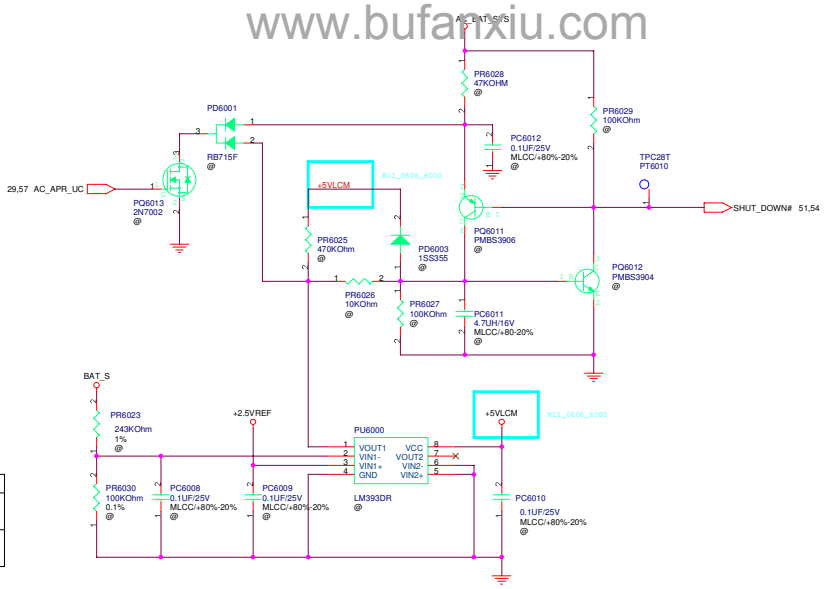
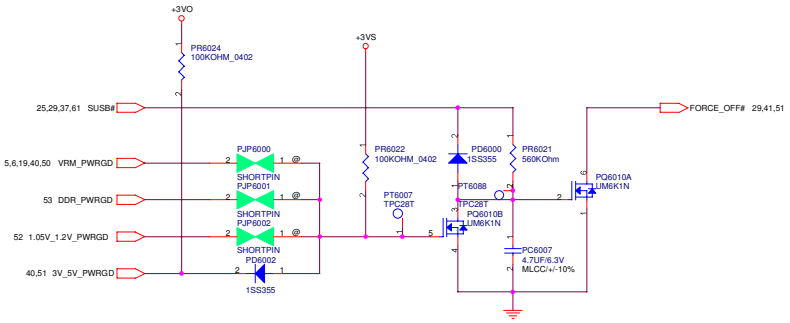


	8.575V	11.625V
R6023	243KOhm 10G2132433130 30 1%	365KOhm 10G2133653130 10 1%
R6024	100KOhm 10G2131003230 10 0.1%	100KOhm 10G2131003230 10 0.1%

POWER GOOD DETECTER



TPC28T	PT6003	VRM_PWRGD
TPC28T	PT6004	DDR_PWRGD
TPC28T	PT6005	3V_5V_PWRGD
TPC28T	PT6006	1.05V_1.2V_PWRGD

Title : POWER_PROTECT			
<OrgName>	Engineer: Anny		
Size: Custom	Project Name: X51RL		Rev: 2.0
Date: Tuesday, July 03, 2007	Sheet 60 of 63		

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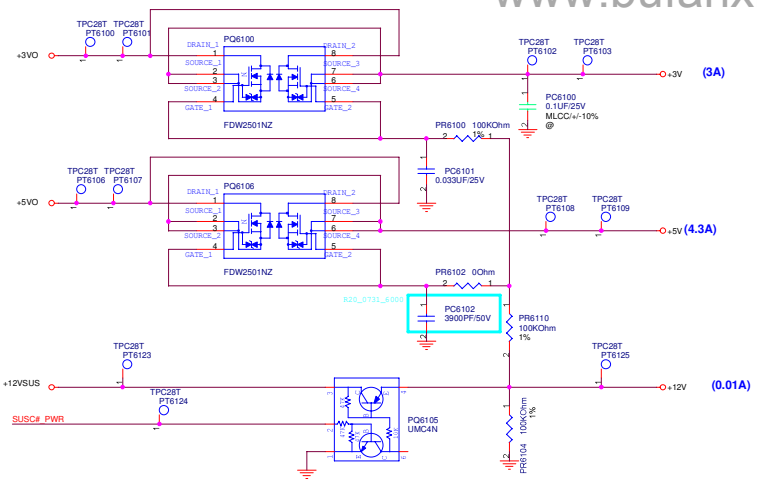
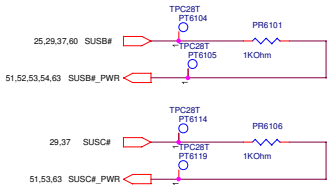
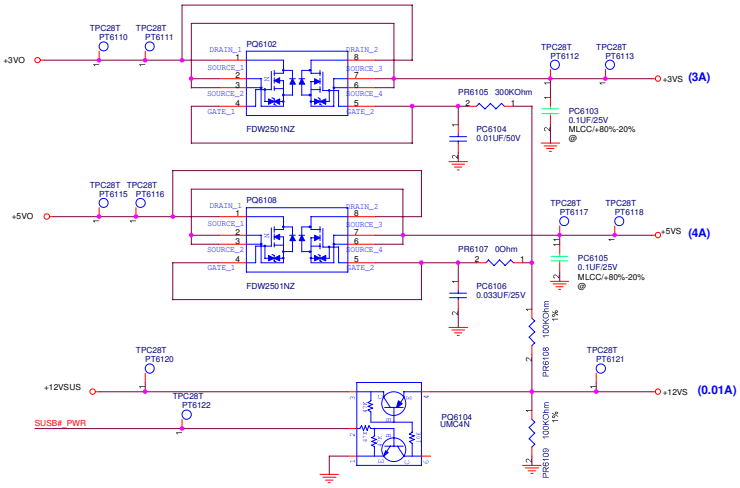
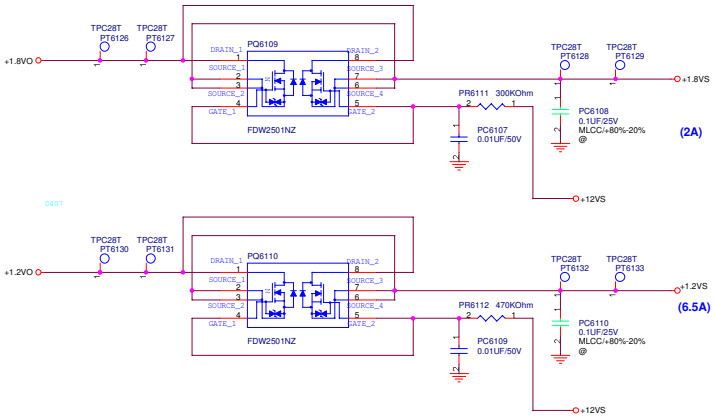
SUSC#_PWR POWER





SUSB#_PWR POWER





ASUS	Title : POWER_LOAD SWITCH		
<OrgName>	Engineer: Anny		
Size: Custom	Project Name: X51RL		Rev: 2.0
Date: Tuesday, July 03, 2007	Sheet 61 of 63		

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AC_BAT_SYS → AC_BAT_SYS 12,41,50,51,52,53,54,57,60
+3VA → +3VA 12,17,29,38,40,54,57,59
+5VA → +5VA 9,37,51,54
+5VO → +5VO 51,52,53,61
+3VO → +3VO 51,52,60,61
+3VSUS → +3VSUS 6,17,19,20,23,25,29,34,40,51
+5VSUS → +5VSUS 30,51
+3V → +3V 17,25,26,27,31,35,37,42,43,44,61
+3VS → +3VS 2,4,5,9,12,13,14,15,17,18,19,20,21,22,23,25,26,28,29,31,32,33,34,37,39,40,42,43,50,52,60,61

+12VSUS → +12VSUS 51,61
+12V → +12V 23,36,37,54,61
+12VS → +12VS 12,33,37,61

+5V → +5V 12,25,30,36,37,38,44,59,61
+5VS → +5VS 4,13,20,22,23,28,29,30,37,38,50,61

+1.2VO → +1.2VO 52,61
+1.2VSUS → +1.2VSUS 20,52
+1.2VS → +1.2VS 6,7,9,10,20,37,61
+1.8VO → +1.8VO 53,61
+1.8V → +1.8V 8,10,14,15,16,37,53

+VCCP → +VCCP 3,5,6,10,17,19,20,52

+0.9VS → +0.9VS 16,37,53
BAT → BAT 57
+5VCHG → +5VCHG 57,59
+5VLCM → +5VLCM 59,60
+2.5VREF → +2.5VREF 54,59,60
+VCORE → +VCORE 3,50

BAT_CON → BAT_CON 41,57

FOR POWER TEST

+3VA → PJP6300 (1 2 2) SGL_JUMP @ → CPU_VRON_PWR 50
+3VA → PJP6301 (1 2 2) SGL_JUMP @ → SUSB#_PWR → SUSB#_PWR 51,52,53,54,61
+3VA → PJP6302 (1 2 2) SGL_JUMP @ → SUSC#_PWR → SUSC#_PWR 51,53,61
+3VA → PJP6303 (1 2 2) SGL_JUMP @ → VSUS_ON_PWR → VSUS_ON_PWR 51

Title : POWER_SIGNAL		
<OrgName>	Engineer: Anny	
Size: Custom	Project Name: X51RL	Rev: 2.0
Date: Tuesday, July 03, 2007	Sheet 63 of 63	

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R2.0

Item	Before	After	Reason	Owner	Date
R20_1109_50		Add PCE5001 PCE5005, PQ5002, PQ5004, PQ5005 and PQ5007	VCORE:CPU upgrade to merom reflash		2006.11.09
R20_1109_50	9.31K	11K	VCORE: PR5030 modify to 11K to Increase OCP.		2006.11.09
R20_1109_57	PR5712 and PQ5705 were unmounted	PR5712:36.5K and PQ5705 was mounted.	Charger: Modify PR5712 and PQ5705 for 3S1P select.		2006.11.09

Title : POWER_PIC

<OrgName> Engineer:

Size	Project Name	Rev
Custom	X51RL	2.0

Date: Monday, May 21, 2007 Sheet 64 of 63

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T12Rv Block Diagram V2.0

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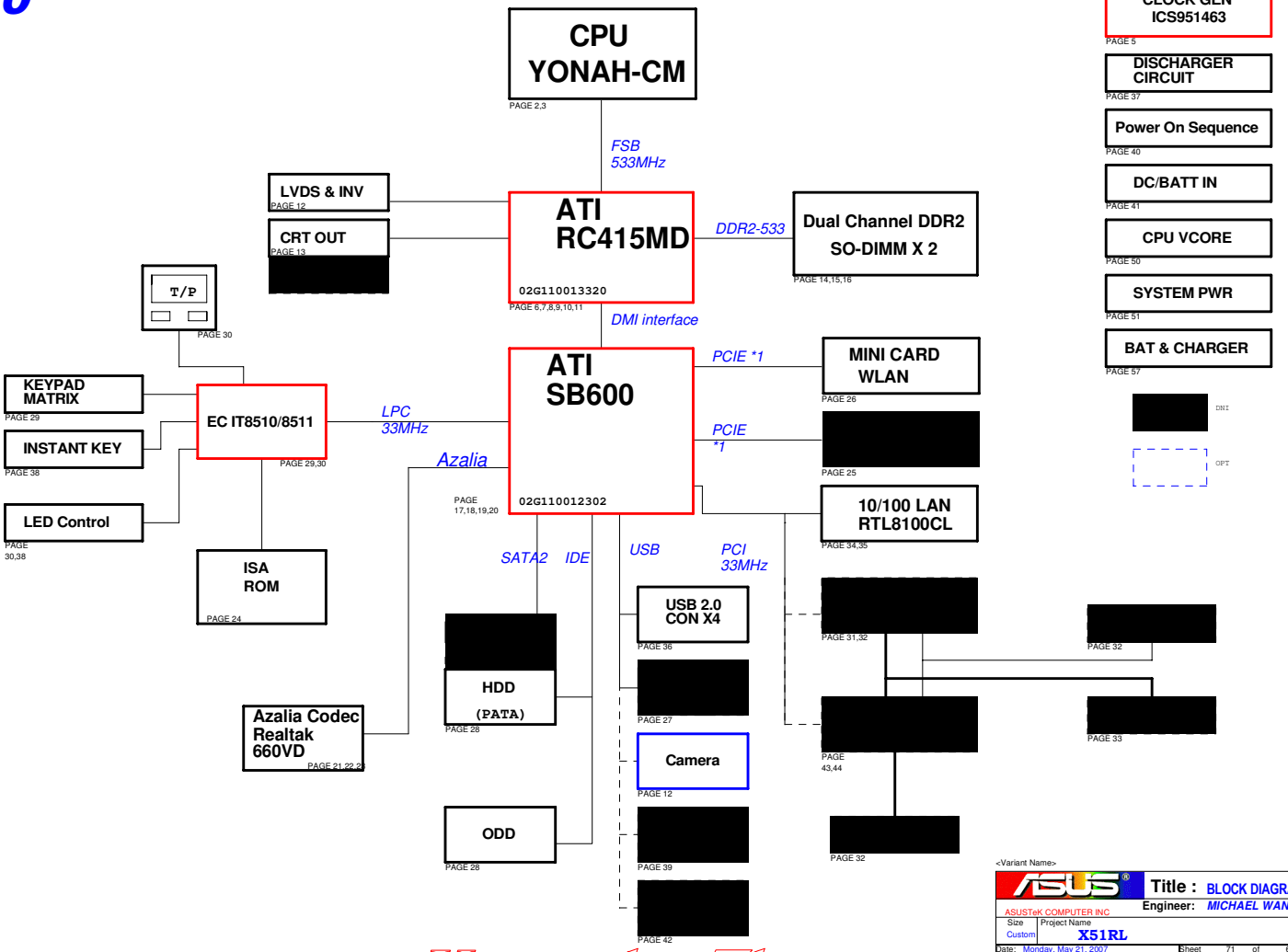

<Variant Name>

ASUSTeK COMPUTER INC

Title : BLOCK DIAGRAM

Engineer: MICHAEL WANG

Size	Project Name	Rev
Custom	X51RL	2.0

Date: Monday, May 21, 2007 Sheet 71 of 63

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T12Rg Block Diagram V2.0

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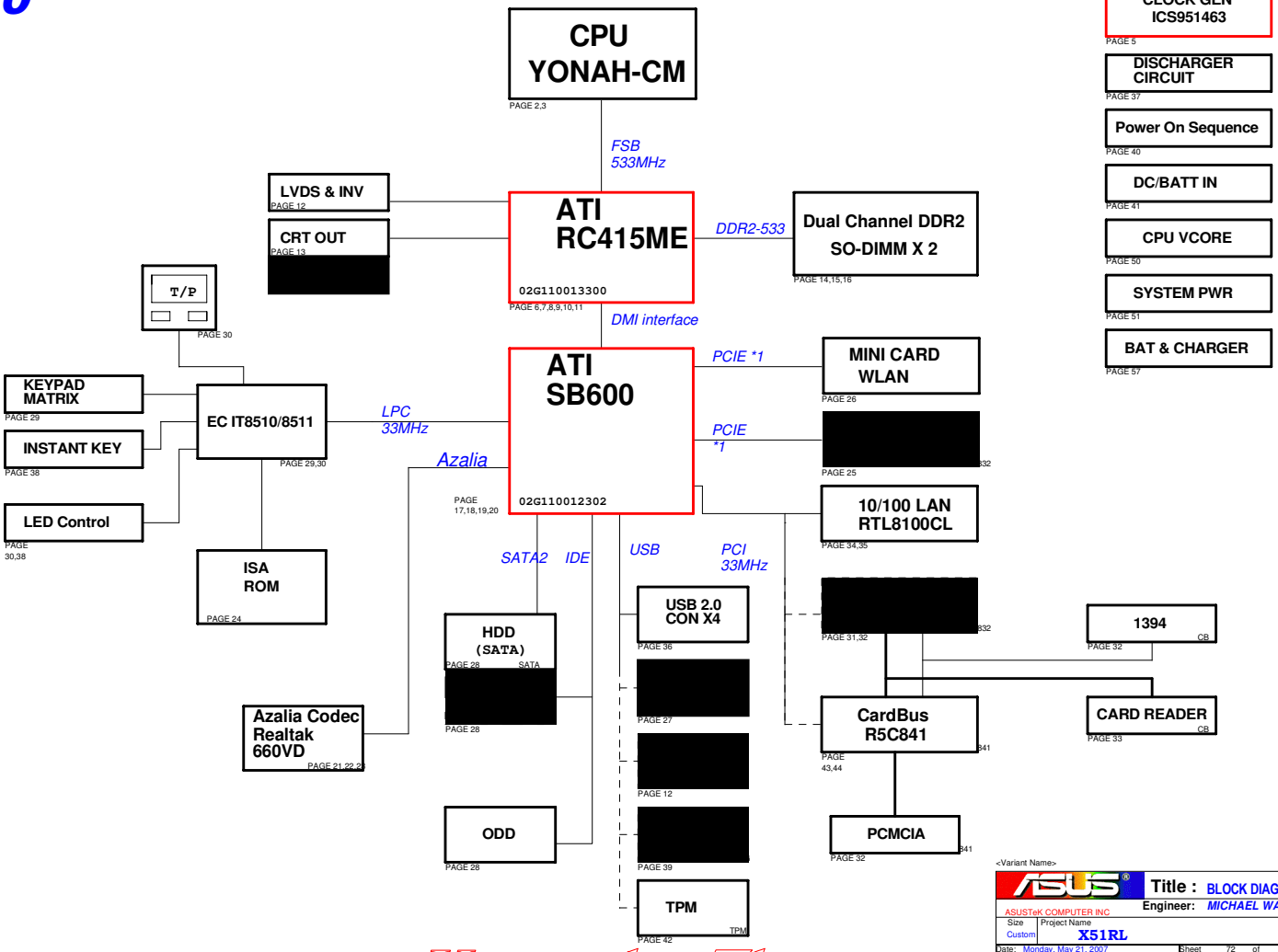

<Variant Name>

ASUSTeK COMPUTER INC

Title : BLOCK DIAGRAM

Engineer: MICHAEL WANG

Size	Project Name	Rev
Custom	X51RL	2.0

Date: Monday, May 21, 2007 Sheet 72 of 63

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X51 Block Diagram V2.0

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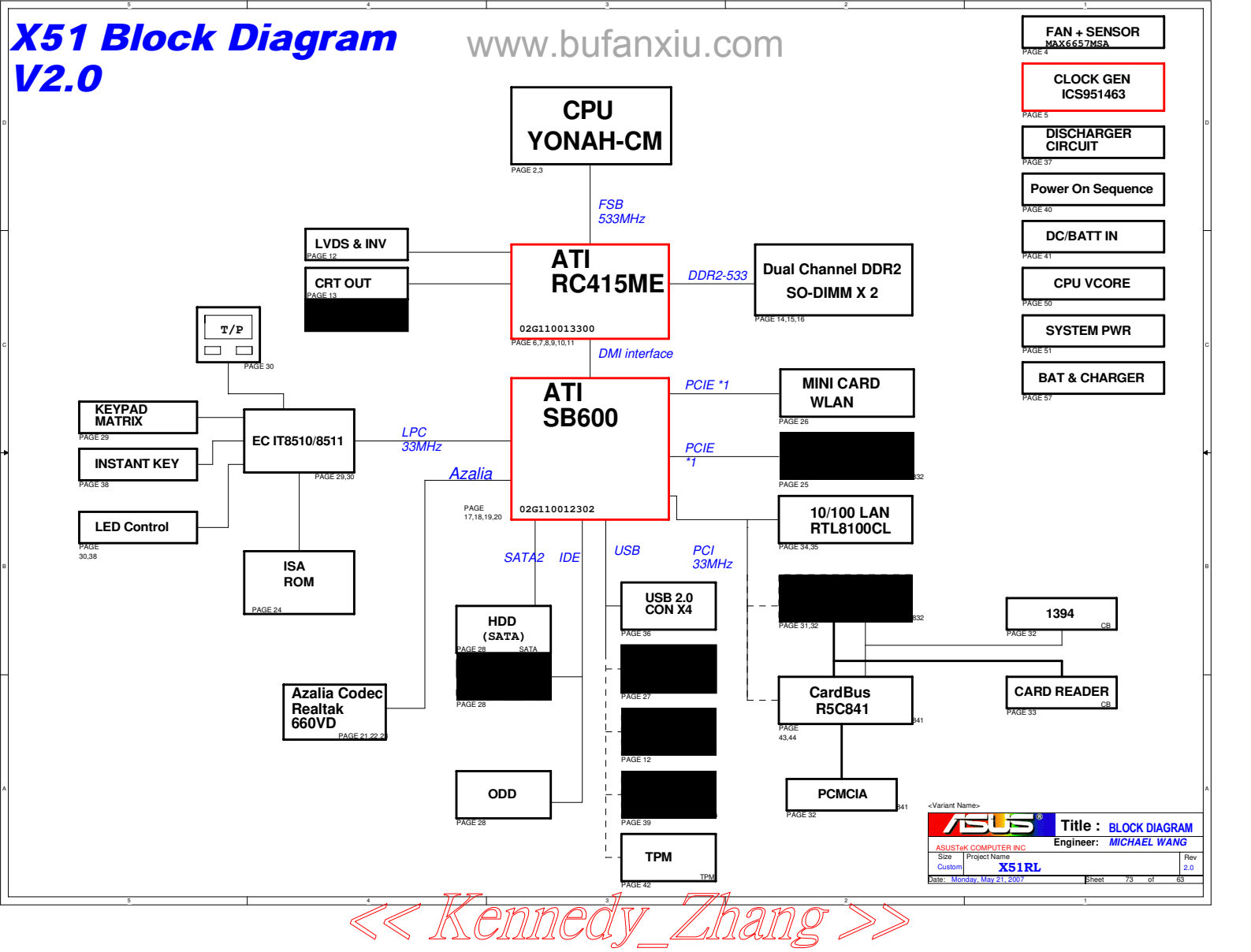

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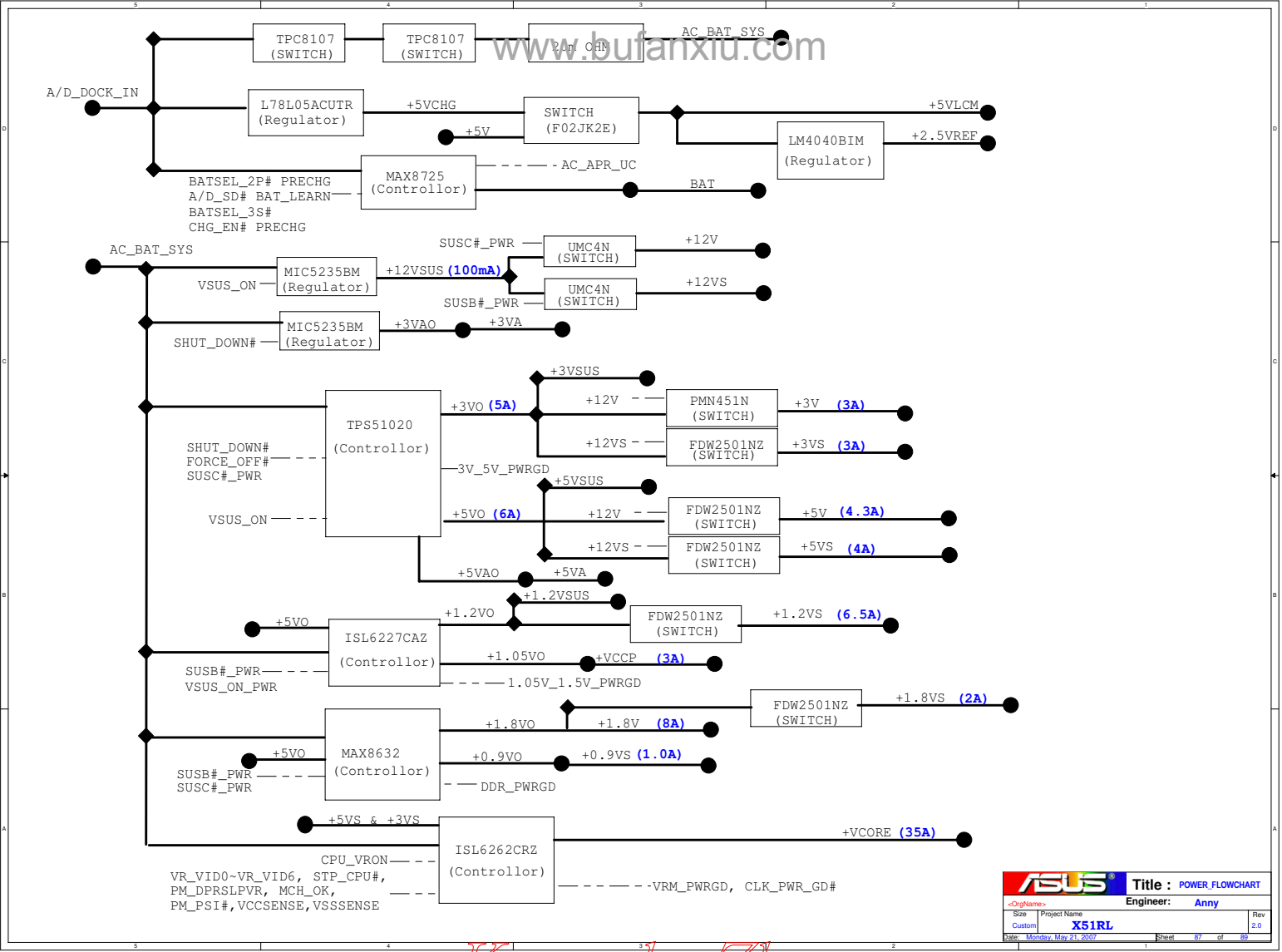

Title : POWER_FLOWCHART		
<OrgName>	Engineer: Anny	
Size: Custom	Project Name: X51RL	Rev: 2.0
Date: Monday, May 21, 2007	Sheet 87 of 89	

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