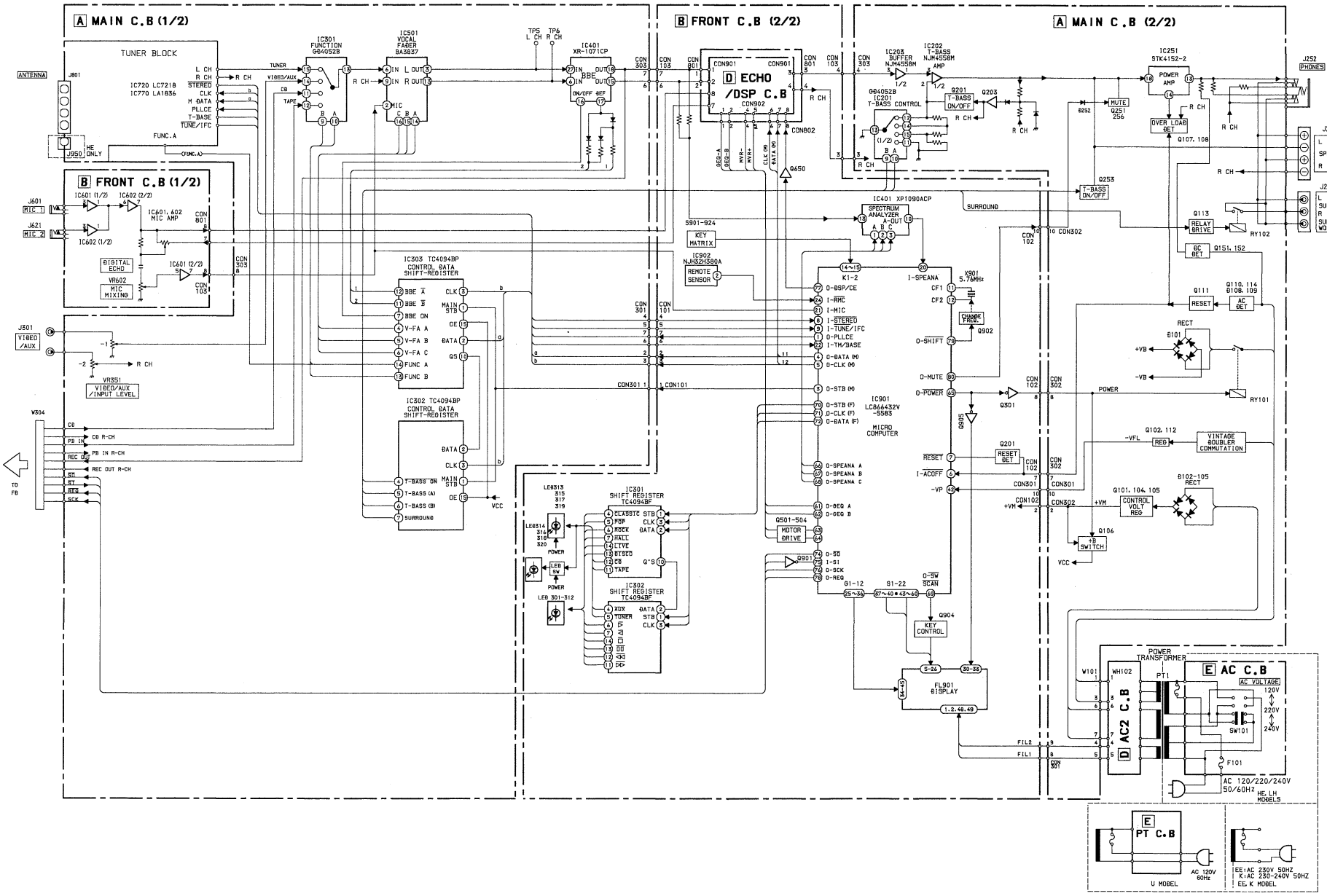
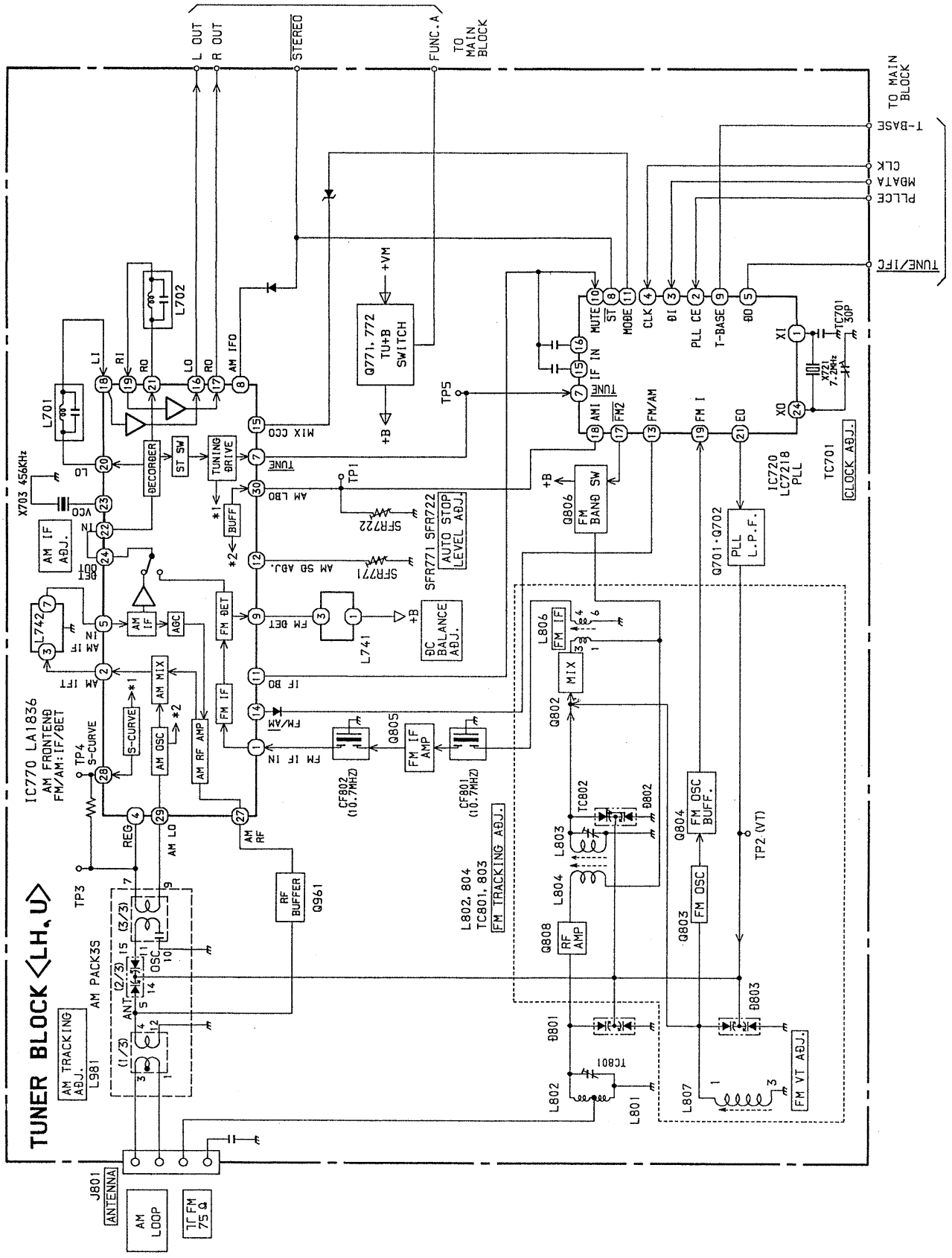
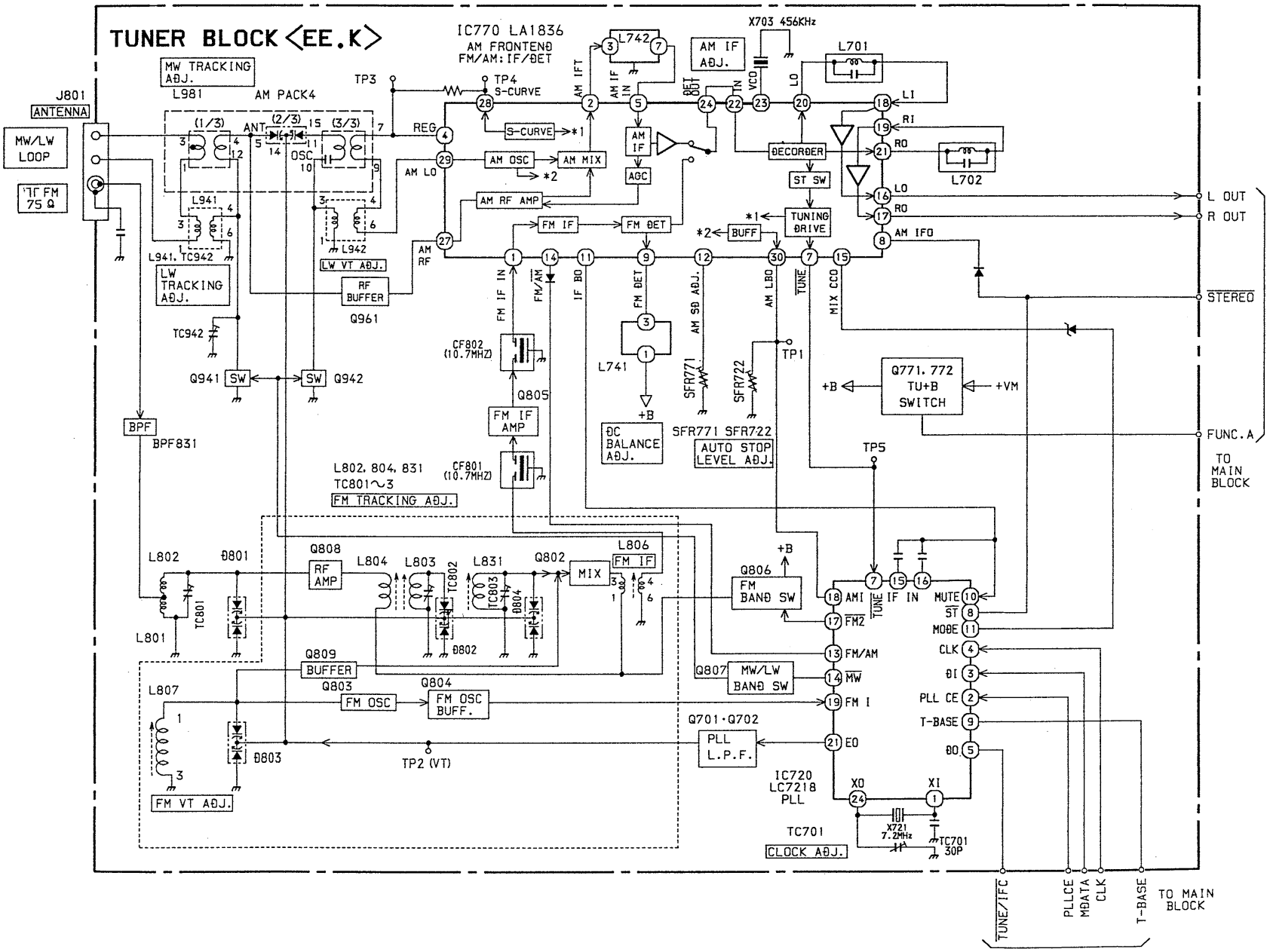
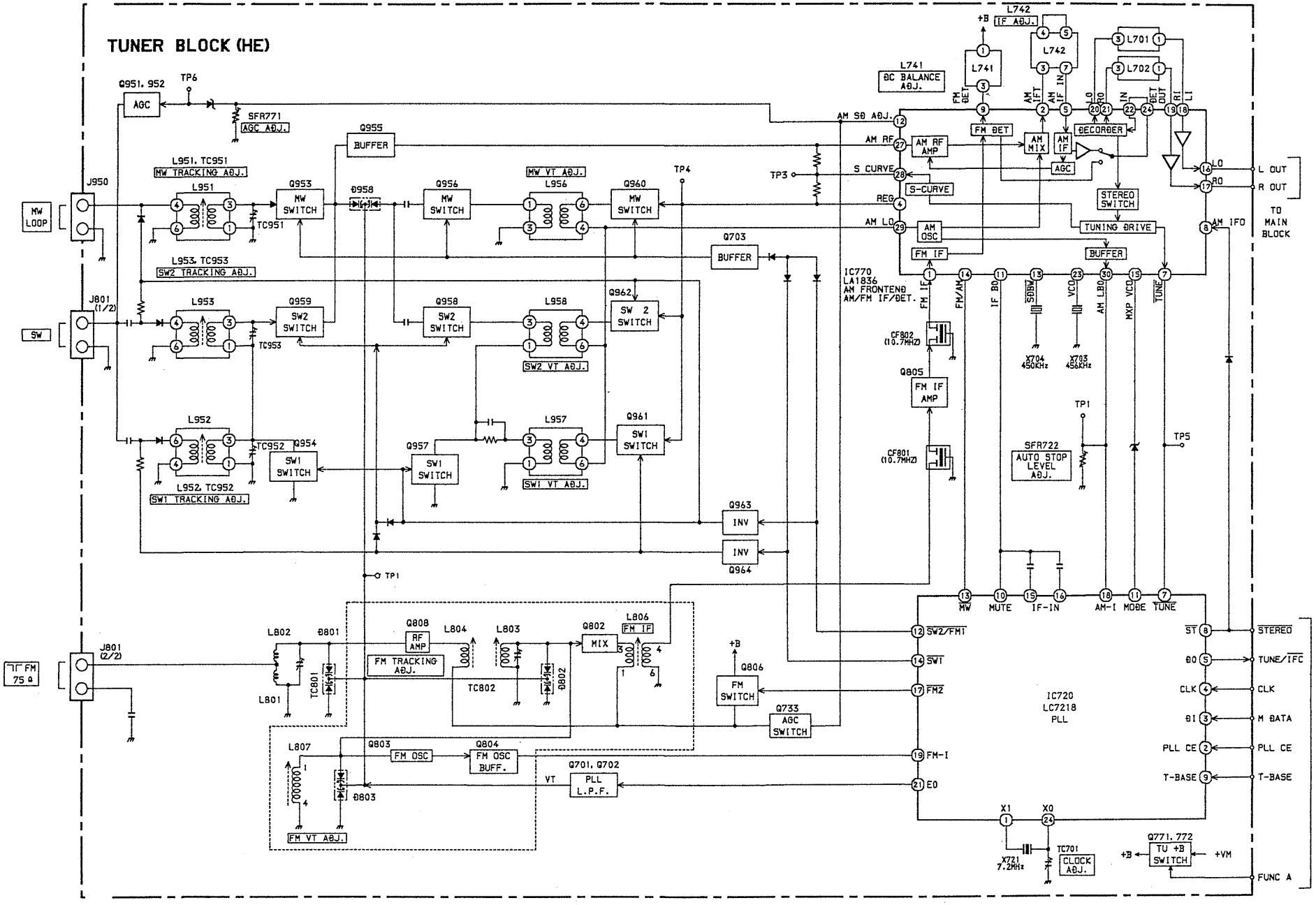
BLOCK DIAGRAM – 1 (MAIN)

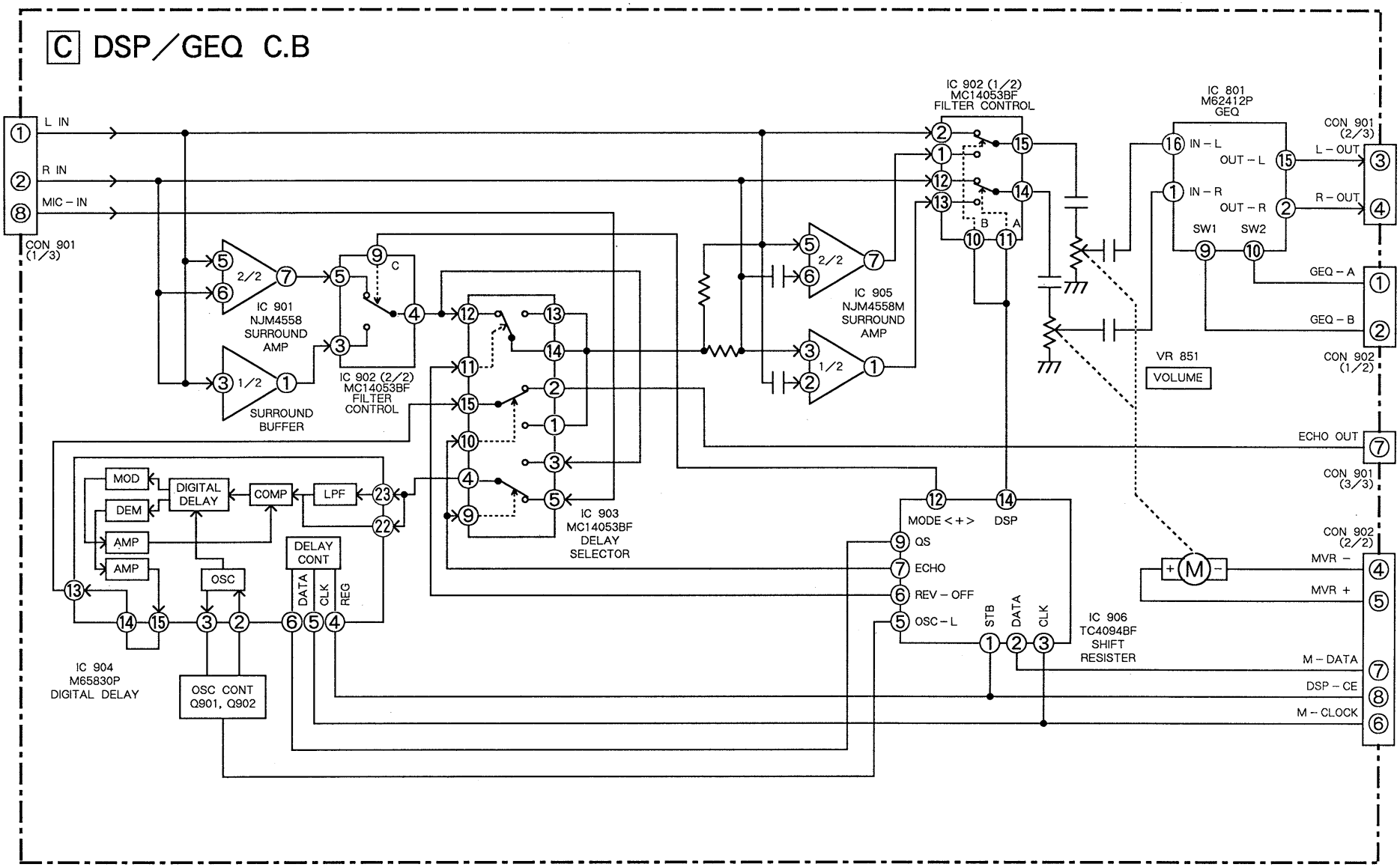


BLOCK DIAGRAM – 2 (TUNER : LH, U)

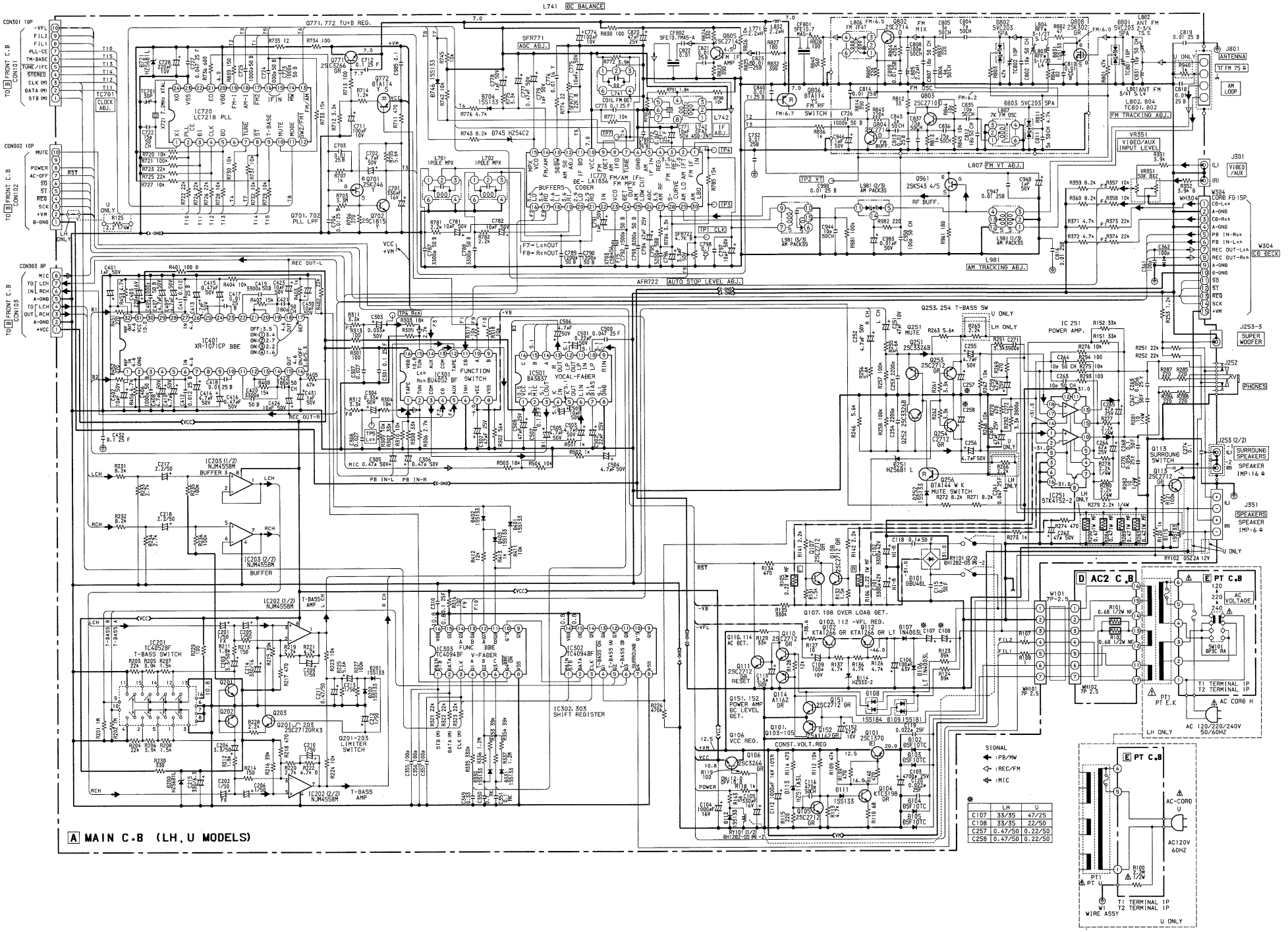



TUNER BLOCK <EE.K>
IC770 LA1836
AM FRONTEND
FM/AM: IF/DET
X703 456KHz
L742
AM IF ADJ.
L701
L702
MW TRACKING ADJ.
L981
AM PACK4
J801
ANTENNA
MW/LW LOOP
FM 75Ω
TP3
TP4 S-CURVE
S-CURVE
AM OSC
AM MIX
AM IF
AGC
AM RF AMP
FM IF
FM DET
BUFF
TUNING DRIVE
DECORDER
ST SW
AM IFO
L941
L942
L941, TC942
LW TRACKING ADJ.
LW VT ADJ.
RF BUFFER
Q961
TC942
Q941 SW
SW Q942
BPF
BPF831
CF802 (10.7MHZ)
CF801 (10.7MHZ)
Q805
FM IF AMP
L802, 804, 831
TC801~3
FM TRACKING ADJ.
L741
DC BALANCE ADJ.
SFR771
SFR722
SFR771 SFR722
AUTO STOP LEVEL ADJ.
TP1
TP5
Q771, 772
TU+B SWITCH
+B
+VM
L OUT
R OUT
STEREO
FUNC.A
TO MAIN BLOCK
L802
D801
Q808
RF AMP
L804
L803
L831
Q802
MIX
L806
FM IF
TC801
TC802
TC803
D804
D802
L801
Q809
BUFFER
Q803
L807
FM OSC
Q804
FM OSC BUFF.
D803
TP2 (VT)
FM VT ADJ.
Q806
FM BAND SW
Q807
MW/LW BAND SW
Q701·Q702
PLL L.P.F.
IC720
LC7218
PLL
XO
XI
X721
7.2MHz
TC701
30P
TC701
CLOCK ADJ.
TUNE/IFC
PLLCE
MDATA
CLK
T-BASE
TO MAIN BLOCK

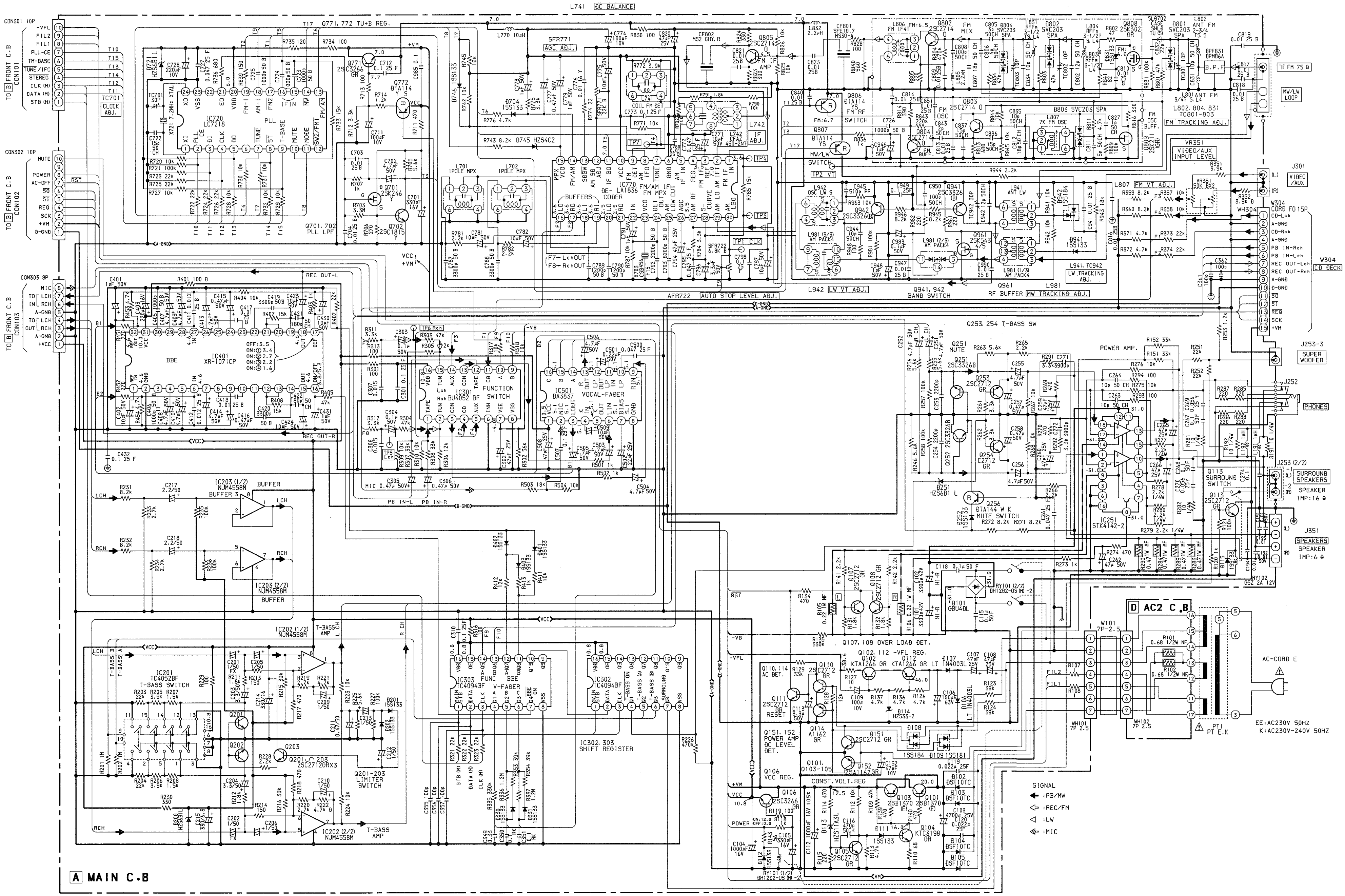

TUNER BLOCK (HE)
AGC
Q951, 952
TP6
SFR771
AGC ADJ.
BUFFER
Q955
L951, TC951
MW TRACKING ADJ.
MW VT ADJ.
J950
MW LOOP
Q953
MW SWITCH
D958
Q956
L956
Q960
TP4
TP3
L953, TC953
SW2 TRACKING ADJ.
J801 (1/2)
SW
L953
Q959
SW2 SWITCH
Q958
L958
Q962
SW 2 SWITCH
SW2 VT ADJ.
L952
TC952
Q954
SW1 SWITCH
Q957
L957
Q961
SW1 VT ADJ.
L952, TC952
SW1 TRACKING ADJ.
Q703
BUFFER
Q963
INV
Q964
TP1
IC770
LA1836
AM FRONTEND
AM/FM IF/DET.
AM SD ADJ.
AM RF
AM RF AMP
S CURVE
S-CURVE
REG
AM LO
AM OSC
FM IF
L741
DC BALANCE ADJ.
L742
IF ADJ.
L701
L702
FM DET
AM MIX
AM IF
AGC
DECORDER
STEREO SWITCH
TUNING DRIVE
BUFFER
AM IFO
L OUT
R OUT
TO MAIN BLOCK
CF802 (10.7MHZ)
CF801 (10.7MHZ)
Q805
FM IF AMP
X704 450KHz
X703 456KHz
SFR722
AUTO STOP LEVEL ADJ.
TP5
J801 (2/3)
FM 75Ω
L802
D801
Q808
RF AMP
FM TRACKING ADJ.
L804
L803
Q802
MIX
L806
FM IF
TC802
TC801
D802
L801
Q806
FM SWITCH
Q733
AGC SWITCH
L807
Q803
FM OSC
Q804
FM OSC BUFF.
D803
FM VT ADJ.
Q701, Q702
PLL L.P.F.
VT
IC720
LC7218
PLL
SW2/FM1
SW1
FM2
FM-I
EO
MW
MUTE
IF-IN
AM-I
MODE
TUNE
ST
DO
CLK
DI
PLL CE
T-BASE
STEREO
TUNE/IFC
CLK
M DATA
PLL CE
T-BASE
FUNC A
TO MAIN BLOCK
X1
XO
X721 7.2MHz
TC701 CLOCK ADJ.
Q771, 772 TU +B SWITCH
+B
+VM


C DSP/GEQ C.B
L IN
R IN
MIC – IN
CON 901 (1/3)
IC 901 NJM4558 SURROUND AMP
SURROUND BUFFER
IC 902 (2/2) MC14053BF FILTER CONTROL
IC 902 (1/2) MC14053BF FILTER CONTROL
IC 905 NJM4558M SURROUND AMP
IC 801 M62412P GEQ
IN – L
IN – R
OUT – L
OUT – R
SW1
SW2
CON 901 (2/3)
L – OUT
R – OUT
GEQ – A
GEQ – B
CON 902 (1/2)
VR 851
VOLUME
ECHO OUT
CON 901 (3/3)
MOD
DEM
AMP
AMP
DIGITAL DELAY
COMP
LPF
OSC
DELAY CONT
DATA
CLK
REG
IC 903 MC14053BF DELAY SELECTOR
IC 904 M65830P DIGITAL DELAY
OSC CONT Q901, Q902
MODE < + >
DSP
QS
ECHO
REV – OFF
OSC – L
STB
DATA
CLK
IC 906 TC4094BF SHIFT RESISTER
CON 902 (2/2)
MVR –
MVR +
M – DATA
DSP – CE
M – CLOCK

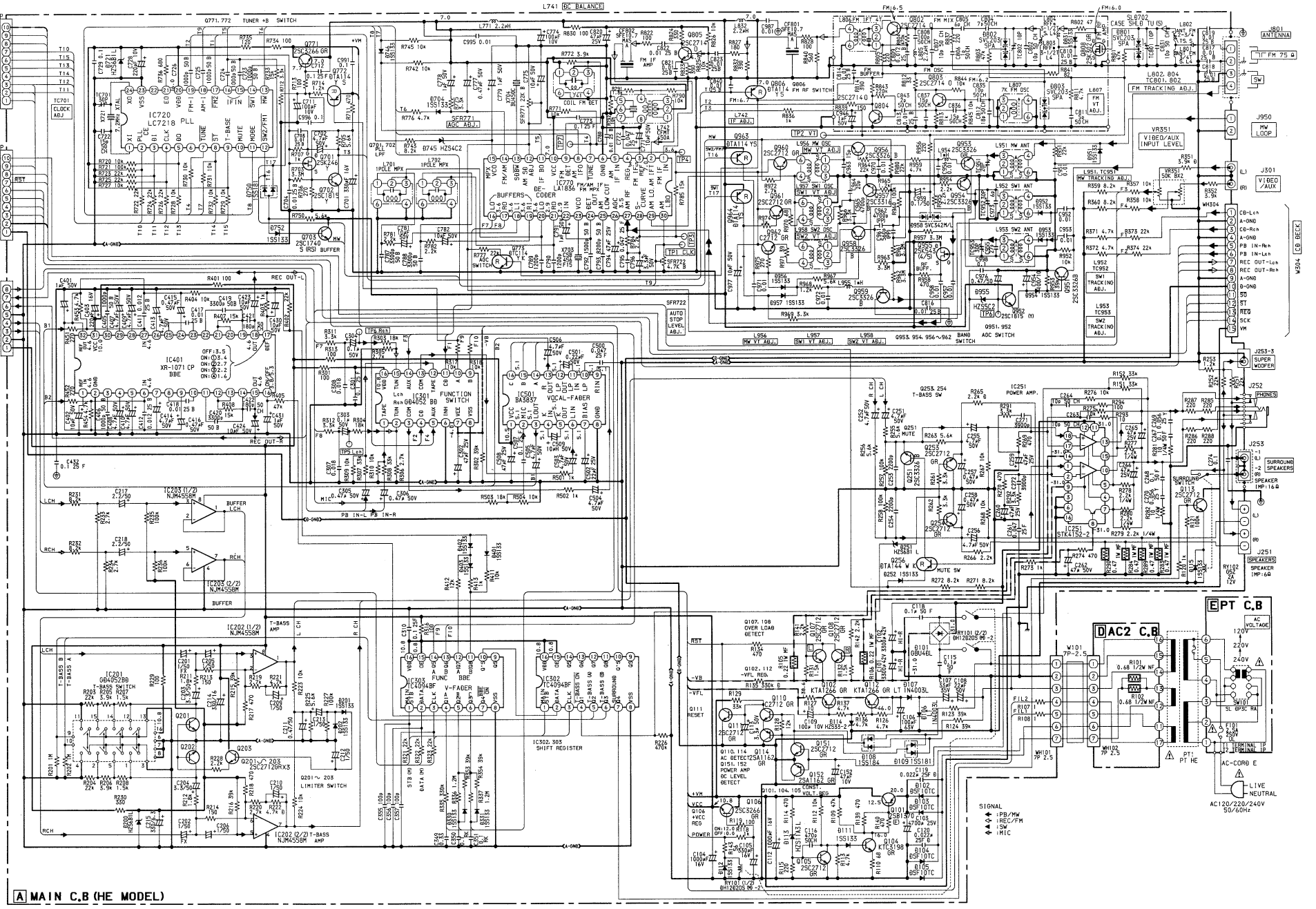
SCHEMATIC DIAGRAM – 1 (MAIN : LH, U)



SCHEMATIC DIAGRAM – 2 (MAIN : EE, K)

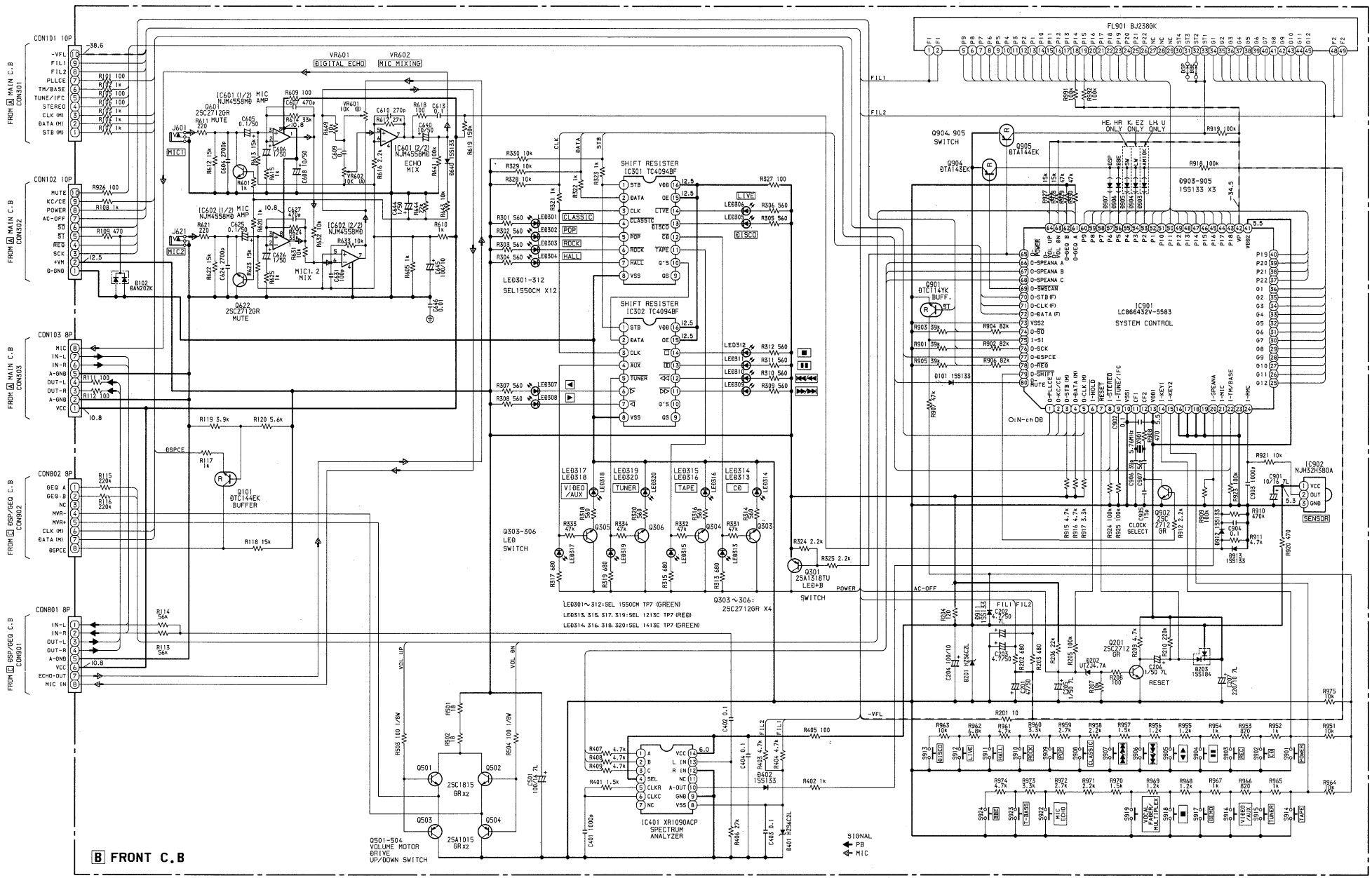


SCHEMATIC DIAGRAM – 3 (MAIN : HE)

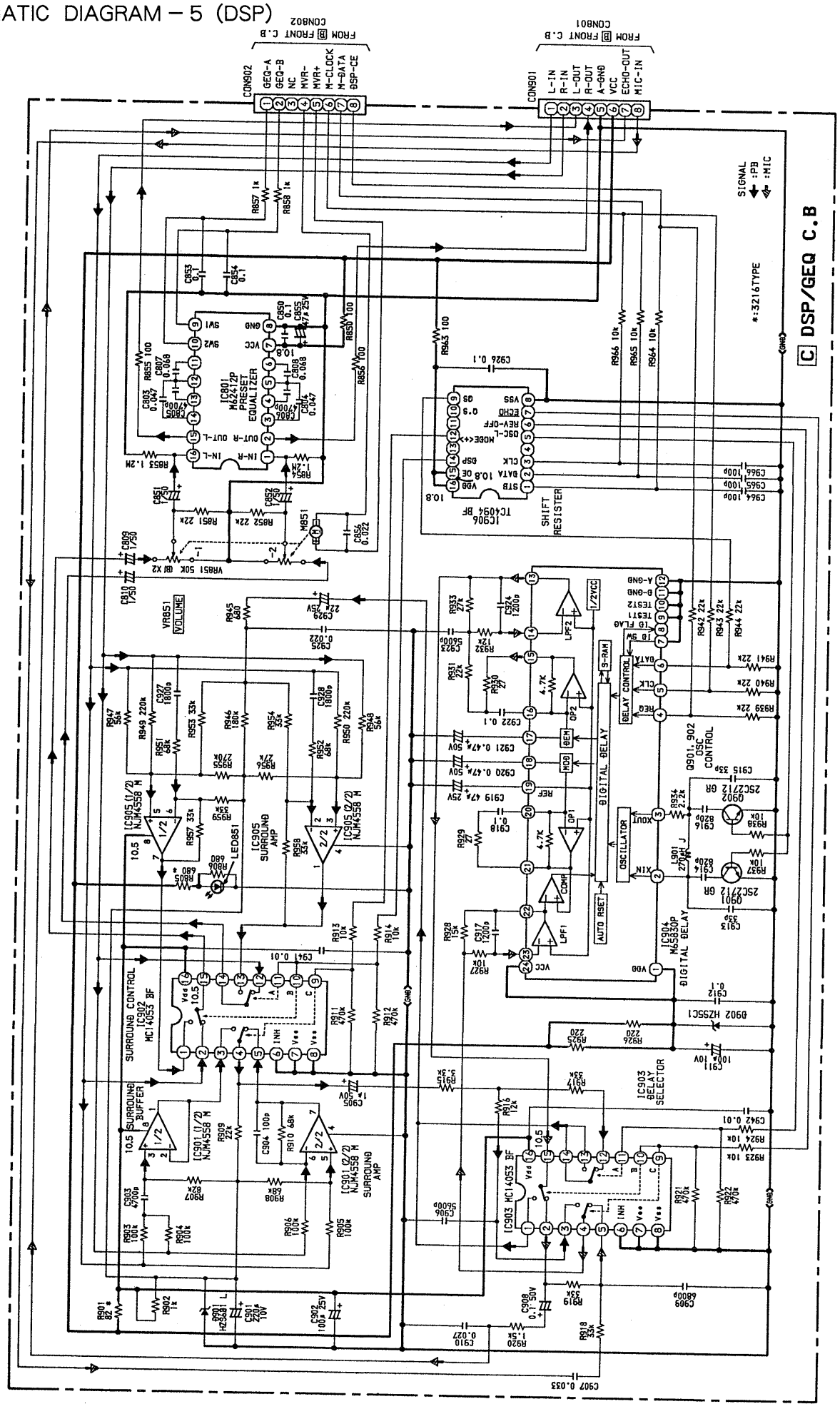


A MAIN C.B (HE MODEL)

SCHEMATIC DIAGRAM – 4 (FRONT)

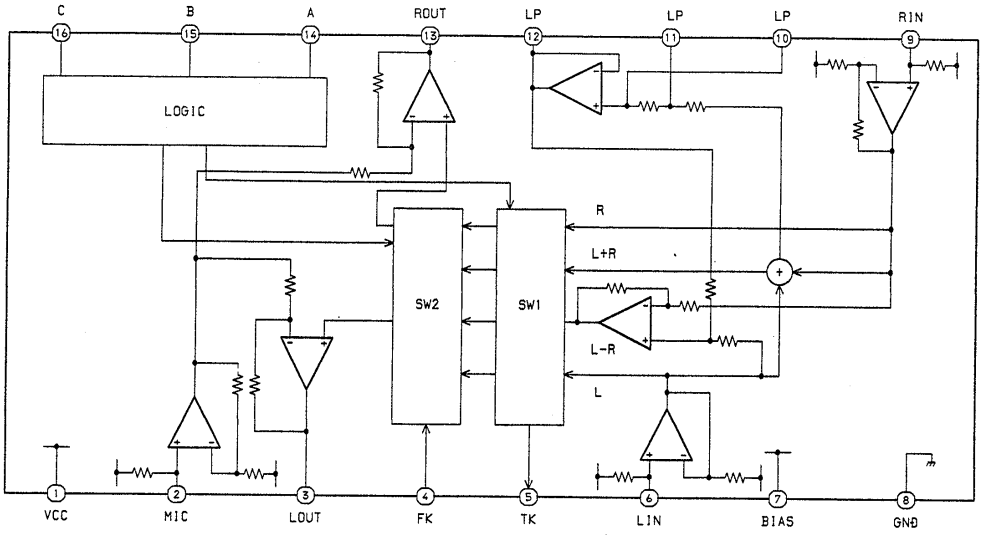


SCHEMATIC DIAGRAM – 5 (DSP)

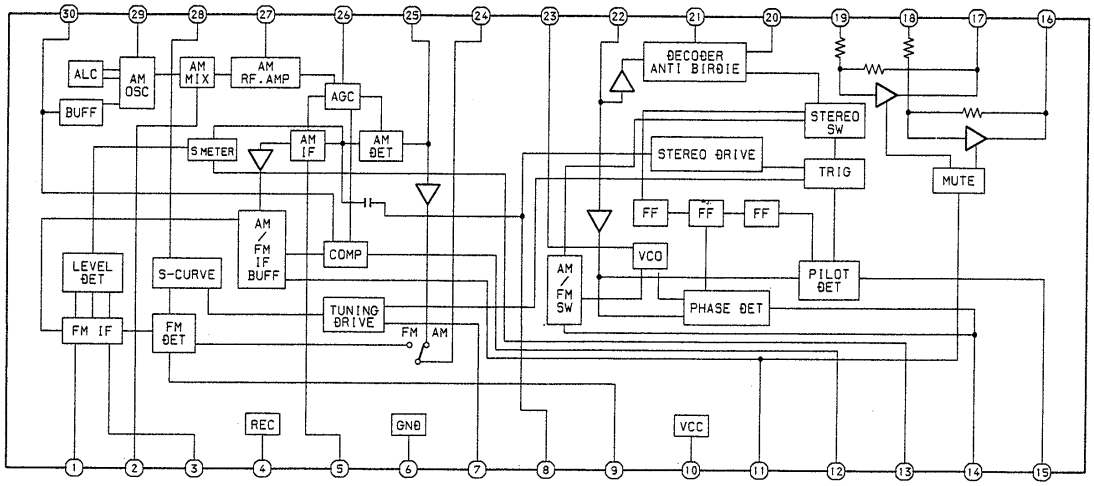


IC BLOCK DIAGRAM

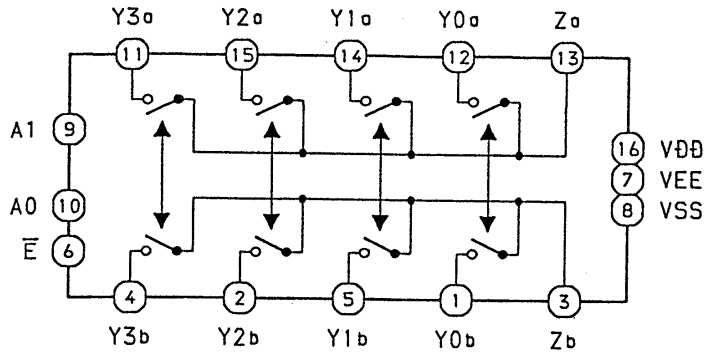
IC,BA3837



IC,LA1836



IC,GD4052



PIN NAMES

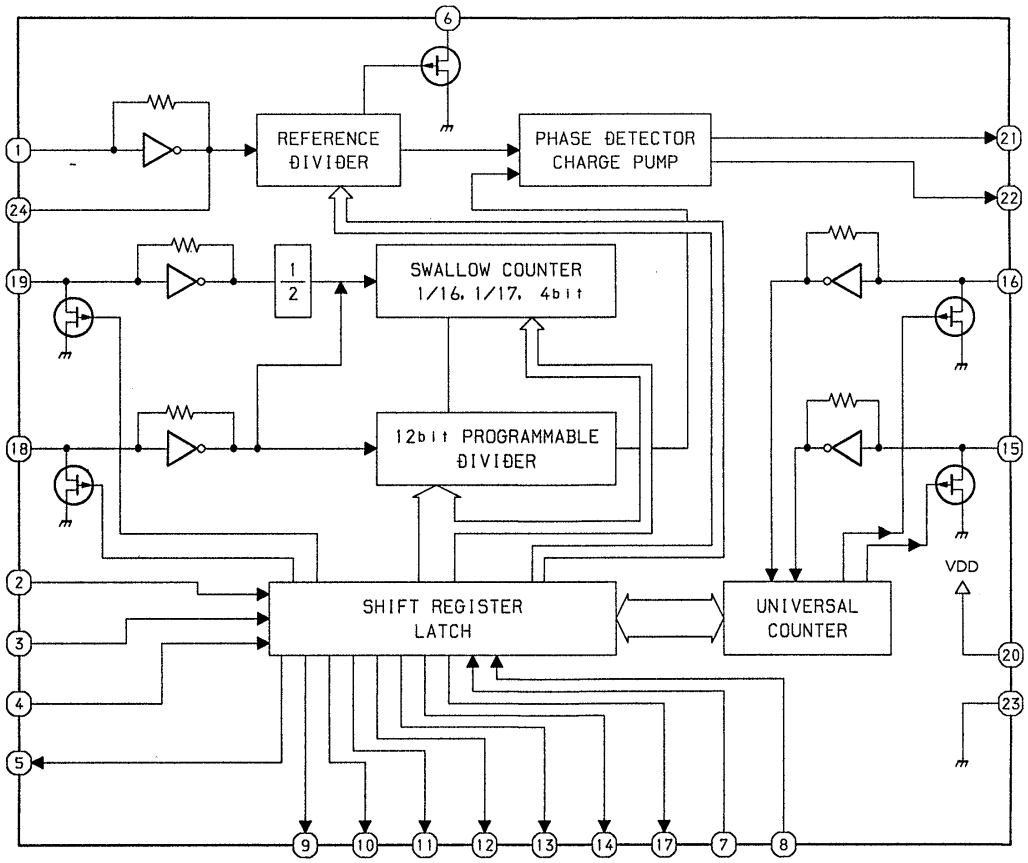
Y0a - Y3a	Independent Inputs/Outputs
Y0b - Y3b	Independent Inputs/Outputs
A1, A1	Address Inputs
$\overline{E}$	Enable Input (Active LOW)
Za, Zb	Common Input/Output

TRUTH TABLE

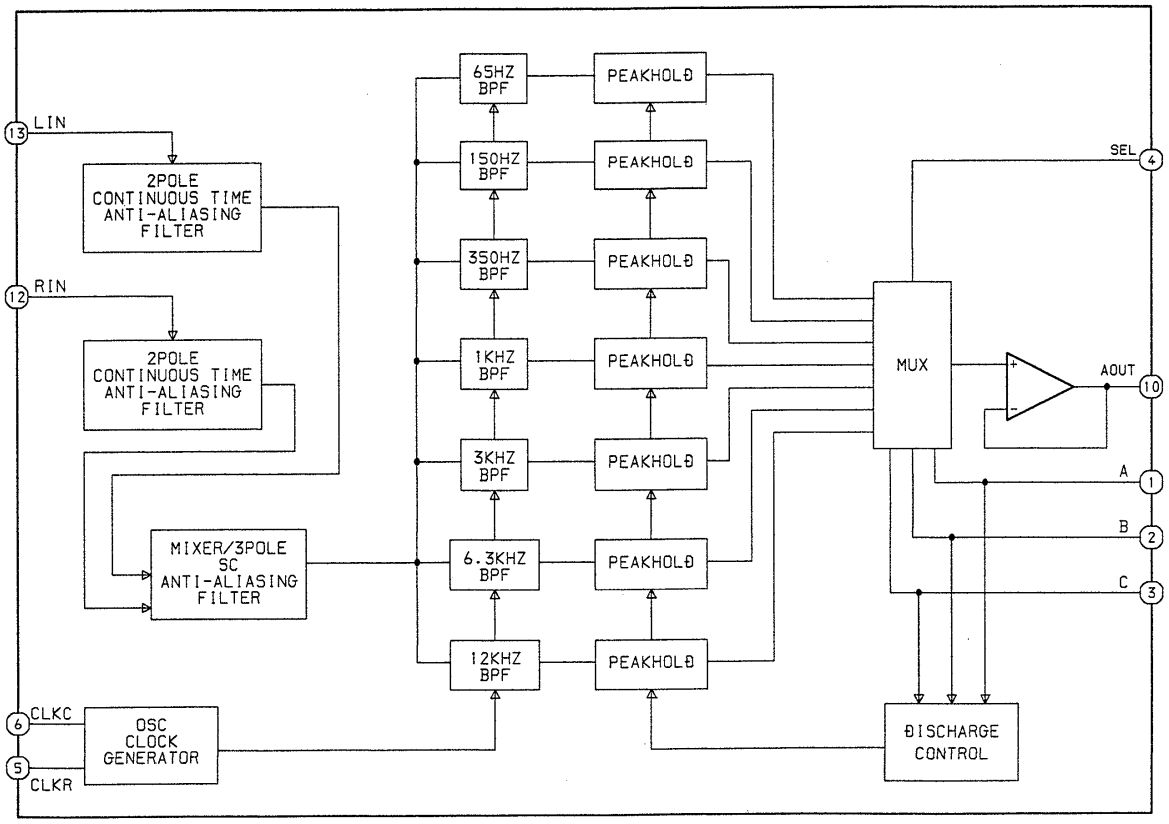
INPUTS			CHANNELS			
E	A1	A0	Y0-Z	Y1-Z	Y2-Z	Y3-Z
L	L	L	ON	OFF	OFF	OFF
L	L	H	OFF	ON	OFF	OFF
L	H	L	OFF	OFF	ON	OFF
L	H	H	OFF	OFF	OFF	ON
H	X	X	OFF	OFF	OFF	OFF

L:LOW Level, H:HIGH Level, X:Don't care

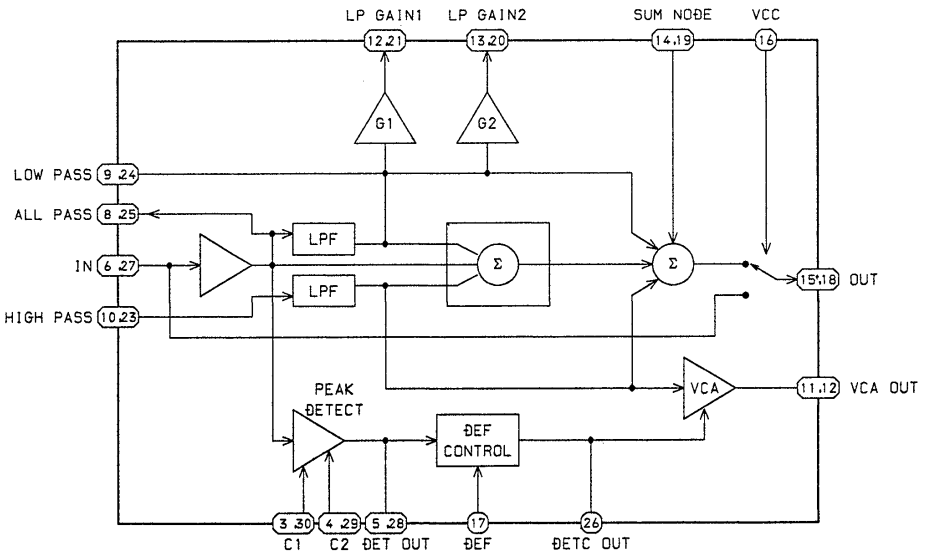
IC,LC7218



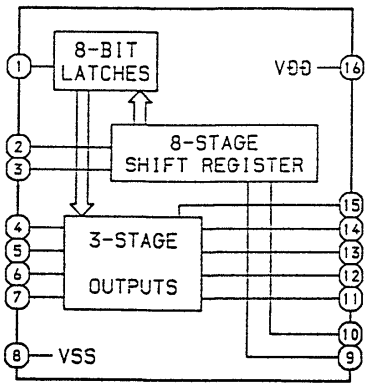
IC,XR1090



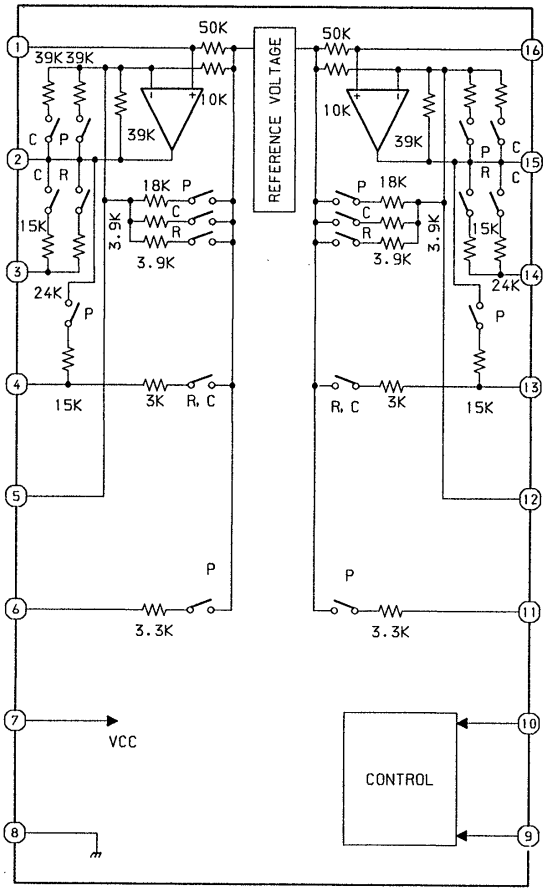
IC,XR1071CP



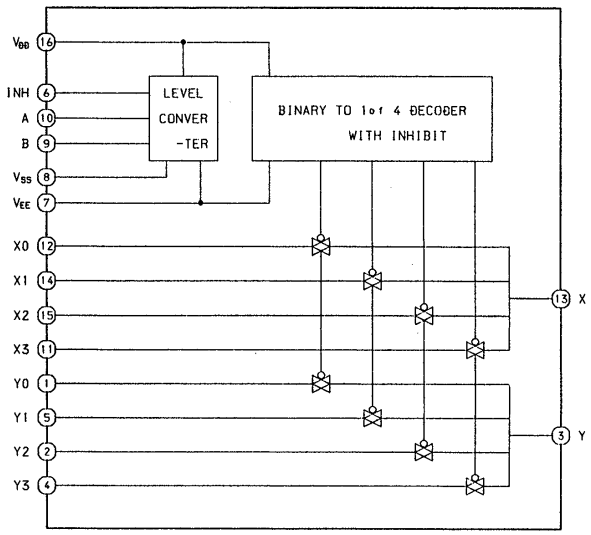
IC,TC4094



IC,M62412P



IC,BU4052BF



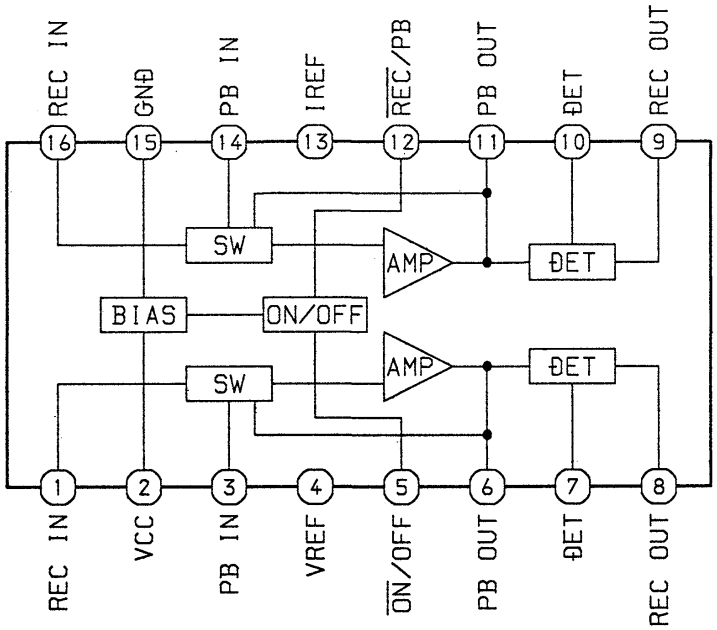
TRUTH TABLE

INHIBIT	A	B	ON SWITCH
L	L	L	X0.Y0
L	H	L	X1.Y1
L	L	H	X2, Y2
L	H	H	X3, Y3
H	×	×	NONE

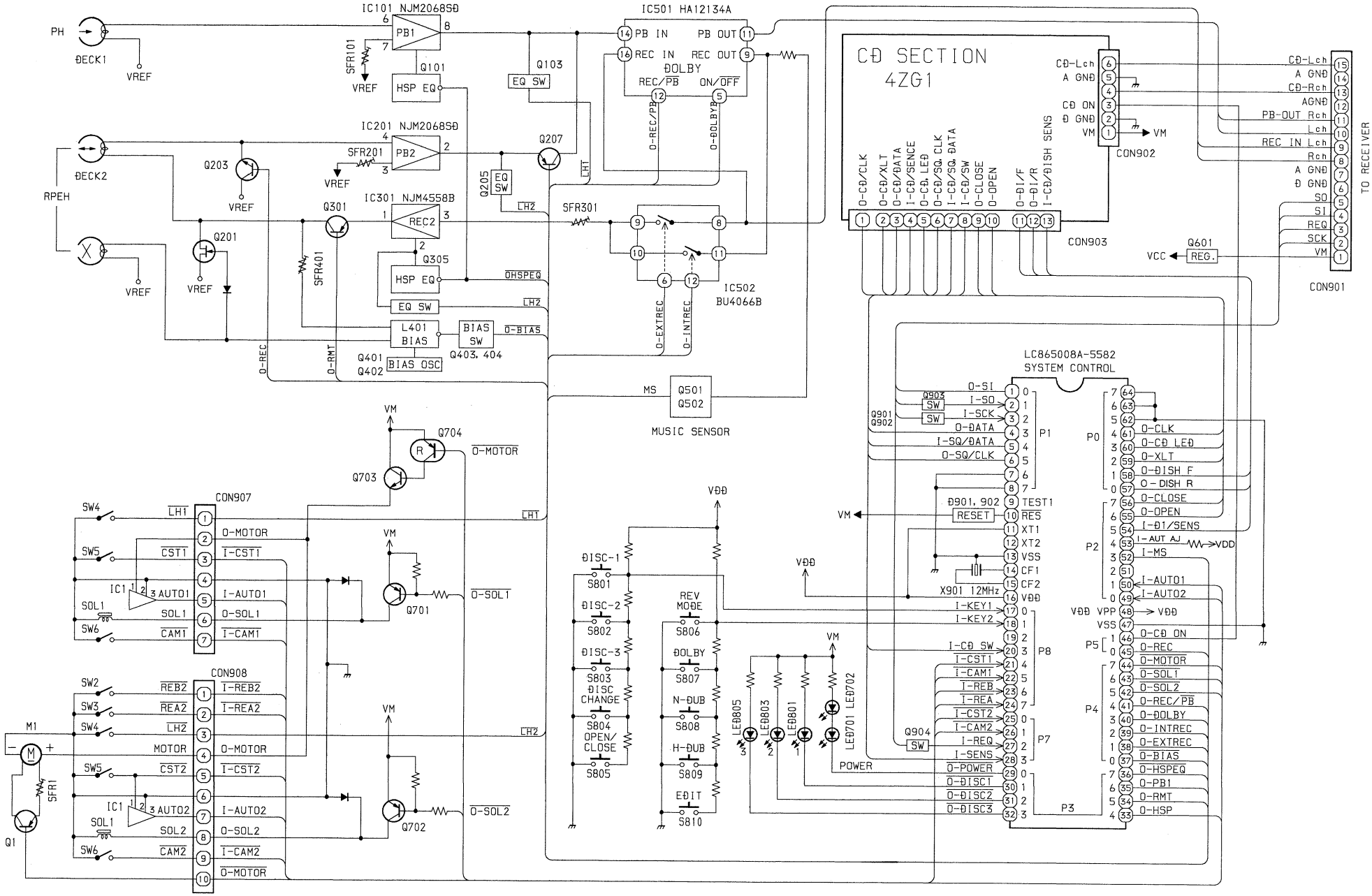
TRUTH TABLE ×=Don't Care

IC BLOCK DIAGRAM

IC,HA12134A



BLOCK DIAGRAM – 1



SCHEMATIC DIAGRAM – 1 (MAIN)