

Compal Confidential

EG50_BZ

Q5WT6 Schematics Document

AMD Brazos

Brazos with Ontario / Hudson M3L

UMA only

2011-12-16

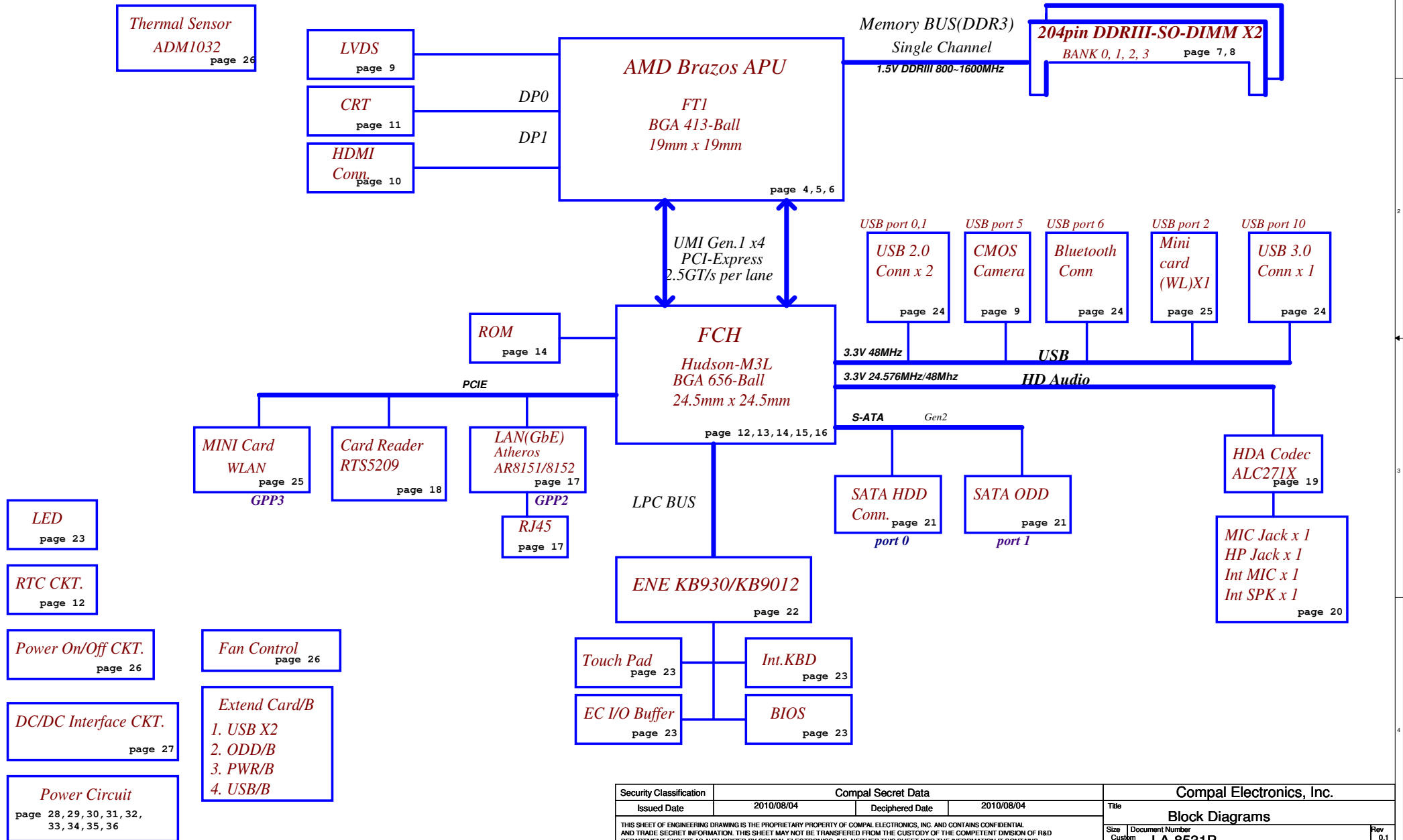
LA-8531P REV: 0.3



Part Number = DA60000RP00

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Brazos



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+VSB	VSB always on power rail	ON	ON	ON*
+3VALW	3.3V always on power rail	ON	ON	ON*
+5VALW	5V always on power rail	ON	ON	ON*
+1.1VALW	1.1V always on power rail	ON	ON	ON*
+APU_CORE	Core voltage for CPU (0.7-1.2V)	ON	OFF	OFF
+APU_CORE_NB	1.0V switched power rail	ON	OFF	OFF
+1.5V	1.5V power rail for CPU VDDIO and DDRIII	ON	ON	OFF
+0.75VS	0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail for APU VDD10	ON	OFF	OFF
+1.1VS	1.1VS switched power rail	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VS	5V switched power rail	ON	OFF	OFF
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF
+3VSG	3.3V switched power rail for GPU	ON	OFF	OFF
+1.8VSG	1.8V switched power rail for GPU	ON	OFF	OFF
+1.5VSG	1.5V switched power rail for GPU	ON	OFF	OFF
+1.0VSG	1.0V switched power rail for GPU	ON	OFF	OFF
+3V_LAN	3.3V power rail for LAN	ON	ON	OFF
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	V _{AD_BID min}	V _{AD_BID typ}	V _{AD_BID max}
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

EC SM Bus1 address

EC SM Bus2 address

Device	Address	HEX	Device	Address	HEX
Smart Battery	0001-011xb	NA	EMC1403-2(GPU)	1001-101xb	9EH

SM Bus Controller 0

(FCH_SMB1 ~ FCH_SMB4, SMB_ALERT#)

Device	Address	HEX
APU SIC/SID (FCH_SMB3)		
H_THERMTRIP# (FCH_ALERT#)		

SM Bus Controller 1

(FCH_SMB0)

Device	Address	HEX
DDR DIMM1 (FCH_SMB0)	1001-000xb	90
DDR DIMM2 (FCH_SMB0)	1001-001xb	92
WLAN (FCH_SMB0)		

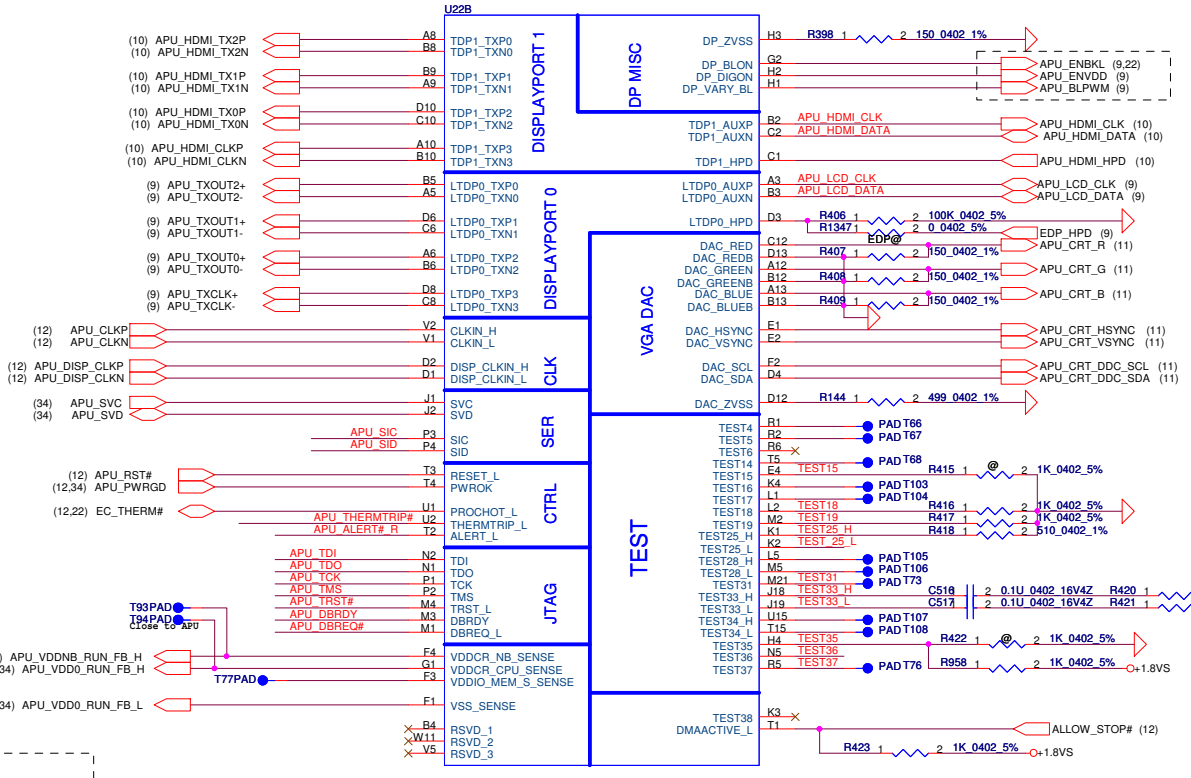
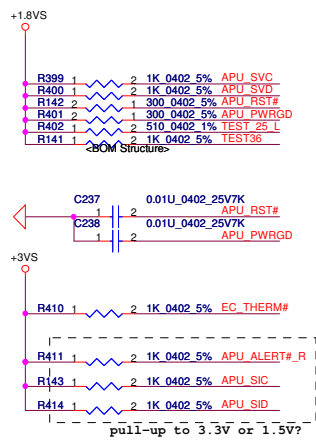
BTO Option Table

BTO Item	BOM Structure
AR8152	8152@
AR8151	8151@
Bluetooth	BT@
ALC271X	271X@
ALC281X	281X@
LVDS	LVDS@
EDP	EDP@
ODD zero power	ZERO@
APU_1.4G	1.4G@
APU_1.7G	1.7G@
normal ODD	ODD@

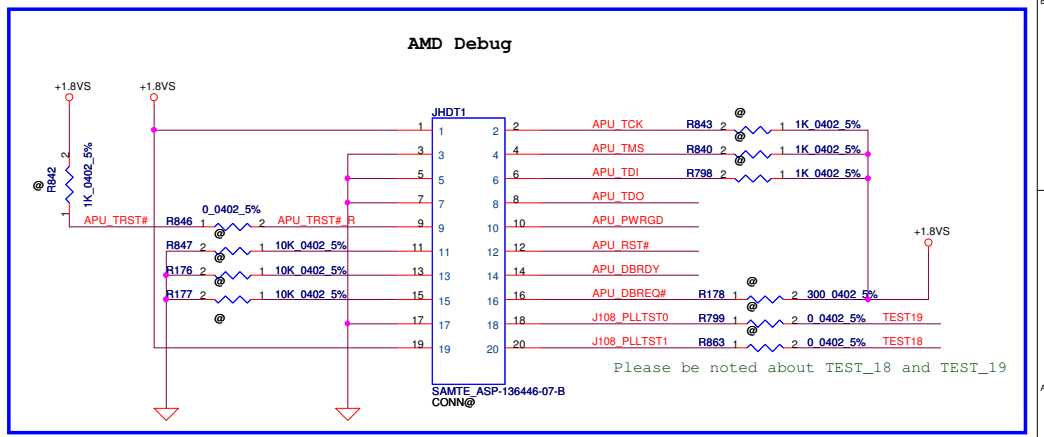
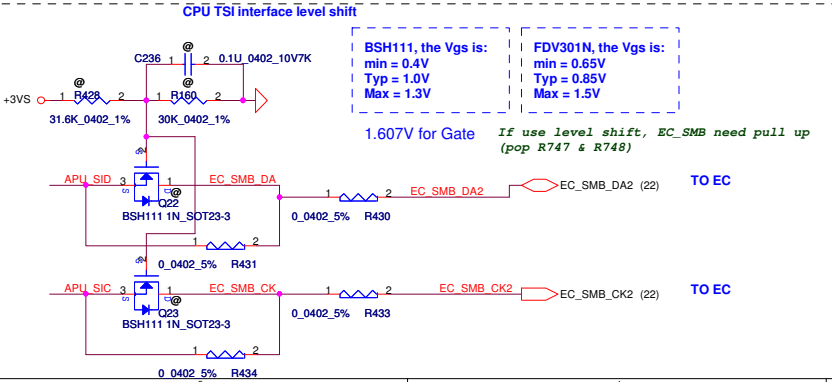
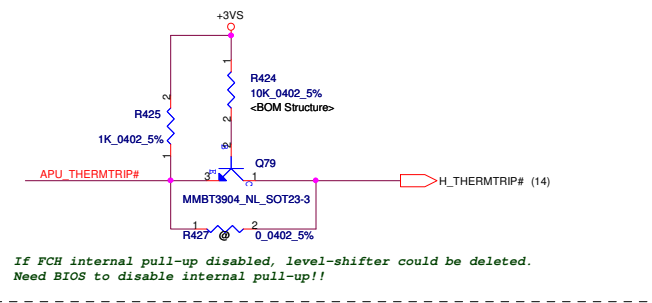
Project ID Table

Board ID	PCB Revision
0	R01
1	R02
2	R03
3	
4	
5	
6	
7	

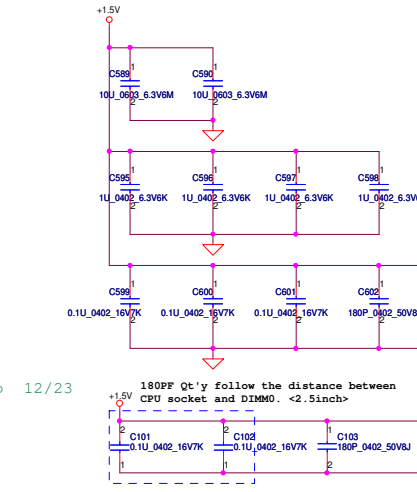
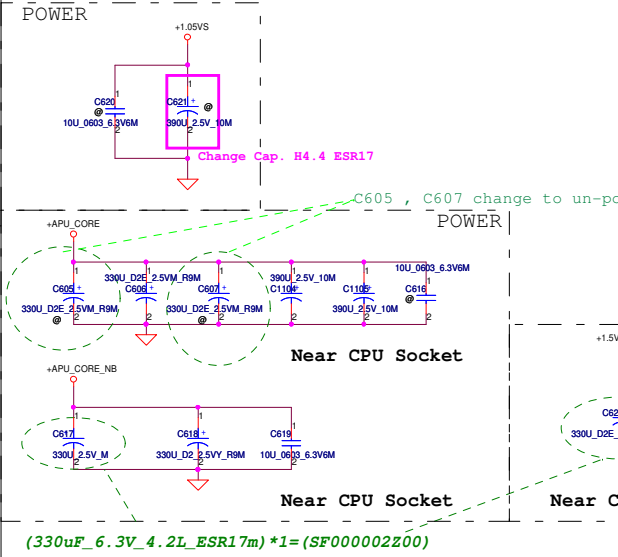
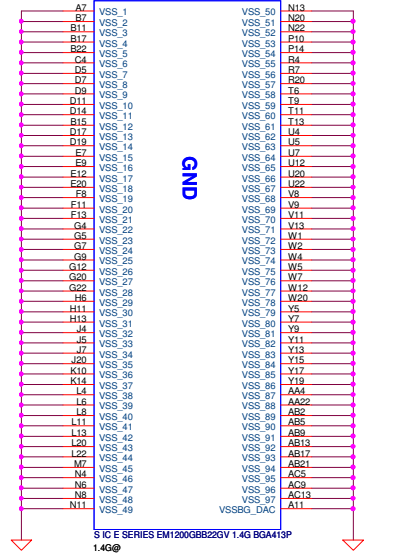
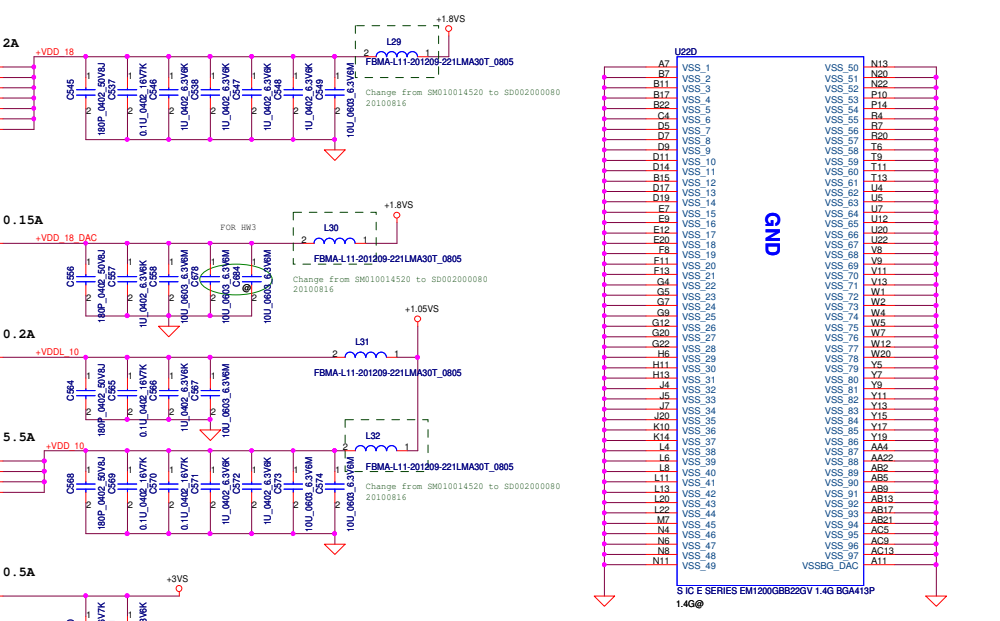
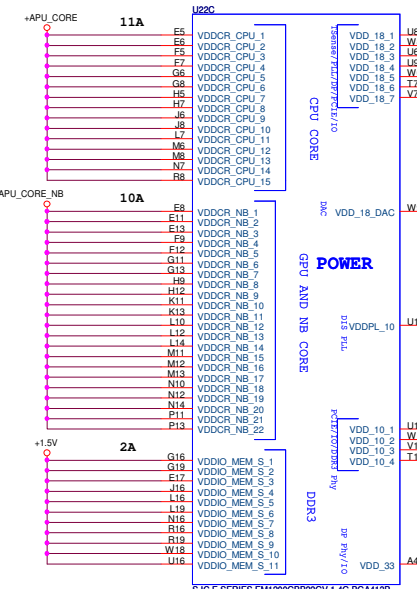
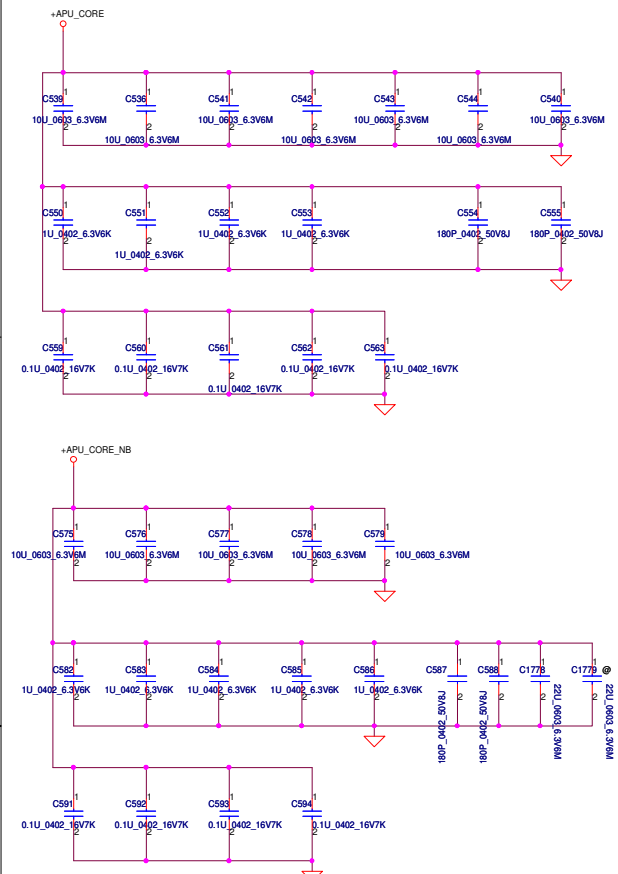
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U22
1.7G@
SIC E SERIES EM1800GBB22GV 1.7G BGA413P
SA00005DW30



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Issued Date	2010/08/04	Deciphered Date	2010/08/04	FT1 CTRL/DP/CRT	
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Power Cap. Summary

APU

- *S POLY C 330U 2.5V M D2E TPE LESR9M H1.8 ---->+APU_CORE(Qty : 3)
- *S POLY C 330U 2.5V Y D2 LESR9M EEFS H1.9 ---->+APU_CORE_NB(Qty : 1)
- *S_A-P_CAP 390U 2.5V M 6.3X5.7 LESR10M VU ---->+1.05VS(Qty : 1)
- *S POLY C 330U 2.5V Y D2 LESR9M EEFS H1.9 ---->+1.5V(Qty : 1)
- *S ELE CAP 330U 6.3V M 6.3X5.9 LESR15M VU ---->+1.8VS(Qty : 1)
- S_A-P_CAP 390U 2.5V M 6.3X5.7 LESR10M VU ---->+APU_CORE(Qty : 1) Reverse
- S_A-P_CAP 330U 2.5V M 6.3X4.2 R17M VLP5 ---->+APU_CORE_NB(Qty : 1) Reverse
- 1.4G@

DDR3

- S POLY C 330U 2V M X LESR6M SX H1.9 ---->+1.5V(Qty : 1) Reserve

FCH

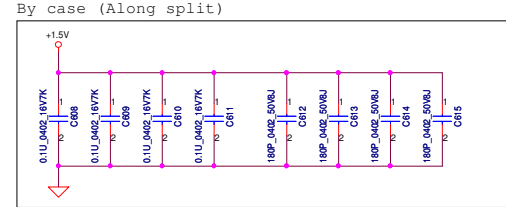
- *S POLY C 330U 2.5V Y D2 LESR9M EEFS H1.9 ---->+1.1VS(Qty : 1)

GPU

- *S POLY C 330U 2V M X LESR6M SX H1.9 ---->+VGA_CORE(Qty : 1) *Change as OS_CON Cap. next phase*
- *S_A-P_CAP 390U 2.5V M 6.3X5.7 LESR10M VU ---->+VGA_CORE(Qty : 1)
- S POLY C 330U 2V M X LESR6M SX H1.9 ---->+VGA_CORE(Qty : 1) Reserve
- *S_A-P_CAP 390U 2.5V M 6.3X5.7 LESR10M VU ---->+1.5VSG(Qty : 1)

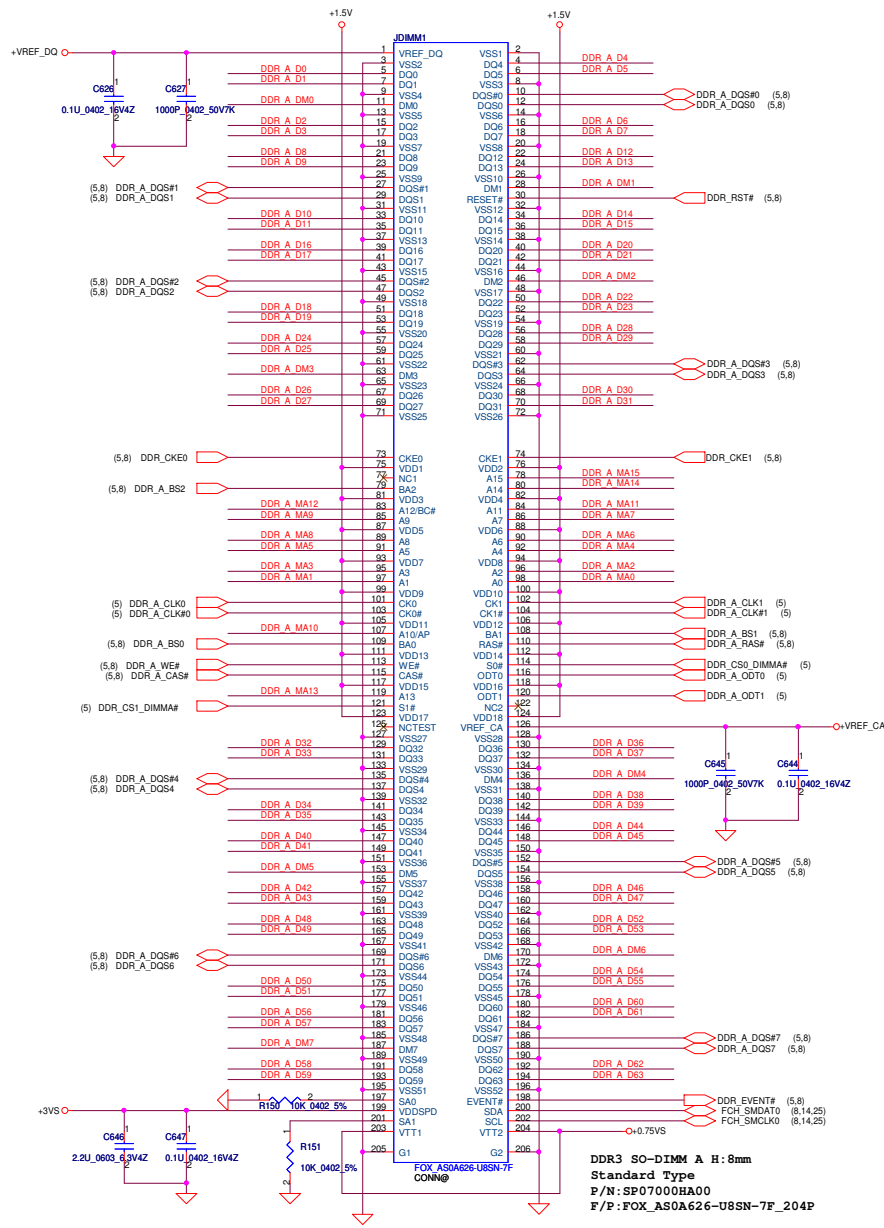
USB

- *S_A-P_CAP 220U 6.3V M C45 R17M SVPE H4.4 ---->+USB_VCCA(Qty : 1)

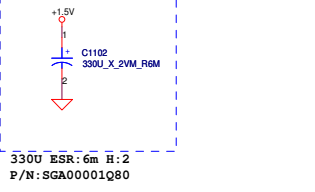
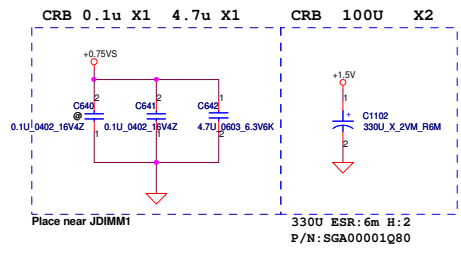
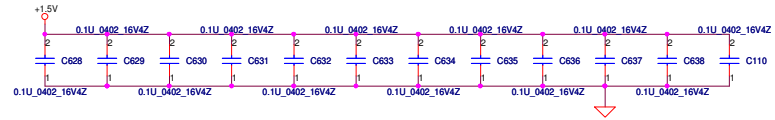
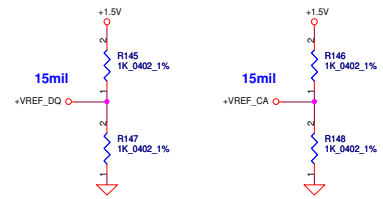
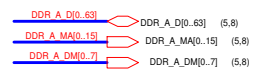


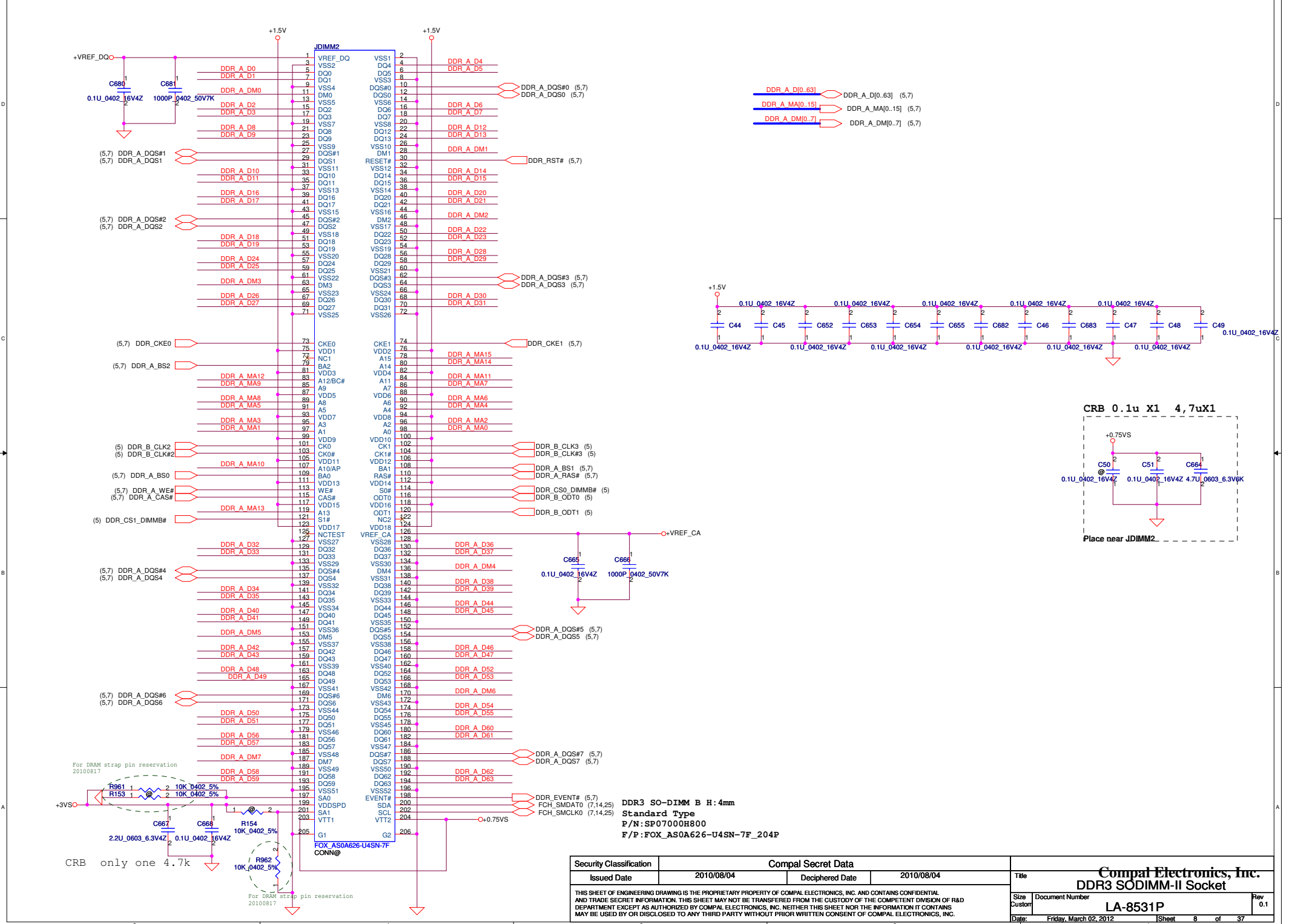
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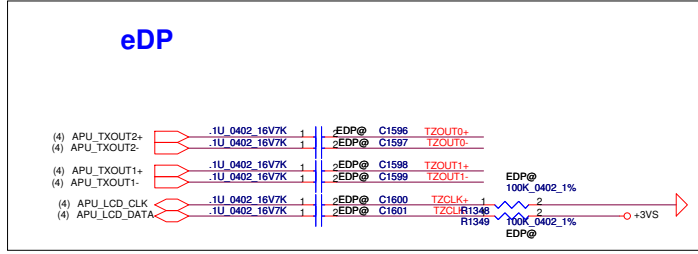
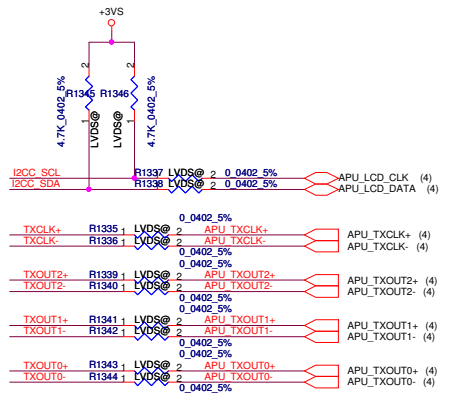
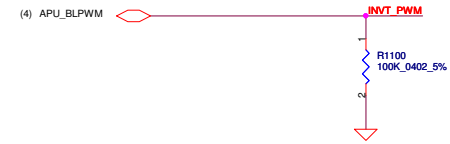
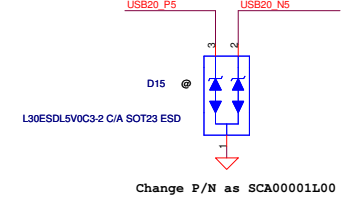
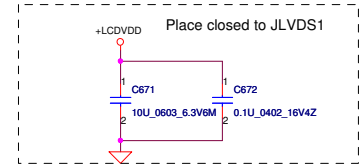
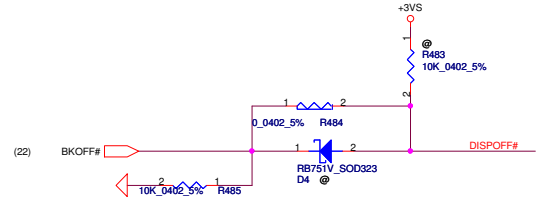
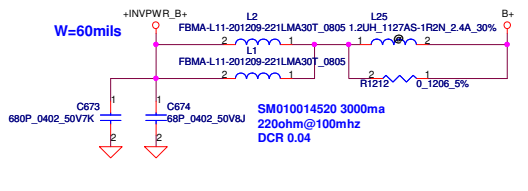
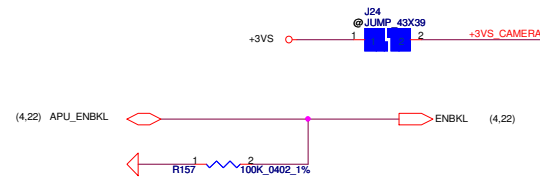
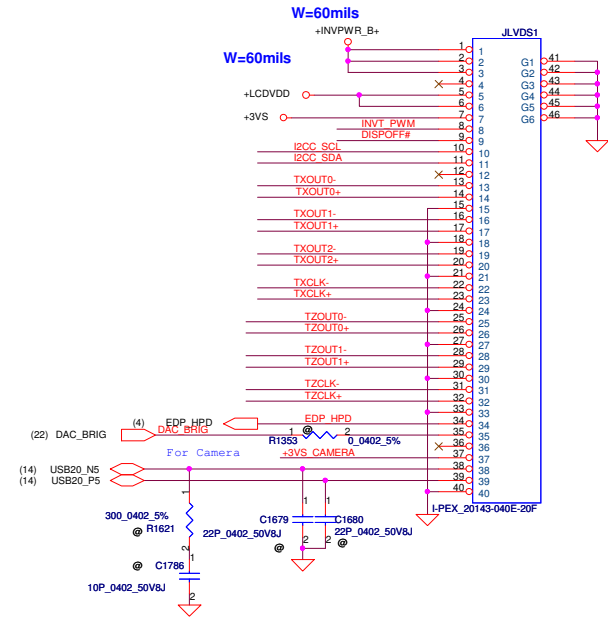
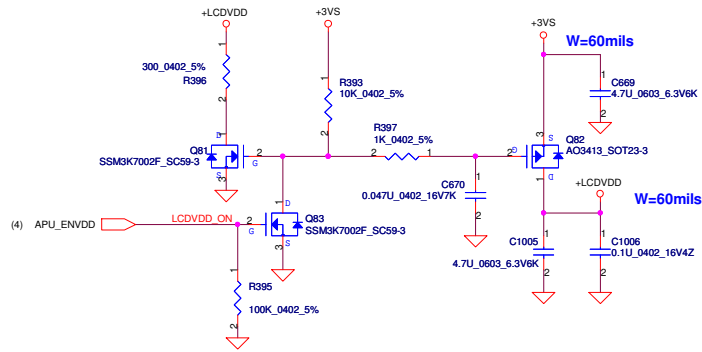
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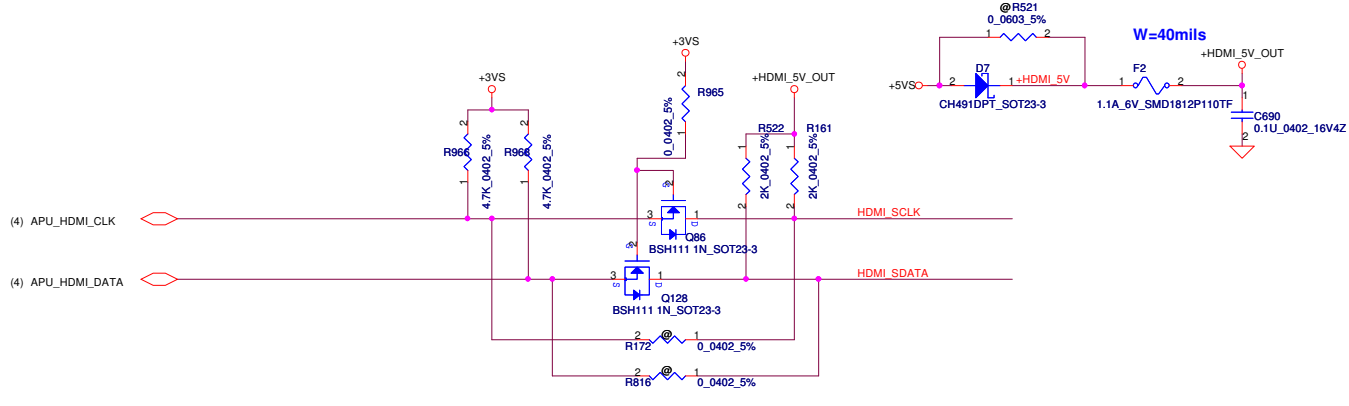




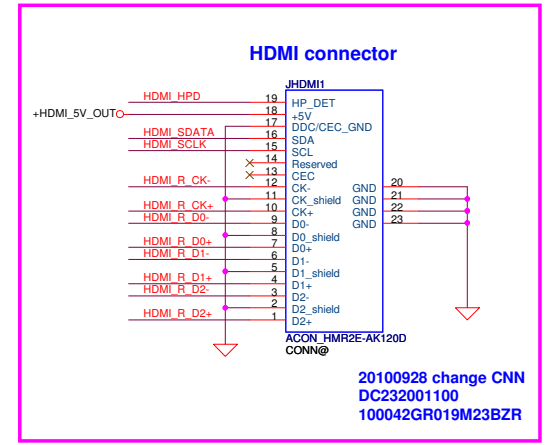
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LCD POWER CIRCUIT

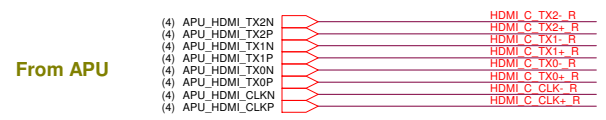
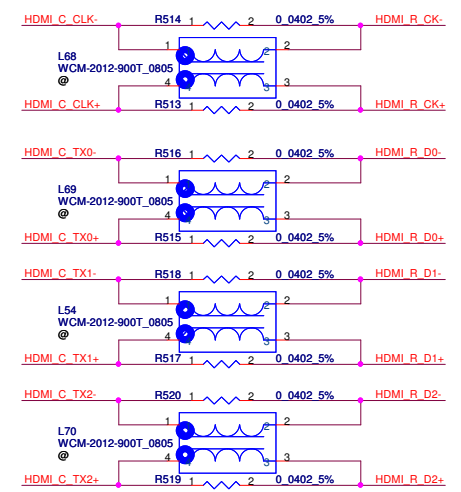
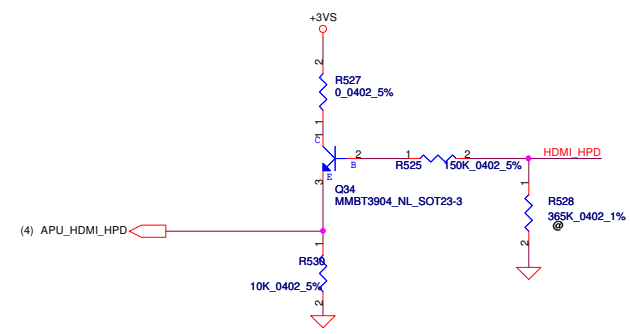




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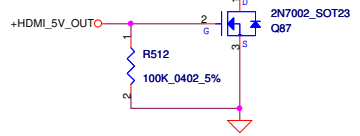


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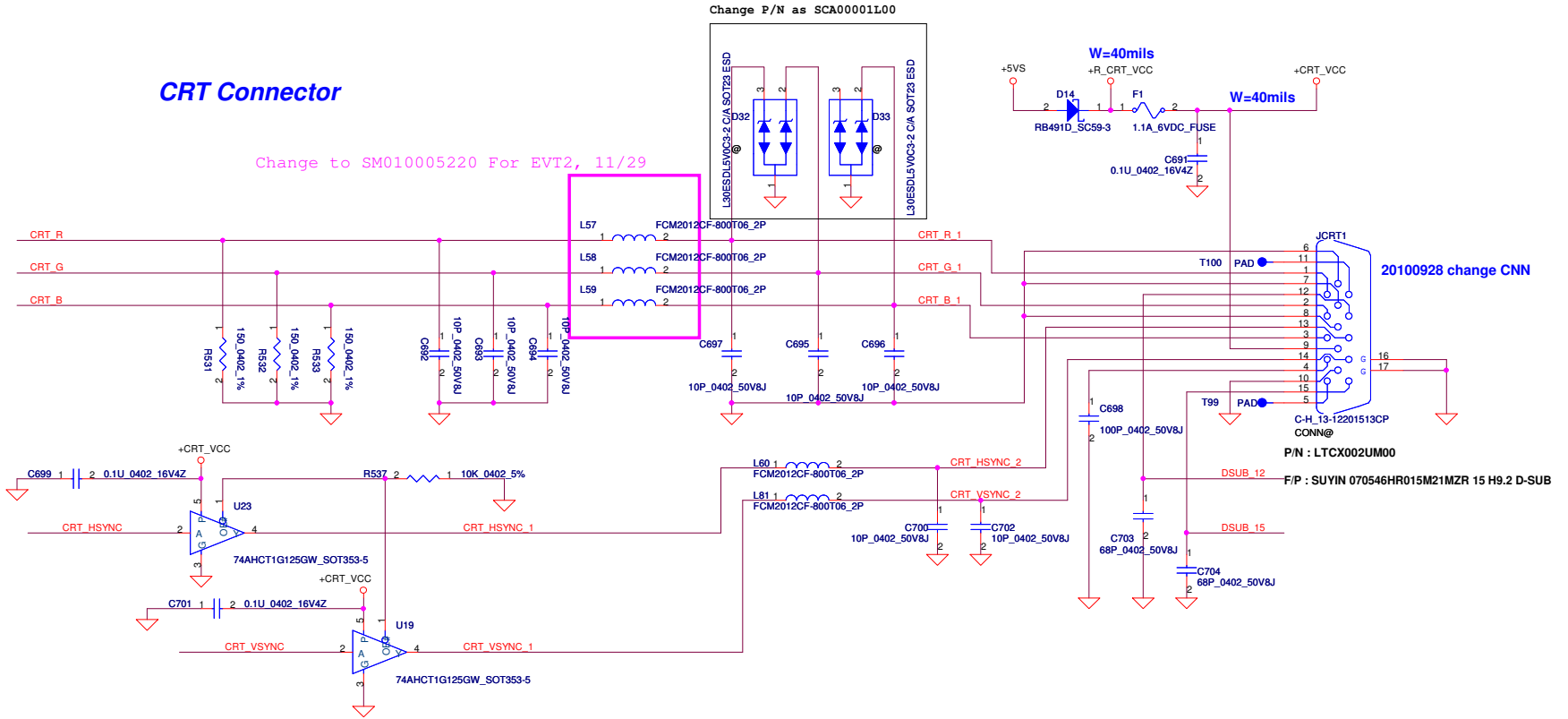
Place closed to JHDMI1

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HDMI C TX1+ R	C511	2	1	0.1U_0402_16V7K	HDMI C TX1+ R	R505	2	499_0402_1%
HDMI C TX0- R	C512	2	1	0.1U_0402_16V7K	HDMI C TX0- R	R503	2	499_0402_1%
HDMI C TX0+ R	C513	2	1	0.1U_0402_16V7K	HDMI C TX0+ R	R502	2	499_0402_1%
HDMI C CLK- R	C514	2	1	0.1U_0402_16V7K	HDMI C CLK- R	R501	2	499_0402_1%
HDMI C CLK+ R	C515	2	1	0.1U_0402_16V7K	HDMI C CLK+ R	R500	2	499_0402_1%



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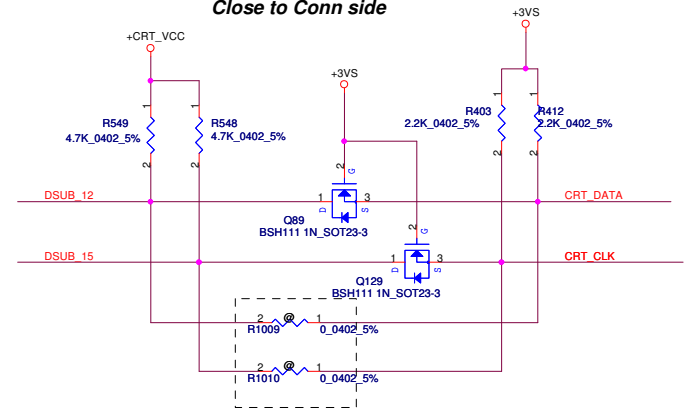
CRT Connector



From APU

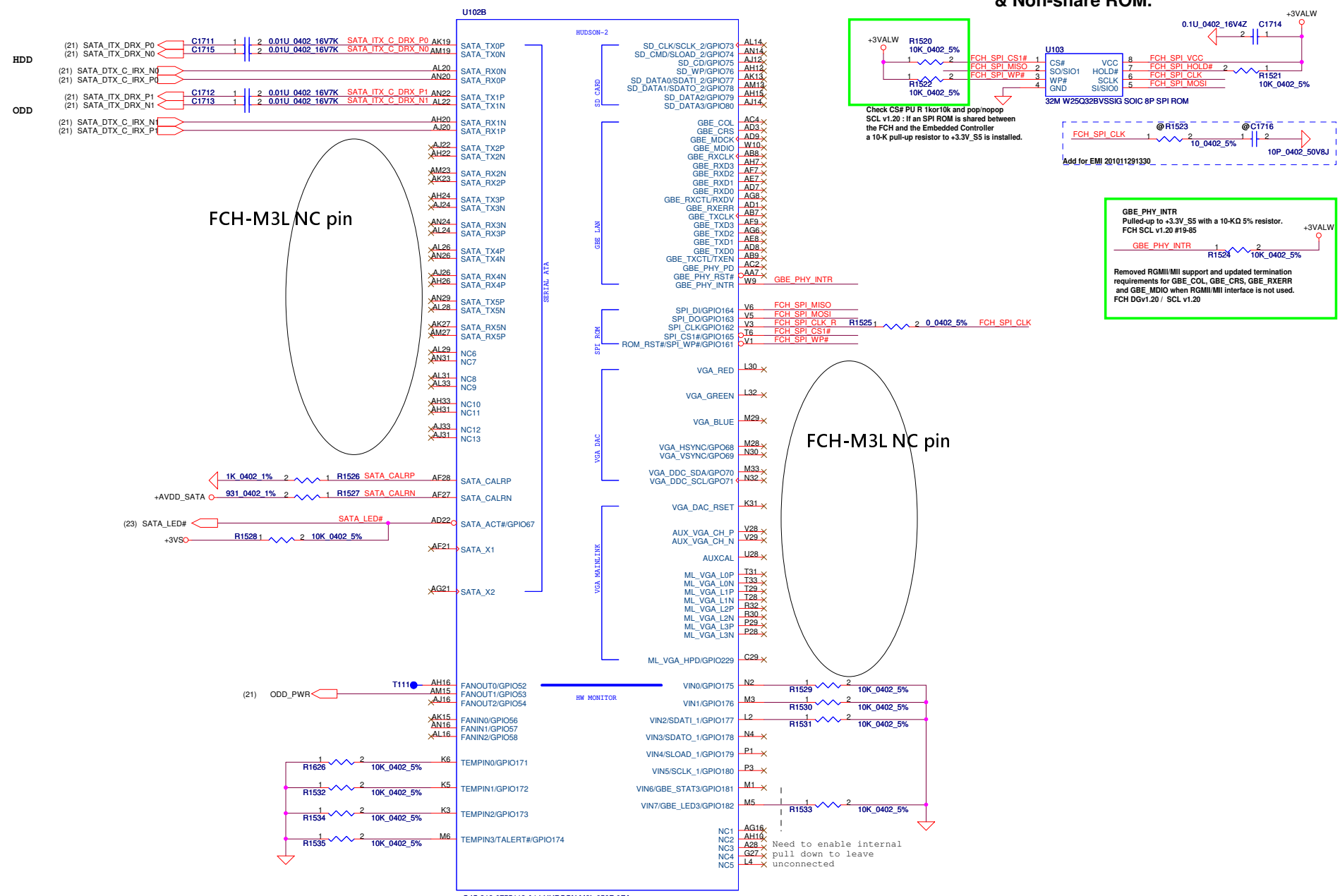
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- (4) APU_CRT_G APU_CRT_G CRT_G
- (4) APU_CRT_B APU_CRT_B CRT_B
- (4) APU_CRT_HSYNC APU_CRT_HSYNC CRT_HSYNC
- (4) APU_CRT_VSYNC APU_CRT_VSYNC CRT_VSYNC
- (4) APU_CRT_DDC_SDA APU_CRT_DDC_SDA CRT_DATA
- (4) APU_CRT_DDC_SCL APU_CRT_DDC_SCL CRT_CLK

Close to Conn side



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4MB SPI ROM & Non-share ROM.

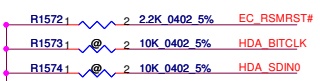
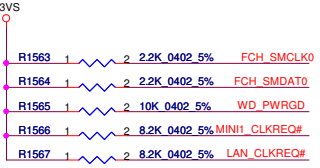
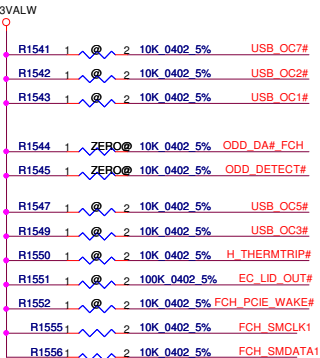
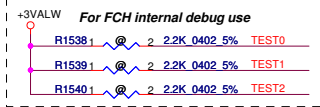
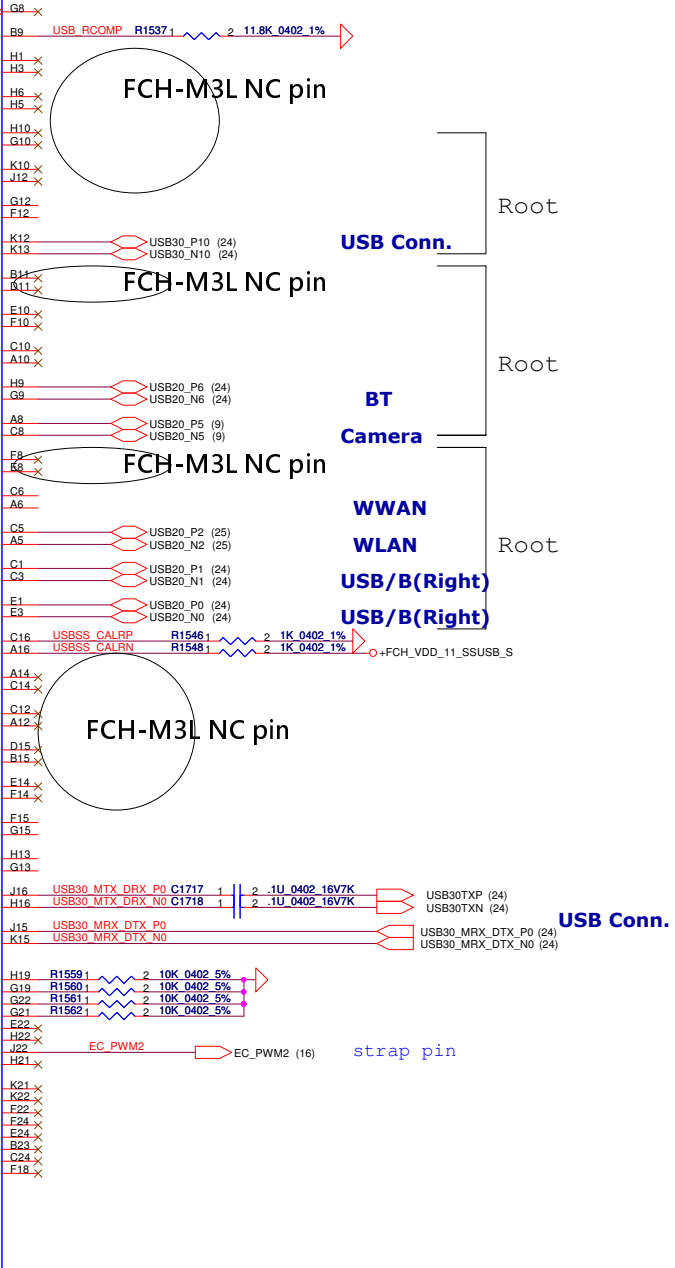
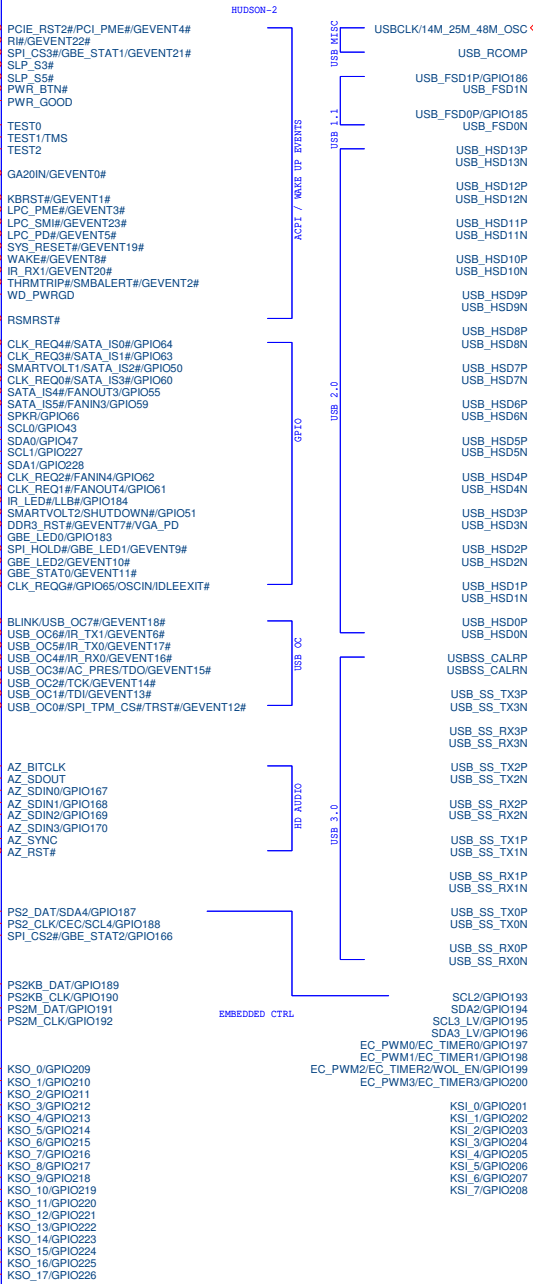
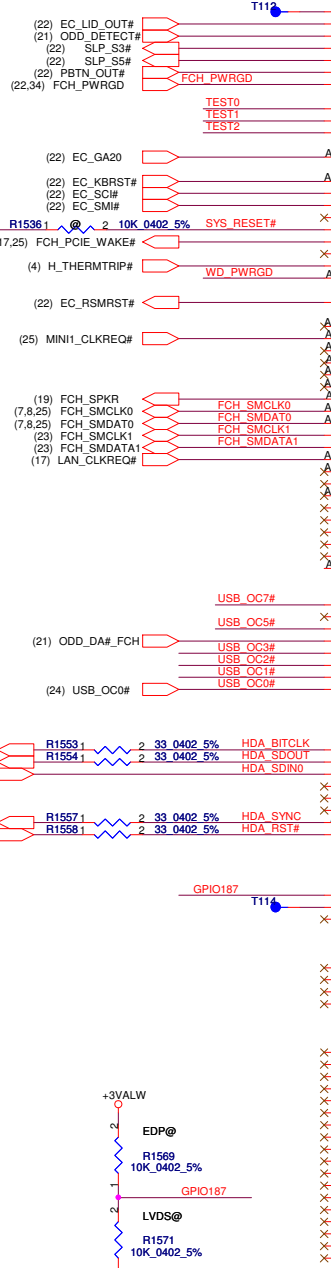


S IC 218-0755113 A14 HUDSON M3L 656P 0FA

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				Size	Document Number	Rev
				Custom	LA8681P	0.1
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PCIE_RST2 : Reset PCIE device on Hudson 3

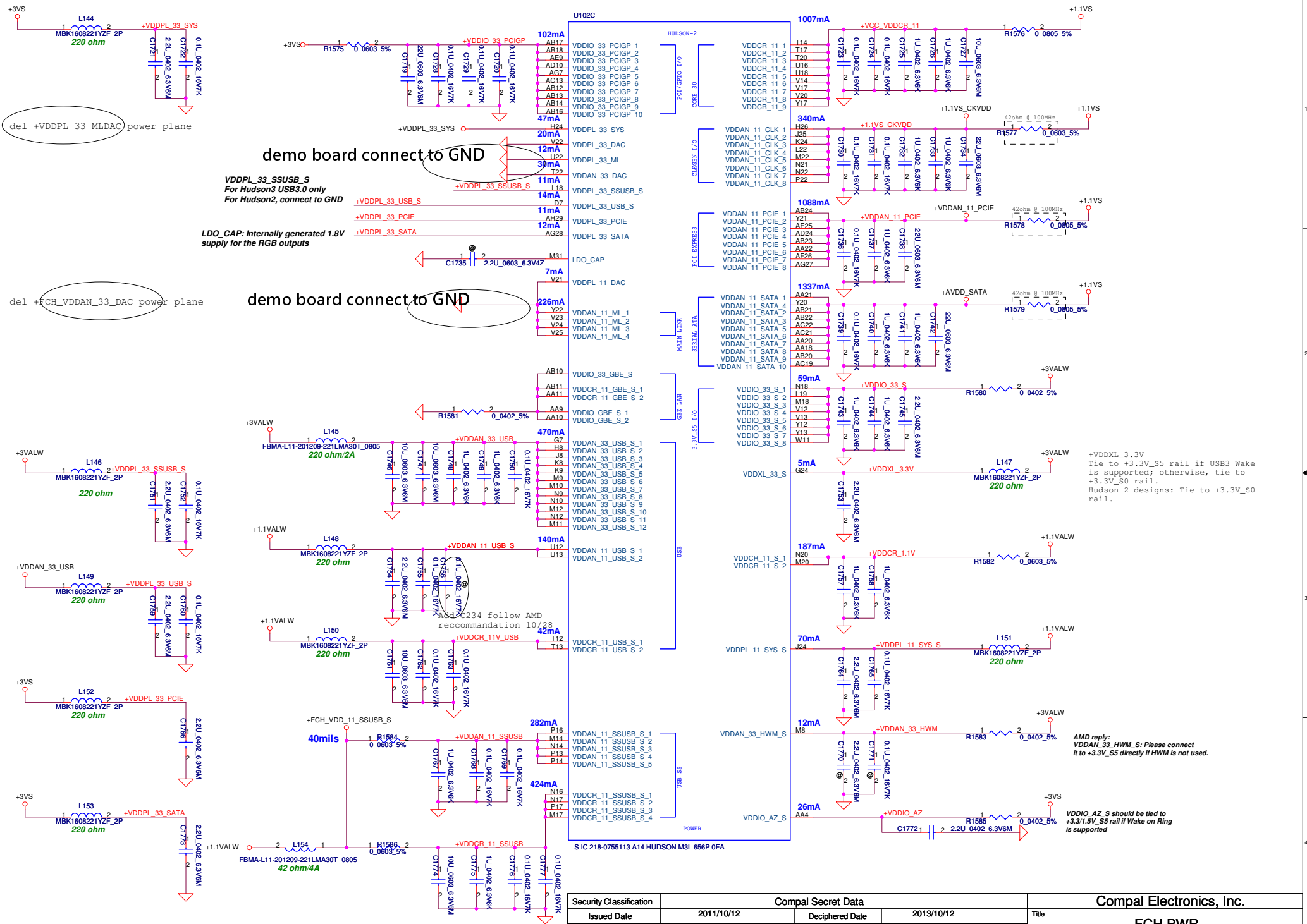
U102D



GPIO187	
0	LVDS
1	EDP

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Size	Document Number	Rev		Date: Friday, March 02, 2012	
Custpm	LA8681P	0.1		Sheet 14 of 37	



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				Custom	L A8681P	0.1		
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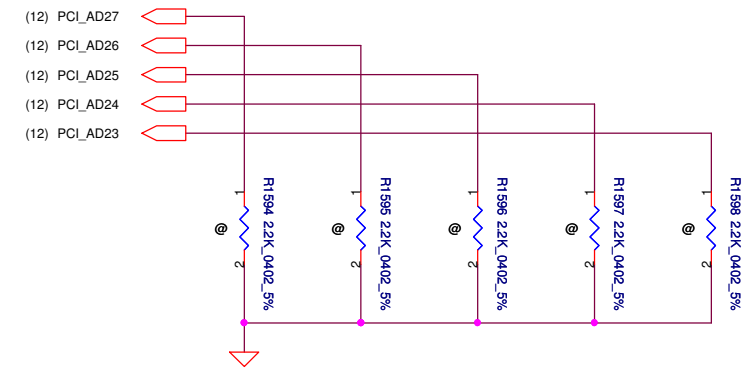
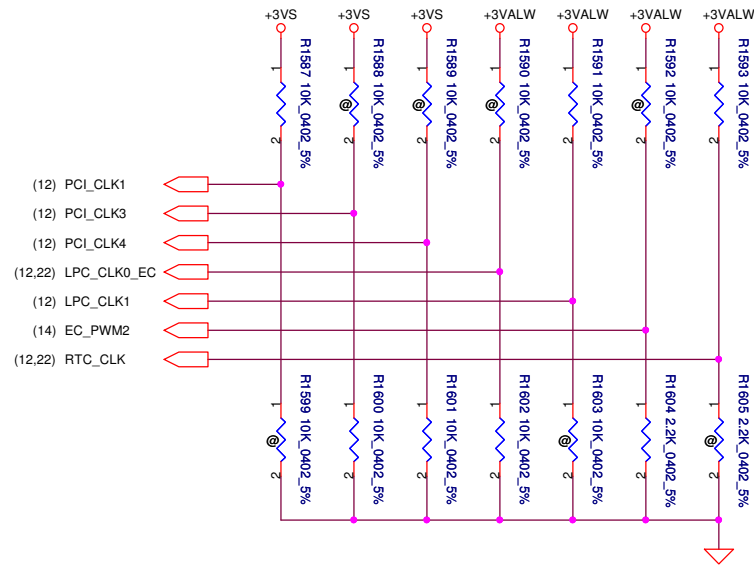
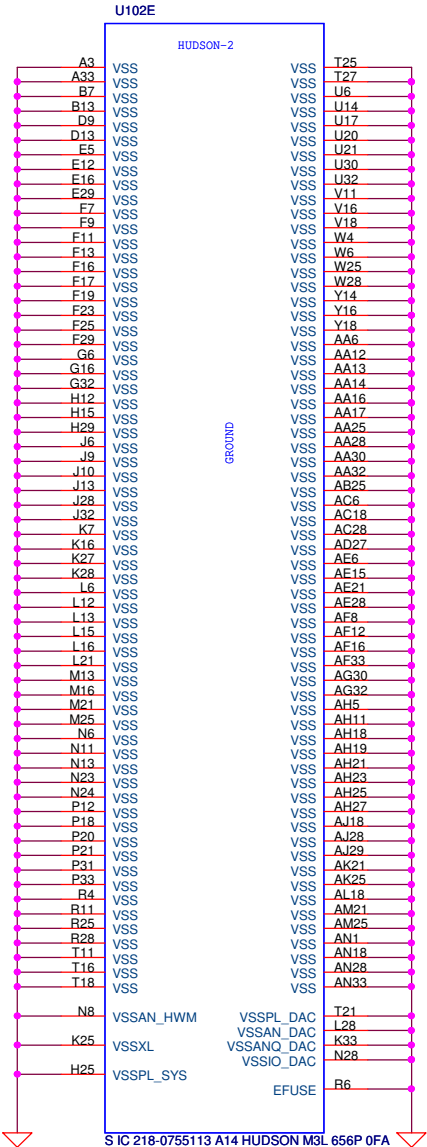
STRAP PINS

	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0_EC	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAPS	NON_FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	FORCE PCIE GEN1	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLE	SPI ROM DEFAULT	S5 PLUS MODE ENABLED

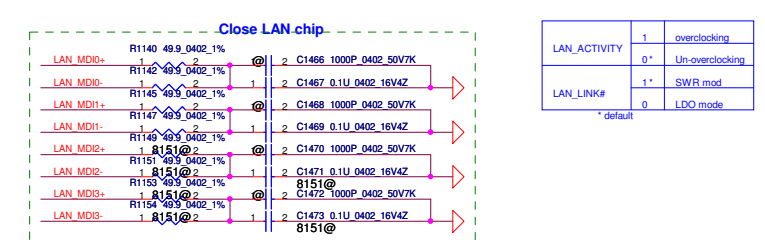
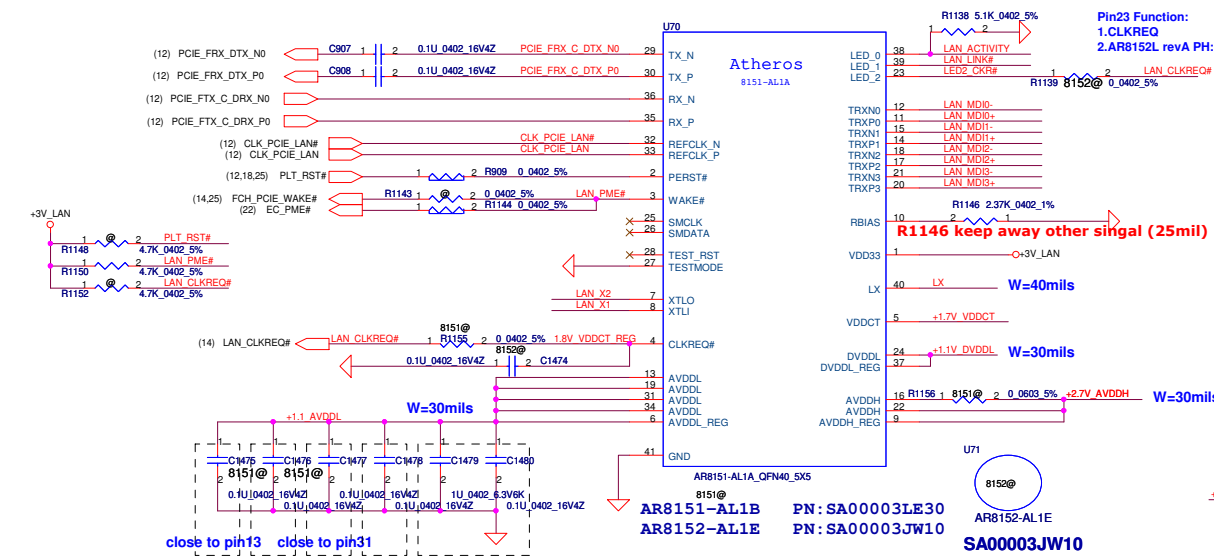
DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]

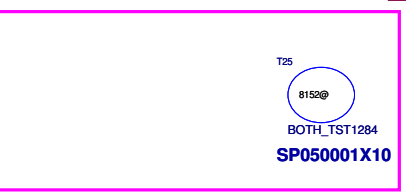
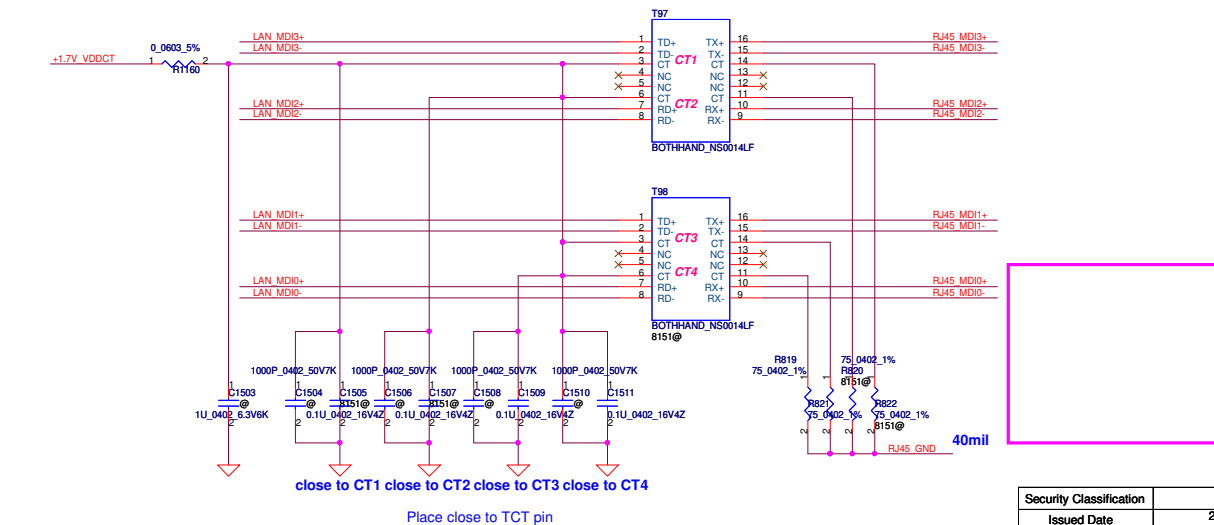
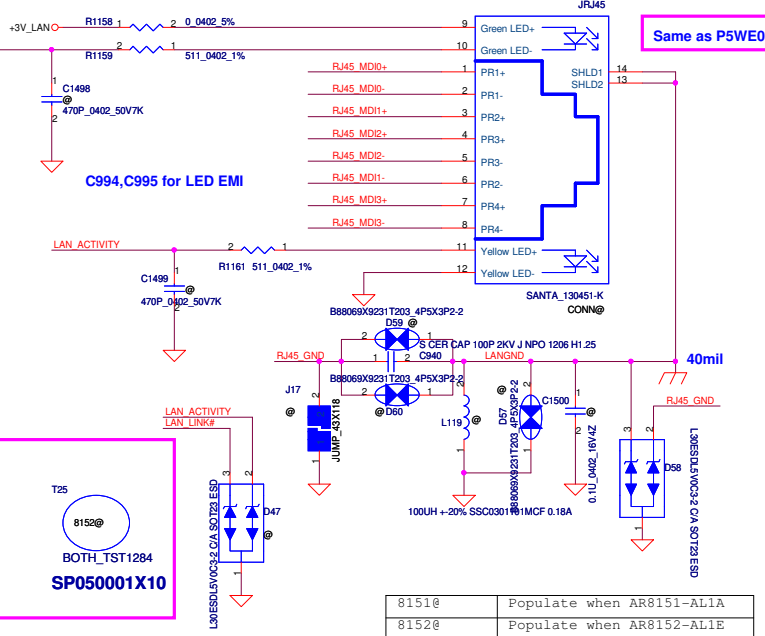
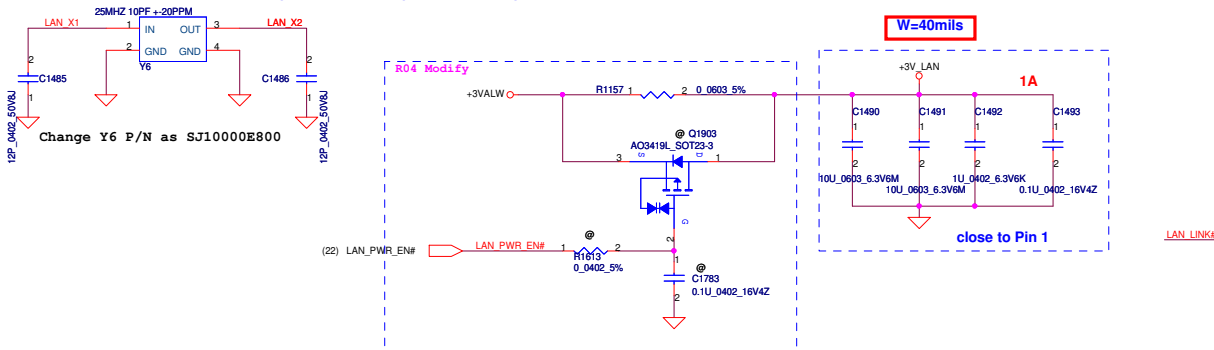
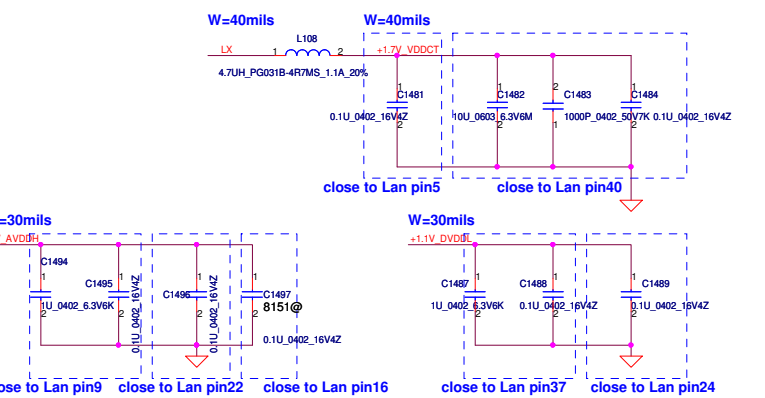
	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT



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Size B	Document Number	Rev		0.1	
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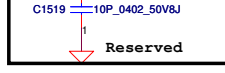
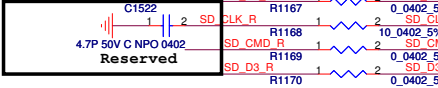
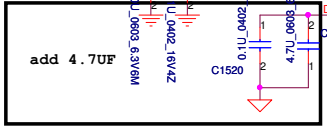
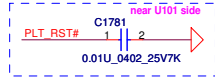
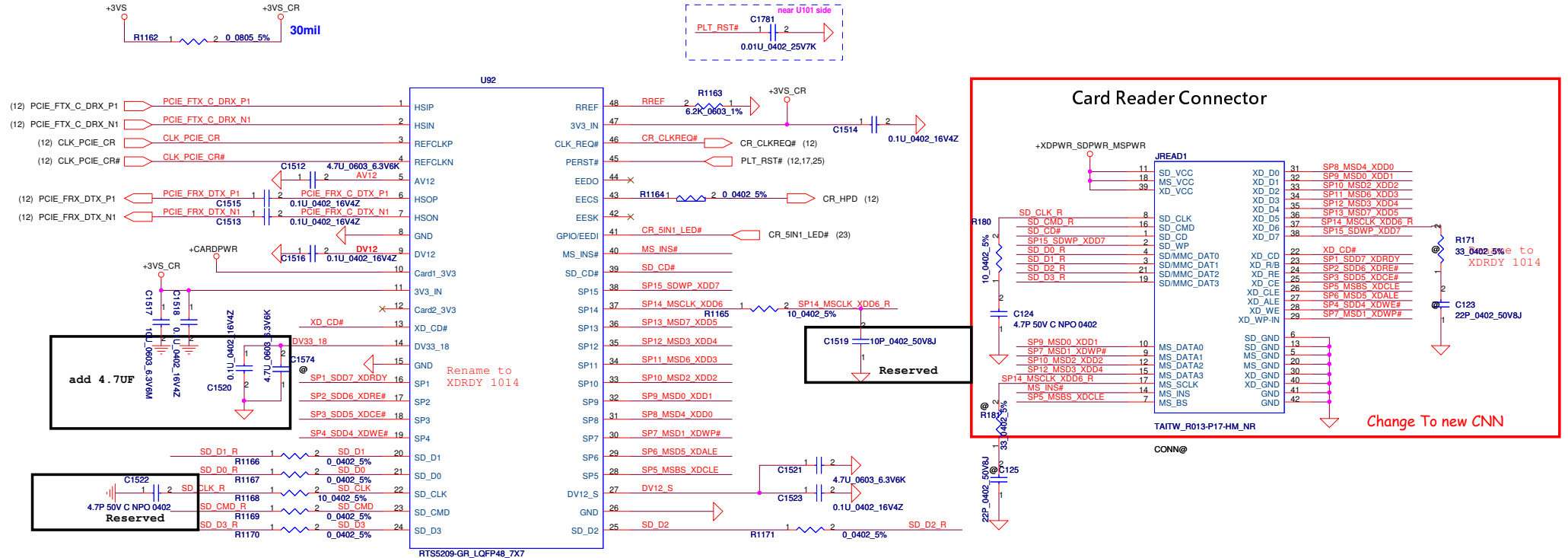


LAN_ACTIVITY	1	overclocking
	0*	Un-overclocking
LAN_LINK#	1*	SWR mod
	0	LDO mode
		* default

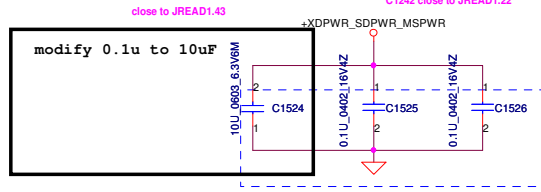


8151@	Populate when AR8151-AL1A
8152@	Populate when AR8152-AL1E

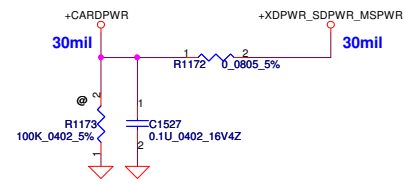
RTS5209-GR



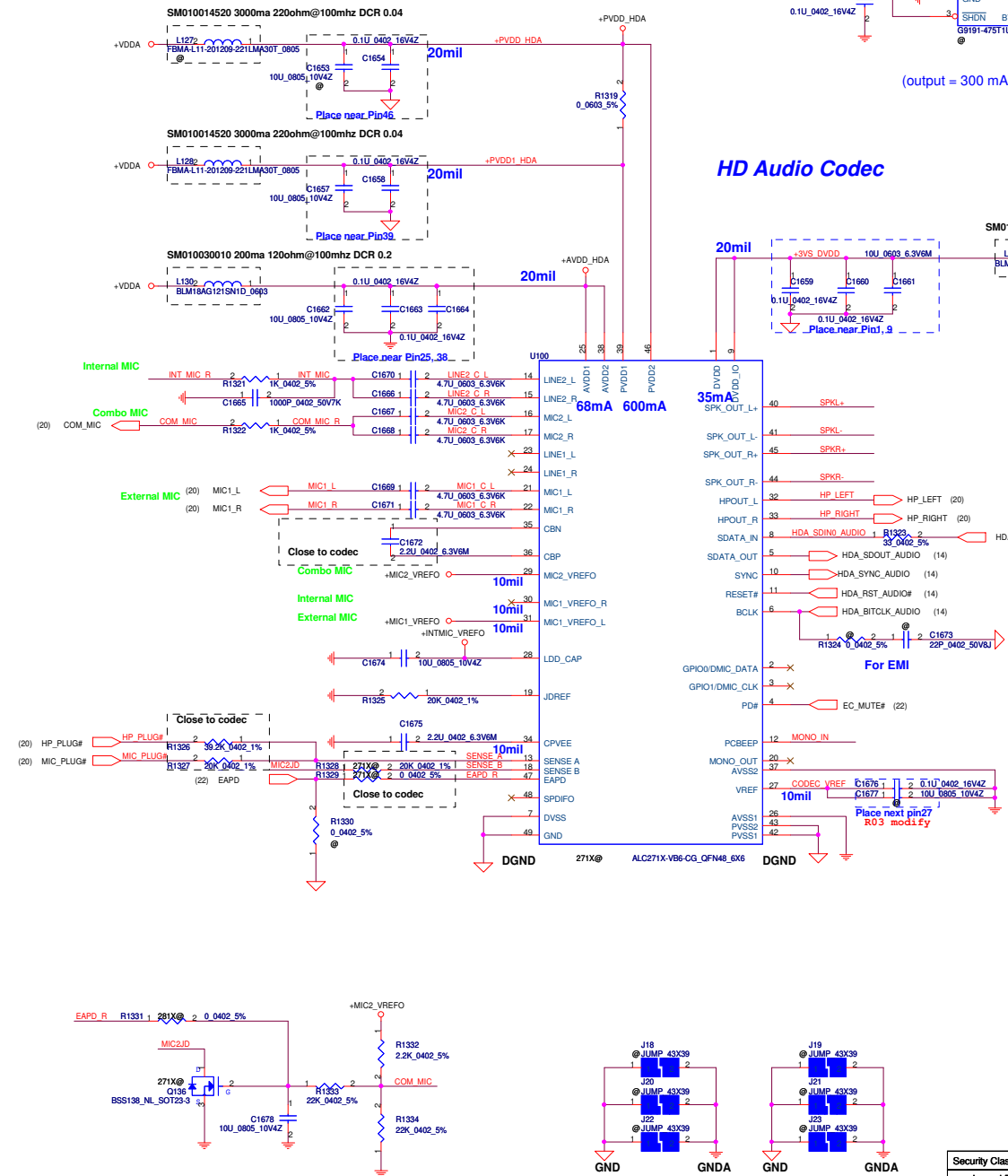
check X'tal?



C1524, C1525 close to connector



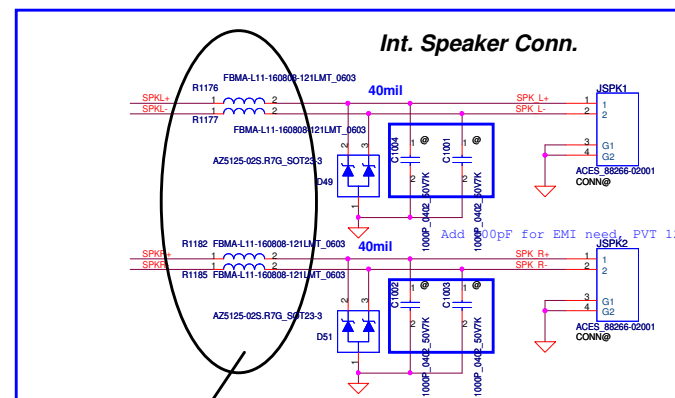
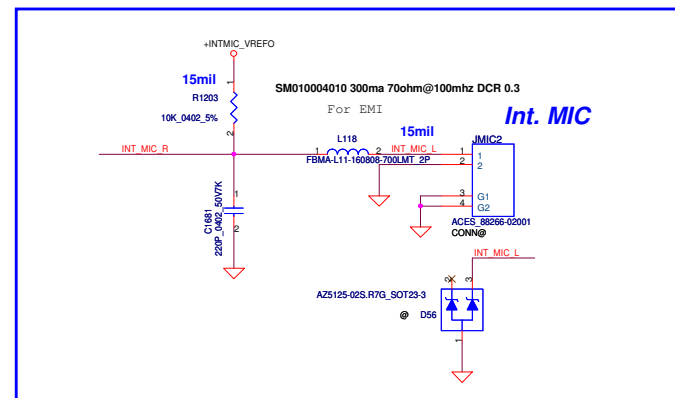
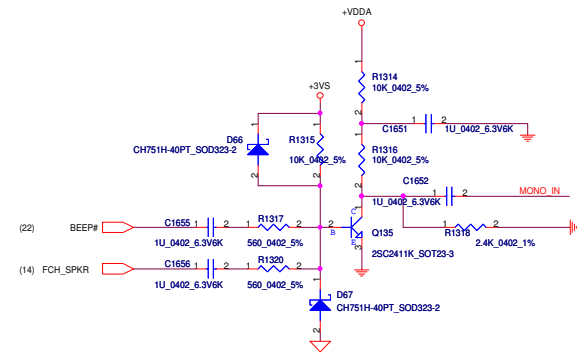
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Size	Document Number	Rev		
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(output = 300 mA)

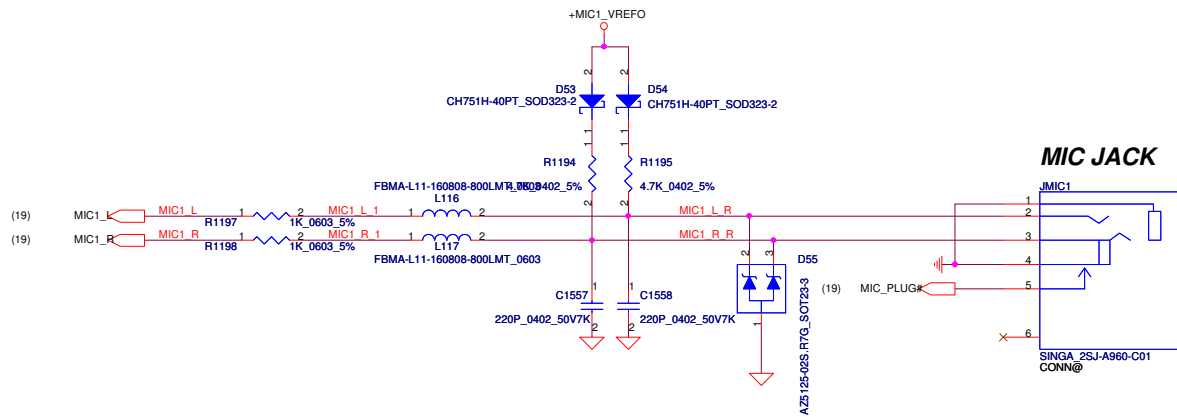
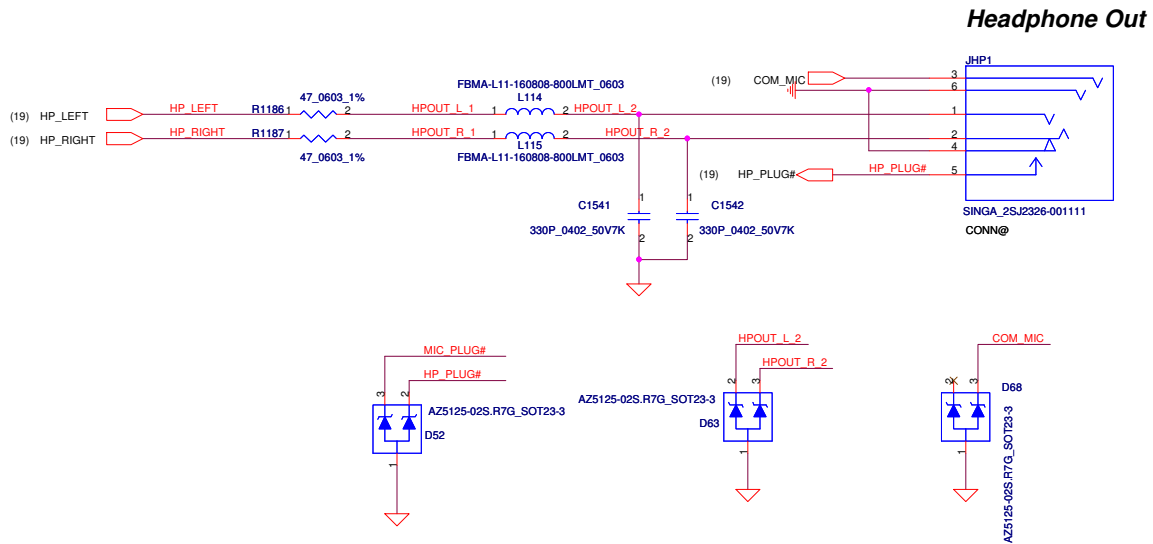
HD Audio Codec

SM010030010 200ma 120ohm@100mhz DCR 0.2



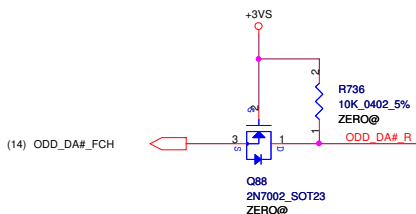
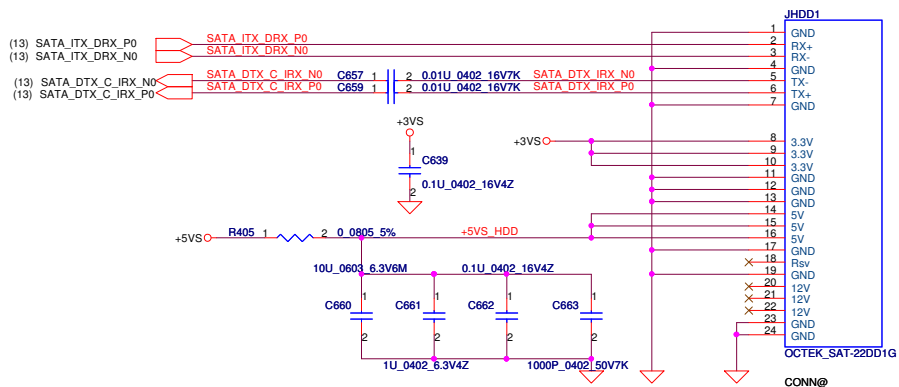
R1182/R1185/R1176/R1177 change to FBMA-L11-160808-121LMT(0603) For EMC Require , PVT 12/30

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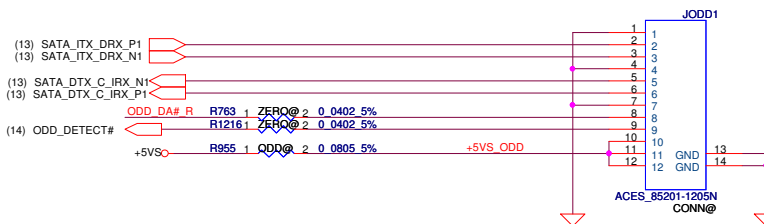
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				Date:	Friday, March 02, 2012
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SATA HDD Conn.

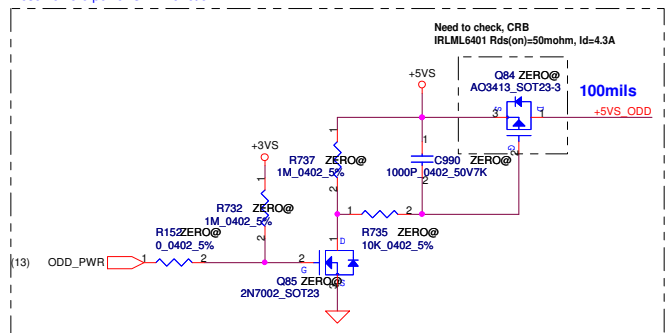


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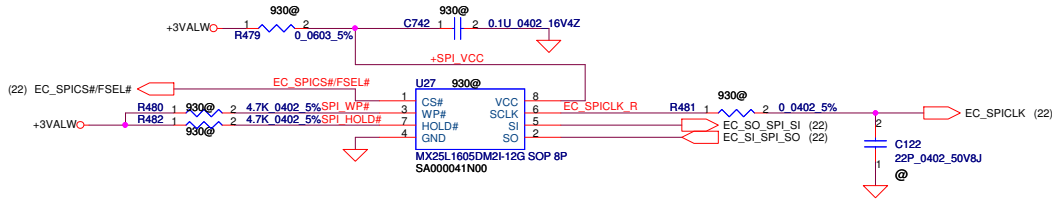
SATA ODD Conn.



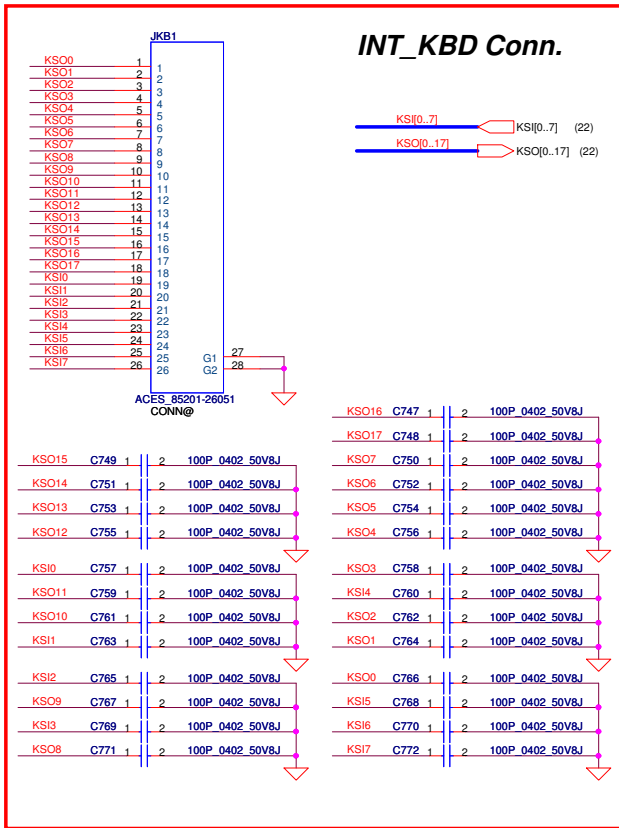
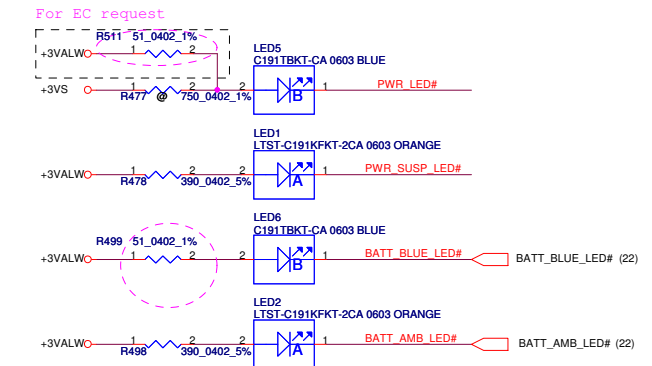
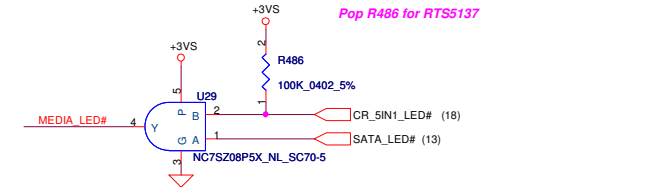
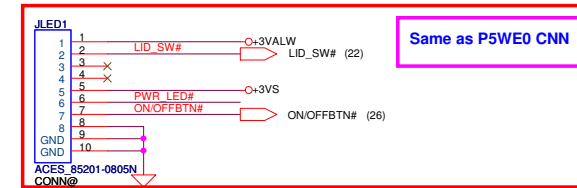
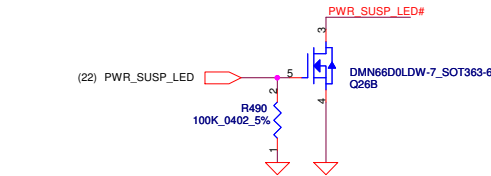
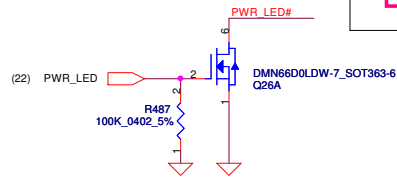
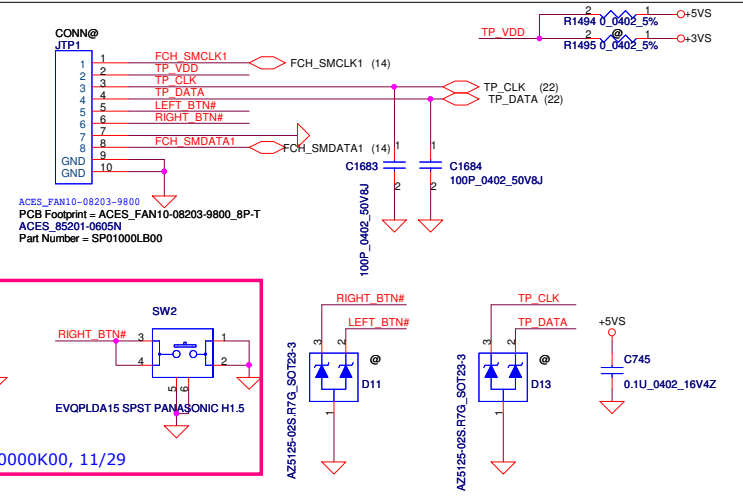
8/13
Reserve zero power ODD Function



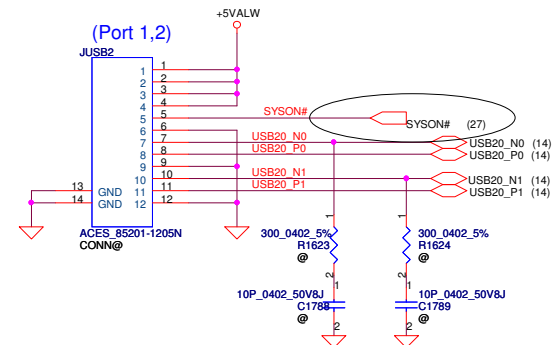
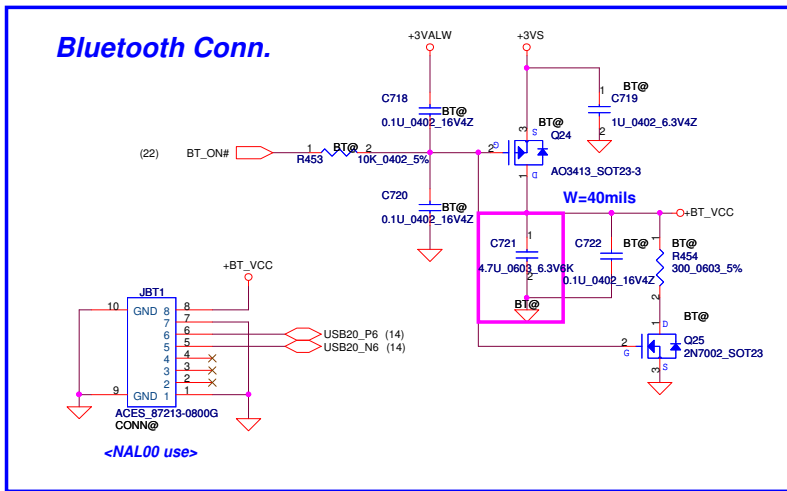
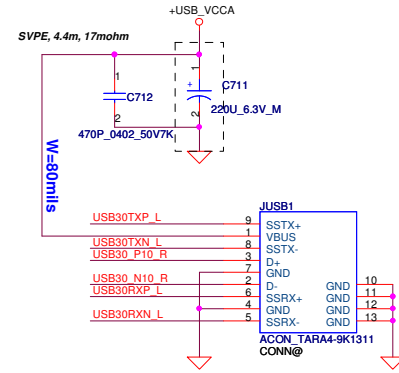
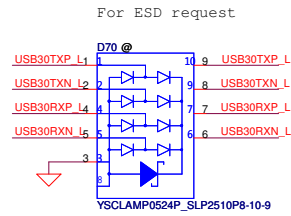
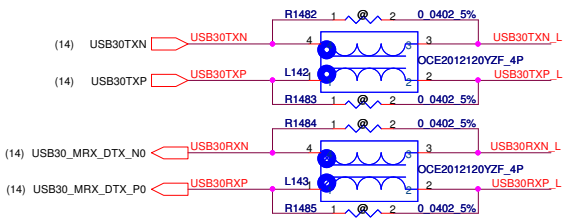
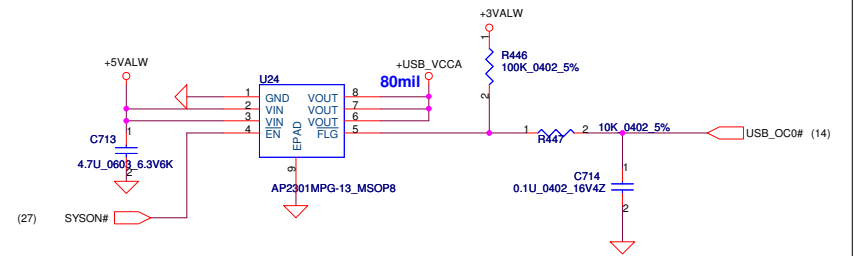
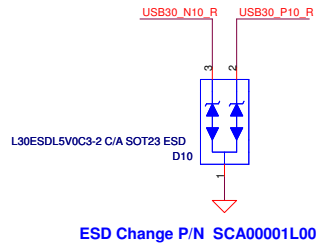
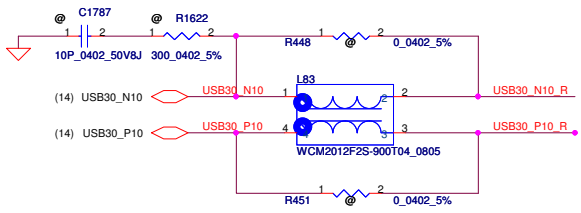
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				Rev: 0.1
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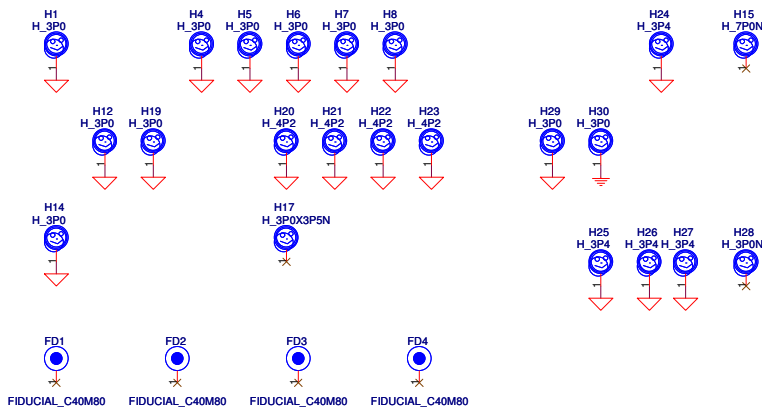
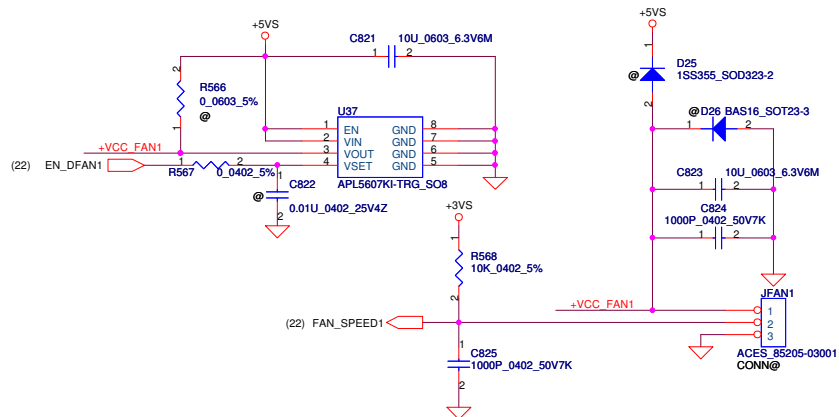
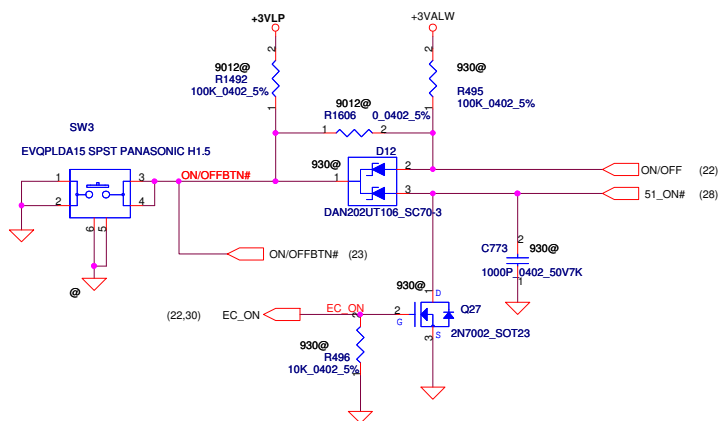
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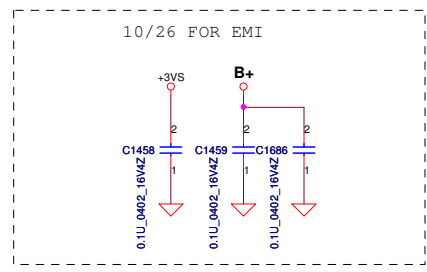
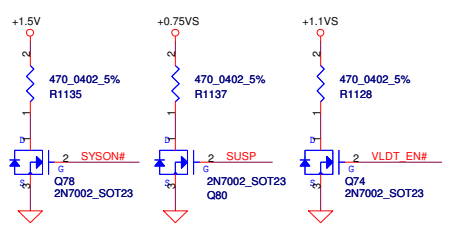
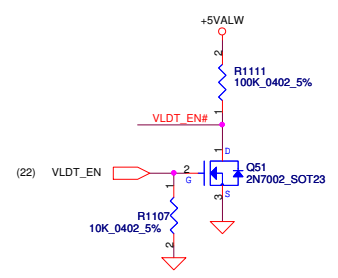
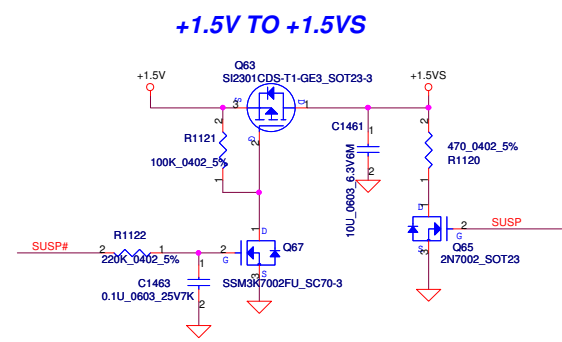
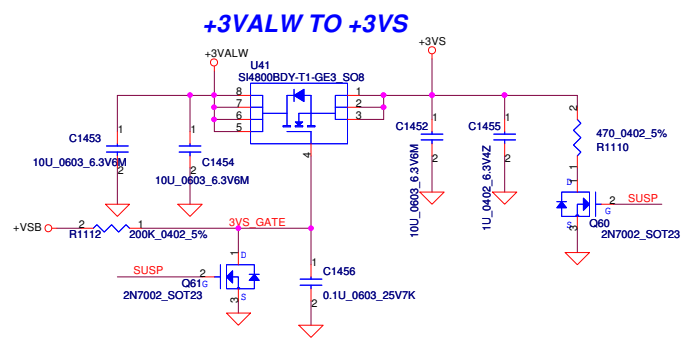
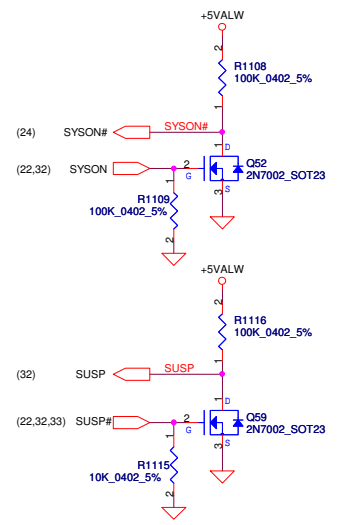
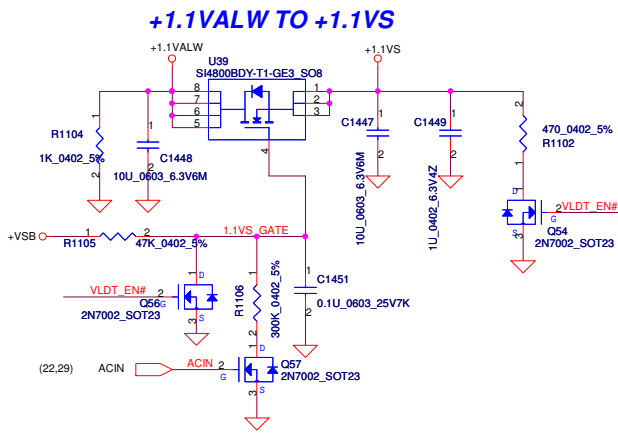
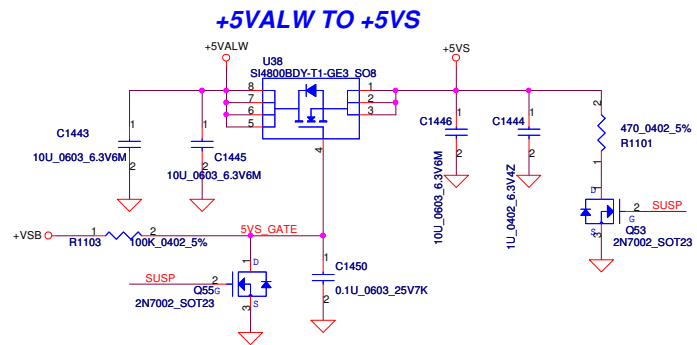
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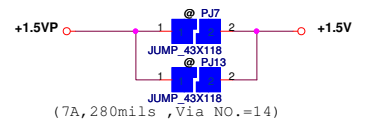
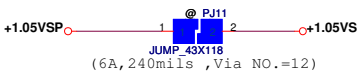
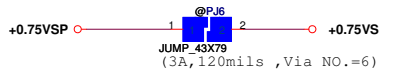
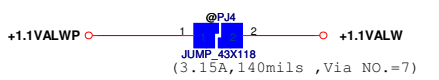
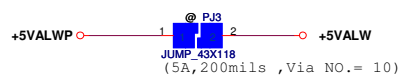
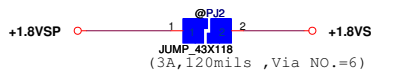
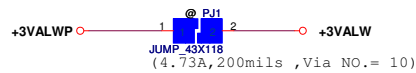
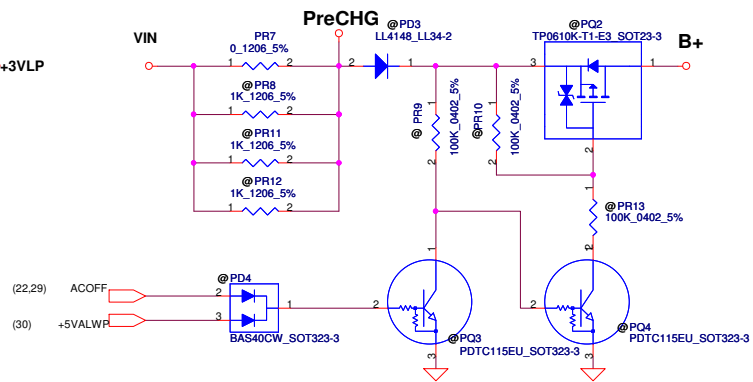
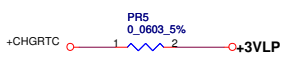
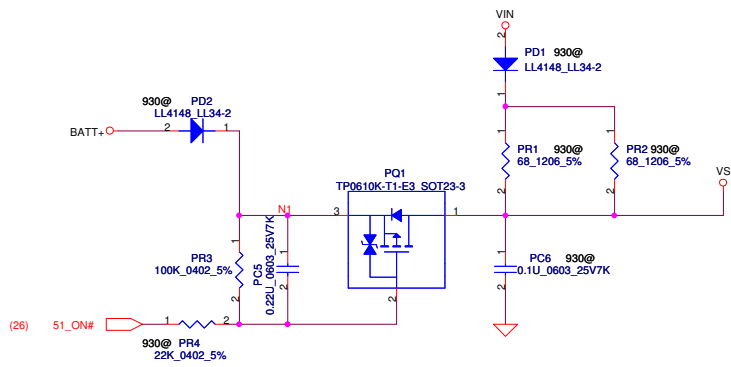
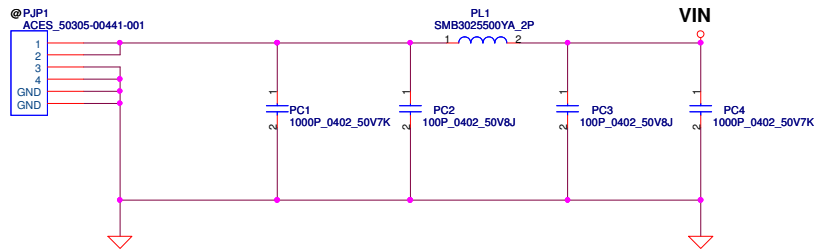
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Size	Document Number	LA-8531P		Rev
Customer				0.1
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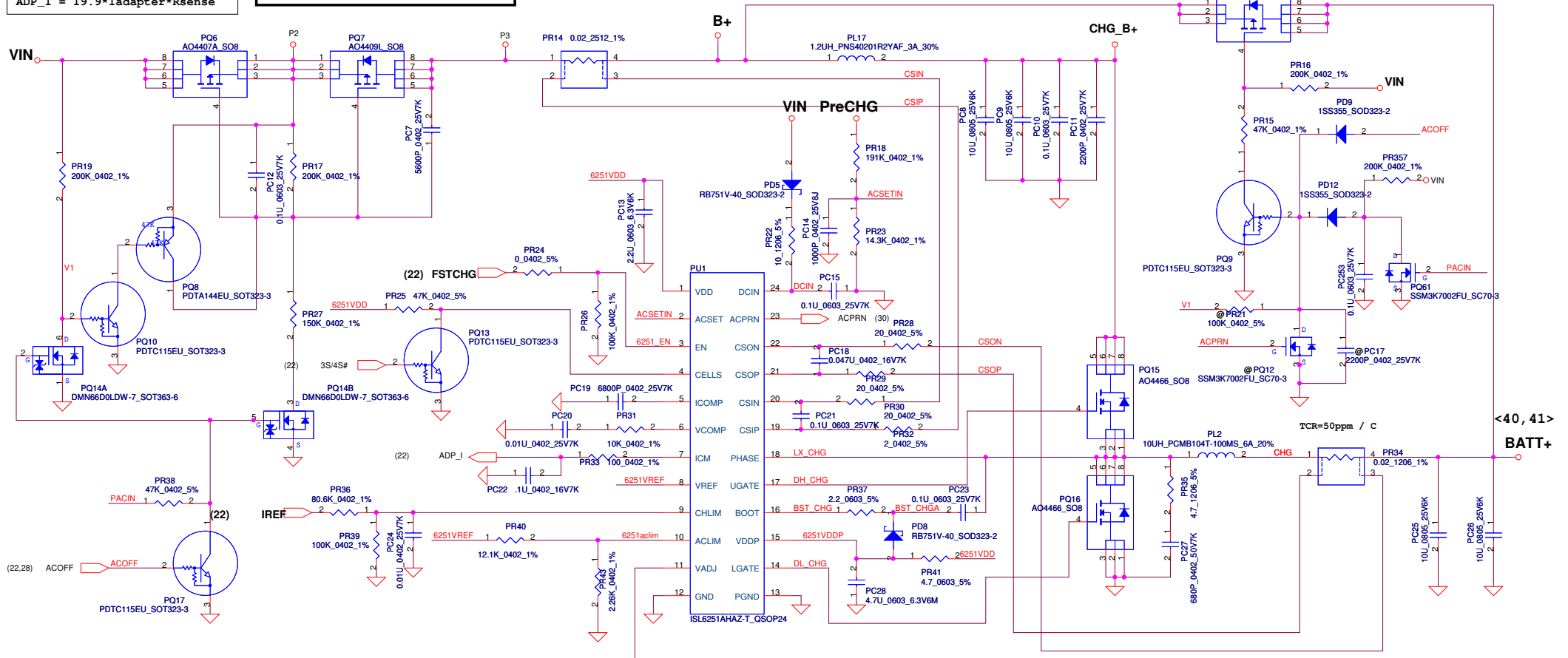


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Iada=0~3. 421A (40W/19V=3. 421A)

CP = 85%*Iada ; CP = 2.91A

ADP_I = 19.9*Iadapter*Rsense



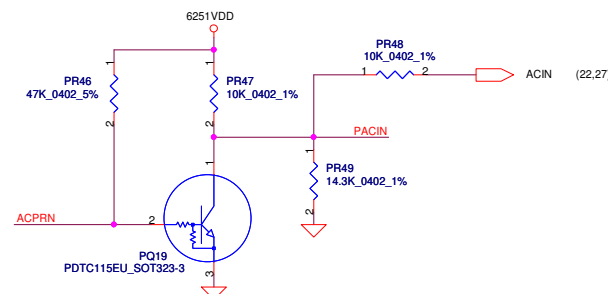
CP mode
 $I_{input} = (1/0.02) (0.02 * V_{ac1m} / 2.39 + 0.02)$
 where $V_{ac1m} = 0.396V$, $I_{input} = 2.91A$

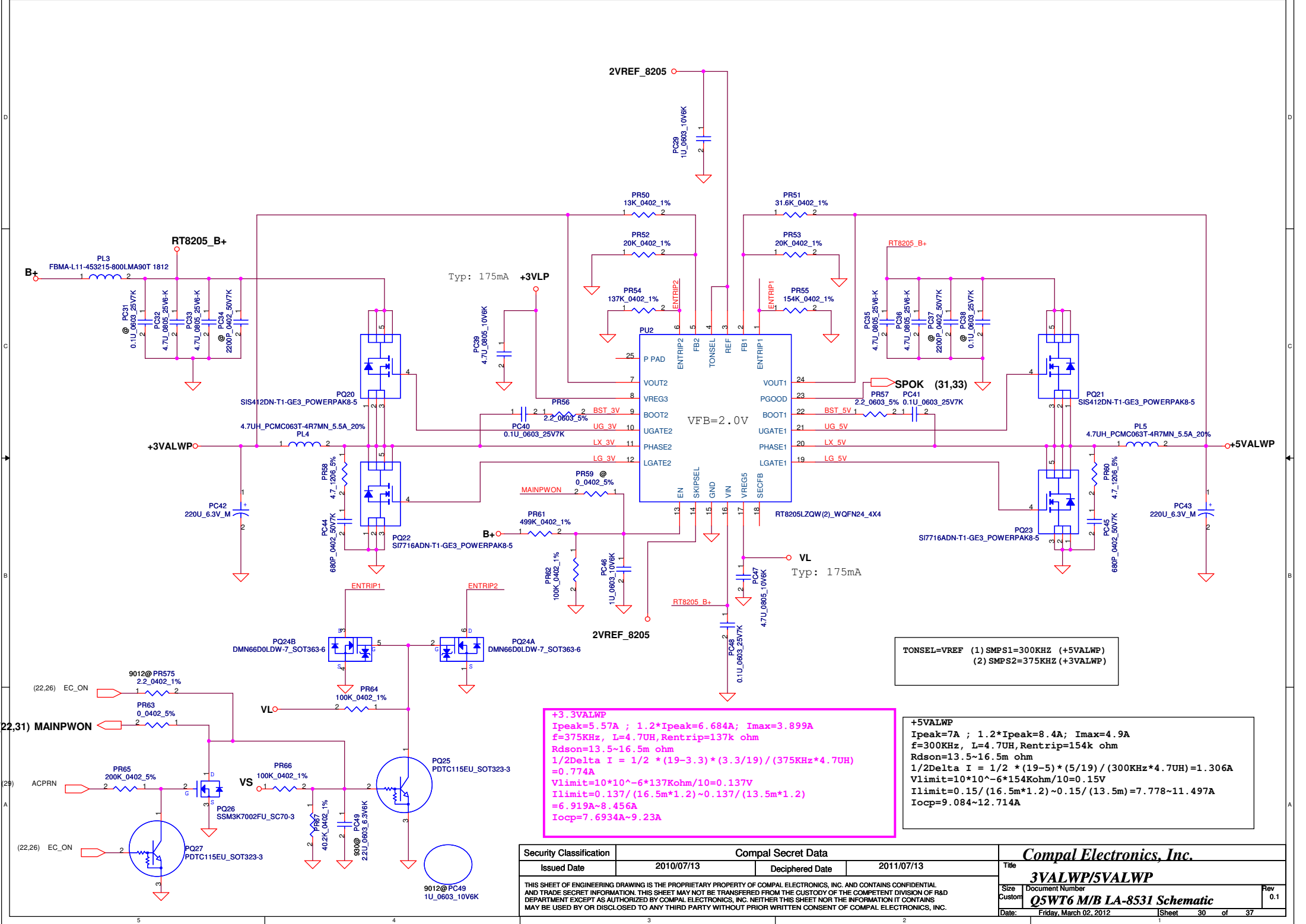
BATT Type	Charging Voltage (0x15)	CV mode
Normal 3S LI-ON Cells	12600mV	12.60V

CC=0.6~4.48A
 $I_{REF} = 0.7224 * I_{charge}$
 $I_{REF} = 0.43V \sim 3.24V$

Ki
 $V_{chlim} = I_{ref} * (PR374 / (PR372 + PR374))$
 $= I_{ref} * (100K / (80.6K + 100K))$
 $= I_{ref} * 0.5537$
 $I_{charge} = (165mV / PR369) * (V_{chlim} / 3.3V)$
 $= (165m / 20m) * (1 / 3.3V) * I_{ref} * 0.5537$
 $= 1.3842 * I_{ref}$
 $I_{ref} = 0.7224 * I_{charge} \Rightarrow Ki = 0.7224$

Kv
 $R_{internal} = 514K$ $R_{ec} = 3K$ $R1 = PR379 = 15.4K$ $R2 = PR381 = 31.6K$
 $R = 514K // 31.6K // (15.4K + 3K) = 11.372K$
 $r = 514K // 514K // 31.6K = 28.14K$
 $V_{cell} = 0.175 * V_{adj} + 3.99V$
 $4.2V = 0.175 * V_{adj} + 3.99V \Rightarrow V_{adj} = 1.2V$
 $V_{adj} = V_{ref} * (R / (R + 514K)) + CALIBRATE * (r / (r + 514K))$
 $1.1483 = CALIBRATE * 0.6046 \Rightarrow CALIBRATE = 1.899$
 $1.899 = (4.2 - (V_{cell} + A * 0.175)) * Kv = (4.2 - (4.2 + A * 0.175)) * Kv$
 $A = V_{ref} * (R / (R + 514K)) = 0.052$
 $Kv = 9.451$





Typ: 175mA +3VLP

VFB=2.0V

Typ: 175mA

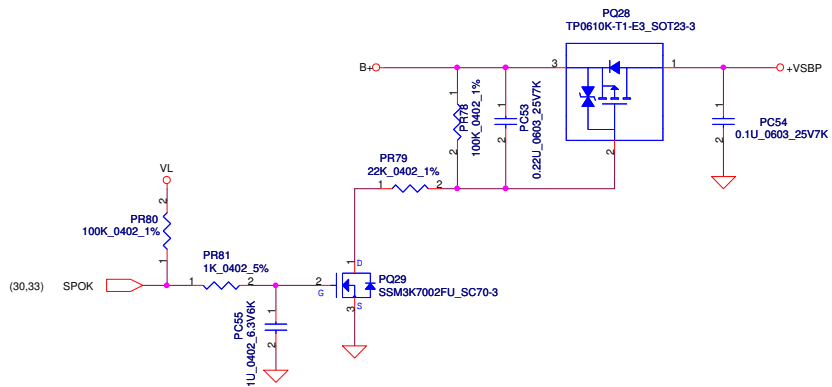
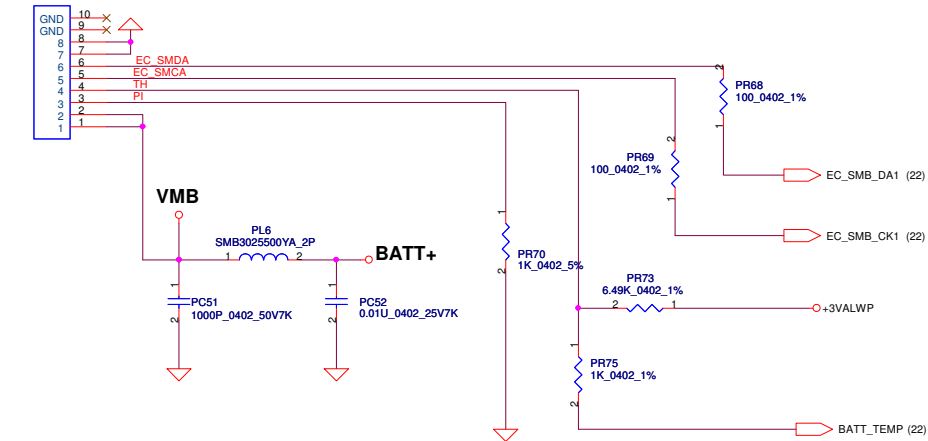
+3.3VALWP
 Ipeak=5.57A ; 1.2*Ipeak=6.684A; Imax=3.899A
 f=375KHz, L=4.7UH, Rentrip=137k ohm
 Rds(on)=13.5~16.5m ohm
 1/2Delta I = 1/2 *(19-3.3) *(3.3/19) / (375KHz*4.7UH)
 =0.774A
 Vlimit=10*10^-6*137Kohm/10=0.137V
 Ilimit=0.137/(16.5m*1.2)~0.137/(13.5m*1.2)
 =6.919A~8.456A
 Iocp=7.6934A~9.23A

TONSEL=VREF (1) SMPS1=300KHZ (+5VALWP)
 (2) SMPS2=375KHZ (+3VALWP)

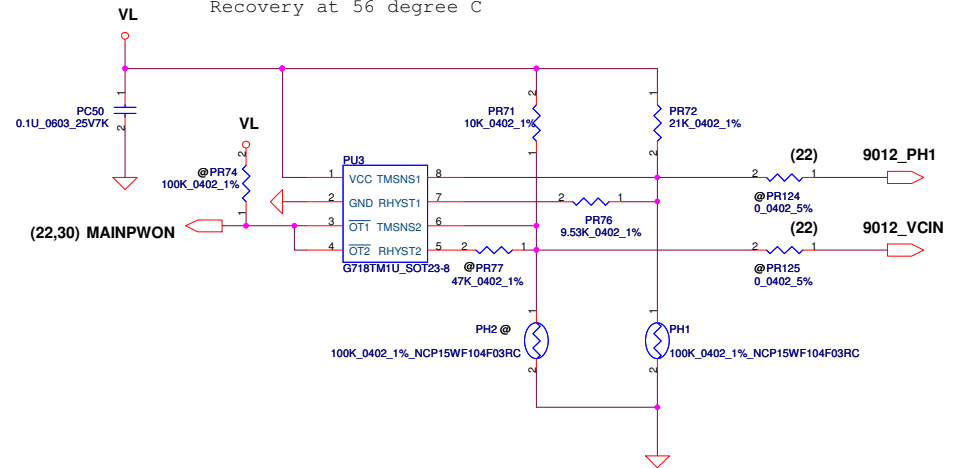
+5VALWP
 Ipeak=7A ; 1.2*Ipeak=8.4A; Imax=4.9A
 f=300KHz, L=4.7UH, Rentrip=154k ohm
 Rds(on)=13.5~16.5m ohm
 1/2Delta I = 1/2 *(19-5) *(5/19) / (300KHz*4.7UH)=1.306A
 Vlimit=10*10^-6*154Kohm/10=0.15V
 Ilimit=0.15/(16.5m*1.2)~0.15/(13.5m)=7.778~11.497A
 Iocp=9.084~12.714A

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CONN@_PJP2
SUYIN_201275GR008G13GZR



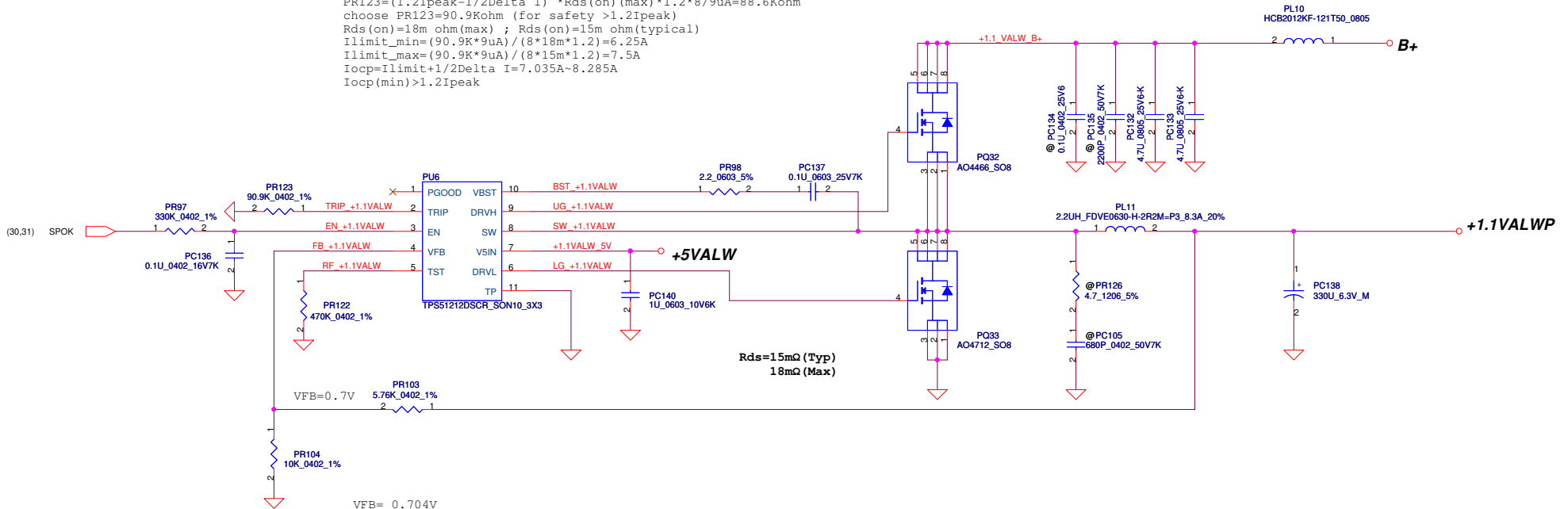
PH1 under CPU bottom side :
CPU thermal protection at 92 degree C
Recovery at 56 degree C



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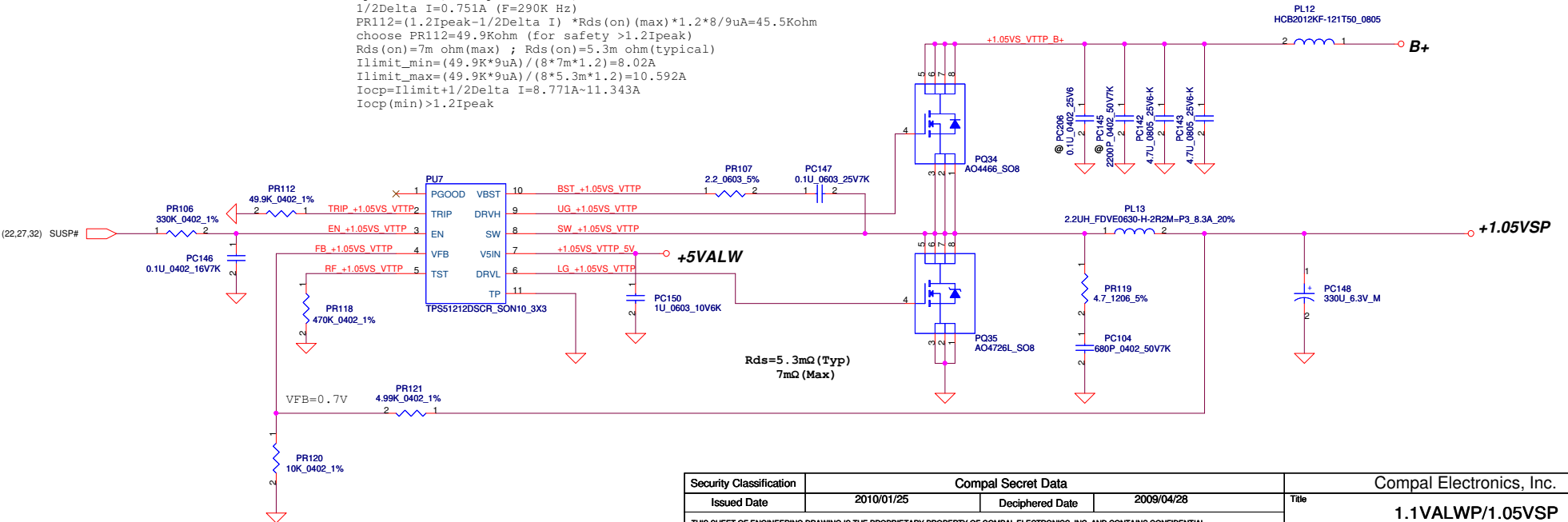
VFB= 0.704V
 $V_o = VFB * (1 + PR103 / PR104) = 1.103V$
 Freq= 266~314KHz , 290KHz (typ)

Ipeak=4.5A ; 1.2*Ipeak=5.4A ; Imax=3.15A
 $1/2\Delta I = 0.785A$ (F=290K Hz)
 $PR123 = (1.2 * I_{peak} - 1/2\Delta I) * R_{ds(on)}(max) * 1.2 * 8/9\mu A = 88.6K\Omega$
 choose PR123=90.9Kohm (for safety >1.2Ipeak)
 $R_{ds(on)} = 18m\Omega$ (max) ; $R_{ds(on)} = 15m\Omega$ (typical)
 $I_{limit_min} = (90.9K * 9\mu A) / (8 * 18m * 1.2) = 6.25A$
 $I_{limit_max} = (90.9K * 9\mu A) / (8 * 15m * 1.2) = 7.5A$
 $I_{ocp} = I_{limit} + 1/2\Delta I = 7.035A \sim 8.285A$
 $I_{ocp(min)} > 1.2 * I_{peak}$

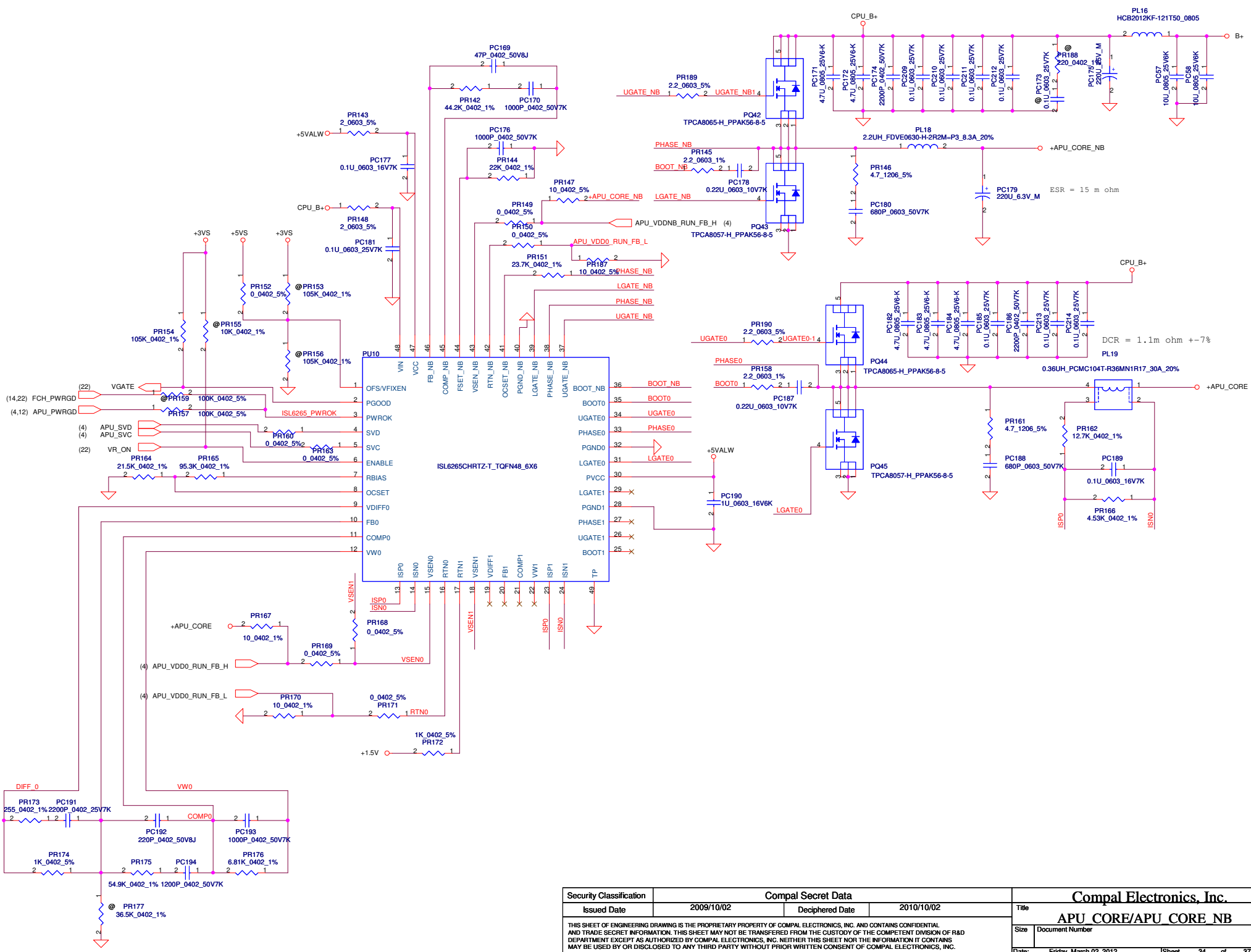


VFB= 0.704V
 $V_o = VFB * (1 + PR121 / PR120) = 1.05V$
 Freq= 266~314KHz , 290KHz (typ)

Ipeak=5.7A ; 1.2*Ipeak=6.84A ; Imax=3.899A
 $1/2\Delta I = 0.751A$ (F=290K Hz)
 $PR112 = (1.2 * I_{peak} - 1/2\Delta I) * R_{ds(on)}(max) * 1.2 * 8/9\mu A = 45.5K\Omega$
 choose PR112=49.9Kohm (for safety >1.2Ipeak)
 $R_{ds(on)} = 7m\Omega$ (max) ; $R_{ds(on)} = 5.3m\Omega$ (typical)
 $I_{limit_min} = (49.9K * 9\mu A) / (8 * 7m * 1.2) = 8.02A$
 $I_{limit_max} = (49.9K * 9\mu A) / (8 * 5.3m * 1.2) = 10.592A$
 $I_{ocp} = I_{limit} + 1/2\Delta I = 8.771A \sim 11.343A$
 $I_{ocp(min)} > 1.2 * I_{peak}$



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				Rev: 0.3

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		Modify 40W adapter CP point	0.1	29	PR14 change to SD00000CI10 (S RES 1/2W 0.05 +-1% 1206 100PPM/C) PR40 change to SD034470180 (S RES 1/16W 4.7K +-1% 0402)	2011/10/28	EVT
2		Modify +1.05VSP OCP	0.1	33	PR112 change to SD034499280 (S RES 1/16W 49.9K +-1% 0402)	2011/10/28	EVT
3		Modify +1.1VALWP OCP	0.1	33	PR123 change to SD034909280 (S RES 1/16W 90.9K +-1% 0402)	2011/10/28	EVT
4		Modify +1.5VP OCP	0.1	32	PR88 change to SD034681180 (S RES 1/16W 6.81K +-1% 0402)	2011/10/28	EVT
5		Modify ISN CHOKE P/N	0.1	29	PL17 change to SH00000N300 (S COIL 1.2UH +-30% PNS40201R2YAF 3A)	2011/10/28	EVT
6		Modify bead P/N	0.1	30	PL3 change to SM01000JF00 (S SUPPRE_ FBMA-L11-453215-800LMA90T 1812)	2011/10/28	EVT
7		Change boost resister from 0 ohm to 2.2 ohm for RT8207 & TPS51125	0.1	30	PR87 & PR98 & PR107 change from 0 ohm to 2.2 ohm	2011/11/17	EVT2
8		Modify power sequence for RT8207(+1.5VP & 0.75VSP)	0.1	30	PR91 change from 0 ohm to 200K ohm	2011/11/17	EVT2
9		Modify compoment P/N for material issue	0.1	29	PQ7 change from SB00000I600(S TR SI4459ADY-T1-GE3 1P SO8) to SB00000JD10 (S TR AO4409L 1P SO8)	2011/11/23	EVT2
10		design change for EC(9012)	0.1	28	delete PD1,PD2,PR1,PR2,PR4,PC6	2011/11/28	EVT2
11		design change for EC(9012)	0.1	29	add PR575(S RES 1/16W 2.2 +-1% 0402) PC49 change to 1U_0603_10V6K	2011/11/28	EVT2
12		design change for EC(9012)	0.1	31	add PR124(0_0402_5%)	2011/11/28	EVT2
13					change PR56,PR57 from 0 ohm to 2.2 ohm		
14		Improve EMI performance	0.2		add PR58,PR60,PR93,PR119 (SD001470B80,S RES 1/4W 4.7 +-5% 1206) add PC44,PC45,PC104 (SE074681K80,S CER CAP 680P 50V K X7R 0402) add PC130 (SE025681K80,S CER CAP 680P 50V K X7R 0603) change PR189,PR190 from 0 ohm to 2.2 ohm	2011/12/20	DVT
15							
16		Modify +5VALW voltage for USB port voltage drop (HW request +5VALW up 3%)	0.2	31	change PR51 from 30K ohm to 31.6K ohm	2011/12/20	DVT

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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		Modify compoment P/N for material shortage issue	0.2		change PC8,PC9,PC25,PC26,PC57,PC58 to SE00000QK00 (S CER CAP 10U 25V K X5R 0805 H1.25	2011/12/20	DVT
2		Change OTP from 9012 to G718	0.2	31	Delete PR124 (0_0402_5%)	2011/12/28	DVT
3		Change CP for 65W adapter	0.3	29	Change PR14 from SD00000CI10(S RES 1/2W 0.05 +-1% 1206 100PPM/C) to SD000001F00 (S RES 1W .02 +-1% 2512)	2012/2/6	PVT
4		Change CP for 65W adapter	0.3	29	Change PR40 from 4.7K to 4.7K Change PR43 from 20K to 2.26K	2012/2/6	PVT
5		Modify for compoment common P/N	0.3	32	change PQ36 from SB000009Q80 to SB000009610	2012/2/13	PVT
6		Modify for compoment P/N for cost concern	0.3	32	change PC128 from SGA00002280 (S POLY C 330U 2.5V Y D2 LESR15M CX H1.9) to SGA20331E10 (S POLY C 330U 2V Y D2 LESR9M EEFSX H1.9)	2012/2/24	PVT
7							
8							
9							
10							
11							
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	5	4	3	2	1
	<p>2011/10/06 P13. DEL net SMIB(R1219) for EMC request P17. change C940 to 120PF (SE00000U400) P23. modify C747-C772 BOM structure for ESD request P17. modify D58 BOM structure P19. modify D49 D51 BOM structure P20. modify D52 D55 D63 D68 BOM structure P24. modify D10 BOM structure</p>	<p>2011/12/16 ADD ZERO8,1,408,1,708 P04. modify R430,R431,R433,R434 0ohm symbol,change C237,C238 bom structure P09. modify R484 0ohm symbol P12. ADD GPIO30,GPIO31,modify R1503-R1508,R1510-R1513 0ohm symbol P13. change ODD_FWR to GPIO53 P14. DEL GPIO190 P17. modify R909,R1144 0ohm symbol P18. modify R1164 0ohm symbol P22. change R470 to 18K P26. change SW3 to @</p>	<p>2012/02/09 P13. add R1626</p> <p>2012/02/13 P13. change R1626 Bom structure update FWR schematic</p> <p>2012/03/02 P26. add H29 H30 for ME request update FWR schematic</p>		
D	<p>2011/10/11 P26. del H6 update PWR schematic</p> <p>2011/10/14 for ESD request P19. change D56 to SCA00001A00 update PWR schematic P25. change C1576 to 150UF P24. change JUSB1 to DC233007000</p>	<p>2011/12/19 P23. change LED1,2,4 to SC500005920 change LED3,5,6,7 to SC591TBKA10 P14. change ODD_DETECT# to U102_W7 change ODD_DA#_FCH to U102_P6</p>	<p>2012/03/05 P22. change R470 to 56K</p>		
	<p>2011/10/18 update PWR schematic</p> <p>2011/10/19 P02. update page no. P19. change U100,pin26 to AGND P21. add JTF2 P26. del H28,29 add H28_3P0 update PWR schematic</p>	<p>2011/12/21 update PWR schematic</p> <p>2011/12/22 for ESD request P06. add C1778,C1779 P12. add C1780 P15. add C1781 P22. add C1782 for small size request change Y6,Y7 to SJ10000E500</p>			
C	<p>2011/10/24 P09. R393 pin1 change to +3VS R396 change to 0402 size P27. R1101,R1102,R1110,R1120,R1128,R1135,R1137 change to 0402 size for EMC request P17. change C940 to 100pf SE00000U900</p>	<p>2011/12/23 P11. modify L57-L59 symbol P22. add R1611 pull high add R1612 pull GND</p>			
	<p>2011/10/26 for EMC request P27. modify C1457-C1460, Add C1686 for EC request P22. Add C1685 for FWR request P30. change PL3 to SM01000JF00</p>	<p>2011/12/28 P13. modify U103 to SA00003K800 P22. modify R1611,1612 BOM structure P23. change LED1,2,4 to SC500005930 update PWR schematic for EMI request P17. change T37,98 to SP050006H00 P18. change C1248,C1522 to 4.7P SE07147AB80 change R1808,R1168,R1165 to 10ohm SD028100A80 change C15198 to 10P SE071100J80 for ESD request P06. modify C1778 BOM structure P18. modify C1781 BOM structure P22. modify C1782 BOM structure</p>			
	<p>2011/10/28 P02. update block diagram P19. change JUMP location to J18-J23</p>				
	<p>2011/10/31 update PWR schematic</p>	<p>2012/01/20 add ODD# for normal ODD P12. Y7 change to SJ0000E800 P17. Y6 change to SJ0000E800 P18. C1522,C124 change to SE07147AC80 P21. change R955 to ODD# P22. change R470 to SD028330200 for FWT BOARD ID P23. R478,R498,R1217 change to SD028390080 P27. Del U95 R311,R499 change to SD00008H80 R1218 change to SD00003S80 P25. ADD +3VALW_WLAN net ADD J24,J25 jump</p>			
B	<p>2011/11/18 P12. Change chipset to M3L P14. Add GPIO189 for panel BOM control P22. co-lay KB930/9012 P23. update JTP1 footprint P25. Del JMINI2 P27. Del U95 update power schematic</p>				
	<p>2011/11/23 P23. D118, D138 for ESD P26. Add R1606 update power schematic</p>	<p>2012/02/01 P09. Add J24 for AOIC P17. Add R1613,C1783,Q1903,R1157 Add net LAN_FWR_EN# P22. Add net WLAN_FWR_ON,LAN_FWR_EN# EC_BT_OFF#,WLAN_PME# P25. Del Q137,D69,J24 and net BT_ON# Add net WLAN_PME#,EC_BT_OFF#,WLAN_FWR_ON Add R1620,R1618,C1785,R1619,Q1902,Q1904,R1617</p>			
	<p>2011/11/24b P24. modify JUSB2 net name P14. change EDP status to GPIO187 and modify H/L update power schematic</p>				
	<p>2011/11/25 P14. change LAN_CLKREQ# to U102.AG25 change MINI1_CLKREQ# to U102.AE24 P22. change VGRIT to U26.97 change ACTN to U26.110 change 3S/4S# to U26.98</p>	<p>2012/02/02 P25. ADD R1621 for RTC P12. C1704,C1705 change to SE071100J80 P17. C1485,C1486 change to SE071120J80</p>			
A	<p>2011/11/29 P11. change L57-L59 to SM010005220 for CRT issue P12. change U102 to SA00005DY10 P23. change SW1, SW2 to SN100000K00 update PWR schematic</p>	<p>2012/02/07 update POWER schematic update U22 to SA00005DX30,SA00005DW30 update U102 to SA00005DY70 P09. add R1621,C1786 P24. add R1622-24,C1787-89 P25. add R1625,C1790 del R1621 P04. del R169 change AMD Debug component to @</p>			

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