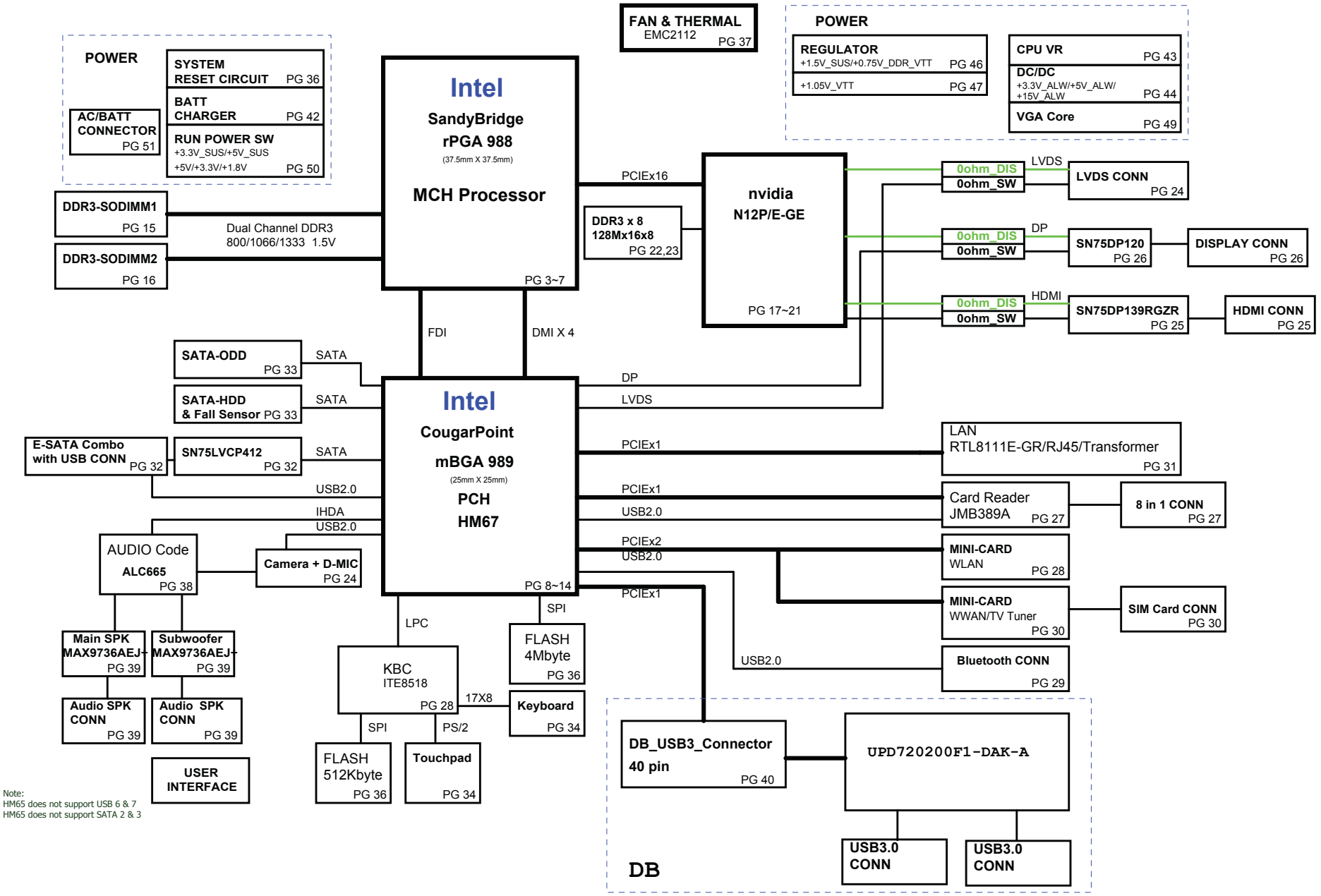
_DIS ==> Discrete Only
_SW ==> Optimus Only
_UMA ==> UMA Only

GM6C MLK Optimus, Discrete & UMA

VER : 1A
PWA:
PWB:



Note:
HM65 does not support USB 6 & 7
HM65 does not support SATA 2 & 3

Quanta Computer Inc.
PROJECT : GM6C MLK DIS

Size	Document Number	Rev
	Block Diagram	1A

Date: Friday, January 07, 2011 Sheet 1 of 59

Table of Contents

Power States

POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
+PWR_SRC	10V~+19V	24,30,45,46,47,48,49,50,51	MAIN POWER		S0~S5
+RTC_CELL	+3.0V~+3.3V	08,11,29,30	RTC		S0~S5
+5V_ALW2	+5V	37,46,52,53	LARGE POWER	MAIN POWER	S0~S5
+5V_ALW	+5V	13,33,44,46,47,48,49,50,51,52	LARGE POWER	ALW_ON	S0~S5
+3.3V_ALW	+3.3V	29,30,35,36,37,42,44,45,46,47,51,52,53	8051 POWER	3.3V_ALW_ON	S0~S5
+5V_SUS	+5V	11,33,34,37,51,52	SLP_S5# CTRLD POWER	SUS_ON	
+3.3V_SUS	+3.3V	07,08,09,10,11,13,14,19,24,28,29,37,41,42,44 ,48,49,50,52	SLP_S5# CTRLD POWER	SUS_ON	
+1.5V_SUS	+1.5V	03,05,13,14,47,50,52	SODIMM POWER	SUS_ON	
+0.75V_DDR_VTT	+0.75V	13,14,47,52	SODIMM POWER	RUN_ON	
+5V_RUN	+5V	11,18,24,25,35,36,38,39,40,51,52	SLP_S3# CTRLD POWER	RUN_ON	
+3.3V_RUN	+3.3V	3,7,8,9,10,11,13,14,15,17,24,25,26,28,29,30 ,31,32,33,35,37,38,39,40,41,42,46,51,52,60	SLP_S3# CTRLD POWER	RUN_ON	
+1.8V_RUN	+1.8V	05,11,44,52	SDVO POWER	RUN_ON	
+1.8V_RUN_GFX	+1.8V	17,18,21,22,44,52	VGA POWER	RUN_ON	
+1.5V_RUN	+1.5V	11,18,19,20,28,31,32,52	VGA POWER	RUN_ON	
+VCC_GFX_CORE	+0.9V~+1.2V	18,21,50	VGA POWER	RUN_ON	
+1.05V_PCH	+1.05V	08,09,11,15,48	PCH POWER	RUN_ON	
+VCC_CORE	+0.7V~+1.77V	05,51	CPU CORE POWER	IMVP_VR_ON	
+LCDVCC	+3.3V	24	LCD Power	LCDVCC_TST_EN & ENVDD	
+5V_MOD	+5V	35	MOD Power	MODC_EN	
+5V_HDD	+5V	35	HDD Power	HDDC_EN	
+1.1V_VTT	+1.1V	03,05,10,11,49,60	CPU POWER	RUN_ON	
+1.1V_GFX_PCIE	+1.1V	18,50	VGA POWER	GFX_ON	

GND PLANE	PAGE	DESCRIPTION
⏚ GND	ALL	

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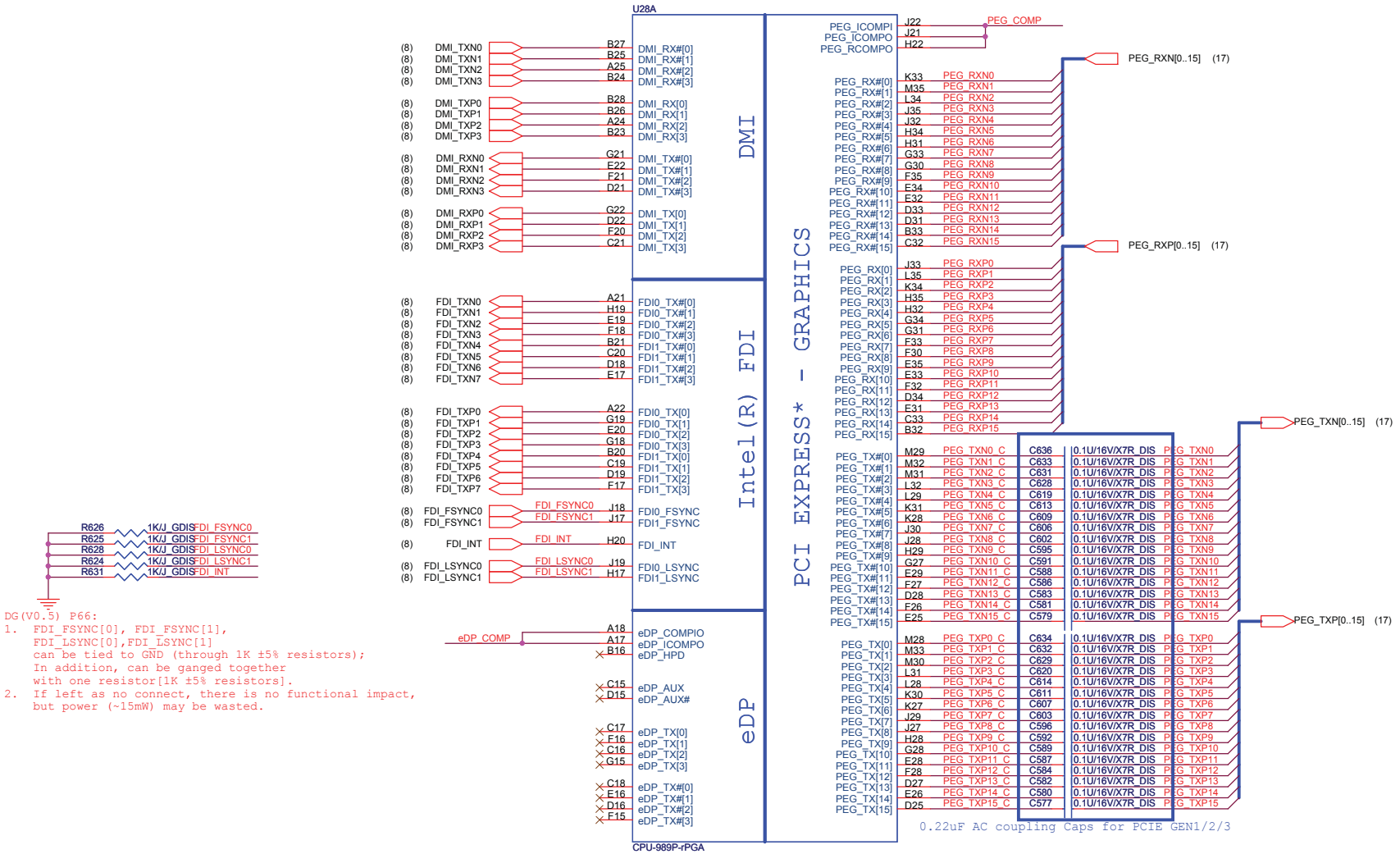
PROJECT : GM6C MLK DIS

Size	Document Number	Rev
	Frontage	1A

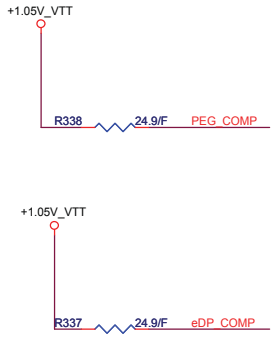
Date: Friday, January 07, 2011 Sheet 2 of 59

Sandy Bridge Processor (DMI,PEG,FDI)



DG(V0.5) P66:
1. FDI_FSYNC[0], FDI_FSYNC[1], FDI_LSYNC[0],FDI_LSYNC[1] can be tied to GND (through 1K ±5% resistors); In addition, can be ganged together with one resistor[1K ±5% resistors].
2. If left as no connect, there is no functional impact, but power (~15mW) may be wasted.

DP & PEG Compensation



Quanta Computer Inc.
PROJECT : GM6C MLK DIS

Size	Document Number	Rev
	Sandy Bridge 1/5	1A
Date: Friday, January 07, 2011	Sheet 3 of 59	

Sandy Bridge Processor (CLK,MISC,JTAG)

WW31.MOW Page 5 (SNB_IVB# N.A at SNB EDS #27637 0.7v1)

U28B

MISC: TP19 H_SNB_IVB# C26 PROC_SELECT#; (28) H_CPUDET# AN34 SKTOCC#

THERMAL: TP21 TP_CATERR# AL33 CATERR#; (28) EC_PECI R352 43/J H_PECI AN33 PECI; (28,42,43) VR_HOT# R358 56/J H_PROCHOT# AL32 PROCHOT#; (12) H_THERM# AN32 THERMTRIP#

shut down when asserted

Over 130 degree C will drive low

PWR MANAGEMENT: provide power management status (form PCH to CPU)

(8) PM_SYNC R372 *0/J_short_NC PM_SYNC_R AM34 PM_SYNC

(12) H_PWRGOOD R373 *0/J_short_NC PWRGOOD_R AP33 UNCOREPWRGOOD; R374 10K/J

PM_DRAM_PWRGD_R V8 SM_DRAMPWROK

+1.05V_VTT R368 *75/J_NC; CPU_PLTRST# R359 *43/J_NC CPU_PLTRST#_R AR33 RESET#

CLOCKS: BCLK A28, BCLK# A27 → CLK_CPU_BCLKP (10), CLK_CPU_BCLKN (10) DMI clock

DPLL_REF_CLK A16 CLK_DPLL_SSCLKP_R, DPLL_REF_CLK# A15 CLK_DPLL_SSCLKN_R; R629 Ra *0_NC → CLK_DPLL_SSCLKP (10), CLK_DPLL_SSCLKN (10) eDP clock

R627 Rb 1K/J, R630 Rc 1K/J → +1.05V_VTT

	DIS	SW
Ra	NA	0 ohm
Rb	1K ohm	NA
Rc	1K ohm	NA

DDR3 MISC: SM_DRAMRST# R8 CPU_DRAMRST# **S3 Power reduce**

SM_RCOMP[0] AK1 SM_RCOMP_0 R322 140/F; SM_RCOMP[1] A5 SM_RCOMP_1 R312 25.5/F; SM_RCOMP[2] A4 SM_RCOMP_2 R313 200/F **26.1 change to 25 ohm**

JTAG & BPM: PRDY# AP29, PREQ# AP27 XDP_PREQ# → T5

TCK AR26 XDP_TCK, TMS AR27 XDP_TMS, TRST# AP30 XDP_TRST#

TDI AR28 XDP_TDI, TDO AP26 → T2

DBR# AL35 → T11

BPM#[0] AT28 → T3; BPM#[1] AR29 → T6; BPM#[2] AR30 → T7; BPM#[3] AT30 → T10; BPM#[4] AP32 → T9; BPM#[5] AR31 → T4; BPM#[6] AT31 → T12; BPM#[7] AR32 → T8

CPU-989P-rPGA

+1.05V_VTT

XDP_TMS R364 51/J; XDP_TDI R363 51/J; XDP_PREQ# R365 *51/J_NC; XDP_TCLK R341 51/J; XDP_TRST# R375 51/J

Option for Prochot# function
68 ohm for unused, 62 ohm for used

+1.05V_VTT

H_PROCHOT# R367 *68/J_NC; VR_HOT# R366 62/J

IN	OUT
L	L
H	High-Z

+3.3V_SUS

C414 *0.1U/16V/X7R_NC

U19 *74LVC1G07GW_NC (NC, VCC, IN, GND, OUT)

(11,17,27,28,29,30,31,40) PLTRST#

CPU_PLTRST#

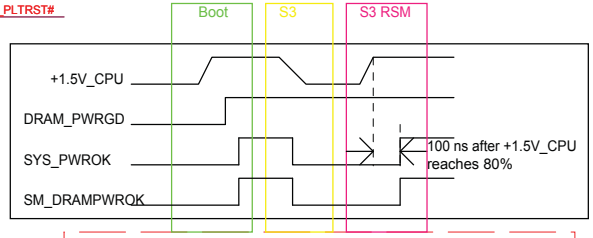
level shift for reset pin(07/12)

R714 1.5K/F

CPU_PLTRST#_R

R723 750/F

Pin1	Pin2	Pin4
L	L	L
L	H	L
H	L	L
H	H	High-Z



+1.5V_SUS keep DDR3_DRAMRST# high to avoid CPU_DRAMRST# low when into S3 (Because can't reset DRAM when into S3)

3/16 Change topology; Add AND gate based on DG rev0.9

+3.3V_SUS

C574 0.1U/16V/X7R

R489 200/J

(8) PM_DRAM_PWRGD

(8) SYS_PWROK

U27 74AHC1G09GW

PM_DRAM_PWRGD_Q

+1.5V_SUS_CPU

02/25 Update R8232, R8233 value and routing, Add R8583 follow PDG 0.71 #440484

R613 200/F

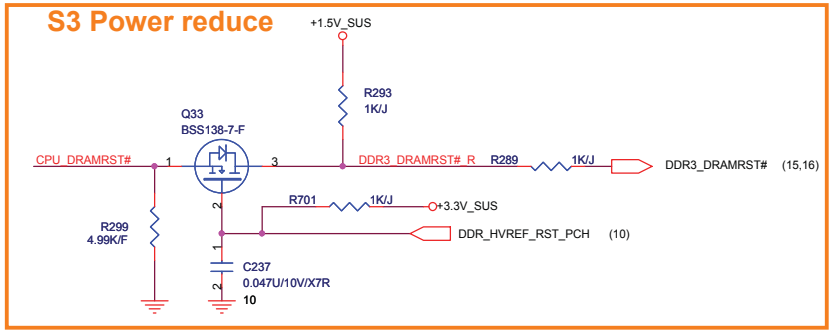
R615 130/F PM_DRAM_PWRGD_R

R616 *39/J_NC

Q68 *2N7002K_NC

PS_S3CNTRL (6,8,15)

S3 Power reduce



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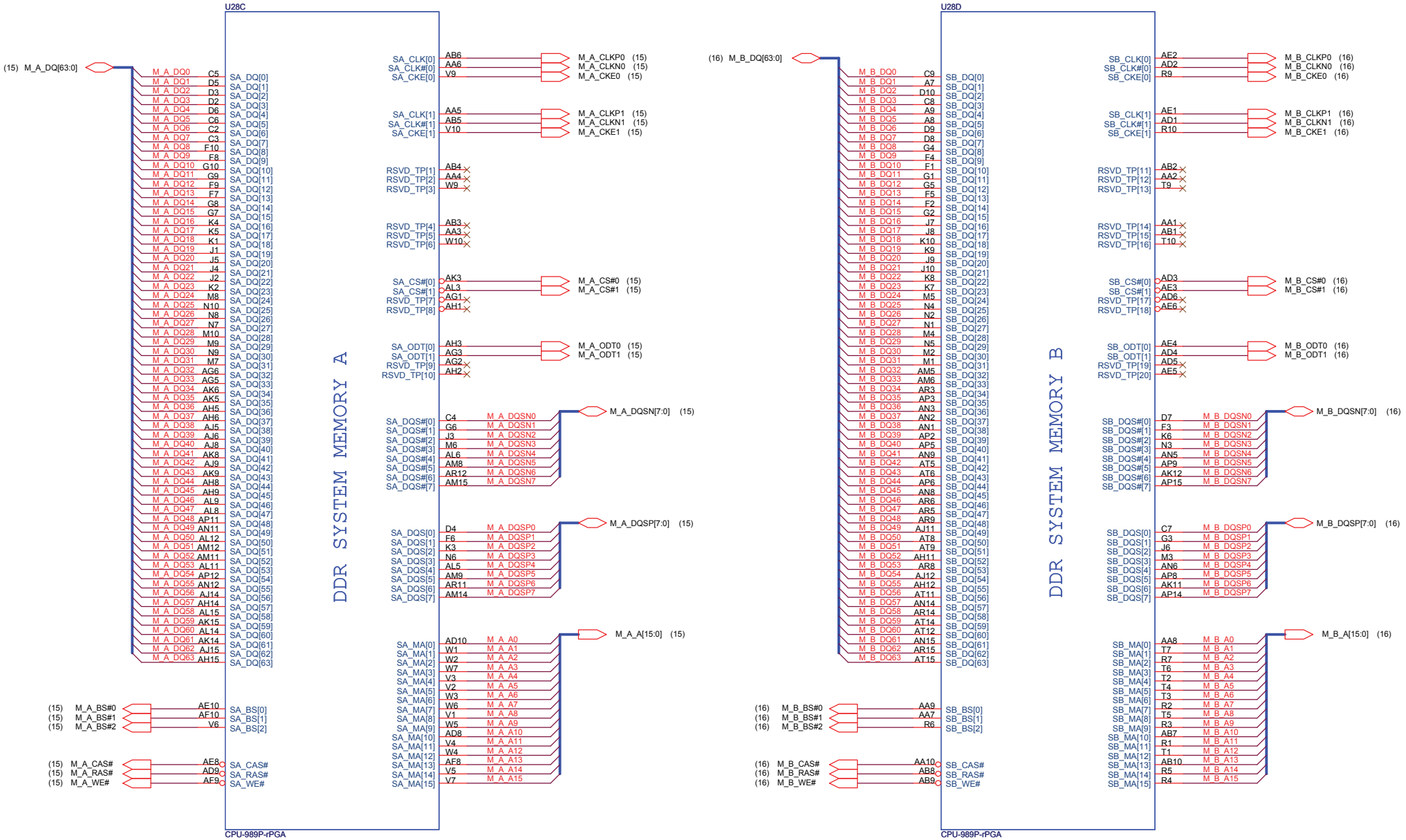
PROJECT : GM6C MLK DIS

Size	Document Number	Rev
	Sandy Bridge 2/5	1A

Date: Friday, January 07, 2011 Sheet 4 of 57

Sandy Bridge Processor (DDR3)



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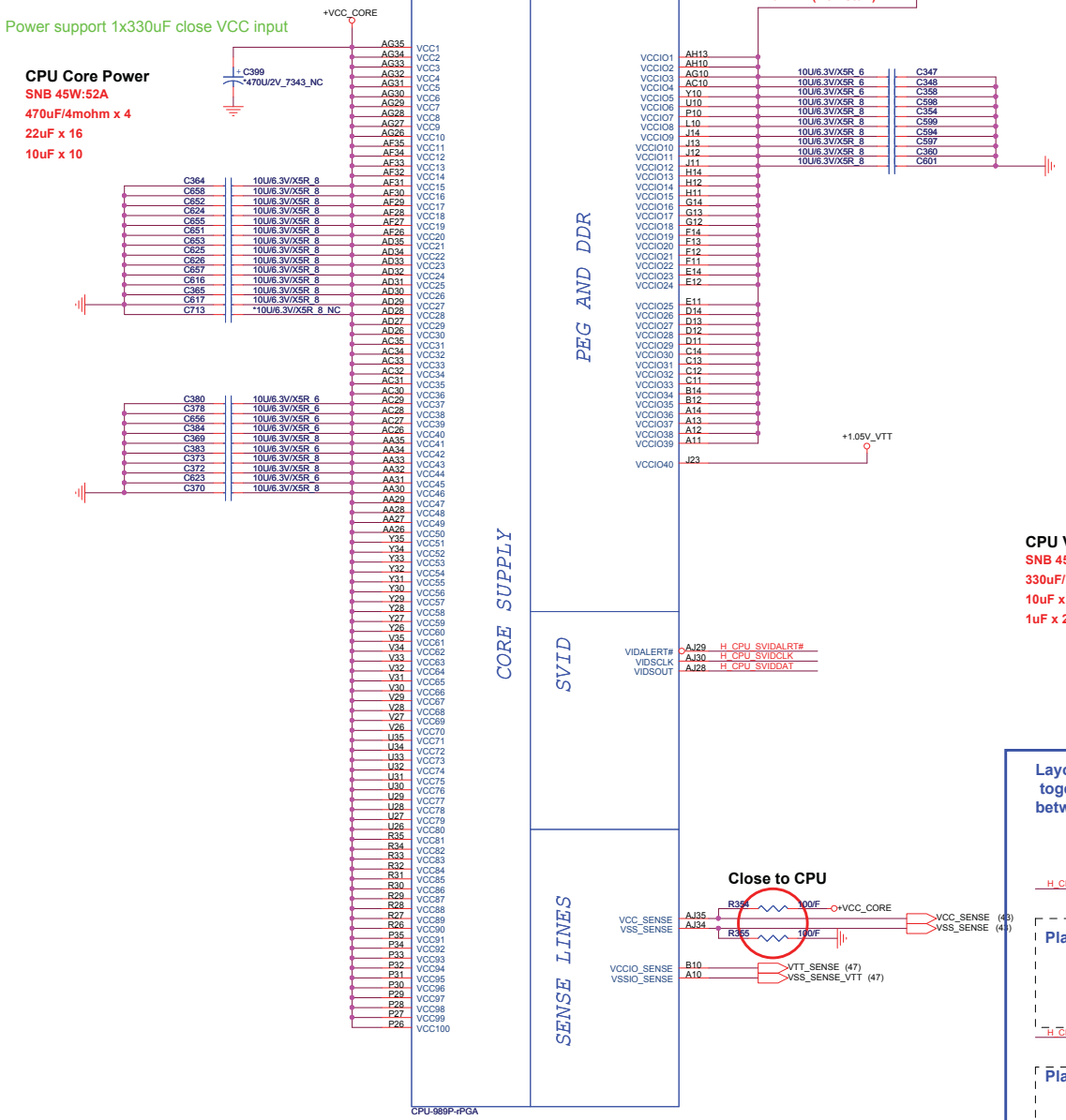
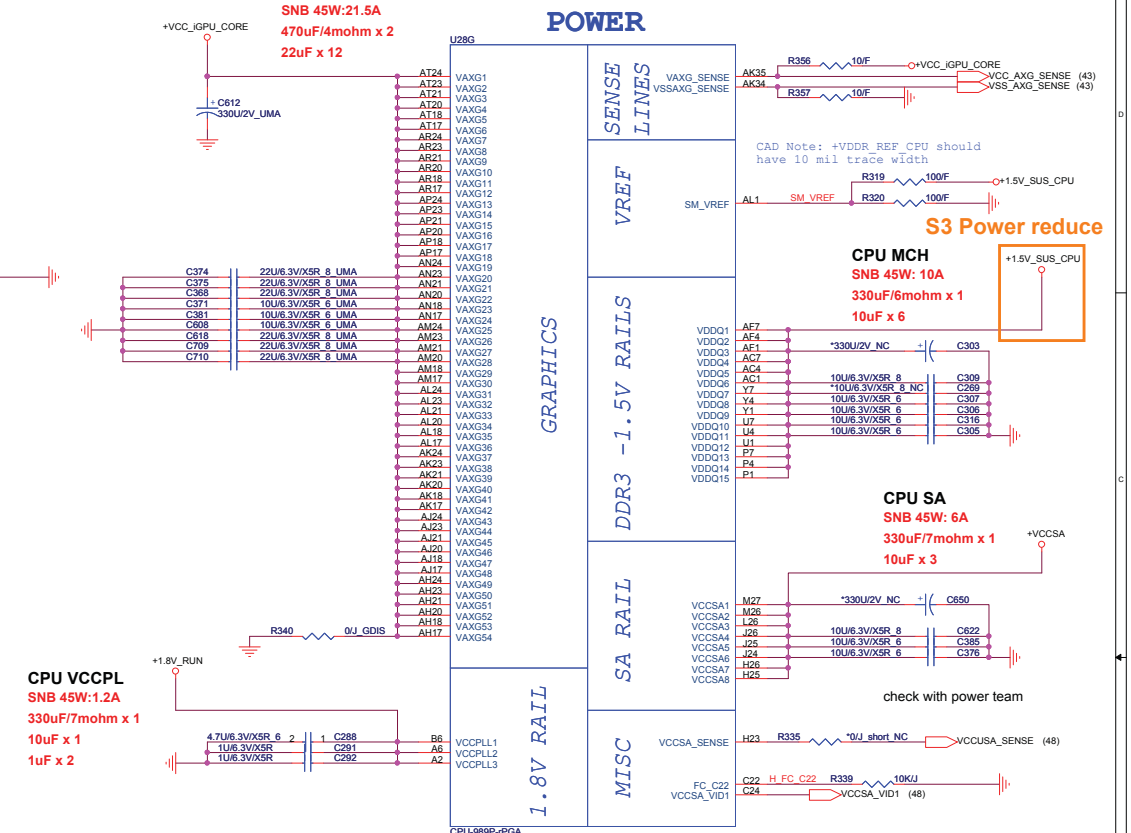
PROJECT : GM6C MLK DIS

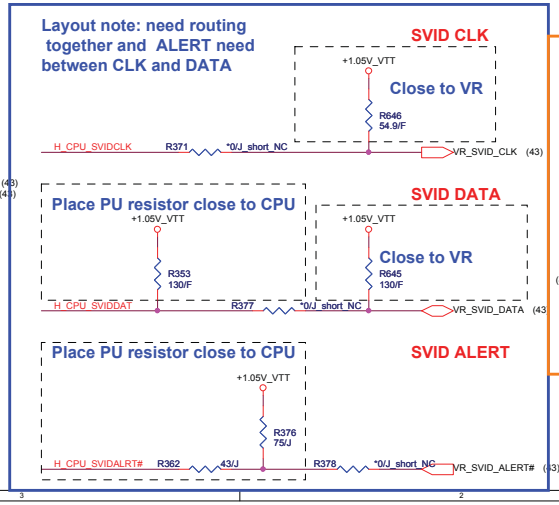
Size	Document Number	Rev
	Sandy Bridge 3/5	1A
Date: Friday, January 07, 2011	Sheet 5 of 59	

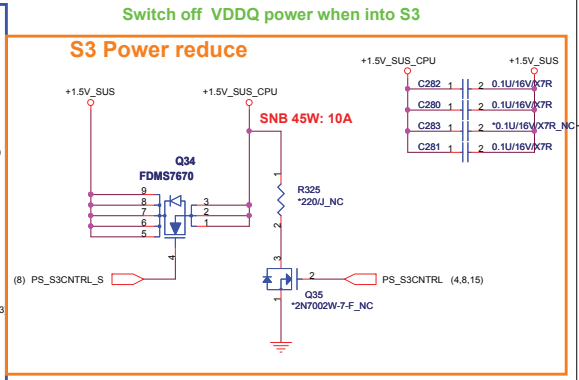
Sandy Bridge Processor (POWER)



Sandy Bridge Processor (GRAPHIC POWER)







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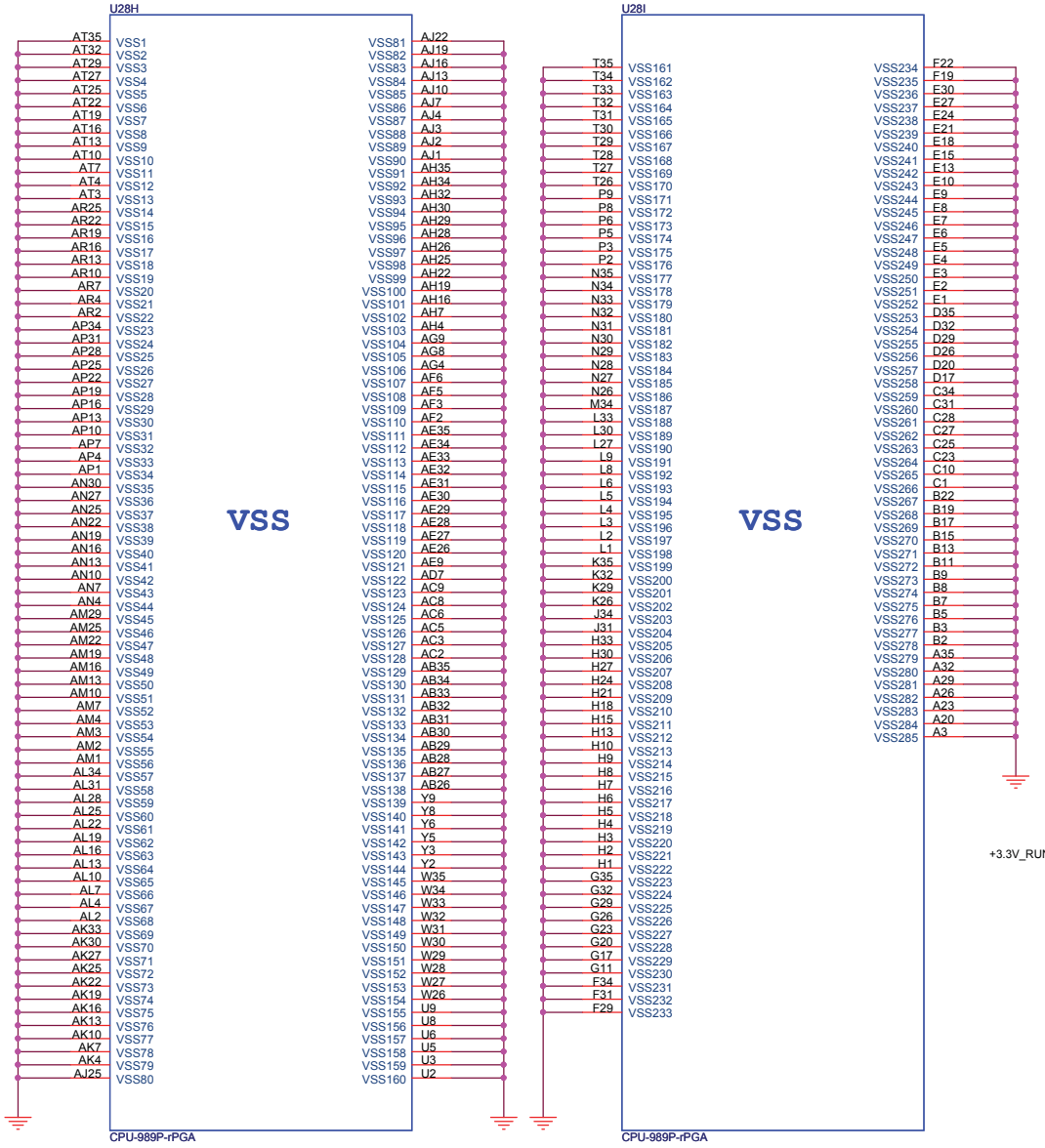
PROJECT : GM6C MLK DIS

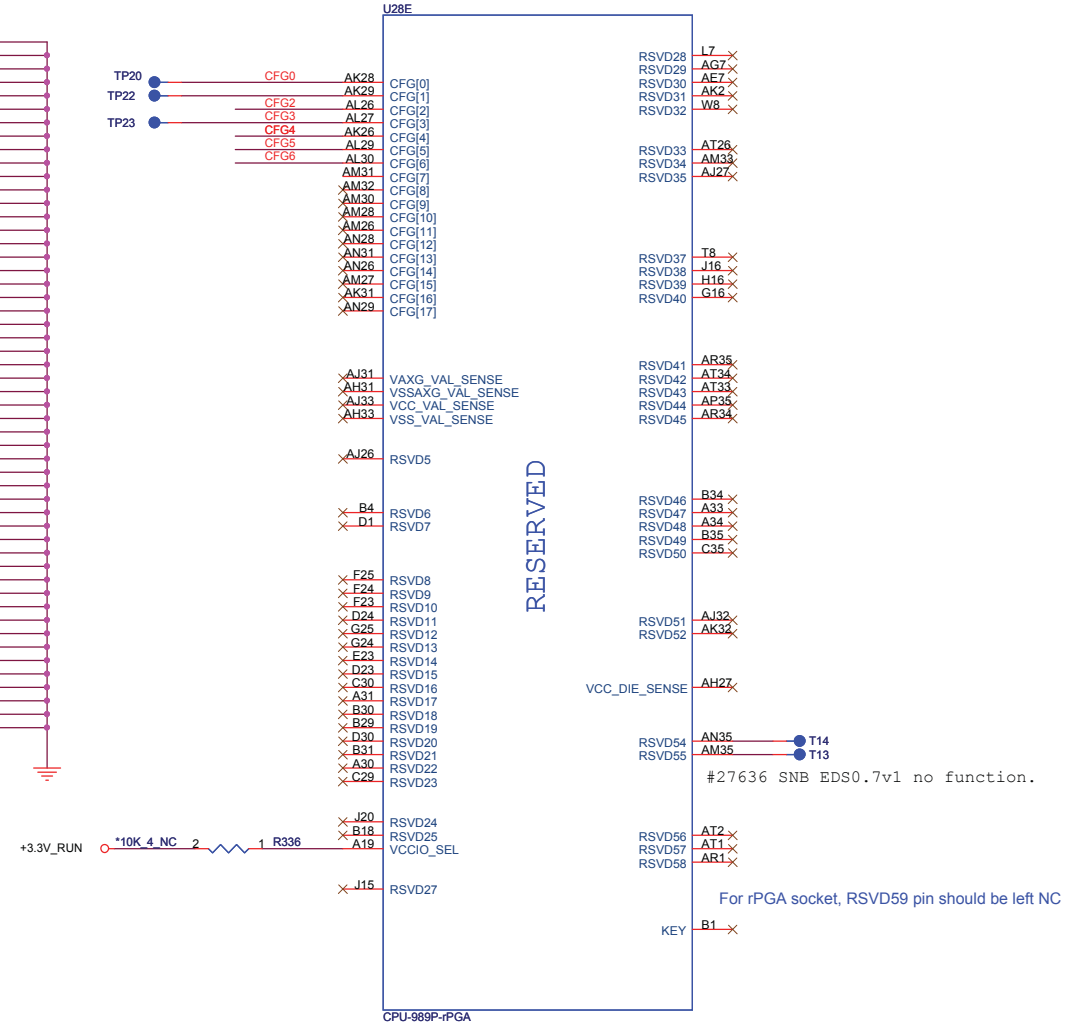
Size	Document Number	Rev
	Sandy Bridge 4/5	1A

Date: Friday, January 07, 2011 Sheet 6 of 59

Sandy Bridge Processor (GND)



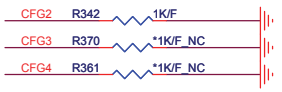
Sandy Bridge Processor (RESERVED, CFG)

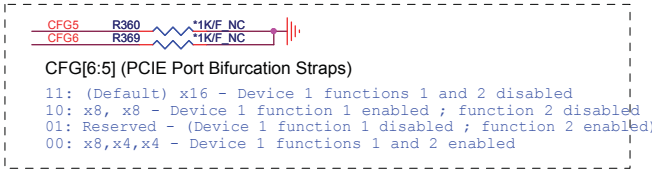


Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Number Reversed
CFG3 (PCI-E Static x4 Lane Reversal)	PCI-E Static x4 Lane Reversal	PEG wait for BIOS training
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP





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PROJECT : GM6C MLK DIS

Size	Document Number	Rev
	Sandy Bridge 5/5	1A

Date: Friday, January 07, 2011 Sheet 7 of 59

Cougar Point (DMI,FDI,PM)

U29C

+RTC_CELL
R703 330K/J
DSWVREN
R702 *330K/J_NC

On Die DSW VR Enable
High = Enable (Default)
Low = Disable

DMI_RXN0 (3) → BC24 DMI0RXN
DMI_RXN1 (3) → BE20 DMI1RXN
DMI_RXN2 (3) → BG18 DMI2RXN
DMI_RXN3 (3) → BG20 DMI3RXN
DMI_RXP0 (3) → BE24 DMI0RXP
DMI_RXP1 (3) → BC20 DMI1RXP
DMI_RXP2 (3) → BJ18 DMI2RXP
DMI_RXP3 (3) → BJ20 DMI3RXP
DMI_TXN0 (3) → AW24 DMI0TXN
DMI_TXN1 (3) → AW20 DMI1TXN
DMI_TXN2 (3) → BB18 DMI2TXN
DMI_TXN3 (3) → AV18 DMI3TXN
DMI_TXP0 (3) → AY24 DMI0TXP
DMI_TXP1 (3) → AY20 DMI1TXP
DMI_TXP2 (3) → AY18 DMI2TXP
DMI_TXP3 (3) → AU18 DMI3TXP

+1.05V_VTT — R379 49.9/F — DMI_COMP → BJ24 DMI_ZCOMP, BG25 DMI_IRCOMP
R641 750/F → BH21 DMI2RBIAS

FDI_RXN0 BJ14 ← FDI_TXN0_R
FDI_RXN1 AY14 ← FDI_TXN1_R
FDI_RXN2 BE14 ← FDI_TXN2_R
FDI_RXN3 BH13 ← FDI_TXN3_R
FDI_RXN4 BC12 ← FDI_TXN4_R
FDI_RXN5 BJ12 ← FDI_TXN5_R
FDI_RXN6 BG10 ← FDI_TXN6_R
FDI_RXN7 BG9 ← FDI_TXN7_R
FDI_RXP0 BG14 ← FDI_TXP0_R
FDI_RXP1 BB14 ← FDI_TXP1_R
FDI_RXP2 BF14 ← FDI_TXP2_R
FDI_RXP3 BG13 ← FDI_TXP3_R
FDI_RXP4 BE12 ← FDI_TXP4_R
FDI_RXP5 BG12 ← FDI_TXP5_R
FDI_RXP6 BJ10 ← FDI_TXP6_R
FDI_RXP7 BH9 ← FDI_TXP7_R

FDI_INT AW16 — FDI_INT_R — R387 0_UMA → FDI_INT (3)
FDI_FSYNC0 AV12 — FDI_FSYNC0_R — RP7 0_UMA → FDI_FSYNC0 (3)
FDI_FSYNC1 BC10 — FDI_FSYNC1_R — RP7 0_UMA → FDI_FSYNC1 (3)
FDI_LSYNC0 AV14 — FDI_LSYNC0_R — RP8 0_UMA → FDI_LSYNC0 (3)
FDI_LSYNC1 BB10 — FDI_LSYNC1_R — RP8 0_UMA → FDI_LSYNC1 (3)

RP16 0_UMA: FDI_TXN0_R / FDI_TXP0_R → FDI_TXN0 (3) / FDI_TXP0 (3)
RP6 0_UMA: FDI_TXN1_R / FDI_TXP1_R → FDI_TXN1 (3) / FDI_TXP1 (3)
RP5 0_UMA: FDI_TXN2_R / FDI_TXP2_R → FDI_TXN2 (3) / FDI_TXP2 (3)
RP13 0_UMA: FDI_TXN3_R / FDI_TXP3_R → FDI_TXN3 (3) / FDI_TXP3 (3)
RP4 0_UMA: FDI_TXN4_R / FDI_TXP4_R → FDI_TXN4 (3) / FDI_TXP4 (3)
RP15 0_UMA: FDI_TXN5_R / FDI_TXP5_R → FDI_TXN5 (3) / FDI_TXP5 (3)
RP14 0_UMA: FDI_TXN6_R / FDI_TXP6_R → FDI_TXN6 (3) / FDI_TXP6 (3)
RP17 0_UMA: FDI_TXN7_R / FDI_TXP7_R → FDI_TXN7 (3) / FDI_TXP7 (3)

PCH Pull-high/low(CLG)

+3.3V_RUN
CLKRUN# R666 10K/J
XDP_DBRST# R673 10K/J
R674 *1K/J_NC
RSMRST# R706 10K/J
SYS_PWROK_R R441 10K/J

+3.3V_SUS
PM_RI# R698 10K/J
PM_BATLOW# R483 10K/J
PCIE_WAKE# R696 10K/J
SUS_PWR_ACK R700 10K/J
AC_PRESENT R479 *10K/J_NC
PCH_GPIO29 R492 10K/J

SUS_PWR_ACK C12 → SUSACK#
XDP_DBRST# K3 → SYS_RESET# (T41, T26)
SYS_PWROK R450 *0/J_short_NC → SYS_PWROK_R P12 → SYS_PWROK
(28) EC_PWROK — R440 *0/J_NC, R435 *0/J_short_NC → PWROK_R L22 → PWROK
(28,36,37) HWPG — R431 *0/J_NC, R432 *0/J_short_NC → APWROK_R L10 → APWROK (T23, T24)
(4) PM_DRAM_PWRGD → PM_DRAM_PWRGD B13 → DRAMPWROK
(28) RSMRST# → RSMRST# C21 → RSMRST#
(28) SUS_PWR_ACK → SUS_PWR_ACK K16 → SUSWARN#/SUSPWRDNACK/GPIO30
(28) SIO_PWRBTN# — R484 *0/J_short_NC → PWRBTN# E20
(28) AC_PRESENT — T29 → AC_PRESENT H20 → ACPRESENT / GPIO31
PM_BATLOW# E10 → BATLOW# / GPIO72
PM_RI# A10 → RI#

System Power Management

DSWVRMEN A18 ← DSWVREN
DPWROK F22 — R705 *0/J_short_NC → RSMRST#
WAKE# B9 → PCIE_WAKE# → PCIE_WAKE# (40)
+3V CLKRUN# / GPIO32 N3 → CLKRUN# → CLKRUN# (28)
+3V_S5 SUS_STAT# / GPIO61 G8
+3V_S5 SUSCLK / GPIO62 N14 → SUSCLK → T21
+3V_S5 SLP_S5# / GPIO63 D10 → T1 → SIO_SLP_S5# (28,46)
SLP_S4# H4 → T25
+3V_S5 SLP_S3# F4 → T35 → SIO_SLP_S3# (28,46)
SLP_A# G10
SLP_SUS# G16
PMSYNCH AP14 → PM_SYNC (4)
+3V_S5 SLP_LAN# / GPIO29 K14 → PCH_GPIO29 → T30
DSW

CougarPoint_R1P0

S3 Power reduce

+5V_ALW
R496 10K/J
PS_S3CNTRL → PS_S3CNTRL (4,6,15)
SIO_SLP_S3# — R505 *10K/J_NC — Q49 BSS138-7-F

+15V_ALW
R490 100K/J
Q45 BSS138-7-F
PS_S3CNTRL_S (6)
PS_S3CNTRL — C478 *0.01U/25/X7R_NC 25

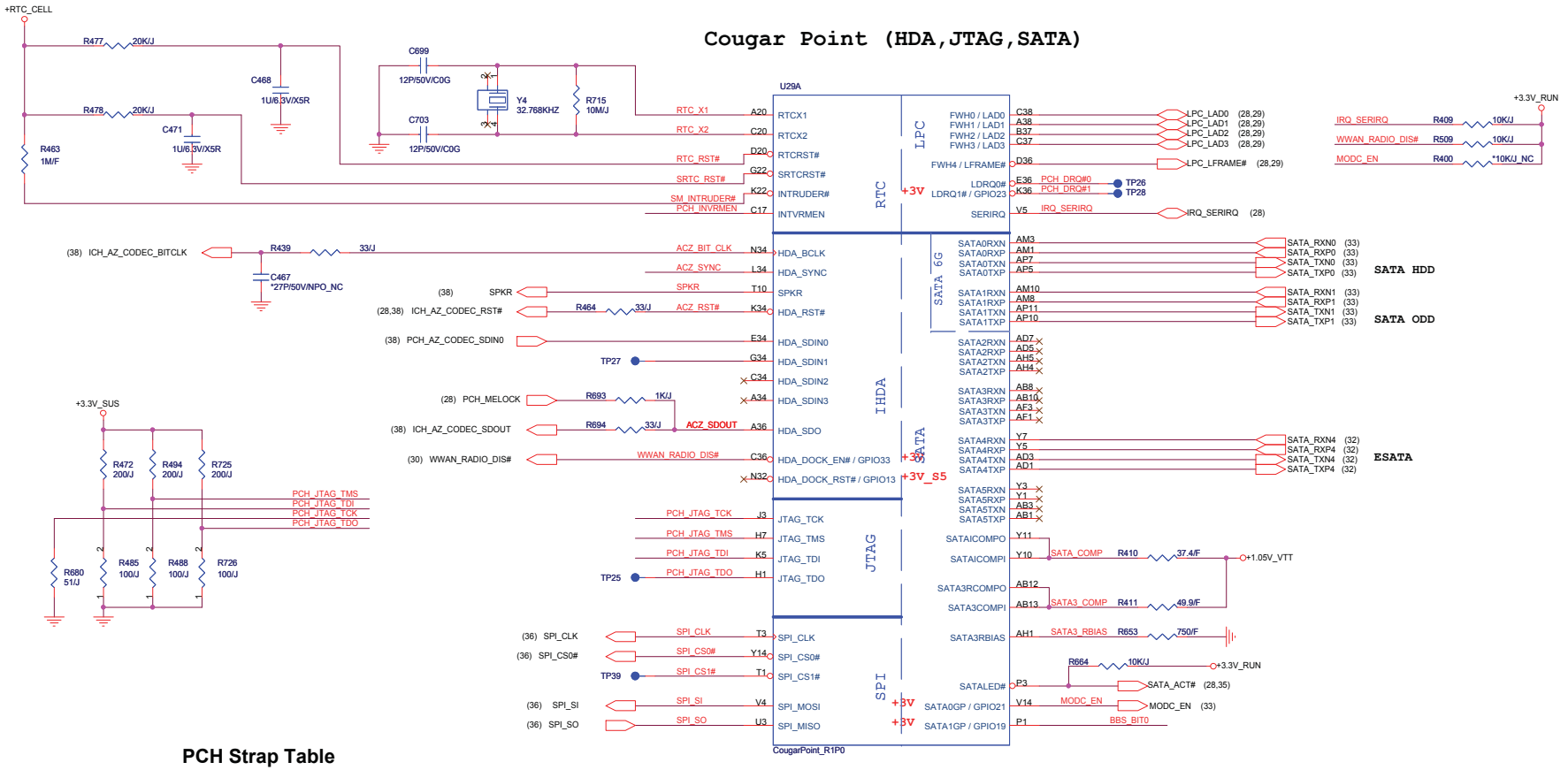
System PWR_OK(CLG)

+3.3V_SUS
C469 *0.1U/16V/X7R_NC
U20 TC7SH08FU
(4) SYS_PWROK → SYS_PWROK
IMVP_PWRGD (28,37,43)
EC_PWROK
R447 100K/J

Quanta Computer Inc.
PROJECT : GM6C MLK DIS

Size	Document Number	Rev
	Cougar Point 1/7	1A
Date: Friday, January 07, 2011	Sheet 8 of 59	

Cougar Point (HDA,JTAG,SATA)



PCH Strap Table

Pin Name	Strap description	Sampled	Configuration
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	**Default weak pull-up on GNT0/1#** **[Need external pull-down for LPC BIOS]**
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK	
HDA_SYNC	On-Die PLL VR Volatge Select	RSMRST	0 = Support by 1.8V (weak PD) 1 = Support by 1.5V
HDA_SDO	Flash Descriptor Security	PWROK	0 = Default (weak pull-down 20K) 1 = Override
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	**Should be always pull-up**
DF_TVS	DMI and FDI Tx/Rx Termination Voltage	PWROK	weak pull-down 20kohm **0 = Set to Vss** **1 = Set to Vcc (weak pull-down 20K)**

GNT1#	GNT0#	Boot Location
1	1	SPI *
0	0	LPC

Quanta Computer Inc.

PROJECT : GM6C MLK DIS

Size	Document Number	Rev
	Cougar Point 2/7	1A
Date: Friday, January 07, 2011	Sheet 9 of 59	

Cougar Point-M (PCI-E,SMBUS,CLK)

Note:Place TX DC blocking caps close to PCH.

U29B

Mini WWAN
(30) PCIE_RXN1 — BG34 PERN1
(30) PCIE_RXP1 — BJ34 PERP1
C402 0.1U/16V/X7R PCIE_TXN1_C — AV32 PETN1
C403 0.1U/16V/X7R PCIE_TXP1_C — AU32 PETP1
(30) PCIE_TXN1
(30) PCIE_TXP1

Mini WLAN
(29) PCIE_RXN2 — BE34 PERN2
(29) PCIE_RXP2 — BF34 PERP2
C400 0.1U/16V/X7R PCIE_TXN2_C — BB32 PETN2
C401 0.1U/16V/X7R PCIE_TXP2_C — AY32 PETP2
(29) PCIE_TXN2
(29) PCIE_TXP2

BG36 PERN3
BJ36 PERP3
AV34 PETN3
AU34 PETP3

USB 3.0
(40) PCIE_RXN4 — BF36 PERN4
(40) PCIE_RXP4 — BE36 PERP4
C405 0.1U/16V/X7R PCIE_TXN4_C — AY34 PETN4
C404 0.1U/16V/X7R PCIE_TXP4_C — BB34 PETP4
(40) PCIE_TXN4
(40) PCIE_TXP4

Card Reader
(27) PCIE_RXN5 — BG37 PERN5
(27) PCIE_RXP5 — BH37 PERP5
C407 0.1U/16V/X7R PCIE_TXN5_C — AY36 PETN5
C406 0.1U/16V/X7R PCIE_TXP5_C — BB36 PETP5
(27) PCIE_TXN5
(27) PCIE_TXP5

Giga Bit LOM
(31) PCIE_RXN6 — BJ38 PERN6
(31) PCIE_RXP6 — BG38 PERP6
C408 0.1U/16V/X7R PCIE_TXN6_C — AU36 PETN6
C409 0.1U/16V/X7R PCIE_TXP6_C — AV36 PETP6
(31) PCIE_TXN6
(31) PCIE_TXP6

BG40 PERN7
BJ40 PERP7
AY40 PETN7
BB40 PETP7

BE38 PERN8
BC38 PERP8
AW38 PETN8
AY38 PETP8

PCI-E*

+3V_S5

SMBUS
SMBALERT# / GPIO11 — E12 — RSV_SMBALERT#
SMBCLK — H14 — PCH_SMBCLK — PCH_SMBCLK (29)
SMBDATA — C9 — PCH_SMBDATA — PCH_SMBDATA (29)
SML0ALERT# / GPIO60 — A12 — DDR_HVREF_RST_PCH (4)
SML0CLK — C8 — SMB_CLK_ME0
SML0DATA — G12 — SMB_DATA_ME0
SML1ALERT# / PCHHOT# / GPIO74 — C13 — PCH_GPIO74
SML1CLK / GPIO58 — E14 — SMB_CLK_ME1
SML1DATA / GPIO75 — M16 — SMB_DATA_ME1

Controller Link
CL_CLK1 — M7
CL_DATA1 — T11
CL_RST1# — P10

CLOCKS
Y40 CLKOUT_PCIE0N
Y39 CLKOUT_PCIE0P
CLK_PEG0_REQ# — J2 — PCIECLKRQ0# / GPIO73 — +3V_S5
PEG_A_CLKRQ# / GPIO47 — M10 — PEG_CLKREQ# — PEG_CLKREQ# (17)
CLKOUT_PEG_A_N — AB37 — CLK_PCIE_VGAN (17)
CLKOUT_PEG_A_P — AB38 — CLK_PCIE_VGAP (17)

Mini WLAN
(29) CLK_PCIE_MINI1N — AB49 CLKOUT_PCIE1N
(29) CLK_PCIE_MINI1P — AB47 CLKOUT_PCIE1P
(29) MINI1CLK_REQ# — MINI1CLK_REQ# — M1 — PCIECLKRQ1# / GPIO18 — +3V
CLKOUT_DMI_N — AV22 — CLK_CPU_BCLKN (4)
CLKOUT_DMI_P — AU22 — CLK_CPU_BCLKP (4)

Card Reader
(27) CLK_PCIE_CRN — AA48 CLKOUT_PCIE2N
(27) CLK_PCIE_CRP — AA47 CLKOUT_PCIE2P
CLKOUT_DP_N — AM12 — CLK_DPLL_SSCLKN (4)
CLKOUT_DP_P — AM13 — CLK_DPLL_SSCLKP (4)

Enable Free-Running
(confirm with BIOS) 0628
CLK_PCIE_REQ2# — V10 — PCIECLKRQ2# / GPIO20 — +3V
CLKIN_DMI_N — BF18 CLK_BUF_PCIE_3GPLLN — R381 10K/J
CLKIN_DMI_P — BE18 CLK_BUF_PCIE_3GPLLP — R383 10K/J

Mini WWAN
(30) CLK_PCIE_MINI3N — Y37 CLKOUT_PCIE3N
(30) CLK_PCIE_MINI3P — Y36 CLKOUT_PCIE3P
(30) MINI2CLK_REQ# — MINI2CLK_REQ# — A8 — PCIECLKRQ3# / GPIO25 — +3V_S5
CLKIN_GND1_N — BJ30 CLK_BUF_BCLKN — R642 10K/J
CLKIN_GND1_P — BG30 CLK_BUF_BCLKP — R643 10K/J

USB3.0
(40) CLK_PCIE_USB30N — Y43 CLKOUT_PCIE4N
(40) CLK_PCIE_USB30P — Y45 CLKOUT_PCIE4P
(40) CLK_PCIE_USB30_REQ# — CLK_PCIE_USB30_REQ# — L12 — PCIECLKRQ4# / GPIO26 — +3V_S5
CLKIN_DOT_96N — G24 CLK_BUF_DREFCLKN — R453 10K/J
CLKIN_DOT_96P — E24 CLK_BUF_DREFCLKP — R452 10K/J

Giga Bit LOM
(31) CLK_PCIE_LOMN — V45 CLKOUT_PCIE5N
(31) CLK_PCIE_LOMP — V46 CLKOUT_PCIE5P
(31) LOM_CLK_REQ# — LOM_CLK_REQ# — L14 — PCIECLKRQ5# / GPIO44 — +3V_S5
CLKIN_SATA_N — AK7 CLK_BUF_DREFSSCLKN — R403 10K/J
CLKIN_SATA_P — AK5 CLK_BUF_DREFSSCLKP — R402 10K/J

REFCLK14IN — K45 CLK_PCH_14M — R434 10K/J
CLKIN_PCILOOPBACK — H45 CLK_PCI_FB — CLK_PCI_FB (11)

AB42 CLKOUT_PEG_B_N
AB40 CLKOUT_PEG_B_P
PEG_B_CLKRQ# — E6 — PEG_B_CLKRQ# / GPIO56 — +3V_S5
XTAL25_IN — V47 XTAL25_IN
XTAL25_OUT — V49 XTAL25_OUT

T18 CLK_PCH_SRC6N — V40 CLKOUT_PCIE6N
T19 CLK_PCH_SRC6P — V42 CLKOUT_PCIE6P
XCLK_RCOMP — Y47 XCLK_RCOMP — R661 90.9/F — +1.05V_VTT
CLK_PCIE_REQ6# — T13 — PCIECLKRQ6# / GPIO45 — +3V_S5

V38 CLKOUT_PCIE7N
V37 CLKOUT_PCIE7P
CLK_PCIE_REQ7# — K12 — PCIECLKRQ7# / GPIO46 — +3V_S5

T16 CLK_PCIE_XDPN — AK14 CLKOUT_ITPXDP_N
T15 CLK_PCIE_XDPP — AK13 CLKOUT_ITPXDP_P

FLEX CLOCKS
+3V CLKOUTFLEX0 / GPIO64 — K43 — HDMI_PWR_CTRL — HDMI_PWR_CTRL (25)
+3V CLKOUTFLEX1 / GPIO65 — F47 — CLK_VGA_27M_R — R684 22/J_GDIS — CLK_VGA_27M (19)
+3V CLKOUTFLEX2 / GPIO66 — H47 — TEST_WOOFER_EN — TEST_WOOFER_EN (39)
+3V CLKOUTFLEX3 / GPIO67 — K49 — CLK_VGA_27M_SS_R — R442 *22/J_NC — CLK_VGA_27M_SS (19)

CougarPoint_R1P0

+3V_SUS
PCH_SMBCLK 2.2K/F R482
PCH_SMBDATA 2.2K/F R697
SMB_CLK_ME0 2.2K/F R713
SMB_DATA_ME0 2.2K/F R476
SMB_CLK_ME1 2.2K/F R462
SMB_DATA_ME1 2.2K/F R457
RSV_SMBALERT# 10K/F R471
PCH_GPIO74 10K/F R712

WLAN, WWAN, DIMM0, DIMM1, 3-axis fall sensor

+3.3V_SUS
Q43 2N7002W-7-F
SMB_CLK_ME1 — SMBCLK1 (28)
+3.3V_SUS
Q42 2N7002W-7-F
SMB_DATA_ME1 — SMBDAT1 (28)

EC

PCIE Clock Request

+3.3V_SUS
R695 10K/J MINI2CLK_REQ#
R685 10K/J CLK_PEG0_REQ#
R481 10K/J LOM_CLK_REQ#
R475 10K/J PEG_B_CLKRQ#
R473 10K/J PEG_CLKREQ#
R451 10K/J CLK_PCIE_REQ6#
R467 10K/J CLK_PCIE_USB30_REQ#
R480 10K/J CLK_PCIE_REQ7#

+3.3V_RUN
R436 10K/J HDMI_PWR_CTRL
R667 10K/J MINI1CLK_REQ#
R405 10K/J CLK_PCIE_REQ2#

PCIECLKRQ{0,3,4,5,6,7}# should have a 10K pull-up to +V3.3A.PCIECLKRQ{1,2} should have a 10K pull-up to +3.3S

Change as big package (UM9)

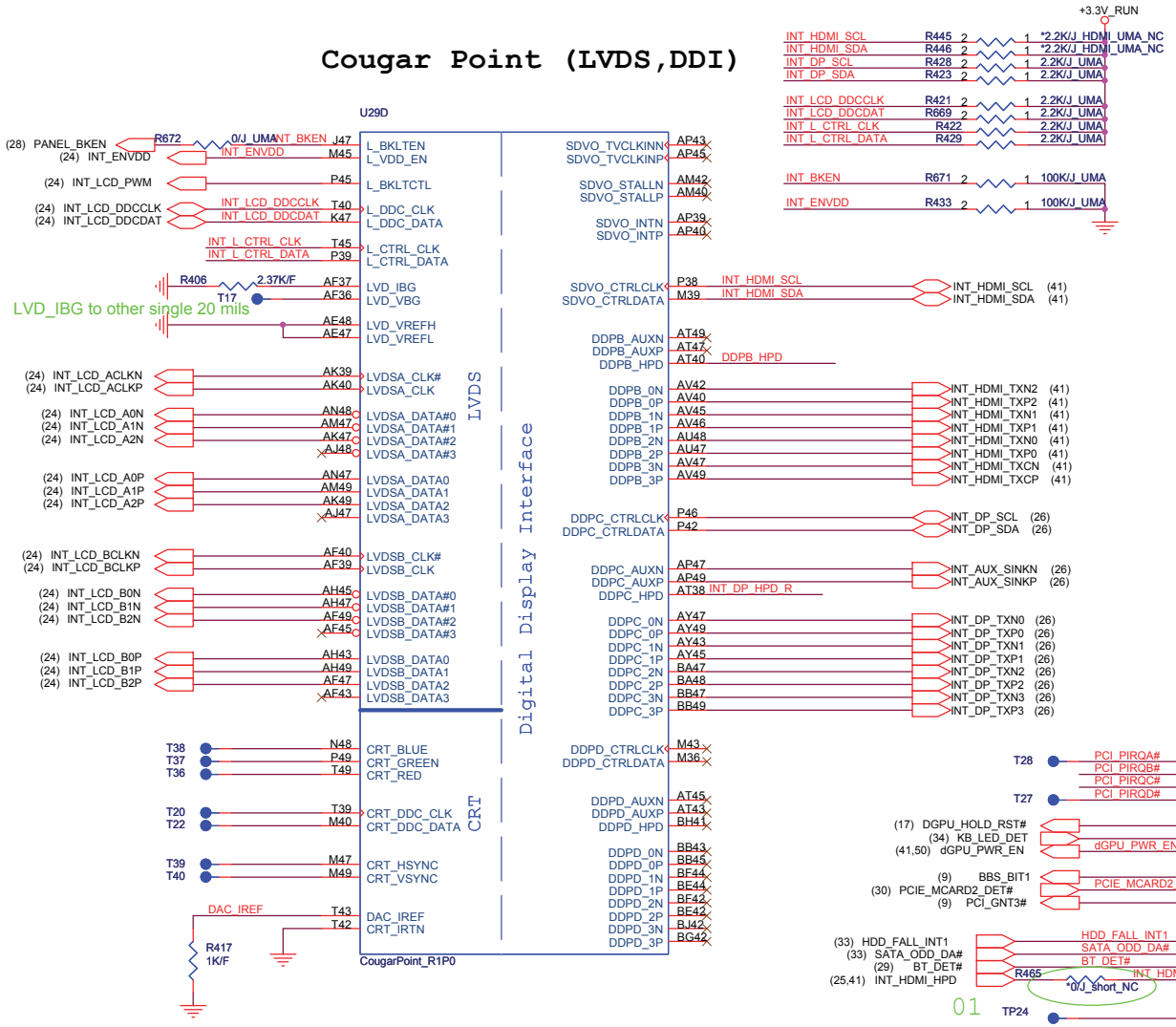
25MHz Clock for DCI Function

XTAL25_IN — R662 1M/J — XTAL25_OUT
Y3 25MHz
C683 22P/50V/NPO
C685 22P/50V/NPO

Quanta Computer Inc.
PROJECT : GM6C MLK DIS

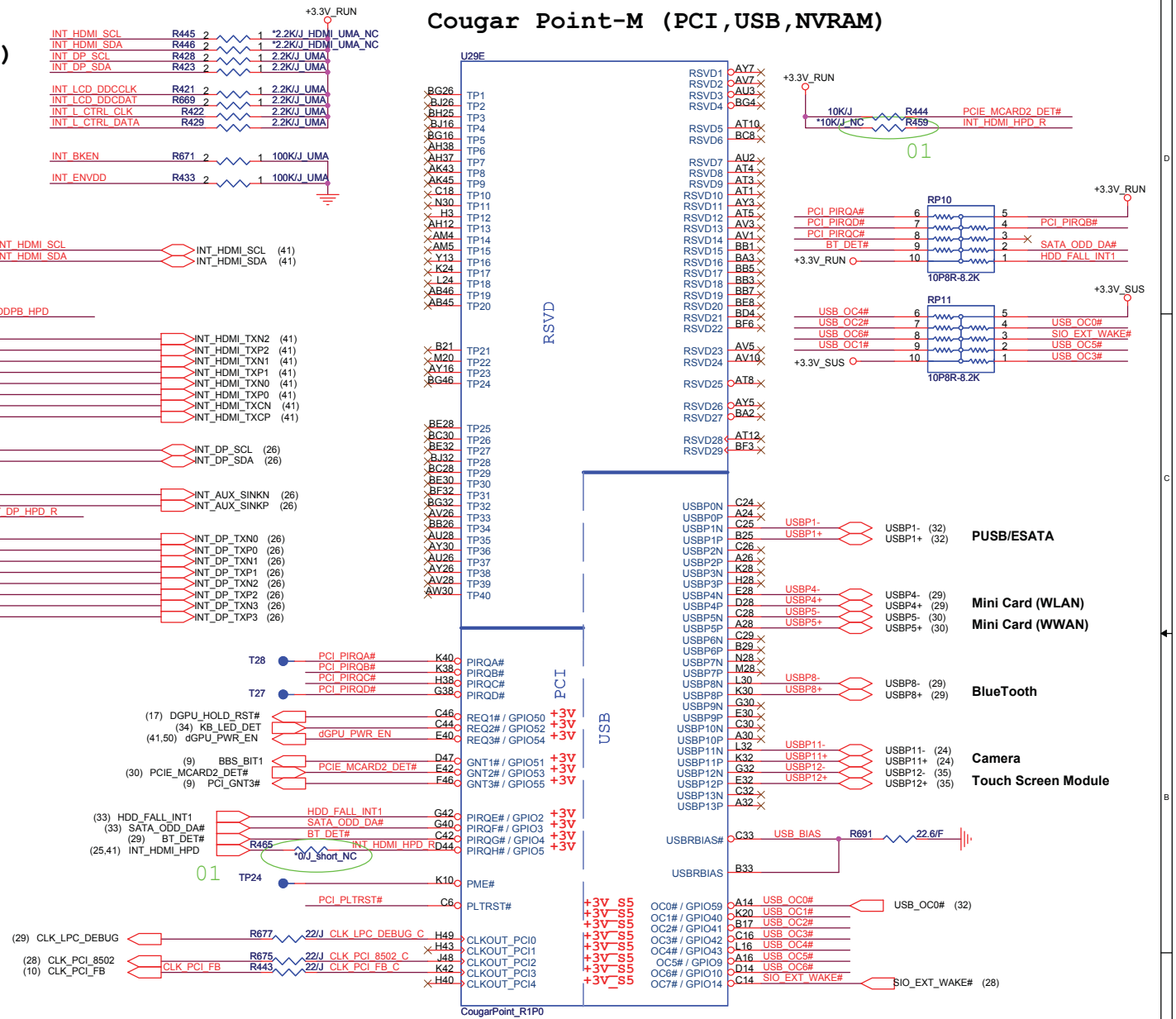
Size	Document Number	Rev
	Cougar Point 3/7	1A
Date: Friday, January 07, 2011	Sheet 10 of 59	

Cougar Point (LVDS,DDI)



LVD_IBG to other single 20 mils

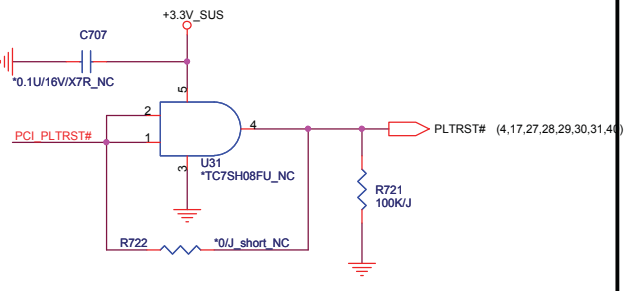
Cougar Point-M (PCI,USB,NVRAM)



TBC if there's OC issue 0629 (It's OK, DP has redriver IC)

Non-iAMT

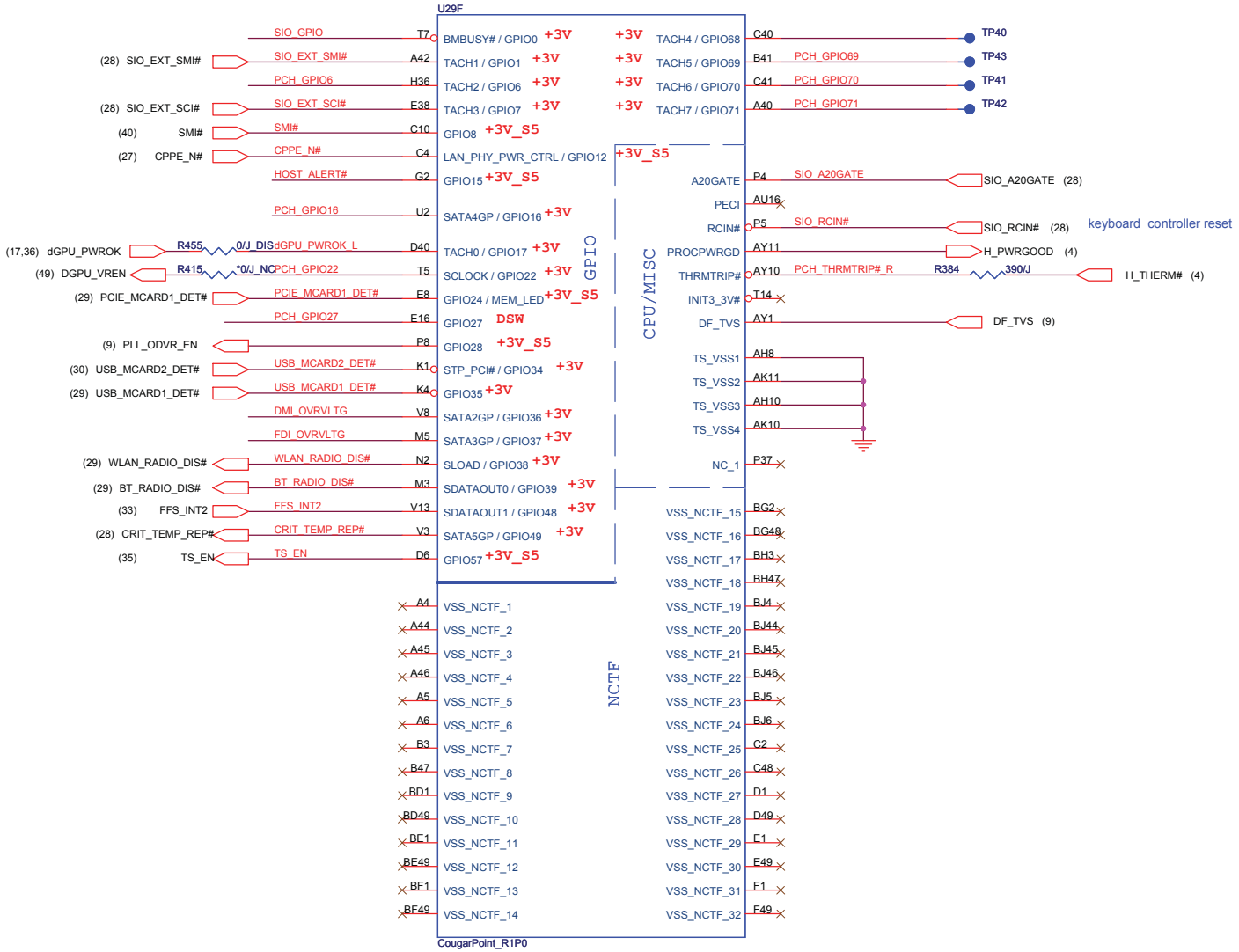
Add Buffers as needed for Loading and fanout concerns.

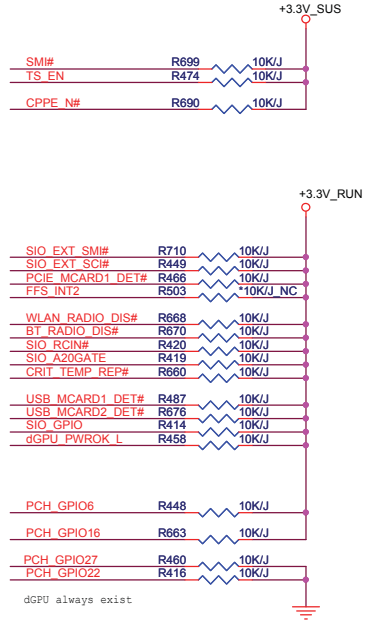


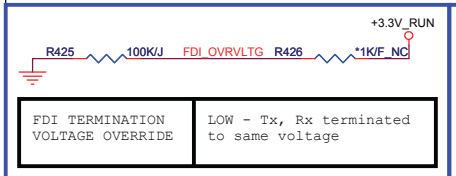
change to R01 schematic

Quanta Computer Inc.		
PROJECT : GM6C MLK DIS		
Size	Document Number: Cougar Point 4/7	Rev: 1A
Date: Friday, January 07, 2011	Sheet 11 of 59	

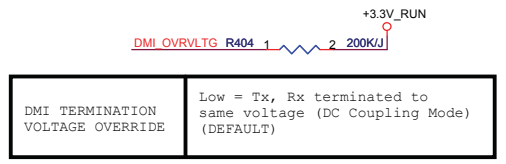
Cougar Point (GPIO,VSS_NCTF,RSVD)





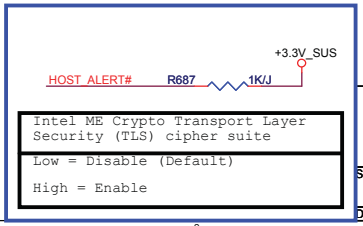


FDI TERMINATION VOLTAGE OVERRIDE	LOW - Tx, Rx terminated to same voltage



DMI TERMINATION VOLTAGE OVERRIDE	Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)

internal PD resistor 20K-ohm
To avoid voltage be divided,
please change GPIO36 PU resistor from
10K-ohm to 200K-ohm. (07/12)

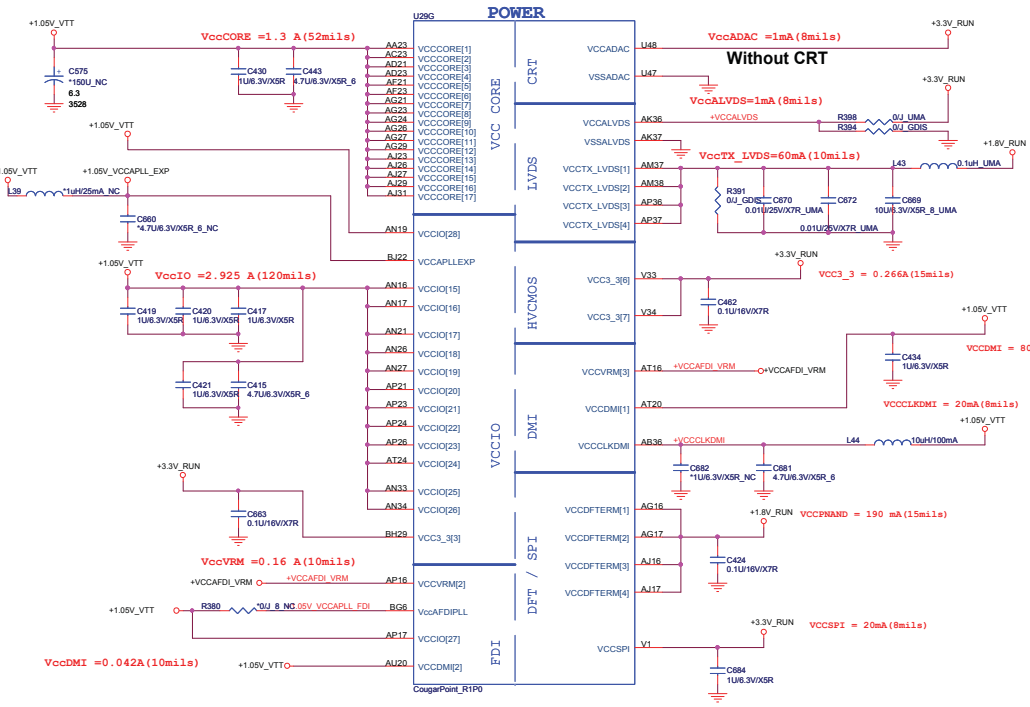


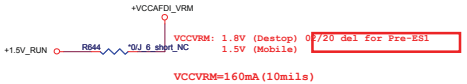
Intel ME Crypto Transport Layer Security (TLS) cipher suite	
Low = Disable (Default)	
High = Enable	

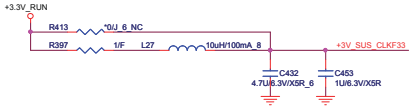
Quanta Computer Inc.
PROJECT : GM6C MLK DIS

Size	Document Number	Rev
	Cougar Point 5/7	1A
Date: Friday, January 07, 2011	Sheet 12 of 59	

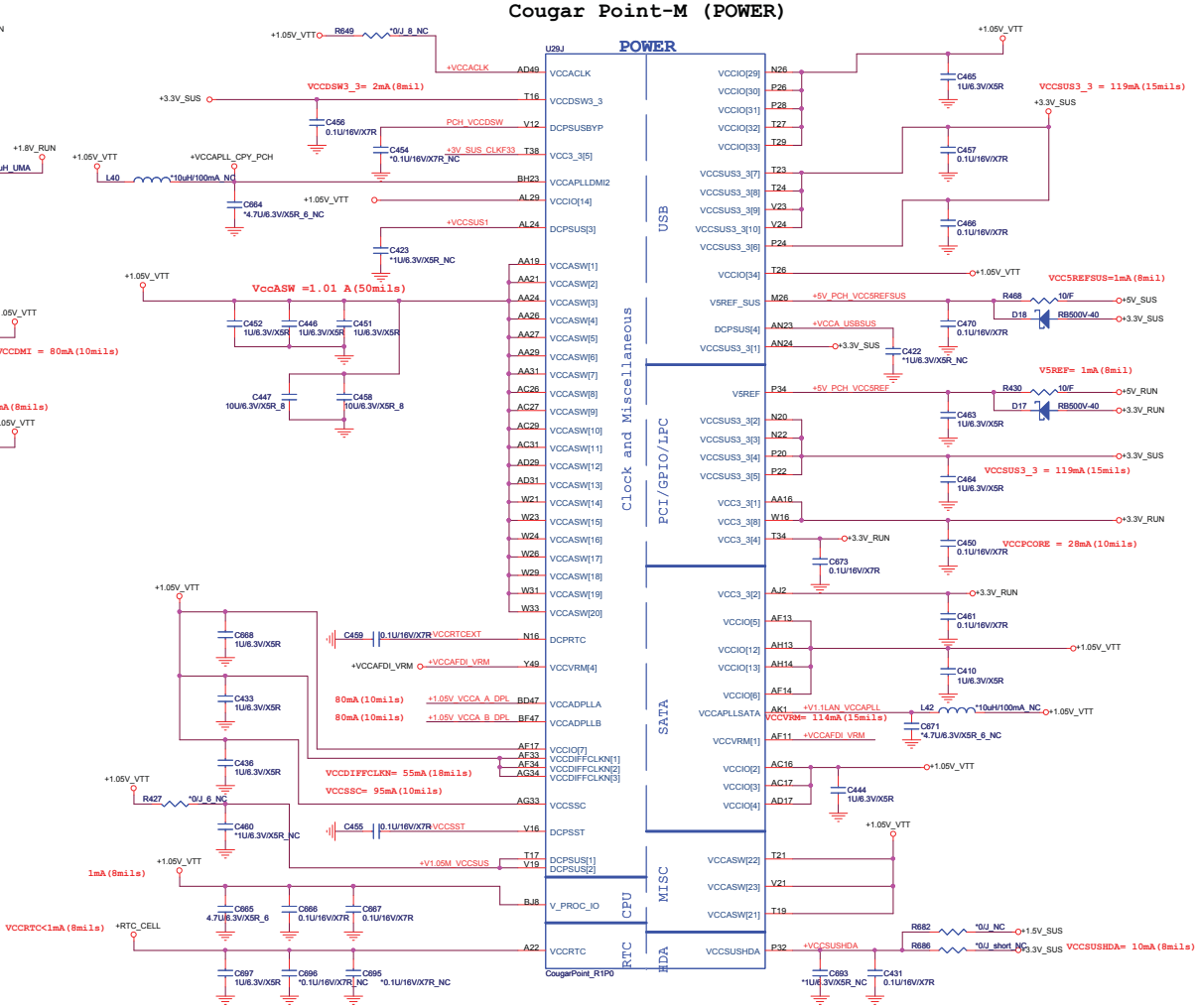
COUGAR POINT (POWER)

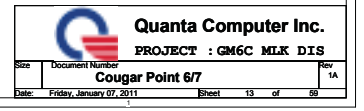






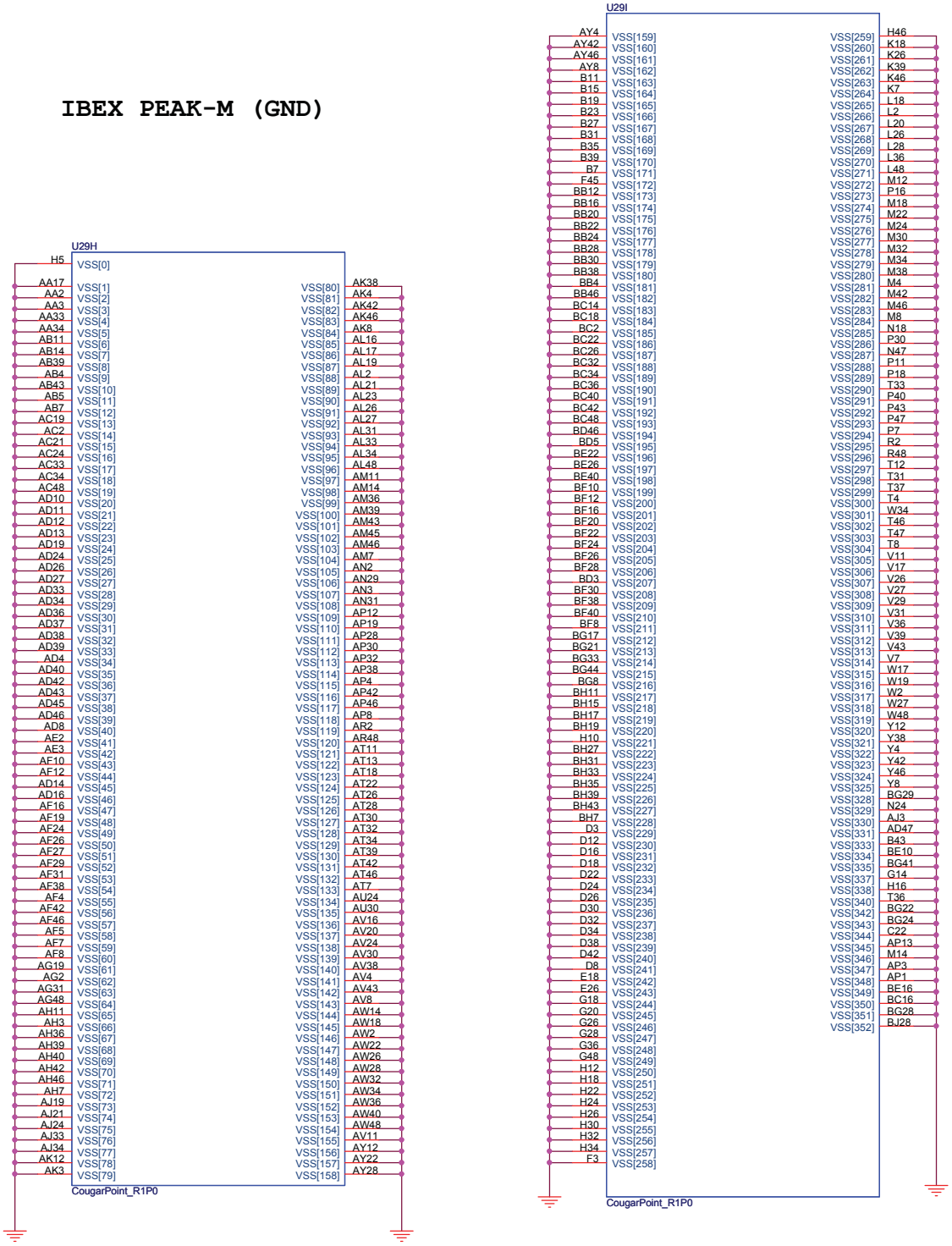
Cougar Point-M (POWER)





PCH6 (CLG)

IBEX PEAK-M (GND)



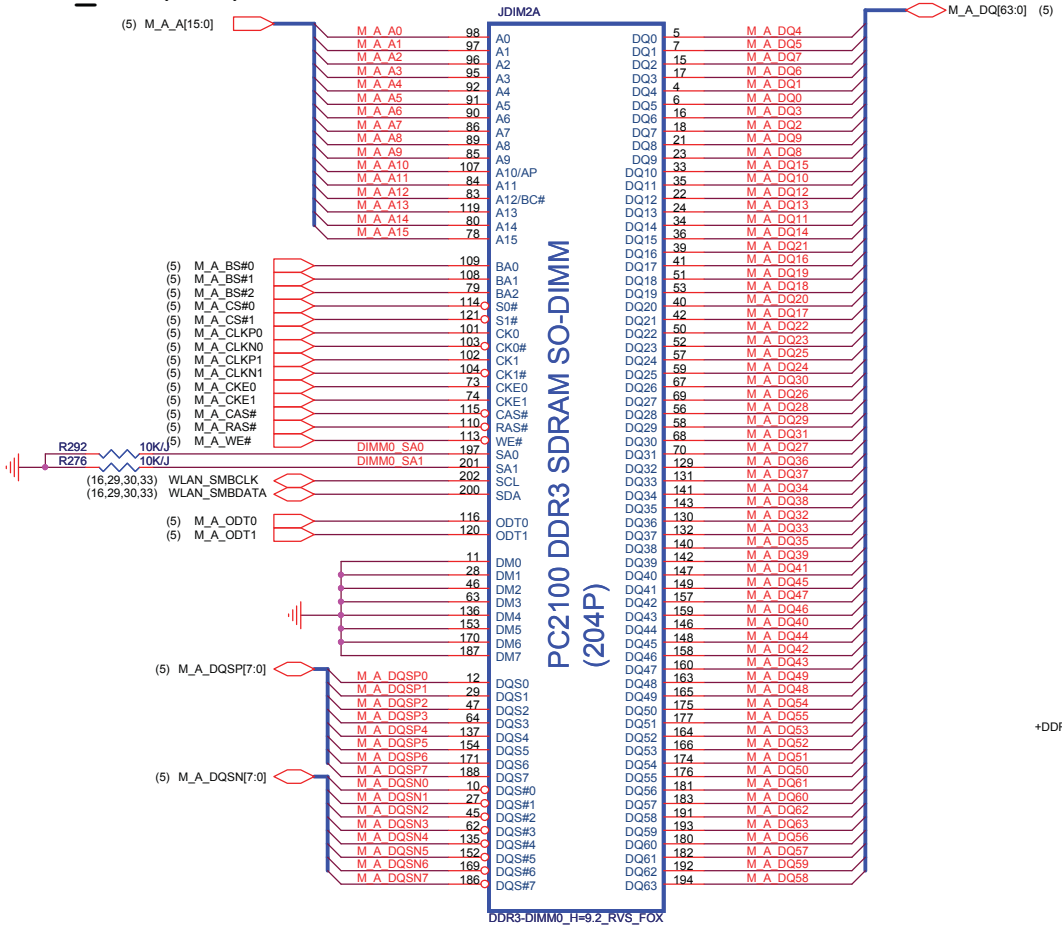
Quanta Computer Inc.

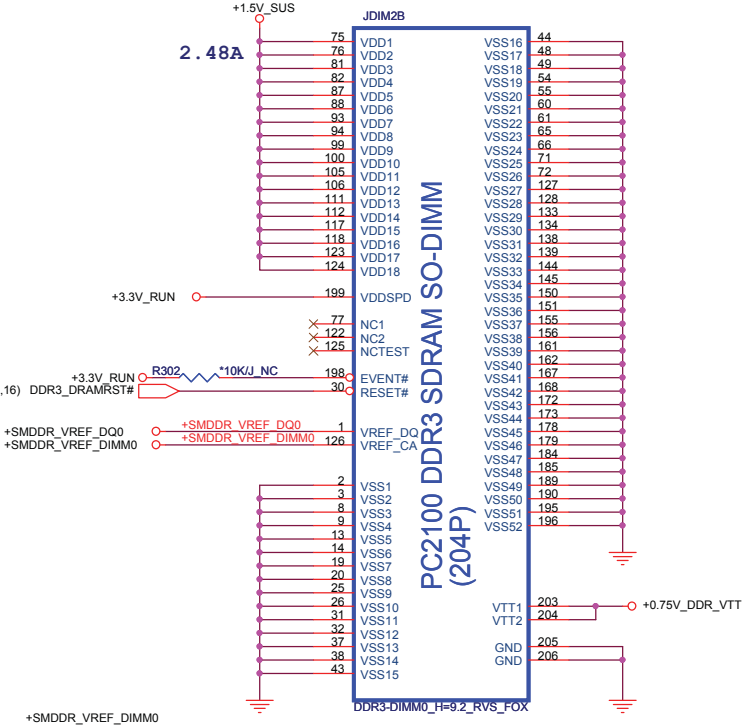
PROJECT : GM6C MLK DIS

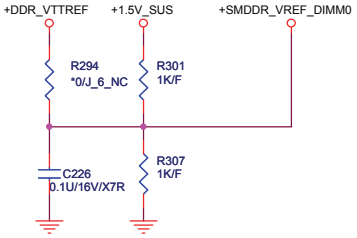
Size	Document Number	Rev
	Cougar Point 7/7	1A

Date: Friday, January 07, 2011 Sheet 14 of 59

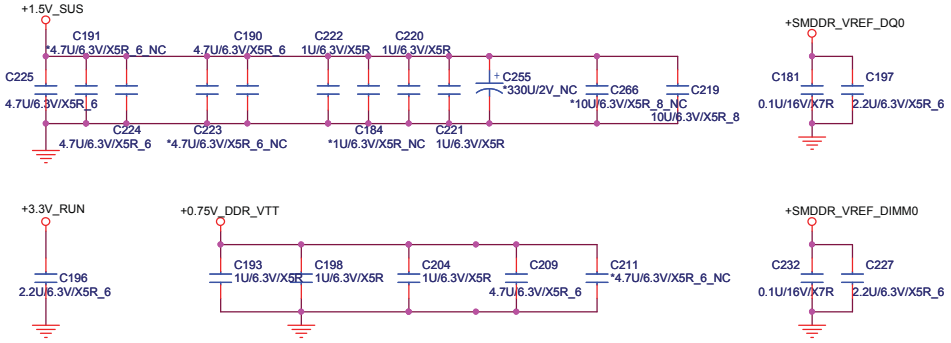
DDR_STD (DDR)



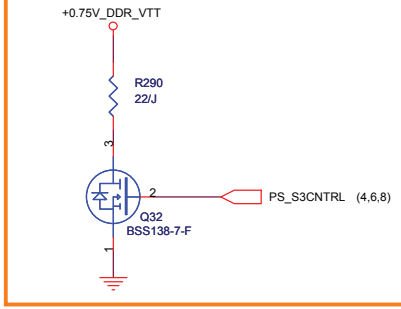




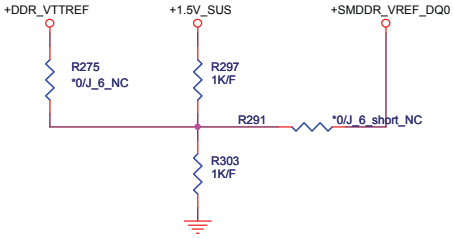
Place these Caps near So-Dimm0.



S3 Power reduce



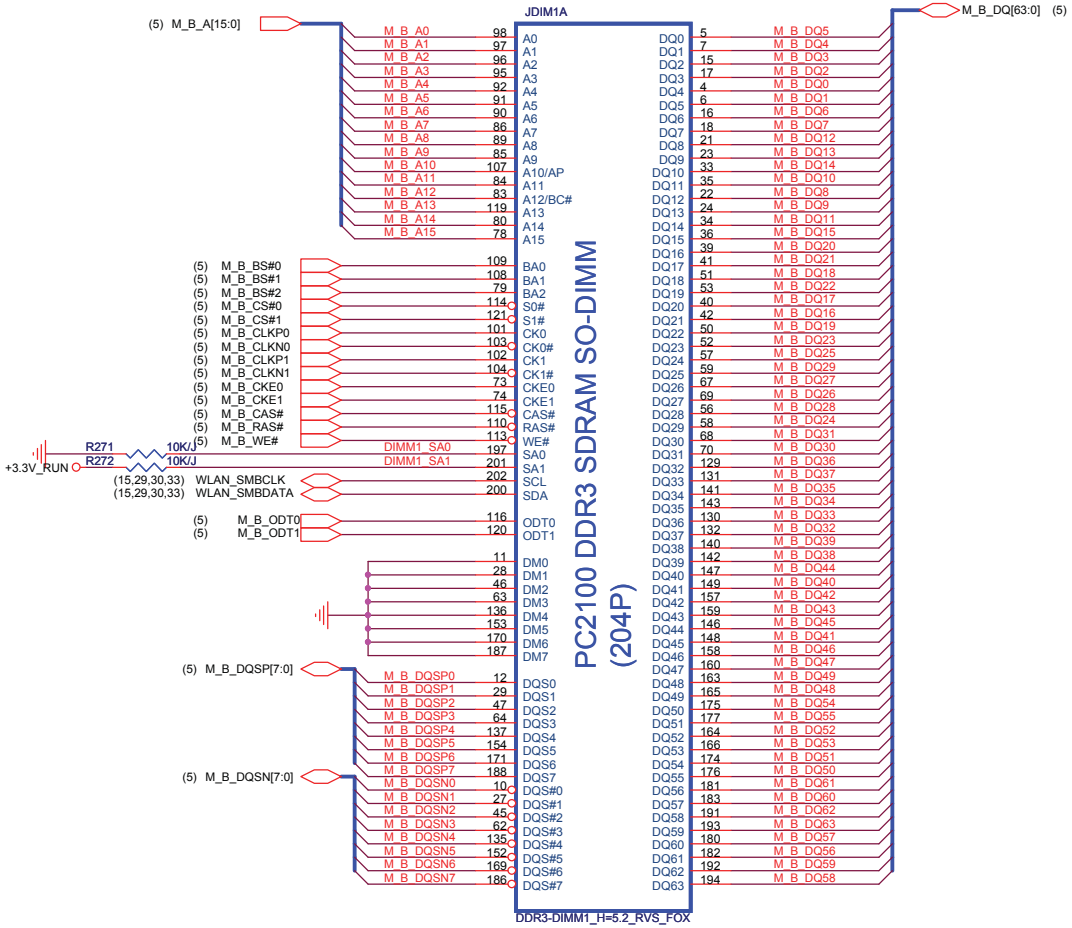
M1 VREF Solution

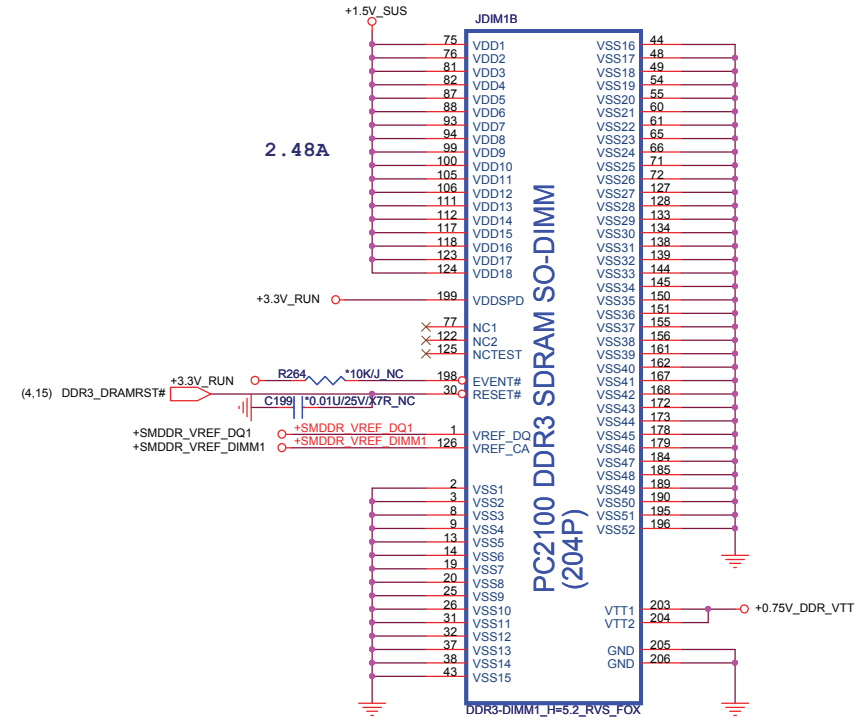


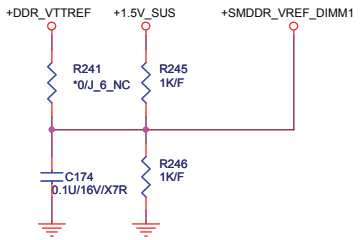
Quanta Computer Inc.

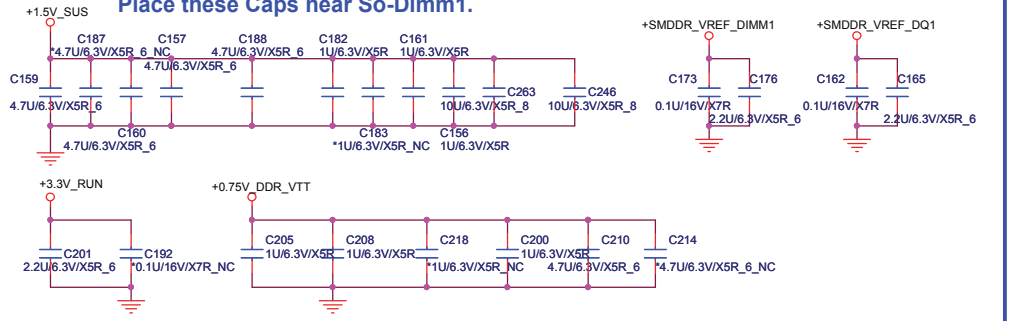
PROJECT : GM6C MLK DIS

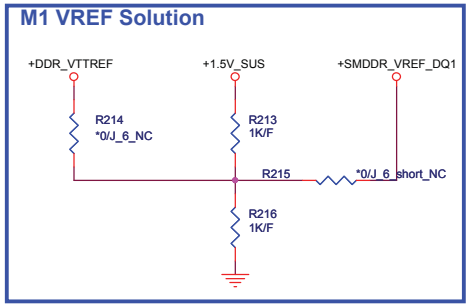
Size	Document Number	Rev
	DDRIII SO-DIMM-0	1A
Date: Friday, January 07, 2011	Sheet 15 of 59	









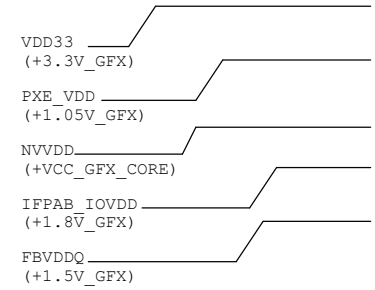


Quanta Computer Inc.

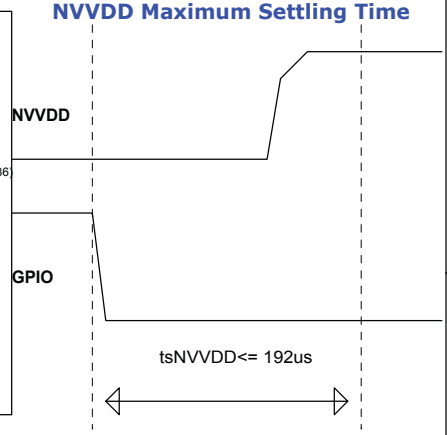
PROJECT : GM6C MLK DIS

Size	Document Number	Rev
	DDRIII SO-DIMM-1	1A
Date: Friday, January 07, 2011	Sheet 16 of 59	

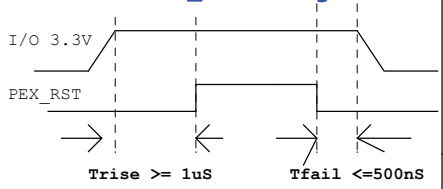
power up sequence

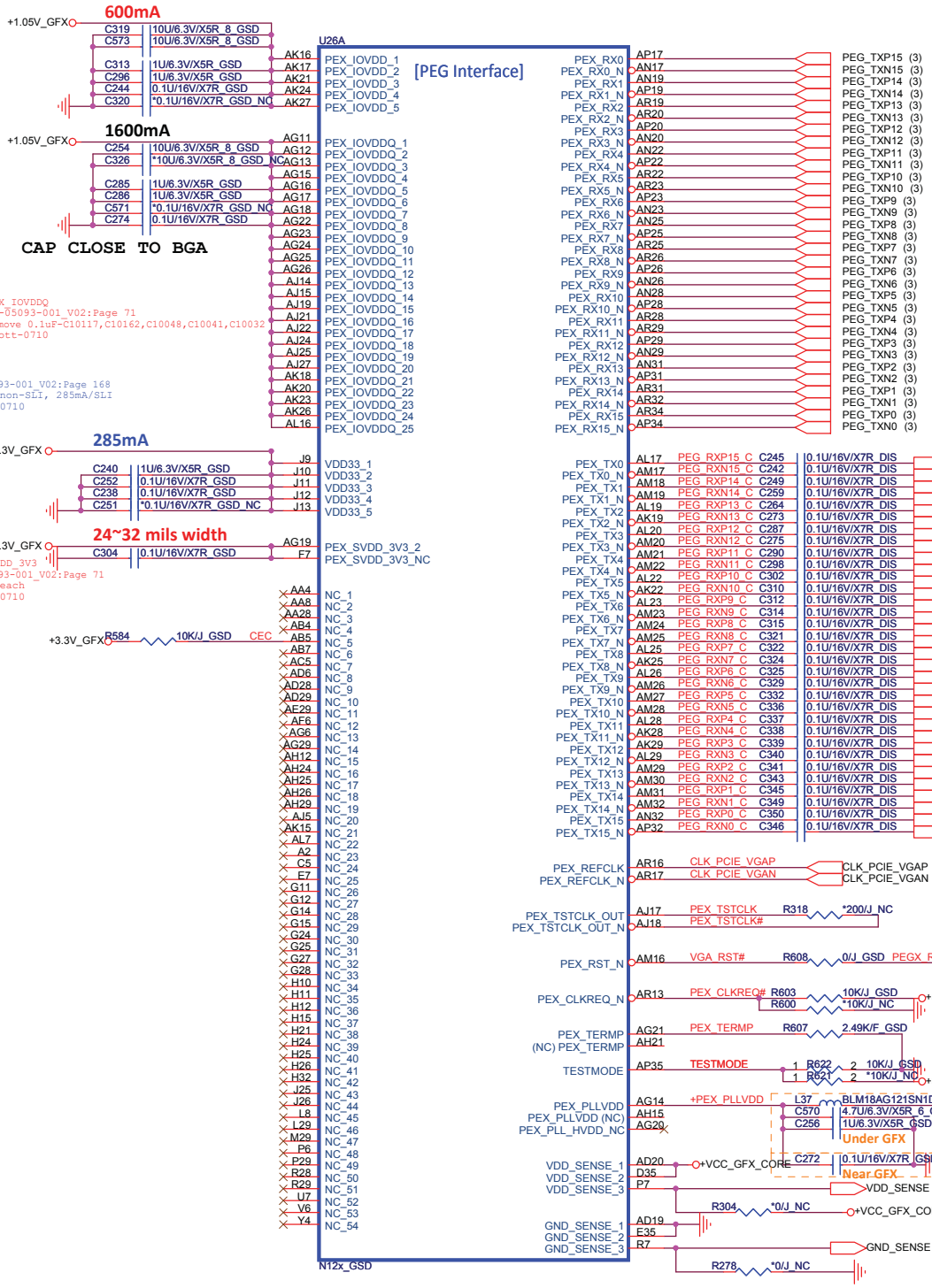


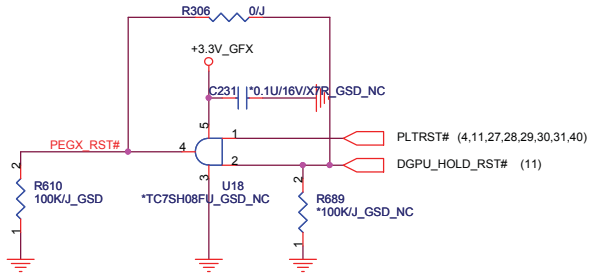
NVVDD Maximum Settling Time

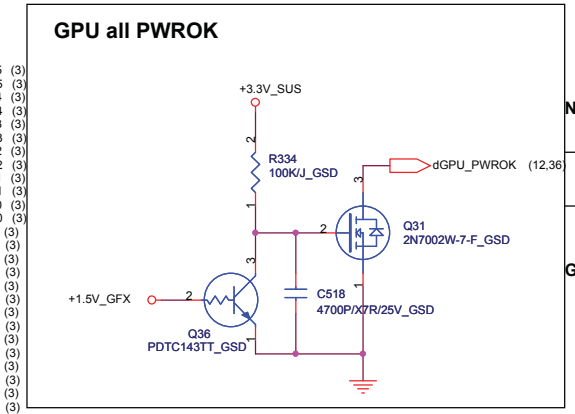


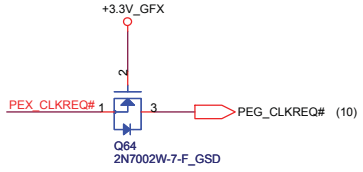
PEX_RST timing







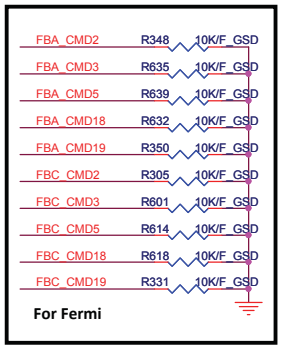




240mA
24~32 mils width

Quanta Computer Inc.	PROJECT : GM6C MLK DIS	
Size	Document Number: DGPU 1/5 (PEG)	Rev 1A
Date: Friday, January 07, 2011	Sheet 17 of 59	

Memory ODT,CKE,RST Termination
DG-05093-001_V02:Page 97
PRD-05272-002_v01:Page 3



VMA_DQ[63:0] → VMA_DQ[63:0] (22)
VMC_DQ[63:0] → VMC_DQ[63:0] (23)

(22) FBA_CMD[30:0]

U26B — [MEMORY I/F A]

FBA_CMD0	U30	FBA_CMD0 (FBA_CMD25)
FBA_CMD1	V30	FBA_CMD1 (FBA_CMD23)
FBA_CMD2	U31	FBA_CMD2
FBA_CMD3	V32	FBA_CMD3 (FBA_CMD0)
FBA_CMD4	T35	FBA_CMD4 (FBA_CMD10)
FBA_CMD5	U33	FBA_CMD5 (FBA_CMD26)
FBA_CMD6	W32	FBA_CMD6 (FBA_CMD14)
FBA_CMD7	W33	FBA_CMD7
FBA_CMD8	W31	FBA_CMD8 (FBA_CMD1)
FBA_CMD9	W34	FBA_CMD9 (FBA_CMD22)
FBA_CMD10	U34	FBA_CMD10 (FBA_CMD20)
FBA_CMD11	U35	FBA_CMD11 (FBA_CMD24)
FBA_CMD12	U32	FBA_CMD12 (FBA_CMD18)
FBA_CMD13	T34	FBA_CMD13 (FBA_CMD9)
FBA_CMD14	T33	FBA_CMD14 (FBA_CMD29)
FBA_CMD15	W30	FBA_CMD15 (FBA_CMD8)
FBA_CMD16	AB30	FBA_CMD16 (FBA_CMD27)
FBA_CMD17	AA30	FBA_CMD17 (FBA_CMD15)
FBA_CMD18	AB31	FBA_CMD18 (FBA_CMD11)
FBA_CMD19	AA32	FBA_CMD19 (FBA_CMD16)
FBA_CMD20	AB33	FBA_CMD20 (FBA_CMD28)
FBA_CMD21	Y32	FBA_CMD21 (FBA_CMD3)
FBA_CMD22	Y33	FBA_CMD22 (FBA_CMD17)
FBA_CMD23	AB34	FBA_CMD23 (FBA_CMD5)
FBA_CMD24	AB35	FBA_CMD24 (FBA_CMD4)
FBA_CMD25	Y35	FBA_CMD25 (FBA_CMD21)
FBA_CMD26	W35	FBA_CMD26 (FBA_CMD6)
FBA_CMD27	Y34	FBA_CMD27 (FBA_CMD13)
FBA_CMD28	Y31	FBA_CMD28 (FBA_CMD19)
FBA_CMD29	Y30	FBA_CMD29 (FBA_CMD12)
FBA_CMD30	W29	FBA_CMD30
	Y29	FBA_CMD31 (NC)

(22) VMA_DM[7:0]

VMA_DM0	P32	FBA_DQM0
VMA_DM1	H34	FBA_DQM1
VMA_DM2	J30	FBA_DQM2
VMA_DM3	P30	FBA_DQM3
VMA_DM4	AF32	FBA_DQM4
VMA_DM5	AL32	FBA_DQM5
VMA_DM6	AL34	FBA_DQM6
VMA_DM7	AF35	FBA_DQM7

(22) VMA_WDQS[7:0]

VMA_WDQS0	L34	FBA_DQS_WP0
VMA_WDQS1	H35	FBA_DQS_WP1
VMA_WDQS2	J32	FBA_DQS_WP2
VMA_WDQS3	N31	FBA_DQS_WP3
VMA_WDQS4	AE31	FBA_DQS_WP4
VMA_WDQS5	AJ32	FBA_DQS_WP5
VMA_WDQS6	AJ34	FBA_DQS_WP6
VMA_WDQS7	AC33	FBA_DQS_WP7

(22) VMA_RDQS[7:0]

VMA_RDQS0	L35	FBA_DQS_RN0
VMA_RDQS1	G35	FBA_DQS_RN1
VMA_RDQS2	H31	FBA_DQS_RN2
VMA_RDQS3	N32	FBA_DQS_RN3
VMA_RDQS4	AD32	FBA_DQS_RN4
VMA_RDQS5	AJ31	FBA_DQS_RN5
VMA_RDQS6	AJ35	FBA_DQS_RN6
VMA_RDQS7	AC34	FBA_DQS_RN7

+1.5V_GFX → FBVDDQ_1 AA27, FBVDDQ_2 AA29, FBVDDQ_3 AA31, FBVDDQ_4 AB27, FBVDDQ_5 AB29, FBVDDQ_6 AC27, FBVDDQ_7 AD27, FBVDDQ_8 AE27, FBVDDQ_9 AJ28, FBVDDQ_10 B18, FBVDDQ_11 E21, FBVDDQ_12 G17, FBVDDQ_13 G18, FBVDDQ_14 G22, FBVDDQ_15 G8, FBVDDQ_16 G9, FBVDDQ_17 H29, FBVDDQ_18 J14, FBVDDQ_19 J15

C388 4.7U/6.3V/X5R_6_GSD
C261 1U/6.3V/X5R_GSD
C262 1U/6.3V/X5R_GSD
C366 0.1U/16V/X7R_GSD
C300 0.1U/16V/X7R_GSD
C330 0.1U/16V/X7R_GSD
C213 0.1U/16V/X7R_GSD
C328 0.1U/16V/X7R_GSD
C344 0.1U/16V/X7R_GSD
C334 *0.1U/16V/X7R_GSD_NC
C333 0.1U/16V/X7R_GSD

FBVDDQ
DG-05093-001_V02:Page 98
DA-05206_V04:Page 21
Scott-0710

N12x_GSD

FBA_DQ0	L32	VMA_DQ0
FBA_DQ1	N33	VMA_DQ1
FBA_DQ2	L33	VMA_DQ2
FBA_DQ3	N34	VMA_DQ3
FBA_DQ4	N35	VMA_DQ4
FBA_DQ5	P35	VMA_DQ5
FBA_DQ6	P33	VMA_DQ6
FBA_DQ7	P34	VMA_DQ7
FBA_DQ8	K35	VMA_DQ8
FBA_DQ9	K33	VMA_DQ9
FBA_DQ10	K34	VMA_DQ10
FBA_DQ11	H33	VMA_DQ11
FBA_DQ12	G34	VMA_DQ12
FBA_DQ13	G33	VMA_DQ13
FBA_DQ14	E34	VMA_DQ14
FBA_DQ15	E33	VMA_DQ15
FBA_DQ16	G31	VMA_DQ16
FBA_DQ17	F30	VMA_DQ17
FBA_DQ18	G30	VMA_DQ18
FBA_DQ19	G32	VMA_DQ19
FBA_DQ20	K30	VMA_DQ20
FBA_DQ21	K32	VMA_DQ21
FBA_DQ22	H30	VMA_DQ22
FBA_DQ23	K31	VMA_DQ23
FBA_DQ24	L31	VMA_DQ24
FBA_DQ25	L30	VMA_DQ25
FBA_DQ26	M32	VMA_DQ26
FBA_DQ27	N30	VMA_DQ27
FBA_DQ28	M30	VMA_DQ28
FBA_DQ29	P31	VMA_DQ29
FBA_DQ30	R32	VMA_DQ30
FBA_DQ31	R30	VMA_DQ31
FBA_DQ32	AG30	VMA_DQ32
FBA_DQ33	AG32	VMA_DQ33
FBA_DQ34	AH31	VMA_DQ34
FBA_DQ35	AF31	VMA_DQ35
FBA_DQ36	AF30	VMA_DQ36
FBA_DQ37	AE30	VMA_DQ37
FBA_DQ38	AC32	VMA_DQ38
FBA_DQ39	AD30	VMA_DQ39
FBA_DQ40	AN33	VMA_DQ40
FBA_DQ41	AL31	VMA_DQ41
FBA_DQ42	AM33	VMA_DQ42
FBA_DQ43	AL33	VMA_DQ43
FBA_DQ44	AK30	VMA_DQ44
FBA_DQ45	AK32	VMA_DQ45
FBA_DQ46	AJ30	VMA_DQ46
FBA_DQ47	AH30	VMA_DQ47
FBA_DQ48	AH33	VMA_DQ48
FBA_DQ49	AH35	VMA_DQ49
FBA_DQ50	AH34	VMA_DQ50
FBA_DQ51	AH32	VMA_DQ51
FBA_DQ52	AJ33	VMA_DQ52
FBA_DQ53	AL35	VMA_DQ53
FBA_DQ54	AM34	VMA_DQ54
FBA_DQ55	AM35	VMA_DQ55
FBA_DQ56	AF33	VMA_DQ56
FBA_DQ57	AE32	VMA_DQ57
FBA_DQ58	AF34	VMA_DQ58
FBA_DQ59	AE35	VMA_DQ59
FBA_DQ60	AE34	VMA_DQ60
FBA_DQ61	AE33	VMA_DQ61
FBA_DQ62	AB32	VMA_DQ62
FBA_DQ63	AC35	VMA_DQ63

FBA_CLK0 T32 VMA_CLK0 → VMA_CLK0 (22)
FBA_CLK0_N T31 VMA_CLK0# → VMA_CLK0# (22)
FBA_CLK1 AC31 VMA_CLK1 → VMA_CLK1 (22)
FBA_CLK1_N AC30 VMA_CLK1# → VMA_CLK1# (22)
15mils width

(FBA_DEBUG) FBA_DEBUG0 T30 FBA_DEBUG R327 *60.4/F_NC +1.5V_GFX
(NC) FBA_DEBUG1 T29
FB_VREF_NC J27 +FB_VREF1 TP16
15mils width

FB_DLLAVDD1 AG27 +FB_DLLAVDD
(NC) FB_DLLAVDD2 AF28
(NC) FB_DLLAVDD3 J19 R321 0/J_GSD
12mils width

FB_PLLAVDD1 AF27
(NC) FB_PLLAVDD2 AE28
(NC) FB_PLLAVDD3 J18 R315 0/J_GSD
12mils width

L26 BLM18PG300SN1_GSD +1.05V_GFX
C362 2_4.7U/6.3V/X5R_6_GSD
C331 1U/6.3V/X5R_GSD
C357 0.1U/16V/X7R_GSD
C356 0.1U/16V/X7R_GSD
Near GPU
Under GPU

FB_DLLAVDD/FB_PLLAVDD
DG-05093-001_V02:Page 100
DA-05206-001_V04: Page 22

FBA_DEBUG
PRD-05272-002_v01:Page 3

(23) FBC_CMD[30:0]

U26C — MEMORY I/F C

FBC_CMD0	F18	FBB_CMD0 (FBC_CMD25)
FBC_CMD1	E19	FBB_CMD1 (FBC_CMD23)
FBC_CMD2	D18	FBC_CMD2
FBC_CMD3	C17	FBB_CMD3 (FBC_CMD0)
FBC_CMD4	F19	FBB_CMD4 (FBC_CMD10)
FBC_CMD5	C19	FBB_CMD5 (FBC_CMD26)
FBC_CMD6	B17	FBB_CMD6 (FBC_CMD14)
FBC_CMD7	E20	FBC_CMD7
FBC_CMD8	B19	FBB_CMD8 (FBC_CMD1)
FBC_CMD9	D20	FBB_CMD9 (FBC_CMD22)
FBC_CMD10	A19	FBB_CMD10 (FBC_CMD20)
FBC_CMD11	D19	FBB_CMD11 (FBC_CMD24)
FBC_CMD12	C20	FBB_CMD12 (FBC_CMD18)
FBC_CMD13	F20	FBB_CMD13 (FBC_CMD9)
FBC_CMD14	B20	FBB_CMD14 (FBC_CMD29)
FBC_CMD15	G21	FBB_CMD15 (FBC_CMD8)
FBC_CMD16	F22	FBB_CMD16 (FBC_CMD27)
FBC_CMD17	F24	FBB_CMD17 (FBC_CMD15)
FBC_CMD18	F23	FBB_CMD18 (FBC_CMD11)
FBC_CMD19	C25	FBB_CMD19 (FBC_CMD16)
FBC_CMD20	C23	FBB_CMD20 (FBC_CMD28)
FBC_CMD21	F21	FBB_CMD21 (FBC_CMD3)
FBC_CMD22	F22	FBB_CMD22 (FBC_CMD17)
FBC_CMD23	D21	FBB_CMD23 (FBC_CMD5)
FBC_CMD24	A23	FBB_CMD24(FBC_CMD4)
FBC_CMD25	D22	FBB_CMD25 (FBC_CMD21)
FBC_CMD26	B23	FBB_CMD26 (FBC_CMD6)
FBC_CMD27	C22	FBB_CMD27 (FBC_CMD13)
FBC_CMD28	B22	FBB_CMD28 (FBC_CMD19)
FBC_CMD29	A22	FBB_CMD29 (FBC_CMD12)
FBC_CMD30	A20	FBC_CMD30
	G20	FBC_CMD31 (NC)

(23) VMC_DM[7:0]

VMC_DM0	A16	FBC_DQM0
VMC_DM1	D10	FBC_DQM1
VMC_DM2	F11	FBC_DQM2
VMC_DM3	D15	FBC_DQM3
VMC_DM4	D27	FBC_DQM4
VMC_DM5	D34	FBC_DQM5
VMC_DM6	A34	FBC_DQM6
VMC_DM7	D28	FBC_DQM7

(23) VMC_WDQS[7:0]

VMC_WDQS0	C14	FBC_DQS_WP0
VMC_WDQS1	A10	FBC_DQS_WP1
VMC_WDQS2	E10	FBC_DQS_WP2
VMC_WDQS3	D14	FBC_DQS_WP3
VMC_WDQS4	E26	FBC_DQS_WP4
VMC_WDQS5	D32	FBC_DQS_WP5
VMC_WDQS6	A32	FBC_DQS_WP6
VMC_WDQS7	B26	FBC_DQS_WP7

(23) VMC_RDQS[7:0]

VMC_RDQS0	B14	FBC_DQS_RN0
VMC_RDQS1	B10	FBC_DQS_RN1
VMC_RDQS2	D9	FBC_DQS_RN2
VMC_RDQS3	E14	FBC_DQS_RN3
VMC_RDQS4	F26	FBC_DQS_RN4
VMC_RDQS5	D31	FBC_DQS_RN5
VMC_RDQS6	A31	FBC_DQS_RN6
VMC_RDQS7	A26	FBC_DQS_RN7

+1.5V_GFX → FBVDDQ_20 J16, FBVDDQ_21 J17, FBVDDQ_22 J20, FBVDDQ_23 J21, FBVDDQ_24 J22, FBVDDQ_25 J23, FBVDDQ_26 J24, FBVDDQ_27 J29, FBVDDQ_28 N27, FBVDDQ_29 P27, FBVDDQ_30 R27, FBVDDQ_31 T27, FBVDDQ_32 U27, FBVDDQ_33 U29, FBVDDQ_34 V27, FBVDDQ_35 V29, FBVDDQ_36 V34, FBVDDQ_37 W27, FBVDDQ_38 Y27

N12x_GSD

FBC_DQ0	B13	VMC_DQ0
FBC_DQ1	D13	VMC_DQ1
FBC_DQ2	A13	VMC_DQ2
FBC_DQ3	A14	VMC_DQ3
FBC_DQ4	C16	VMC_DQ4
FBC_DQ5	B16	VMC_DQ5
FBC_DQ6	A17	VMC_DQ6
FBC_DQ7	D16	VMC_DQ7
FBC_DQ8	C13	VMC_DQ8
FBC_DQ9	B11	VMC_DQ9
FBC_DQ10	C11	VMC_DQ10
FBC_DQ11	A11	VMC_DQ11
FBC_DQ12	C10	VMC_DQ12
FBC_DQ13	C8	VMC_DQ13
FBC_DQ14	B8	VMC_DQ14
FBC_DQ15	A8	VMC_DQ15
FBC_DQ16	E8	VMC_DQ16
FBC_DQ17	F8	VMC_DQ17
FBC_DQ18	F10	VMC_DQ18
FBC_DQ19	F9	VMC_DQ19
FBC_DQ20	F12	VMC_DQ20
FBC_DQ21	D8	VMC_DQ21
FBC_DQ22	D11	VMC_DQ22
FBC_DQ23	E11	VMC_DQ23
FBC_DQ24	D12	VMC_DQ24
FBC_DQ25	E13	VMC_DQ25
FBC_DQ26	F13	VMC_DQ26
FBC_DQ27	F14	VMC_DQ27
FBC_DQ28	F15	VMC_DQ28
FBC_DQ29	E16	VMC_DQ29
FBC_DQ30	F16	VMC_DQ30
FBC_DQ31	F17	VMC_DQ31
FBC_DQ32	D29	VMC_DQ32
FBC_DQ33	F27	VMC_DQ33
FBC_DQ34	F28	VMC_DQ34
FBC_DQ35	E28	VMC_DQ35
FBC_DQ36	D26	VMC_DQ36
FBC_DQ37	F25	VMC_DQ37
FBC_DQ38	D24	VMC_DQ38
FBC_DQ39	E25	VMC_DQ39
FBC_DQ40	E32	VMC_DQ40
FBC_DQ41	F32	VMC_DQ41
FBC_DQ42	D33	VMC_DQ42
FBC_DQ43	E31	VMC_DQ43
FBC_DQ44	C33	VMC_DQ44
FBC_DQ45	F29	VMC_DQ45
FBC_DQ46	D30	VMC_DQ46
FBC_DQ47	E29	VMC_DQ47
FBC_DQ48	B29	VMC_DQ48
FBC_DQ49	C31	VMC_DQ49
FBC_DQ50	C29	VMC_DQ50
FBC_DQ51	B31	VMC_DQ51
FBC_DQ52	C32	VMC_DQ52
FBC_DQ53	B32	VMC_DQ53
FBC_DQ54	B35	VMC_DQ54
FBC_DQ55	B34	VMC_DQ55
FBC_DQ56	A29	VMC_DQ56
FBC_DQ57	B28	VMC_DQ57
FBC_DQ58	A28	VMC_DQ58
FBC_DQ59	C28	VMC_DQ59
FBC_DQ60	C26	VMC_DQ60
FBC_DQ61	D25	VMC_DQ61
FBC_DQ62	B25	VMC_DQ62
FBC_DQ63	A25	VMC_DQ63

FBC_CLK0 E17 VMC_CLK0 → VMC_CLK0 (23)
FBC_CLK0_N D17 VMC_CLK0# → VMC_CLK0# (23)
FBC_CLK1 D23 VMC_CLK1 → VMC_CLK1 (23)
FBC_CLK1_N E23 VMC_CLK1# → VMC_CLK1# (23)

FBA_DEBUG
PRD-05272-002_v01:Page 3

(FBC_DEBUG) FBB_DEBUG0 G19 FBC_DEBUG R314 *60.4/F_NC +1.5V_GFX
(NC) FBB_DEBUG1 G16

FB_CAL_PD_VDDQ K27 FB_CAL_PD_VDDQ R326 40.2/F_GSD +1.5V_GFX
(NC) FB_CAL_PD_VDDQ K28
FB_CAL_PU_GND L27 FB_CAL_PU_GND R323 40.2/F_GSD
(NC) FB_CAL_PU_GND L28

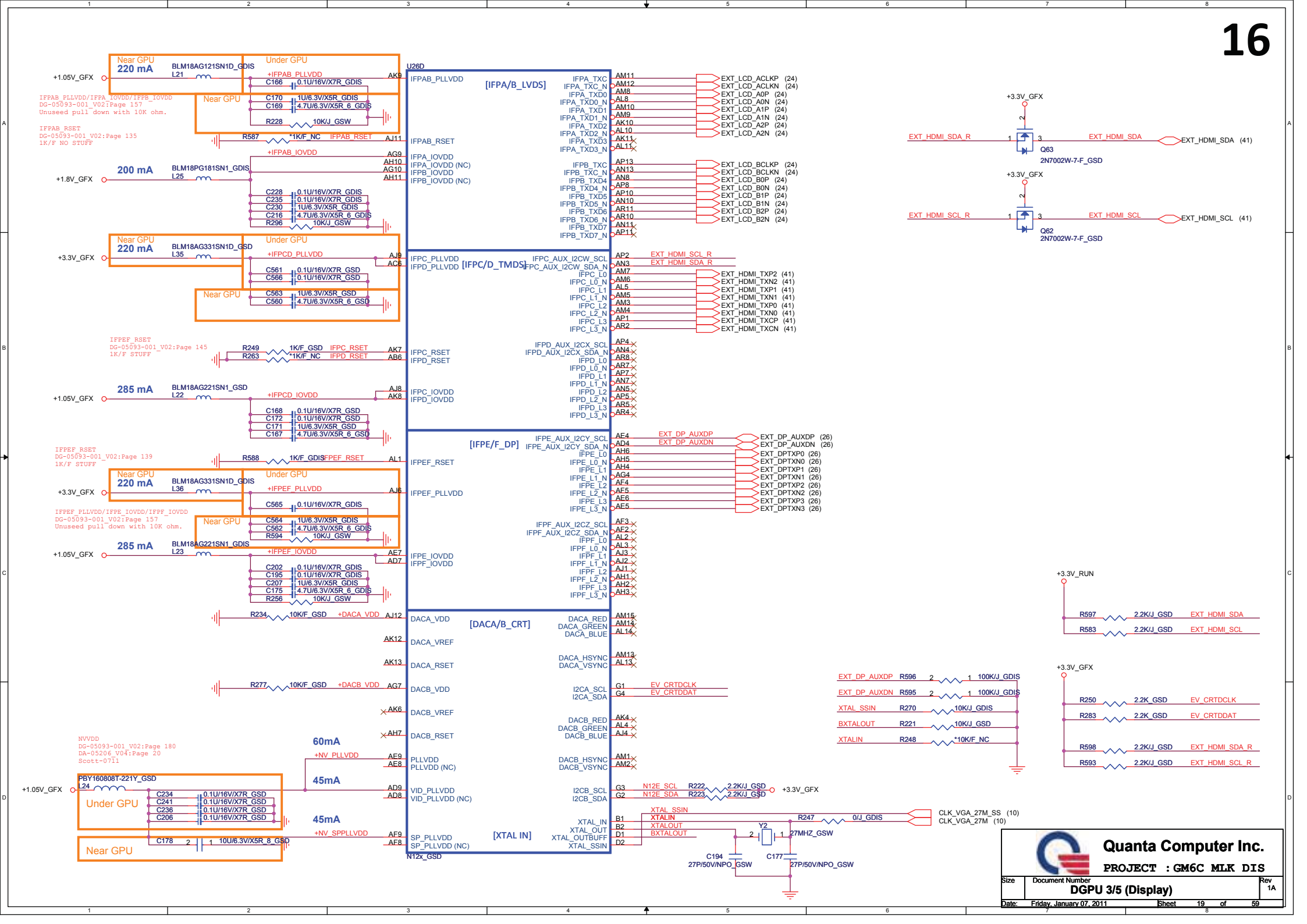
FB_CAL_TERM_GND M27 FB_CAL_TERM_GND R324 60.4/F_GSD
(NC) FB_CAL_TERM_GND M28

FB_CAL_PD_VDDQ/FB_CAL_PU_GND
DG-05093-001_V02:Page 94
FB_CAL_TERM_GND
DG-05093-001_V02:Page 94
40.2/F or 60.4/F dependent on GPU SKU

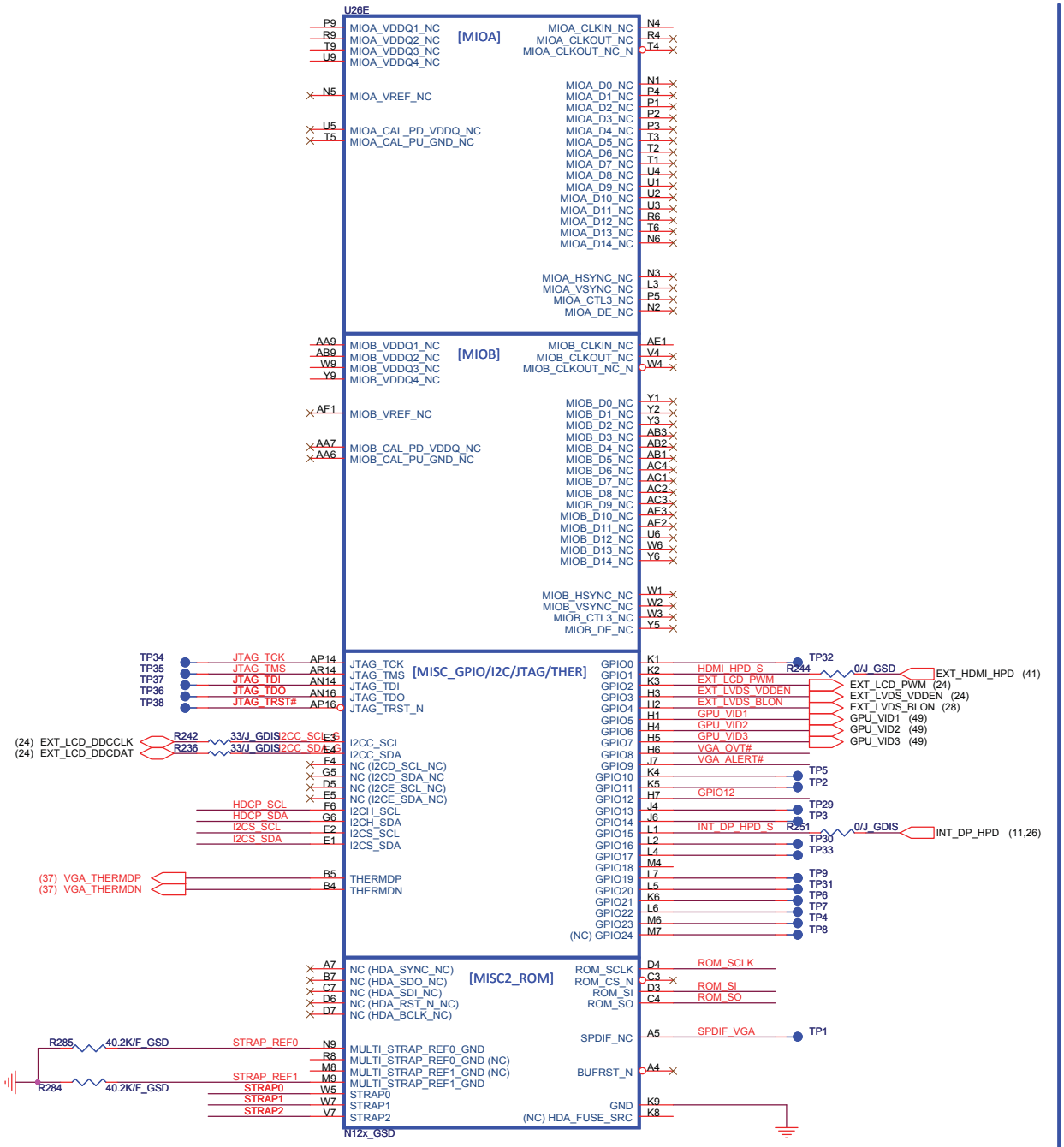
(17,19,50) +1.05V_GFX
(17,22,23,50) +1.5V_GFX

Quanta Computer Inc.
PROJECT : GM6C MLK DIS

Size	Document Number	Rev
	DGPU 2/5 (Memory)	1A
Date: Friday, January 07, 2011	Sheet 18 of 59	



Quanta Computer Inc.			
PROJECT : GM6C MLK DIS			
Size	Document Number		Rev
	DGPU 3/5 (Display)		1A
Date: Friday, January 07, 2011	Sheet 19 of 59		



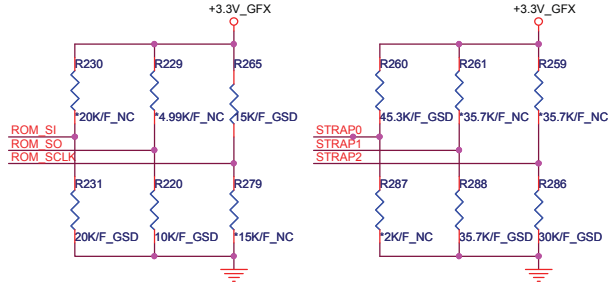
	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO NB10X	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE	0001
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM	X010
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	XXXX
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	1110
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111

VRAM Configuration Table

RAMCFG [3:0]	DESCRIPTION	Quanta PN(Q buy)	Quanta PN(W buy)	Vendor PN
0x3(0011)	900MHz 512MB(64M*16) Samsung	AKD5LGHT500		K4W1G1646E-HC11
0x2(0010)	900MHz 512MB(64M*16) Hynix	AKD5LZWTW02		H5TQ1G63DFR-11C
0x6(0110)	900MHz 1GB(128M*16) Hynix	AKD5MGWTW00		H5TQ2G63BFR-11C
0x7(0111)	900MHz 1GB(128M*16) Samsung	AKD5MGWT500		K4W2G1646C-HC11

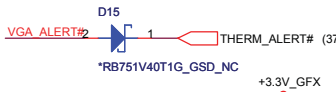
ROM_SI Strap Bit for RAM Mapping

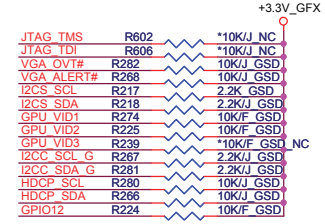
	PU	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

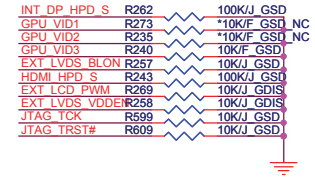


STRAP2 ROM_SCLK

N12P-GE (AJ0N12P0T02)	PD 30K	PU 15K	0xDF5	
N12P-GT (AJ0N12P0T03)	PD 35K	PU 15K	0xDF6	
N12P-GS (AJ0N12P0T04)	PD 25K	PU 15K	0xDF4	







GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	N/A	N/A	
1	IN	N/A	Hot plug detect for IFP link C
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVVDD VID0
6	OUT	N/A	NVVDD VID1
7	OUT	N/A	NVVDD VID2
8	I/O	LOW	OVERT
9	I/O	LOW	ALERT
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI Raster Sync
12	IN	N/A	AC PWR Detect Input
13	OUT	N/A	Power Supply Control
14	OUT	N/A	Power Supply Control
15	OUT	N/A	Hot plug detect for IFP link E
16	OUT	N/A	Programmable Fan Control
17	OUT	N/A	Reserved
19	OUT	N/A	Reserved
20	OUT	N/A	Hot plug detect for IFP link D
21	OUT	N/A	Reserved
22	OUT	N/A	Hot plug detect for IFP link F
23	OUT	N/A	SLI Swap Ready single
23	OUT	N/A	

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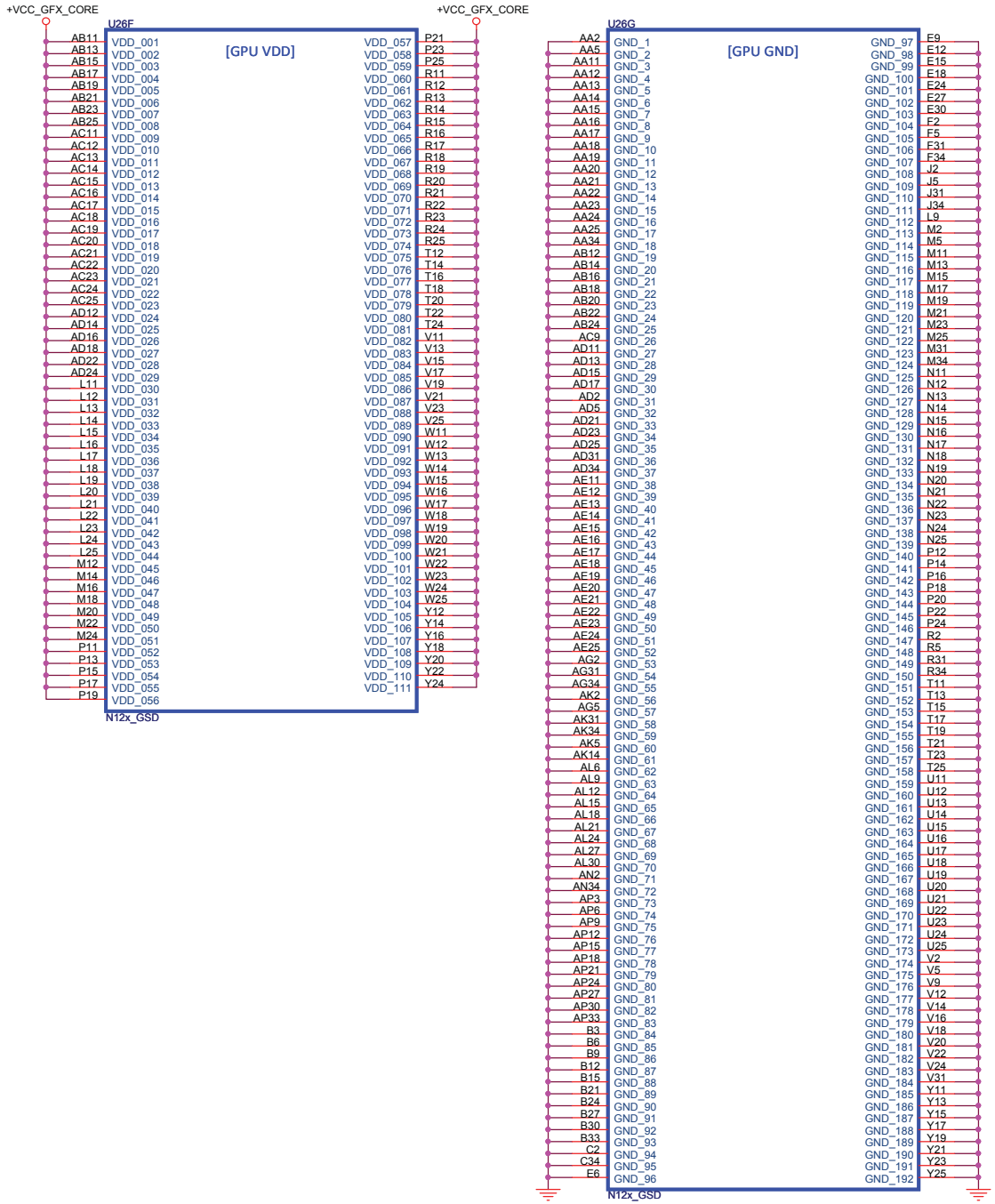
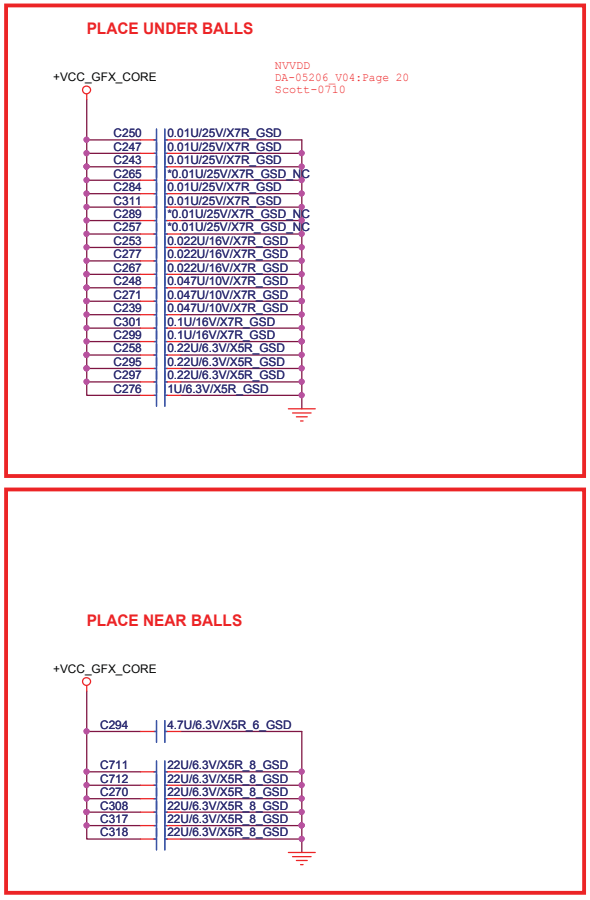
PROJECT : GM6C MLK DIS

Size	Document Number	Rev
	DGPU 4/5 (MIO/GPIO)	1A

Date: Friday, January 07, 2011 Sheet 20 of 59

31.56A





Quanta Computer Inc.

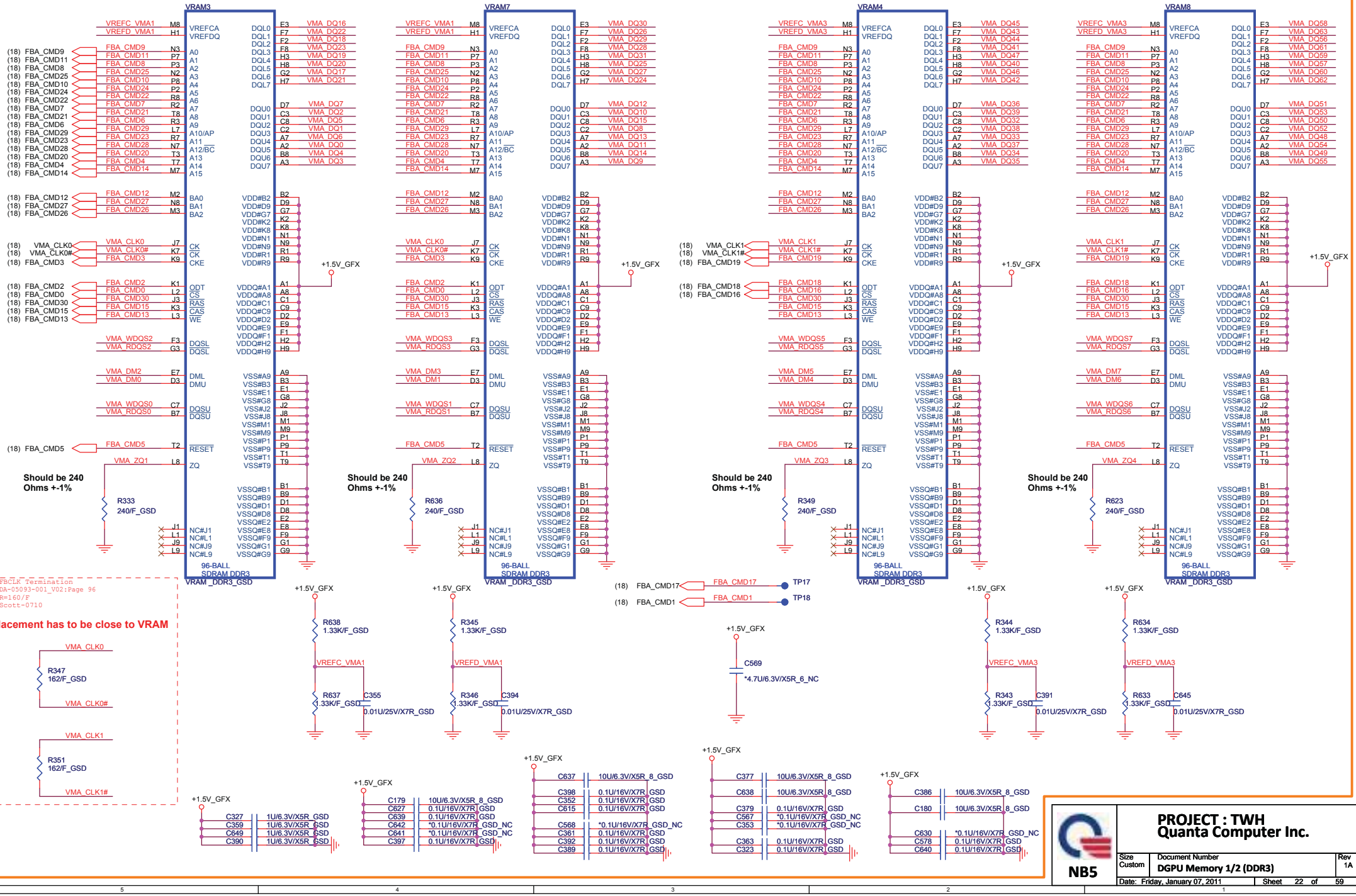
PROJECT : GM6C MLK DIS

Size	Document Number	Rev
	DGPU 5/5 (Power/Ground)	1A

Date: Friday, January 07, 2011 Sheet 21 of 59

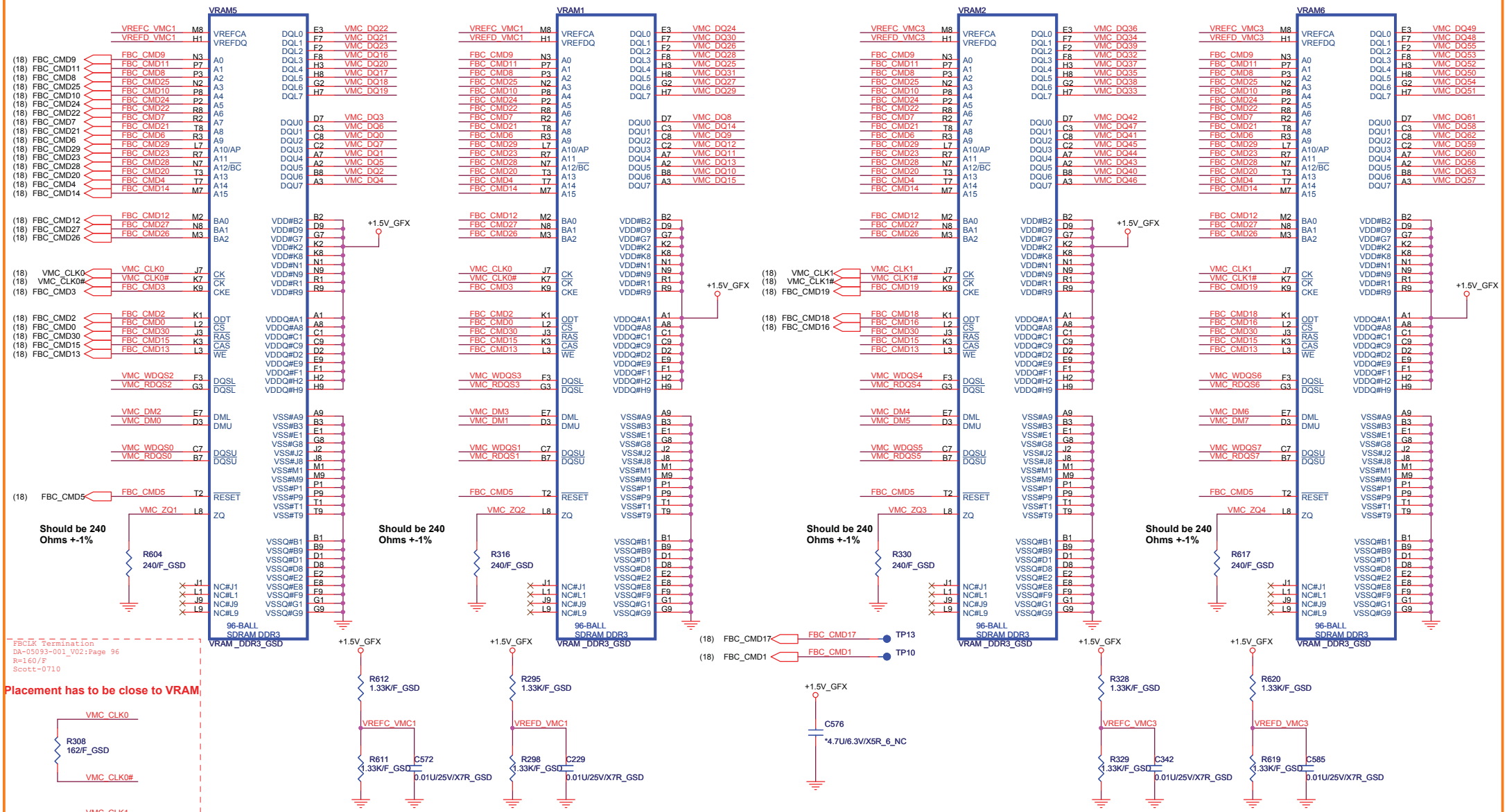
CHANNEL A: 256MB/512MB DDR3

(18) VMA_DQ[63..0]
(18) VMA_DM[7..0]
(18) VMA_WDQS[7..0]
(18) VMA_RDQS[7..0]



CHANNEL B: 256MB/512MB DDR3

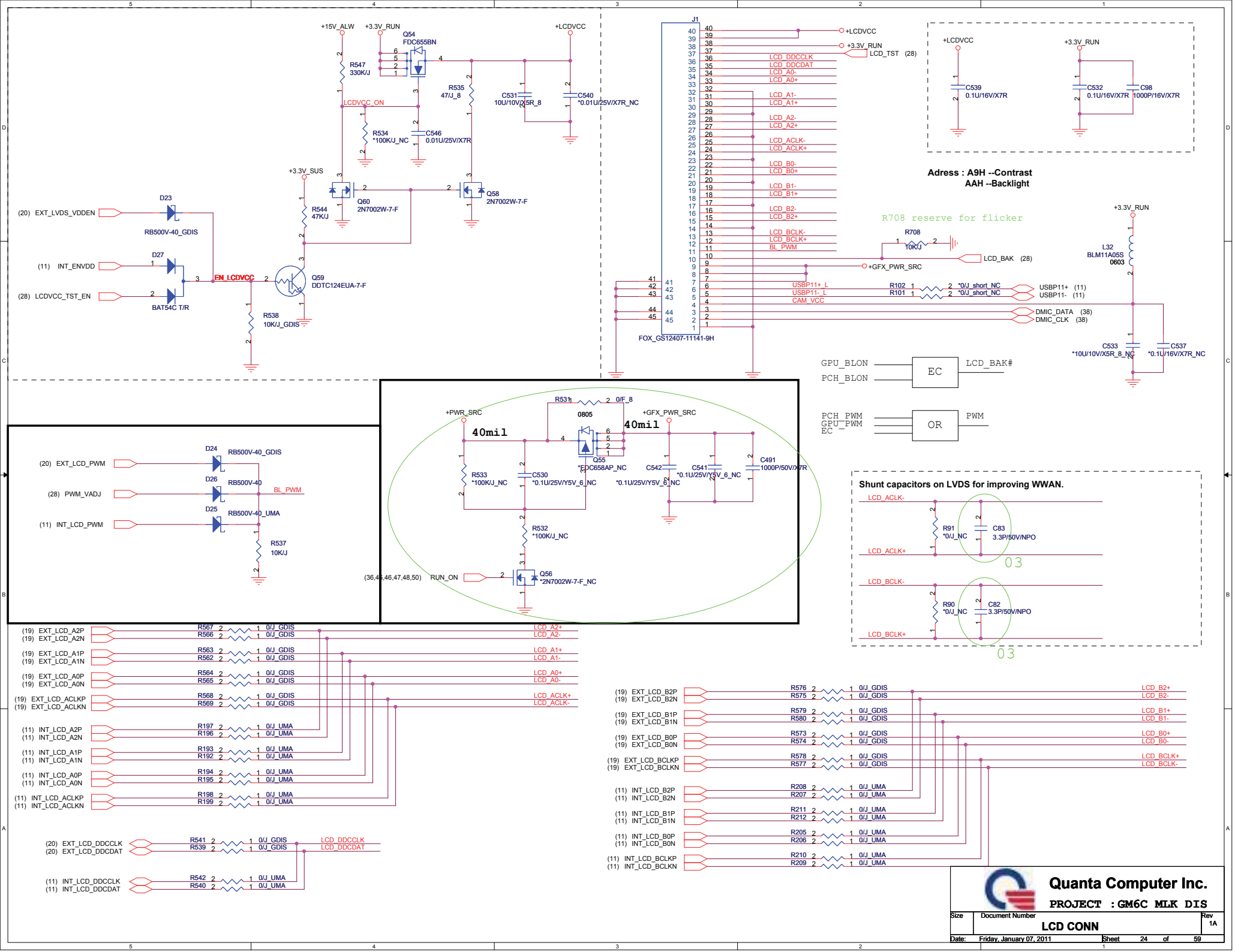
(18) VMC_DQ[63..0]
(18) VMC_DM[7..0]
(18) VMC_WDQS[7..0]
(18) VMC_RDQS[7..0]



NB5

PROJECT : TWH
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DGPU Memory 2/2 (DDR3)	1A
Date: Friday, January 07, 2011	Sheet 23 of 59	


+15V_ALW
+3.3V_RUN
Q54
FDC655BN
R547
330K/J
LCDVCC_ON
R535
47/J_8
C531
10U/10V/X5R_8
C540
*0.01U/25V/X7R_NC
R534
*100K/J_NC
C546
0.01U/25V/X7R
+LCDVCC
+3.3V_SUS
Q60
2N7002W-7-F
Q58
2N7002W-7-F
R544
47K/J
D23
RB500V-40_GDIS
(20) EXT_LVDS_VDDEN
D27
(11) INT_ENVDD
BAT54C T/R
(28) LCDVCC_TST_EN
EN_LCDVCC
Q59
DDTC124EUA-7-F
R538
10K/J_GDIS
J1
FOX_GS12407-11141-9H
LCD_DDCCLK
LCD_DDCDAT
LCD_A0-
LCD_A0+
LCD_A1-
LCD_A1+
LCD_A2-
LCD_A2+
LCD_ACLK-
LCD_ACLK+
LCD_B0-
LCD_B0+
LCD_B1-
LCD_B1+
LCD_B2-
LCD_B2+
LCD_BCLK-
LCD_BCLK+
BL_PWM
+GFX_PWR_SRC
LCD_TST (28)
USBP11+_L
USBP11-_L
CAM_VCC
R102
R101
*0/J_short_NC
USBP11+ (11)
USBP11- (11)
DMIC_DATA (38)
DMIC_CLK (38)
C539
0.1U/16V/X7R
C532
0.1U/16V/X7R
C98
1000P/16V/X7R
Adress : A9H --Contrast
AAH --Backlight
R708 reserve for flicker
R708
10K/J
LCD_BAK (28)
L32
BLM11A05S
0603
C533
*10U/10V/X5R_8_NC
C537
*0.1U/16V/X7R_NC
GPU_BLON
PCH_BLON
EC
LCD_BAK#
PCH_PWM
GPU_PWM
EC_
OR
PWM
D24
RB500V-40_GDIS
D26
RB500V-40
D25
RB500V-40_UMA
(20) EXT_LCD_PWM
(28) PWM_VADJ
(11) INT_LCD_PWM
BL_PWM
R537
10K/J
+PWR_SRC
+GFX_PWR_SRC
40mil
40mil
R531
0/F_8
0805
Q55
*EDC658AP_NC
R533
*100K/J_NC
C530
*0.1U/25V/Y5V_6_NC
C542
*0.1U/25V/Y5V_6_NC
C541
*0.1U/25V/Y5V_6_NC
C491
1000P/50V/X7R
R532
*100K/J_NC
(36,45,46,47,48,50) RUN_ON
Q56
*2N7002W-7-F_NC
Shunt capacitors on LVDS for improving WWAN.
R91
*0/J_NC
C83
3.3P/50V/NPO
R90
*0/J_NC
C82
3.3P/50V/NPO
03
03
(19) EXT_LCD_A2P
(19) EXT_LCD_A2N
(19) EXT_LCD_A1P
(19) EXT_LCD_A1N
(19) EXT_LCD_A0P
(19) EXT_LCD_A0N
(19) EXT_LCD_ACLKP
(19) EXT_LCD_ACLKN
R567
R566
R563
R562
R564
R565
R568
R569
0/J_GDIS
LCD_A2+
LCD_A2-
LCD_A1+
LCD_A1-
LCD_A0+
LCD_A0-
LCD_ACLK+
LCD_ACLK-
(11) INT_LCD_A2P
(11) INT_LCD_A2N
(11) INT_LCD_A1P
(11) INT_LCD_A1N
(11) INT_LCD_A0P
(11) INT_LCD_A0N
(11) INT_LCD_ACLKP
(11) INT_LCD_ACLKN
R197
R196
R193
R192
R194
R195
R198
R199
0/J_UMA
(19) EXT_LCD_B2P
(19) EXT_LCD_B2N
(19) EXT_LCD_B1P
(19) EXT_LCD_B1N
(19) EXT_LCD_B0P
(19) EXT_LCD_B0N
(19) EXT_LCD_BCLKP
(19) EXT_LCD_BCLKN
R576
R575
R579
R580
R573
R574
R578
R577
LCD_B2+
LCD_B2-
LCD_B1+
LCD_B1-
LCD_B0+
LCD_B0-
LCD_BCLK+
LCD_BCLK-
(11) INT_LCD_B2P
(11) INT_LCD_B2N
(11) INT_LCD_B1P
(11) INT_LCD_B1N
(11) INT_LCD_B0P
(11) INT_LCD_B0N
(11) INT_LCD_BCLKP
(11) INT_LCD_BCLKN
R208
R207
R211
R212
R205
R206
R210
R209
(20) EXT_LCD_DDCCLK
(20) EXT_LCD_DDCDAT
R541
R539
LCD_DDCCLK
LCD_DDCDAT
(11) INT_LCD_DDCCLK
(11) INT_LCD_DDCDAT
R542
R540
Quanta Computer Inc.
PROJECT : GM6C MLK DIS
Size
Document Number
LCD CONN
Rev
1A
Date: Friday, January 07, 2011
Sheet 24 of 59

HDMI

EQUALIZATION SETTING
PC1:PC0=0:0 8dB
PC1:PC0=0:1 4dB Recommanded
PC1:PC0=1:0 12dB
PC1:PC0=1:1 0dB

SCLZ/SDAZ Low-level input/output Voltage
CFG01:CFG00=0:0 VIL:<0.4V VOL:0.6V (Default)
CGF01:CGF00=0:1 VIL:<0.36V VOL:0.55V
CGF01:CGF00=1:0 VIL:<0.44V VOL:0.65V
CGF01:CGF00=1:1 VIL:<0.36V VOL:0.6V

+3.3V_RUN
L9 *BLM18PG181SN1_NC
+VCC_HDMI
C46 *1U/6.3V/X5R_NC
C78 *0.1U/16V/X7R_NC
C63 *0.1U/16V/X7R_NC

U5 *SN75DP139RGZR_NC
POWER: VCC (2,11,15,21,26,33,40,46)
GND (1,5,12,18,24,27,31,36,37,43,49 EPAD)
CONTROL: DDC_EN, PC0, PC1, DDCBUF_EN, CFG, RT_EN#, OE#, REXT

(41) HDMI_TXCP_L / HDMI_TXCN_L — C51 / C49 0.1U/16V/X7R — HDMI_TXCP_R / HDMI_TXCN_R — IN_D1+ / IN_D1- (39/38) — OUT_D1+ / OUT_D1- (22/23) — HDMI_CLK+_C / HDMI_CLK-_C
(41) HDMI_TXP0_L / HDMI_TXN0_L — C55 / C52 0.1U/16V/X7R — HDMI_TXP0_R / HDMI_TXN0_R — IN_D2+ / IN_D2- (42/41) — OUT_D2+ / OUT_D2- (19/20) — HDMI_TX0+_C / HDMI_TX0-_C
(41) HDMI_TXP1_L / HDMI_TXN1_L — C60 / C56 0.1U/16V/X7R — HDMI_TXP1_R / HDMI_TXN1_R — IN_D3+ / IN_D3- (45/44) — OUT_D3+ / OUT_D3- (16/17) — HDMI_TX1+_C / HDMI_TX1-_C
(41) HDMI_TXP2_L / HDMI_TXN2_L — C64 / C61 0.1U/16V/X7R — HDMI_TXP2_R / HDMI_TXN2_R — IN_D4+ / IN_D4- (48/47) — OUT_D4+ / OUT_D4- (13/14) — HDMI_TX2+_C / HDMI_TX2-_C
(41) HDMI_SCL_S — HDMI_SCL_S — SCL (9) — SCL_SINK (28) — HDMI_CLK
(41) HDMI_SDA_S — HDMI_SDA_S — SDA (8) — SDA_SINK (29) — HDMI_DAT
(11,41) INT_HDMI_HPD — INT_HDMI_HPD — HPD (7) — HPD_SINK (30) — HDMI_DET_L — R38 *1K/J_NC — HDMI_DET
R388 *100K/J_NC

+3.3V_RUN — R49 *100K/J_NC
R40 *4.7K/J_NC DDC_EN
R86 *4.7K/J_NC PC0
R73 *4.7K/J_NC PC1
CFG00
(10) HDMI_PWR_CTRL — R37 *0/J_NC — OE#
R74 *3.9K/J_NC
R72 *4.7K/J_NC PC0
R47 *0/J_NC
PQ1 *2N7002W-7-F_NC — HDMI_DET
R46 *4.7K/J_NC CFG00

+5V_HDMI — R7 2.2K/J — R3 2.2K/J
CN2 LTS_ABA-HDM-024-P07
HDMI_TX2+ / HDMI_TX2- / HDMI_TX1+ / HDMI_TX1- / HDMI_TX0+ / HDMI_TX0- / HDMI_CLK+ / HDMI_CLK-
HDMI_CLK / HDMI_DAT
HDMI_DET
+5V_HDMI — HDMIF1 NANOSMDC110F-2 — +5V_RUN
C513 *0.1U/16V/X7R_NC
C514 0.1U/16V/X7R

Reserve for EMI and close to HDMI CONN
*EXC24CG900U_NC L1: HDMI_TX2+_C / HDMI_TX2-_C ↔ HDMI_TX2+ / HDMI_TX2-
*EXC24CG900U_NC L4: HDMI_TX0+_C / HDMI_TX0-_C ↔ HDMI_TX0+ / HDMI_TX0-
*EXC24CG900U_NC L2: HDMI_TX1+_C / HDMI_TX1-_C ↔ HDMI_TX1+ / HDMI_TX1-
*EXC24CG900U_NC L3: HDMI_CLK+_C / HDMI_CLK-_C ↔ HDMI_CLK+ / HDMI_CLK-

change
HDMI_TXCP_R / HDMI_TXCN_R → HDMI_CLK+_C / HDMI_CLK-_C
HDMI_TXP0_R / HDMI_TXN0_R → HDMI_TX0+_C / HDMI_TX0-_C
HDMI_TXP1_R / HDMI_TXN1_R → HDMI_TX1+_C / HDMI_TX1-_C
HDMI_TXP2_R / HDMI_TXN2_R → HDMI_TX2+_C / HDMI_TX2-_C

UMA change to 680ohm
R736 499/F HDMI_TX2+
R734 499/F HDMI_TX2-
R737 499/F HDMI_TX1+
R731 499/F HDMI_TX1-
R729 499/F HDMI_TX0+
R733 499/F HDMI_TX0-
R735 499/F HDMI_CLK+
R730 499/F HDMI_CLK-
+3.3V_RUN — Q75 2N7002W-7-F — R732 1M

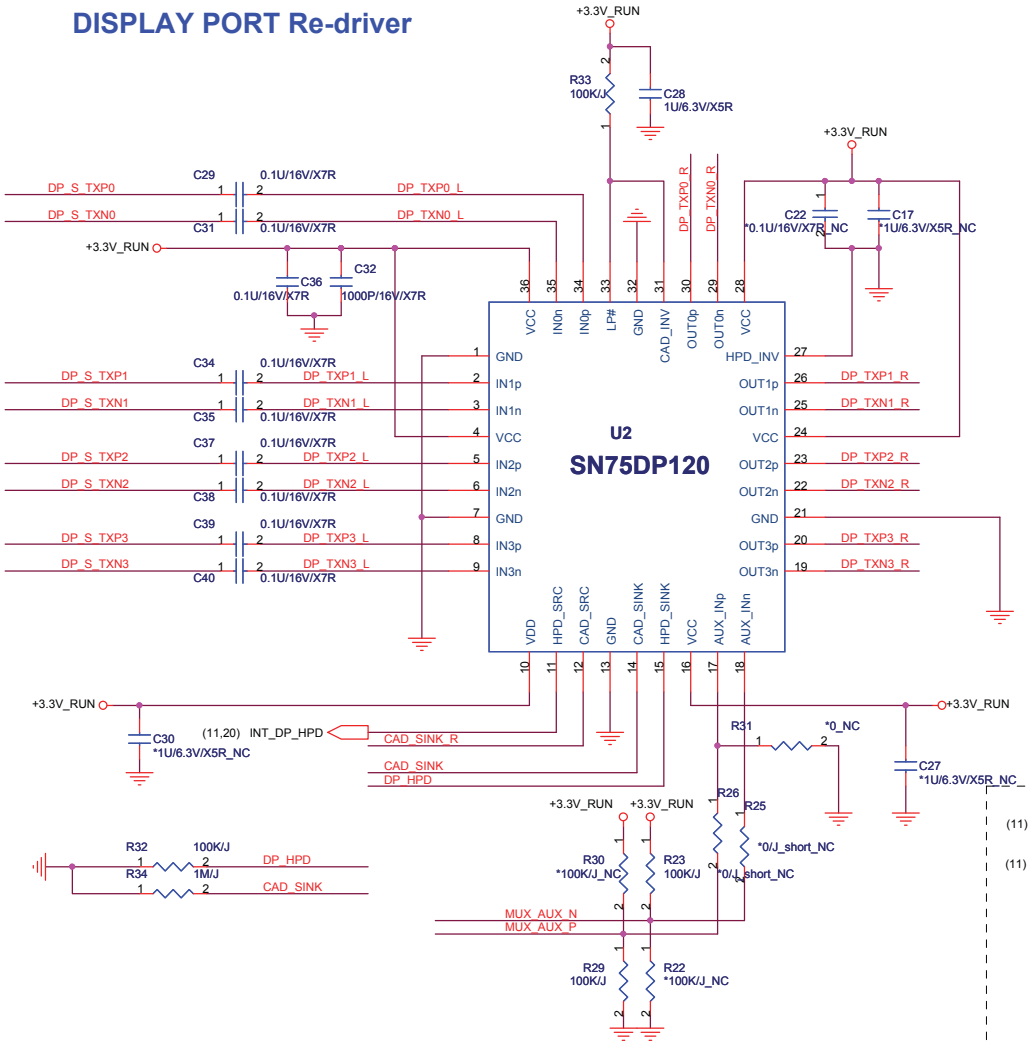
+3.3V_RUN — Q74 MMST3904-7-F — HDMI_HPD — R727 150K — HDMI_DET
(11,41) INT_HDMI_HPD — R728 10K

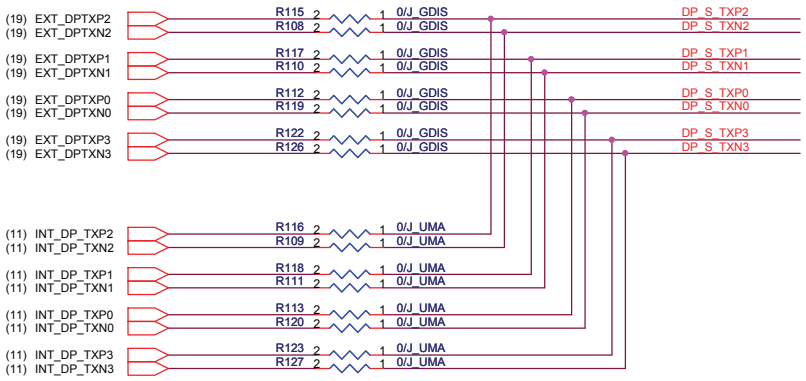
+3.3V_RUN — R709 2.2K/J — R437 2.2K/J
(41) HDMI_SCL_S — HDMI_SCL_S — Q73 FDV301N — HDMI_CLK
+3.3V_RUN
(41) HDMI_SDA_S — HDMI_SDA_S — Q72 FDV301N — HDMI_DAT

Quanta Computer Inc.
PROJECT : GM6C MLK DIS

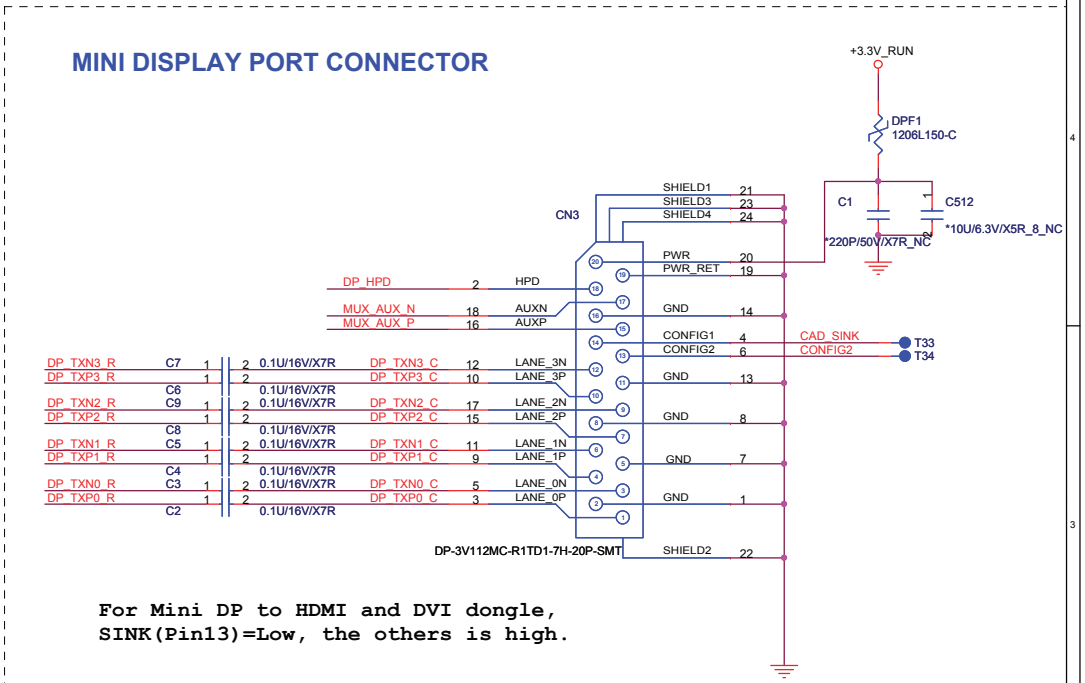
Size	Document Number	Rev
	HDMI CONN	1A
Date: Friday, January 07, 2011	Sheet 25 of 59	

DISPLAY PORT Re-driver

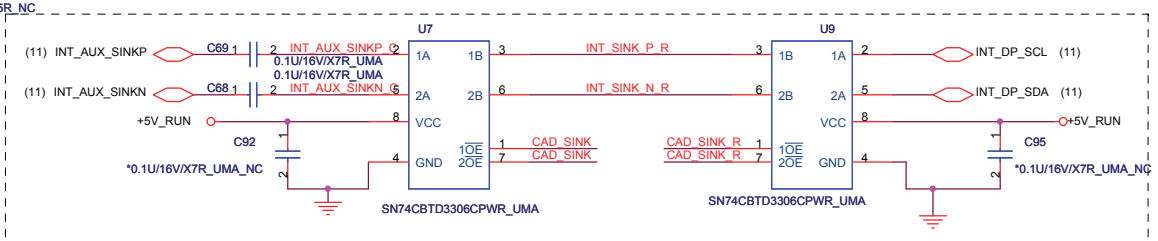


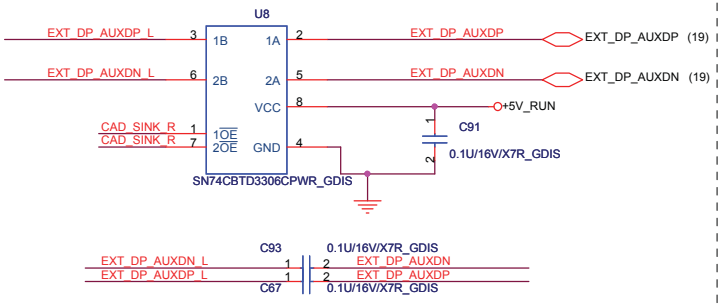


MINI DISPLAY PORT CONNECTOR

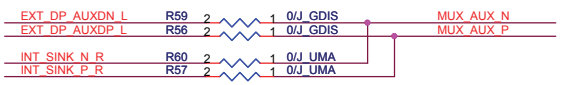


For Mini DP to HDMI and DVI dongle, SINK(Pin13)=Low, the others is high.





OE	Output
L	A=B
H	Z



Quanta Computer Inc.

PROJECT : GM6C MLK DIS

Size	Document Number	Rev
	MINI DP CONN	1A

Date: Friday, January 07, 2011 Sheet 26 of 59

2.2uF cap is no more than 250mils away from the power pin and a have a min trace width of 40mils.

MIDO Single End = 50 ohm

MIDO[0..5] Single Skew
Should be smaller +/- 100 mil
for SDA3.Application

Needs close to Pin17: 12mil/<250mil

Layout Note:
Place this cap close to pin 18

For AMD Platform only, Intel doesn't need to connect to PCH(Vendor)

W/L=20mil/<200mil

Card Reader interface signal mapping

PIN	Default	SD / MMC	MS	XD
MDIO00	SD/MMC/MS/xD	SD_D0	MS_D0	XD_D0
MDIO01		SD_D1	MS_D1	XD_D1
MDIO02		SD_D2	MS_D2	XD_D2
MDIO03		SD_D3	MS_D3	XD_D3
MDIO04		SD_CMD	MS_BS	XD_WE#
MDIO05		SD_CLK	MS_CLK	XD_CE#
MDIO06		SD_WP		XD_WP#
MDIO07				XD_CLE
MDIO08		MMC_D4	MS_D4	XD_D4
MDIO09		MMC_D5	MS_D5	XD_D5
MDIO10		MMC_D6	MS_D6	XD_D6
MDIO11		MMC_D7	MS_D7	XD_D7
MDIO12				XD_RE#
MDIO13				XD_R/B#
MDIO14				XD_ALE
CR1_LEDN		SD_LED#	MS_LED#	XD_LED#
CR1_PCTLN		SD_PWR#	MS_PWR#	XD_PWR#
CR1_CD0		SD_CD#		
CR1_CD1			MS_CD#	
CR1_CD2				XD_CD#

Quanta Computer Inc.			
PROJECT : GM6C MLK DIS			
Size	Document Number: Card Reader (JMB389)		Rev 1A
Date: Friday, January 07, 2011	Sheet 27 of 59		

BX1 leakage issue workaround circuit
R96,C104 no stuff,R100 stuff
BX2 will close it.
R96,C104 stuff,R100 no stuff

Layout Note: Place these caps close to ITE8502

Layout Note: Place PC169 close to ITE8502

IT8518E/CX

U11

LPC
CIR
UART port
EXTERNAL SERIAL FLASH
SPI ENABLE
KBMX
SM BUS
PS/2
GPIO
PWM
WAKE UP
A/D D/A
CLOCK
BAT

Thermal, MMB

For Crystal-Free

prochot pin level shift

Board ID Straps

Config_0	Config_1	GM6/GM6C
0	0	UMA
0	1	Optimum-GE
1	0	Studio Discrete
1	1	Optimum-GS

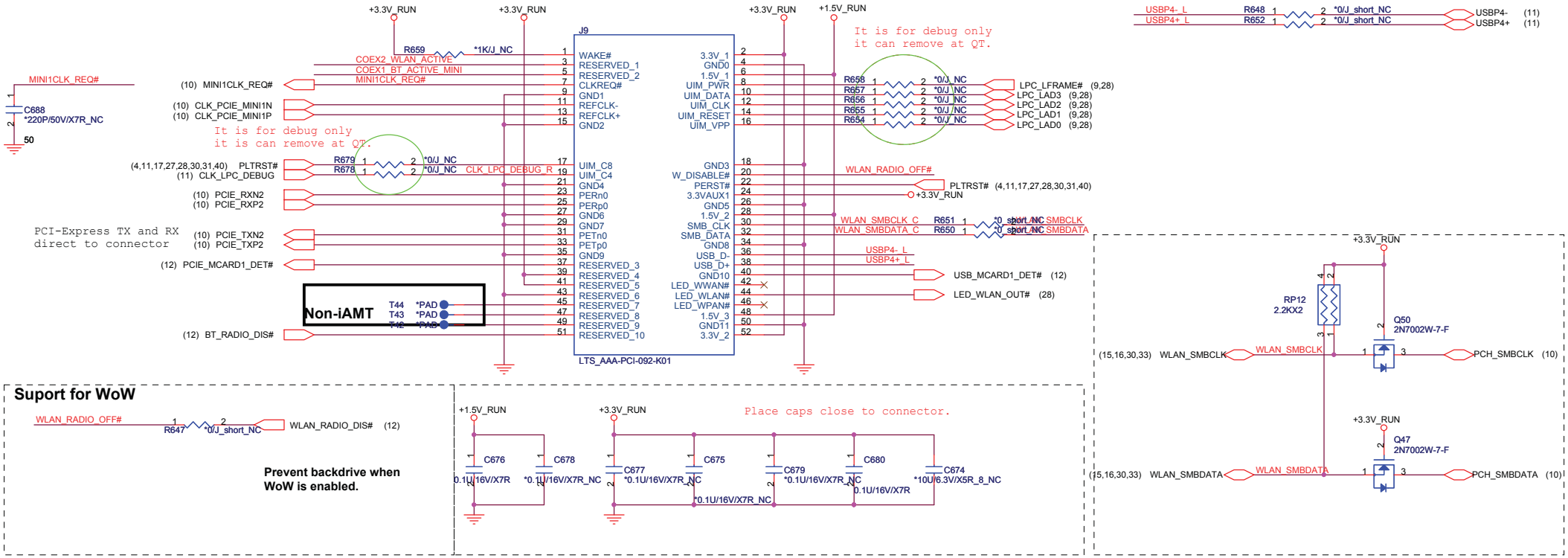
USB_BACK_EN#	BID1	GM6/GM6C
0	0	SSI (X00)
0	1	PT (X01)
1	0	ST (X02)
1	1	QT (A00)
0	0	(A01)

Quanta Computer Inc.
PROJECT : GM6C MLK DIS

Size	Document Number	Rev
	SIO (ITE8518)	1A

Date: Friday, January 07, 2011 Sheet 28 of 59

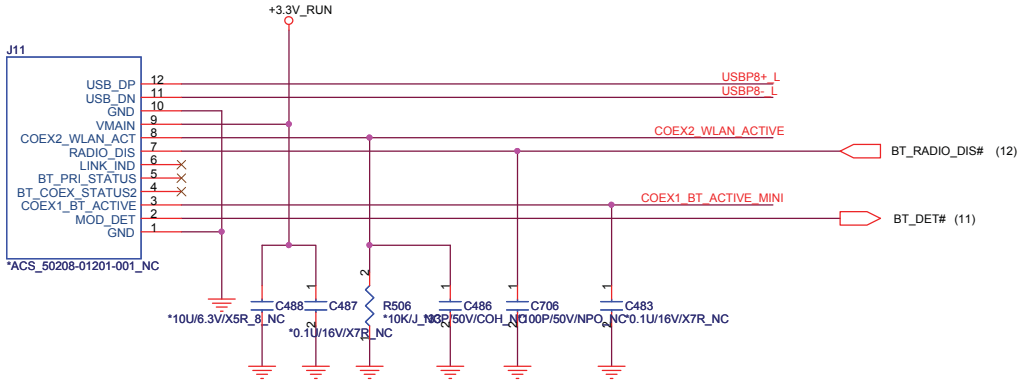
MiniCard WLAN connector

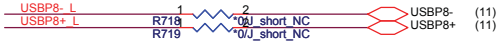


Suport for WoW

Prevent backdrive when WoW is enabled.

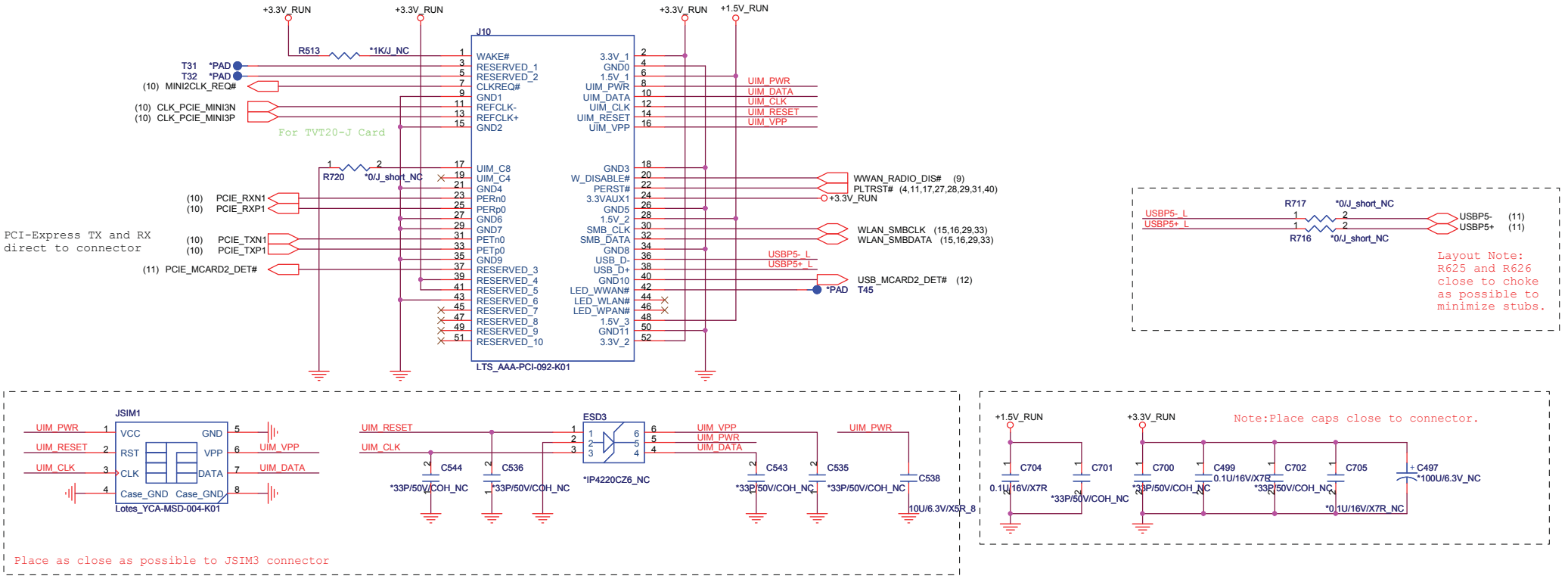
Support Dell BT375 (Little Stone) module (XPS) W TO B





Quanta Computer Inc.		
PROJECT : GM6C MLK DIS		
Size	Document Number: MINI-Card (WLAN/WPAN)	Rev 1A
Date: Friday, January 07, 2011	Sheet 29 of 59	

MiniCard WWAN connector

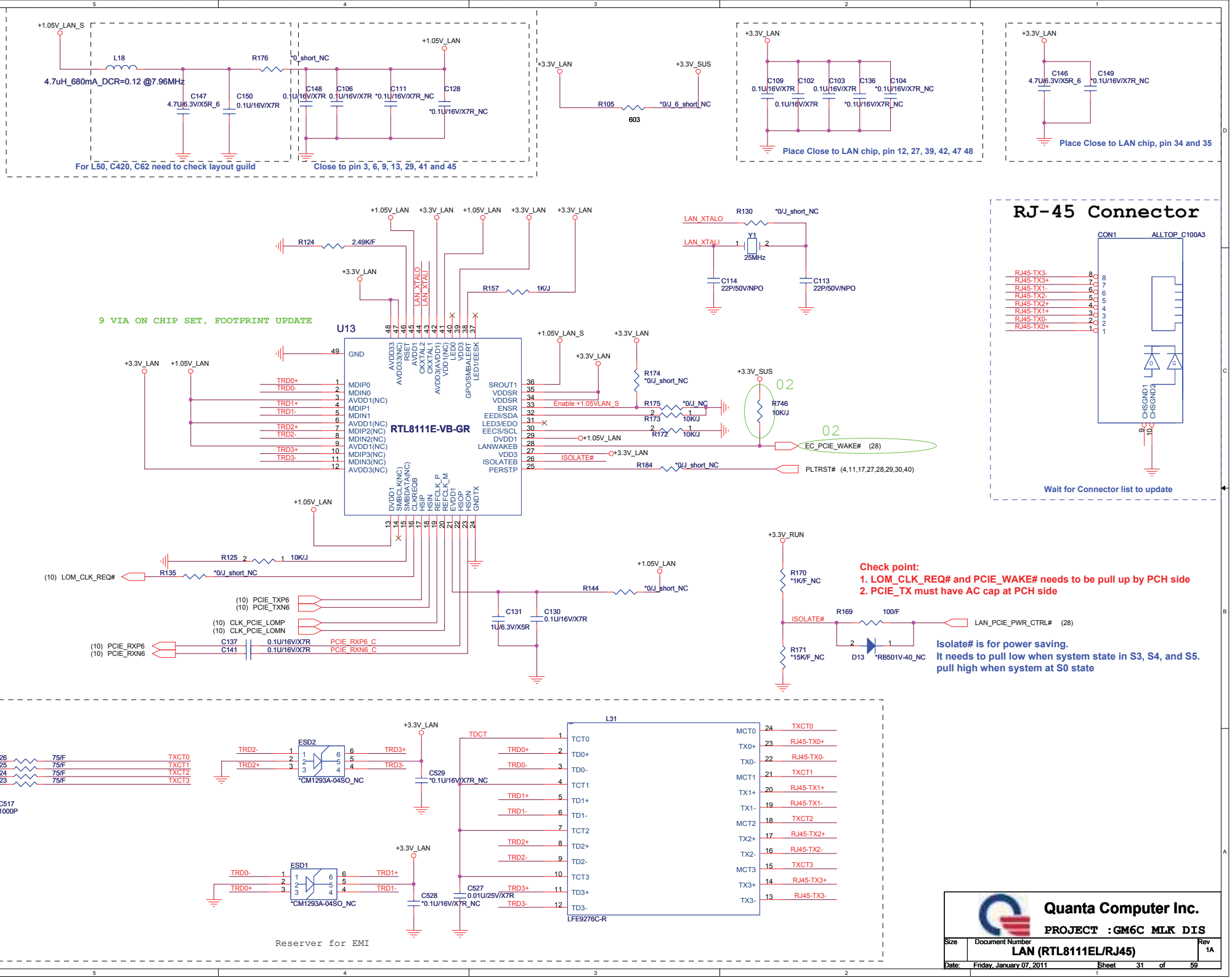


Quanta Computer Inc.

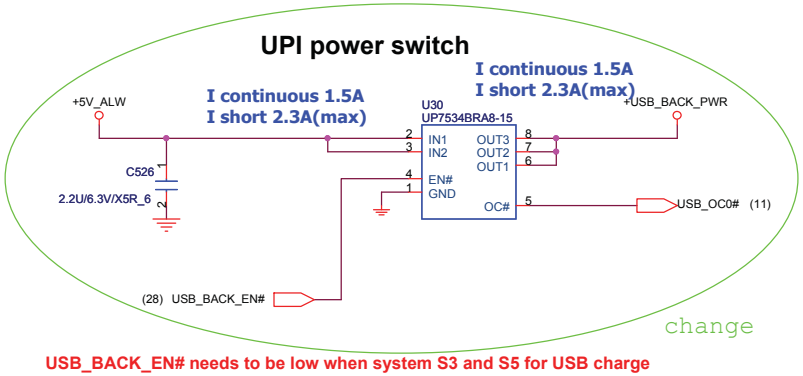
PROJECT : GM6C MLK DIS

Size	Document Number	Rev
	MINI-Card (WWAN)	1A

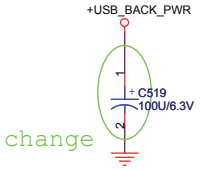
Date: Friday, January 07, 2011 Sheet 30 of 59


+1.05V_LAN_S
L18
4.7uH_680mA_DCR=0.12 @7.96MHz
R176
*0_short_NC
+1.05V_LAN
C147
4.7U/6.3V/X5R_6
C150
0.1U/16V/X7R
C148
0.1U/16V/X7R
C106
0.1U/16V/X7R
C111
*0.1U/16V/X7R_NC
C128
*0.1U/16V/X7R_NC
For L50, C420, C62 need to check layout guild
Close to pin 3, 6, 9, 13, 29, 41 and 45
+3.3V_LAN
R105
603
+3.3V_SUS
*0/J_6_short_NC
+3.3V_LAN
C109
0.1U/16V/X7R
C102
0.1U/16V/X7R
C103
0.1U/16V/X7R
C136
0.1U/16V/X7R
C104
*0.1U/16V/X7R_NC
Place Close to LAN chip, pin 12, 27, 39, 42, 47 48
+3.3V_LAN
C146
4.7U/6.3V/X5R_6
C149
*0.1U/16V/X7R_NC
Place Close to LAN chip, pin 34 and 35
RJ-45 Connector
CON1
ALLTOP_C100A3
RJ45-TX3-
RJ45-TX3+
RJ45-TX1-
RJ45-TX2-
RJ45-TX2+
RJ45-TX1+
RJ45-TX0-
RJ45-TX0+
CHSGND1
CHSGND2
Wait for Connector list to update
9 VIA ON CHIP SET, FOOTPRINT UPDATE
U13
RTL8111E-VB-GR
+1.05V_LAN
+3.3V_LAN
R124
2.49K/F
R157
1K/J
LAN_XTALO
LAN_XTALI
R130
*0/J_short_NC
Y1
25MHz
C114
22P/50V/NPO
C113
22P/50V/NPO
+1.05V_LAN_S
R174
*0/J_short_NC
Enable +1.05VLAN_S
R175
*0/J_NC
R173
10K/J
R172
10K/J
+3.3V_SUS
R746
10K/J
02
EC_PCIE_WAKE# (28)
ISOLATE#
R184
*0/J_short_NC
PLTRST# (4,11,17,27,28,29,30,40)
TRD0+
TRD0-
TRD1+
TRD1-
TRD2+
TRD2-
TRD3+
TRD3-
R125
10K/J
R135
*0/J_short_NC
(10) LOM_CLK_REQ#
(10) PCIE_TXP6
(10) PCIE_TXN6
(10) CLK_PCIE_LOMP
(10) CLK_PCIE_LOMN
(10) PCIE_RXP6
(10) PCIE_RXN6
C137
C141
0.1U/16V/X7R
PCIE_RXP6_C
PCIE_RXN6_C
C131
1U/6.3V/X5R
C130
0.1U/16V/X7R
R144
*0/J_short_NC
+3.3V_RUN
R170
*1K/F_NC
R171
*15K/F_NC
ISOLATE#
R169
100/F
LAN_PCIE_PWR_CTRL# (28)
D13
*RB501V-40_NC
Check point:
1. LOM_CLK_REQ# and PCIE_WAKE# needs to be pull up by PCH side
2. PCIE_TX must have AC cap at PCH side
Isolate# is for power saving.
It needs to pull low when system state in S3, S4, and S5.
pull high when system at S0 state
R526
R525
R524
R523
75/F
TXCT0
TXCT1
TXCT2
TXCT3
C517
1000P
ESD2
*CM1293A-04SO_NC
C529
*0.1U/16V/X7R_NC
ESD1
*CM1293A-04SO_NC
C528
*0.1U/16V/X7R_NC
C527
0.01U/25V/X7R
L31
LFE9276C-R
TDCT
TCT0
TD0+
TD0-
TCT1
TD1+
TD1-
TCT2
TD2+
TD2-
TCT3
TD3+
TD3-
MCT0
TX0+
TX0-
MCT1
TX1+
TX1-
MCT2
TX2+
TX2-
MCT3
TX3+
TX3-
TXCT0
RJ45-TX0+
RJ45-TX0-
TXCT1
RJ45-TX1+
RJ45-TX1-
TXCT2
RJ45-TX2+
RJ45-TX2-
TXCT3
RJ45-TX3+
RJ45-TX3-
Reserver for EMI
Quanta Computer Inc.
PROJECT : GM6C MLK DIS
Size
Document Number
LAN (RTL8111EL/RJ45)
Rev
1A
Date: Friday, January 07, 2011
Sheet 31 of 59

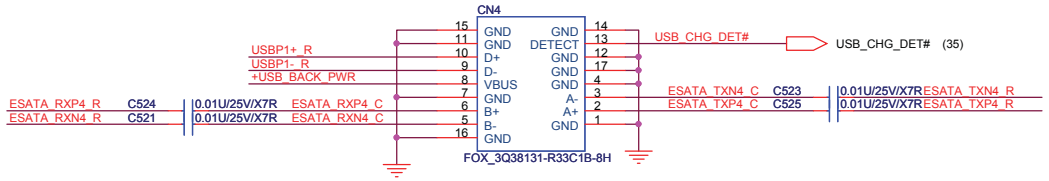
ESATA + USB Conn + Power Share

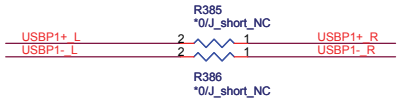


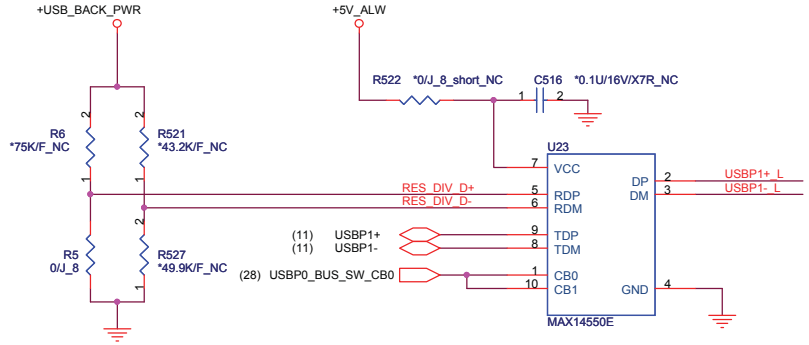
USB_BACK_EN# needs to be low when system S3 and S5 for USB charge



This pin connects to 3VALW ON POWER LOGIC







EC needs to drive CB0/CB1 pins to low when system S3/S5 and dirve high when system S0.

U49 PN and Footprint needs to double check

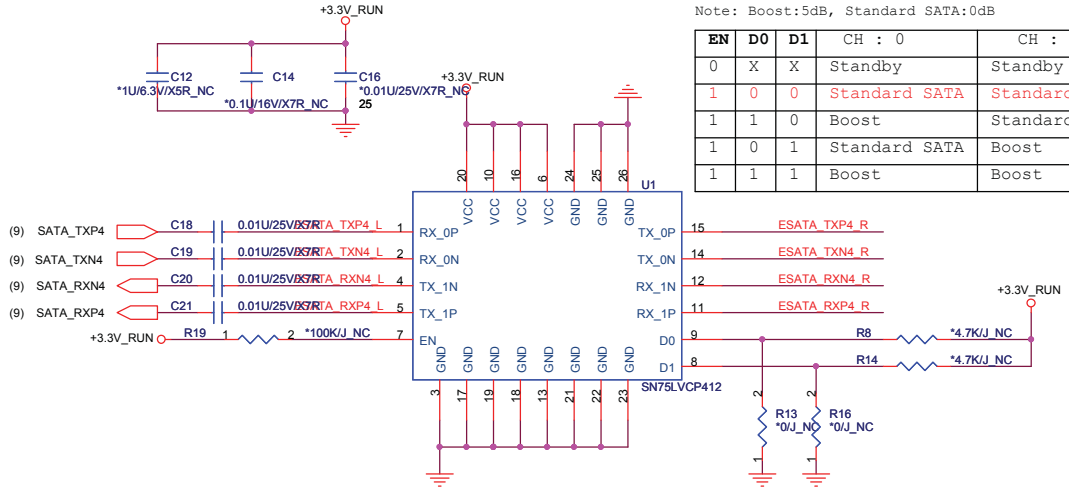
R15 needs to be 49.9K_F if we use external resisters.

CB0	CB1	Function
0	0	Auto Detection active
1	1	USB Function only

(5V)-43.2K-(D-)-49.9K-GND (about 2.68V)
(5V)-75.0K-(D+)-49.9K-GND (about 2.00V)

E-SATA Re-driver

Layout Note: Please put those on the same side of MB PCB



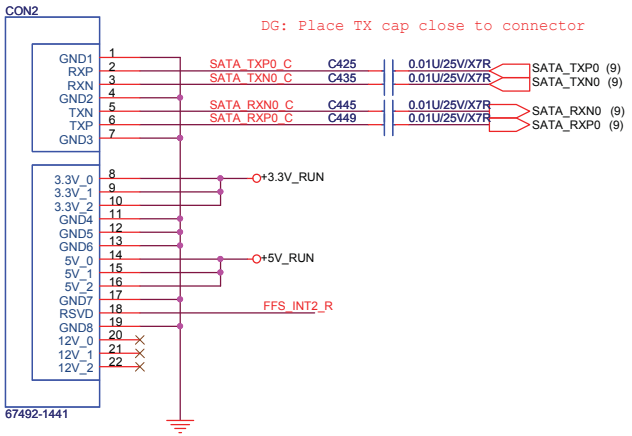
Note: Boost:5dB, Standard SATA:0dB

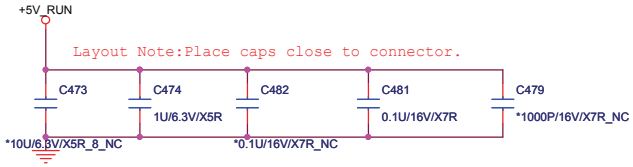
EN	D0	D1	CH : 0	CH : 1
0	X	X	Standby	Standby
1	0	0	Standard SATA	Standard SATA
1	1	0	Boost	Standard SATA
1	0	1	Standard SATA	Boost
1	1	1	Boost	Boost

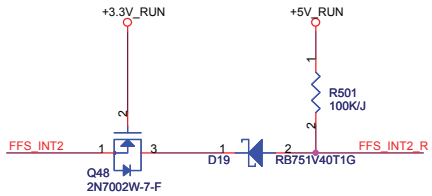
Quanta Computer Inc.
PROJECT : GM6C MLK DIS

Size	Document Number	Rev
	Righ PUSB/ESATA	1A
Date: Friday, January 07, 2011	Sheet 32 of 59	

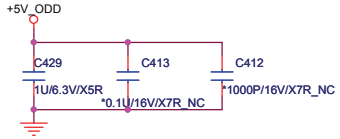
SATA Connector.

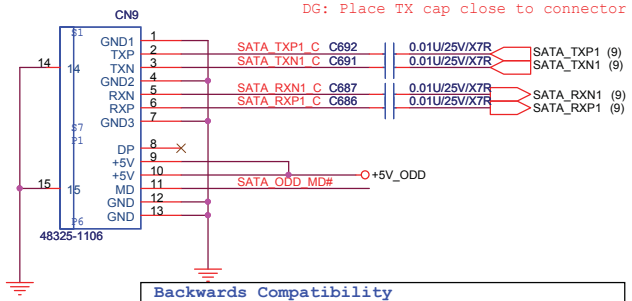




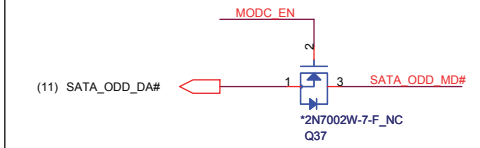


ODD Connector





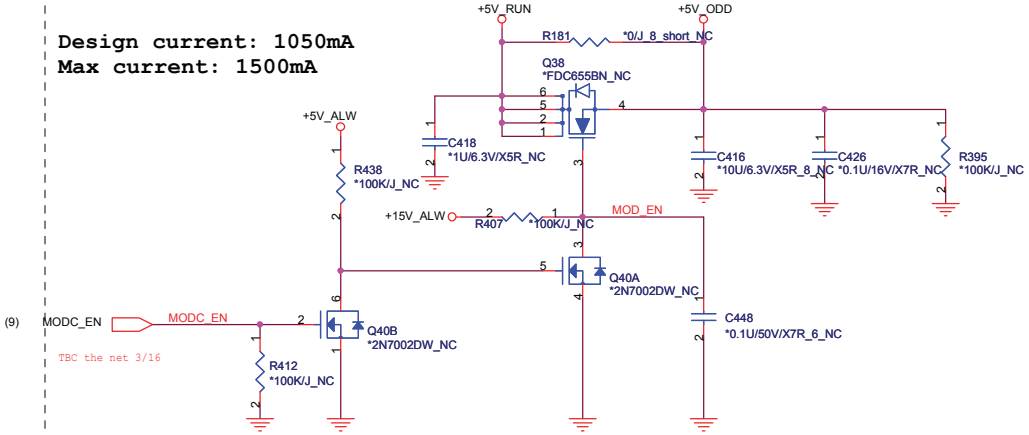
Backwards Compatibility



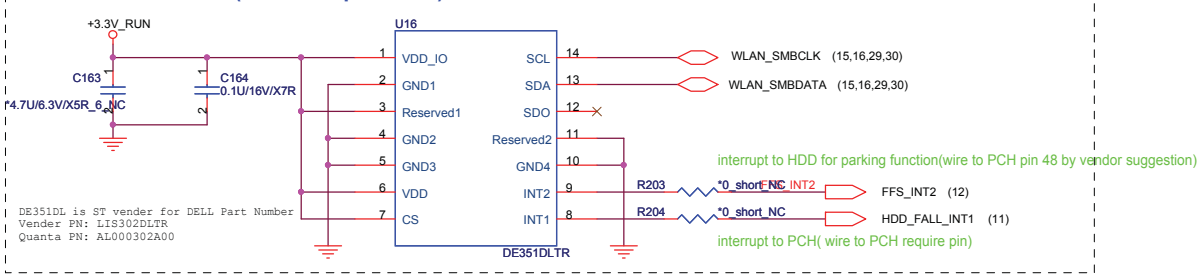
Drive powered on, MD# is High
Drive powered off, MD# is Low

Because the drive does not support ZPODD, the driver never powers off the power FET and never connects the MD/DA pin to the drive

Design current: 1050mA
Max current: 1500mA



3-axis Fall Sensor (HDD data protector)

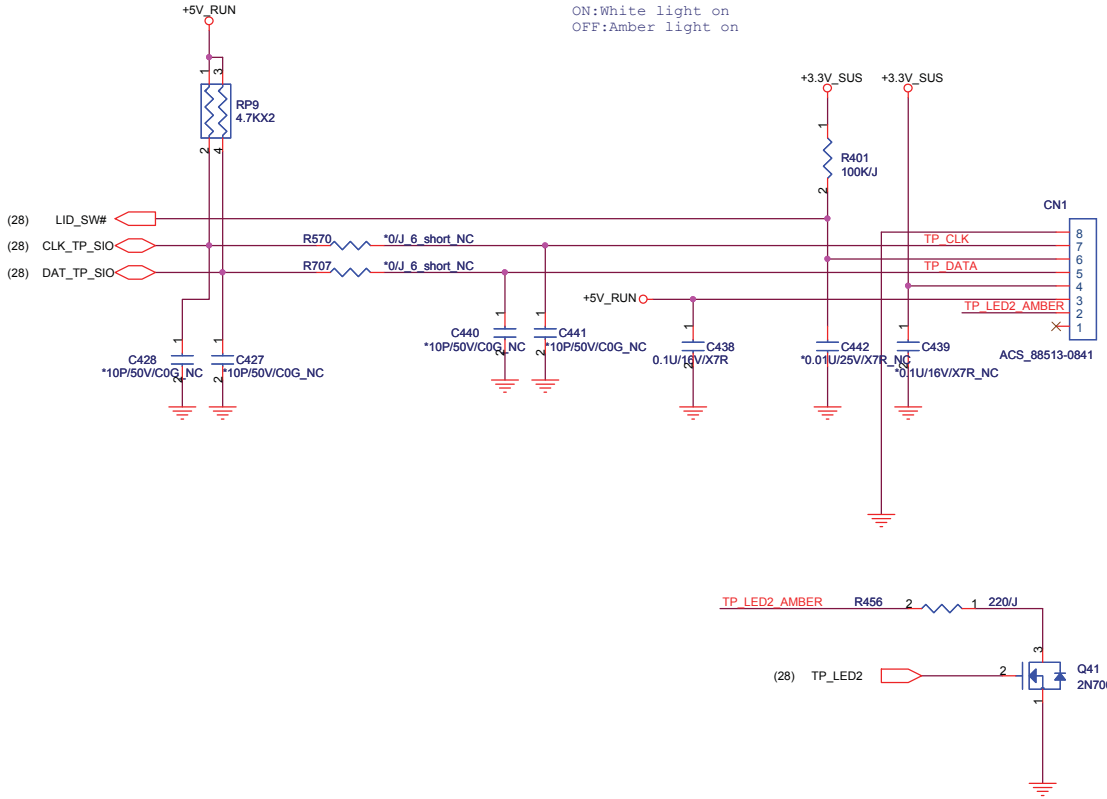


Quanta Computer Inc.
PROJECT : GM6C MLK DIS

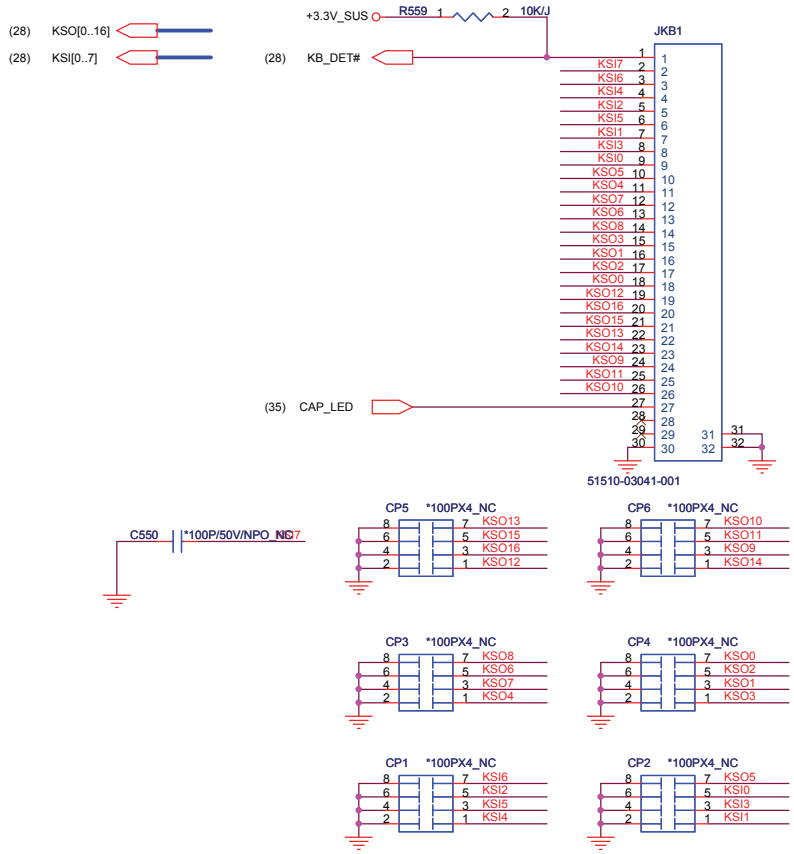
Size	Document Number	Rev
	SATA (HDD&ODD)	1A
Date: Friday, January 07, 2011	Sheet 33 of 59	

Touch Pad

ON:White light on
OFF:Amber light on



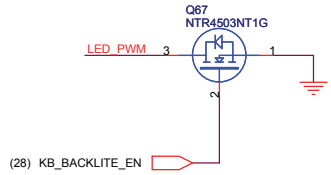
KEYBOARD CONNECTOR

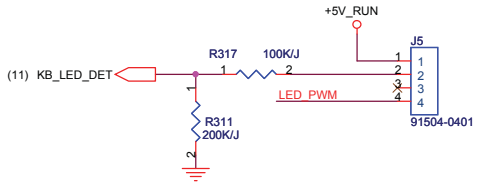


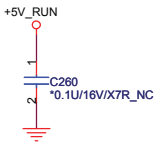
Layout Note: 100P CAPS CLOSE TO JKB3

Key board illumination

+KB_LED power trace width >10 mil

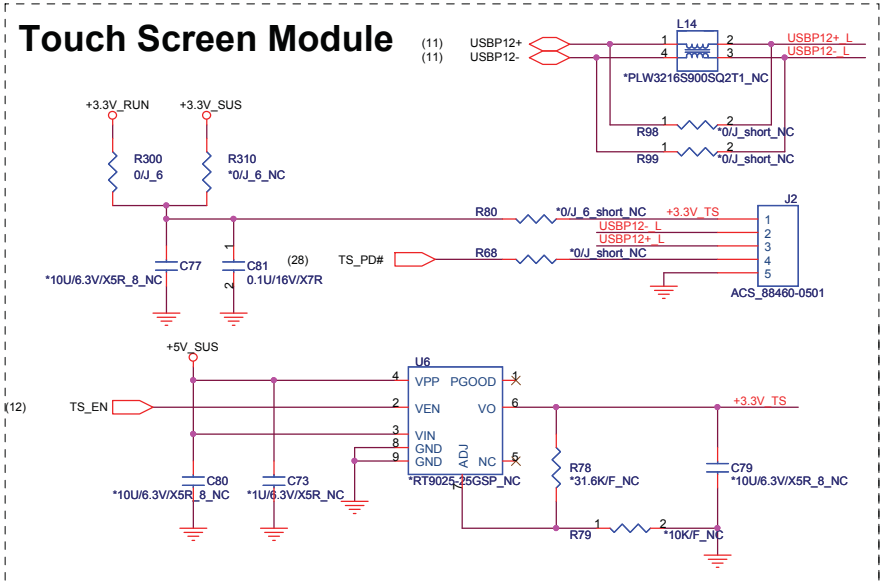




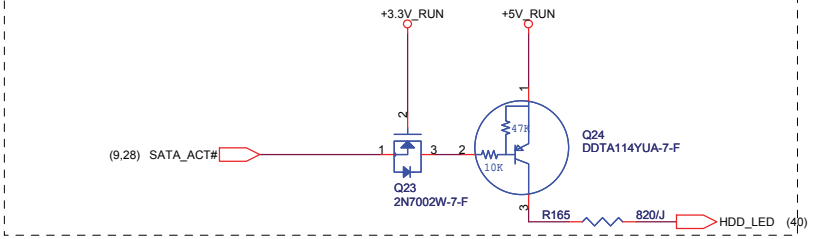


Quanta Computer Inc.		
PROJECT : GM6C MLK DIS		
Size	Document Number: TP/KB	Rev: 1A
Date: Friday, January 07, 2011	Sheet 34 of 59	

Touch Screen Module

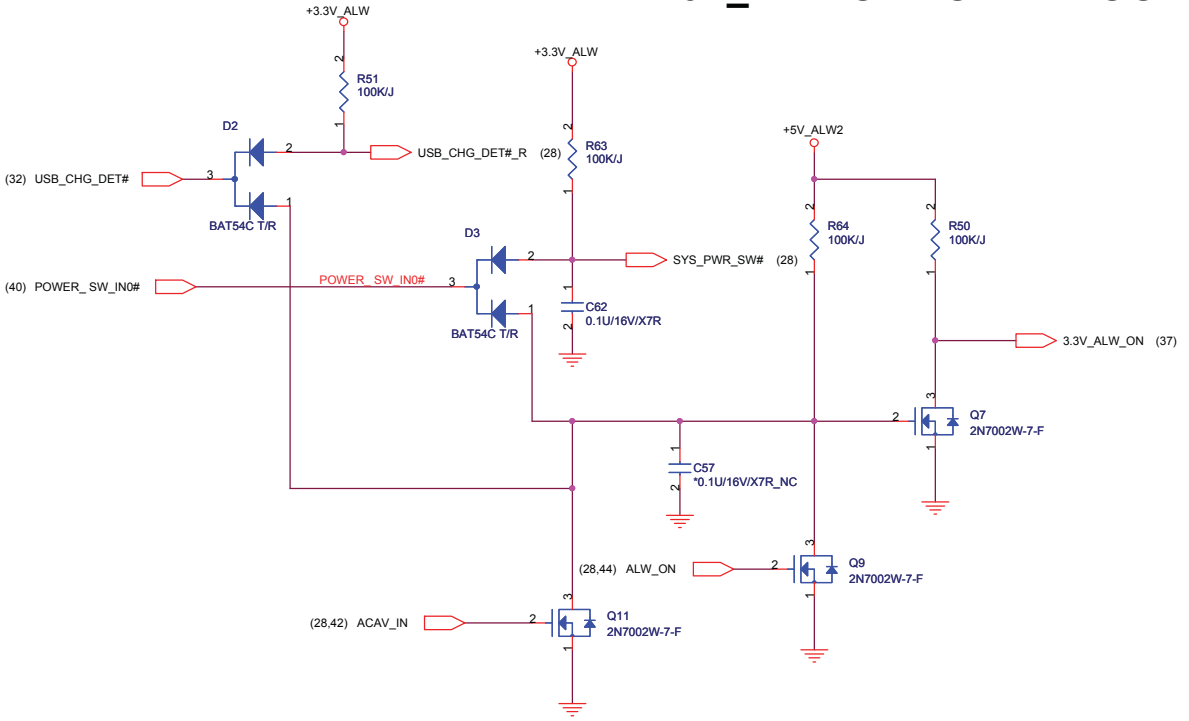


HDD activity LED.

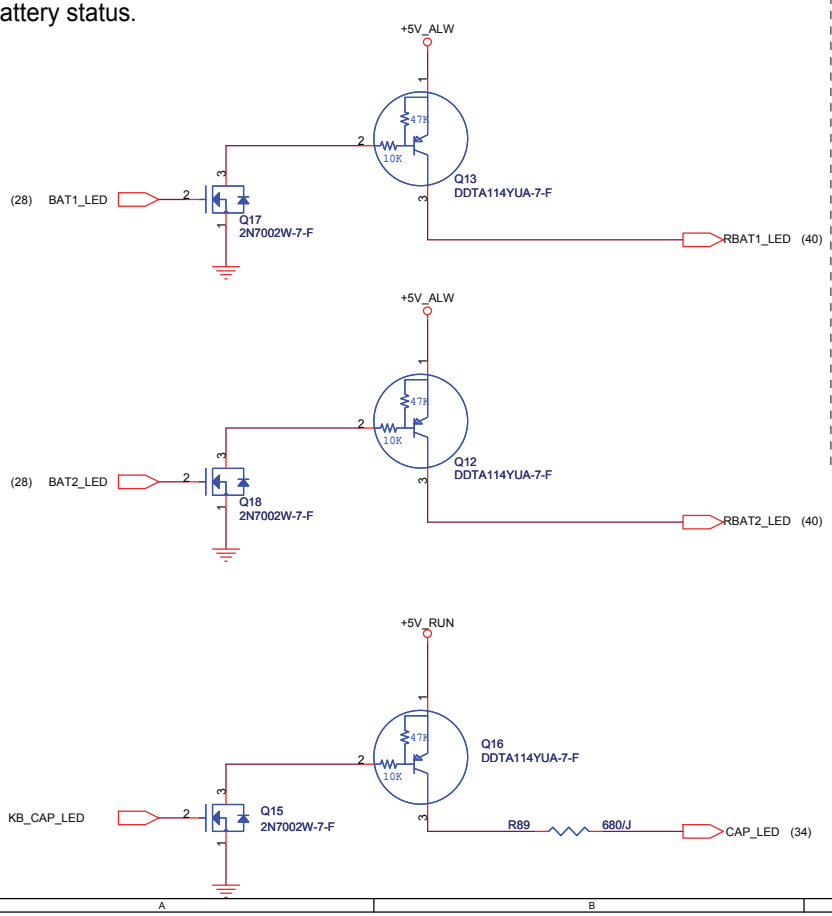


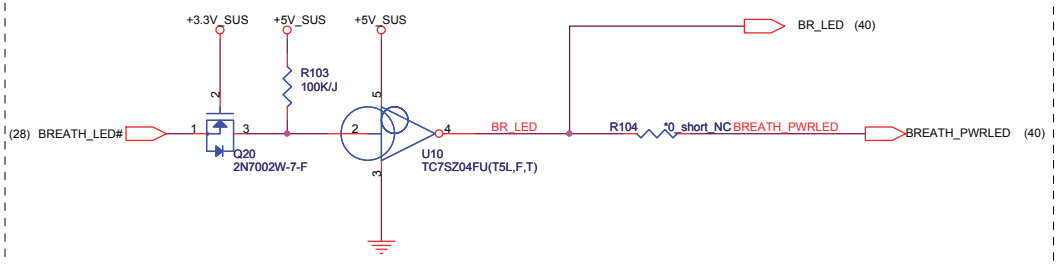
Power button for Engineer

3V_ALW ON POWER LOGIC



Battery status.



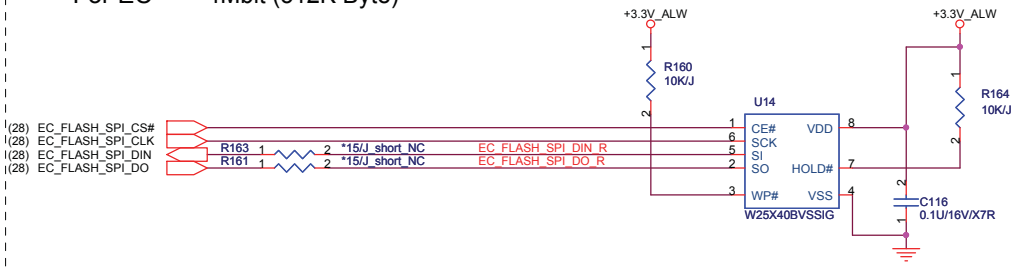


Quanta Computer Inc.

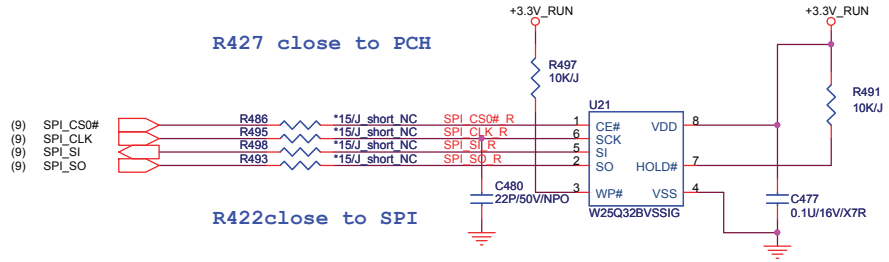
PROJECT : GM6C MLK DIS

Size	Document Number	Rev
	SWITCH/LED/T-Screen	1A
Date: Friday, January 07, 2011	Sheet 35 of 59	

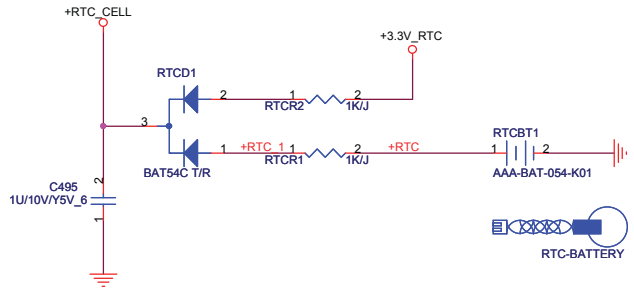
For EC 4Mbit (512K Byte)



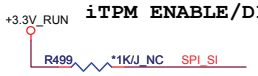
For PCH 32Mbit (4M Byte)



RTC BATTERY

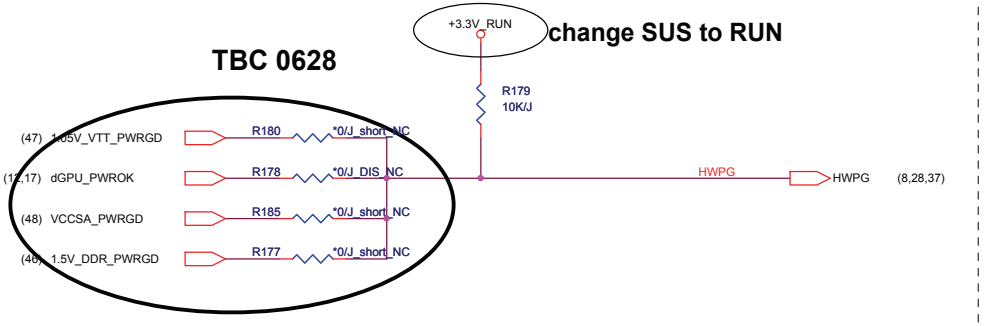


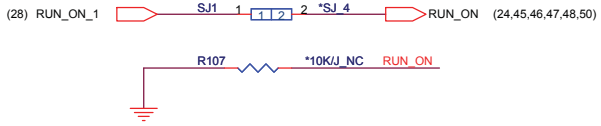
iTPM ENABLE/DISABLE



TPM Function	R428
Enable	Mount
Disable	NC (Default)

RESET CIRCUIT

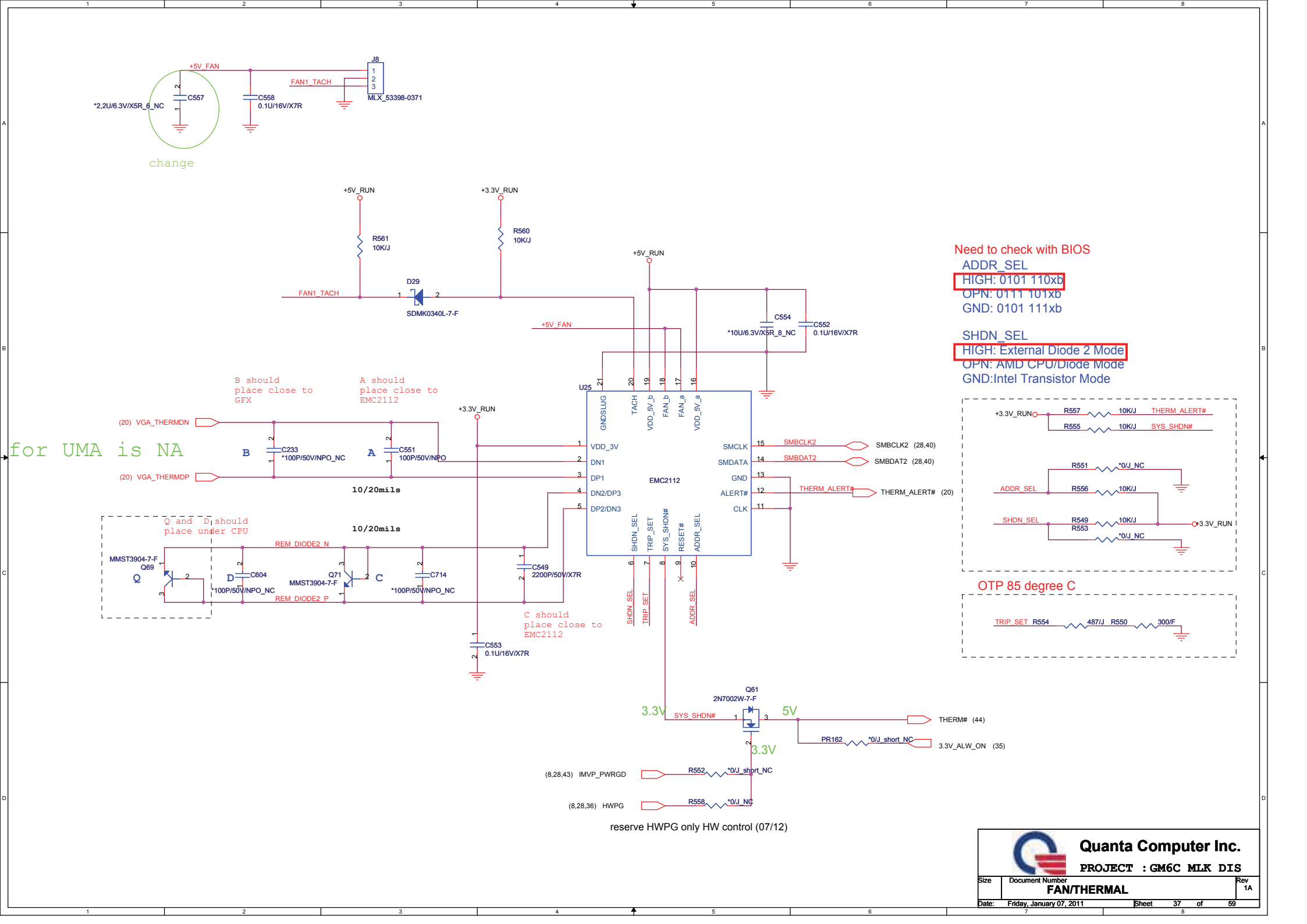




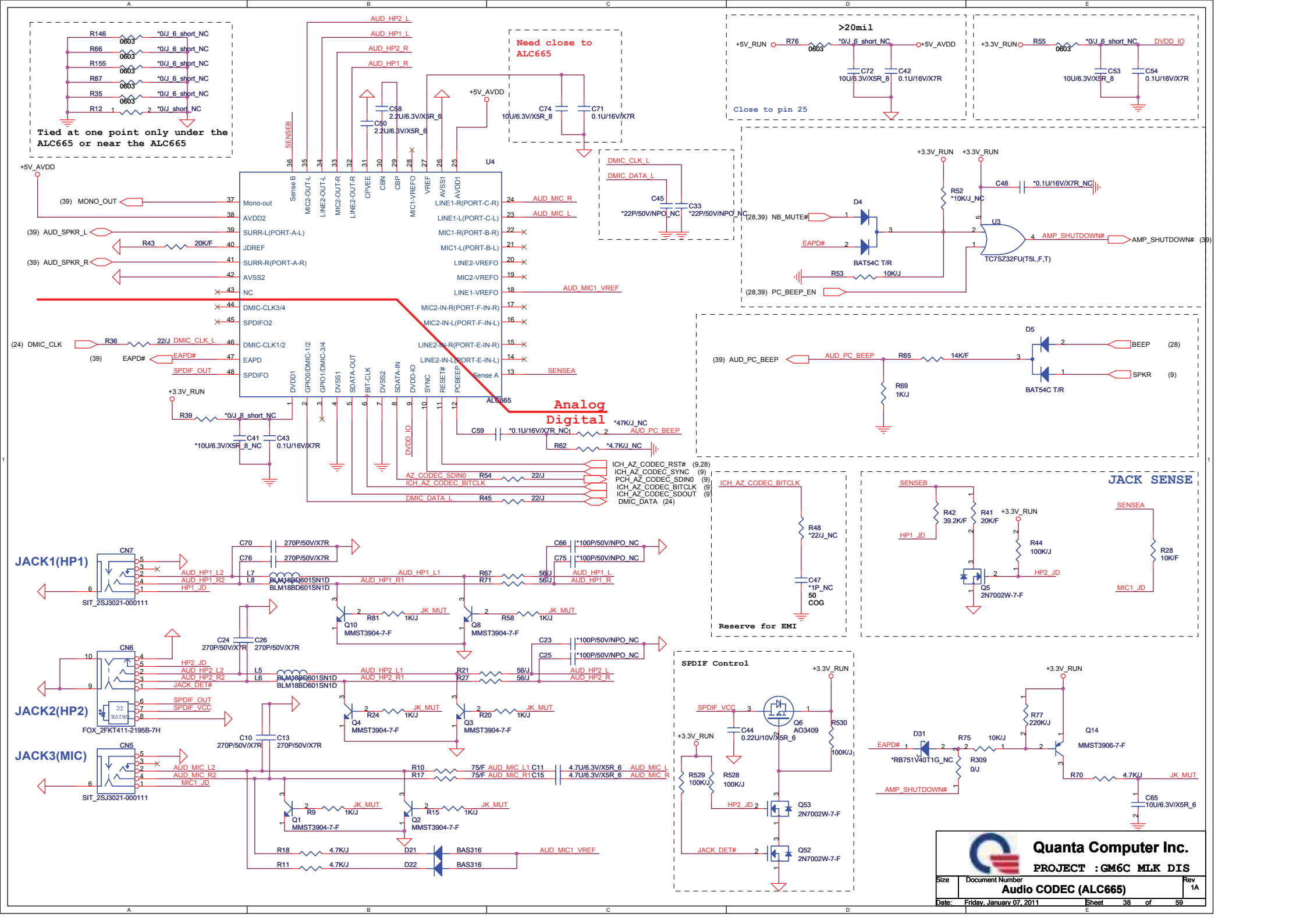
Quanta Computer Inc.

PROJECT : GM6C MLK DIS

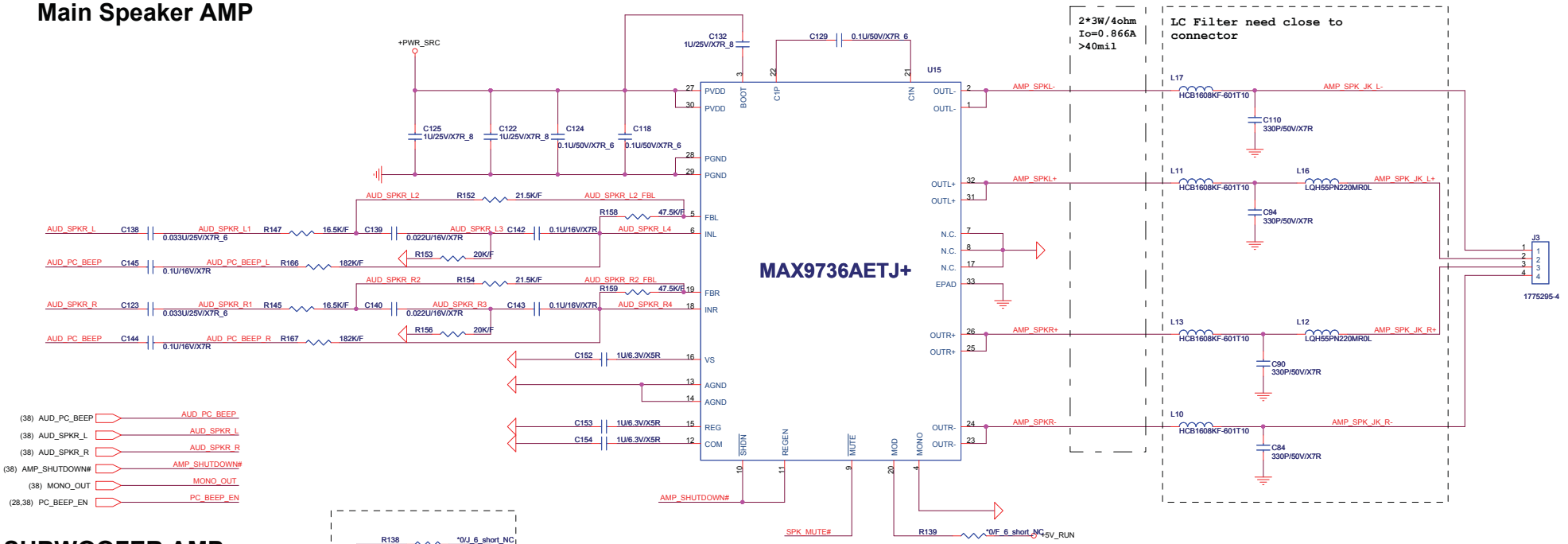
Size	Document Number	Rev
	FLASH/RTC/RESET CIRCUIT	1A
Date: Friday, January 07, 2011	Sheet 36 of 59	



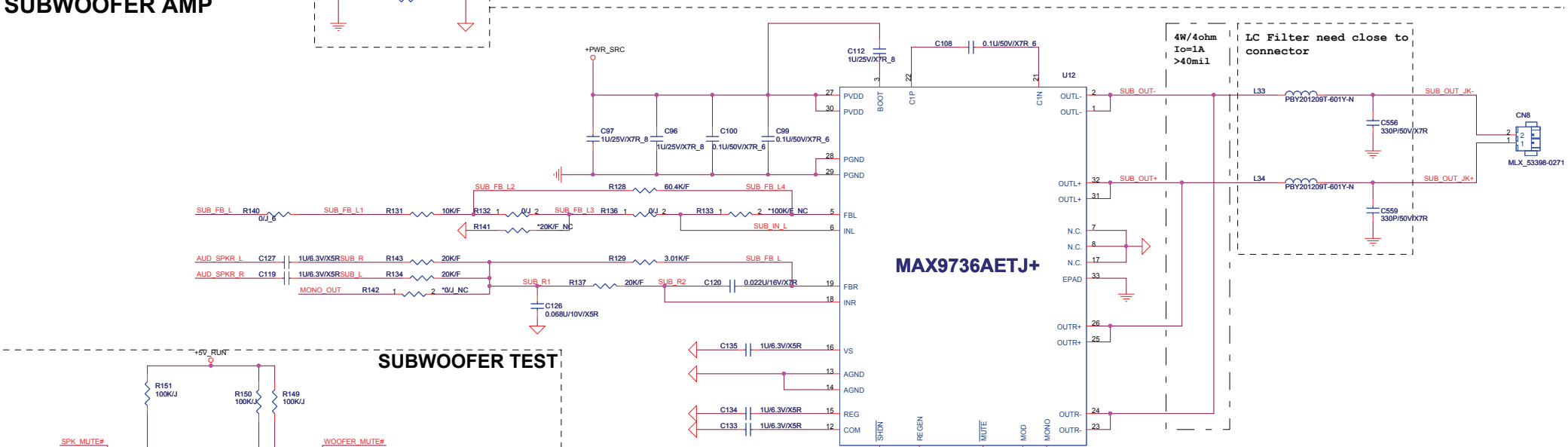
Quanta Computer Inc.		
PROJECT : GM6C MLK DIS		
Size	Document Number: FAN/THERMAL	Rev: 1A
Date: Friday, January 07, 2011	Sheet 37 of 59	


Tied at one point only under the ALC665 or near the ALC665
Need close to ALC665
>20mil
Close to pin 25
U4
ALC665
Analog
Digital
JACK1(HP1)
JACK2(HP2)
JACK3(MIC)
JACK SENSE
SPDIF Control
Reserve for EMI
Quanta Computer Inc.
PROJECT : GM6C MLK DIS
Audio CODEC (ALC665)
Date: Friday, January 07, 2011
Sheet 38 of 59

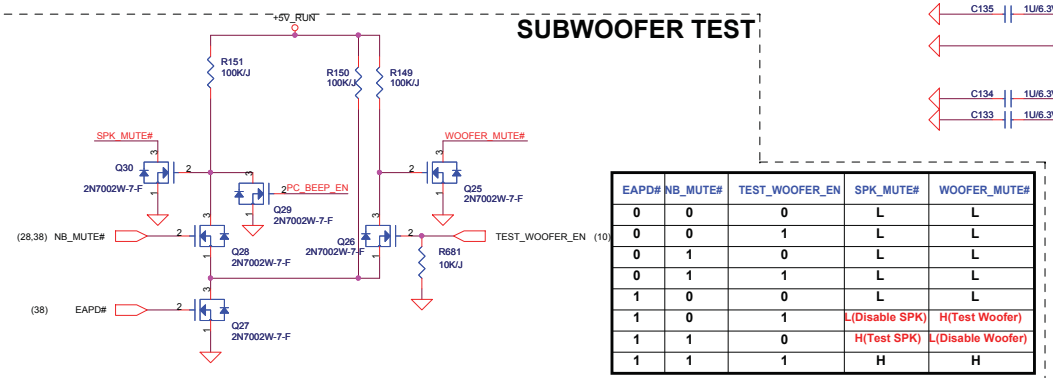
Main Speaker AMP



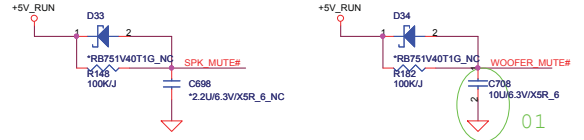
SUBWOOFER AMP



SUBWOOFER TEST



EAPD#	NB_MUTE#	TEST_WOOFER_EN	SPK_MUTE#	WOOFER_MUTE#
0	0	0	L	L
0	0	1	L	L
0	1	0	L	L
0	1	1	L	L
1	0	0	L	L
1	0	1	L(Disable SPK)	H(Test Woofer)
1	1	0	H(Test SPK)	L(Disable Woofer)
1	1	1	H	H

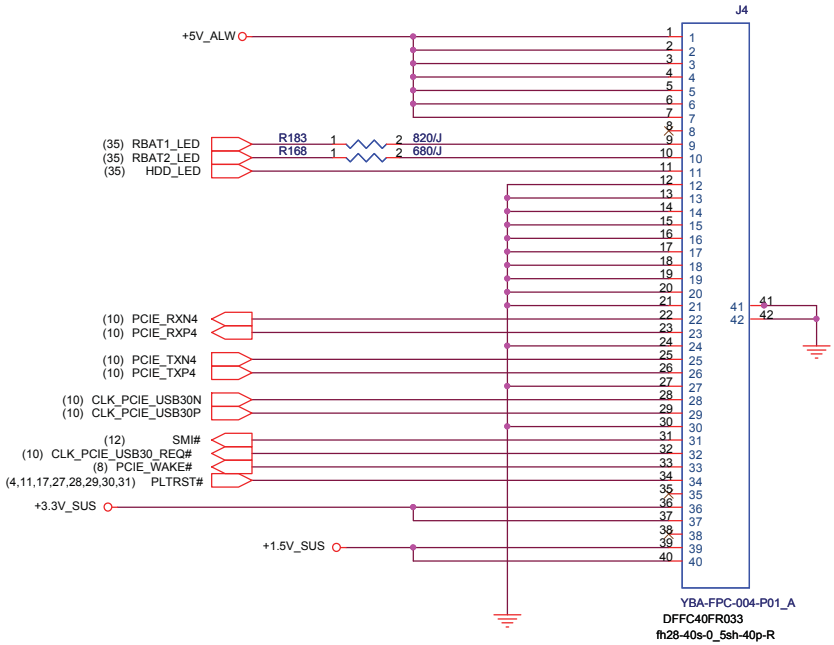


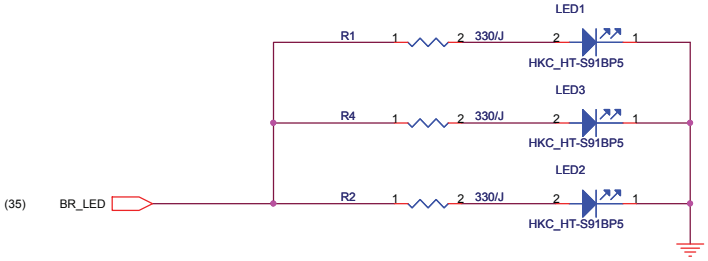
Quanta Computer Inc.

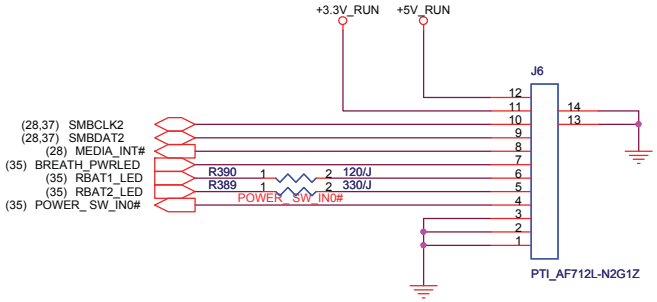
PROJECT : GM6C MLK DIS

Size	Document Number	Rev
	Audio AMP (MAX9736A)	1A
Date: Friday, January 07, 2011	Sheet 39 of 59	

01





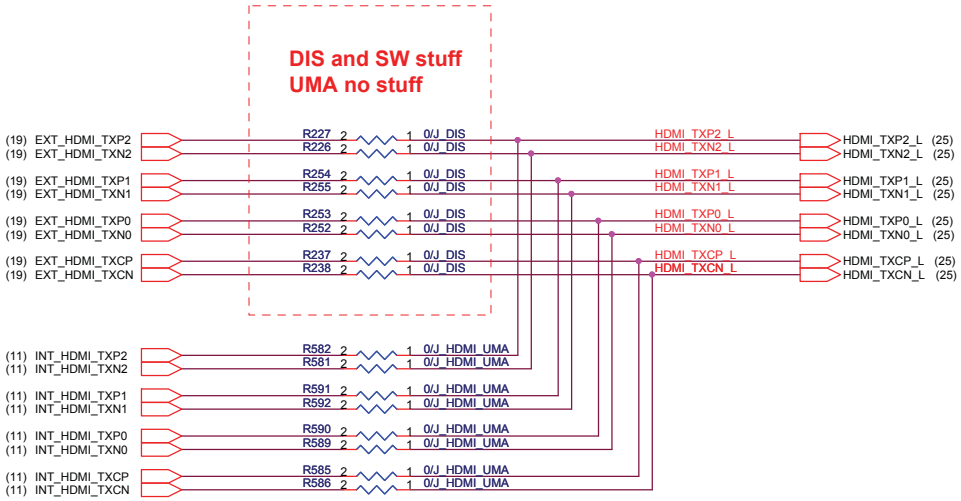


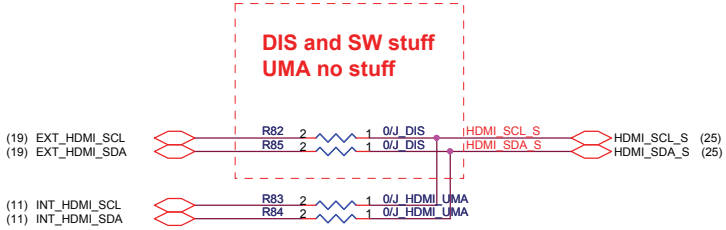
Quanta Computer Inc.

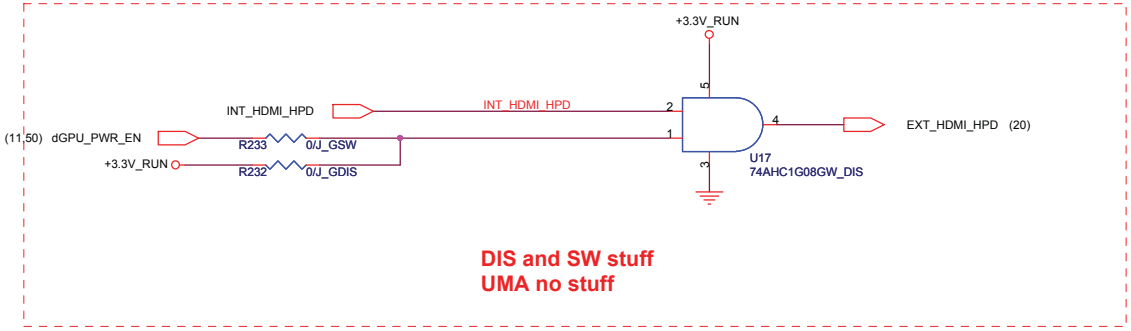
PROJECT : GM6C MLK DIS

Size	Document Number	Rev
	Left USB/MMB CONN	1A
Date: Friday, January 07, 2011	Sheet 40 of 59	

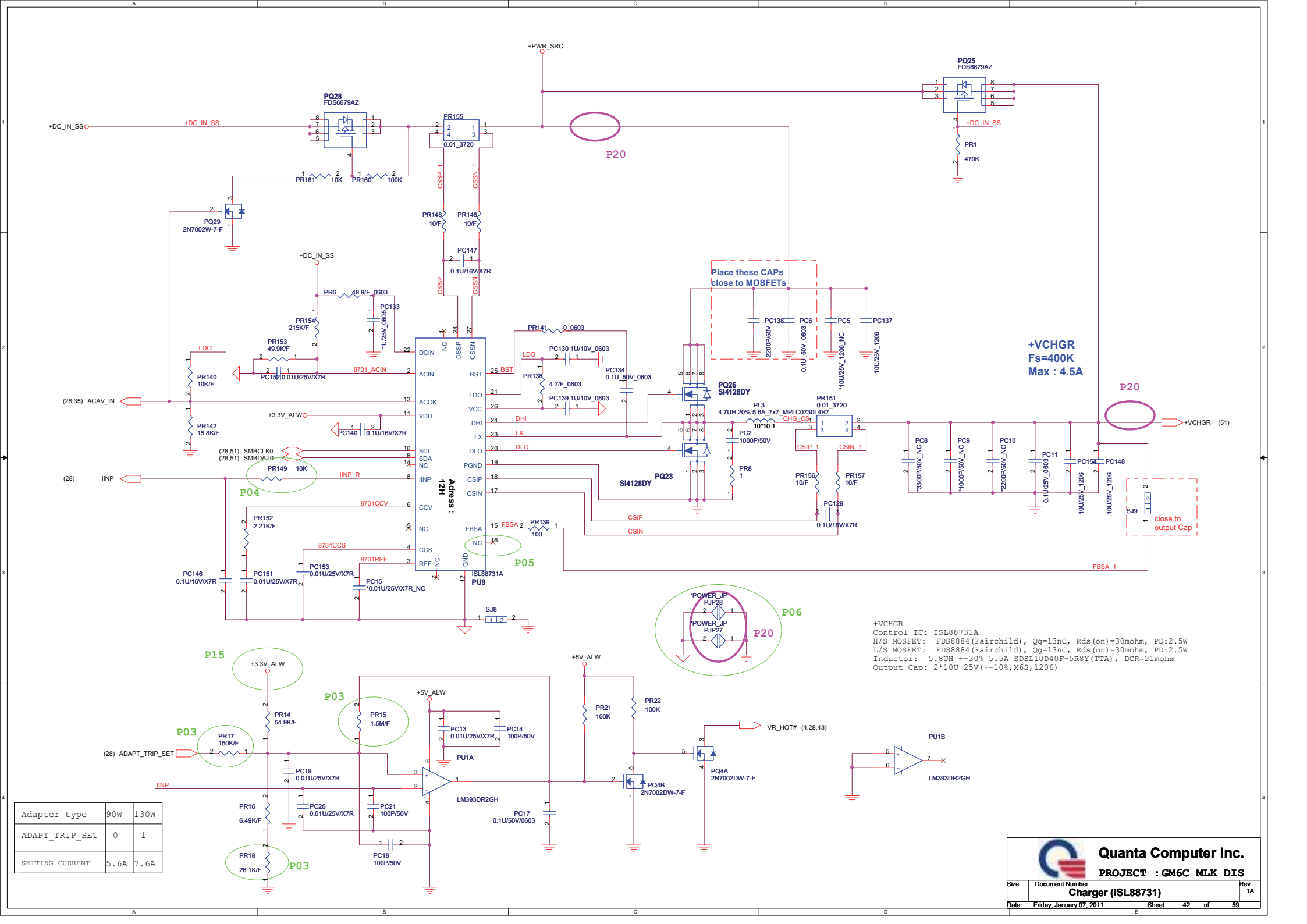
HDMI Switch







Quanta Computer Inc.		
PROJECT : GM6C MLK DIS		
Size	Document Number: BLANK	Rev: 1A
Date: Friday, January 07, 2011	Sheet 41 of 59	



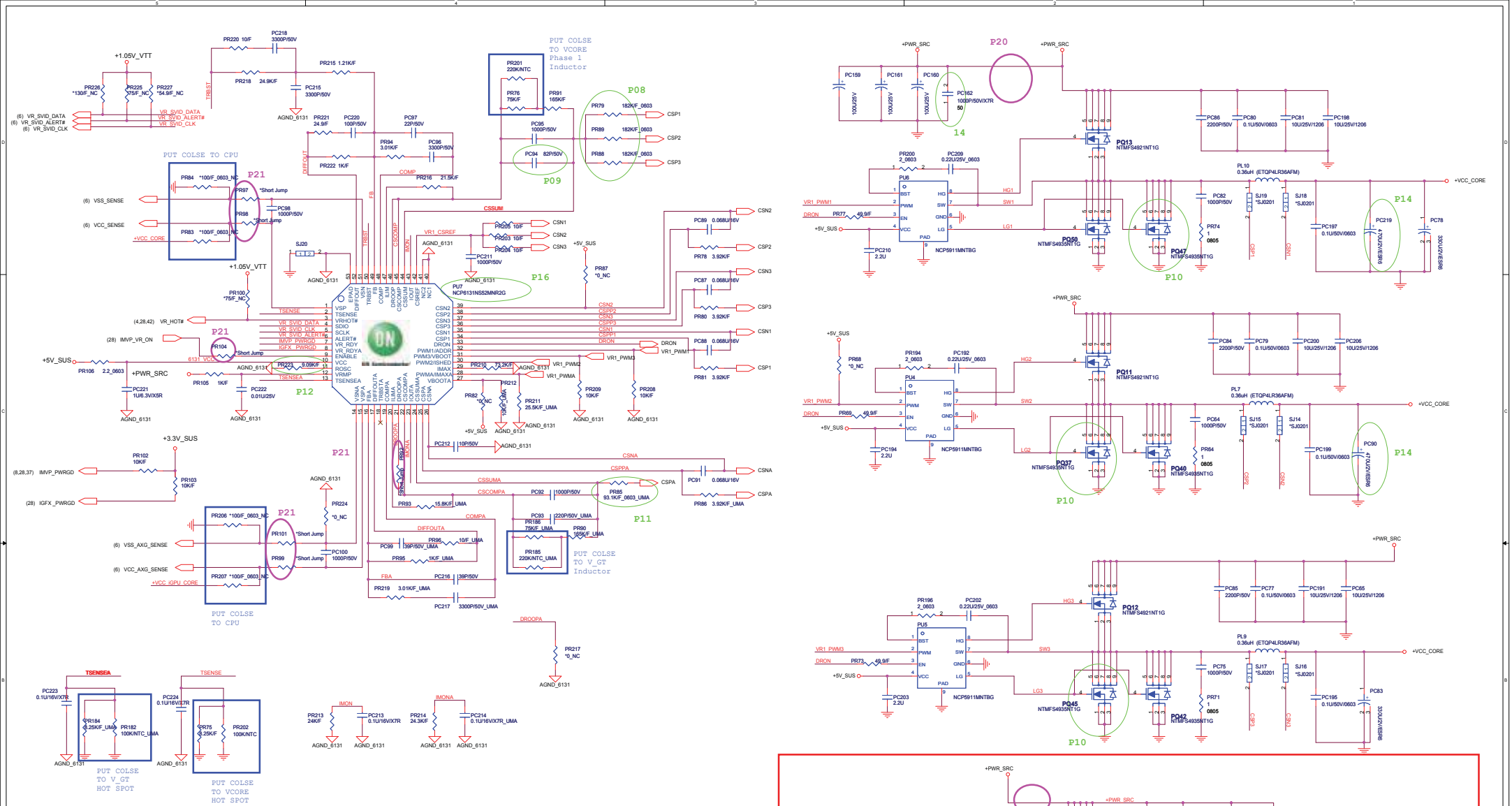
Adapter type	90W	130W
ADAPT_TRIP_SET	0	1
SETTING CURRENT	5.6A	7.6A

Quanta Computer Inc.

PROJECT : GM6C MLK DIS

Size	Document Number	Rev
	Charger (ISL88731)	1A

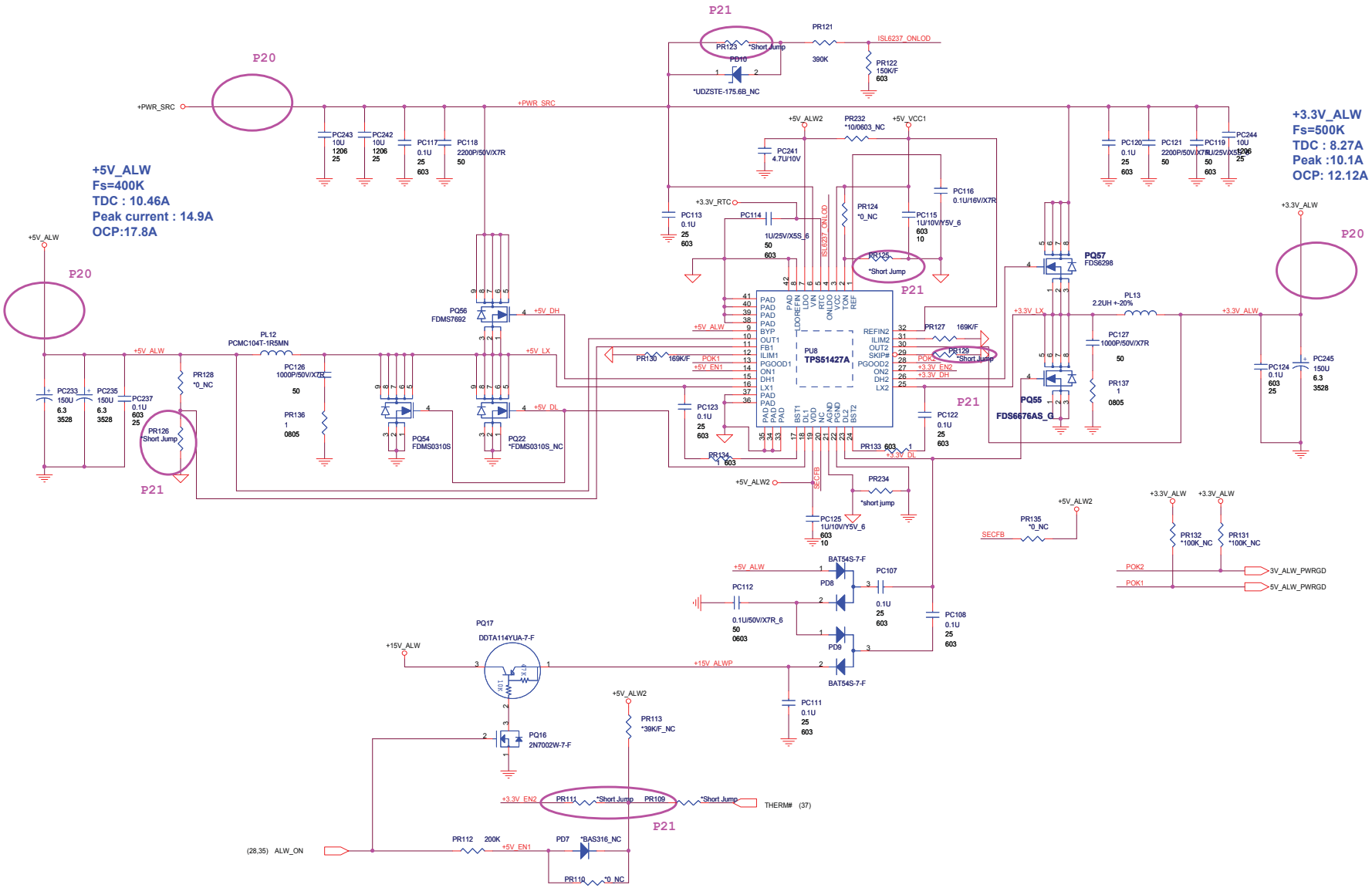
Date: Friday, January 07, 2011 Sheet 42 of 59



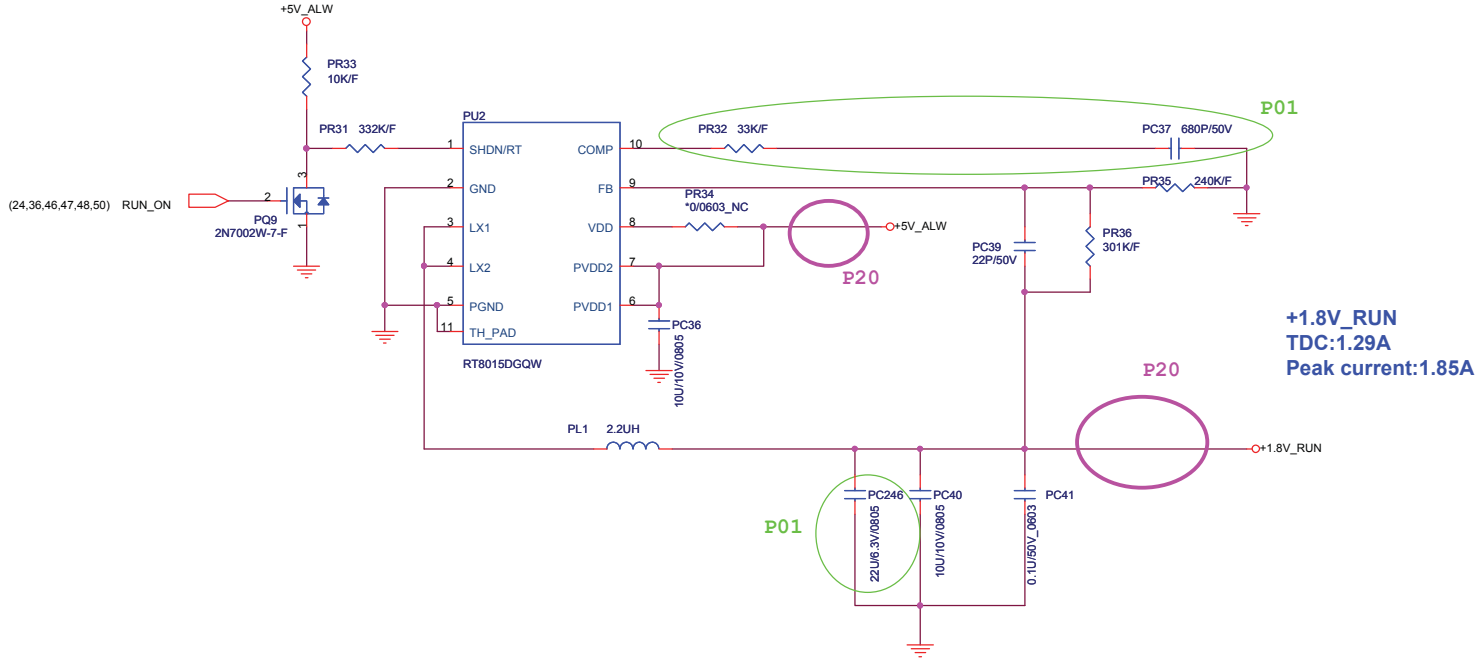
Reference	Discrete	UMA	Optimus
PR82	0(CS00002JB38)	NC	NC
PC91	0(CS00002JB38)	0.068U/16V(CH3683K1B09)	0.068U/16V(CH3683K1B09)
PC92	0(CS00002JB38)	1000P/50V(CH21006JB10)	1000P/50V(CH21006JB10)
PC212	0(CS00002JB38)	10P/50V(CH01006JB08)	10P/50V(CH01006JB08)
PR217	0(CS00002JB38)	NC	NC
PC216	0(CS00002JB38)	39P/50V(CH03906JB06)	39P/50V(CH03906JB06)
PC100	0(CS00002JB38)	1000P/50V(CH21006JB10)	1000P/50V(CH21006JB10)
PR224	0(CS00002JB38)	NC	NC
PR214	0(CS00002JB38)	24.3K/F(CS32432FB19)	24.3K/F(CS32432FB19)
PC223	0(CS00002JB38)	0.1U/10V(CH4102K1B03)	0.1U/10V(CH4102K1B03)

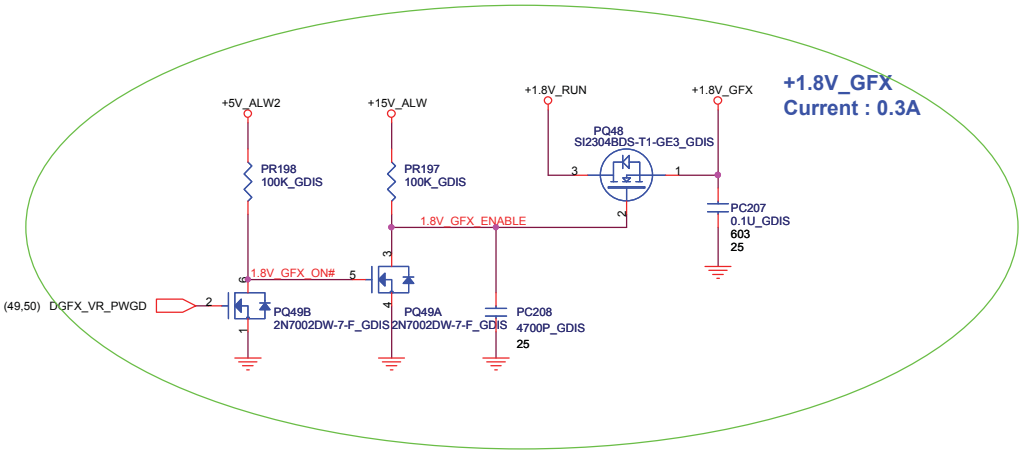
	UMA	Optimus
PC180, C612	470uF CH747RM8800	330uF CH733RM8831

Quanta Computer Inc.
PROJECT : GM6C MLK DIS
Size | Document Number: CPU_VCORE (NCP6131S) | Rev: 1A
Date: Friday, January 07, 2011 | Sheet 43 of 59

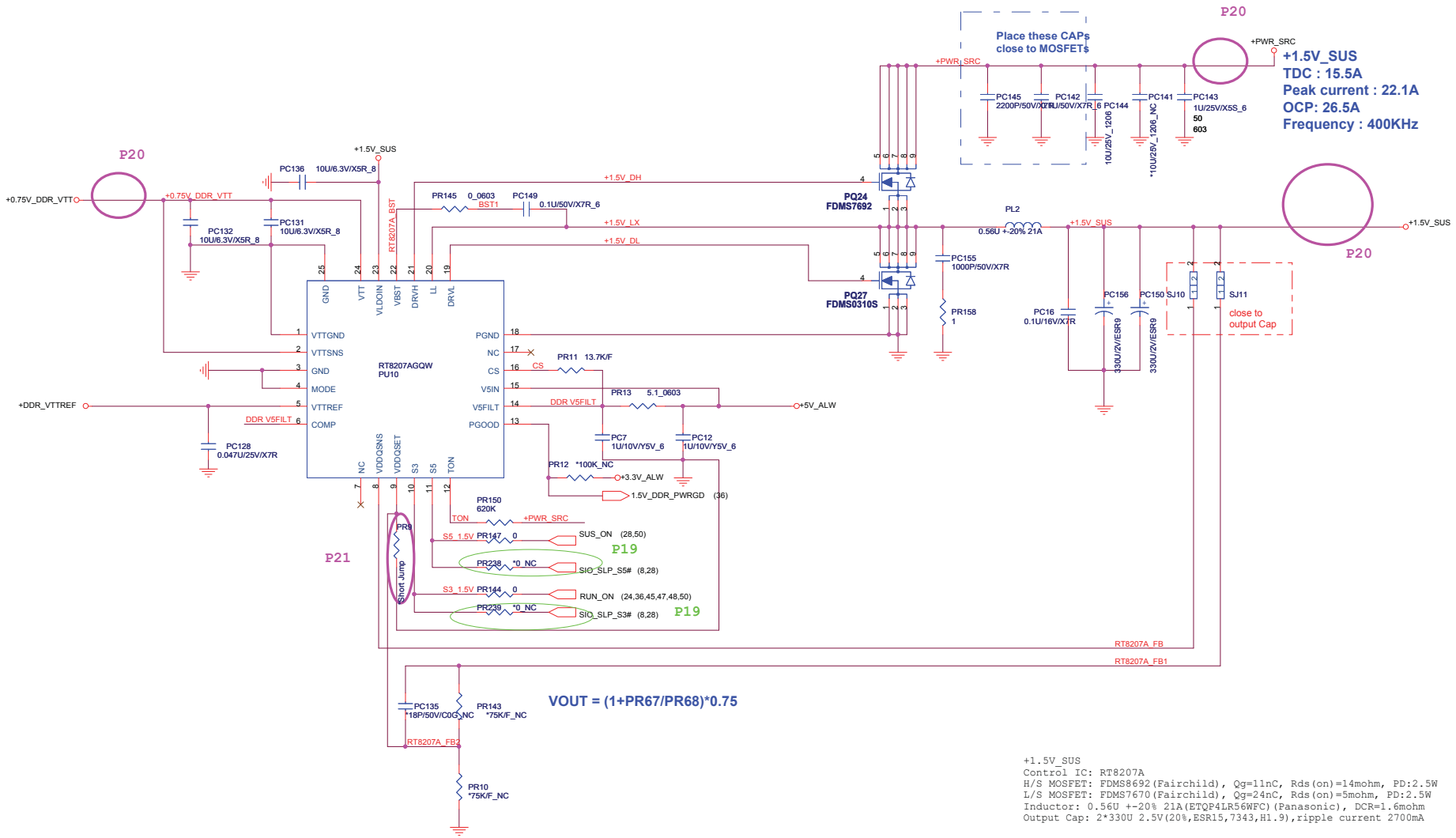


Quanta Computer Inc.			
PROJECT : GM6C MLK DIS			
Size	Document Number		Rev
	3.3V_ALW / 5V_ALW(TPS51427A)		1A
Date: Friday, January 07, 2011	Sheet 44 of 59		





Quanta Computer Inc.		
PROJECT : GM6C MLK DIS		
Size	Document Number: 1.8V_RUN & 1.8V_RUN_GFX	Rev: 1A
Date: Friday, January 07, 2011	Sheet 45 of 59	



+1.5V_SUS
Control IC: RT8207A
H/S MOSFET: FDMS8692(Fairchild), Qg=11nC, Rds(on)=14mohm, PD:2.5W
L/S MOSFET: FDMS7670(Fairchild), Qg=24nC, Rds(on)=5mohm, PD:2.5W
Inductor: 0.56U +-20% 21A(ETQP4LR56WFC)(Panasonic), DCR=1.6mohm
Output Cap: 2*330U 2.5V(20%,ESR15,7343,H1.9),ripple current 2700mA

VDDQ and VTT discharge control

MODE pin	Discharge mode
V5IN	No discharge
VDDQ	Tracking discharge
S4/GND	Non-tracking discharge

VDDQ output voltage selection

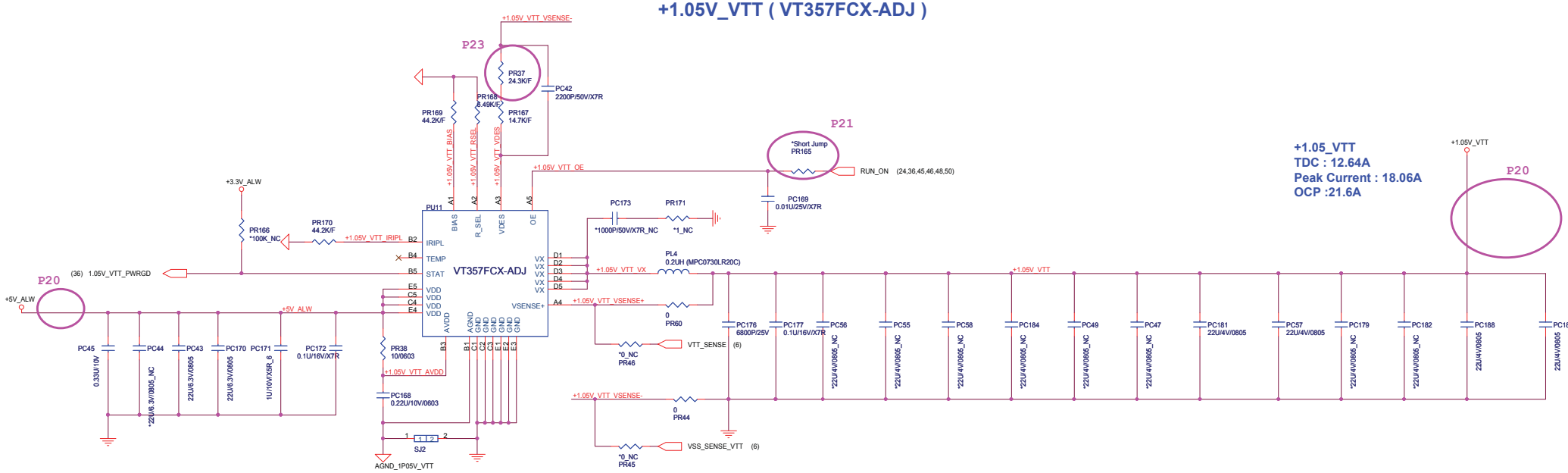
VDDQSET	VDDQ(V)	VTTREF and VTT	NOTE
GND	1.5V	VDDQSNS/2	DDR3
V5IN	1.8V	VDDQSNS/2	DDR2
FB Resistors	Adjusting	VDDQSNS/2	1.5V < VVDDQ < 3V

Outputs Management by S3, S5 control

State	S3	S5	VDDQ	VTTREF	VTT
S0	HI	HI	On	On	On
S3	LO	HI	On	On	Off (Hi-Z)
S4/S5	LO	LO	On (discharge)	Off (discharge)	Off (discharge)

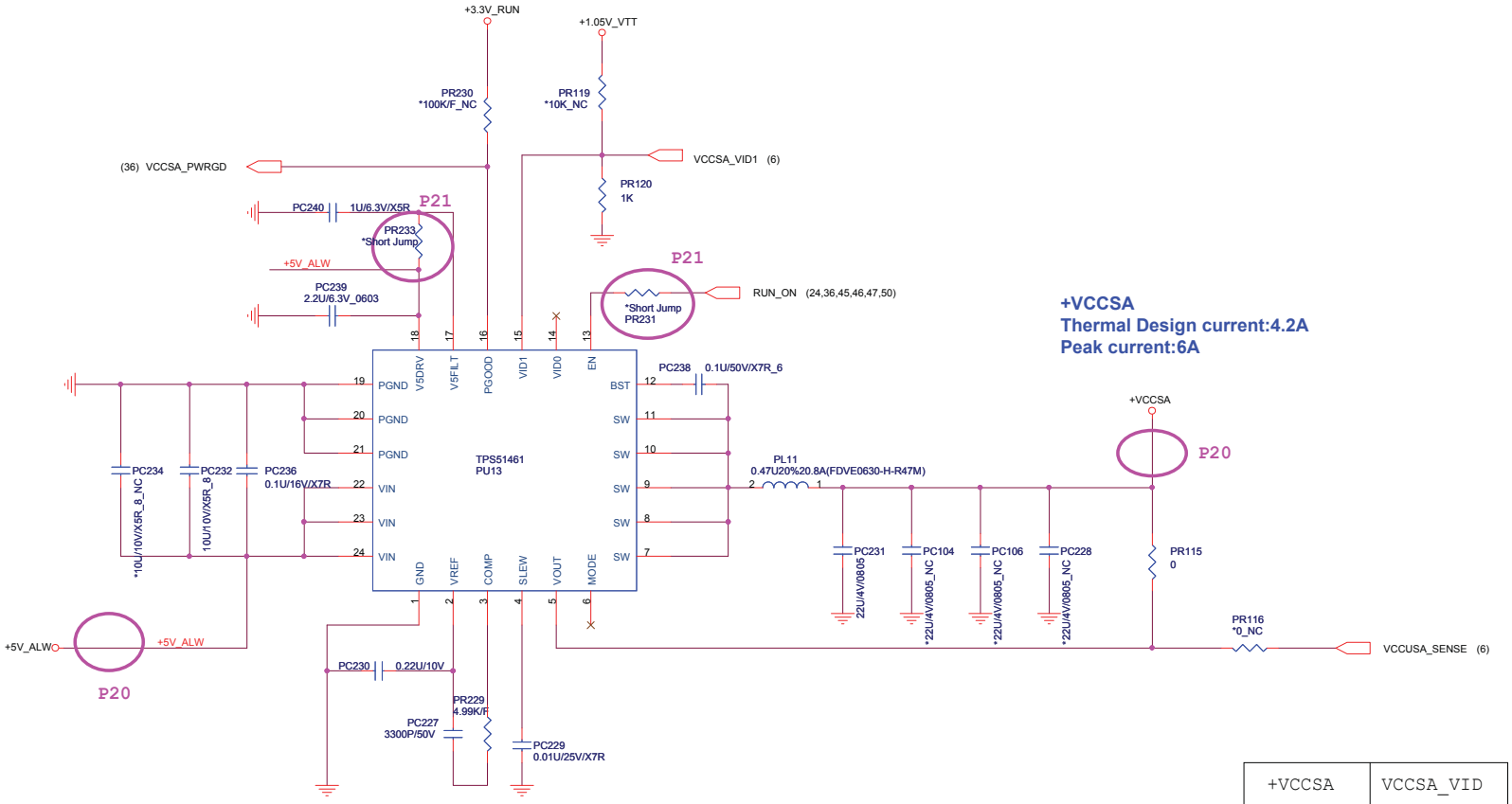
Quanta Computer Inc.
PROJECT : GM6C MLK DIS
Size | Document Number: 1.5V_SUS & 0.75_DDR_VTT (RT8207) | Rev: 1A
Date: Friday, January 07, 2011 | Sheet 46 of 59

+1.05V_VTT (VT357FCX-ADJ)



Route +1.05V_VTT_VSENSE+ and +1.05V_VTT_VSENSE-
as differential pair

Quanta Computer Inc.		
PROJECT : GM6C MLK DIS		
Size	Document Number: 1.05V_VTT	Rev: 1A
Date: Friday, January 07, 2011	Sheet 47 of 59	



+VCCSA	VCCSA_VID
0.8V	High
0.9V	Low

Quanta Computer Inc.

PROJECT : GM6C MLK DIS

Size	Document Number	Rev
	VCCSA (TPS51461)	1A

Date: Friday, January 07, 2011 Sheet 48 of 59

N12P-GE:

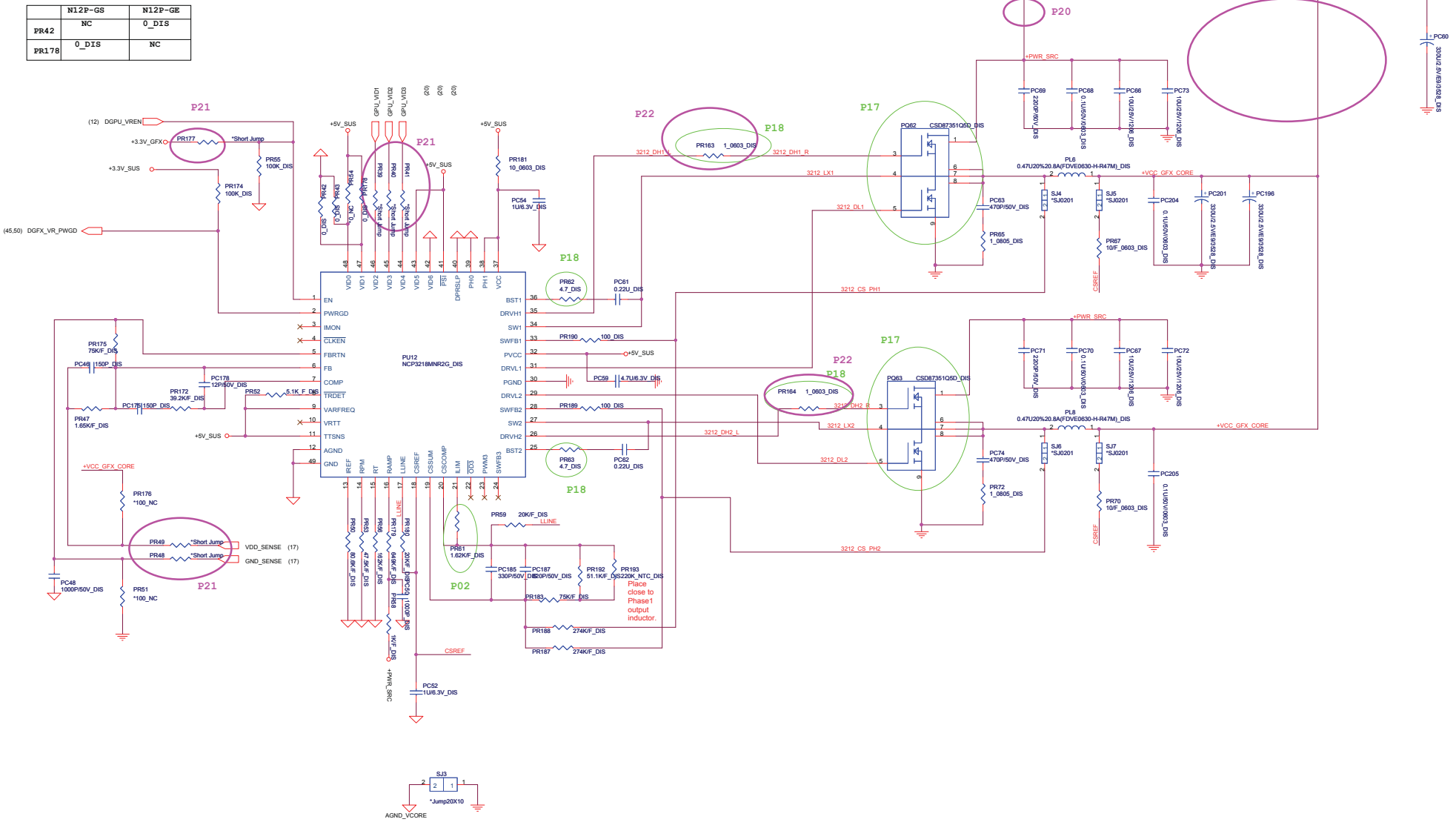
	GPU_VID3	GPU_VID2	GPU_VID1
0.85V	1	0	1
0.95V	0	1	1
1.0V	0	1	0

N12P-GS:

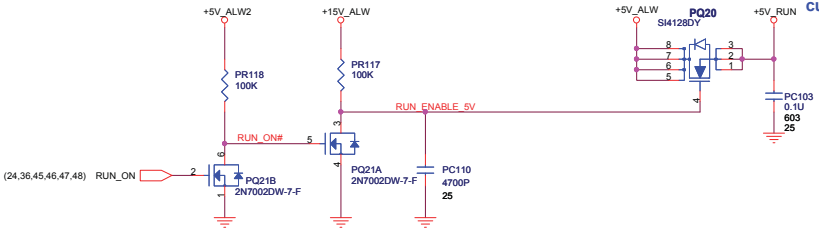
	GPU_VID3	GPU_VID2	GPU_VID1
0.825V	1	0	1
0.975V	0	1	0
1.0V	0	0	1

	N12P-GS	N12P-GE
PR42	NC	0_DIS
PR178	0_DIS	NC

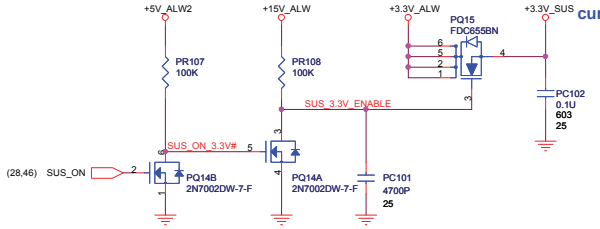
+VCC_GFX_CORE
Fs=300K
Current:21.81A
OCP:52A



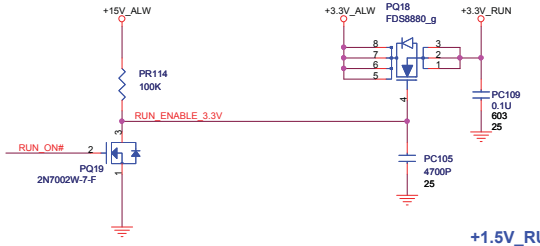
+5V_RUN
current : 2.52A



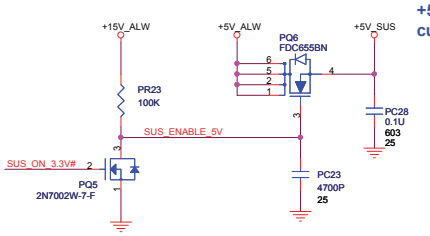
+3.3V_SUS
current : 0.35A



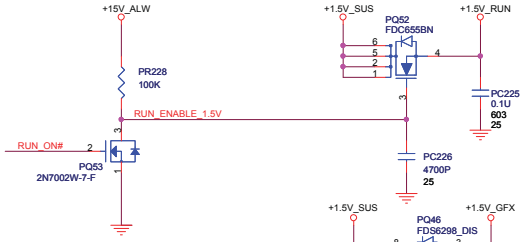
+3.3V_RUN
current : 5.12A



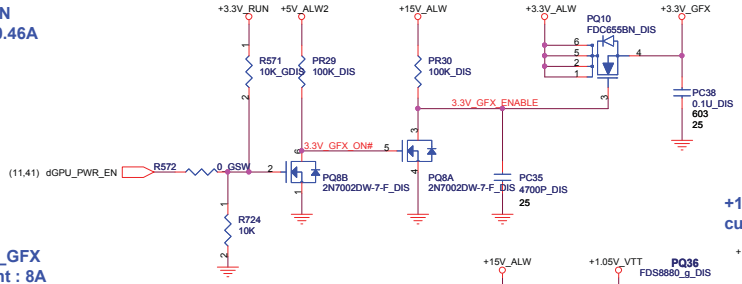
+5V_SUS
current : 2.1A



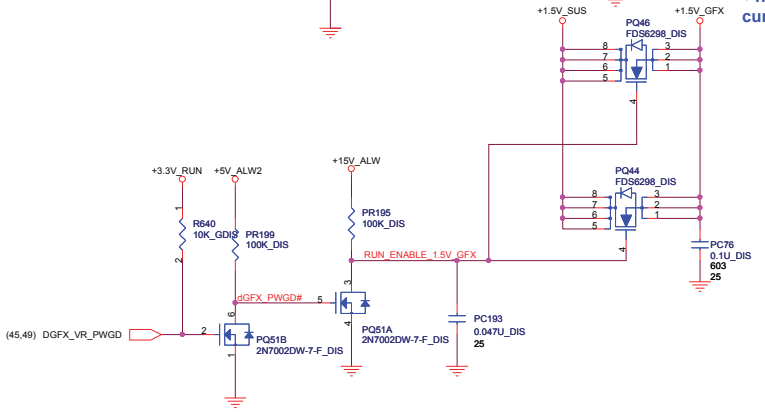
+1.5V_RUN
current : 0.46A



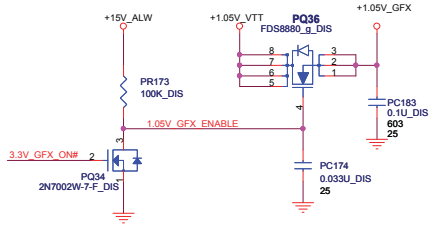
+3.3V_GFX
current: 1.38A



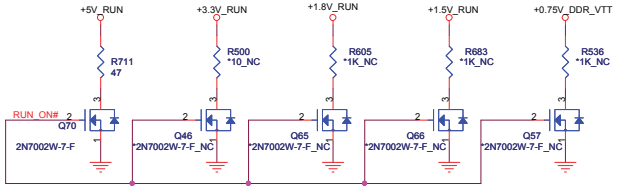
+1.5V_GFX
current : 8A

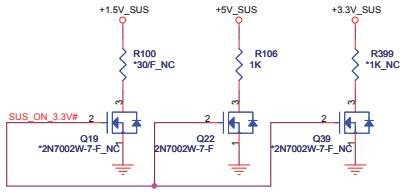


+1.05V_GFX
current : 3.83A



Reserve discharge path

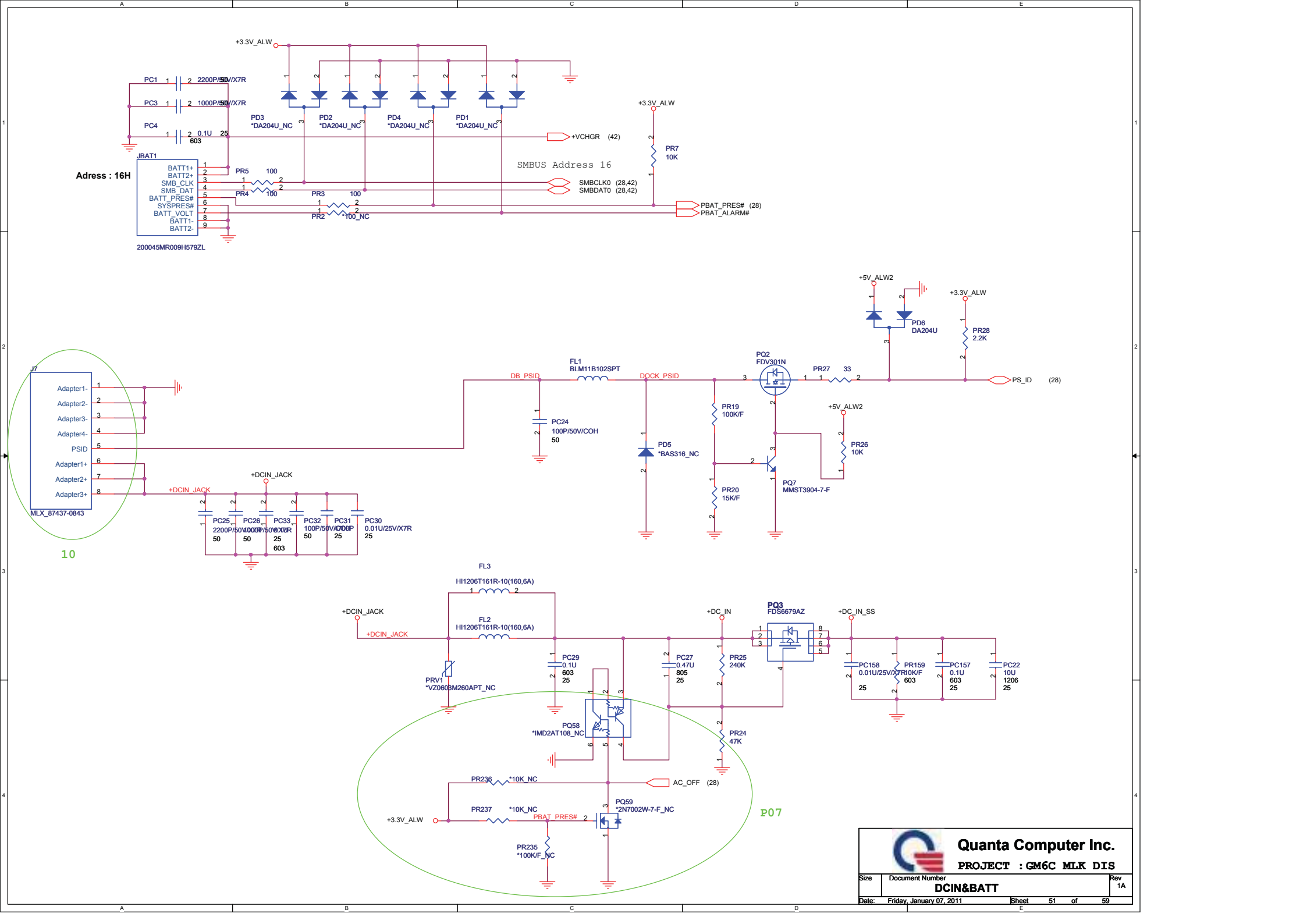


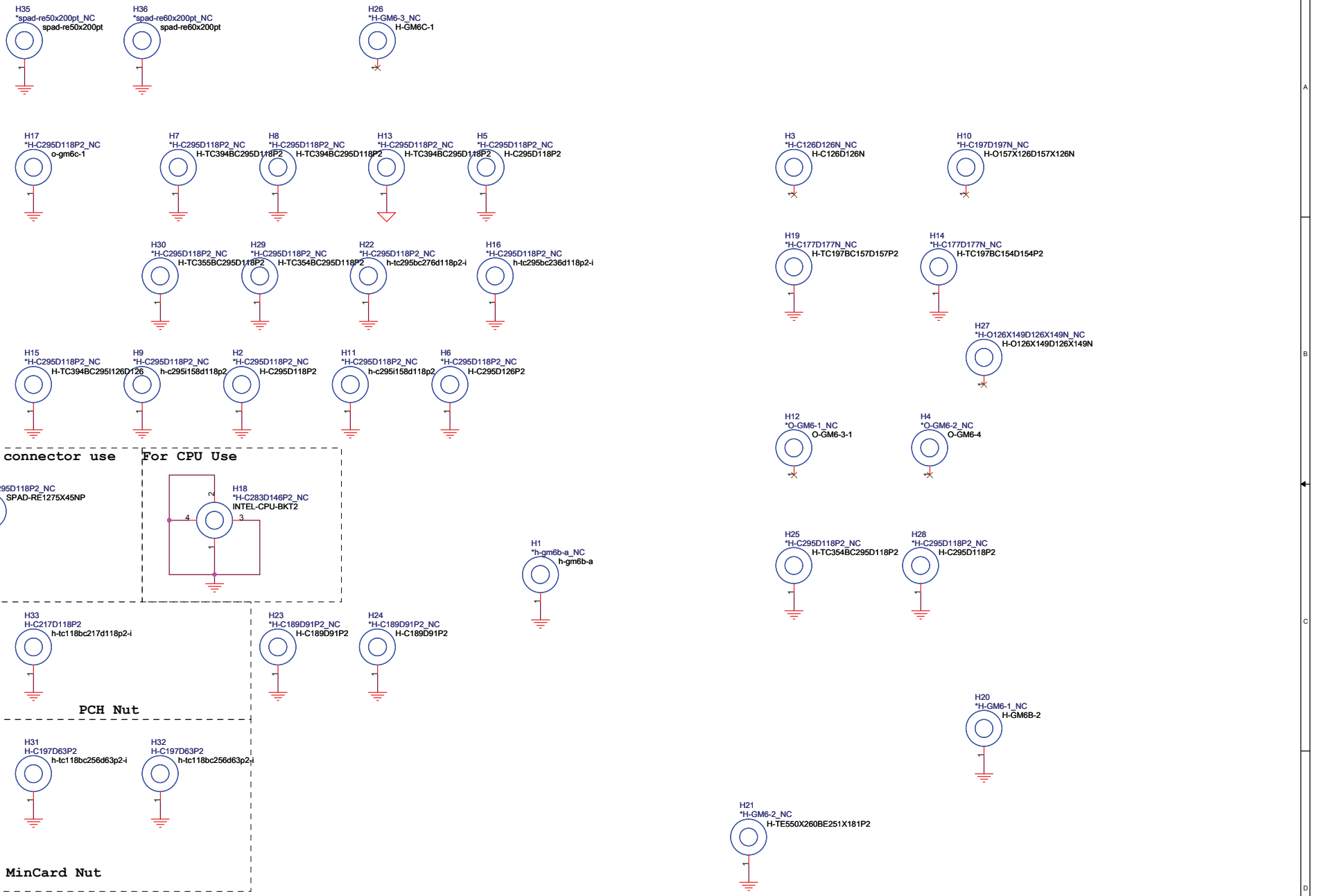


Quanta Computer Inc.

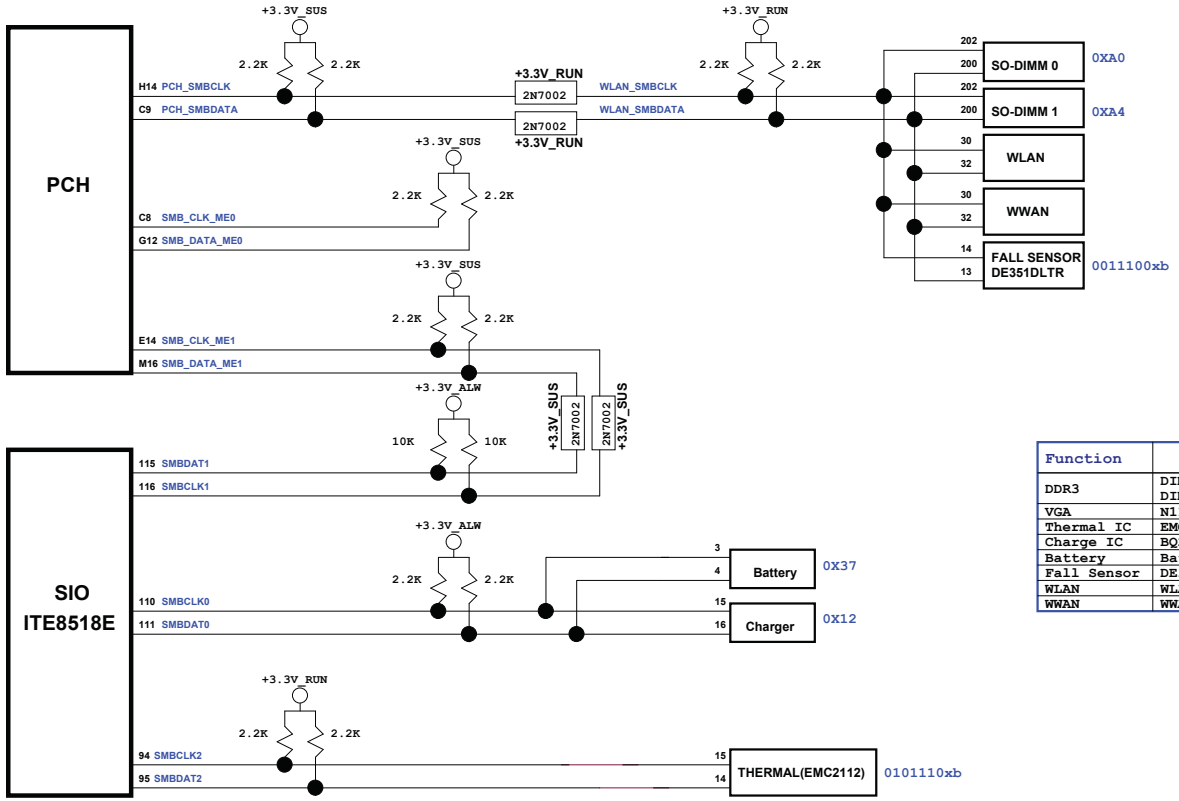
PROJECT : GM6C MLK DIS

Size	Document Number	Rev
	Run Power Switch	1A
Date: Friday, January 07, 2011	Sheet 50 of 59	


+3.3V_ALW
PC1 2200P/50V/X7R
PC3 1000P/50V/X7R
PC4 0.1U 25 603
PD3 *DA204U_NC
PD2 *DA204U_NC
PD4 *DA204U_NC
PD1 *DA204U_NC
+VCHGR (42)
JBAT1
Adress : 16H
BATT1+
BATT2+
SMB_CLK
SMB_DAT
BATT_PRES#
SYSPRES#
BATT_VOLT
BATT1-
BATT2-
PR5 100
PR4 100
PR3 100
PR2 *100_NC
SMBUS Address 16
SMBCLK0 (28,42)
SMBDAT0 (28,42)
PR7 10K
PBAT_PRES# (28)
PBAT_ALARM#
200045MR009H579ZL
+5V_ALW2
PD6 DA204U
PR28 2.2K
J7
Adapter1-
Adapter2-
Adapter3-
Adapter4-
PSID
Adapter1+
Adapter2+
Adapter3+
MLX_87437-0843
DB_PSID
FL1 BLM11B102SPT
DOCK_PSID
PQ2 FDV301N
PR27 33
PS_ID (28)
PC24 100P/50V/COH 50
PD5 *BAS316_NC
PR19 100K/F
PR20 15K/F
PQ7 MMST3904-7-F
PR26 10K
+DCIN_JACK
PC25 2200P/50V/X7R 50
PC26 1000P/50V/X7R 50
PC33 0.1U/25V/X7R 25 603
PC32 100P/50V/COH 50
PC31 470P 25
PC30 0.01U/25V/X7R 25
10
FL3 HI1206T161R-10(160,6A)
FL2 HI1206T161R-10(160,6A)
PRV1 *VZ0603M260APT_NC
PC29 0.1U 603 25
PC27 0.47U 805 25
PQ58 *IMD2AT108_NC
PR25 240K
PQ3 FDS6679AZ
+DC_IN
+DC_IN_SS
PC158 0.01U/25V/X7R 25
PR159 10K/F 603
PC157 0.1U 603 25
PC22 10U 1206 25
PR24 47K
PR236 *10K_NC
AC_OFF (28)
PR237 *10K_NC
PBAT_PRES#
PQ59 *2N7002W-7-F_NC
PR235 *100K/F_NC
P07
Quanta Computer Inc.
PROJECT : GM6C MLK DIS
Size
Document Number
DCIN&BATT
Rev 1A
Date: Friday, January 07, 2011
Sheet 51 of 59

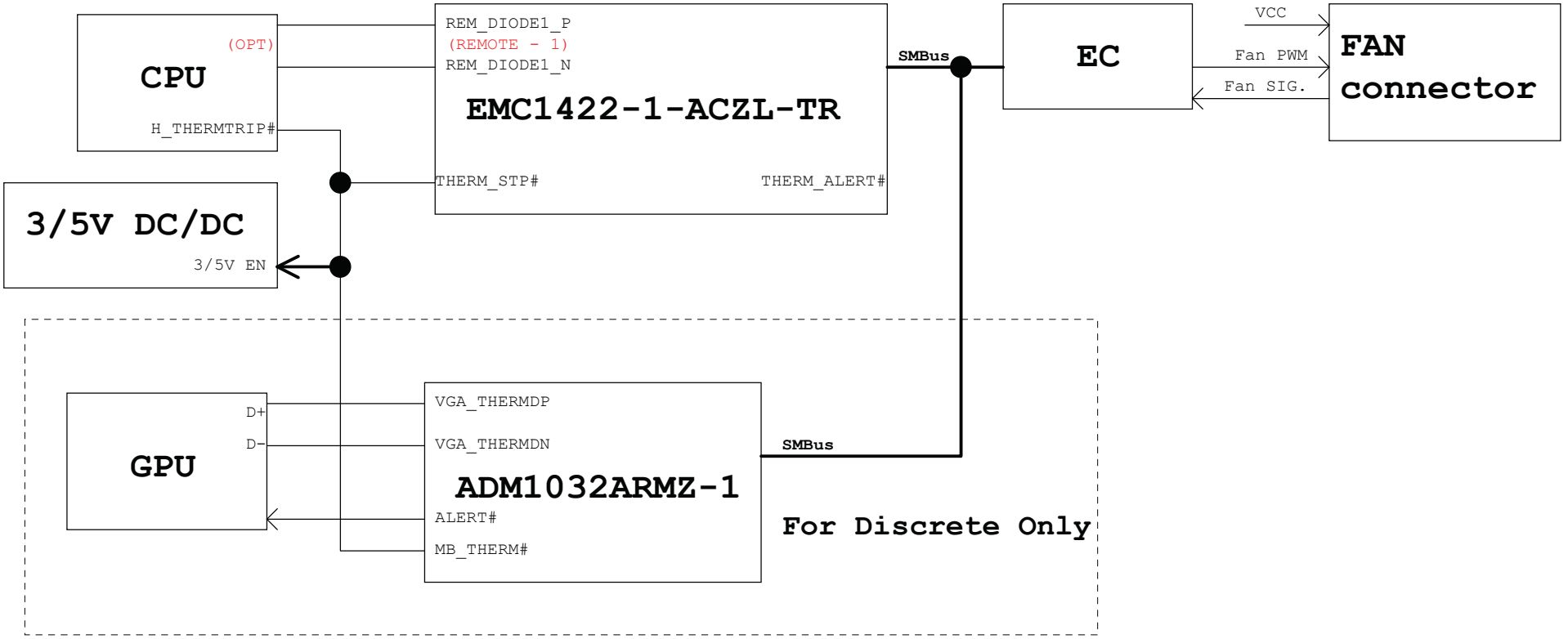


Quanta Computer Inc.		
PROJECT : GM6C MLK DIS		
Size	Document Number: PAD & SCREW	Rev: 1A
Date: Friday, January 07, 2011	Sheet 52 of 59	



Function	IC	SMBus Address
DDR3	DIMM0 DIMM1	A0 A4
VGA	N11P	9E
Thermal IC	EMC2112	0011100xb
Charge IC	BQ24765RUVR	0x12
Battery	Battery	0X37
Fall Sensor	DE351DLTR	0101110xb
WLAN	WLAN Module	X
WWAN	WWAN Module	X

Quanta Computer Inc.
PROJECT : GM6C MLK DIS
Size | Document Number: SMBUS | Rev: 1A
Date: Friday, January 07, 2011 Sheet 53 of 59



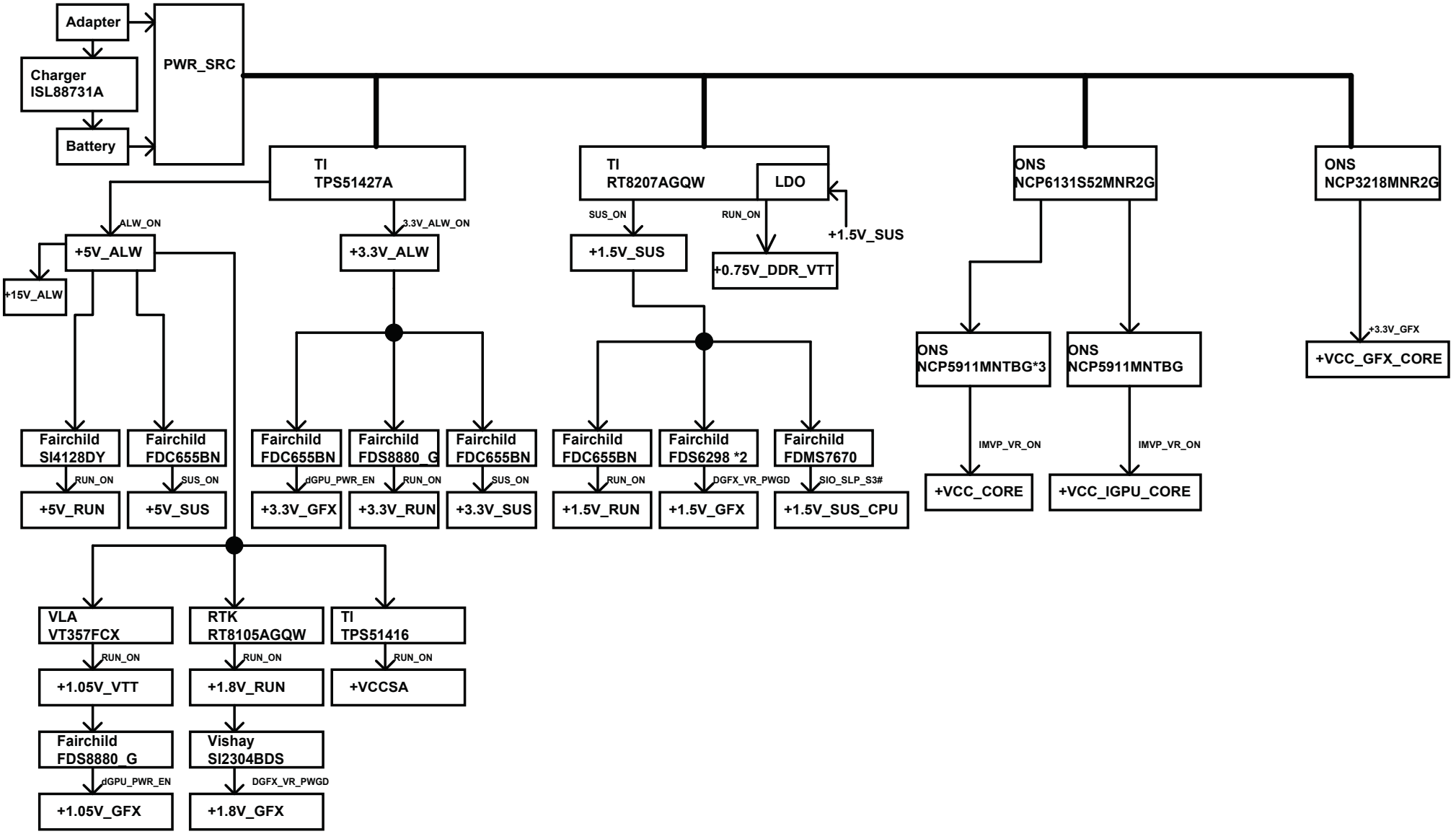
Quanta Computer Inc.

PROJECT : GM6C MLK DIS

Size	Document Number	Rev
	THERMAL MAP	1A

Date: Friday, January 07, 2011 Sheet 54 of 59

VER : 1A



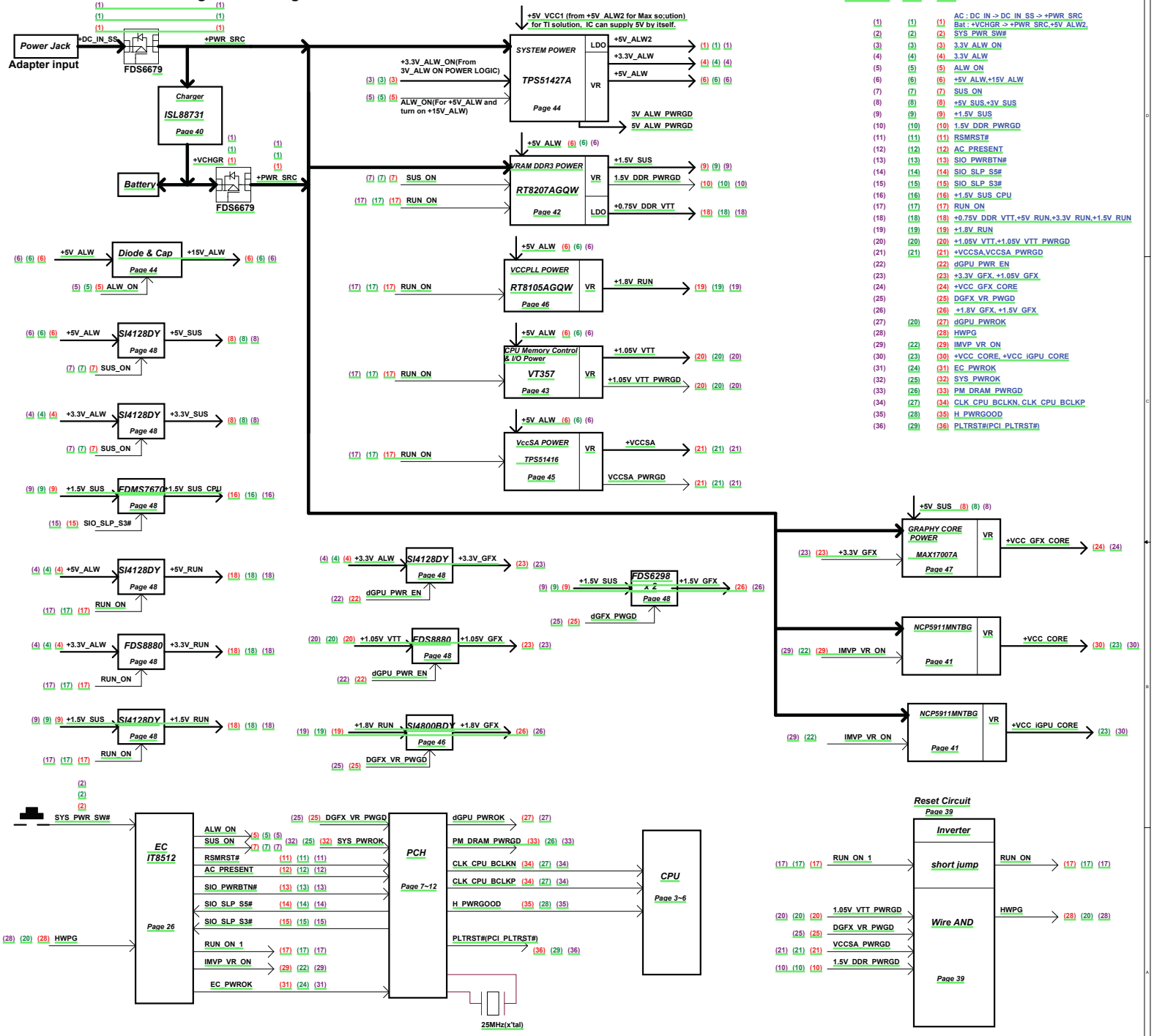
Quanta Computer Inc.

PROJECT : GM6C MLK DIS

Size	Document Number	Rev
	Power Block Diagram	1A

Date: Friday, January 07, 2011 Sheet 55 of 59

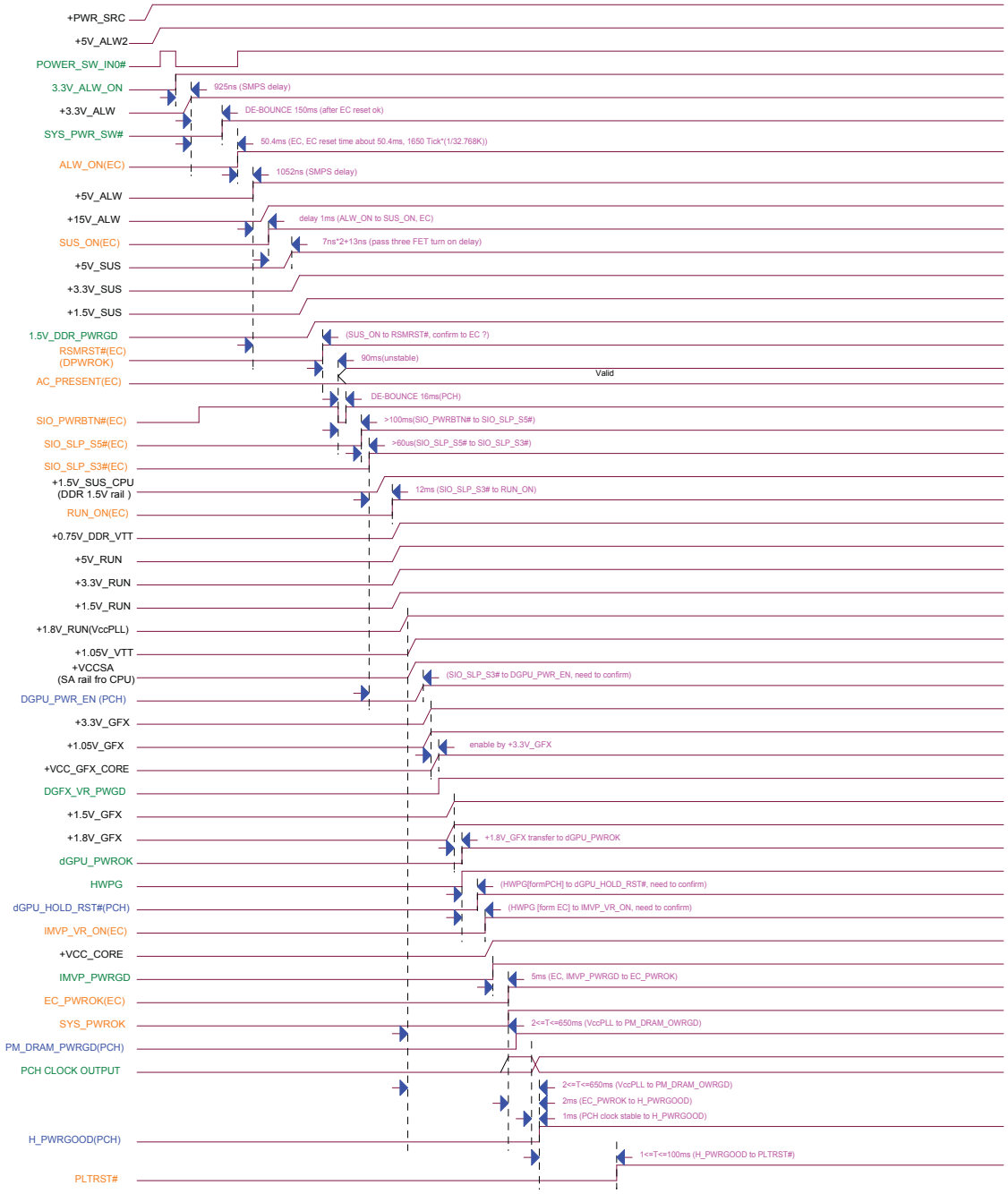
GM6C-MLK Power Design Block Diagram



OPTIMUS	UMA	DIS	
(1)	(1)	(1)	AC : DC_IN -> DC_IN_SS -> +PWR_SRC Bat : +VCHGR -> +PWR_SRC,+5V_ALW2,
(2)	(2)	(2)	SYS_PWR_SW#
(3)	(3)	(3)	3.3V_ALW_ON
(4)	(4)	(4)	3.3V_ALW
(5)	(5)	(5)	ALW_ON
(6)	(6)	(6)	+5V_ALW,+15V_ALW
(7)	(7)	(7)	SUS_ON
(8)	(8)	(8)	+5V_SUS,+3V_SUS
(9)	(9)	(9)	+1.5V_SUS
(10)	(10)	(10)	1.5V_DDR_PWRGD
(11)	(11)	(11)	RSMRST#
(12)	(12)	(12)	AC_PRESENT
(13)	(13)	(13)	SIO_PWRBTN#
(14)	(14)	(14)	SIO_SLP_S5#
(15)	(15)	(15)	SIO_SLP_S3#
(16)	(16)	(16)	+1.5V_SUS_CPU
(17)	(17)	(17)	RUN_ON
(18)	(18)	(18)	+0.75V_DDR_VTT,+5V_RUN,+3.3V_RUN,+1.5V_RUN
(19)	(19)	(19)	+1.8V_RUN
(20)	(20)	(20)	+1.05V_VTT,+1.05V_VTT_PWRGD
(21)	(21)	(21)	+VCCSA,VCCSA_PWRGD
(22)		(22)	dGPU_PWR_EN
(23)		(23)	+3.3V_GFX, +1.05V_GFX
(24)		(24)	+VCC_GFX_CORE
(25)		(25)	DGFX_VR_PWGD
(26)		(26)	+1.8V_GFX, +1.5V_GFX
(27)	(20)	(27)	dGPU_PWROK
(28)		(28)	HWPG
(29)	(22)	(29)	IMVP_VR_ON
(30)	(23)	(30)	+VCC_CORE, +VCC_iGPU_CORE
(31)	(24)	(31)	EC_PWROK
(32)	(25)	(32)	SYS_PWROK
(33)	(26)	(33)	PM_DRAM_PWRGD
(34)	(27)	(34)	CLK_CPU_BCLKN, CLK_CPU_BCLKP
(35)	(28)	(35)	H_PWRGOOD
(36)	(29)	(36)	PLTRST#(PCI_PLTRST#)

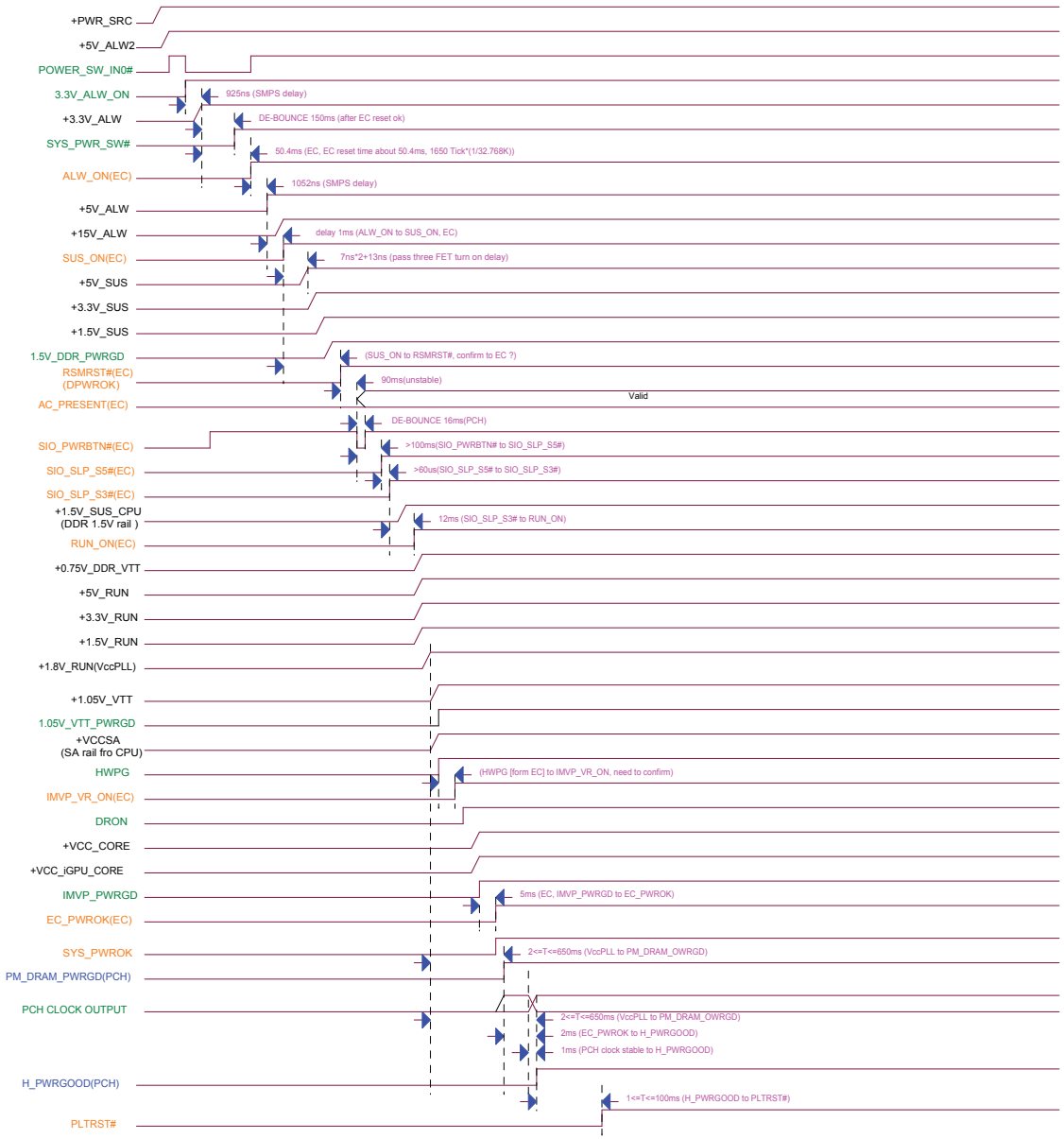
Quanta Computer Inc.			
PROJECT : GM6C_MLK_DIS			
Size	Document Number		Rev
	Power sequence Block		1A
Date: Friday, January 07, 2011		Sheet 56 of 59	

GM6C_MLK_DIS Power on Timing(BATTERY MODE)



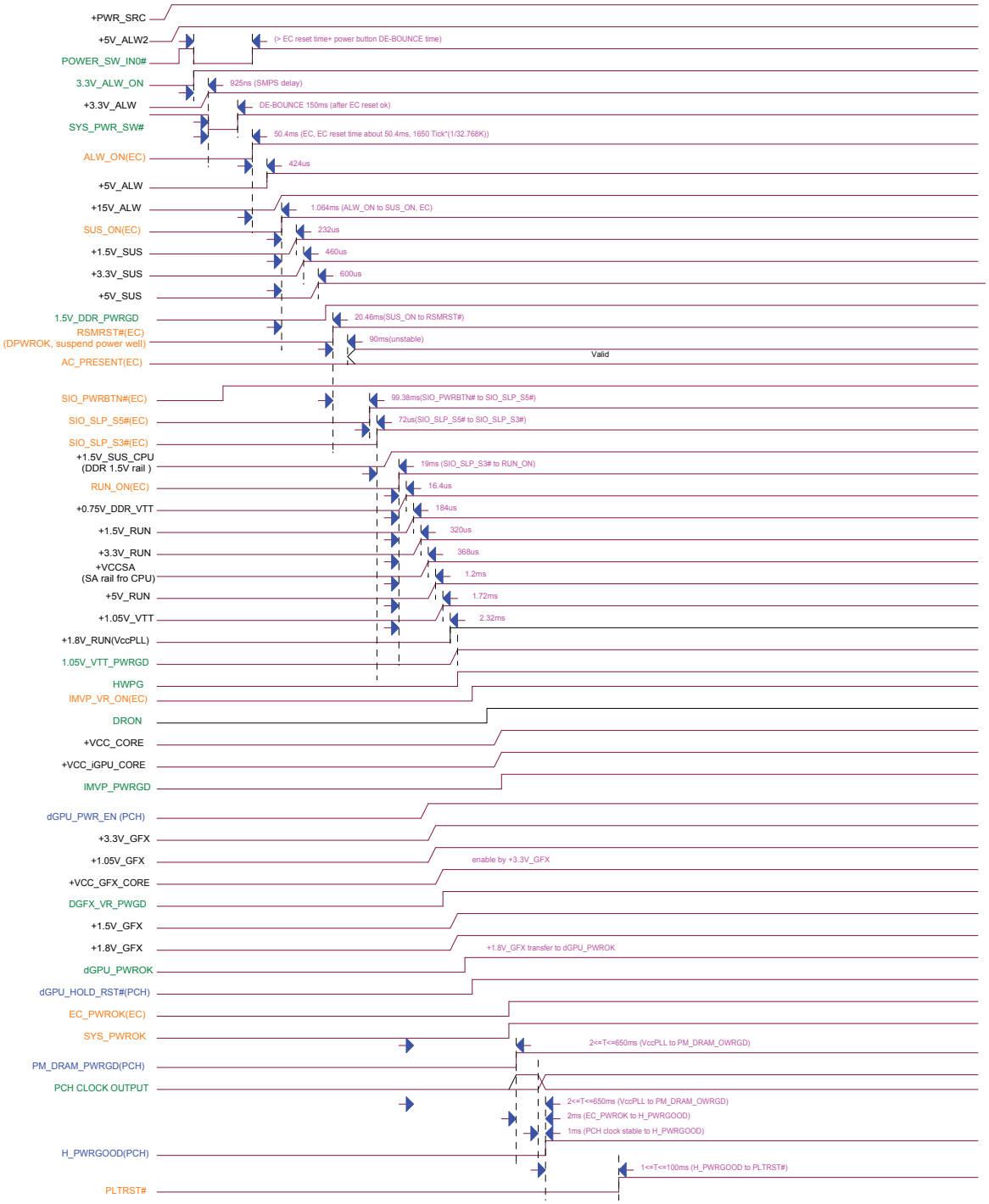
Quanta Computer Inc.		
PROJECT : GM6C MLK DIS		
Size	Document Number: POWER SEQUENCE(DIS)	Rev: 1A
Date: Friday, January 07, 2011	Sheet 57 of 59	

GM6C_MLK_UMA Power on Timing(BATTERY MODE)



Quanta Computer Inc.		
PROJECT : GM6C MLK DIS		
Size	Document Number: POWER SEQUENCE(UMA)	Rev: 1A
Date: Friday, January 07, 2011	Sheet 58 of 59	

GM6C_MLK_OPTIMUS Power on Timing(BATTERY MODE)



Quanta Computer Inc.

PROJECT : GM6C MLK DIS

Size	Document Number	Rev
	POWER SEQUENCE(OPTIMUS)	1A
Date: Friday, January 07, 2011	Sheet 59 of 59	