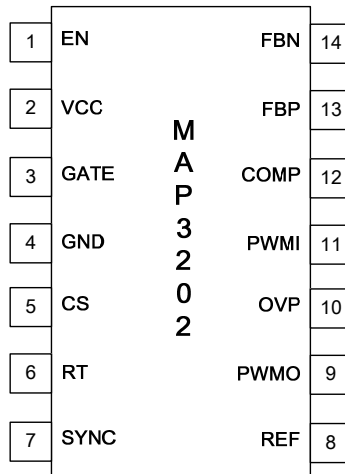
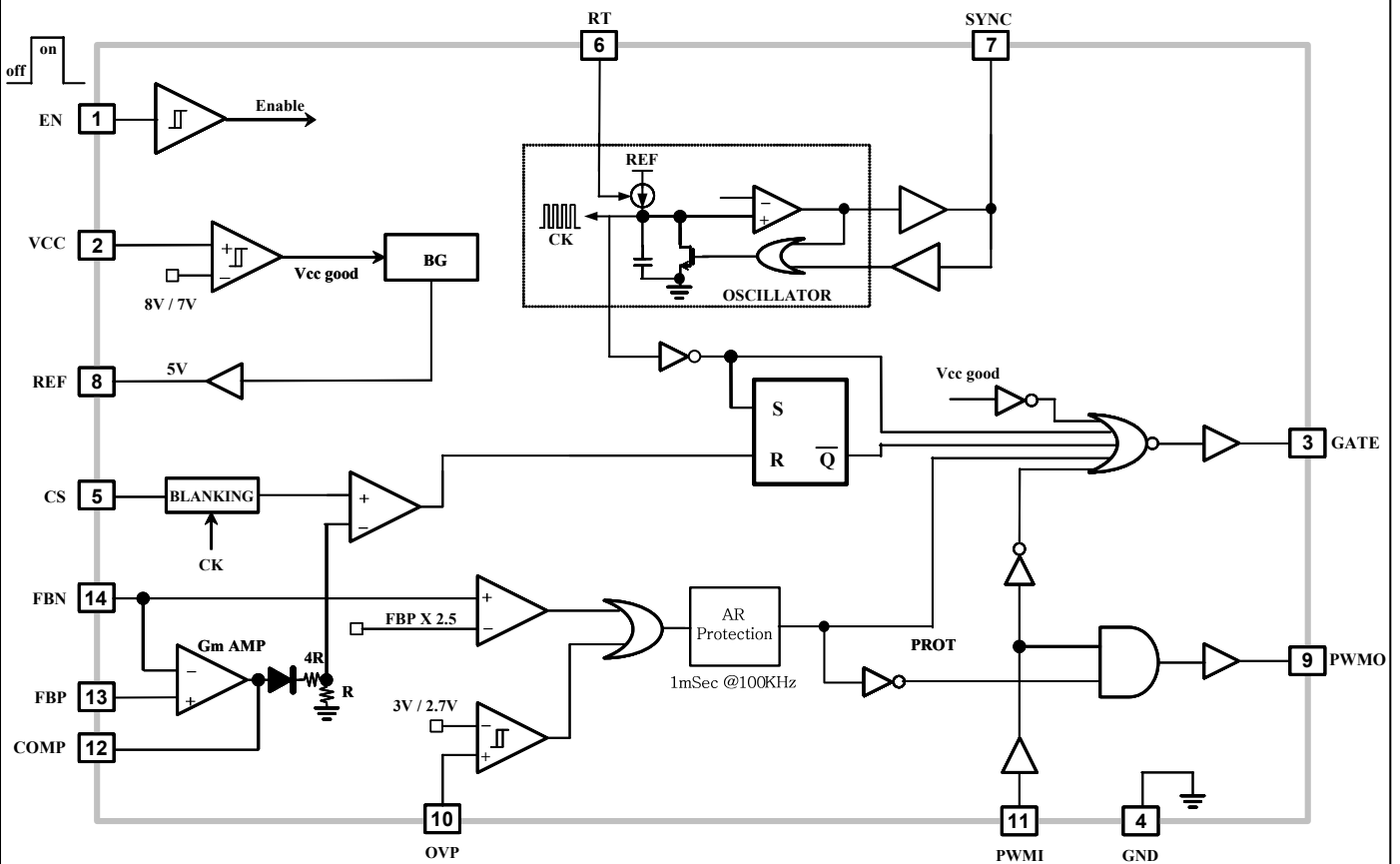


Pin Configuration



Functional Block Diagram



Pin Description

PIN NO	Description	
1	EN	Enable
2	VCC	Power Supply Input
3	GATE	Gate Drive Output for Boost Converter
4	GND	GND
5	CS	Current Sense of Boost Converter
6	RT	Oscillators Frequency Set
7	SYNC	Oscillators Synchronizing Input
8	REF	Reference Voltage
9	PWMO	PWM Gate Driver Output
10	OVP	Over Voltage Protection
11	PWMI	PWM Gate Driver Input
12	COMP	Error AMP. Compensation
13	FBP	Error AMP. Non-inverting Input/Positive Current Sense
14	FBN	Error AMP. Inverting Input/Negative Current Sense

Absolute Maximum Ratings (1)

PARAMETER	VALUE	UNIT
VCC	-0.3 ~ 20	V
GATE, PWMO	-0.3 ~ 20	V
EN, CS, RT, SYNC, REF, OVP, PWMI, COMP, FBP, FBN	-0.3 ~ 6.0	V
Operating Junction Temperature Range	-40 ~ 150	°C
Storage Temperature Range	-65 ~ 150	°C
Lead temperature(soldering, 10sec)	260	°C
Thermal Resistance (θ_{JA})	110	°C/W

Note1: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

$V_{CC}=12V$, $V_{P\text{WMI}}=5V$, $T_a=25^\circ\text{C}$, unless otherwise specified

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
SUPPLY						
$V_{CC,OP}$	Input voltage range	$T_a=-40^\circ\text{C} \sim 85^\circ\text{C}$	8.5	-	18	V
I_Q	Operation quiescent current	$V_{P\text{WMI}}=0V$	-	1.2	2	mA
V_{UVLO}	Under-voltage lockout threshold	-	7.5	8	8.5	V
	Under-voltage lockout hysteresis	-	-	1	-	V
REFERENCE						
V_{REF}	Reference pin voltage	$T_a=-40^\circ\text{C} \sim 85^\circ\text{C}$	4.90	5.00	5.10	V
		$T_a=25^\circ\text{C}$	4.95	5.00	5.05	V
V_{REFLI}	Line regulation	$I_{REF}=0\mu\text{A}$, $V_{P\text{WMI}}=0V$, $C_{REF}=0.1\mu\text{F}$	-	-	0.02	%/V
V_{REFLO}	Load regulation	$I_{REF}=0\sim 500\mu\text{A}$, $V_{P\text{WMI}}=0V$, $C_{REF}=0.1\mu\text{F}$	-	-	1	%/mA
GATE						
I_{SOURCE}	Gate short circuit current	$V_{GATE}=0$, $V_{CC}=12V$	0.4	-	-	A
I_{SINK}	Gate sink current	$V_{GATE}=12V$, $V_{CC}=12V$	0.8	-	-	A
T_{RISE}	GATE output rise time	$C_{GATE}=1nF$, $V_{CC}=12V$	-	50	85	ns
T_{FALL}	GATE output fall time	$C_{GATE}=1nF$, $V_{CC}=12V$	-	25	45	ns
Enable						
V_{EN}	Enable input voltage	$V_{EN,L}$: Logic Low	-	-	0.4	V
		$V_{EN,H}$: Logic High	2.0	-	5.5	V
Current Sense						
T_{BLANK}	Leading Edge Blanking	-	100	-	375	ns
T_{DELAY}	Delay to output of CS comparator (3)	$V_{COMP}=5V$, $V_{CS}=0V$ to 600mV step	-	-	180	ns
$V_{CS,MAX}$	Maximum CS Voltage	$F_{BP} - F_{BN} \geq 0.2V$	0.325	0.36	0.395	V
Internal Transconductance Opamp						
A_V	Open loop DC Gain	Output open	-	50	-	dB
V_{CM}	Input common-mode range (3)	-	-0.3	-	2.2	V
V_O	Output Voltage Low Limit	$V_{CC}=12V$, $V_{FBN} - V_{FBP} > 0.2$	-	0.6	-	V
	Output Voltage High Limit	$V_{CC}=12V$, $V_{FBP} - V_{FBN} > 0.2$	-	2.6	-	V
G_m	Transconductance (3)	-	400	670	1000	$\mu\text{A/V}$

Electrical Characteristics (continued)V_{CC}=12V, V_{PWMI}=5V, Ta=25°C, unless otherwise specified

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Internal Transconductance Opamp						
I _{BIAS}	Input Bias current	-	-	0.5	1	nA
V _{OFFSET}	Input Offset voltage	-	-5	-	5	mV
I _{AMP_SOURCE}	AMP Source Current	V _{FBN} =1V, V _{FBP} =2V, V _{COMP} =1.5V	-	-100	-	uA
I _{AMP_SINK}	AMP Sink Current	V _{FBN} =2V, V _{FBP} =1V, V _{COMP} =1.5V	-	100	-	uA
Oscillator						
F _{OSC}	Oscillator frequency (100KHz ~ 400KHz)	Ta=-40°C ~ 85°C, RT=500kΩ	90	100	110	kHz
		Ta=25°C, RT=500kΩ	95	100	105	kHz
		Ta=-40°C ~ 85°C, RT=123kΩ	340	400	460	kHz
D _{MAX}	Maximum duty cycle	-	-	90	-	%
Synchronizing (External Input)						
V _{IL_SYNC}	SYNC Input voltage Low level	-	-	-	0.8	V
V _{IH_SYNC}	SYNC Input voltage high level	-	2	-	5.5	V
T _{SYNC_MIN}	SYNC minimum input pulse width(3)	V _{SYNC} = 0V to 5V	20	-	-	ns
T _{SYNC_MAX}	SYNC maximum input pulse width	V _{SYNC} = 0V to 5V	-	-	0.05 /fosc	ns
PWM Input						
V _{PWMI(LO)}	PWMI input low voltage	Ta=-40°C ~ 85°C	-	-	0.8	V
V _{PWMI(HI)}	PWMI input high voltage	Ta=-40°C ~ 85°C	2.0	-	5.5	V
R _{PWMI}	PWMI pull-down resistance	V _{PWMI} =5V	50	100	150	kΩ
PWM Output						
T _{RISE,PWMO}	PWM Output rise time	1nF capacitance at PWMO	-	-	300	ns
T _{FALL,PWMO}	PWM Output fall time	1nF capacitance at PWMO	-	-	200	ns
Auto Restart Protection (AUTO)						
T _{AR}	Auto Restart Time	F _{OSC} = 100KHz	-	1	-	ms
Over Voltage Protection (OVP)						
V _{OVP}	Over voltage protection	-	2.94	3.0	3.06	V
V _{OVPH}	Over voltage protection hysteresis		-	0.3	-	V
T _{OVP}	OVP Filtering time(3)		-	200	-	ns

Electrical Characteristics (continued)

$V_{CC}=12V$, $V_{P\text{WMI}}=5V$, $T_a=25^\circ\text{C}$, unless otherwise specified

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Short Current Protection (SCP)						
$V_{\text{TH,SCP}}$	SCP Comparator threshold voltage	$V_{\text{FBP}} = 1V$ ($V_{\text{TH,SCP}} = V_{\text{FBP}} * 2.5$)	2.25	2.5	2.75	V
T_{OFF}	Propagation time for short current detection	$V_{\text{FBP}}=1V$, $V_{\text{FBN}}=2.0$ to $3.0V$ step V_{PWMO} goes from high to low	-	-	250	ns

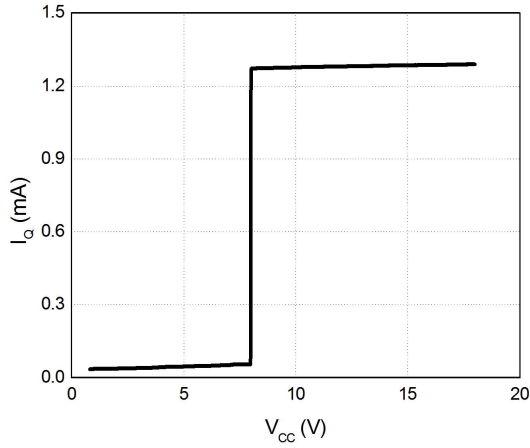
Note2: Stress beyond the maximum ratings listed above may incur permanent damage to the device. Operating above the recommended conditions for extended time may stress the device and affect device reliability. Also the device may not operate normally above the recommended operating conditions. These are stress ratings only.

Note3: These parameters, although guaranteed by design, are not tested in mass production.

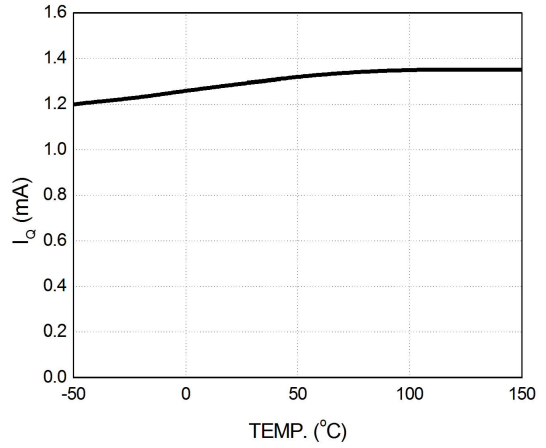
Typical Operating Characteristics

Unless otherwise noted, $V_{CC} = 12V$, $V_{PWM} = 5V$, and $T_a = 25^\circ C$.

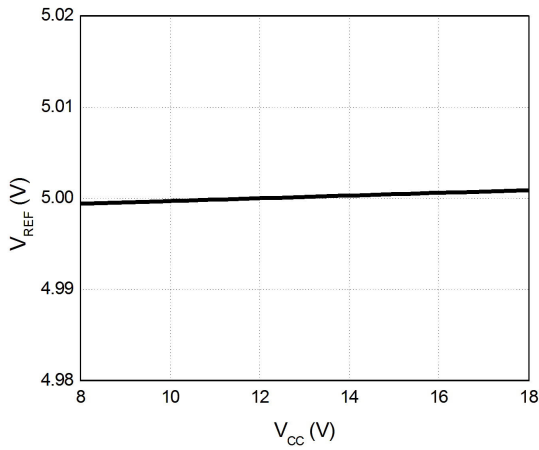
Quiescent Current vs. Vcc



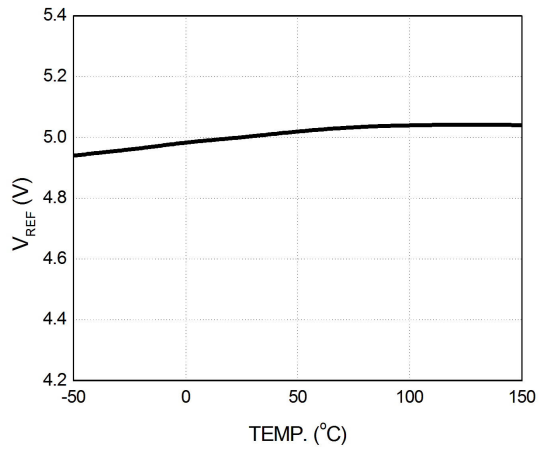
Quiescent Current vs. Temp



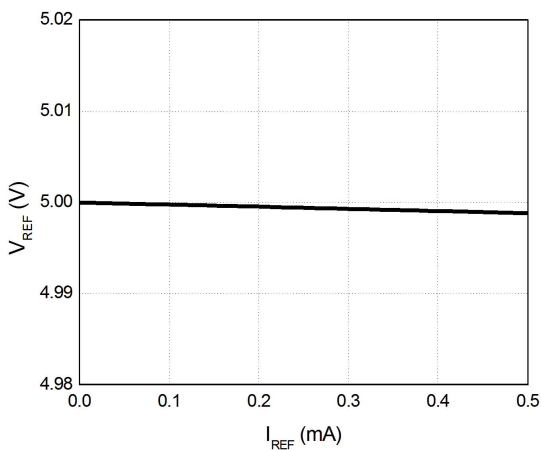
V_{REF} Line Regulation Voltage



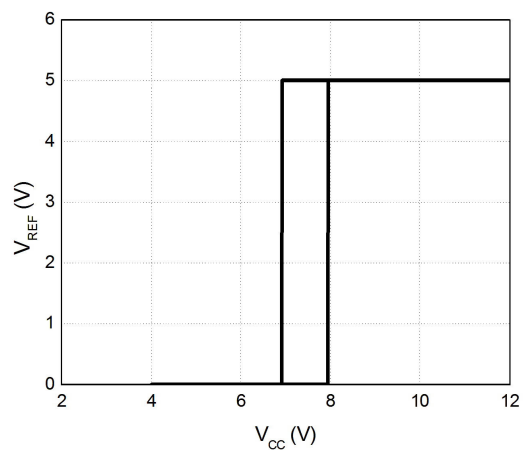
V_{REF} vs. Temp



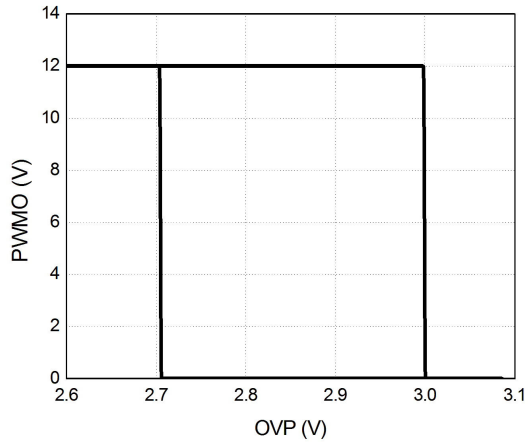
V_{REF} Load Regulation Voltage



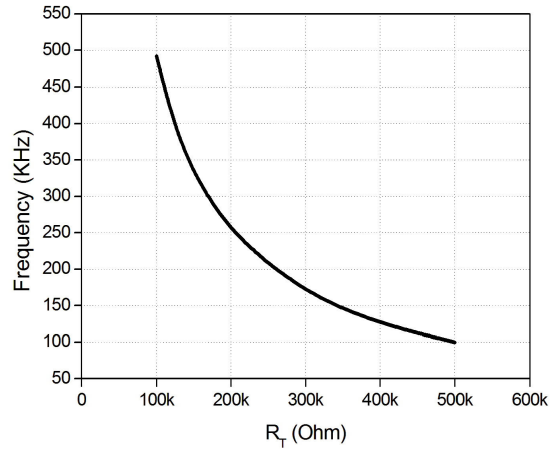
Under Voltage Lock Out (UVLO)



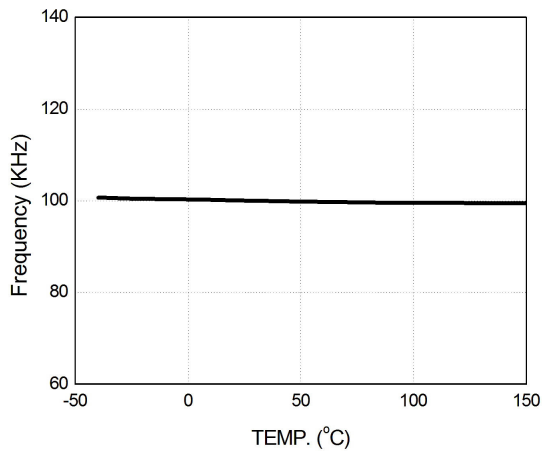
Over Voltage Protection.(OVP)



Frequency vs. RT



Frequency vs. Temp



Application Information

Current Mode Boost switching regulator operation

The MAP3202 is operated in current mode PWM Boost regulation method, which shows fast frequency response while maintaining stable output voltage.

It features stable response by using the recommended combination of resistor and capacitor at COMP and GND pin for specific condition of wide input voltage, Output voltage and variable Load condition.

Internal 5V Low Dropout Regulator

The MAP3202 has LDO embedded in it to supply Internal analog, logic circuit and external REF Pin. This LDO operates at a voltage level where Vcc is higher than the UVLO voltage. It provides maximum 10mA of output current through regulator which has 2% accuracy of performance.

To stabilize the voltage of REF Pin, it is recommended to use low ESR capacitor which is as low as 1uF and connect it between REF and GND Pin, and install it as close as to Pin.

Boost Converter Switching Frequency

The MAP3202 can set the switching frequency of Boost converter by connecting external resistor between RT and GND Pin. Recommended switching frequency is 100 KHz to 400 KHz.

See Figure 1 for switching frequency adjustment resistor (RT)

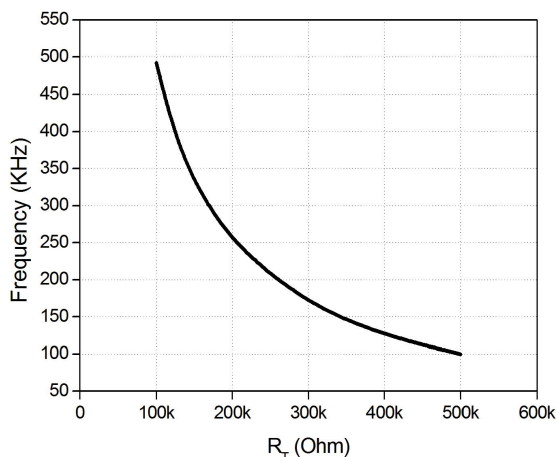


Figure 1 Boost switching frequency vs. RT

The Boost switching frequency can be decided in the following equation.

$$T_{osc}(us) = \frac{RT(Kohm) + 1.75}{50}$$

SYNCHRONIZATION

The MAP3202's switching frequency can be set by internal clock or by external master clock signal through SYNC Pin. The clock signal of SYNC Pin needs to be faster than internal Oscillator clock to ensure normal switching operation.

When synchronizing multiple MAP3202 on single board, all SYNC Pin ICs of each device should be short to make all devices in sync on the Oscillator clock of the fastest device. It is recommended to use low ESR capacitor which is as low as 10pF and connect it between SYNC and GND Pin each device, and install it as close as to Pin.

In this case, the number of synchronized devices differs depending on the operation frequency of Oscillator.

If this function of peer to peer synchronization is not used, the SYNC pin may be required to be open or short to GND. It is recommended to connect SYNC Pin to GND because this solution provides better immunity against parasitic noise from layout.

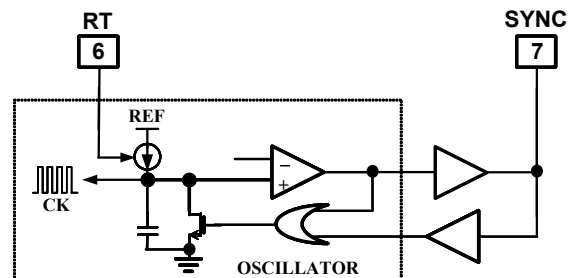


Figure 2 Internal OSC & SYNC circuit

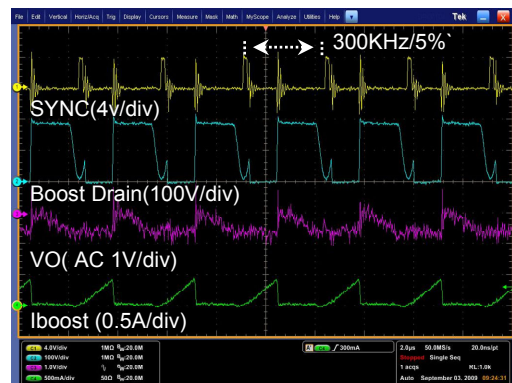


Figure 3 Synchronization by external clock (Fixed 100 KHz → 300 KHz)

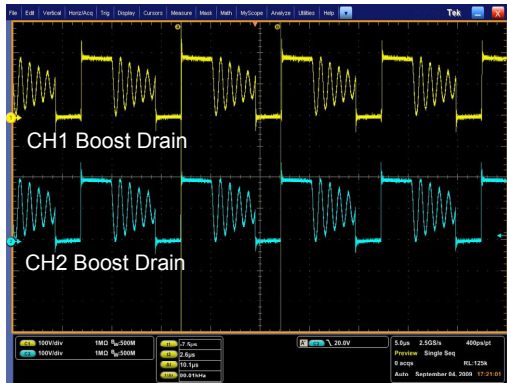


Figure 4 Peer - to -peer synchronization (Fixed 100 KHz)

PROTECTION

The MAP3202 offers the features such as UVLO, Boost current limit, Over Voltage Protection and Short Current Protection of LED (SCP). OVP and SCP are operated in auto restart protection mode.

1. Under Voltage Lock Out (UVLO)

When VCC voltage reaches over 8V, UVLO starts operating which enables Internal 5V Regulator, making all internal control circuits including oscillator, gate driver and protection circuit ready for operation and output pin of GATE, PWM0 and COMP starts operating depending on the input status of PWMI.

If VCC voltage drops below 7V during normal operation, UVLO starts operating, shutting down Internal Control Circuit and stopping operation of GATE, PWM0 and COMP. It is followed by disabling of internal 5V regulator, and shut off of all IC operation.

2. Maximum Boost Current Limit

MAP3202 has the internal current limit threshold voltage, 0.36V (Typ.). If the sense voltage on CS pin exceeds 0.36V, MAP3202 limits boost on duty every pulse.

MAP3202's CS circuitry has the Leading edge blank time at 100nS (min.).

3. Over Voltage Protection (OVP)

The MAP3202 offers over voltage protection in order to protect MOSFET of boost converter and external component connected to Output pin when output voltage is in abnormal condition.

OVP Circuit monitors whether output voltage is stable level or not

If OVP Pin voltage reaches threshold condition (3V Typ.), it can shut off the switching of GATE and PWM0 and then output voltage is falling as much as the leakage current time. If the voltage of OVP Pin reaches OVP falling threshold (2.7V Typ.), IC releases protection mode. In this time, protection releasing can be decided as value of capacitor with the longer discharge between auto restart time and the time of leakage current connected to output.

The over voltage protection can be decided in the following equation.

- Protection voltage:

$$V_{out} = 3 * \frac{Ro1 + Ro2}{Ro2}$$

- Protection release voltage:

$$V_{out} = 2.7 * \frac{Ro1 + Ro2}{Ro2}$$

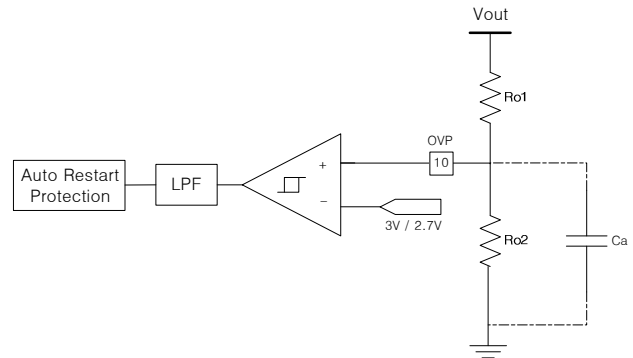


Figure 5 Over voltage protection circuit

The MAP3202 included LPF (low pass filter) of 200nS (Typ.) in OVP circuit for better noise immunity, It may need a high noise margin when Ro1 and Ro2 use high resistance value in order to minimize Power loss.

The total values of Ro1 and Ro2 need to be lower than 1Mohm. In this case, it is recommended to add Capacitor.

4. Short Current Protection of LED (SCP)

The MAP3202 offers protection circuit to prevent short current when LED string is shorted

In Figure 6 when LED string is shorted, the voltage of FBN Pin can be calculated in the following equation

$$V_{FBN} = I_{LED} * R_{LED}$$

If the voltage of FBN pin exceeds the voltage of FBP X 2.5, MAP3202 goes into SCP mode.

It is recommended which FBP max voltage 1.5V.

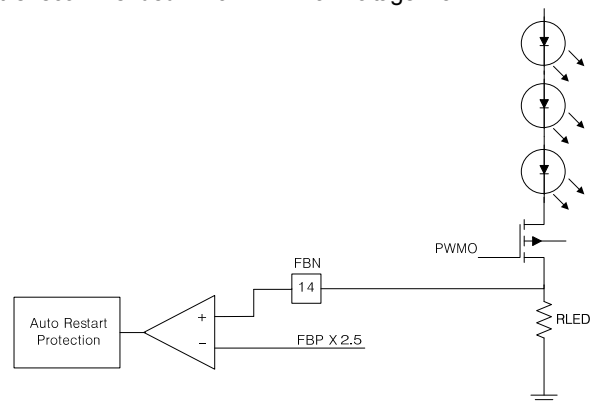


Figure 6 Short current protections

SCP Circuit uses very fast comparator in order to turn off MOSFET when the abnormal condition of SCP Level is detected. Because high current can be driven into channel of MOSFET when LED string is shorted.

5. Auto-Restart Protection

The MAP3202 offers Auto Restart protection function which is recovered into normal operation mode when protection condition is cleared. The auto restart time (T_{AR}) is fixed at 1mS, $F_{osc} = 100KHz$. it is recovered to normal operating mode if SCP or OVP condition is cleared.

Dimming Control

1. LED Current

The MAP3202 decides LED Current setting by the value of RLED resistance and voltage on FBP pin as below

$$LED_Current = \frac{V_{FBP}}{R_{LED}}$$

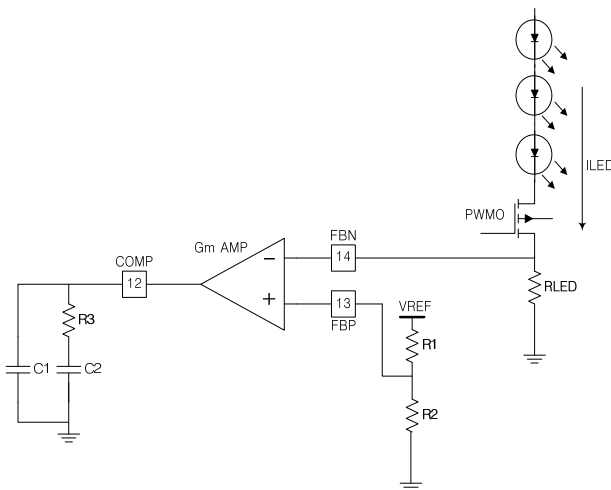


Figure 7 LED Current Setting

2. PWM Dimming

The MAP3202 makes same phase PWMO output from logic PWM signal of PWMI using internal Level shift. PWMO of operating voltage level is between GND and VCC.

Inductor Selection

Inductor value should be decided before system design. Because the selection of the inductor affects the operating mode of CCM (Continuous current mode) or DCM (Discontinuous current mode). In CCM operation, inductor size should be bigger, even though the ripple current and peak current of inductor can be small.

In DCM operation, even ripple current and peak current of inductor should be large while the inductor size can be smaller so that it is more effective in BLU of TV and Notebook application.

The MAP3202 was designed for DCM operation.

In CCM operation, sub-harmonic oscillation may occur if duty cycle exceeds over 50%. Because there is no slope compensation functions.

The following is the equation to calculate max value of Inductor in DCM operation.

$$L_{(max)} = \frac{[(1-D)^2 * D * R_{O(max)} * T_{s(min)}]}{2}$$

Where,

$R_{O(max)}$ = Maximum output impedance

$T_{S(min)}$ = Minimum Switching Period

Closed Loop Network Selection

The MAP3202 controls in peak current mode. Current mode easily achieves compensation by consisting simple single Pole from Double Pole that LC filter makes at Voltage mode

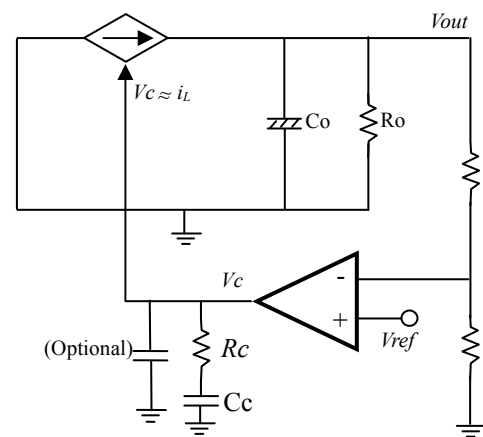


Figure 8 Current mode Loop Compensation

1. Select f_c (Crossover frequency)

In general, crossover frequency is selected from 1/3 ~ 1/6 range of the switching frequency. If f_c is large, there is possibility of oscillation to occur, although time response gets better.

On the other hand, if f_c is small, time response will be bad, while it has improved stability, which may cause over shoot or under shoot in abnormal condition.

It should be noted that f_c should be set at smaller location than RHP Zero.

$$f_{RHP} = \frac{R_o * (1-D)^2}{2\pi * L}$$

2. Select f_{PO}

$$f_{PO} = f_c * G_O$$

$$(G_O = DC \text{ Gain of plant} = \frac{A}{B})$$

$$A = \frac{1}{\frac{2}{R} + \frac{(m-0.5)*(1-D)^3}{L*F}}$$

Selecting approximately $m = 1.4$

$$B = R_S * (1 - D)$$

R_S = Sensing Resistor

3. Select Pole and Zero

$$f_{PO} = \frac{1}{2\pi * \frac{C_C}{Y * G_{EA}}}$$

G_{EA} = Gm-Amp Transconductance

$$Y = \text{Attenuation} - \text{Ratio} = \frac{V_{FPN}}{V_O}$$

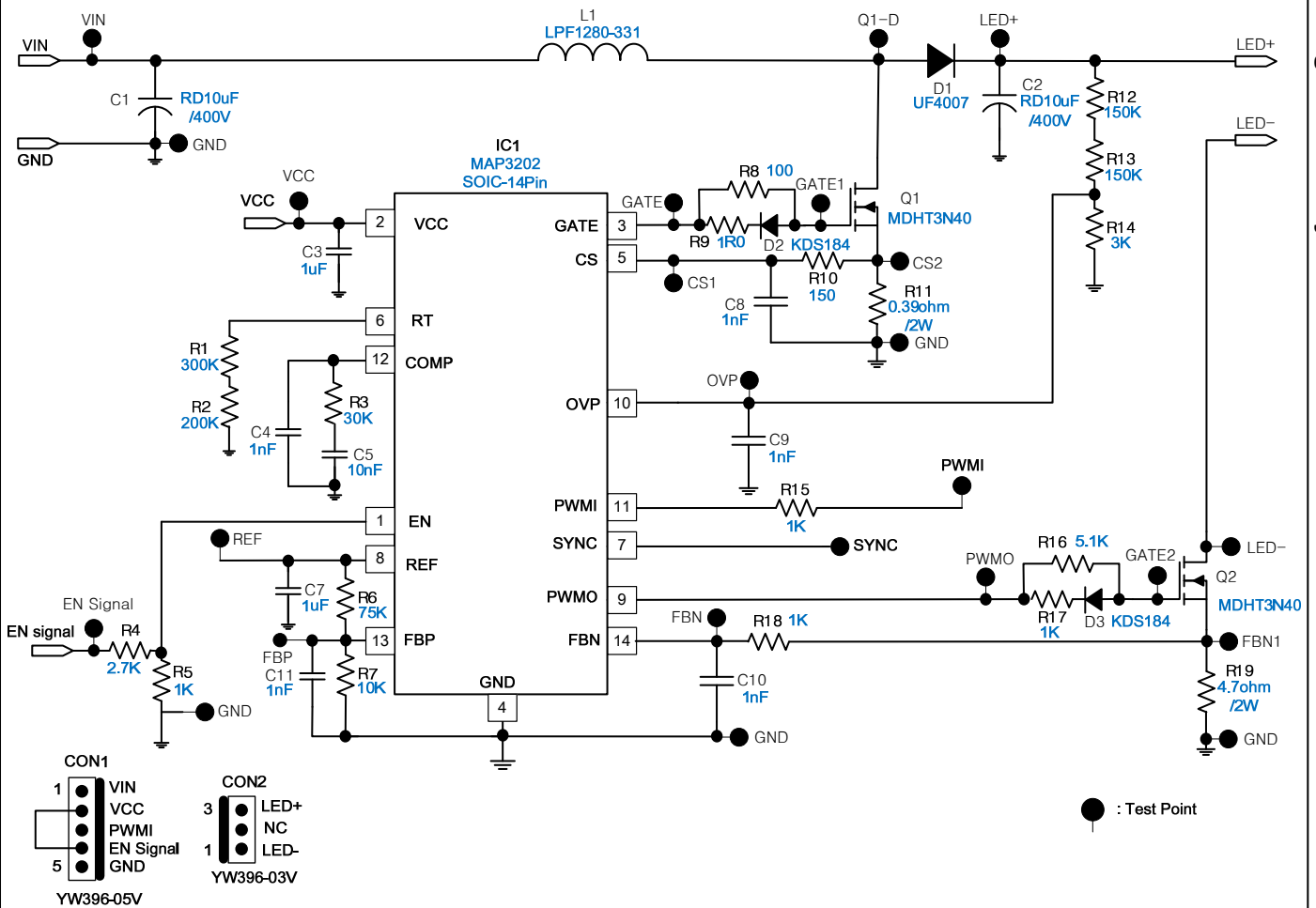
$$f_{Z1} = \frac{1}{2\pi * R_C * C_C}$$

Zero is set at the same location of output pole in system design, if ESR of output capacitor is large, Pole should be set at same frequency in order to compensate the Zero of ESR.

$$f_{P1(OP)} = \frac{1}{2\pi * R_C * C_{OP}}$$

Evaluation Board Schematic

Condition : Vin=120V, Vout = 63LEDs, LED current = 125mA, OVP set = 303V, Release = 272V, SW Frequency=100KHz

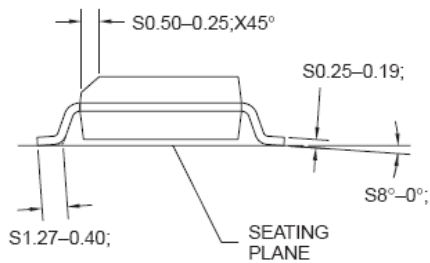
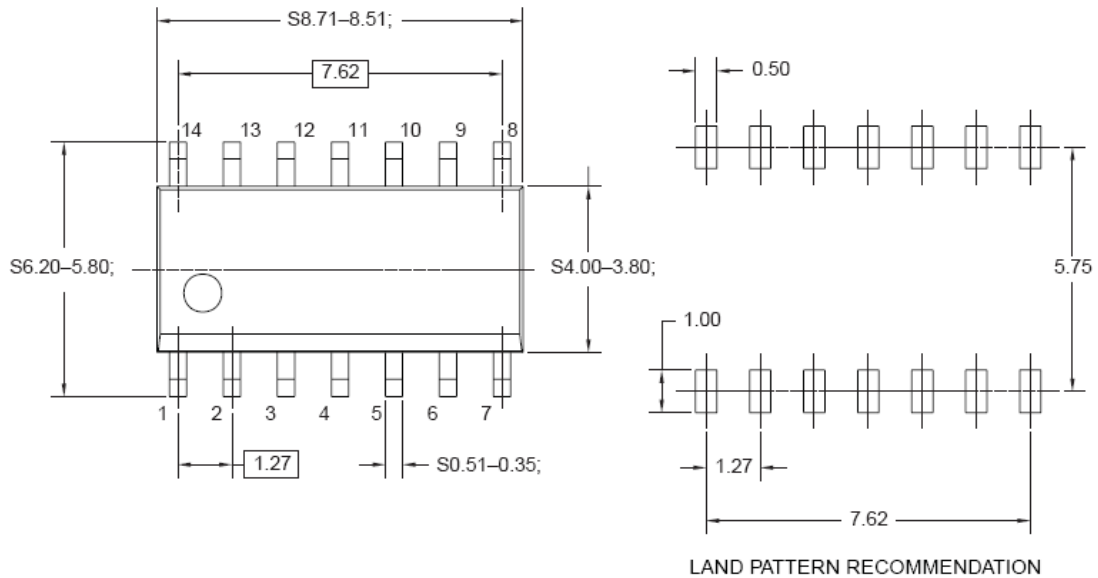


Evaluation Board Part List

	Spec	Vendor	P/N
Input Capacitor	10uF/400V	Samwha ¹	RD10uF/400V
Output Capacitor	10uF/400V	Samwha ¹	RD10uF/400V
Inductor	330uH	ABCO ²	LPF1280-331
Boost MOSFET	3A/400V, N-Ch, SOT223	MagnaChip	MDHT3N40
Dimming MOSFET	3A/400V, N-Ch, SOT223	MagnaChip	MDHT3N40
Ultrafast Diode	1A/1000V	VISHAY	UF4007
IC	PWM Controller	MagnaChip	MAP3202

- SAMWHA :
 - ELECTROLYTIC CAPACITOR, SAMWHA ELECTRIC tel : +82-43-261-0200, <http://www.samwha.co.kr/electric>
 - MLCC CAPACITOR, SAMWHA CAPACITOR tel : +82-31-330-5872, <http://www.samwha.co.kr/capacitor>
- ABCO tel : +82-31-730-5000, <http://www.abco.co.kr>

Physical Dimensions



14Lead SOIC

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MagnaChip Semiconductor Ltd.

891, Daechi-Dong, Kangnam-Gu, Seoul, 135-738 Korea

Tel : 82-2-6903-3451 / Fax : 82-2-6903-3668 ~9

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Revision History

Date	Version	Changes
2010-03-18	Version 1.0	Initial release.
2012-03-15	Version 1.1	Changed Absolute Maximum Ratings 5.0V to 6.0V