

TEAC

SERVICE MANUAL

PD-H500C

Compact Disc Player

NOTES

- PC boards shown are viewed from parts side.
- The parts with no reference number or no parts number in the exploded views are not supplied.
- As regards the resistors and capacitors, refer to the circuit diagrams contained in this manual.
- \triangle Parts marked with this sign are safety critical components. They must be replaced with identical components- refer to the appropriate parts list and ensure exact replacement.
- Parts of [] mark can be used only with the version designated.
[DM]: JAPAN [T/C]: U.S.A, CANADA
[EUR]: EUROPE [UK]: UK

CONTENTS

SPECIFICATIONS.....
MEASUREMENT AND ADJUSTMENT METHODS.....
IC PIN FUNCTION.....
WIRING DIAGRAM.....
BLOCK DIAGRAM.....
SCHEMATIC DIAGRAM.....
PRINTED CIRCUIT BOARDS.....
EXPLODED VIEW.....
ELECTRICAL PARTS LIST.....

Specifications

Laser System : 3-beam laser
Digital Filter : 8-times oversampling
Frequency Response : 20-20,000Hz(±2dB)
Error Correction Method :
 Cross Interleave Reed-Solomon code
S/N Ratio : More than 100dB
 (IHF "A" Filter used)
THD : Less than 0.02% (1KHz)
Output Voltage : 2V RMS

Power Consumption : 12W
Dimensions (W×H×D) : 285×131×292mm
Weight : 3.9Kg

Standard Accessories

Remote control cord
Signal output cord

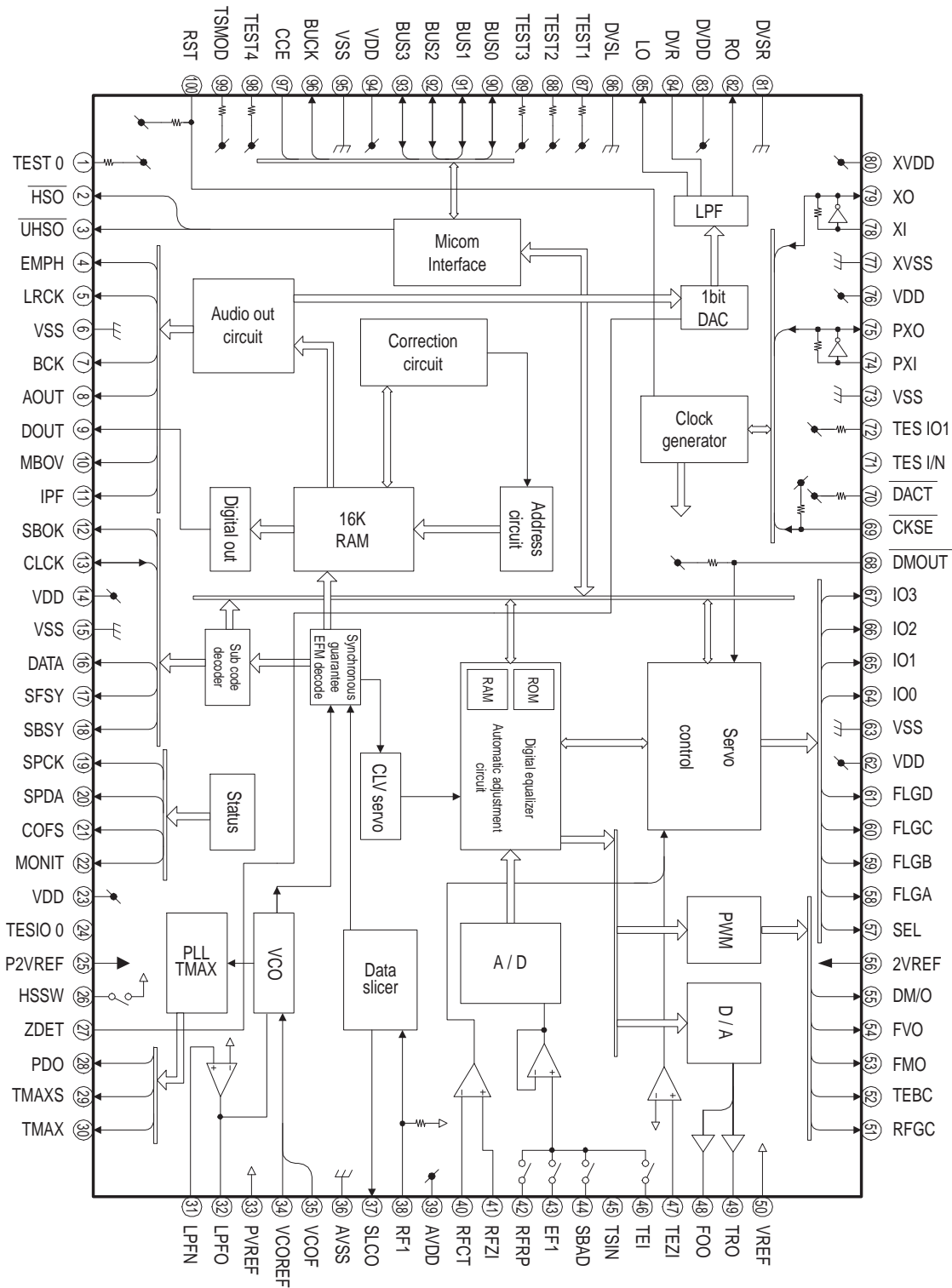
- * Improvements may result in specification or feature changes without notice.
- * Photos and illustrations may differ slightly from production models.

TC9432AF/ TC9462AF (Digital Signal Processor)

PIN No.	NAME	I/O	FUNCTIONAL DESCRIPTION	REMARKS															
1	TEST0	-	Test mode terminal. Normally, keep at open.	With pull-up resistor.															
2	$\overline{\text{HSO}}$	O	Playback speed mode flag output terminal.	-															
3	$\overline{\text{UHSO}}$	O	<table border="1" style="width: 100%; border-collapse: collapse; margin: 5px;"> <thead> <tr> <th style="text-align: center;">$\overline{\text{UHSO}}$</th> <th style="text-align: center;">$\overline{\text{HSO}}$</th> <th style="text-align: center;">PLAYBACK SPEED</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">H</td> <td style="text-align: center;">H</td> <td style="text-align: center;">Normal</td> </tr> <tr> <td style="text-align: center;">H</td> <td style="text-align: center;">L</td> <td style="text-align: center;">2 times</td> </tr> <tr> <td style="text-align: center;">L</td> <td style="text-align: center;">H</td> <td style="text-align: center;">4 times</td> </tr> <tr> <td style="text-align: center;">L</td> <td style="text-align: center;">L</td> <td style="text-align: center;">-</td> </tr> </tbody> </table>		$\overline{\text{UHSO}}$	$\overline{\text{HSO}}$	PLAYBACK SPEED	H	H	Normal	H	L	2 times	L	H	4 times	L	L	-
$\overline{\text{UHSO}}$	$\overline{\text{HSO}}$	PLAYBACK SPEED																	
H	H	Normal																	
H	L	2 times																	
L	H	4 times																	
L	L	-																	
4	EMPH	O	Subcode Q data emphasis flag output terminal. Emphasis ON at "H" level and OFF at "L" level. The output polarity can invert by command.	-															
5	LRCK	O	Channel clock output terminal. (44.1 kHz) L-ch at "L" level and R-ch at "H" level. The output polarity can invert by command.	-															
6	Vss	-	Digital GND terminal.	-															
7	BCK	O	Bit clock output terminal. (1.4112 MHz)	-															
8	AOUT	O	Audio data output terminal.	-															
9	DOUT	O	Digital data output terminal.	-															
10	MBOV	O	Buffer memory over signal output terminal. Over at "H" level.	-															
11	IPF	O	Correction flag output terminal. At "H" level, AOUT output is made to correction impossibility by C2 correction processing.	-															
12	SBOK	O	Subcode Q data CRCC check adjusting result output terminal. The adjusting result is OK at "H" level.	-															
13	CLCK	I/O	Subcode P-W data readout clock input/output terminal. This terminal can select by command bit.	-															
14	VDD	-	Digital power supply voltage terminal.	-															
15	Vss	-	Digital GND terminal.	-															
16	DATA	O	Subcode P-W data output terminal.	-															
17	SFSY	O	Playback frame sync signal output terminal.	-															
18	SBSY	O	Subcode block sync signal output terminal.	-															
19	SPCK	O	Processor status signal readout clock output terminal.	-															
20	SPDA	O	Processor status signal output terminal.	-															
21	COFS	O	Correction frame clock output terminal. (7.35 kHz)	-															
22	MONIT	O	Internal signal (DSP internal flag and PLL clock) output terminal. Selected by command.	-															
23	VDD	-	Digital power supply voltage terminal.	-															
24	TESIO0	I	Test input/output terminal. Normally, keep at "L" level.	-															
25	P2VREF	-	PLL double reference voltage supply terminal.	-															
26	HSSW	O	2/4 times speed at "VREF" voltage.	2-state output (PVREF, HiZ)															
27	ZDET	O	1 bit DA converter zero detect flag output terminal.	-															
28	PDO	O	Phase difference signal output terminal of EFM signal and PLCK signal.	3-state output (P2VREF, PVREF, Vss)															
29	TMAXS	O	TMAX detection result output terminal. Selected by command bit (TMPS).	-															
30	TMAX	O	TMAX detection result output terminal. Selected by command bit (TMPS).	3-state output (P2VREF, HiZ, Vss)															
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DIFFERENCE RESULT	TMAX OUTPUT																		
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PIN No.	NAME	I/O	FUNCTIONAL DESCRIPTION	REMARKS
31	LPFN	I	LPF amplifier inverting input terminal for PLL.	Analog input.
32	LPFO	O	LPF amplifier output terminal for PLL.	Analog output.
33	PVREF	-	PLL reference voltage supply terminal.	-
34	VCOREF	I	VCO center frequency reference level terminal. Normally, keep at "PVREF" level.	-
35	VCOF	O	VCO filter terminal.	Analog output.
36	AVss	-	Analog GND terminal.	-
37	SLCO	O	Data slice level output terminal.	Analog output.
38	RFI	I	RF signal input terminal.	Analog input (Zin : selected by command)
39	AVDD	-	Analog power supply voltage terminal.	-
40	RFCT	I	RFRP signal center level input terminal.	Analog input (Zin : 50k Ω)
41	RFZI	I	RFRP zero cross input terminal.	Analog input.
42	RFRP	I	RF ripple signal input terminal.	Analog input.
43	FEI	I	Focus error signal input terminal.	Analog input.
44	SBAD	I	Sub-beam adder signal input terminal.	Analog input.
45	TSIN	I	Test input terminal. Normally, keep at "VREF" level.	Analog input.
46	TEI	I	Tracking error signal input terminal. Track in at tracking servo on.	Analog input.
47	TEZI	I	Tracking error zero cross input terminal.	Analog input (Zin : 10k Ω)
48	FOO	O	Focus servo equalizer output terminal.	Analog output (2VREF~AVSS)
49	TRO	O	Tracking servo equalizer output terminal.	-
50	VREF	-	Analog reference voltage supply terminal.	-
51	RFGC	O	RF amplitude adjustment control signal output terminal.	3-state PWM signal output. (2VREF, VREF, VSS) (PWM carrier = 88.2 kHz)
52	TEBC	O	Tracking balance control signal output terminal.	
53	TEBC	O	Feed equalizer output terminal.	
54	TEBC	O	Speed error signal or feed search equalizer output terminal.	(PWM carrier = 88.2 kHz)
55	DMO	O	Disk equalizer output terminal. (PWM carrier = 88.2 kHz for DSP, Synchronize to PXO)	3-state PWM signal output.(2VREF, VREF, VSS)
56	2VREF	-	Analog double reference voltage supply terminal.	-
57	SEL	O	APC circuit ON/OFF indication signal output terminal. At the laser on time, UHF = L at "HiZ" level and UHF = H at "H" level.	-
58	FLGA	O	External flag output terminal for internal signal. Can select signal from TEZC, FOON, FOK and RFZC by command.	-
59	FLGB	O	External flag output terminal for internal signal. Can select signal from DECT, FOON, FMON and RFZC by command.	-
60	FLGC	O	External flag output terminal for internal signal. Can select signal from TRON, TRSR, FOK and SRCH by command.	-
61	FLGD	O	External flag output terminal for internal signal. Can select signal from TRON, DMON, HYS and SHC by command.	-
62	VDD	-	Digital power supply voltage terminal.	-
63	VSS	-	Digital GND terminal.	-
64	IO0	I/O	General I/O terminal. Can change over input port or output port by command. At the input mode time can readout a state of terminal (H/L) by read command. At the output mode time can control a state of terminal (H/L/HiZ) by command.	-
65	IO1			
66	IO2			
67	IO3			

PIN No.	NAME	I/O	FUNCTIONAL DESCRIPTION	REMARKS
68	$\overline{\text{DMOUT}}$	I	This terminal controls IO0-IO3 terminal. At "L" level time, IO0, 1 out feed equalizer signal of 2-state PWM. IO2, 3 out disk equalizer signal of 2-state PWM.	With pull-up resistor.
69	$\overline{\text{CKSE}}$	I	Normally, keep at open.	With pull-up resistor.
70	$\overline{\text{DACT}}$	I	DAC test mode terminal. Normally, keep at open.	With pull-up resistor.
71	TESIN	I	Test input terminal. Normally, keep at "L" level.	Analog input.
72	TESIO1	I	Test input/output terminal. Normally, keep at "L" level.	Analog input.
73	Vss	-	Digital GND terminal.	-
74	PXI	I	Crystal oscillator connecting input terminal for DSP. Normally, keep at "L" level.	-
75	PXO	O	Crystal oscillator connecting output terminal for DSP.	-
76	VDD	-	Digital power supply voltage terminal.	-
77	XVss	-	Oscillator GND terminal for system clock.	-
78	XI	I	Crystal oscillator connecting input terminal for system clock.	-
79	XO	O	Crystal oscillator connecting output terminal for system clock.	-
80	XVDD	-	Oscillator power supply voltage terminal for system clock.	-
81	DVSR	-	Analog GND terminal for DA converter. (R-ch)	-
82	RO	O	R channel data forward output terminal.	-
83	DVDD	-	Analog supply voltage terminal for DA converter.	-
84	DVR	-	Reference voltage terminal for DA converter.	-
85	LO	O	L channel data forward output terminal.	-
86	DVSL	-	Analog GND terminal for DA converter. (L-ch)	-
87	TEST1	I	Test mode terminal. Normal, keep at open.	With pull-up resistor.
88	TEST2	I	Test mode terminal. Normal, keep at open.	With pull-up resistor.
89	TEST3	I	Test mode terminal. Normal, keep at open.	With pull-up resistor.
90	BUS0	I/O	Micom interface data input/output terminal.	Schmit input. With pull-up resistor.
91	BUS1	I/O		
92	BUS2	I/O		
93	BUS3	I/O		
94	VDD	-	Digital Ppower supply voltage terminal.	-
95	Vss	-	Digital GND terminal.	-
96	BUCK	I	Micom interface clock input terminal.	Schmit input.
97	$\overline{\text{CCE}}$	I	Command and data sending/receiving chip enable signal input terminal. The bus line becomes active at "L" level.	Schmit input.
98	TEST4	I	Test mode terminal. Normal, keep at open.	With pull-up resistor.
99	$\overline{\text{TSMOD}}$	I	Local test mode selection terminal.	With pull-up resistor.
100	$\overline{\text{RST}}$	I	Reset signal input terminal. Reset at "L" level.	With pull-up resistor.

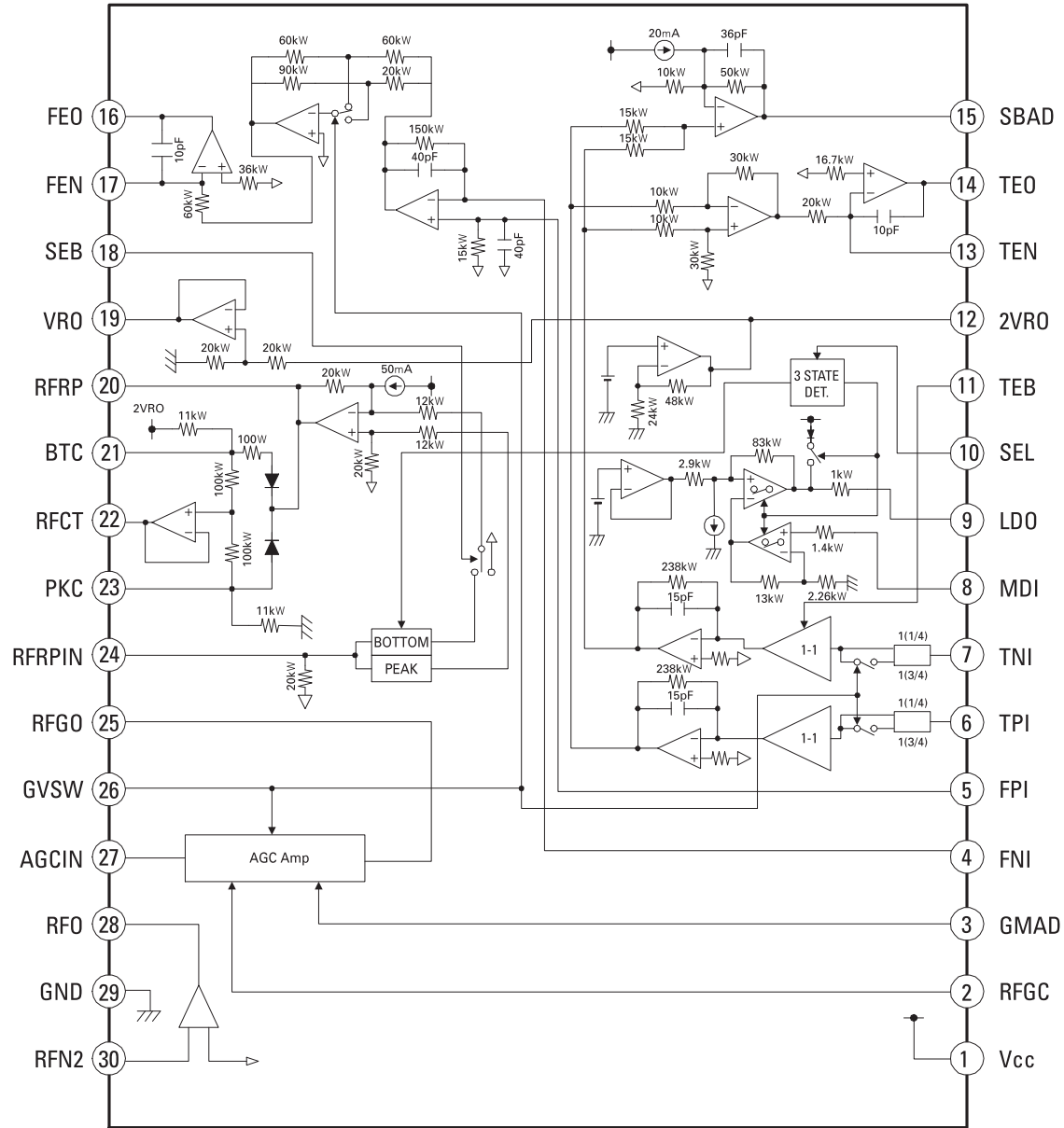


TA2150FN

PIN No.	SYMBOL	I/O	FUNCTION DESCRIPTION	REMARKS																
1	VCC	-	Power supply input terminal.	-																
2	RFGC	I	RF amplitude adjustment control signal input terminal. Controlled by 3-PWM signals. (PWM carrier = 88.2kHz)	3 signals input. (2VRO, VRO, GND)																
3	GMAD	I	Open loop gain adjustment terminal for AGC amp.	(Note 1)																
4	FNI	I	Main beam I-V amp input terminal.	Connected to pin diode output B + D (through resistor)																
5	FPI	I	Main beam I-V amp input terminal.	Connected to pin diode output A + C (through resistor)																
6	TPI	I	Sub beam I-V amp input terminal.	Connected to pin diode output F.																
7	TNI	I	Sub beam I-V amp input terminal.	Connected to pin diode output E.																
8	MDI	I	Monitor photo diode amp input terminal.	Connected to pin monitor photo diode.																
9	LDO	O	Laser diode amp input terminal.	Connected to laser diode control circuit.																
10	SEL	I	Laser diode control signal input terminal and APC circuit ON/OFF control signal terminal. <table border="1" data-bbox="565 997 1068 1171"> <thead> <tr> <th>SEL LEVEL</th> <th>APC CIRCUIT</th> <th>LDO</th> <th>DETECT FREQUENCY</th> </tr> </thead> <tbody> <tr> <td>GND</td> <td>OFF</td> <td>Connected to Vcc through resistor (1 kΩ)</td> <td>Low</td> </tr> <tr> <td>Hiz</td> <td>ON</td> <td>Control signal output</td> <td>Low</td> </tr> <tr> <td>Vcc</td> <td>ON</td> <td>Control signal output</td> <td>High</td> </tr> </tbody> </table>	SEL LEVEL	APC CIRCUIT	LDO	DETECT FREQUENCY	GND	OFF	Connected to Vcc through resistor (1 k Ω)	Low	Hiz	ON	Control signal output	Low	Vcc	ON	Control signal output	High	3 signals input. (Vcc, Hiz, GND)
SEL LEVEL	APC CIRCUIT	LDO	DETECT FREQUENCY																	
GND	OFF	Connected to Vcc through resistor (1 k Ω)	Low																	
Hiz	ON	Control signal output	Low																	
Vcc	ON	Control signal output	High																	
11	TEB	I	Tracking error balance adjustment signal input terminal. Controlled by 3-PWM signal. (PWM carrier = 88.2 kHz)	3 signals input (2VRO, VRO, GND)																
12	2VRO	O	Reference voltage (2VRO) output terminal. 2VRO = 4.2 V when Vcc = 5 V	-																
13	TEN	I	TE amp negative input terminal.	Connected to TEO through feedback resistor.																
14	TEO	O	TE error signal output terminal.	-																
15	SBAD	O	Sub beam adder signal output terminal.	-																
16	FEO	O	Focus error signal output terminal.	-																
17	FEN	I	FE amp negative input terminal.	Connected to FEO through feedback resistor.																
18	SEB	I	RFRP output circuit switching terminal. <table border="1" data-bbox="617 1591 1006 1717"> <thead> <tr> <th>SEB LEVEL</th> <th>BOTTON DETECTION</th> <th>PEAK DETECTION</th> </tr> </thead> <tbody> <tr> <td>GND</td> <td>GND</td> <td>GND</td> </tr> <tr> <td>GND</td> <td>GND</td> <td>GND</td> </tr> </tbody> </table>	SEB LEVEL	BOTTON DETECTION	PEAK DETECTION	GND	GND	GND	GND	GND	GND	Low (GND) is for normal use.							
SEB LEVEL	BOTTON DETECTION	PEAK DETECTION																		
GND	GND	GND																		
GND	GND	GND																		

TA2150FN

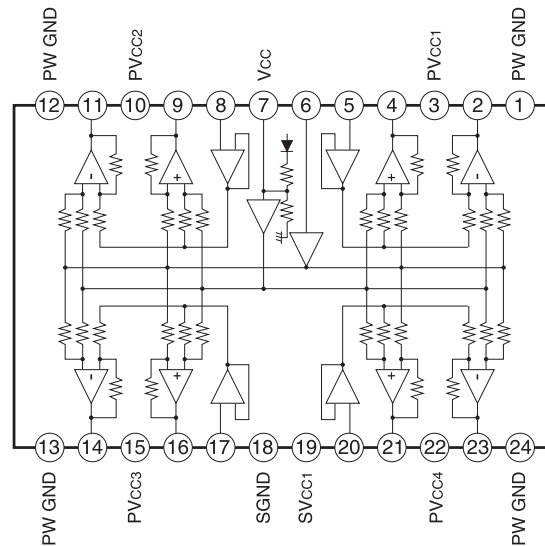
PIN No.	SYMBOL	I/O	FUNCTION DESCRIPTION	REMARKS								
19	VRO	O	Reference signal (VRO) output terminal. VRO = 2.1 V when Vcc = 5 V	-								
20	RFRP	O	Track count signal output terminal.	-								
21	BTC	I	Time constant adjustment terminal for bottom detection.	Adjusted by capacitance.								
22	RFCT	O	RFRP signal center level output terminal.	-								
23	PKC	I	Time constant adjustment terminal for peak detection.	Adjusted by capacitance.								
24	RFRPIN	I	Input terminal for track count signal output amp.	-								
25	RFGO	O	Output terminal for RF signal amplitude adjustment amp.	-								
26	GVSW	I	Amp (AGC, FE, TE) gain switching terminal. <table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <td>GVSW</td> <td>MODE</td> </tr> <tr> <td>GND</td> <td>CD-RW</td> </tr> <tr> <td>Hiz</td> <td>Normal</td> </tr> <tr> <td>Vcc</td> <td>Normal</td> </tr> </table>	GVSW	MODE	GND	CD-RW	Hiz	Normal	Vcc	Normal	Low (GND) is for 5 times gain.
GVSW	MODE											
GND	CD-RW											
Hiz	Normal											
Vcc	Normal											
27	AGCIN	I	Input terminal for RF signal amplitude adjustment amp.	Connected to RFO through capacitance.								
28	RFO	O	Output terminal RF signal amp.	-								
29	GND	-	Ground terminal.	-								
30	RFN2	I	input terminal for RF signal amp.	Connected to pin-diode output A + B + C + D (through resistor).								



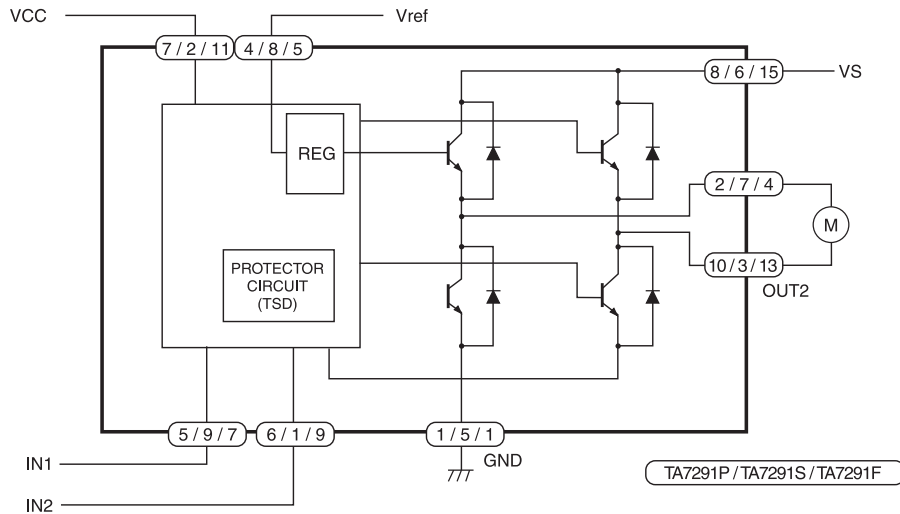
TA2092N (POWER DRIVER)

PIN No.	NAME	DESCRIPTION
1	PW GND	Power GND Connected to substrate. ① , ⑫ , ⑬ , ⑳ pin are connected inside.
2	OUT (-) 1	Inverted output for CH1
3	PVCC1	Supply terminal of output stage for CH1 Supply terminal of output stage are not connected to other channel terminal.
4	OUT (+) 1	Non-inverted output for CH1
5	VIN1	Input for CH1. Not biased inside
6	VRI	Input reference voltage Under condition of $V_{RI} \leq 1.8V$, internal bias circuit is shut off. No signal input condition : $V_{RI} = V_{IN}$
7	VCI	Output reference voltage. $V_{OUT} = V_{CI} = (V_{CC}-V_F)/2$
8	VIN2	Input for CH2
9	OUT (+) 2	Non-inverted output for CH2
10	PVCC2	Supply terminal of output stage for CH2
11	OUT (-) 2	Inverted output for CH2
12	PW GND	Power GND
13	PW GND	Power GND
14	OUT (-) 3	Inverted output for CH3
15	PVCC3	Supply terminal of output stage for CH3
16	OUT (+) 3	Non-inverted output for CH3
17	VIN3	Input for CH3
18	S GND	Supply terminal of small signal GND
19	S Vcc	Small signal GND
20	VIN4	Input for CH4
21	OUT (+) 4	Non-inverted output for CH4
22	PVCC4	Supply terminal of output stage for CH4
23	OUT (-) 4	Inverted output for CH4
24	PW GND	Power GND

BLOCK DIAGRAM



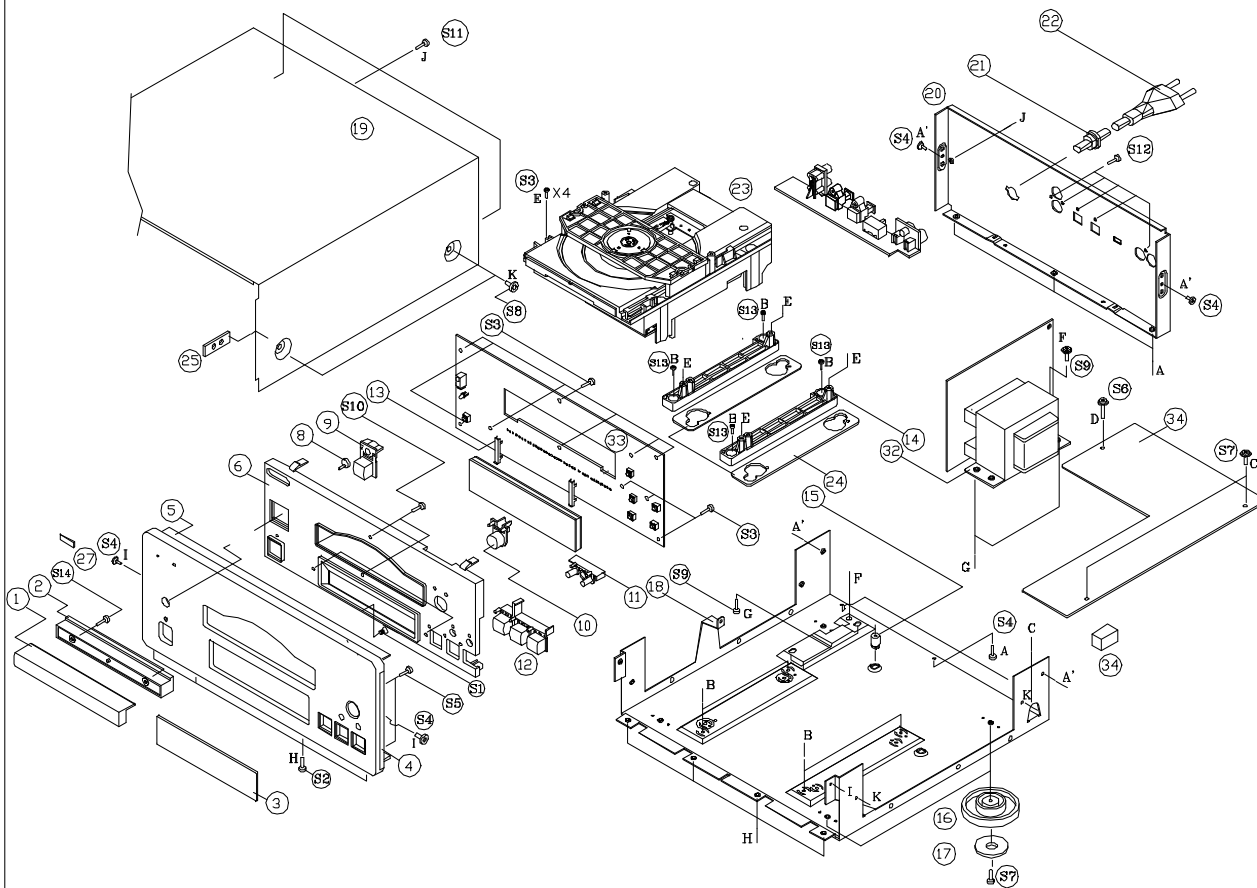
TA7291S (Bridge Driver)



PIN No.		SYMBOL	FUNCTIONAL DESCRIPTION
P	S		
7	2	Vcc	Supply voltage terminal for Logic
8	6	Vs	Supply voltage terminal for motor drive
4	8	Vref	Supply voltage terminal for control
1	5	GND	GND terminal
5	9	IN1	Input terminal
6	1	IN2	Input terminal
2	7	OUT1	Output terminal
10	3	OUT2	Output terminal

- P Type : PIN ③, ⑨ : NC
- S Type : PIN 4 : NC
- F Type : PIN ②, ③, ⑥, ⑧, ⑩, ⑫, ⑭, and ⑯ : NC
- For F Type, We recommend FIN to be connected to the GND.

PD-H500C EXPLODED VIEW(EUR/UK)



NO	PARTS - NO	DESCRIPTION	QTY	MODEL NO.
1	KK028210E1J	FRONT PANEL	1	
2	KK01A52517	DRIVE CD	1	
3	KGUA04M4Y	WINDOW FILP	1	
4	KK02A05C11	PANEL SUB	2	
5	KK04A054VC11	PANEL BL	1	
6	KG04A072N9064	PANEL SUB	1	
7	KG04A245A11	WINDOW SENSOR	1	
8	KG029120	INITIALER POWER	1	
9	KBT0A3872K64	ENDR POWER	1	
10	KBT1A3822K64	ENDR OPEN	1	
11	KBT1A0019	ENDR STOP	1	
12	KBT1A386WK64	ENDR PLAY	1	
13	KND0A289	BRACKET FILT	2	
14	KND0A886	SUPPORT MEDIA	2	
15	KHE0A283	MOUNT PCB	1	
16	KKL1M4472K63	FDD1	4	
17	KHG0A109	FOOT RUBBER	4	
18	KKA0A237	MAIN CHASSIS	1	
19	KKC3B077S21	CABINET TEP	1	
20	KKC3A027KX59	PANEL REAR	1	
21	KK02A05C11	PANEL SUB	1	
22	KK02A05C11	CD MECHANISM ASSY	1	
23	KK02A05C11	RUBBER SUPPORT	2	
24	KHG0A140	RUBBER	4	
25	KHG0A140	RUBBER	4	
26	KHG0A140	RUBBER	4	
27	KG02A047	BRIDGE	1	
28				
29				
30				
31				
32		TRANS POWER	1	
33		SUB PCB ASSY	1	
34		MAIN PCB ASSY	1	

S1	KTR041J	SCREW	1	
S2	KTS04BJ	SCREW	4	
S3	KTB318G	SCREW	15	
S4	KTB318J	SCREW	7	
S5	KH02006	SCREW SPECIAL	4	
S6	KTW314J	SCREW	1	
S7	KTW318J	SCREW	7	
S8	KTB446E2	SCREW	4	
S9	KH02008	SCREW SPECIAL	3	
S10	KTB318F	SCREW	4	
S11	KTB318F7	SCREW	3	
S12	KTB3110E7	SCREW	5	
S13	KH02009	SCREW SPECIAL	4	
S14	KTB318J	SCREW	2	

EXPLODED VIEW LIST

REF. NO.	PARTS NO.	DESCRIPTION	REMARKS
1	9A07264600	ORNAMENT, CD	KGX1A221XC11
2	9A07264300	DOOR, CD	KGR1A152K17
3	9A06240500	WINDOW	KGU1A154Y
4	9A06677600	SIDE BAR	KKM1A062C11
5	9A08792700	PANEL, AL	KKM4A054WC11
6	9A08792200	PANEL, MOLD	KGW4A179M9K64
7	9A08792000	WINDOW, SENSOR	KGU1A245A10
8	9A07301300	INDICATOR, POWER	KGL2A120
9	9A07301200	KNOB, POWER	KBT2A387ZK64
10	9A06314300	KNOB, TACT (OPEN/CLOSE)	KBT1A385YK64
11	9A06239700	KNOB, TACT	KBT1A410C13
12	9A06316000	KNOB, TACT	KBT1A386WK64
13	9A05961600	BRACKET, FLT	KMD1A209
14	9A07265400	SUPPORT, MECHA	KMH1A086
15	9A06229100	MOUNT, PCB	KHE1A023
16	9A06315500	FOOT	KKL1A047ZK63
17	9A06229300	CUSHION, FOOT	KHG1A039Z
18	9A07266100	CHASSIS, MAIN	KUA2A137
19	9A06315900	TOP CABINET	KKC3B077S21
20	9A08792600	PANEL, REAR	KKF2A127KK59
21	△ 9A01376900	BUSHING, AC CORD	KHR129
22	△ 9A08152100	POWER CORD, 2.5A 250V	BJA2B043Z
23	9A08788100	CD MECHANISM ASS'Y	BJDWSL2130KCTB
24	9A08788800	CD PICK-UP ASS'Y	HJDKCTB1H
24	9A07264800	SUPPORT	KHG2A163
25	9A06241700	RUBBER, TRANS	KHG1A143
26	9A05326800	RUBBER	KHG1A024
27	9A06224200	BADGE, TEAC	BGB1A047
32	△ 9A08792800	TRANS, POWER	KL5M020ZE
33	9A08793000	CD SUB PCB ASS'Y	KOP11367B
34	9A08792900	CD MAIN PCB ASS'Y	KOP11366BEUR
F101	△ 9A06868100	FUSE	KBA2C0315TLE
	9A08038100	RING, FERRITE	KLZ9W001Z

INCLUDED ACCESSORIES

REF. NO.	PARTS NO.	DESCRIPTION	REMARKS
	9A08524500	OWNER'S MNL, EUR	KQX1A617Z
	9A05935900	CORD, PIN	KJS4M014Y
	9A05936000	CORD, PIN	KJS4N001Y

CD MAIN PCB ASSY

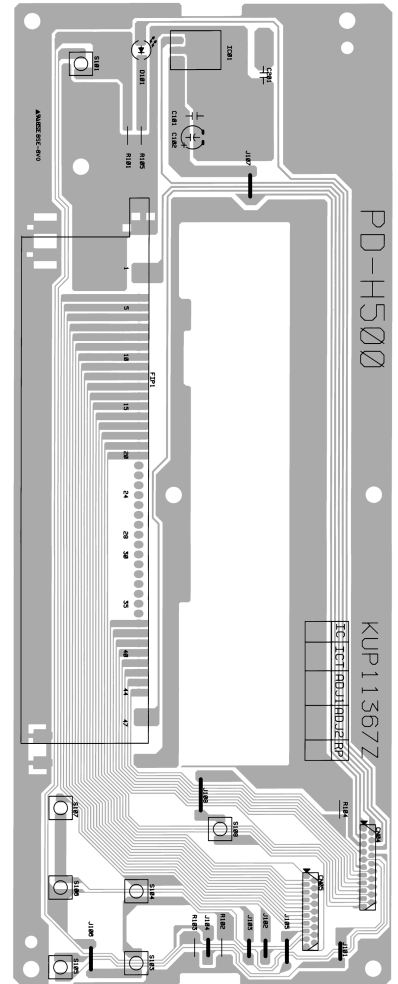
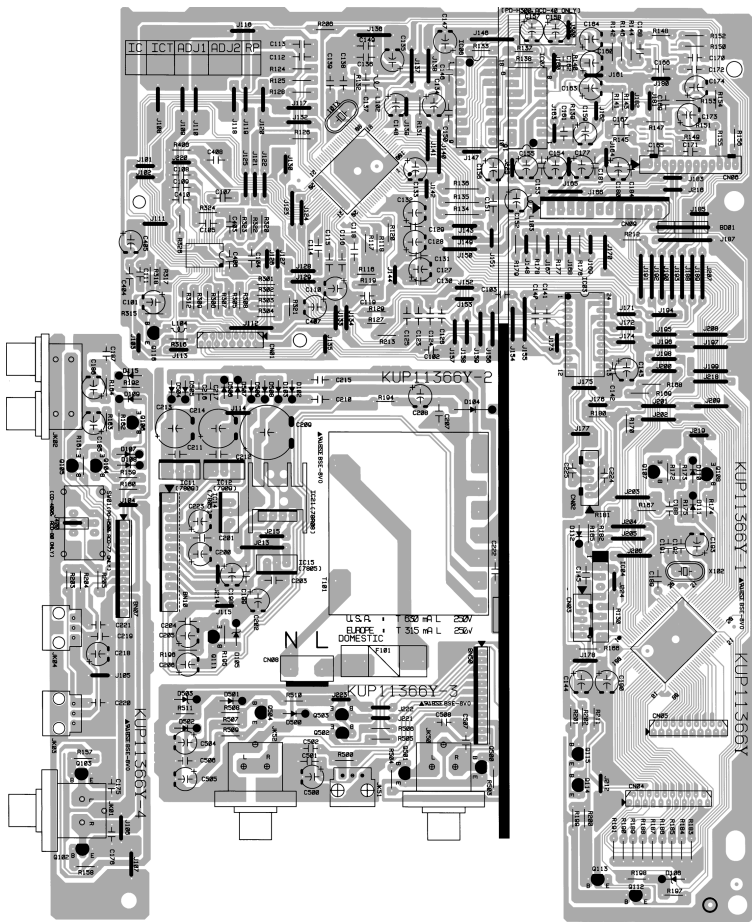
REF. NO.	PARTS NO.	DESCRIPTION
	9A08792900	CD MAIN PCB ASS'Y
	9A08790600	CD MAIN PCB
	9A05961500	PLATE, EARTH
	9A05333500	HEAT SINK
	9A05328200	HOLDER, FUSE
	9A08038100	RING, FERRITE
BD01	9A07050600	BEAD, CORE
C208	△ 9A06764800	C, ELECT 100UF/50V
C209	△ 9A05976300	C, ELECT 2200UF/35V
C213, 214	△ 9A06226700	C, ELECT 1000UF/25V
C223	△ 9A06764900	C, ELECT 100UF/35V
CN01	9A08220300	WAFER, CARD CABLE
CN02	9A05329700	WAFER, MOLEX53014-0610
CN03	9A05356400	WAFER, MOLEX53014-0510
CN04	9A08789600	WAFER, CARD CABLE
CN05	9A08789500	WAFER, C. CABLE
CN06	9A05331000	WAFER, MOLEX 53014-1210
CN08	9A06674400	WAFER
CN09	9A05967800	WAFER
D102, 103	△ 9A05194600	DIODE, 1N4003SRT
D104	△ 9A05194700	DIODE, 1N4003ST
D105	△ 9A06765100	DIODE, ZENER MTZJ27BT
D106	9A06236200	DIODE, ZENER MTZJ6.2BT
D107-111	9A01390500	DIODE, 1N4148MT
D112	9A05194600	DIODE, 1N4003SRT
D115	9A06236200	DIODE, ZENER MTZJ6.2BT
D504-509	△ 9A05194600	DIODE, 1N4003SRT
IC01	9A08788500	IC, TA2150FN
IC02	9A08788700	IC, TC9462F
IC03	9A08788400	IC, TA2092N
IC04	9A08788600	IC, TA7291S
IC05	9A06786000	IC, TMP87PM78F
IC06	9A07263800	IC, SM5841AP
IC07	9A07263700	IC, BV1PCM69P
IC10	9A07343300	IC, NJM2068MD-TE1
IC11	△ 9A08788200	IC, NJM7809FA
IC12	△ 9A08788300	IC, NJM7909FA
IC14, 15	△ 9A05341500	IC, KA7805-ABTU
IC21	△ 9A08790800	IC, KA78R08
IC8, 9	9A07343300	IC, NJM2068MD-TE1
JK01	9A06242100	JACK, LINE IN TERMINAL
JK02	9A06242200	JACK, BOARD
JK03, 04	9A06239100	MODULE, OPTICAL
L102, 103	9A07330400	COIL, AXAIL
L104	9A05356900	COIL, AXAIL 10UH K
Q102, 103	9A05197500	TR, KTD1302T
Q104	9A08791000	TR, KRA107M
Q105	9A08791100	TR, KRC107M
Q106	9A03745100	TR, KSA1175-YTA
Q107	9A08791000	TR, KRA107M

CD MAIN PCB ASSY

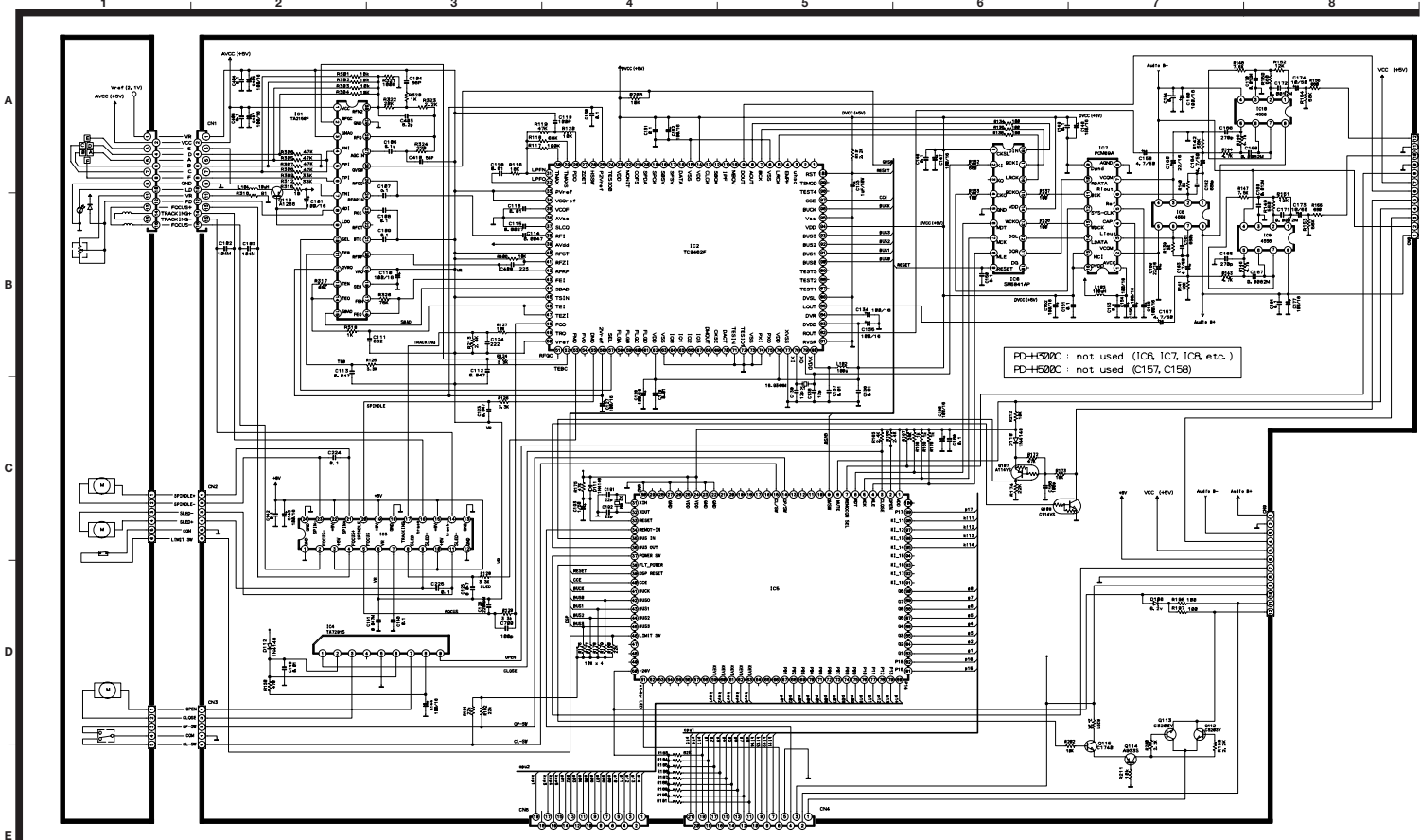
REF. NO.	PARTS NO.	DESCRIPTION
Q108	9A08791100	TR, KRC107M
Q111	9A05196700	TR, KSA916-Y-SHTA
Q112, 113	9A05197400	TR, KTC3203YT
Q114	9A03745100	TR, KSA1175-YTA
Q115	9A03745000	TR, KSC2785-YTA
Q116	9A05895900	TR, KTA1266YT
SW01	9A06244100	SWITCH, SLIDE
T101	△ 9A08792800	TRANS, POWER
X101	9A05193100	CRYSTAL
X102	9A05193000	CRYSTAL

CD SUB PCB ASSY

REF. NO.	PARTS NO.	DESCRIPTION
	9A08793000	CD SUB PCB ASS'Y
	9A08793400	CD SUB PCB
	9A05961600	BRACKET, FLT
CN04	9A08789600	WAFER, CARD CABLE
CN05	9A08789500	WAFER, C. CABLE
D101	9A08147300	LED, RED SLR342VCTB7
FIP1	9A07313300	F. I. P. SVA08MS14
IC01	9A08563600	SENSOR, REMOCON
S101	9A06671200	SW, TACT EVQ21505R
S103-108	9A06671200	SW, TACT EVQ21505R



TEAC SCHEMATIC DIAGRAM PD-H500C/PD-H300C

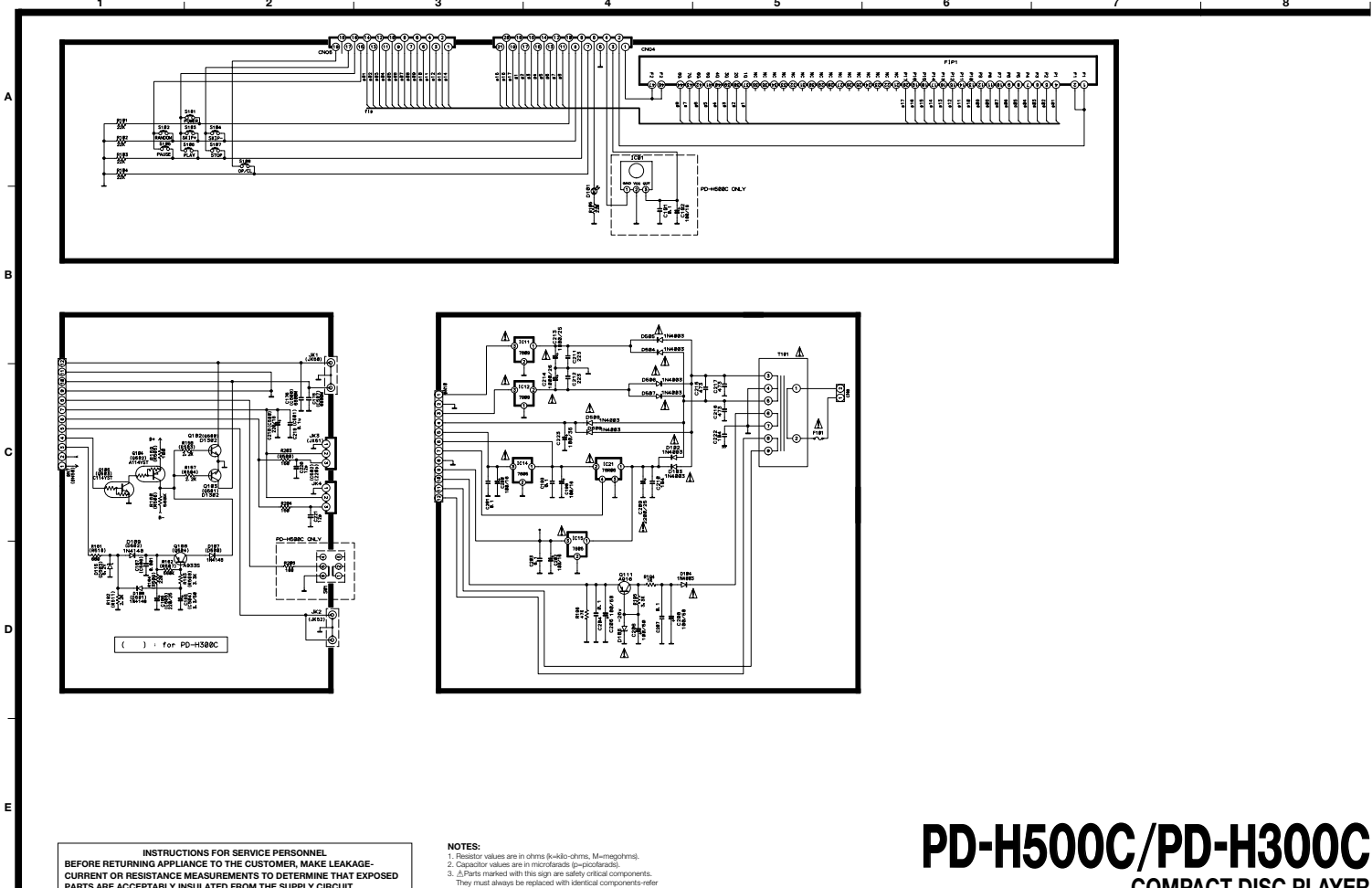


INSTRUCTIONS FOR SERVICE PERSONNEL
 BEFORE RETURNING APPLIANCE TO THE CUSTOMER, MAKE LEAKAGE-CURRENT OR RESISTANCE MEASUREMENTS TO DETERMINE THAT EXPOSED PARTS ARE ACCEPTABLY INSULATED FROM THE SUPPLY CIRCUIT.

NOTES:
 1. Resistor values are in ohms (R-kilo-ohms, M-megohms).
 2. Capacitor values are in microfarads (μ-picofarads).
 3. Parts marked with this sign are safety critical components. They must always be replaced with identical components-refer to the appropriate parts list and ensure exact replacement.

PD-H500C/PD-H300C
 COMPACT DISC PLAYER
 1st Issue; May 2001

TEAC SCHEMATIC DIAGRAM PD-H500C/PD-H300C



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