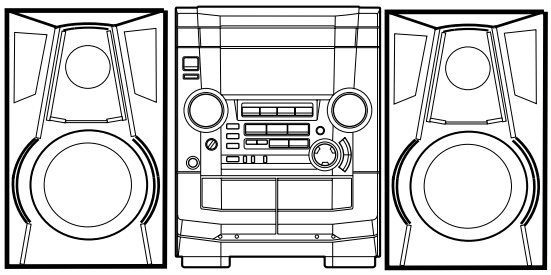
aiwa SERVICE

NSX-BL54 LH
NSX-AJ54 U



SERVICE MANUAL

COMPACT DISC
STEREO SYSTEM

BASIC TAPE MECHANISM : 2ZM-3MK2 YPR4N(LH)
BASIC TAPE MECHANISM : ZZM-3 PR1NF(U)
BASIC CD MECHANISM : AZG-1 ZD8RDC(LH)
BASIC CD MECHANISM : AZG-1 YKZD8RDF(U)

SYSTEM	CD CASSEIVER	SPEAKER	REMOTE CONTROLLER
NSX–BL54	CX–NBL54	SX–WNBL53	RC–ZAS01
NSX–AJ54	CX–NAJ54	SX–WNAJ53	RC–ZAS02

• If requiring information about the CD mechanism, see Service Manual of AZG-1 ZD8RDC (S/M Code No. 09-001-335-3NA)/ AZG-1 YKZD8RDF (S/M Code No. 09-001-335-3N6).

aiwa

S/M Code No. 09-002-429-5N3

DATA

SPECIFICATIONS

Main unit CX-NBL54/CX-NAJ54

FM tuner section

Tuning range	87.5 MHz to 108 MHz
Usable sensitivity (IHF)	13.2 dBf
Antenna terminal	75 ohms (unbalanced)

AM tuner section

Tuning range	530 kHz to 1710 kHz (10 kHz step) 531 kHz to 1602 kHz (9 kHz step)
Usable sensitivity	350 μV/m
Antenna	Loop antenna

Amplifier section

Mid-high frequency amplifier

Power output	Rated: 20 W + 20 W (8 ohms, T.H.D. 1 %, 1 kHz) <LH> Reference : 25 W + 25 W (8 ohms, T.H.D. 10 %, 1 kHz) <LH> 20 W + 20 W (200 Hz - 20kHz, THD less than 1%, 8 ohms) <U>
Total harmonic distortion	0.1 % (10 W, 1 kHz, 8 ohms, DIN AUDIO)

Low frequency amplifier

Power output	Rated: 60 W + 60 W (6 ohms, T.H.D. 1 %, 130 Hz) <LH> Reference : 75 W + 75 W (6 ohms, T.H.D. 10 %, 130 Hz) <LH> 60 W + 60 W (50 Hz - 200 Hz, THD less than 1%, 6 ohms) <U>
Total harmonic distortion	0.1 % (30W, 130 Hz, 6 ohms, DIN AUDIO)
Inputs	VIDEO/AUX: 500 mV
MIC	1.0 mV (10 k ohms) <LH>
Outputs	SPEAKERS HIGH FREQ: accept speakers of 8 ohms or more SPEAKERS LOW FREQ: accept speakers of 6 ohms or more SURROUND SPEAKERS: accept speakers of 8 ohms to 16 ohms PHONES (stereo jack): accepts headphones of 32 ohms or more

Cassette deck section

Track format	4 tracks, 2 channels stereo
Frequency response	50 Hz – 15000 Hz
Recording system	AC bias
Heads	Deck 1: Playback head x 1 Deck 2: Recording/playback head x 1, erase head x 1

Compact disc player section

Laser	Semiconductor laser (λ = 780 nm)
D-A converter	1 bit dual
Signal-to-noise ratio	85 dB (1 kHz, 0 dB)
Harmonic distortion	0.05 % (1 kHz, 0 dB)
Wow and flutter	Unmeasurable

General

Power requirements	120 V/220 – 230 V/240 V AC, switchable 50/60 Hz <LH> 120 V AC, 60 Hz <U>
Power consumption	130 W <LH>, 110 W <U>
Power consumption in standby mode	If the power-economizing mode is ECO OFF: 20 W If the power-economizing mode is ECO ON or ECO AUTO: 0.9 W
Dimensions of main unit (W x H x D)	260 x 326 x 346 mm (10 1/4 x 12 7/8 x 13 5/8 in.)
Weight of main unit	9.0 kg <LH> 8.0 kg (17 lbs 10 oz.) <U>

Speaker system SX-WNBL53/SX-WNAJ53

Speaker system	3 way, Built-in subwoofer (magnetic shielded type)
Speaker units	Subwoofer: 160 mm (6 3/8 in.) cone type Full range: 100 mm (4 in.)cone type Super tweeter: 20 mm (13/16 in.) ceramic type
Impedance	6 ohms/8 ohms
Sensitvity	87 dB/W/m
Dimensions (W x H x D)	230 x 324 x 282 mm (9 1/8 x 12 7/8 x 11 1/8 in.)
Weight	4.8 kg (10 lbs 9 oz)

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ACCESSORIES LIST

DESCRIPTIONで判断できない物は "REFERENCE NAME LIST" を参照してください。
If can't understand for Description please kindly refer to "REFERENCE NAME LIST".

REF. NO	PART NO.	KANRI NO.	DESCRIPTION
1	8A-NFJ-902-010		IB,LH(ESP)B<LH>
1	8A-NFJ-913-010		IB,U(ESF)M<U>
2	8Z-NF8-702-010		RC UNIT,RC-ZAS01<LH>
2	8Z-NF9-702-010		RC UNIT,ZAS02<U>
3	87-006-268-010		ANT,LOOP AM<U>
3	87-A90-030-010		ANT,LOOP AM-NC C<LH>
4	87-043-115-010		FEEDER-ANT,FM
⚠ 5	87-A91-017-010		PLUG,CONVERSION JT-0476<LH>

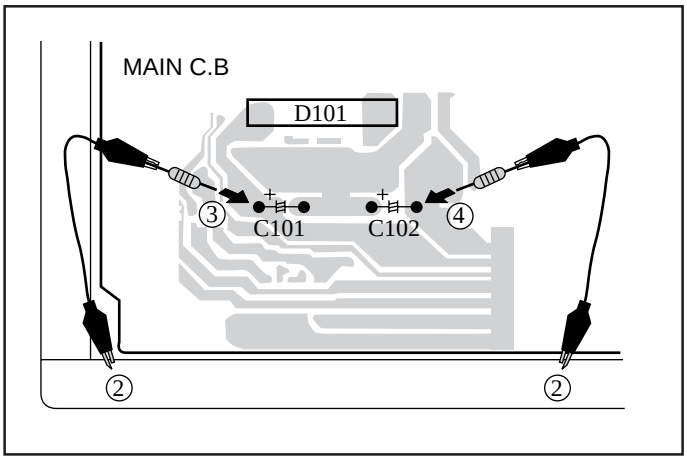
NOTE ON BEFORE STARTING REPAIR

1. Forced discharge of electrolytic capacitor of power supply block

When repair is going to be attempted in the set that uses relay circuit in the power supply block, electric potential is kept charged across the electrolytic capacitors (C101, 102) even though AC power cord is removed. If repair is attempted in this condition, secondary defect can occur.
In order to prevent the secondary trouble, perform the following measures before starting repair work.

Discharge procedure

① Remove the AC power cord.
② Connect a discharging resistor at an end of lead wire that has clips at both ends. Connect the other end of the lead wire to metal chassis.
③ Contact the other end of the discharging resistor to the positive (+) side (+VH) of C101. (For two seconds)
④ Contact the same end of the discharging resistor as step **3** to the negative (-) side (-VH) of C102 in the same way. (For two seconds)
⑤ Check that voltage across C101 and C102 has decreased to 1 V or less using a multimeter or an oscilloscope.



Select a discharging resistor referring to the following table.

Charging voltage (V) (C101, 102)	Discharging resistor (Ω)	Rated power (W)	Parts number
25-48	100	3	87-A00-247-090
49-140	220	5	87-A00-232-090

Note: The reference numbers (C101, C102) of the electrolytic capacitors can change depending on the models. Be sure to check the reference numbers of the charging capacitors on schematic diagram before starting the discharging work.

2. Check items before exchanging the MICROCOMPUTER

Be sure to check the following items before exchanging the MICROCOMPUTER. Exchange the MICROCOMPUTER after confirming that the MICROCOMPUTER is surely defective.

2-1. Regarding the HOLD terminal of the MICROCOMPUTER

When the HOLD terminal (INPUT) of the MICROCOMPUTER is "H", the MICROCOMPUTER is judged to be operating correctly. When this terminal is "L", the main power cannot be turned on. Therefore, be sure to check the terminal voltage of the HOLD terminal before exchange.
When the MICROCOMPUTER is not defective, the HOLD terminal can also go "L" when the POWER AMPLIFIER has any abnormalities that triggers the abnormality detection circuit on the MAIN C. B. that sets the HOLD terminal to "L".

- Good or no good judgement of the MICROCOMPUTER

① Turn on the AC main power.
② Confirm that the main power is turned on and the HOLD terminal of the MICROCOMPUTER keeps the "H" level or not.
③ When the HOLD terminal is "L" level, the abnormality detection circuit is judged to be working correctly and the MICROCOMPUTER is judged to be good.

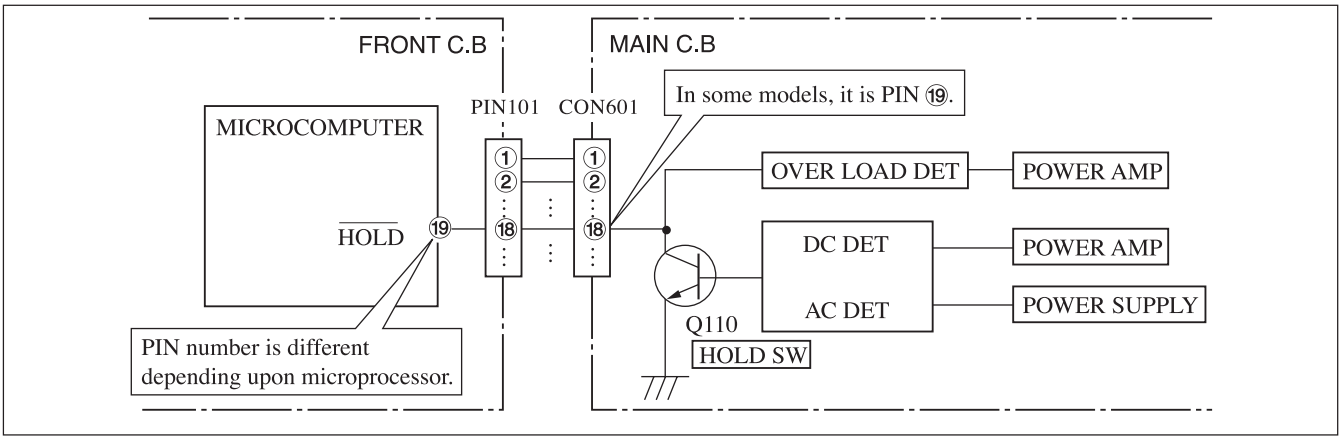


Fig-2-1

In such a case, check also if the POWER AMPLIFIER circuit or power supply circuit has any abnormalities or not.

2-2. Regarding reset

There are cases that the machine does not work correctly because the MICROCOMPUTER is not reset even though the AC power cord is re-inserted, or the software reset (pressing the STOP key + POWER key) is performed.
When the above described phenomenon occurs, it can lead to wrong judgement as if the MICROCOMPUTER is defective and to exchange the MICROCOMPUTER. In such a case, perform the forced-reset by the following procedure and check good or no good of the MICROCOMPUTER.

① Remove the AC power cord.

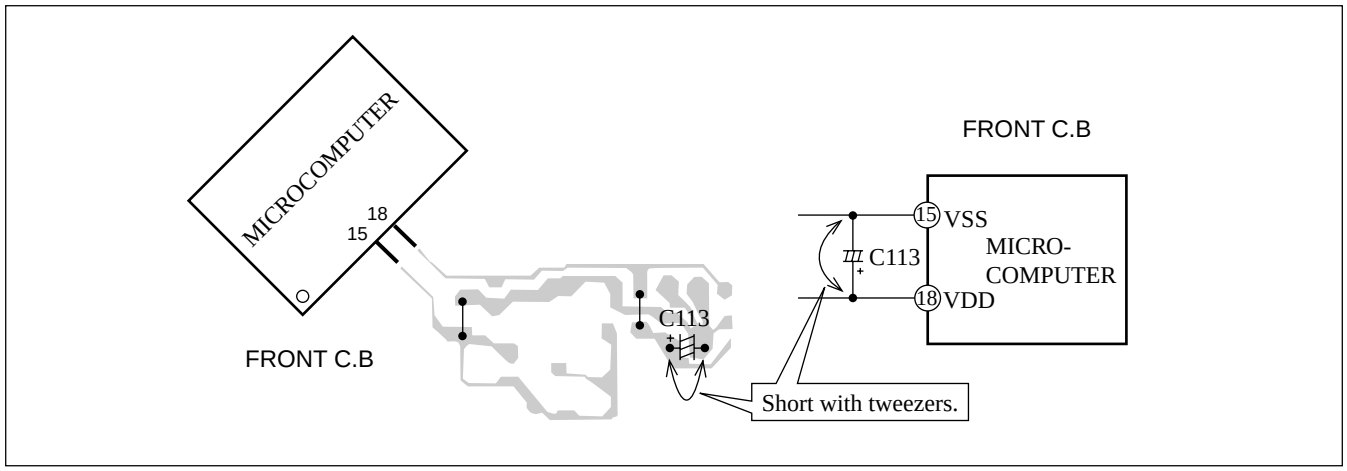


Fig-2-2

② Short both ends of the electrolytic capacitor C113 that is connected to VDD of the MICROCOMPUTER with tweezers.
③ Connect the AC power cord again. If the MICROCOMPUTER returns to the normal operation, the MICROCOMPUTER is good.

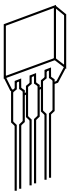
Note: The reference number or MICROCOMPUTER pin number of transistor (Q110) and electrolytic capacitor (C113) can change depending on the models. Be sure to check the reference numbers on schematic diagram before starting the discharging work.

2-3. Confirmation of soldering state of MICROCOMPUTER

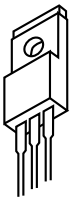
Check the soldering state of the MICROCOMPUTER in addition to the above described procedures. Be sure to exchange the MICROCOMPUTER after surely confirming that the trouble is not caused by poor soldering but the MICROCOMPUTER itself.

TRANSISTOR ILLUSTRATION

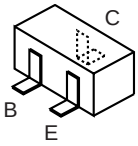
2SC3331
CD1585
CSA952
CSC4115
KTA1266
KTC3198



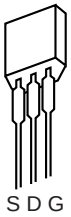
2SA933S
DTC114ES
KTC3199



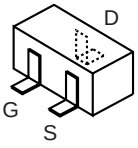
2SB1370



2SA1235
2SC2714
2SC3052
CMBT5401
CMBT5551
KRA102S
KRA107S
KRC102S
RT1N441C
RT1P141C



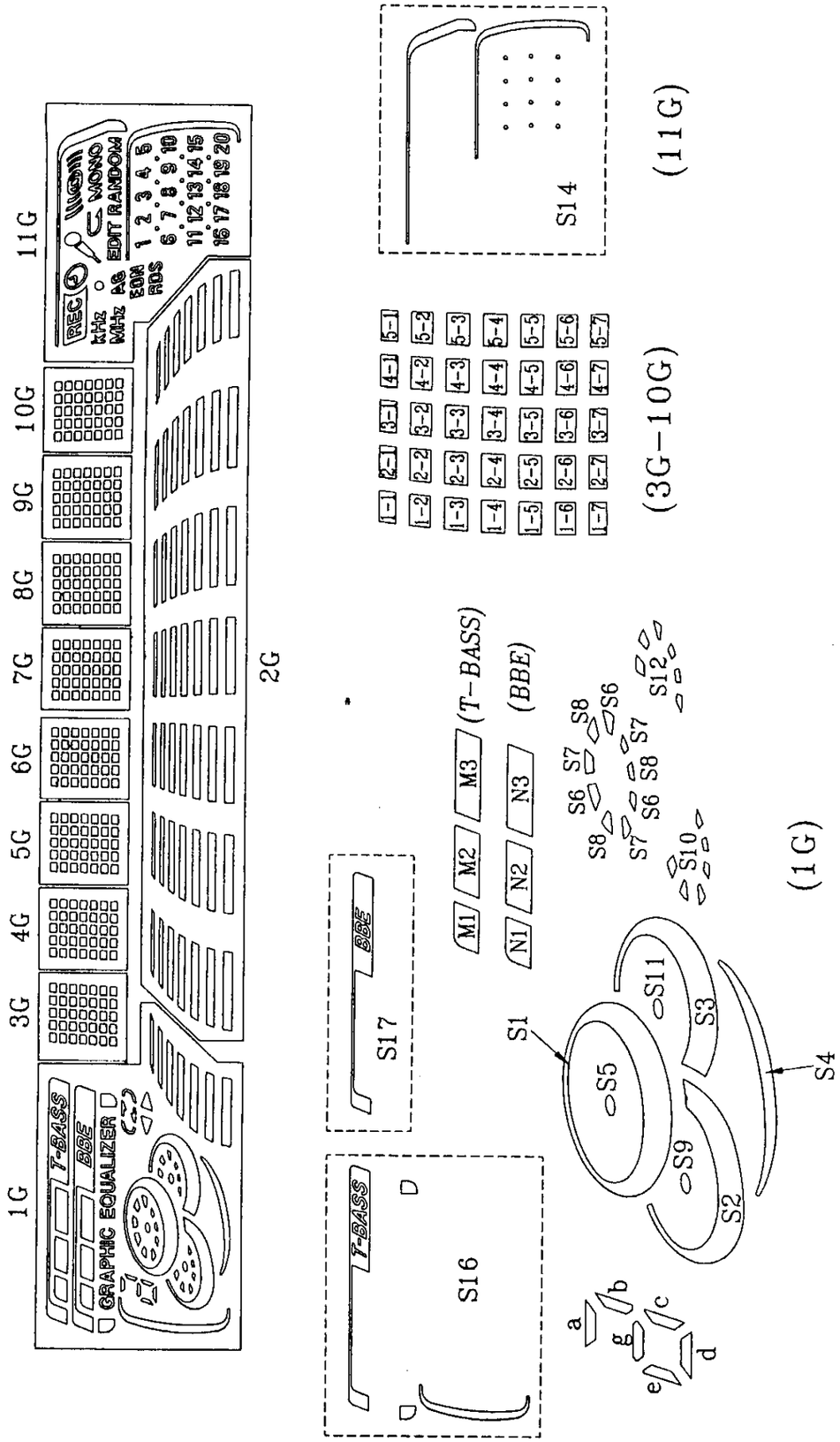
2SJ460
2SK2541

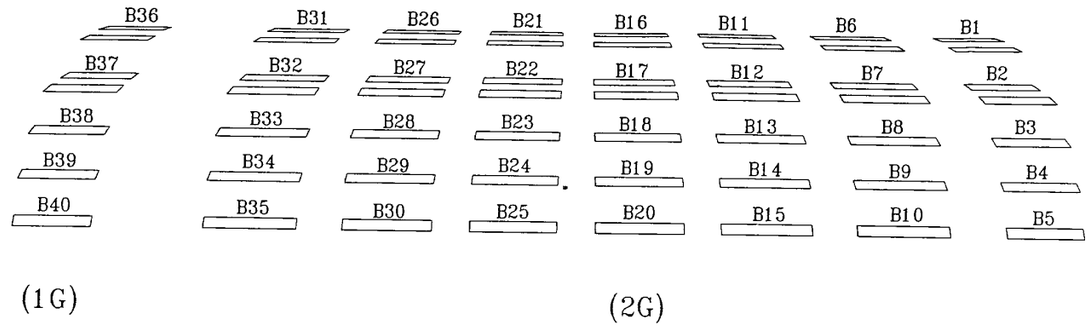


2SJ461
2SK2158

FL (HNA-11MM30) GRID ASSIGNMENT/ANODE CONNECTION

GRID ASSIGNMENT



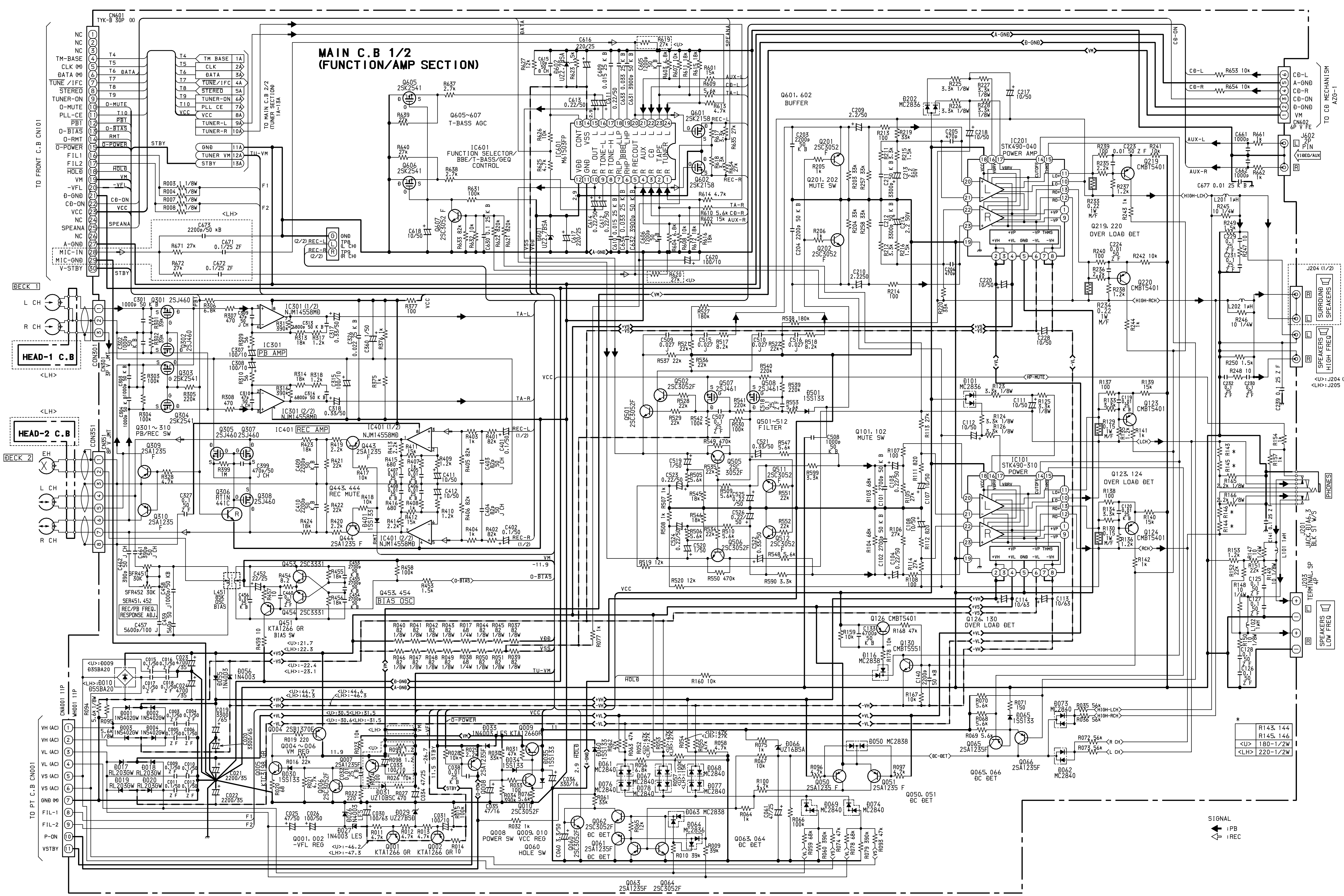


ANODE CONNECTION

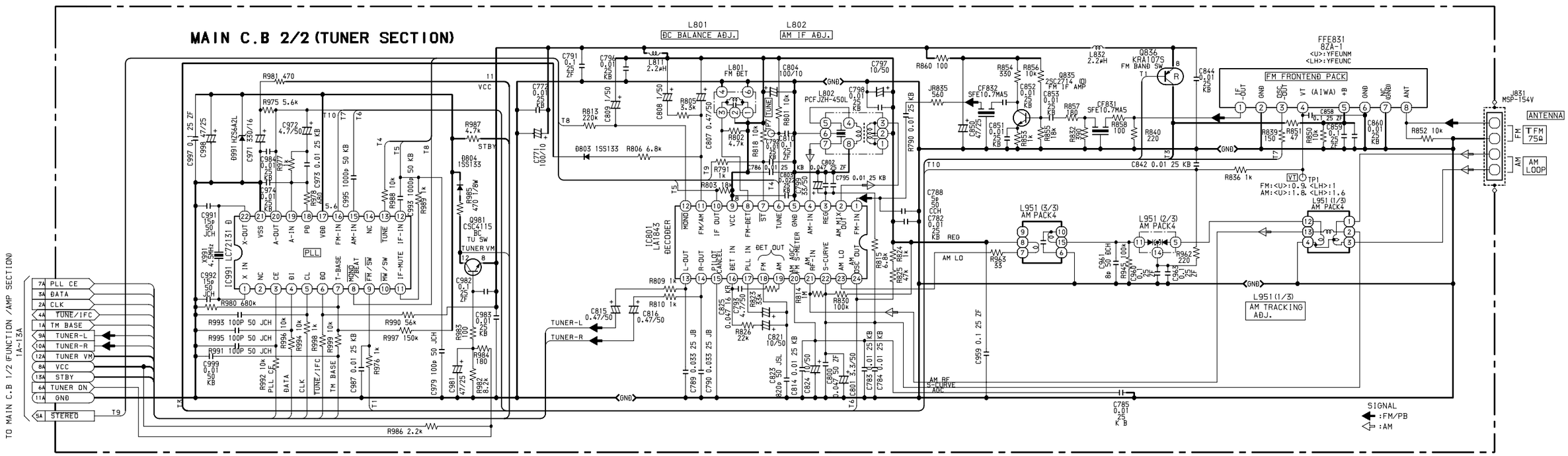
	1G	2G	3G-10G	11G
P1	S17	B35	1-1	
P2	N1	B30	2-1	MONO
P3	N2	B25	3-1	RANDOM
P4	N3	B20	4-1	
P5	GRAPHIC EQUALIZER	B15	5-1	EDIT
P6		B10	1-2	
P7		B5	2-2	REC
P8		B34	3-2	kHz
P9		B29	4-2	MHz
P10		B24	5-2	○
P11	S4	B19	1-3	AS
P12	S2	B14	2-3	EON
P13	S10	B9	3-3	RDS
P14	S9	B4	4-3	S14
P15	S3	B33	5-3	20
P16	S12	B28	1-4	19
P17	S11	B23	2-4	18
P18	S1	B18	3-4	17

	1G	2G	3G-10G	11G
P19	S6	B13	4-4	16
P20	S7	B8	5-4	15
P21	S8	B3	1-5	14
P22	S5	B32	2-5	13
P23	S16	B27	3-5	12
P24	M1	B22	4-5	11
P25	M2	B17	5-5	10
P26	M3	B12	1-6	9
P27	e	B7	2-6	8
P28	a,g,d	B2	3-6	7
P29	b	B31	4-6	6
P30	c	B26	5-6	5
P31	B40	B21	1-7	4
P32	B39	B16	2-7	3
P33	B38	B11	3-7	2
P34	B37	B6	4-7	1
P35	B36	B1	5-7	

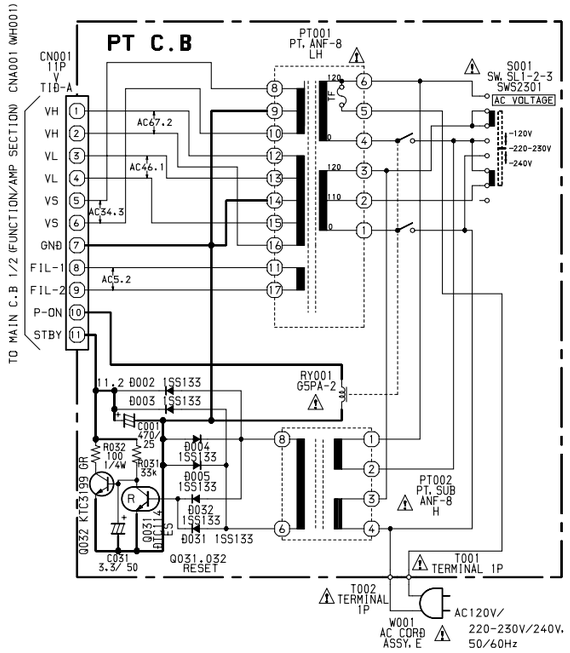
SCHEMATIC DIAGRAM-1 (FUNCTION/AM SECTION)



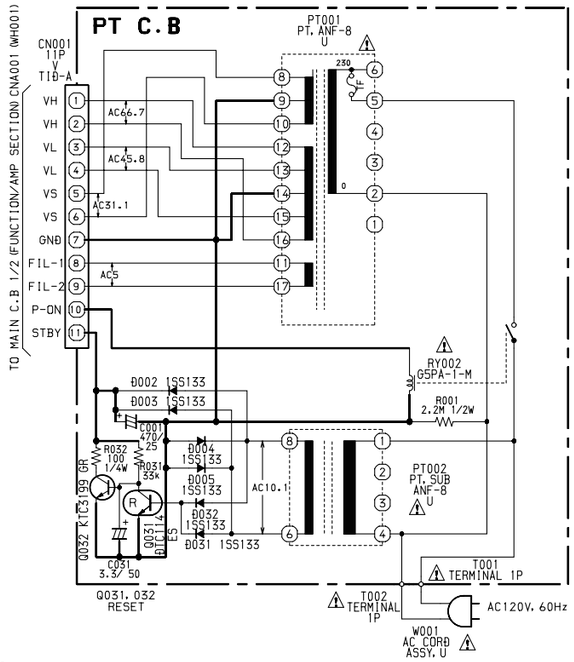
SCHEMATIC DIAGRAM-2 (TUNER SECTION)



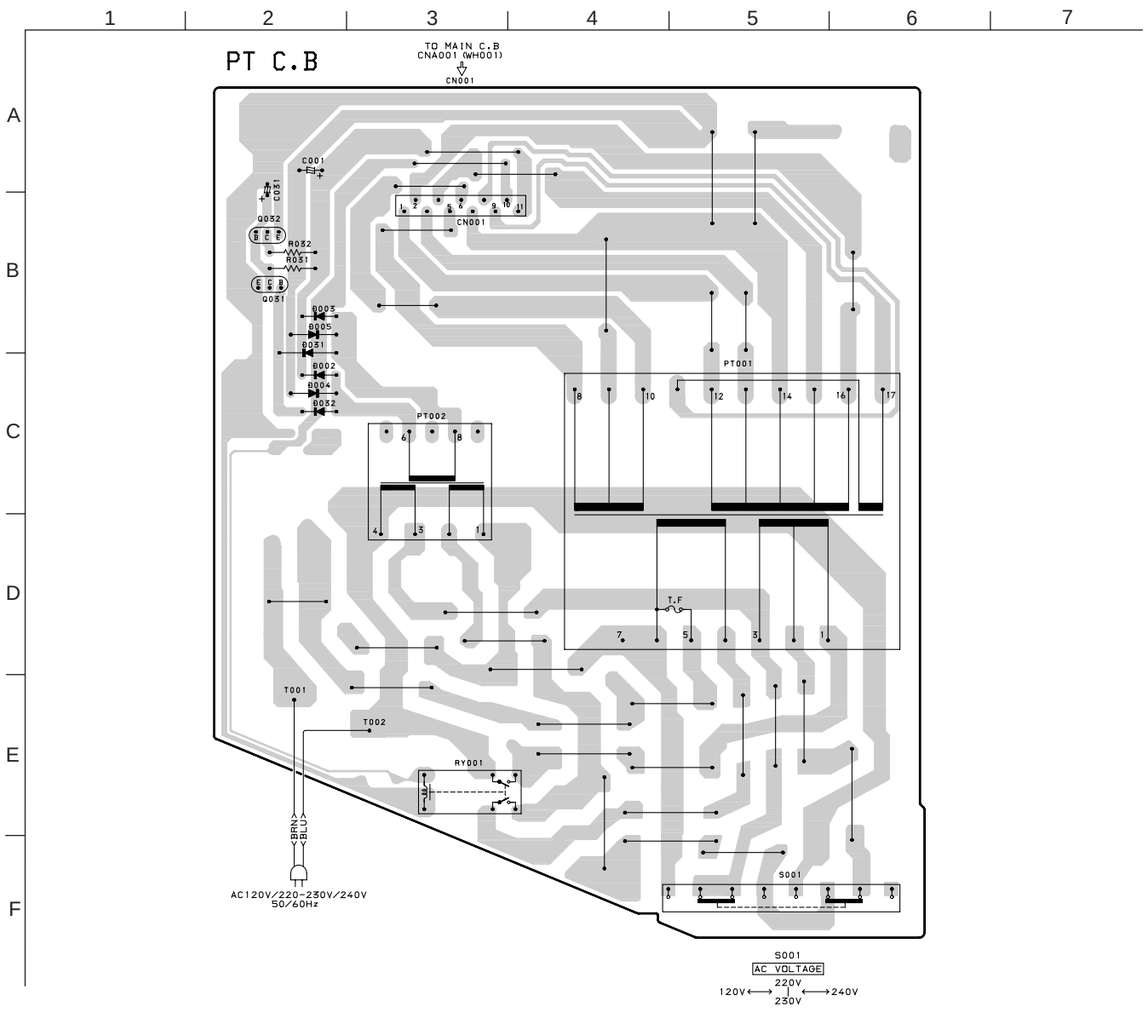
SCHEMATIC DIAGRAM-3 (PT SECTION) <LH>



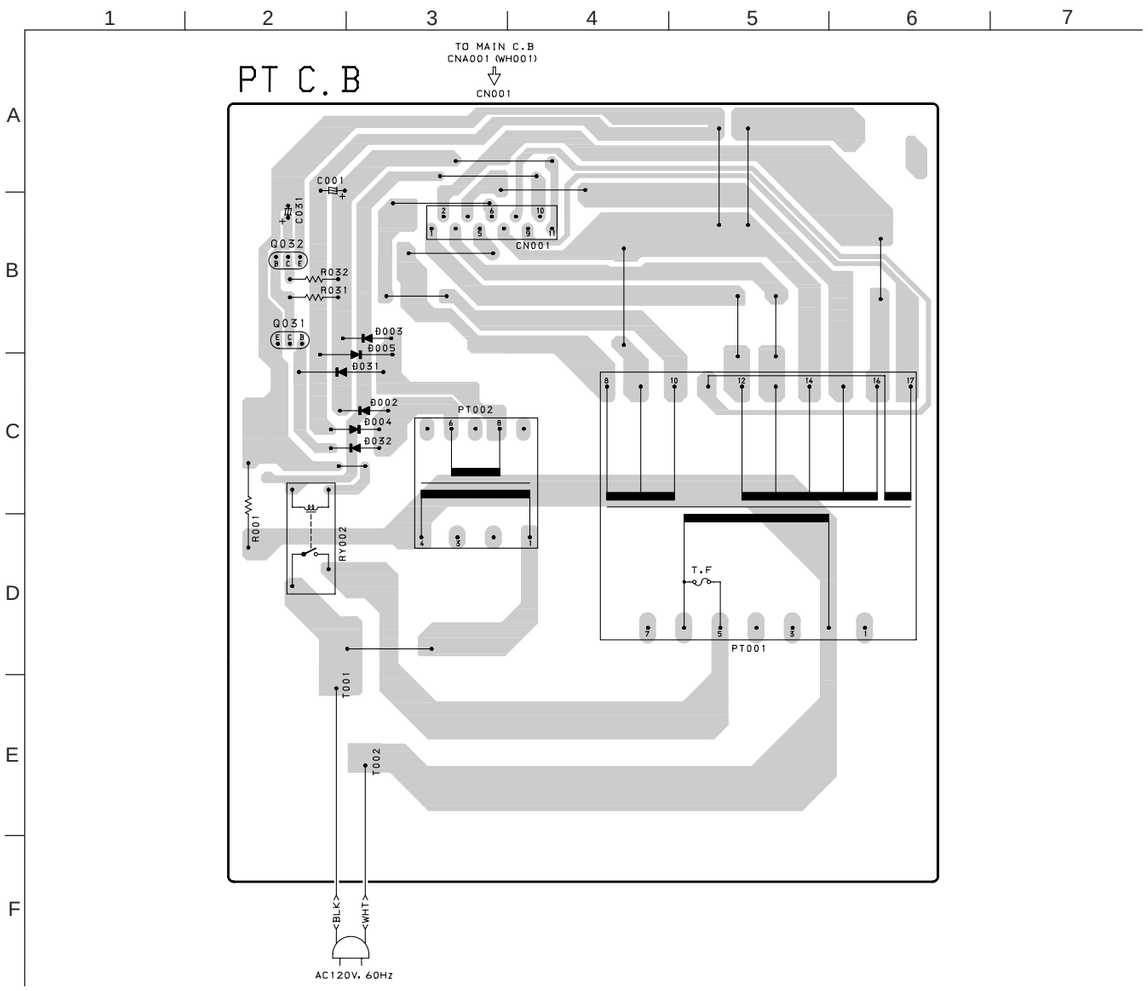
SCHEMATIC DIAGRAM-4 (PT SECTION) <U>



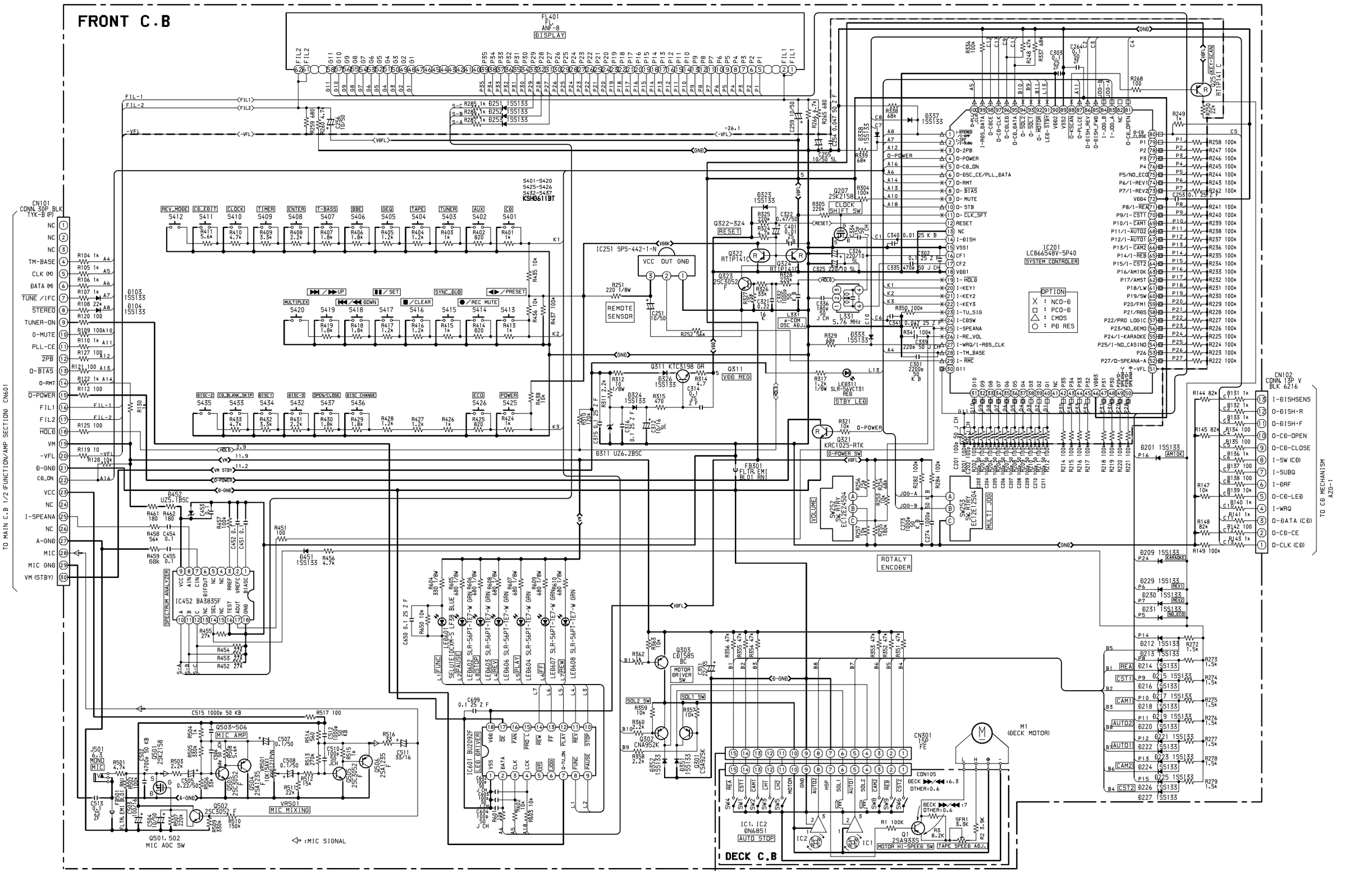
WIRING-2 (PT C.B) <LH>



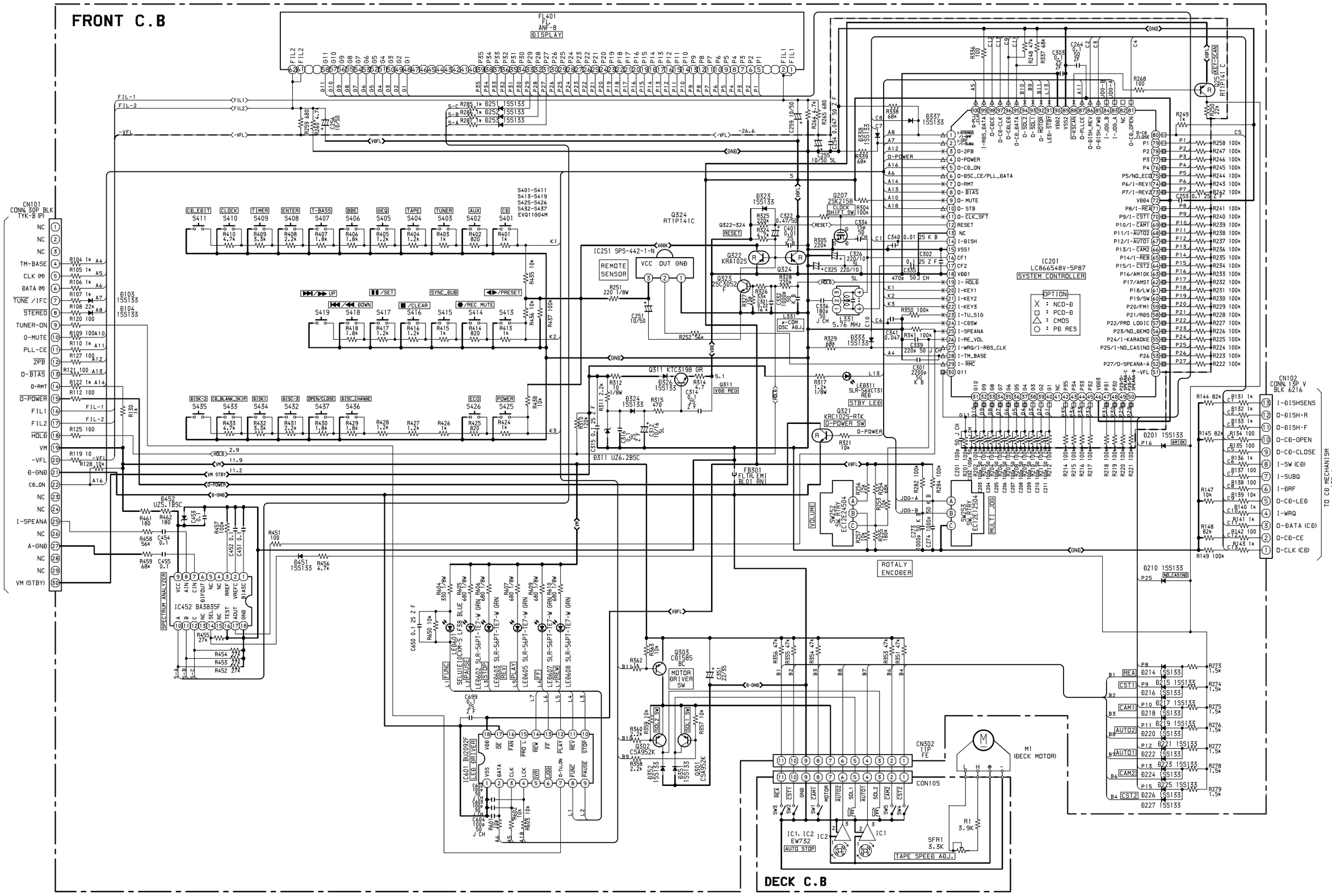
WIRING-3 (PT C.B) <U>



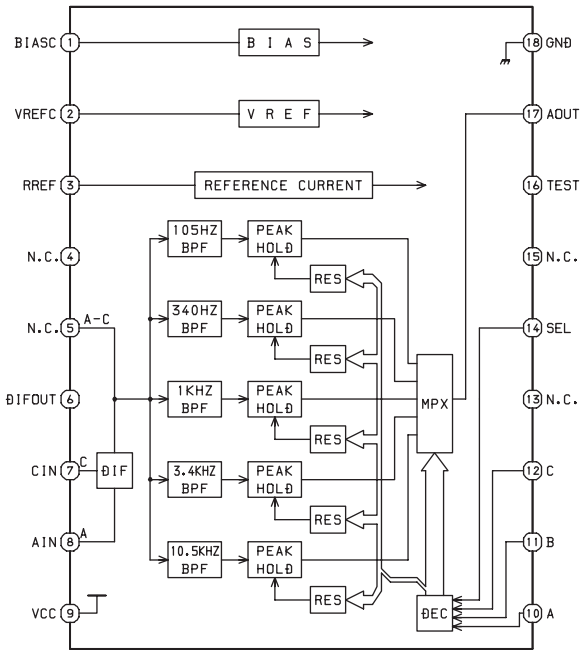
SCHEMATIC DIAGRAM-5 (FRONT SECTION) <LH>



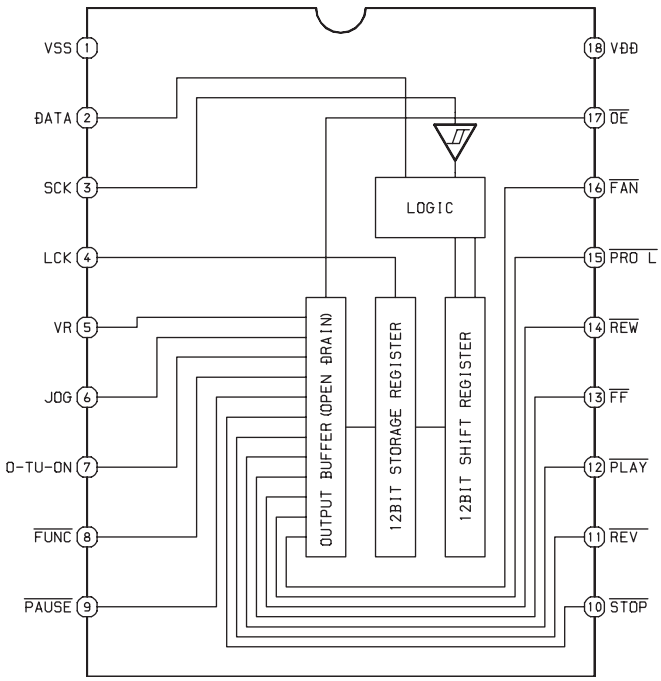
SCHEMATIC DIAGRAM-6 (FRONT SECTION) <U>



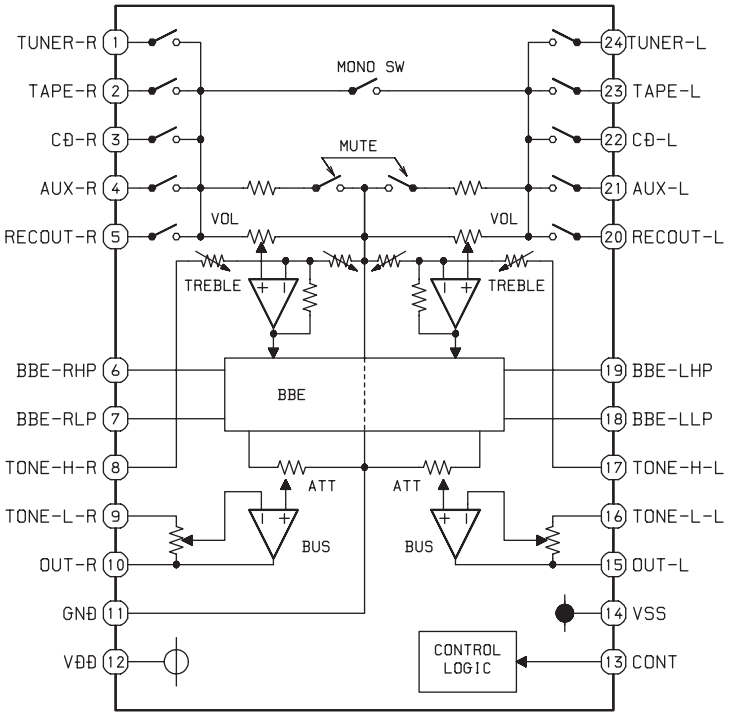
IC, BA3835F



IC, BU2092F



IC, M61503FP

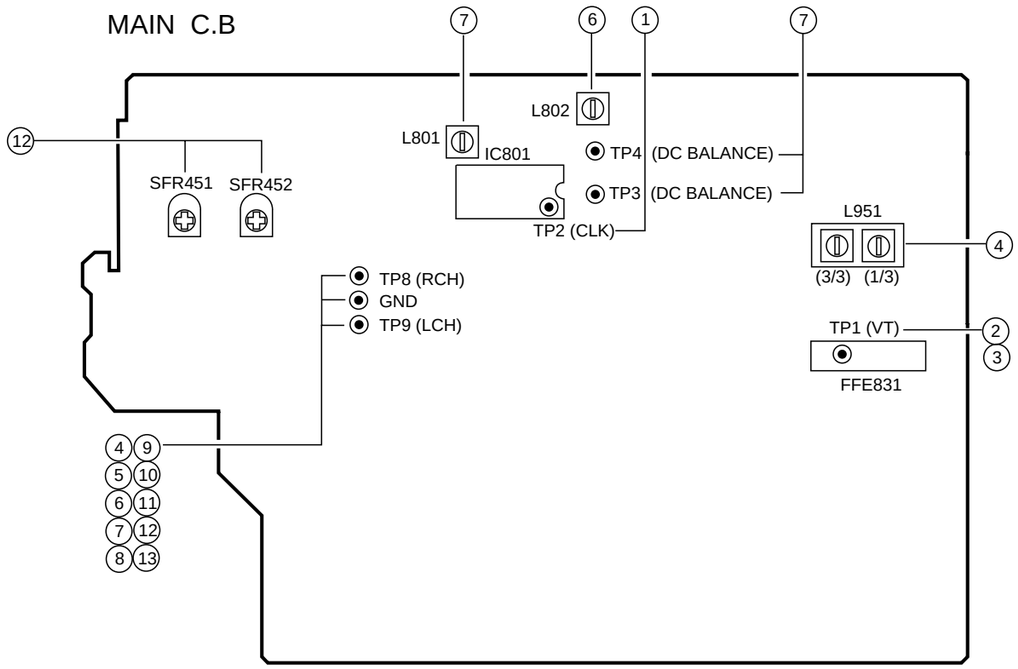


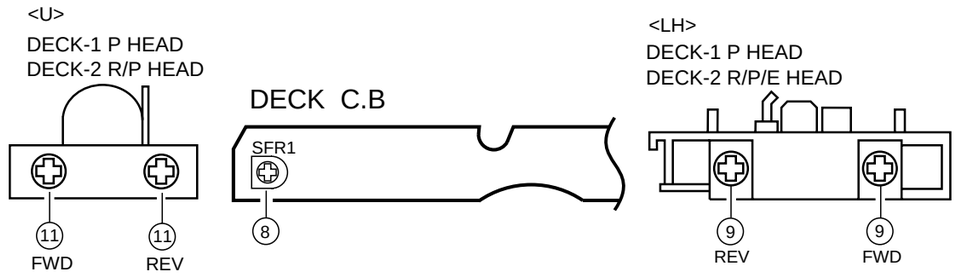
IC DESCRIPTION

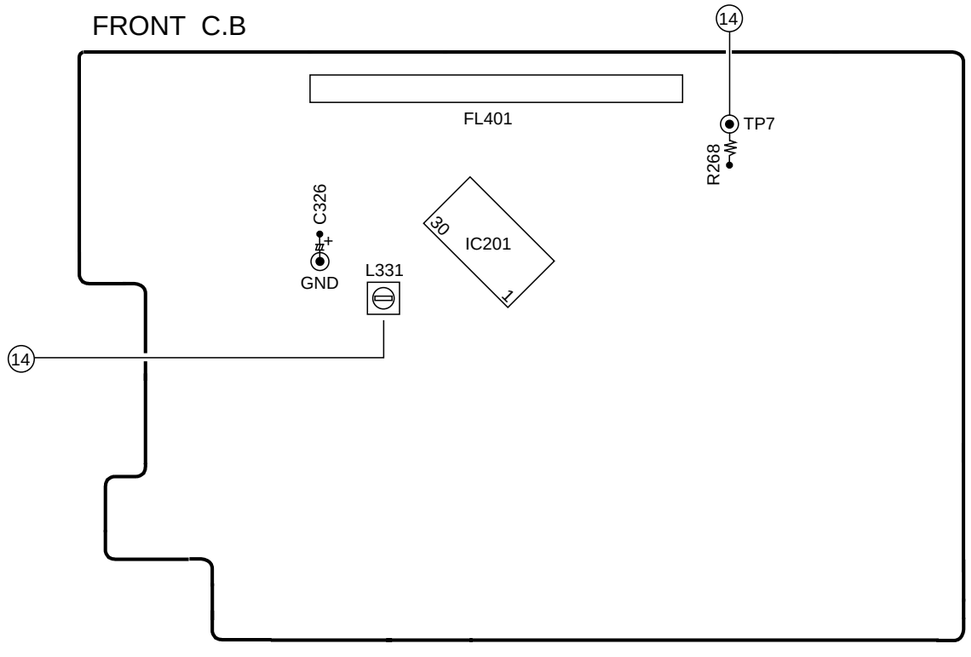
IC, LC866548V-5P87 <U>, LC866548V-5P40 <LH>

Pin No.	Pin Name	I/O	Description
1	I-STEREO/I-DRF	I	Stereo detected input/CD DRF input
2	I-IFC/I-SUBQ	I	Tune IF count serial data input/CD SUBQ input
3	O-2PB	O	Deck 2 playback switch output
4	O-POWER	O	System power supply ON/OFF output
5	O-CD-ON	O	CD power ON/OFF output
6	O-PLL_DATA	O	LED driver, Tuner IC, Function IC data output
7	O-RMT	O	Deck 2 REC MUTE output
8	O-BIAS	O	Deck 2 bias ON/OFF output
9	O-MUTE	O	System mute ON/OFF output
10	O-STB	O	Latch strobe output for LED driver IC
11	O-CLK_SFT	O	Micon clock shift output
12	RESET	I	System reset
13	NC	–	Not connected
14	I-DISH	I	CD turntable photo sensor A/D converter input
15	VSS1	–	GND
16	CF1	–	5.76 MHz oscillator circuit
17	CF2	–	5.76 MHz oscillator circuit
18	VDD1	–	Power supply input
19	I-HOLD	I	Power failure detected input
20	I-KEY1	I	KEY input (A/D)
21	I-KEY2	I	KEY input (A/D)
22	I-KEY3	I	KEY input (A/D)
23	I-TU_SIG	I	Tuner signal input
24	I-CDSW	I	CD mechanical switch A/D converter input
25	I-SPEANA	I	A/D input for spectrum analyzer display
26	I-RE_VOL	I	Rotary encoder input (VOL)
27	I-WRQ/I-RDS_CLK	I	CD WRQ input/Tuner RDS clock input
28	I-TM_BASE	I	Reference clock input for timer watch
29	I-RMC	I	System remotecontrol signal input
30 ~ 40	G11 ~ G1	O	FL GRID output G11 ~ G1
41	NC	–	Not connected
42 ~ 45	P35 ~ P32	O	FL SEGMENT output P35 ~ P32
46	VDD3	–	Power supply input
47 ~ 48	P31 ~ P30	O	FL SEGMENT output P31 ~ P30
49	P29/O-SPEANA-C	O	FL SEGMENT output P29/Spectrum analyzer band switching output
50	P28/O-SPEANA-B	O	FL SEGMENT output P28/Spectrum analyzer band switching output
51	VFL	–	Power supply input for FL display
52	P27/O-SPEANA-A	O	FL SEGMENT output P27/Spectrum analyzer band switch output
53	P26	O	FL SEGMENT output P26
54	P25/I-NO_CASINO	I/O	FL SEGMENT output P25/NO CASINO DEMO input to diode
55	P24/I-KARAOKE	I/O	FL SEGMENT output P24/KARAOKE input to diode
56	P23/NO_DEMO	I/O	FL SEGMENT output P23/NO DEMO input to diode

Pin No.	Pin Name	I/O	Description
57	P22/PRO LOGIC	I/O	FL SEGMENT output P22/PROLOGIC input to diode (not used)
58	P21/RDS	I/O	FL SEGMENT output P21/RDS input to diode
59	P20/FM1	I/O	FL SEGMENT output P20/FM1 input to diode
60	P19/SW	I/O	FL SEGMENT output P19/SW input to diode
61	P18/LW	I/O	FL SEGMENT output P18/LW input to diode
62	P17/AMST	I/O	FL SEGMENT output P17/AMST input to diode
63	P16/AM10K	I/O	FL SEGMENT output P16/AM10K input to diode
64	P15/I-$\overline{\text{CST2}}$	I/O	FL SEGMENT output P15/DECK2 cassette detect switch data input
65	P14/I-$\overline{\text{REB}}$	I/O	FL SEGMENT output P14/DECK2 side-B record OK switch data input
66	P13/I-$\overline{\text{CAM2}}$	I/O	FL SEGMENT output P13/DECK2 CAM switch signal input
67	P12/I-$\overline{\text{AUTO1}}$	I/O	FL SEGMENT output P12/DECK1 AUTO STOP signal input
68	P11/I-$\overline{\text{AUTO2}}$	I/O	FL SEGMENT output P11/DECK2 AUTO STOP signal input
69	P10/I-$\overline{\text{CAM1}}$	I/O	FL SEGMENT output P10/DECK1 CAM switch data input
70	P9/I-$\overline{\text{CST1}}$	I/O	FL SEGMENT output P9/DECK1 cassette detect switch data input
71	P8/I-$\overline{\text{REA}}$	I/O	FL SEGMENT output P8/DECK2 side A record OK switch data input
72	VDD4	–	Power supply input
73	P7/I-REV2	I/O	FL SEGMENT output P7/DECK2 REVERSE mode input to diode
74	P6/I-REV1	I/O	FL SEGMENT output P6/DECK1 REVERSE mode input to diode
75	P5/NO_ECO	I/O	FL SEGMENT output P5/NO ECO MODE input to diode
76 ~ 79	P4 ~ P1	O	FL SEGMENT output P4 ~ P1
80	O-CD CLOSE	O	CD TRAY CLOSE data output
81	O-CD OPEN	O	CD TRAY OPEN data output
82	NC	–	Not connected
83	I-JOG_A	I	Rotary encoder A input (JOG)
84	I-JOG_B	I	Rotary encoder B input (JOG)
85	O-DISH_FWD	O	CD turntable forward rotation output
86	O-DISH_REV	O	CD turntble reverse rotation output
87	O-PLL_CE	O	PLL IC chip enable output
88	O-$\overline{\text{KSCAN}}$	O	Switch SCAN timing output
89	VSS2	–	GND
90	VDD2	–	Power supply input
91	LED-$\overline{\text{STBY}}$	O	STAND BY LED (Echo mode) ouput
92	O-$\overline{\text{MOTOR}}$	O	DECK MOTOR $\overline{\text{ON}}$/OFF output
93	O-$\overline{\text{SOL1}}$	O	DECK1 soleroid ouput
94	O-$\overline{\text{SOL2}}$	O	DECK2 soleroid ouput
95	O-CD-DATA	O	CD DATA output
96	O-CD-LED	O	CD LED output
97	O-CD CLK	O	CD clock output
98	O-CD CE	O	CD chip enable output
99	I-RDS_DATA	I	RDS data input
100	O-PLL_CLK	O	PLL IC CLOCK output







< TUNER SECTION >

1. Clock frequency Check
   Settings : • Test point : TP2
   Method : Set to AM 1710kHz and check that the test point is 2160kHz ± 45Hz.

2. AM VT Check
   Settings : • Test point : TP1 (VT)
   Method : Set to AM 1710kHz, 530kHz and check that the test point is less than 8.5V (1710kHz) and more than 0.6V (530kHz).

3. FM VT Check
   Settings : • Test point : TP1 (VT)
   Method : Set to FM 87.5MHz, 108.0MHz and check that the test point is more than 0.5V (87.5MHz) and less than 8.0V (108.0MHz).

4. AM Tracking Adjustment
   Settings : • Test point : TP8(Lch), TP9(Rch)
   • Adjustment location :
   L951(1/3) 1000kHz
   Method : Set to AM 1000kHz and adjust L951(1/3) so that the level at the test point becomes maximum.

5. FM Tracking Check
   Settings : • Test point : TP8(Lch), TP9(Rch)
   Method : Set to FM 98.0MHz and check that the test point is less than 9dBμV.

6. AM IF Adjustment
   Settings : • Test point : TP8(Lch), TP9(Rch)
   • Adjustment location :
   L802 ..... 1000kHz

7. DC Balance / Mono Distortion Adjustment
   Settings : • Test point : TP3, TP4 (DC Balance)
   : TP8(Lch), TP9(Rch) (Distortion)
   • Adjustment location : L801
   • Input level : 60dBμV
   Method : Set to FM 98.0MHz and adjust L801 so that the voltage between TP3 and TP4 becomes 0V ± 0.3V. Next, check that the distortion is less than 1.3%.

< DECK SECTION >

8. Tape Speed Adjustment (DECK 2)
   Settings : • Test tape : TTA–100
   • Test point : TP8(Lch), TP9(Rch)
   • Adjustment location : SFR1
   Method : Play back the test tape and adjust SFR1 so that the frequency counter reads 3000Hz ± 5Hz and ±45Hz (REV) with respect to forward speed.

9. Head Azimuth Adjustment (DECK 1, DECK 2)
   Settings : • Test tape : TTA–330
   • Test point : TP8(Lch), TP9(Rch)
   • Adjustment location : Head azimuth adjustment screw
   Method : Play back (FWD) the 8kHz signal of the test tape and adjust screw so that the output becomes maximum. Next, perform on REV PLAY mode.

10. PB Frequency Response Check (DECK 1, DECK 2)
    Settings : • Test tape : TTA–300
    • Test point :TP8(Lch), TP9(Rch)
    Method : Play back the 315Hz and 8kHz signals of the test tape and check that the output ratio of the 8kHz signal with respect to that of the 315Hz signal is within 5dB.

11. PB Sensitivity Check (DECK 1, DECK 2)
    Settings : • Test tape : TTA–200
    • Test point : TP8(Lch), TP9(Rch)
    Method : Play back the test tape and check that the output level of the test point is 140mV ± 3dB.

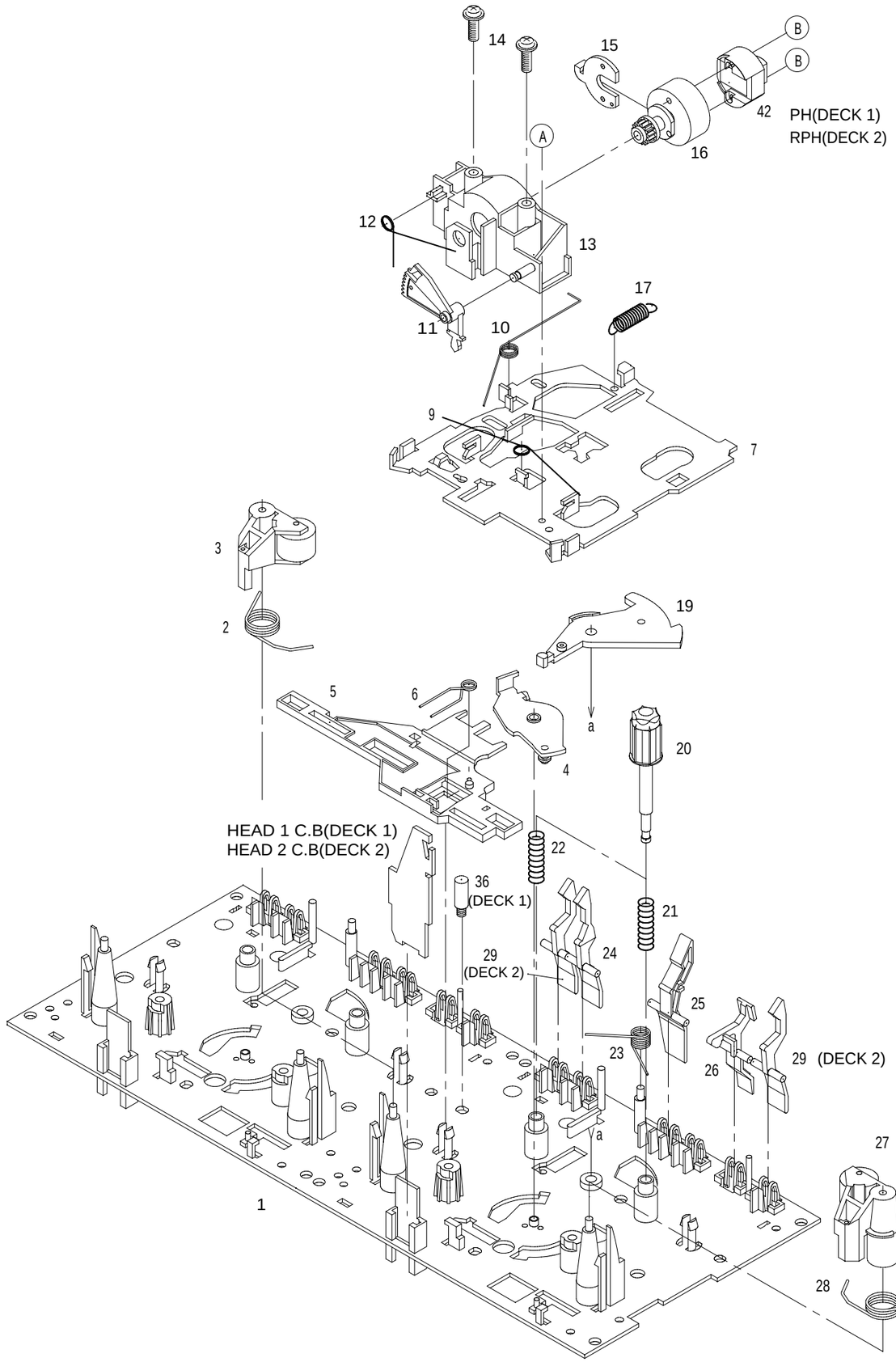
12. REC/PB Frequency Response Adjustment (DECK 2)
    Settings : • Test tape : TTA–602
    • Test point : TP8(Lch), TP9(Rch)
    • Input signal : 1kHz / 8kHz (LINE IN)
    • Adjustment location : SFR451 (Lch)
    SFR452 (Rch)
    Method : Apply a 1kHz signal and REC mode. Then adjust OSC attenuator so that the output level at the TP8, TP9 becomes -20VU. Record and play back the 1kHz and 8kHz signals and adjust SFRs so that the output of the 8kHz signals becomes 0dB ± 0.5dB with respect to that of the 1kHz signal.

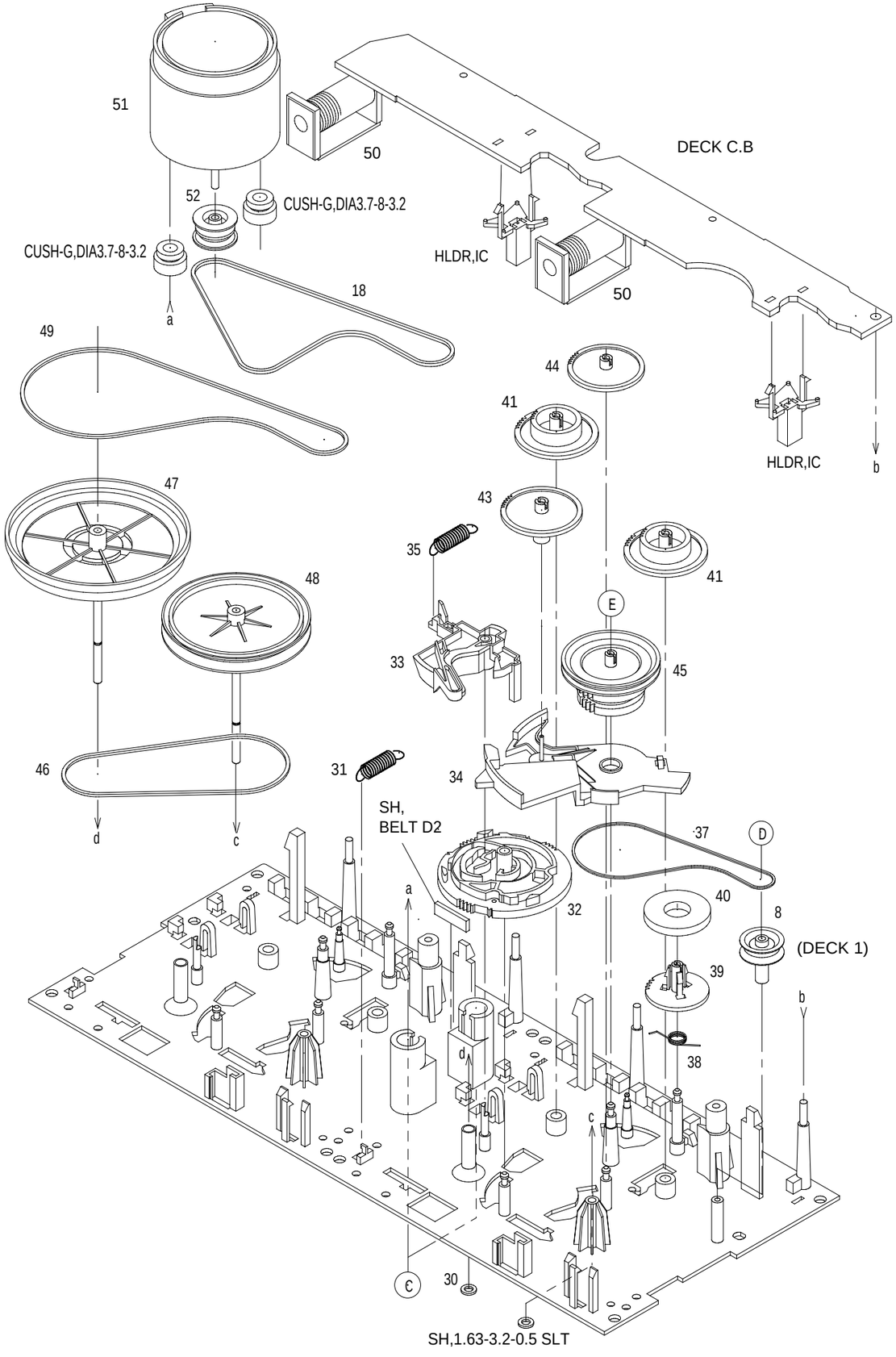
13. REC/PB Sensitivity Check (DECK 2)
    Settings : • Test tape : TTA–602
    • Test point : TP8(Lch), TP9(Rch)
    • Input signal : 1kHz (LINE IN)
    Method : Apply a 1kHz signal and REC mode. Then adjust OSC attenuator so that the output level at TP8, TP9 becomes 0VU. Record and play back the 1kHz signals and check that the output is –2dB ± 3.0dB.

< FRONT SECTION >

14. μ-CON OSC Adjustment
    Settings : • Test point : TP7 and GND
    • Adjustment location : L331
    Method : Insert AC plug while pressing POWER and TUNER function keys. Adjust L331 so that the frequency at the test point is 153.84Hz ± 0.15Hz.

MECHANISM EXPLODED VIEW 1/1 <LH: 2ZM-3MK2 YPR4N>





MECHANISM EXPLODED VIEW 1/1 <U: ZZM-3 PR1NF>