

TITLE : HV550QUB-H11
Preliminary Product Specification
Rev. P0

Fuzhou BOE Optoelectronics Technology Co., Ltd

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S8-65-8D-005

PRODUCT GROUP
TFT-LCD

Rev. P0

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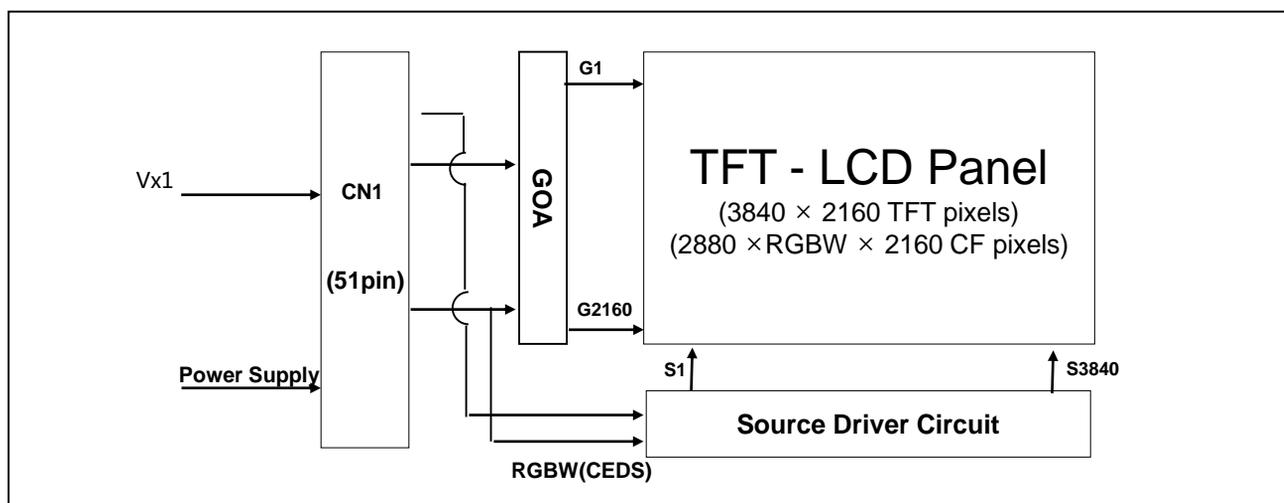
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1.0 GENERAL DESCRIPTION

1.1 Introduction

HV550QUB-H11 is a color active matrix TFT LCD open cell using amorphous silicon TFT's (Thin Film Transistors) as an active switching devices. This module has a 54.64 inch diagonally measured active area with UHD resolutions (3840 horizontal by 2160 vertical pixel array). Each pixel is divided into White, RED, GREEN, BLUE dots which are arranged in island and this module can display 1.07G colors. The TFT-LCD panel used for this module is adapted for a low reflection and higher color type.



1.2 Features

- V by one interface with 8 lanes
- High-speed response
- Low color shift image quality
- 8-bit + FRC color depth, display 1.07G colors
- High luminance and contrast ratio, low reflection and wide viewing angle
- DE (Data Enable) only mode
- ADS technology is applied for high display quality
- RoHS compliant

1.3 Application

- Home Alone Multimedia TFT-LCD TV
- Display Terminals for Control System
- Ultra High Definition TV(UHD TV)
- AV application Products

1.4 General Specification

< Table 1. General Specifications >

Parameter	Specification	Unit	Remark
Active area	1209.6(H) × 680.4(V)	mm	
Number of pixels	3840 horiz. by 2160 vert. TFT Pixel, 2880 horiz. by 2160 vert. RGBW CF pixel arrangement	pixels	
Pixel pitch	315(H) × 315(V)	μm	
Pixel arrangement	Pixels WRGB Island		
Display colors	1.07G (8bits + FRC)	colors	
Display mode	Transmission mode, Normally Black		
Open Cell Transmittance	TBD	%	At center point with BOE BLU
Weight	TBD	Kg	
Power Consumption	18 (Typ.)	Watt	
Surface Treatment	Haze 1% , 3H, Anti-Glare Layer (for Front and Rear)		

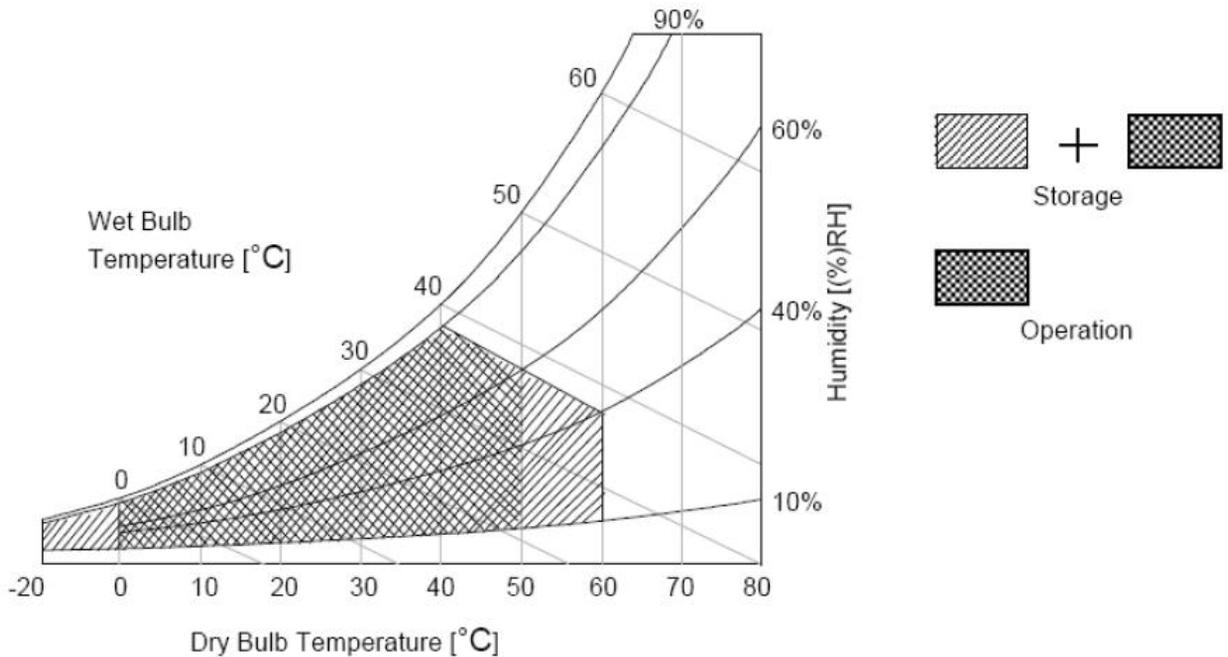
2.0 ABSOLUTE MAXIMUM RATINGS

The followings are maximum values which, if exceed, may cause faulty operation or damage to the unit. The operational and non-operational maximum voltage and current values are listed in Table 2.

< Table 2. Open Cell Electrical Specifications >

[VSS=GND=0V]

Parameter	Symbol	Min.	Max.	Unit	Remark
Power Supply Voltage	VDD	VSS-0.3	13.5	V	Ta = 25 °C
Operating Temperature	T _{OP}	0	+50	°C	Note 1
Storage Temperature	T _{SUR}	-20	+60	°C	
	T _{ST}	-20	+60	°C	
Operating Ambient Humidity	Hop	10	80	%RH	
Storage Humidity	Hst	10	80	%RH	



3.0 ELECTRICAL SPECIFICATIONS

3.1 TFT LCD Open Cell

< Table 3. Open Cell Electrical Specifications >

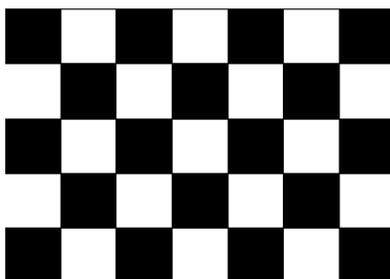
[Ta =25 ± 2 °C]

Parameter	Symbol	Values			Unit	Remark	
		Min	Typ	Max			
Power Supply Input Voltage	VDD	10.8	12	13.2	Vdc		
Power Supply Ripple Voltage	VRP			600	mV		
Power Supply Current	IDD	-	1.5	3	A	Note 1	
Power Consumption	PDD		18	36	Watt		
Rush current	IRUSH	-	-	4	A	Note 2	
V by One Interface	Differential Input High Threshold Voltage	VLVTH		+50	mV		
	Differential Input Low Threshold Voltage	VLVTL	-50		mV		
	Common Input Voltage	VLVC			V		
	Terminating Resistor	Rt	90	100	110	ohm	
CMOS Interface	Input High Threshold Voltage	VIH	2.7	-	3.3	V	
	Input Low Threshold Voltage	VIL	0	-	0.6	V	

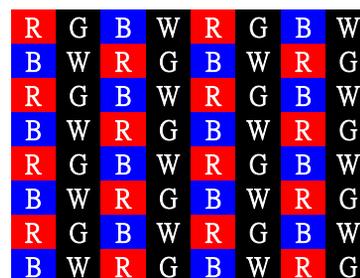
Note 1 : The supply voltage is measured and specified at the interface connector of LCM.

The current draw and power consumption specified is for VDD=12.0V,

a) Typ: Mosaic 7X5(L0/L255)



b) Max : R&G Pattern(L255)



Note 2 : The duration of rush current is about 2ms and rising time of Power Input is 1ms(min)

4.0 OPTICAL SPECIFICATION

The test of optical specifications shall be measured in a dark room (ambient luminance \leq 1 lux and temperature $=25\pm 2^{\circ}\text{C}$) with the equipment of Luminance meter system (Goniometer system and PR730) and test unit shall be located at an approximate distance 180cm from the LCD surface at a viewing angle of θ and Φ equal to 0° . We refer to $\theta_{\Phi=0}$ ($=\theta_3$) as the 3 o'clock direction (the "right"), $\theta_{\Phi=90}$ ($=\theta_{12}$) as the 12 o'clock direction ("upward"), $\theta_{\Phi=180}$ ($=\theta_9$) as the 9 o'clock direction ("left") and $\theta_{\Phi=270}$ ($=\theta_6$) as the 6 o'clock direction ("bottom"). While scanning θ and/or Φ , the center of the measuring spot on the Display surface shall stay fixed. The measurement shall be executed after 30 minutes warm-up period. VDD shall be 12.0V \pm 10% at 25°C . Optimum viewing angle direction is 6 'clock.

< Table 4. Optical Table >

[VDD = 12.0V, Frame rate = 120Hz, Ta = $25\pm 2^{\circ}\text{C}$]

Parameter		Symbol	Condition	Min	Typ	Max	Unit	Remark
Viewing Angle	Horizontal	Θ_3	CR > 10		89		Deg.	Note 1
		Θ_9			89		Deg.	
	Vertical	Θ_{12}			89		Deg.	
		Θ_6			89		Deg.	
Contrast ratio		CR		1000:1	1200:1	-	-	Note 2
Reproduction of color	White	W_x	$\Theta = 0^{\circ}$ (Center) Normal Viewing Angle	TYP. - 0.03	TBD	TYP. + 0.03	-	Note 3
		W_y			TBD		-	
	Red	R_x			TBD		-	
		R_y			TBD		-	
	Green	G_x			TBD		-	
		G_y			TBD		-	
	Blue	B_x			TBD		-	
		B_y			TBD		-	
Response Time	G to G	T_g		-	8	10	ms	Note 4
Cell Transmittance				-	7.15		%	Note 5

Note :

1. Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface.
2. Contrast measurements shall be made at viewing angle of $\theta = 0^\circ$ and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state. (See Figure 1 shown in Appendix) Luminance Contrast Ratio (CR) is defined mathematically.

$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

3. The color chromaticity coordinates specified in Table 9 shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the panel. The BLU is used by BOE.
4. Response time T_g is the average time required for display transition by switching the input signal as below table and is based on Frame rate $f_V = 60\text{Hz}$ to optimize. Each time in below table is defined as Figure 2 and shall be measured by switching the

Measured Response Time	Target																
	0	15	31	47	63	79	95	111	127	143	159	175	191	207	223	239	255
0																	
15																	
31																	
47																	
63																	
79																	
95																	
111																	
127																	
143																	
159																	
175																	
191																	
207																	
223																	
239																	
255																	

5. Definition of Transmittance (T%) :

Module is with white(L255) signal input

$$\text{Transmittance} = \frac{\text{Luminance of LCD Module}}{\text{Luminance of BLU}} \times 100 \%$$

5.0 INTERFACE CONNECTION.

- V by One CN (51Pin) Connector : IS050-C51B-C39-S(UJU) or Equivalent.

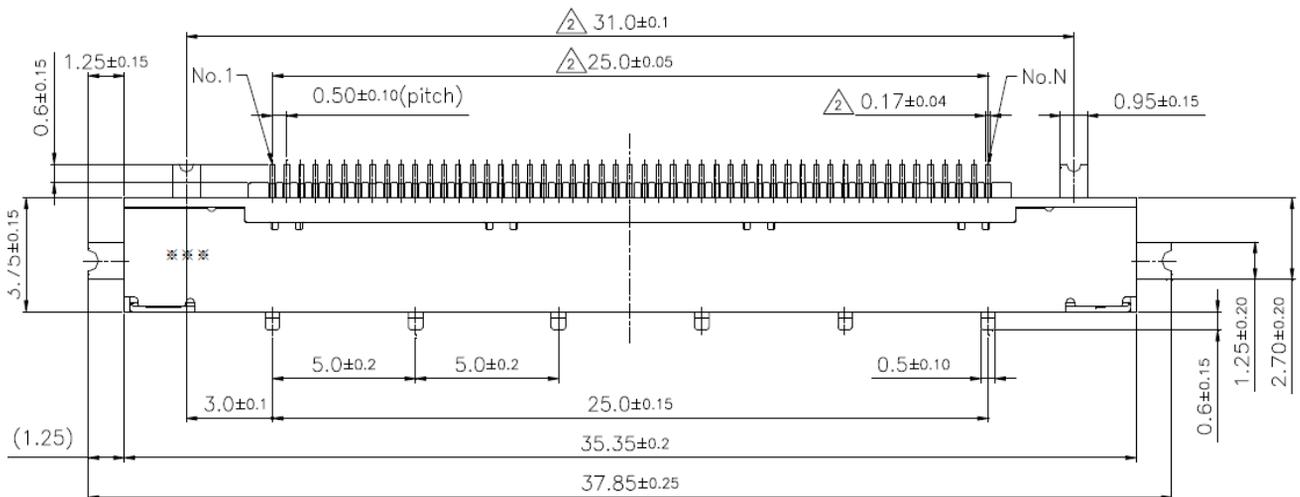
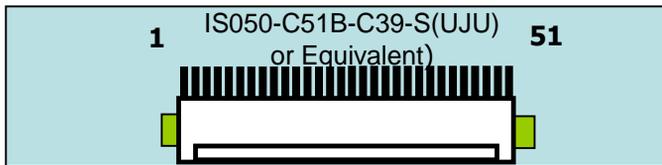
< Table 5. Open Cell Input Connector Pin Configuration >

Pin No	Symbol	Description	Pin No	Symbol	Description
1	VDD	Power Supply +12.0V	21	NC	No Connection
2	VDD	Power Supply +12.0V	22	SEL_SECTION	Low:2 Section(Default) High:1 Section
3	VDD	Power Supply +12.0V	23	NC	No Connection
4	VDD	Power Supply +12.0V	24	GND	Ground
5	VDD	Power Supply +12.0V	25	HTPDN	Hot plug detect
6	VDD	Power Supply +12.0V	26	LOCKN	Lock detect
7	VDD	Power Supply +12.0V	27	GND	Ground
8	VDD	Power Supply +12.0V	28	Rx0n	V-by-One HS Data Lane 0
9	NC	No Connection	29	Rx0p	V-by-One HS Data Lane 0
10	GND	Ground	30	GND	Ground
11	GND	Ground	31	Rx1n	V-by-One HS Data Lane 1
12	GND	Ground	32	Rx1p	V-by-One HS Data Lane 1
13	GND	Ground	33	GND	Ground
14	GND	Ground	34	Rx2n	V-by-One HS Data Lane 2
15	NC	No Connection	35	Rx2p	V-by-One HS Data Lane 2
16	NC	No Connection	36	GND	Ground
17	NC	No Connection	37	Rx3n	V-by-One HS Data Lane 3
18	SDA	SDA	38	Rx3p	V-by-One HS Data Lane 3
19	SCL	SCL	39	GND	Ground
20	NC	No Connection			

Pin No	Symbol	Description	Pin No	Symbol	Description
40	Rx4n	V-by-One HS Data Lane 4	46	Rx6n	V-by-One HS Data Lane 6
41	Rx4p	V-by-One HS Data Lane 4	47	Rx6p	V-by-One HS Data Lane 6
42	GND	Ground	48	GND	Ground
43	Rx5n	V-by-One HS Data Lane 5	49	Rx7n	V-by-One HS Data Lane 7
44	Rx5p	V-by-One HS Data Lane 5	50	Rx7p	V-by-One HS Data Lane 7
45	GND	Ground	51	GND	Ground

Notes : NC(Not Connected) : This pins are only used for BOE internal operations.

Rear view of LCM



IS050-C51B-C39-S(UJU)

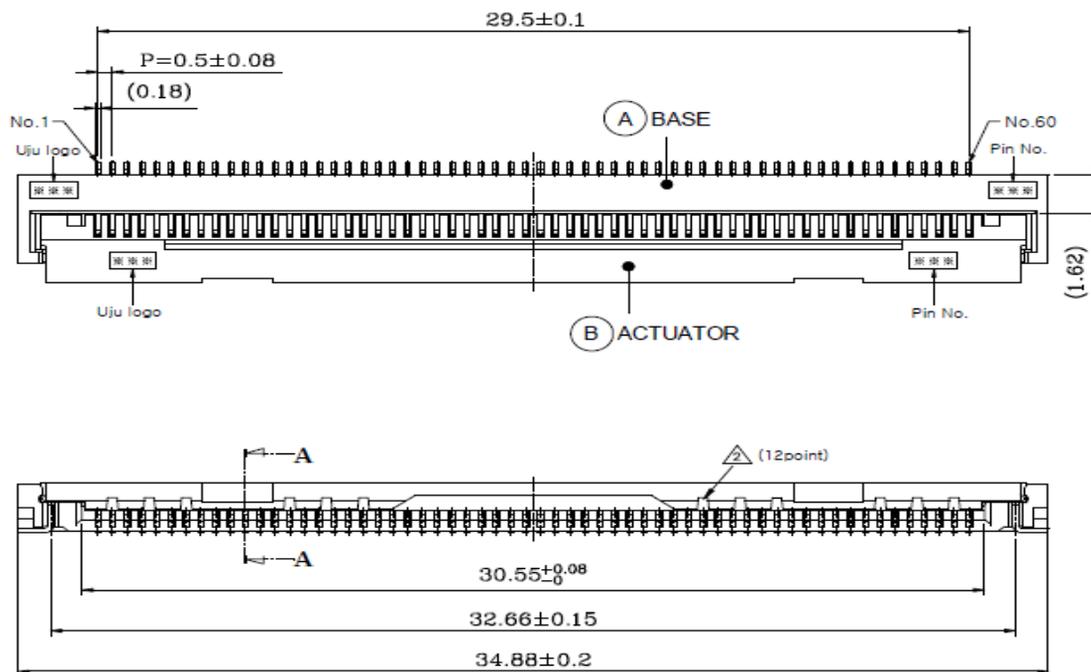
5.0 INTERFACE CONNECTION

- CEDS CN (60Pin) Connector : PF050-L60B-C21(UJU) or MSAK24056P60(STM).

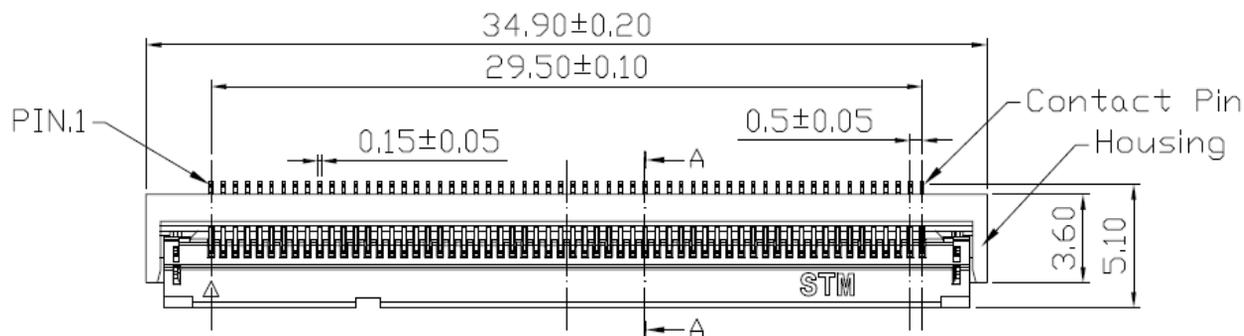
< Table 5. Open Cell Input Connector Pin Configuration >

PIN	Left	Right
1	GMA18	CLK1
2	GMA15	CLK2
3	GMA14	CLK3
4	GMA13	CLK4
5	GMA10	CLK5
6	GMA9	CLK6
7	GMA6	CLK7
8	GMA5	CLK8
9	GMA4	CLK9
10	GMA1	CLK10
11	LOCK_OUT6	NC
12	GND	VDDODD
13	CEDS12-	VDDEVEN
14	CEDS12+	VGL2
15	GND	NC
16	CEDS11-	STV
17	CEDS11+	VGL1
18	GND	VCOM_1
19	CEDS10-	NC
20	CEDS10+	VCOM_0
21	GND	GND
22	CEDS9-	AVDD
23	CEDS9+	AVDD
24	GND	AVDD
25	CEDS8-	AVDD
26	CEDS8+	HAVDD
27	GND	VCC_18
28	CEDS7-	VCC_18
29	CEDS7+	VTERM
30	GND	NC
31	LOCK_OUT3	GND
32	VTERM	CEDS6-
33	VCC_18	CEDS6+
34	VCC_18	GND
35	HAVDD	CEDS5-

36	AVDD	CEDS5+
37	AVDD	GND
38	AVDD	CEDS4-
39	AVDD	CEDS4+
40	GND	GND
41	VCOM_0	CEDS3-
42	NC	CEDS3+
43	VCOM_1	GND
44	VGL1	CEDS2-
45	STV	CEDS2+
46	NC	GND
47	VGL2	CEDS1-
48	VDDEVEN	CEDS1+
49	VDDODD	GND
50	NC	LOCK_OUT3
51	CLK10	GMA18
52	CLK9	GMA15
53	CLK8	GMA14
54	CLK7	GMA13
55	CLK6	GMA10
56	CLK5	GMA9
57	CLK4	GMA6
58	CLK3	GMA5
59	CLK2	GMA4
60	CLK1	GMA1



PF050-L60B-C21(UJU)



MSAK24056P60(STM)

6.0 SIGNAL TIMING SPECIFICATION

< Table 6. Timing Table >

Item		Symbols	Min	Typ	Max	Unit
Frequency		1/Tc	66	74.5	75	MHz
Vertical	Frame Rate	F	47	60	61	Hz
	Total	T _V	2180	2250	2450	T _H
	Display	T _{VD}	2160			T _H
	Blank	T _{VB}	20	90	290	T _H
Horizontal	Total	T _H	530	550	570	T _{CLK}
	Display	T _{HD}	-	480	-	T _{CLK}
	Blank	T _{HB}	-	70	-	T _{CLK}

Notes: This product is DE only mode. The input of Hsync & Vsync signal does not have an effect on normal operation.

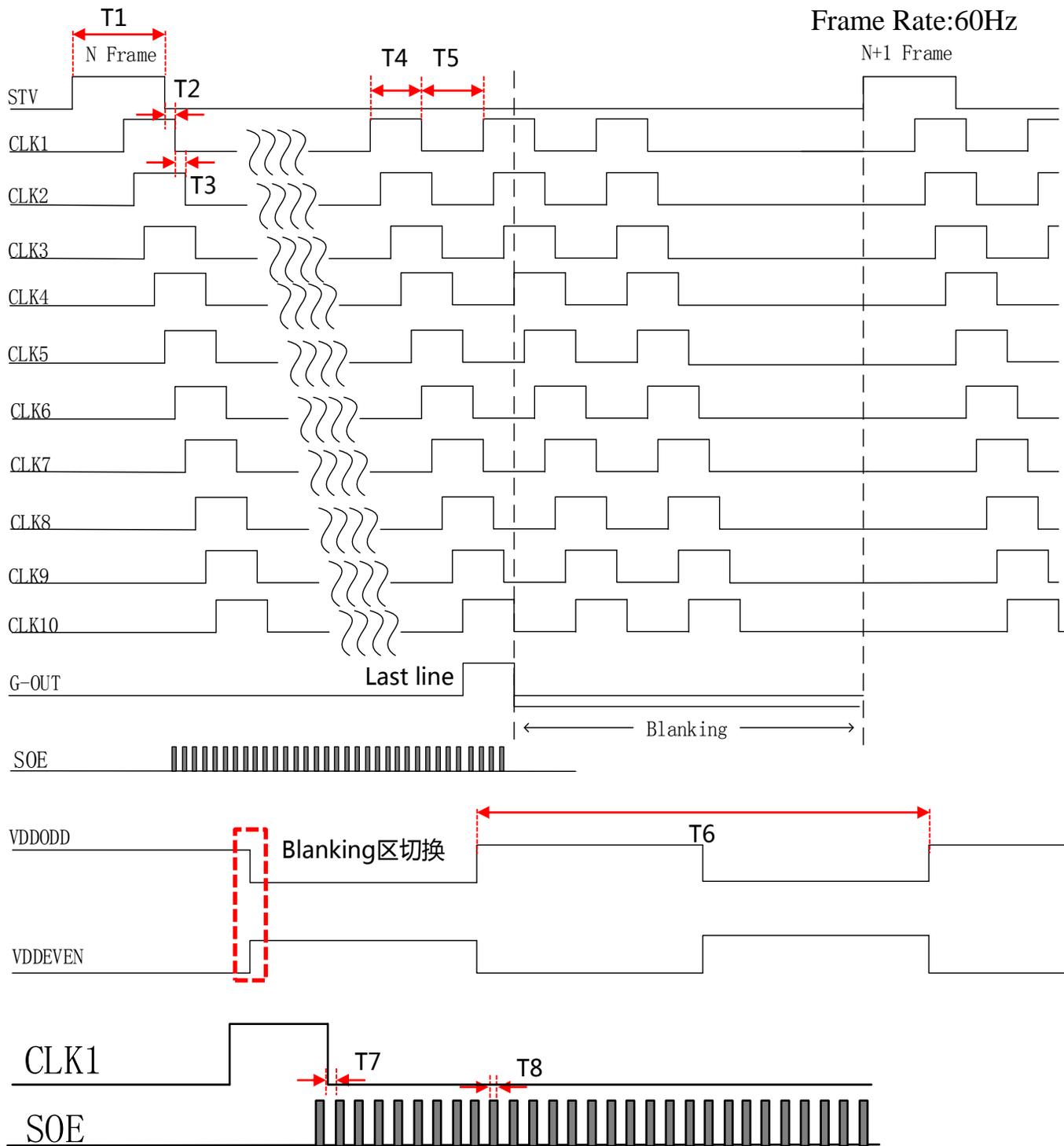
6.0 SIGNAL TIMING SPECIFICATION

- Signal Timing Waveform

H total :4400

V total :2250

Frame Rate:60Hz



6.0 SIGNAL TIMING SPECIFICATION

- Signal Timing Waveform Remark

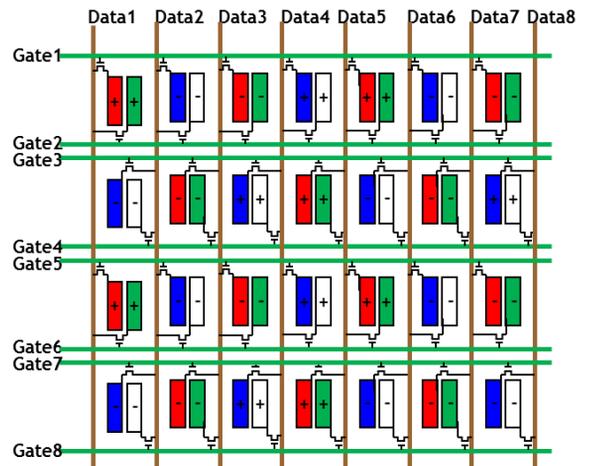
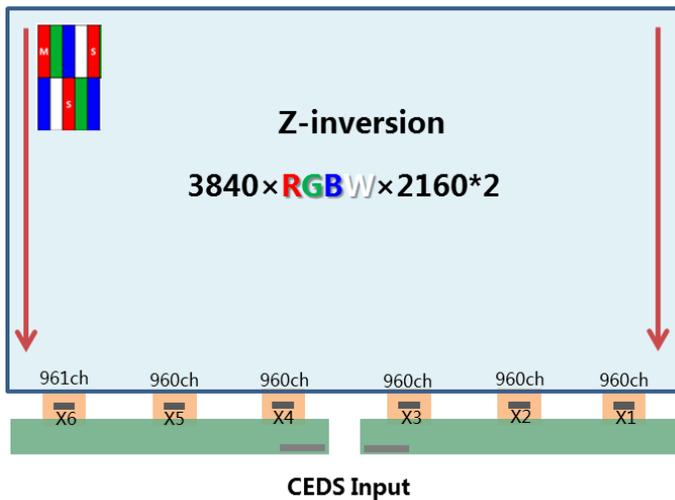
H total :4400

V total :2250

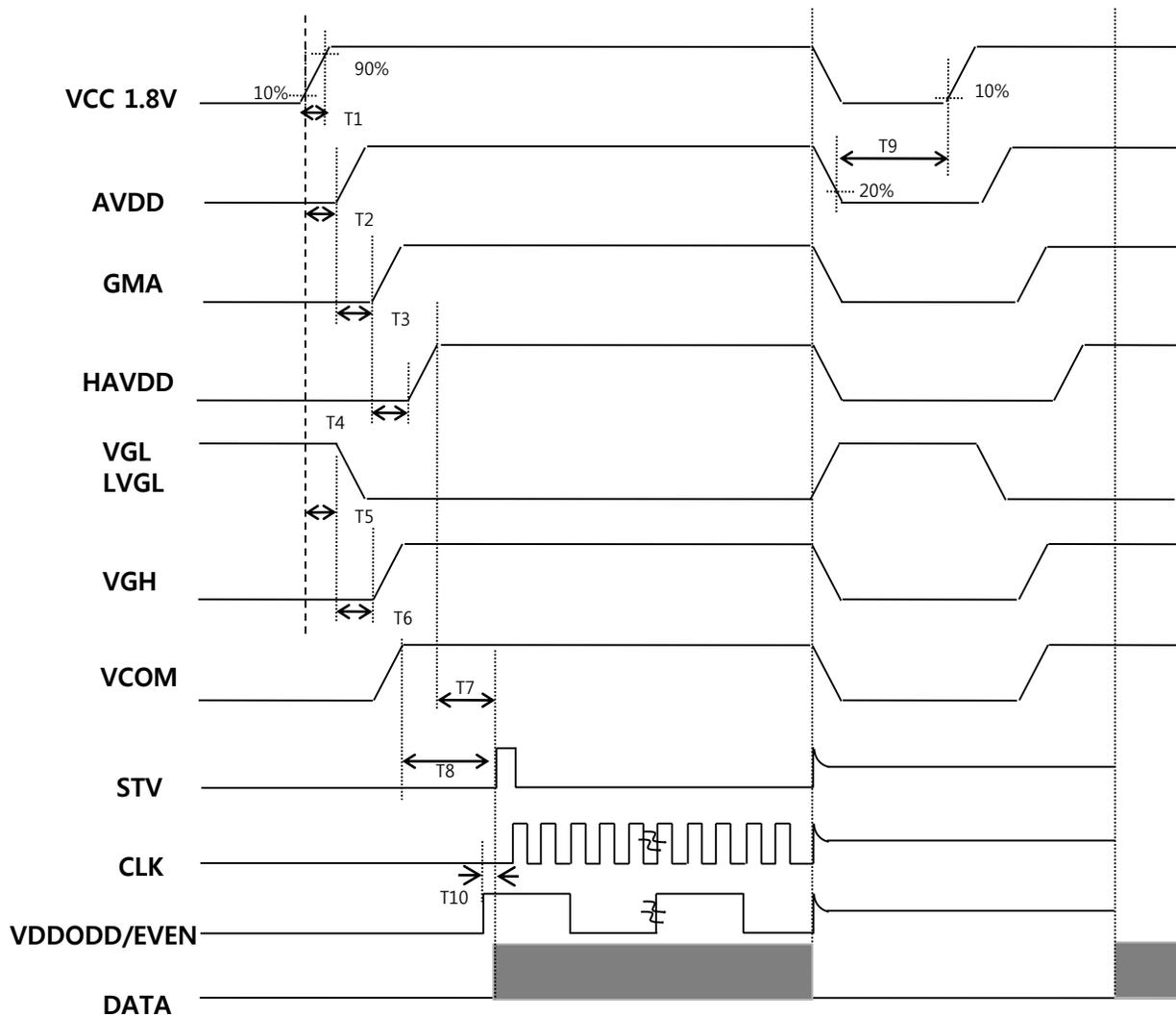
Frame Rate:60Hz

	Min.	Typ.	Max.		
T1	-	33.3us	-	STV Width(9H)	
T2	-	3.7us	-	CLK1 Falling to STV Falling (1H)	
T3	-	3.7us	-	CLK1 Falling to CLK2 Falling(1H)	
T4	-	15.5us	-	CLK High Width(4.2H)	
T5	-	21.5us	-	CLK Low Width(5.8H)	
T6	3s	4s	5s	VDDODD/VDDEVEN Period	在Blanking区变化
T7	-	1.8us	-	GOE	
T8	-	0.25us	-	SOE Width	

- Pixel Structure



- Signal Timing Waveform(Power on/off)



- Signal Timing Waveform(Power on)

T	Min	Type	Max	Unit	Note
T1	0	-	10	ms	
T2	0	-	-	ms	
T3	0	-	-	ms	AVDD must be higher than HAVDD and GMA all the time
T4	0	-	-	ms	AVDD must be higher than HAVDD and GMA all the time
T5	0	-	-	ms	
T6	0	-	-	ms	
T7	0	-	-	ms	
T8	0	-	-	ms	
T9	0	-	-	ms	
T10	50	-	-	ms	

6.1 V by one Misc. Setting.

- a) System side have to put pull high resistor on LOCKN/HTPDN pins.
- b) V by one data mapping as follows.

2 Section								
Hactive= 3840								
	port 0		port 1		port 2		port 3	
	Lane 0	Lane 1	Lane 2	Lane 3	Lane 4	Lane 5	Lane 6	Lane 7
V Blanking	FSBS							
	FSBP							

	FSBP							
	FSBE_SR							
Line 1	Pixel 1	Pixel 2	Pixel 3	Pixel 4	Pixel 1921	Pixel 1922	Pixel 1923	Pixel 1924
	Pixel 5	Pixel 6	Pixel 7	Pixel 8	Pixel 1925	Pixel 1926	Pixel 1927	Pixel 1928

	Pixel 1917	Pixel 1918	Pixel 1919	Pixel 1920	Pixel 3837	Pixel 3838	Pixel 3839	Pixel 3840
H Blanking	FSBS							
	FSBP							

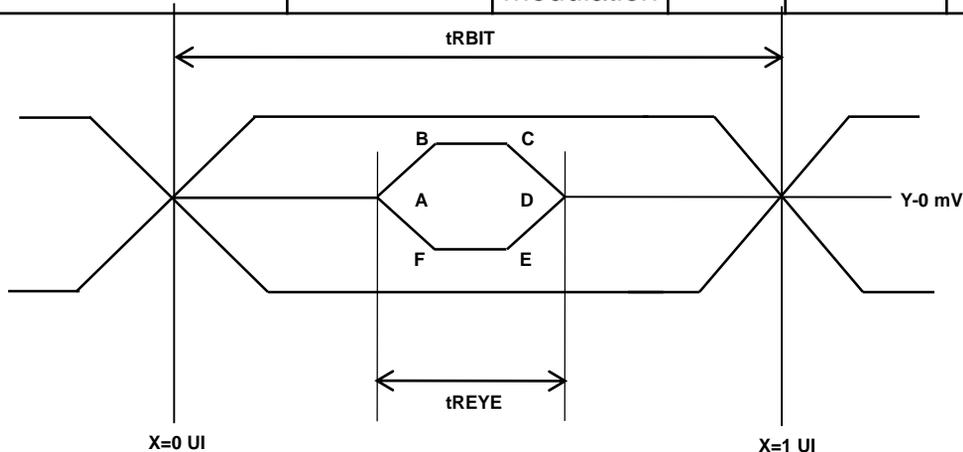
	FSBP							
	FSBE							
Line 2	Pixel 1	Pixel 2	Pixel 3	Pixel 4	Pixel 1921	Pixel 1922	Pixel 1923	Pixel 1924
	Pixel 5	Pixel 6	Pixel 7	Pixel 8	Pixel 1925	Pixel 1926	Pixel 1927	Pixel 1928

	Pixel 1917	Pixel 1918	Pixel 1919	Pixel 1920	Pixel 3837	Pixel 3838	Pixel 3839	Pixel 3840

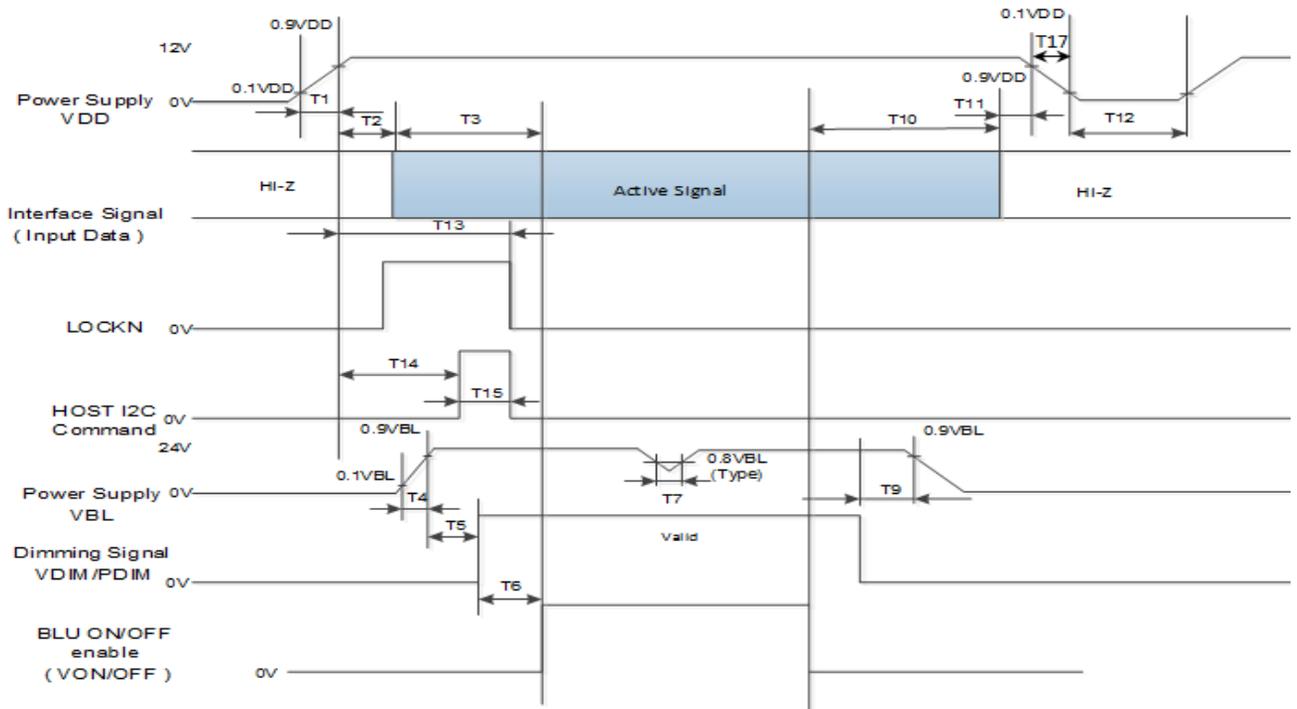
7.0 SIGNAL TIMING WAVEFORMS OF INTERFACE SIGNAL

< Table 7. Signal Timing Waveforms Table >

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Unit Interval(VBO Operation Bit Rate)	tRBIT	3-byte	380	tTCIP/30	1667	PS
		4-byte	285	tTCIP/40	1250	PS
		5-byte	266	tTCIP/50	1000	PS
Eye Width at Package Pin	tREYE	-	-	0.5	-	UI
Eye Width Position A at Package Pin	tA	-	-	0.25	-	UI
Eye Width Position B at Package Pin	tB	-	-	0.3	-	UI
Eye Width Position Cat Package Pin	tC	-	-	0.7	-	UI
Eye Width Position D at Package Pin	tD	-	-	0.75	-	UI
Eye Width Position E at Package Pin	tE	-	-	0.7	-	UI
Eye Width Position F at Package Pin	tF	-	-	0.3	-	UI
Intra – pair Skew	TTOSK_intra	-	-0.3	-	0.3	UI
Intra – pair Skew	TTOSK_inter	-	-5	-	5	UI
SSCG	-	30KHz modulation	-0.5	-	0.5	%



9.0 POWER SEQUENCE



< Table 9. Sequence Table >

Parameter	Values			Units
	Min	Typ	Max	
T1	0.5	-	10	ms
T2	0	-	-	ms
T3	200	-	-	ms
T4	20	-	-	ms
T5	500	-	-	ms
T6	0	-	-	ms
T7	-	-	10	ms
T8	0	-	-	ms
T9	500	-	-	ms
T10	100	-	-	ms
T11	0	-	-	ms
T12	1	-	-	s
T13	200	-	-	ms
T14	1200	-	-	ms
T15	Depends on I2C command			ms

- Notes:
1. Even though T1 is over the specified value, there is no problem if In-Rush current is under Max. Spec.
 2. Back Light must be turn on after power for logic and interface signal are valid.
 3. T17 decreases smoothly, if there were re-bouncing voltage, it must be smaller than 5 volts.

10.0 BIST MODE SPECIFICATION

- BIST controlled by system (Connector pin 176)

BIST Function Test

Pin5 Level	BIST Fuction	BIST Pattern Sequence	Pattern Holding Time	Result
High	Enable	Black -> White -> Red ->Green -> Blue	2s	
Low	Disable	-		



Pattern sequence

11.0 MECHANICAL CHARACTERISTICS

11.1 Dimensional Requirements

Figure 4(located in Appendix) shows mechanical outlines for the model HV550QUB-H11. Other parameters are shown in Table 10.

< Table 10. Dimensional Parameters >

Parameter	Specification	Unit
Active area	1209.6 (H) × 680.4(V)	mm
Pixel pitch	315 (H) × 315 (V)	μm
Number of pixels	3840(H) × 2160(V) (TFT pixel) 2880(H) × 2160(V) (1 CF pixel= R + G + B +W dots)	pixels
Weight	TBD	kg

11.2 Surface Treatment and Polarizer Hardness

The surface of the LCD has an Low haze coating and a coating to Reduce scratching. The front polarizer hardness is at least 2H.

12.0 RELIABILITY TEST

The Reliability test items and its conditions are shown in below.

< Table 11. Reliability Test Parameters >

No	Test Items	Conditions
1	High temperature storage test	Ta = 60 °C, 240 hrs
2	Low temperature storage test	Ta = -20 °C, 240 hrs
3	High temperature & high humidity operation test	Ta = 50 °C, 80%RH, 240hrs
4	High temperature operation test	Ta = 50 °C, 240hrs
5	Low temperature operation test	Ta = 0 °C, 240hrs
6	Thermal shock	Ta = -20 °C ↔ 60 °C (0.5 hr), 100 cycle

This test condition is based on BOE module.

13.0 HANDLING & CAUTIONS

(1) Cautions when taking out the Panel

- Pick the pouch only, when taking out panel from a shipping package.

(2) Cautions for handling the panel

- As the electrostatic discharges may break the LCD panel, handle the LCD panel with care. Peel a protection sheet off from the LCD panel surface as slowly as possible.
- As the LCD panel and back - light element are made from fragile glass material, impulse and pressure to the LCD panel should be avoided.
- As the surface of the polarizer is very soft and easily scratched, use a soft dry cloth without chemicals for cleaning.
- Do not pull the interface connector in or out while the LCD panel is operating.
- Put the panel display side down on a flat horizontal plane.
- Handle connectors and cables with care.

(3) Cautions for the operation

- When the panel is operating, do not lose CLK, ENAB signals. If any one of these signals is lost, the LCD panel would be damaged.
- Obey the supply voltage sequence. If wrong sequence is applied, the panel would be damaged.

(4) Cautions for the atmosphere

- Dew drop atmosphere should be avoided.
- Do not store and/or operate the LCD panel in a high temperature and/or humidity atmosphere. Storage in an electro-conductive polymer packing pouch and under relatively low temperature atmosphere is recommended.

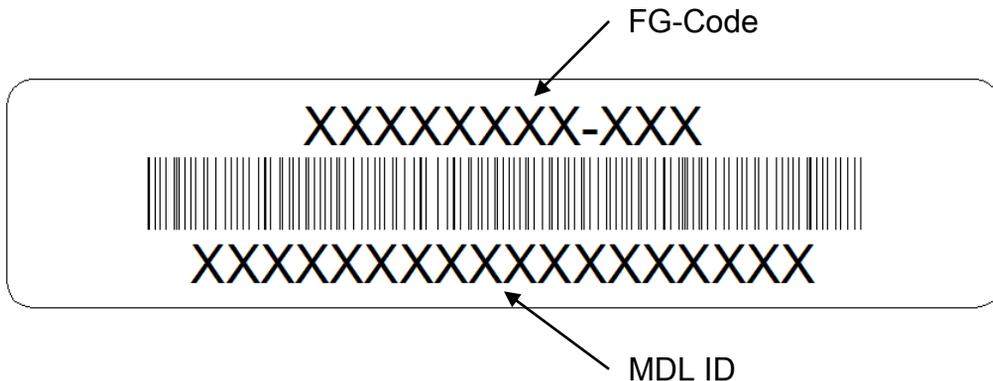
(5) Cautions for the panel characteristics

- Do not apply fixed pattern data signal to the LCD panel at product aging.
- Applying fixed pattern for a long time may cause image sticking.

(6) Other cautions

- Do not disassemble and/or re-assemble LCD panel.
- Do not re-adjust variable resistor or switch etc.
- When returning the panel for repair or etc., Please pack the panel not to be broken. We recommend to use the original shipping packages.

14.0 PRODUCT SERIAL NUMBER



MDL ID Naming Rule:

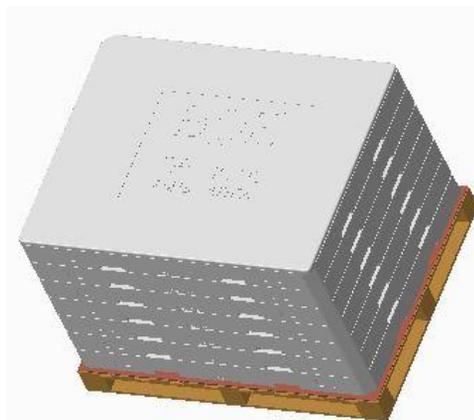
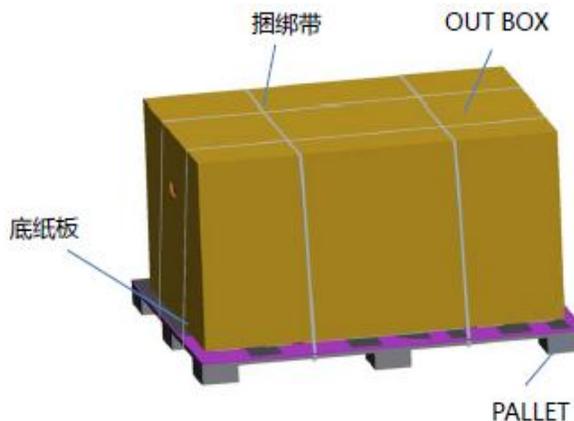
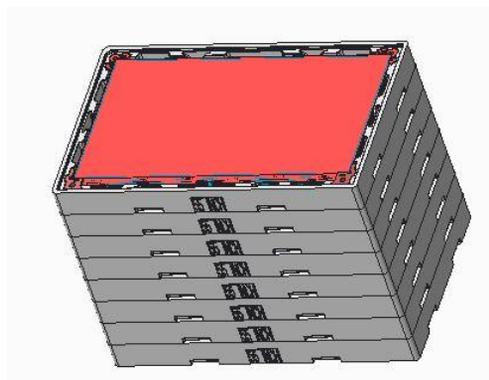
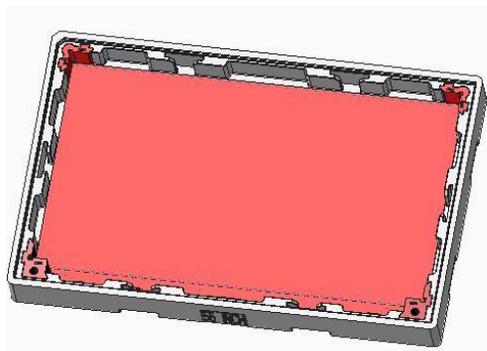
Digit Code	1	2	3	4	5	6	7	8	9	10	11
Description	Model Code GBN		Grade	Line	Year		Month	Model Extension Code			
Digit Code	12	13	14	15	16	17	18				
Description	Serial No						扫码不显示，BOE厂内用				

15.0 Packing

BOE provides the standard shipping container for customers, unless customer specifies their packing information. The standard packing method and Barcode information are shown in below.

15.1 Packing Order

Totally 16pcs panels and 17Pcs EPE Pad Put the box on the pallet,7ea boxes per pallet per box



**Place out box around the boxes.
Pack with 4 packing belts.**

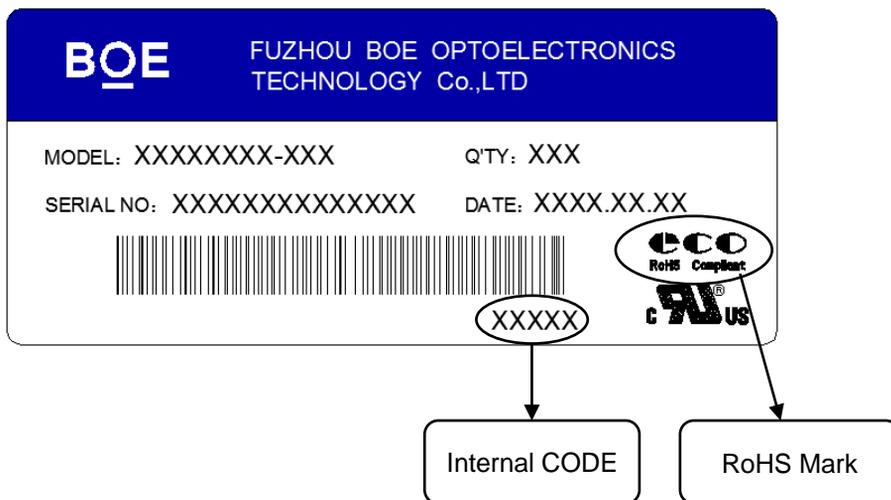
Place wrap film around the boxes.

15.2 Packing Note

- Box Dimension : 1360mmL × 868mmW × 132mmH
- Package Quantity in one Box : 16pcs

15.3 Box Label

- Label Size : 70 mm (L) × 30 mm (W)
- Contents
 - Model : HV550QUB-H11 (FG Code of Product)
 - Q`ty : 16 Open Cell in one box.
 - Serial No. : Box Serial No.
 - Date : Packing Date

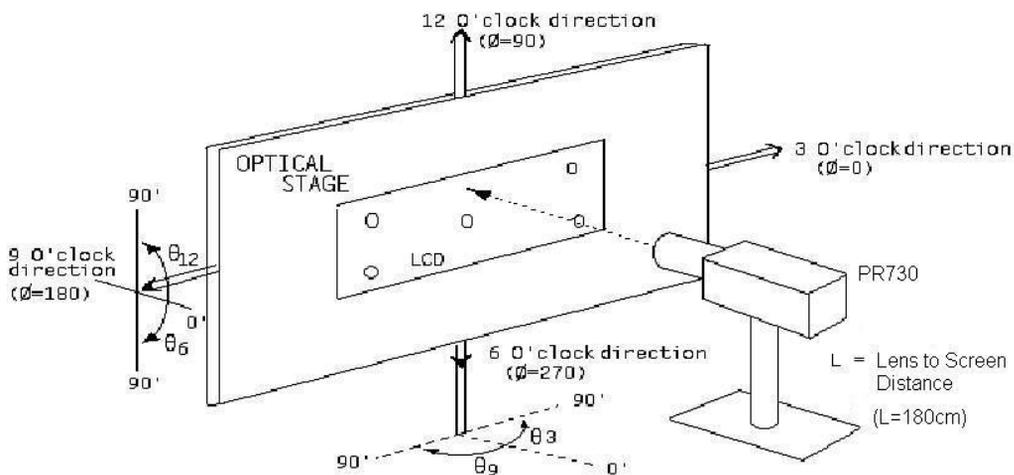


Box ID Naming Rule:

Digit Code	1	2	3	4	5	6	7	8	9	10	11	12	13
Description	Products GBN		Grade	Line	Year		Month	Revision Code	Serial No				

16.0 APPENDIX

< Figure 1. Measurement Set Up >



< Figure 2. Response Time Testing >

