SERVICE MANUAL

Date	Version	Maintenance Level	Author
2014-07-24	V1.0	L1~L4	

1.2 DEVICE OVERVIEW

Position of Keys

1. Earphone Jack	2. Earpiece
3. Volume control key	4. Touch Screen
5. Menu Key	6. Home Key
7. Back Key	8. Front camera lens
9. USB port	10. Power Key
11. Torch	12. Battery cover
13. Speaker	14. Camera lens

CAUTIONS

Please refer to the phone's user's guide for instructions relating to operation, care, and maintenance, which include important safety information.

1. Servicing and alignment must be undertaken by qualified personnel only.

2. Ensure all work is carried out at an anti-static workstation and that an anti-static wrist strap is worn.

3. Use only approved components as specified in the parts list.

4. Ensure all components, modules, screws, and insulators are correctly re-fitted after servicing and alignment

5. Ensure all cables and wires are repositioned correctly

Electrostatic discharge can easily damage the sensitive components of electronic products. Therefore, every service supplier must observe the precautions which mentioned above.

GENERAL REPAIR INFORMATION

1. Make sure your testing equipment is functioning properly before beginning repair work.

2. Before starting repairs you must observe ESD precautions such as being in your ESD protected area and connecting your wristband.

3. Use gloves to avoid corrosion and fingerprints.

4. Cover windows and displays with a protective film to avoid dust and scratches.

5. Use a lint-free cloth to clean the LCD.

6. When cleaning the pads use a soft cloth\ESD brush and isopropanol .

7. Non-faulty mechanical parts (except shielding lids and bent parts or soldered components). May be reused if they are not soldered.

8. When removing the shielding lids make sure to cover it back or replace them with new ones, otherwise the high-frequency leakage can affect the device.

9. Always use the original spare parts.

10. Check the soldering joints of the parts concerned with regard to the fault symptom. And re-solder them if necessary.

11. Remove excess soldering flux after repair.

12. Observe the torque requirements when assembling the unit.

13. please aware that some malfunctions may be software related and solved by an update

Chapter 1

Service tools

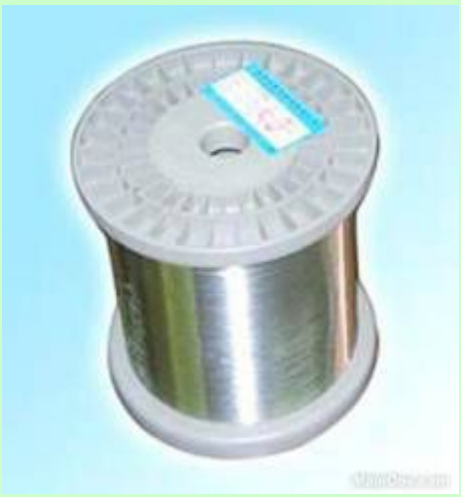
850 Rework station & Solder Iron

DC power supply

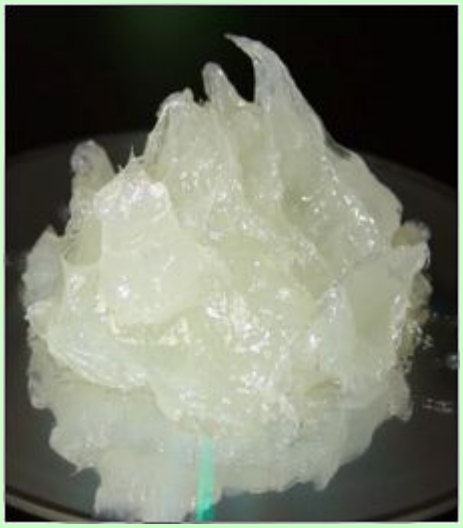
Multimeter

Digital Oscillograph

Screw driver and tweezers



Solder wire



Flux paste

Wrist grounding strap, Antistatic gloves

Chapter 2

Baseband Circuit Analysis

2.1 Mobile solution

MT6572 is a highly integrated baseband platform incorporating both modem and application processing subsystems to enable 3G (UMTS) smart phone applications. The chip integrates a High Speech Cortex-A7 MCU, an ARM MCU and a powerful DSP processor with multimedia capabilities. The MT6572 interfaces to NAND OR EMMC flash memory, 32-bit mobile DDR and LPDDR2 for optimal performance and supports booting from NAND OR EMMC to minimize the overall BOM cost. In addition, an extensive set of interfaces and connectivity peripherals are included to interface to cameras, touch-screen displays, MMC/SD cards and external Bluetooth, WiLAN and GPS modules.

The Application processor, a Cortex-A7 which includes a NEON multimedia processing engine in each core, offers processing power necessary to support the latest OpenOS along

with its demanding applications such as web browsing, email, GPS navigation and games. All while viewed on a high resolution touch screen display with graphics enhanced by the 2D and 3D graphics acceleration. The multi-standard video accelerator and an advanced audio subsystem are also included to provide advanced multimedia applications and services such as -streaming audio and video, a multitude of decoders and encoders such as H.264 and MPEG-4. Other audio supports include FR, EFR, HR and AMR vocoders, polyphonic ringtones and advanced audio functions such as echo cancellation, hands-free speakerphone operation and noise cancellation.

An ARMJZS core, DSP, and 2G and 3G coprocessors provide a powerful modem subsystem capable of supporting Category 8 (7.2 Mbps) HSDPA downlink and Category 6 (5.76 Mbps) HSUPA uplink data rates, as well as Class 12 GPRS and EDGE.

2.2 Baseband Block Diagram

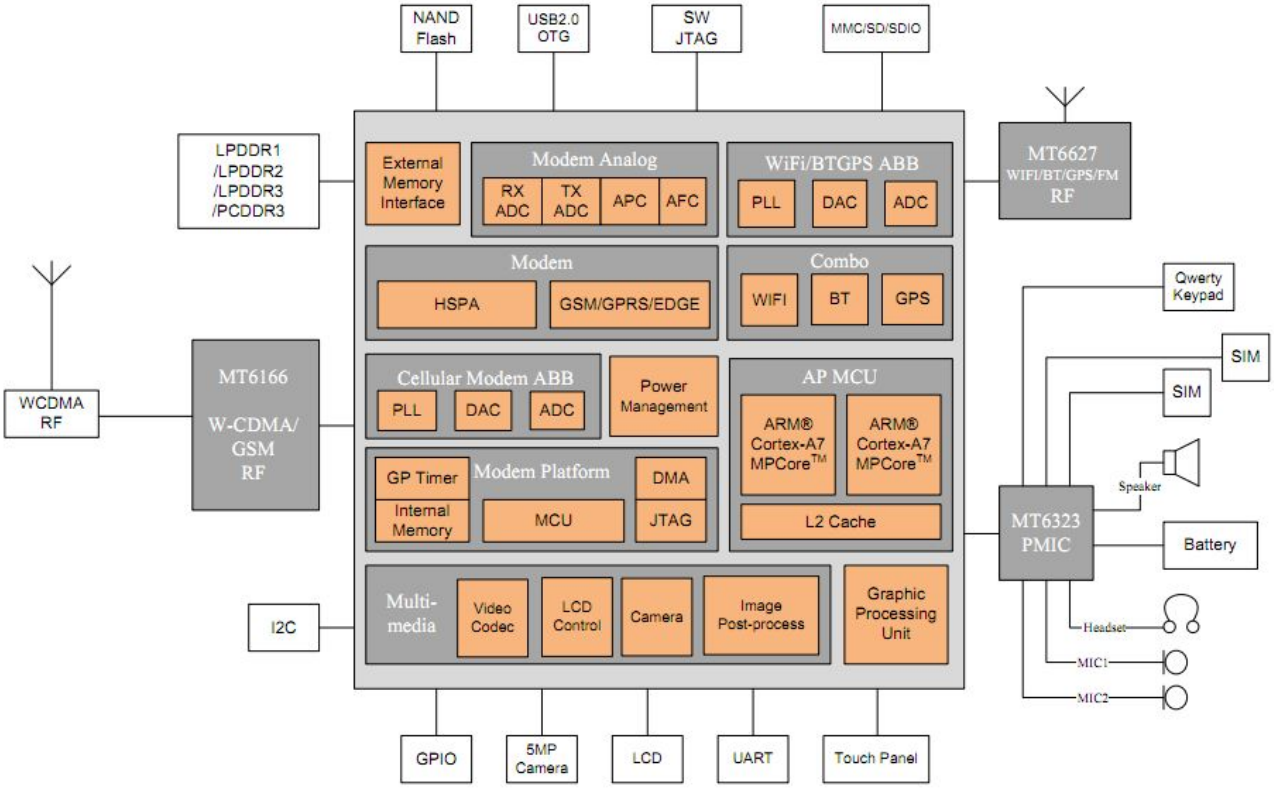


Figure 1. Block diagram of MT6572W

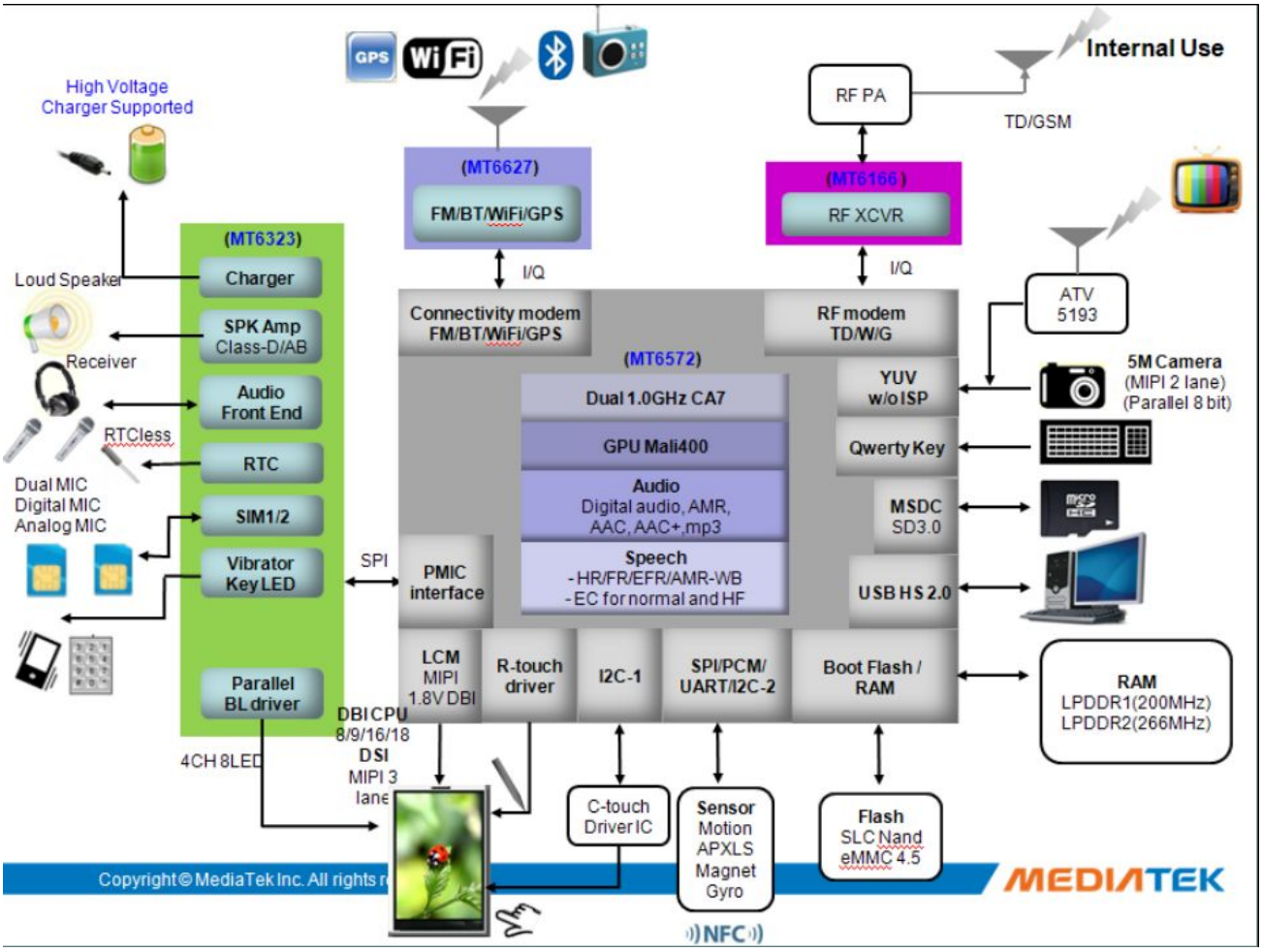


Figure 2-2: Block diagram

MT6572 is a highly integrated 3G system-on-chip (SOC) which incorporates advanced features e.g. HSPA R6 modem, a High Speech Cortex-A7 CPU, 3D graphics (OpenGL|ES 2.0), 3M camera ISP, mDDR 200 MHz/LPDDR2 266MHz and High-Definition 720p video decoder. MT6572 helps phone manufacturers build high-performance 3G smart phones with PC-like browser, 3D gaming and cinema class home entertainment experiences.

2.3 Baseband Chip Pin Description (U100 MT6572)

2.3.1 MCU Subsystem

General

- Smartphone two MCU subsystems architecture
- NAND OR EMMC flash bootloader

AP MCU subsystem

- High Speech Cortex-A7 MCU core for applications/MMI
- Integrated NEON multimedia processing engine
- 32KB I-Cache and 32KB D-Cache
- Dedicated 256KB L2 cache
- Supports DVFS from1.05V to 1.26V

MD MCU subsystem

- 520 MHz ARM + 260 MHz DSP modem cores
- Dedicated 32KB I-Cache and 32KB D-Cache
- 64KB I- and 64KB D- tightly couple memory
- 96KB L2 tightly couple memory
- Hardware-based 2G and 3G modems

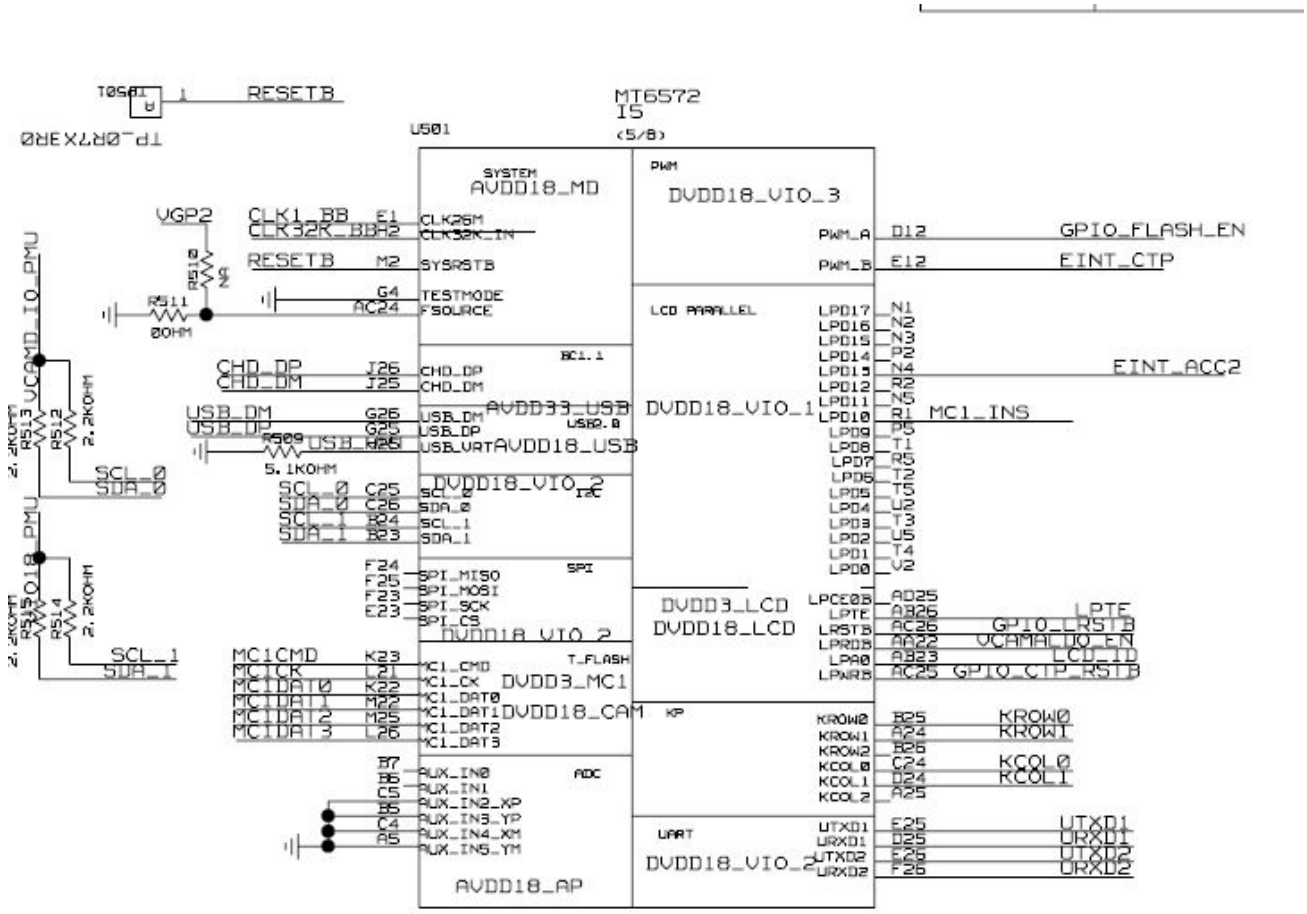


Figure 2-3: CPU U501 MCU part

2.3.2 External Memory Interface

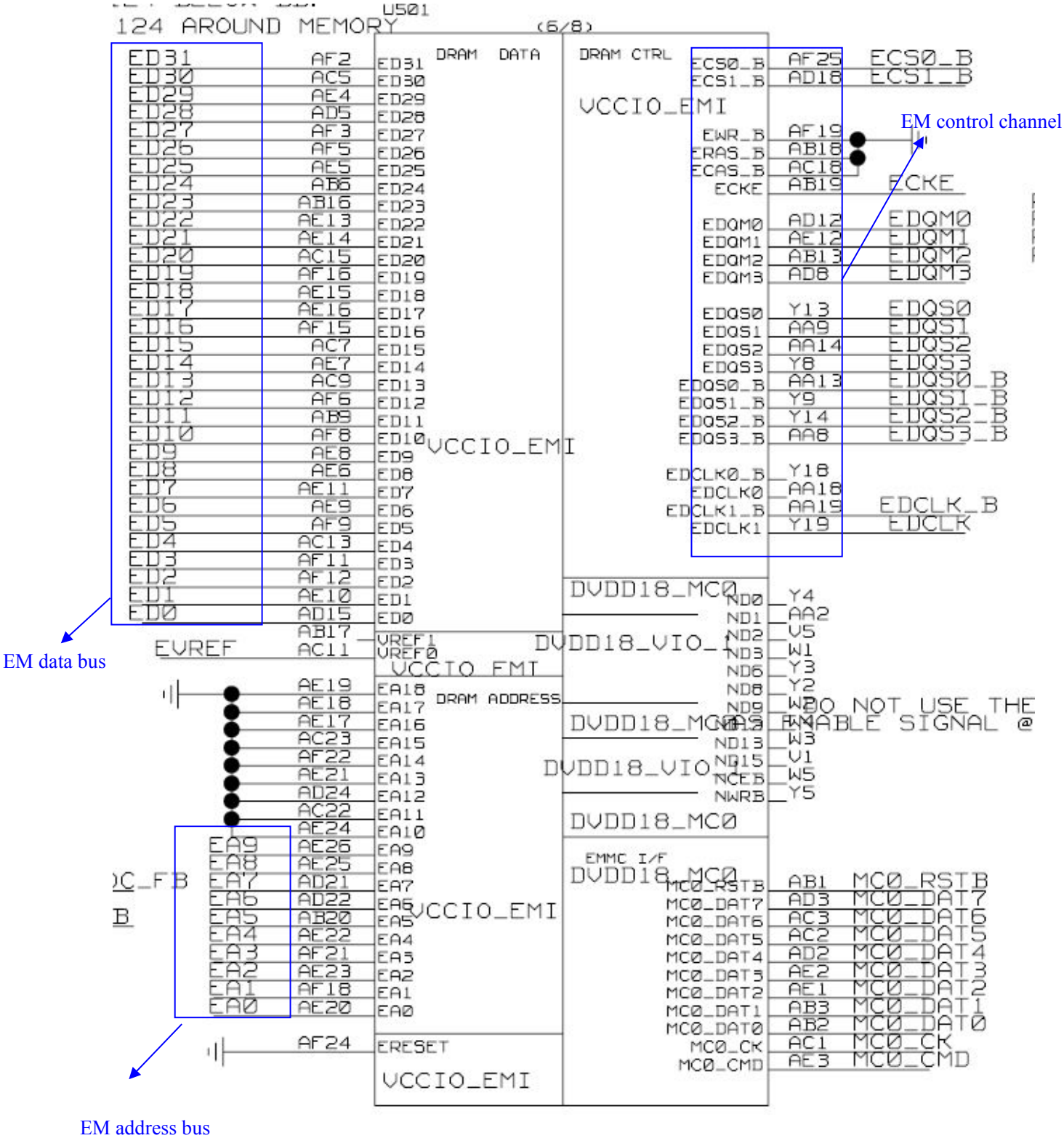


Figure 2-4: CPU U501 External Memory part

External memory interface

- Supports Mobile-DDR/LPDDR2 up to 512MB per device
- 32-bit data bus width
- Memory clock up to 260 MHz
- Supports self-refresh mode

– Low-power operation

- Programmable slew rate for memory controller's IO pads
- Supports 2 external memory devices
- Advanced bandwidth arbitration control

Flash memory IC description (D602)

The KMN5U000ZM is a Multi Chip Package Memory which combines 4GB e·MMC and 4Gbit LPDDR2 S4 SDRAM.

The SAMSUNG e·MMC is an embedded MMC solution designed in a BGA package form. e·MMC operation is identical to a MMC card and therefore is a simple read and write to memory using MMC protocol v4.41 which is a industry standard.
e·MMC consists of NAND flash and a MMC controller. 3V supply voltage is required for the NAND area (VDDF) whereas 1.8V or 3V dual supply voltage (VDD) is supported for the MMC controller. Maximum MMC interface frequency of 52MHz and maximum bus widths of 8 bit are supported.
There are several advantages of using e·MMC. It is easy to use as the MMC interface allows easy integration with any microprocessor with MMC host. Any revision or amendment of NAND is invisible to the host as the embedded MMC controller insulates NAND technology from the host. This leads to faster product development as well as faster times to market.
The embedded flash mangement software or FTL(Flash Transition Layer) of e·MMC manages Wear Leveling, Bad Block Management and ECC. The FTL supports all features of the Samsung NAND flash and achieves optimal performance.

LPDDR2-S4 uses a double data rate architecture on the Command/Address (CA) bus to reduce the number of input pins in the system. The 10-bit CA bus contains command, address, and Bank information. Each command uses one clock cycle, during which command information is transferred on both the positive and negative edge of the clock. LPDDR2-S4 uses a double data rate architecture on the DQ pins to achieve high speed operation. The double data rate architecture is essentially a 4n prefetch architecture with an interface designed to transfer two data bits per DQ every clock cycle at the I/O pins. A single read or write access for the LPDDR2-S4 effectively consists of a single 4n-bit wide, one clock cycle data transfer at the internal SDRAM core and four corresponding n-bit wide, one-half-clock-cycle data transfers at the I/O pins.Read and write accesses to the LPDDR2 are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. For LPDDR2-S4 devices, accesses begin with the registration of an Activate command, which is then followed by a Read or Write command. The address and BA bits registered coincident with the Activate command are used to select the row and the Bank to be accessed. The address bits registered coincident with the Read or Write command are used to select the Bank and the starting column location for the burst access.Prior to normal operation, the LPDDR2 must be initialized.

The KMN5U000ZM is suitable for use in data memory of mobile communication system to reduce not only mount area but also power consumption. This device is available in 162-ball FBGA Type.

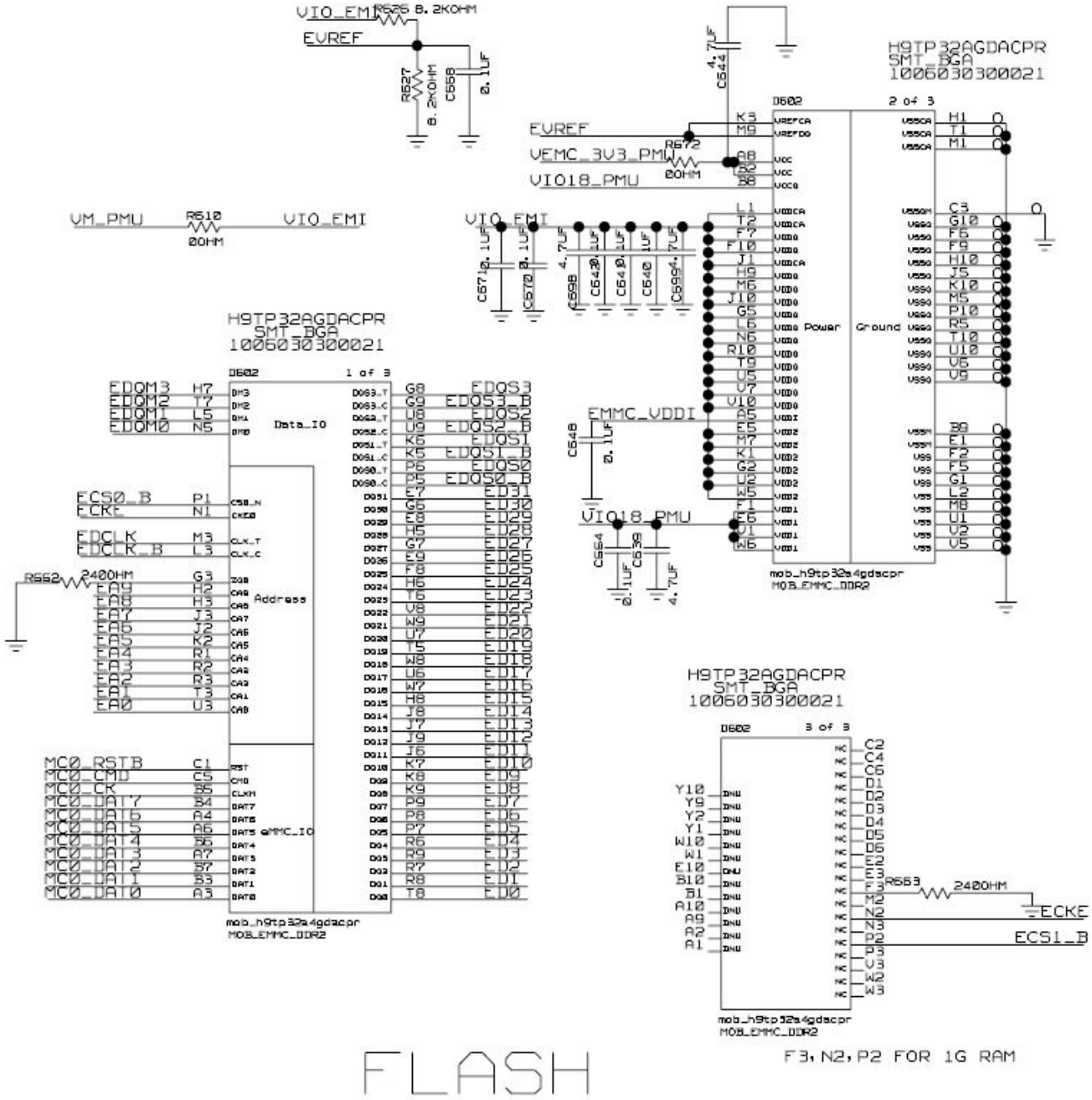
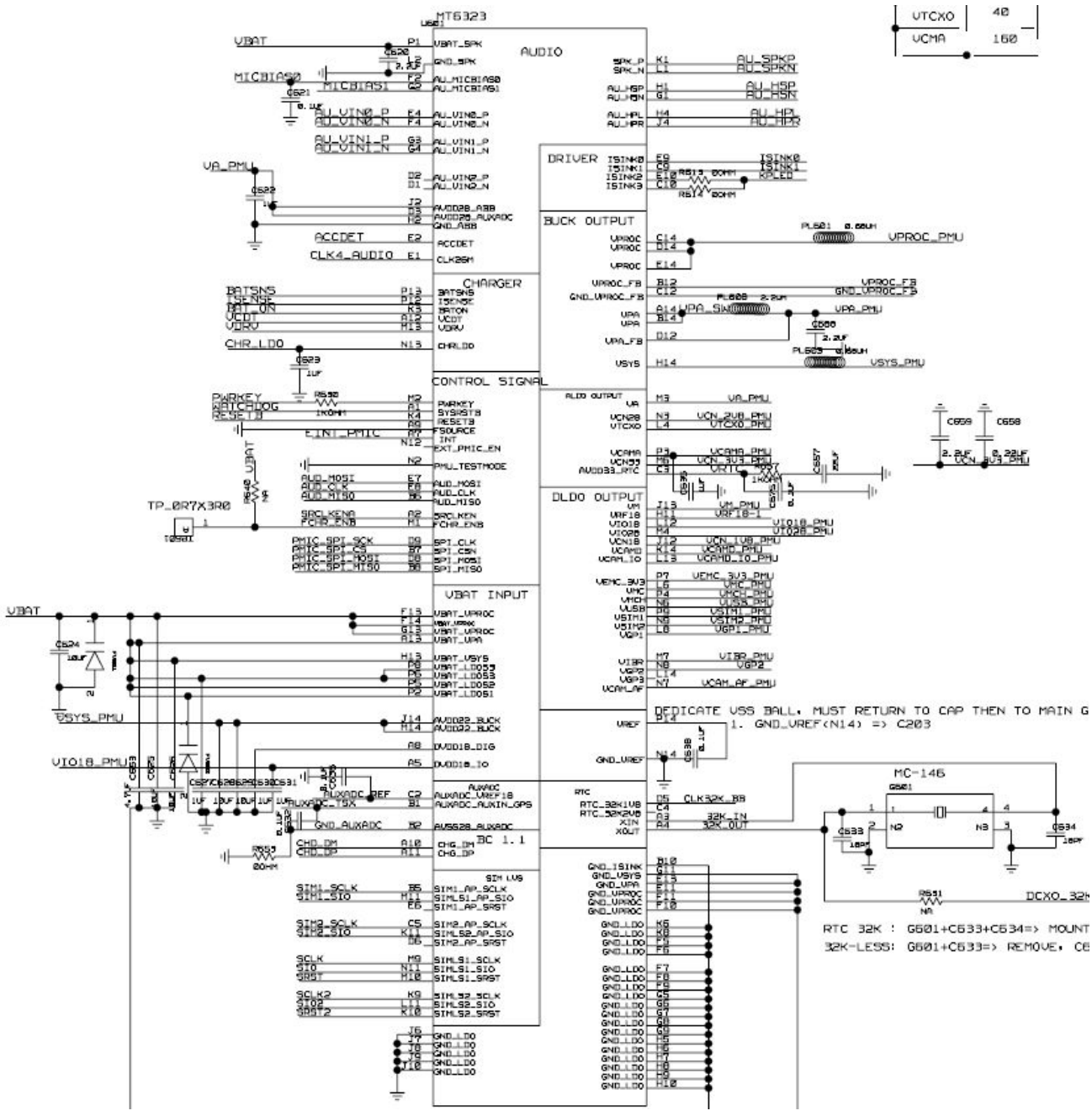


Figure 2-5: Flash memory

2.3.3 Power Manage Unit Interface

A power management is embedded in MT6572 to provide the rich features that an high-end feature phone supports, including Li-ion battery charger, high performance and low quiescent current LDOs, power efficient switching regulator, and drivers for LED and backlight.

The MT6572 offers various low-power features to help reduce system power consumption. MT6572 is also fabricated in an advanced low power 40nm CMOS process, hence providing an overall ultra low leakage solution.



Power on key press input , Low active

Figure 2-6: CPU U501----- Power and Supply part A (Charger\PWR ON\SIM)

Battery charging

The charger controller senses the charger input voltage (CHRIN) from either a standard AC-DC adaptor or an USB charger. When the charger input voltage is within a pre-determined range, the charging process is activated. This detector can resist higher input voltages than other parts of the PMIC. Therefore, if an invalid charging source is detected (> 7.0 V), the charger detector stops the charging process immediately to avoid burning out the chip or even the phone.

After a valid charging source is applied, the detection circuits further check the CHRIN voltage to see if the charger input is high enough. The charging process will be enabled when CHRIN>4V in pre-charge mode (VBAT<3.2V). If VBAT>=3.2V, it requires CHRIN voltage higher than VBAT by 4% to ensure that the battery can be charged up. If the CHRIN voltage becomes lower for some reasons, the charging process will be disabled when CHRIN voltage is no longer higher than VBAT by 2%. The charging ON/OFF status can be observed by the read-only register named CHRDET.

Charging circuit description (U602)

1. Charge Detection

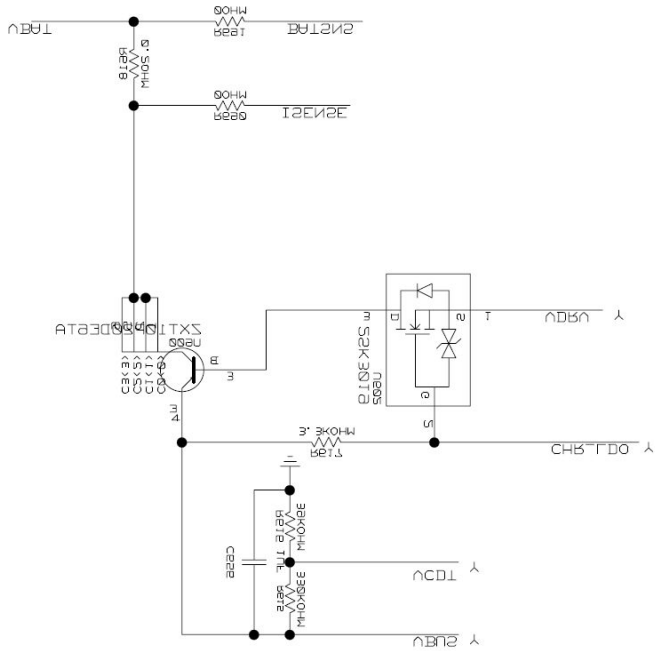


Figure 2-7: charging circuit part

When the charger is active, the charger controller manages the charging phase according to the battery status. During the charging period, the battery voltage is constantly monitored. The battery charger in MT6572 supports pre-charge mode (VBAT<3.2V, switched-off state), CC mode (constant current mode or fast charging mode at the range of 3.2V<VBAT<4.2V) and CV mode (constant voltage mode) to optimize the charging procedure for Li-ion battery.

2. Pre-Charging mode

When the battery voltage is in the UV state, the charger operates in the pre-charge mode. There are two steps in this mode. While the battery voltage is deeply discharged below 2.2V, a IPRECC0 trickle charging current applies to the battery.

When the battery voltage exceeds 2.2V, the closed-loop pre-charge is enabled. The voltage drop across the external Rsense resistor is kept around 25mV (Typ.).

3. Constant Current Charging Mode

As the battery is charged up and over 3.2V, it can switch to the CC mode. (CHREN should be high) In CC mode, several charging currents can be set by programming registers or the external Rsense resistor. The charging current can be determined by Vch,ref/Rsense, where Vch,ref is programmed by registers. For example, if Rsense is selected as 0.2Ohm, the CC mode charging current can be set from 50mA to 800mA. It can accommodate the battery charger to the various charger inputs with different current capability.

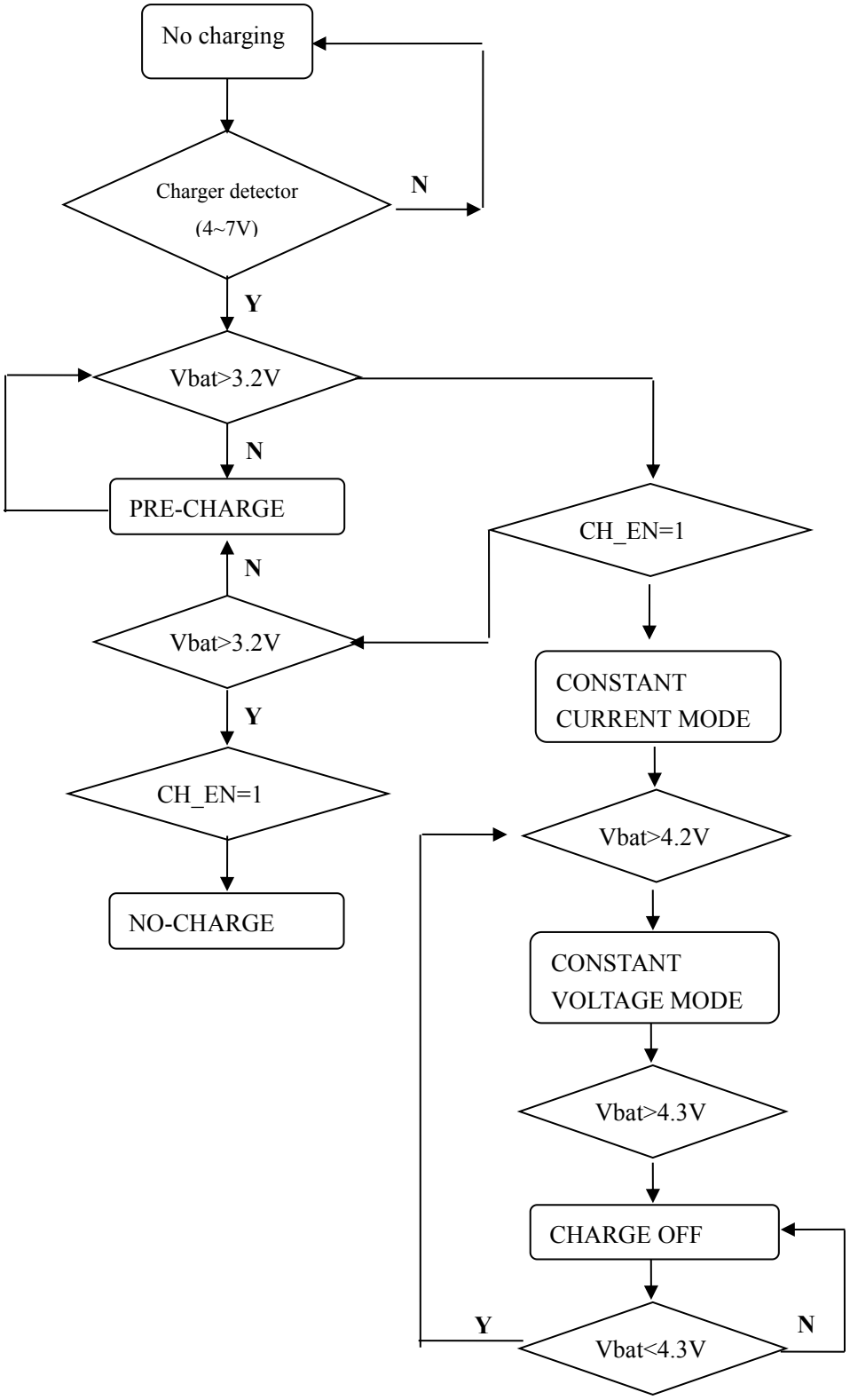
Due to process variation, the charging current may vary form chip to chip. To compensate for this variation, the offset registers can be set in MT6572. The PMIC reads this compensation value and applied the charging current offset when the phone is in the charging state. This compensation value could be obtained during the calibration process in phone production, or it could be constantly observed by the BB while the phone is charging

4. Constant Voltage Charging Mode

If the battery voltage has reached the final value, said 4.2V, a constant voltage is applied to the battery and keeps it at 4.2V. After that, the charging current becomes smaller and smaller. When the charging current is less than a pre-determined threshold for a while, it enters the charge complete state. The charging process will be terminated by setting CHREN=0. The charge complete detection and CHREN control are managed by BB/SW.

Once the battery voltage exceeds 4.3V for any reason, the hardware over voltage protection (OV) will take action and turn off the charger immediately to prevent permanent damage to the battery.

When charging, the PMIC uses GATEDRV pin to control the current flow through the base of the external BJT. The charging current from the collect BJT of is sensed by the voltage drop across the external Rsense resistor (Typ. 0.2 Ω). Then the charging controller and the external components (NMOS,BJT, Rsense and battery) form a regulated charging loop.


No charging
Charger detector
(4~7V)
N
Y
Vbat>3.2V
N
PRE-CHARGE
N
Vbat>3.2V
Y
CH_EN=1
NO-CHARGE
CH_EN=1
CONSTANT
CURRENT MODE
Vbat>4.2V
CONSTANT
VOLTAGE MODE
Vbat>4.3V
CHARGE OFF
Y
Vbat<4.3V
N

Dual SIM Interface

There are two SIM card interface modules to support two SIM cards simultaneously. The SIM card interface circuitry of PMU meets all ETSI and IMT-2000 SIM interface requirements. It provides level shifting needs for low voltage GSM controller to communicate with either 1.8V or 3V SIM cards. All SIM cards contain a clock input, a reset input, and a bi-directional data input/output. The clock and reset inputs to SIM cards are level shifted from the supply of digital IO (Vio) of baseband to the SIM supply (Vsim). The bi-directional data bus is internal pull high to Vsim via 5KΩ resistor.

All pins that connect to the SIM card (Vsim, SRST, SCLK, SIO) withstand over 5kV HBM (human body mode) ESD. In order to ensure proper ESD protection, careful board layout is required.

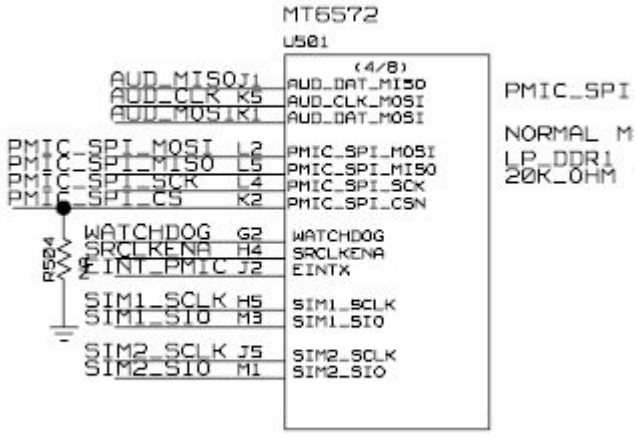


Figure 2-8: Dual SIM circuit part

Power on Sequence

The PMU handles the powering ON and OFF of the handset. There are three ways to power-on the handset system(When VBAT>=3.2V):

- Pulling PWRKEY low (User push PWRKEY)
- Pulling PWRBB high (Baseband BB_WakeUp)
- Valid charger plug-in

Pulling PWRKEY low is a normal way to turn on the handset. That will turn on VCORE,

VPROC, VIO1V8, VIO28/VM12/VM12_INT and VUSB/VTCXO/VA25/VA12/VMC as long as the PWRKEY is kept low. The microprocessor then starts and pulls PWRBB high. After that PWRKEY can be released. Pulling PWRBB high will also turn on the handset. This is the case when the alarm in the RTC expires.

Besides, applying a valid external supply on CHRIN will also turn on the handset. However, If the battery is in UV state (VBAT<3.2V), the handset can't be turned-on in any way.

The UVLO function in the MT6572 prevents system startup when initial voltage of the main battery is below the 3.2V threshold. When the battery voltage is greater than 3.2V, the UVLO comparator switches and the threshold is reduced to 2.9V. This allows the handset to start smoothly unless the battery decays to 2.9V and below.

Once the MT6572 enters UVLO state, it draws very low quiescent current. The VRTC LDO is still active until the DDLO disables it.

PMU ---LDO

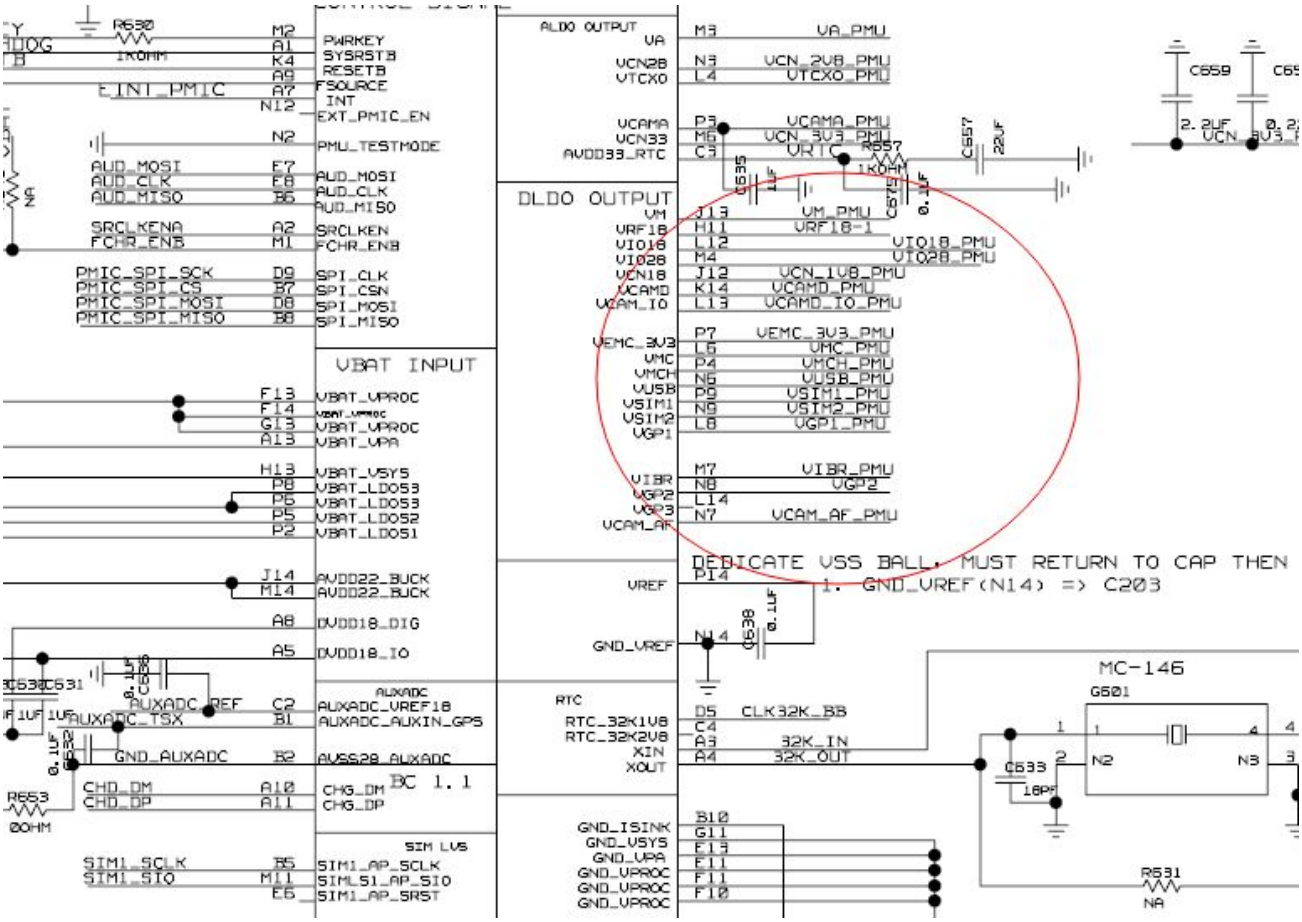
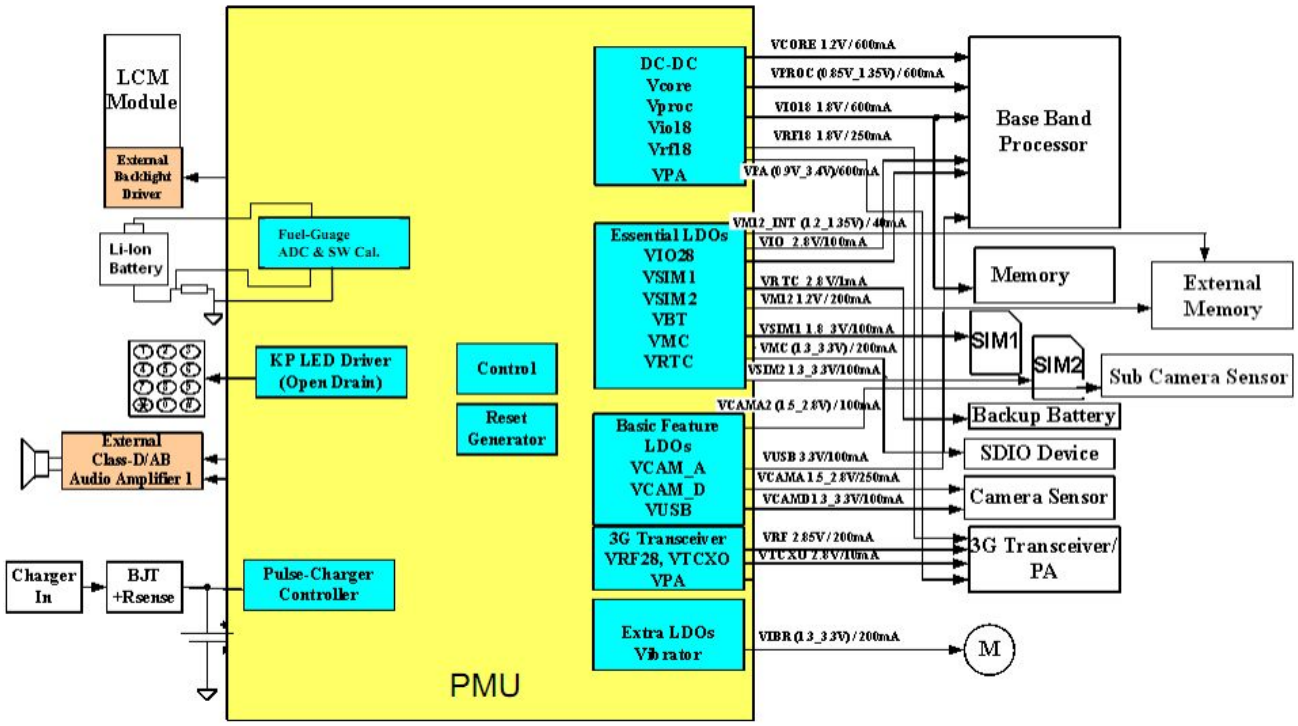


Figure 2-9: CPU U601----- Power and Supply part B



	Symbol	Vout (V)	Iout (mA)	Setting
Buck	VPA	0.9 ~ 3.4 with 0.1 step	600	
	VPROC	0.85 ~ 1.35	600	
	VRF18	1.8	250	
	VCORE	1.2	600	
	VIO1V8	1.8	600	
RF LDO	VRF	2.85	200	
Analog LDO	VTCXO	2.8	10	
	VCAMA	1.5/1.8/2.5/2.8	250	
	VCAMA2	1.5/1.8/2.5/2.8	100	
Digital LDO	VM12	1.2	200	
	VM12_INT	1.2 ~ 1.35	40	
	VIO28	2.8	100	
	VSIM	1.8/3.0	100	
	VUSB	3.3	100	
	VCAMD	1.3/1.5/1.8/2.5/2.8/3.0/3.3	100	
	VCAMD2	1.3/1.5/1.8/2.5/2.8/3.0/3.3	100	
	VSIM2	1.3/1.5/1.8/2.5/2.8/3.0/3.3	100	
	VMC	1.3/1.5/1.8/2.5/2.8/3.0/3.3	200	
Vibrator	VIBR	1.3/1.5/1.8/2.5/2.8/3.0/3.3	200	
RTC	VRTC	2.8	1	

Figure 2-10: PMU LDO output voltage list

2.3.4 Camera Management

Camera ISP: 3MP

- MIPI/Parallel I/F, EIS, face detection

Image Signal Processor

– Integrated image signal processor supporting 3MP up to 15fps

~ Supports electronic image stabilization

~ Supports video stabilization

~ Supports local contrast enhancement

~ Supports preference color adjustment

~ Supports noise reduction

~ Supports edge enhancement (sharpness)

~ Supports face detection and visual tracking

– Supports 2 channel MIPI CSI-2 high-speed camera serial interface

~ Supports Xenon flash

~ Hardware JPEG decode: baseline/progressive with YUV422/YUV420/JFIF formats with 35M pixel/sec

~ Hardware JPEG encoder: baseline coding with 75M pixel/sec

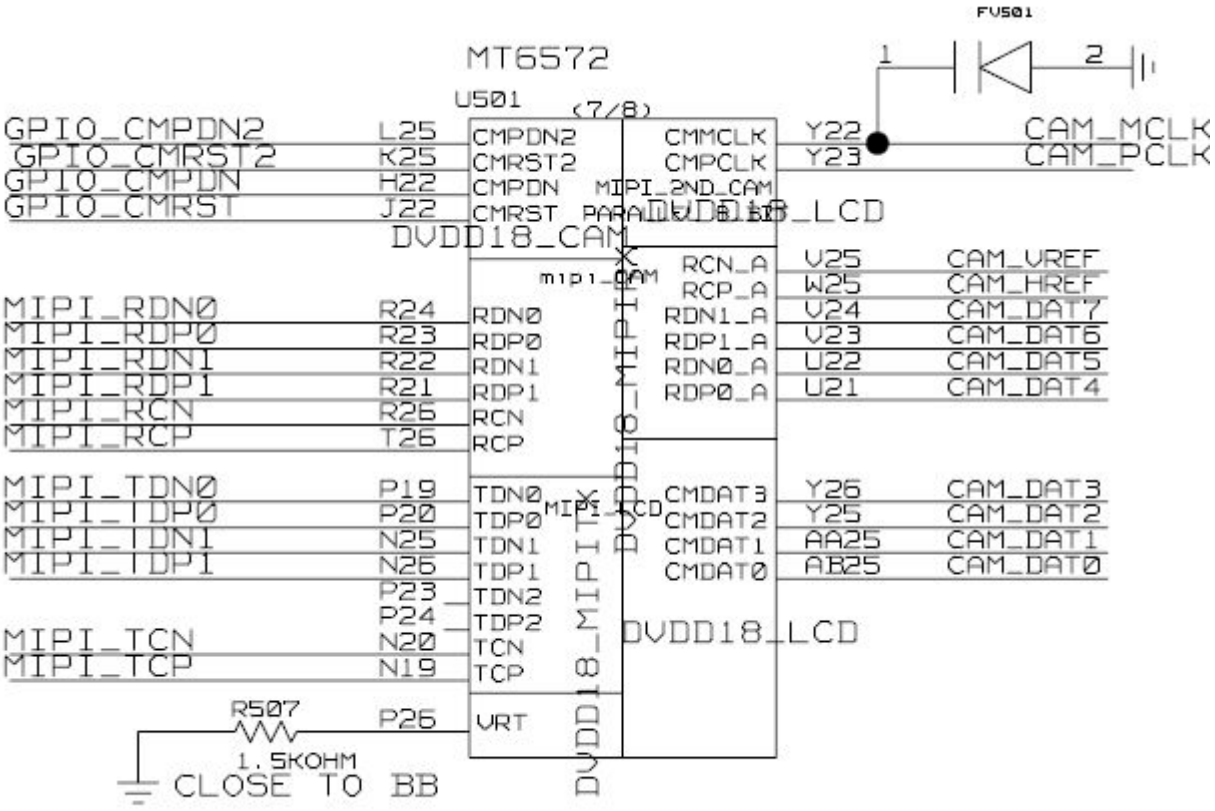
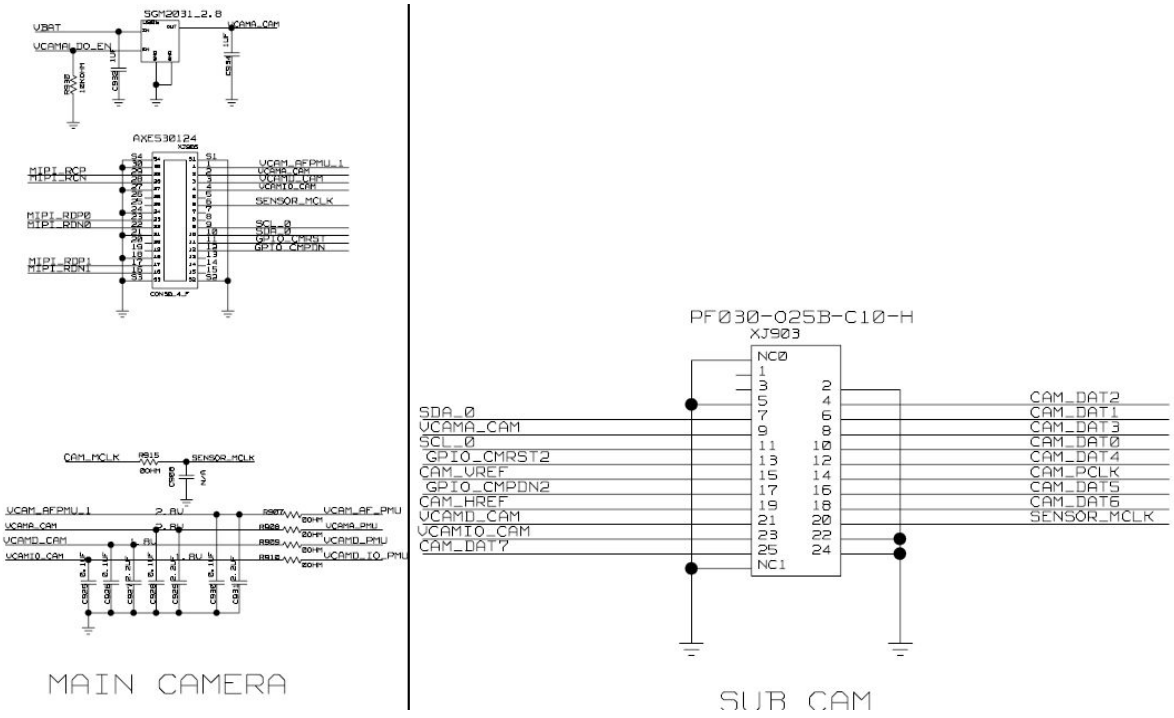


Figure 2-11: CPU U501----- Camera Processor



2.3.5 LCM Management

WVGA(480*800) LCM

– Supports landscape or portrait panel resolution up to qHD (960x540)

- Supports 8/9/16/18/24-bit host interface (MIPI DBI)
- Supports 8/9/16/24/32-bit serial interfaces
- Supports 16/18/24-bit RGB interfaces (MIPI DPI)
- MIPI DSI interface (2 data lanes)
- Embedded LCD gamma correction
- Support true colors
- 6 overlay layers with per-pixel alpha channel and gamma table
- Supports spatial dithering
- Supports 32x32 hardware cursor
- Supports NTSC/PAL TV-Out
- Supports side-by-side format output to stereo 3D panel in both portrait and landscape modes
- Supports external HDMI Tx bridget with high-definition 720p video output

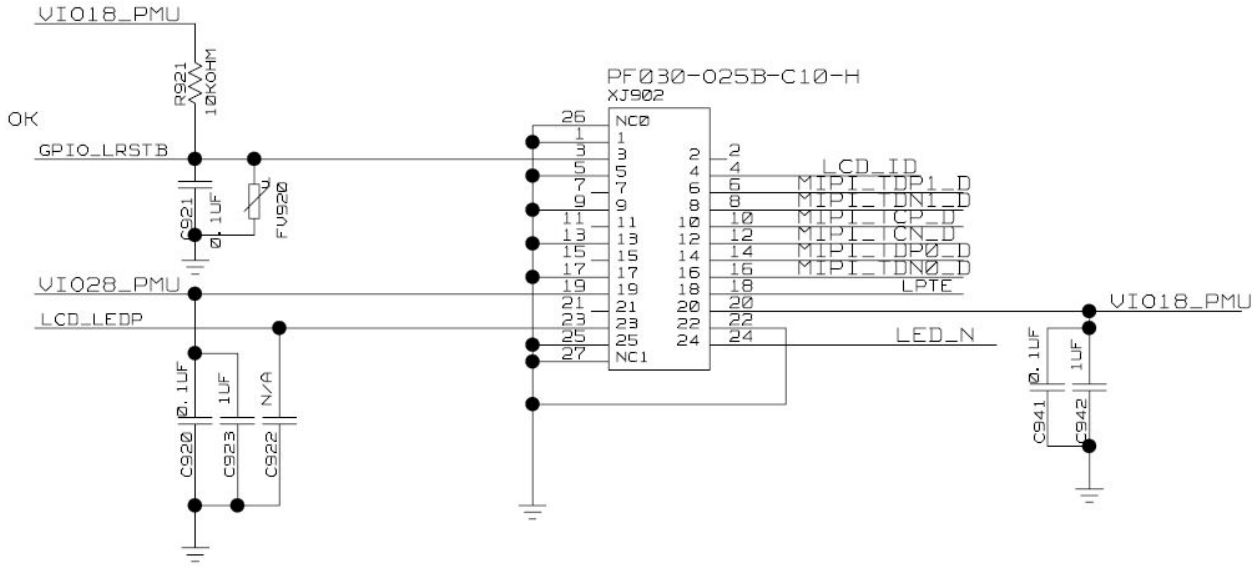


Figure 2-14: LCM connector

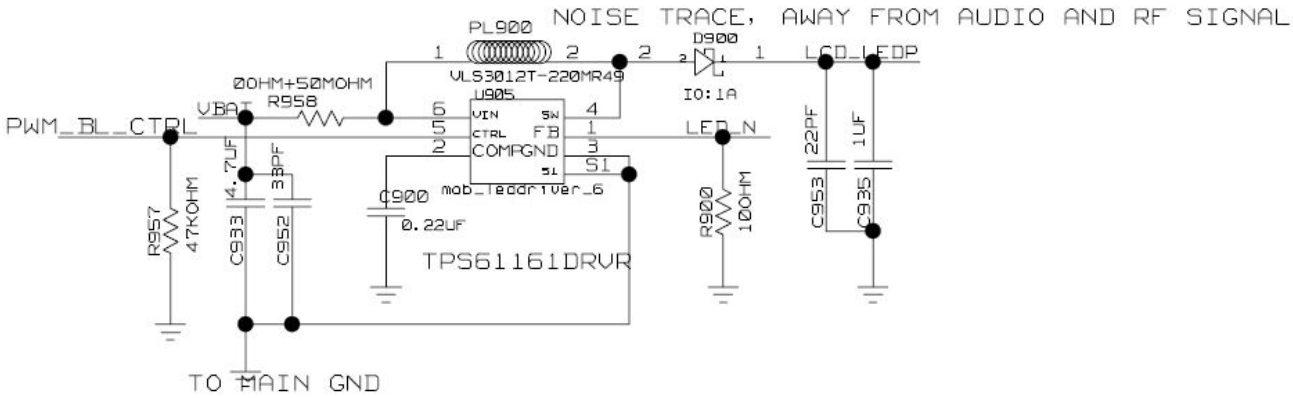


Figure 2-14: LCM Backlight Driver circuit

2.3.6 Audio Management

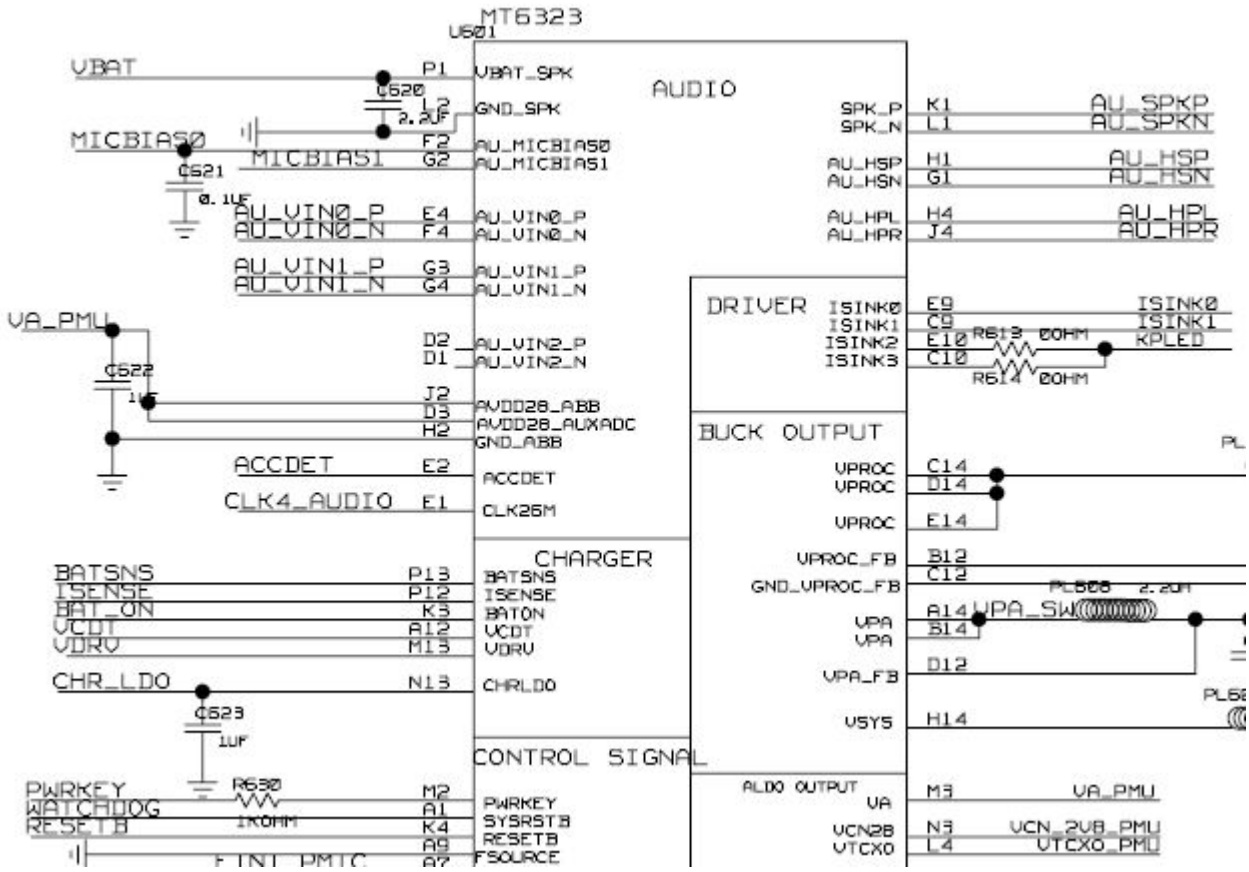


Figure 2-15 CPU U200-----Audio processor part

Audio circuit description

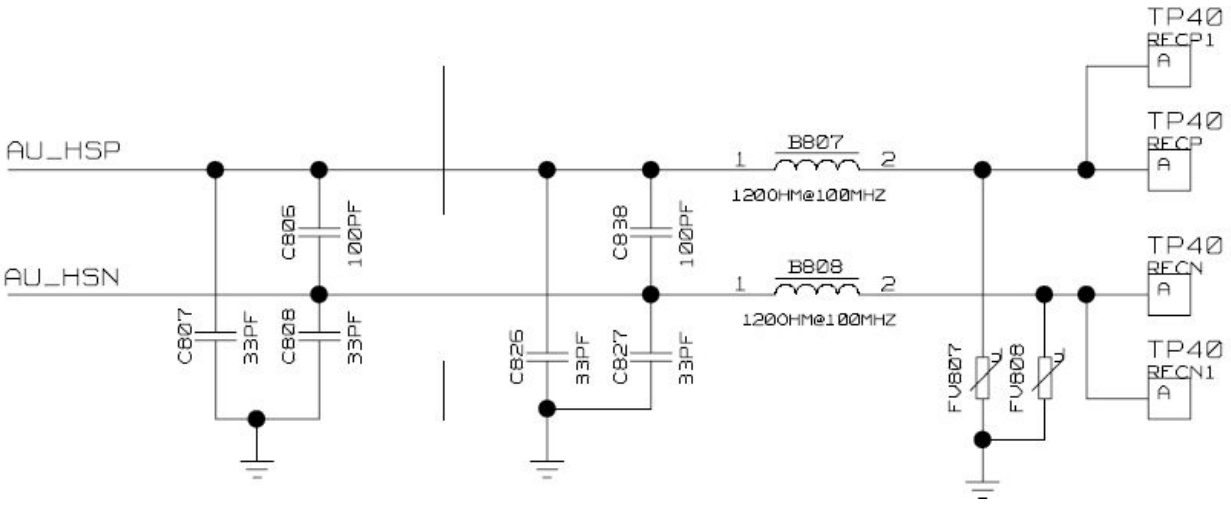


Figure 2-16: Audio output to Receiver

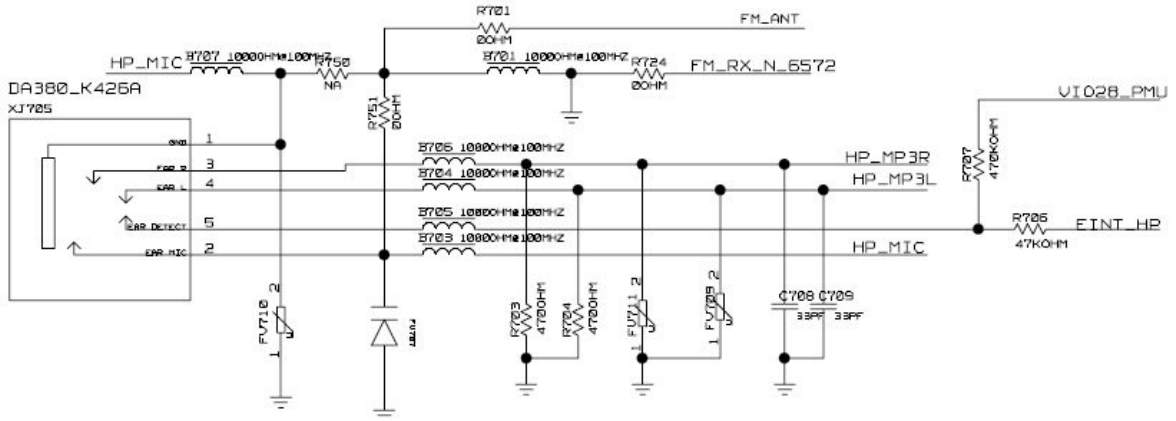


Figure 2-17: Earphone circuit

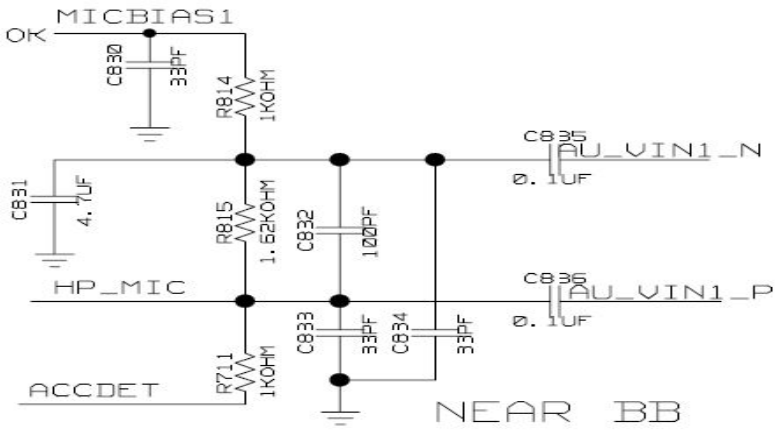


Figure 2-18: Audio circuit of Handset MIC

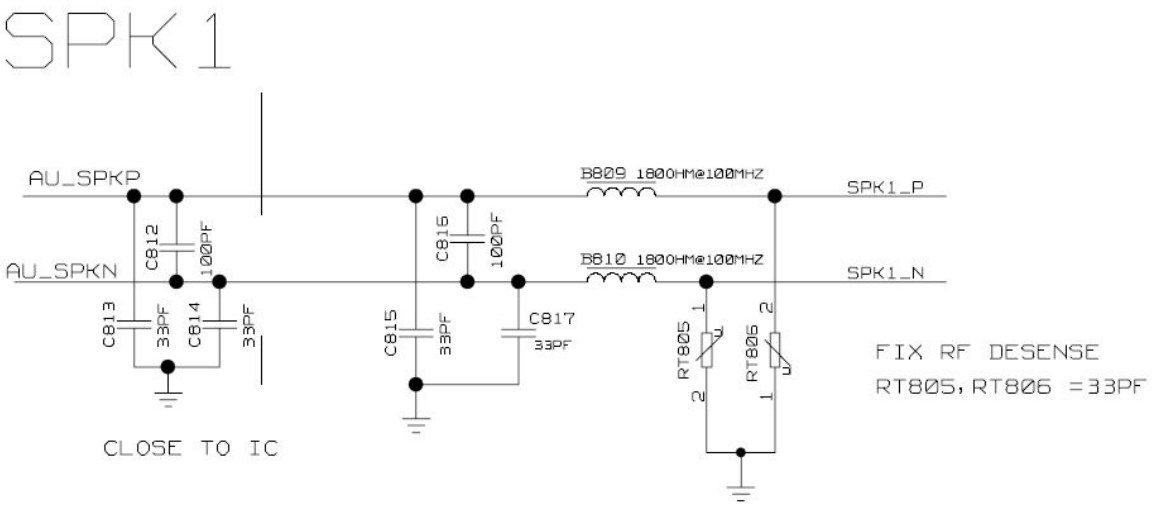
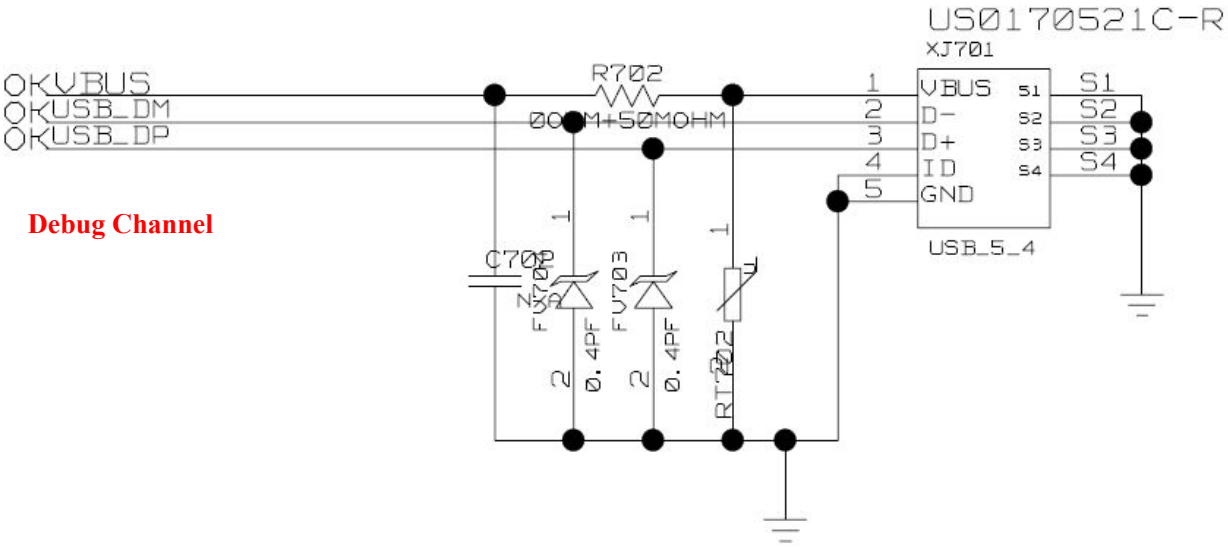


Figure 2-19: Ring tong circuit

2.3.7 I/O interface circuit description (IO291)

Download data / USB communicate channel



Debug Channel

Figure 2-21: I/O interface circuit

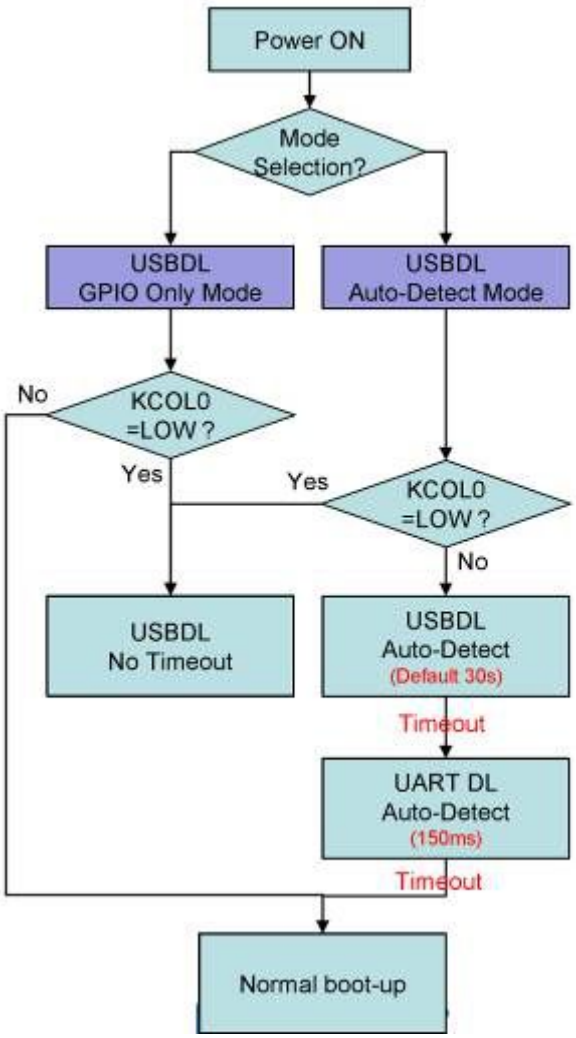
Bootrom USBDL Flow

- How to enter bootrom USB download mode?

– Auto-Detect Mode (default setting)

– GPIO Only Mode

(key matrix KCOL0 tie to GND)



2.3.8 4in1 combo module circuit

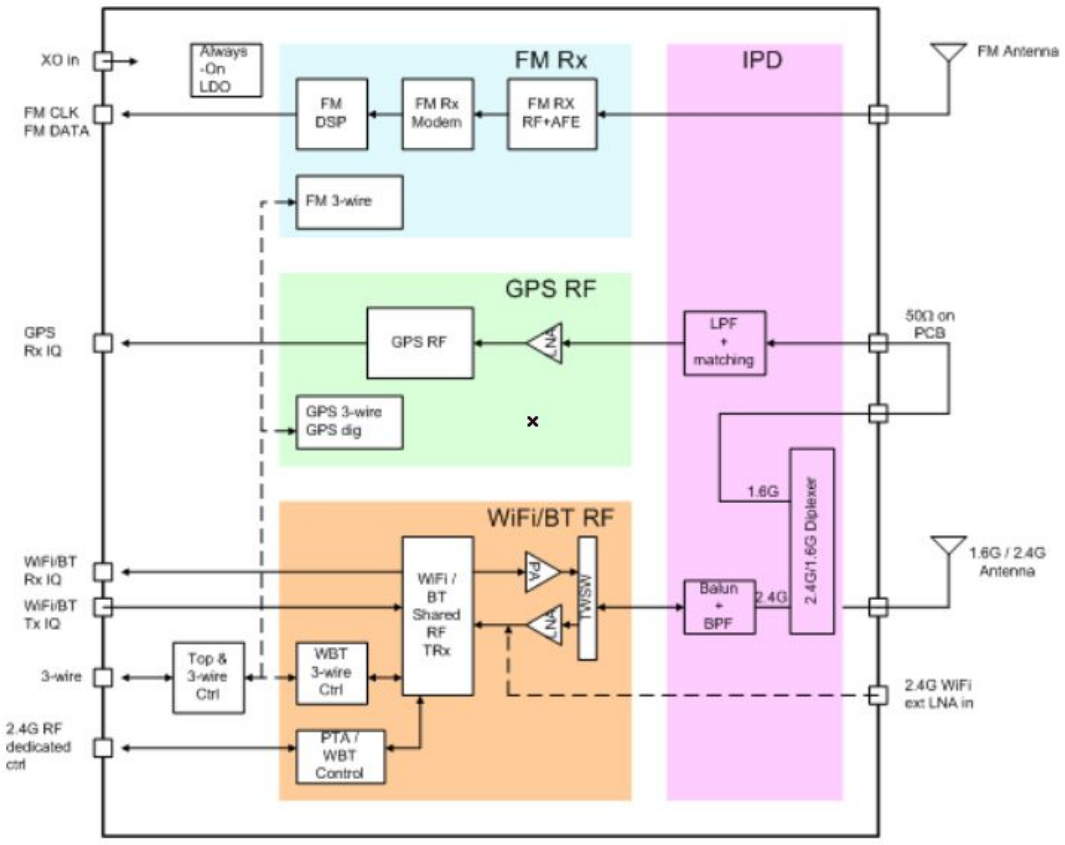
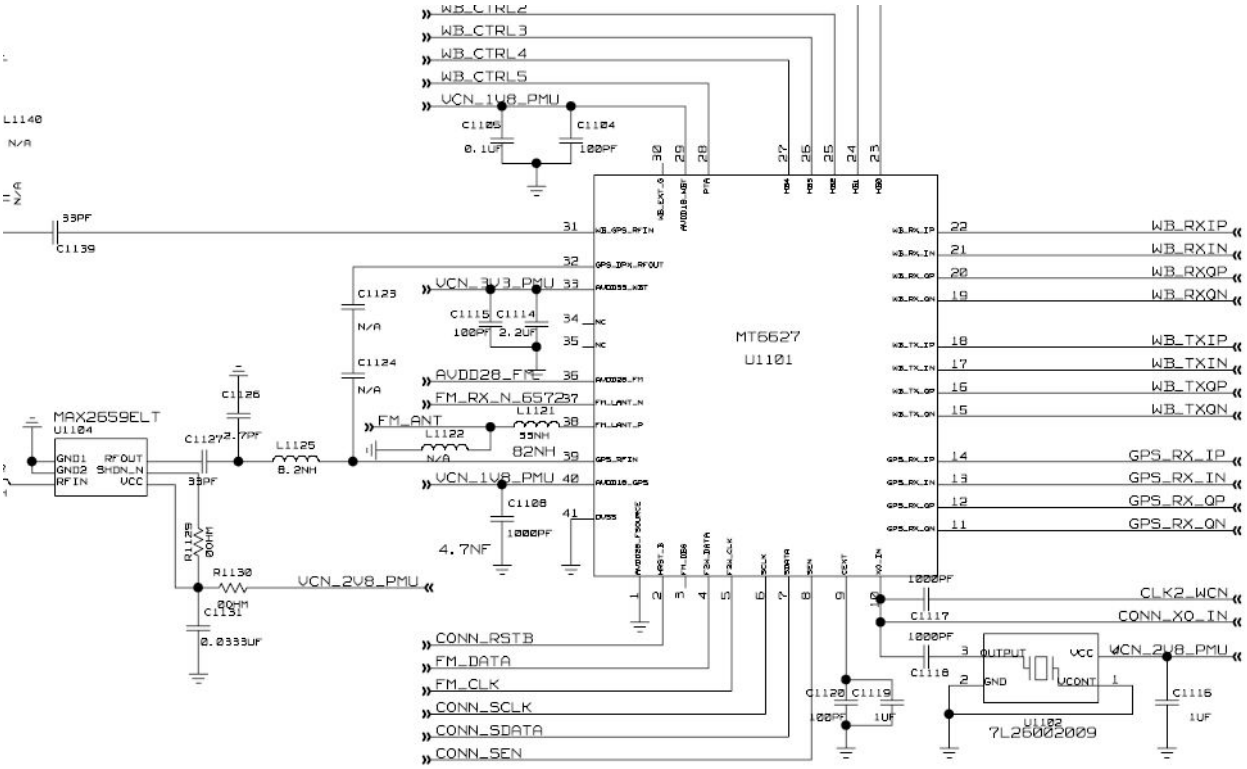
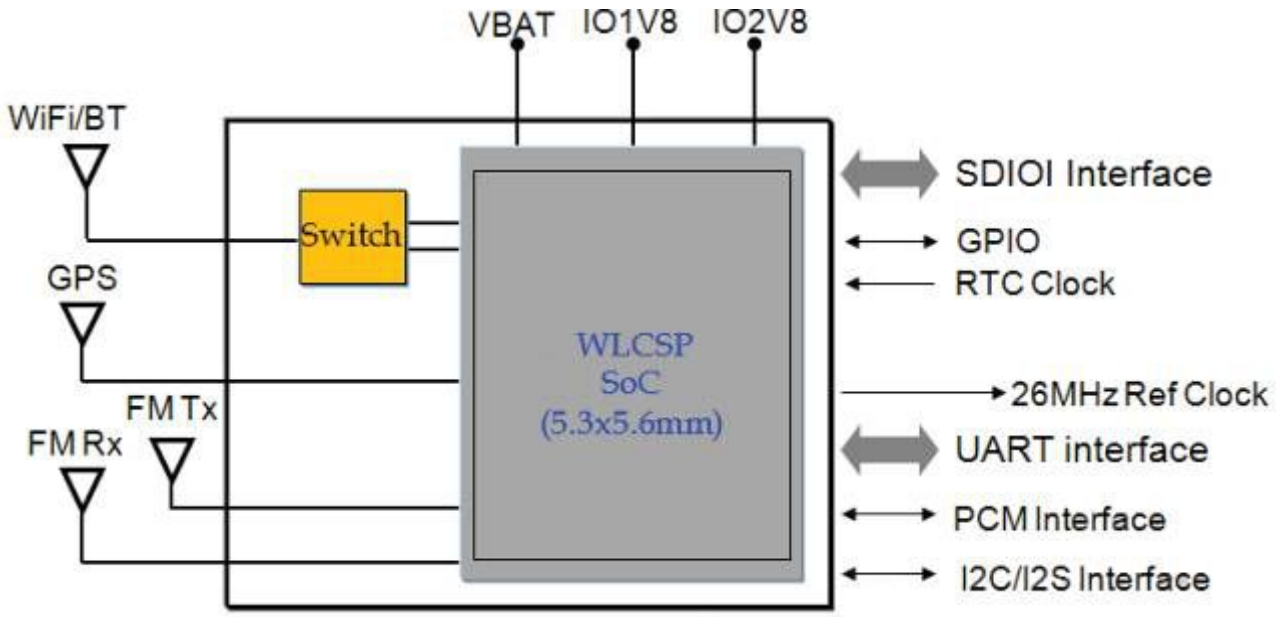


Figure 2-25: Combo module circuit diagram

Specification:

- **WiFi/BT/GPS/FM Tx/Rx full-featured combo module**
- **WiFi self-calibration function embedded**
- **Supported WiFi 11b/g /n features**
- **Supported WiFi SDIO 2.0 (4-bits and 1-bit up to 50MHz)**
- **Bluetooth specification 3.0+HS (802.11 AMP) compliance**
- **Supported Bluetooth 4.0, BT Low Energy (LE)**
- **GPS/GALILEO/QZSS/SBAS(WAAS/MSAS/EGNOS/GAGAN) support**
- **Best GPS sensitivity: -165 dBm tracking sensitivity, -160 hot start sensitivity.**
- **Supported FM 76-108MHz band with 50KHz step.**
- **Supported FM RDS/RBDS**


WB_CTRL3
WB_CTRL4
WB_CTRL5
VCN_1V8_PMU
MT6627
U1101
WB_RXIP
WB_RXIN
WB_RXQP
WB_RXQN
WB_TXIP
WB_TXIN
WB_TXQP
WB_TXQN
GPS_RX_IP
GPS_RX_IN
GPS_RX_QP
GPS_RX_QN
MAX2659ELT
U1104
VCN_3V3_PMU
AVDD28_FM
FM_RX_N_65723
FM_ANT
VCN_1V8_PMU
VCN_2V8_PMU
CLK2_WCN
CONN_XO_IN
VCN_2V8_PMU
CONN_RSTB
FM_DATA
FM_CLK
CONN_SCLK
CONN_SDATA
CONN_SEN
7L26002009


VBAT
IO1V8
IO2V8
WiFi/BT
GPS
FM Tx
FM Rx
Switch
WLCSP
SoC
(5.3x5.6mm)
SDIOI Interface
GPIO
RTC Clock
26MHz Ref Clock
UART interface
PCM Interface
I2C/I2S Interface

- WiFi / BT / GPS / FM combo
- Size : 6.3 x 5.4x1.0 mm
- Pad Pitch : 0.5mm
- Support Interface:

– SDIO (WiFi)

– UART (BT / GPS / FM)

•Block Diagram

– PCM / I2S (BT)

– I2C (FM)

– FM analog audio input/output

- Ref Clock Source

– Supported Xtal / TCXO / PCTCXO

Chapter 3

RF Circuit Analysis

The MT6166 is a RF transceiver targeted at high speed 2G/3G-FDD/TDD muli-mode smart phone and tablet computers implanted in 40nm COM.The RF transceiver function is fully integrated.

Key faeatures

- Direct Conversion (3G), Two Point Modulation (TPM) for GMSK and Small Signal Polar for 8-PSK
  - No external SAW filters required for transmitter (WCDMA//GGE)
  - Dedicated power detection circuits for power control over specific power range
- Hybrid Direct-Conversion (3G) / Low-IF (GGE, DC-HSDPA) receiver
  - *No external SAW filters required for receiver (GGE)*
- Low supply current & operation directly from DC-DC converter
- 26MHz internal DCXO or external VCTCXO operation (with integrated AFC DAC)
  - Three low noise additional Clock Drivers for clocking connectivity / peripheral IC's
  - Ultra Low power 32KHz mode
- Support RF Calibration features for key Rx and Tx specifications (Image rejection, LO feedthrough, DC offset)
- Temperature Measurement sub-system

Transceiver Description

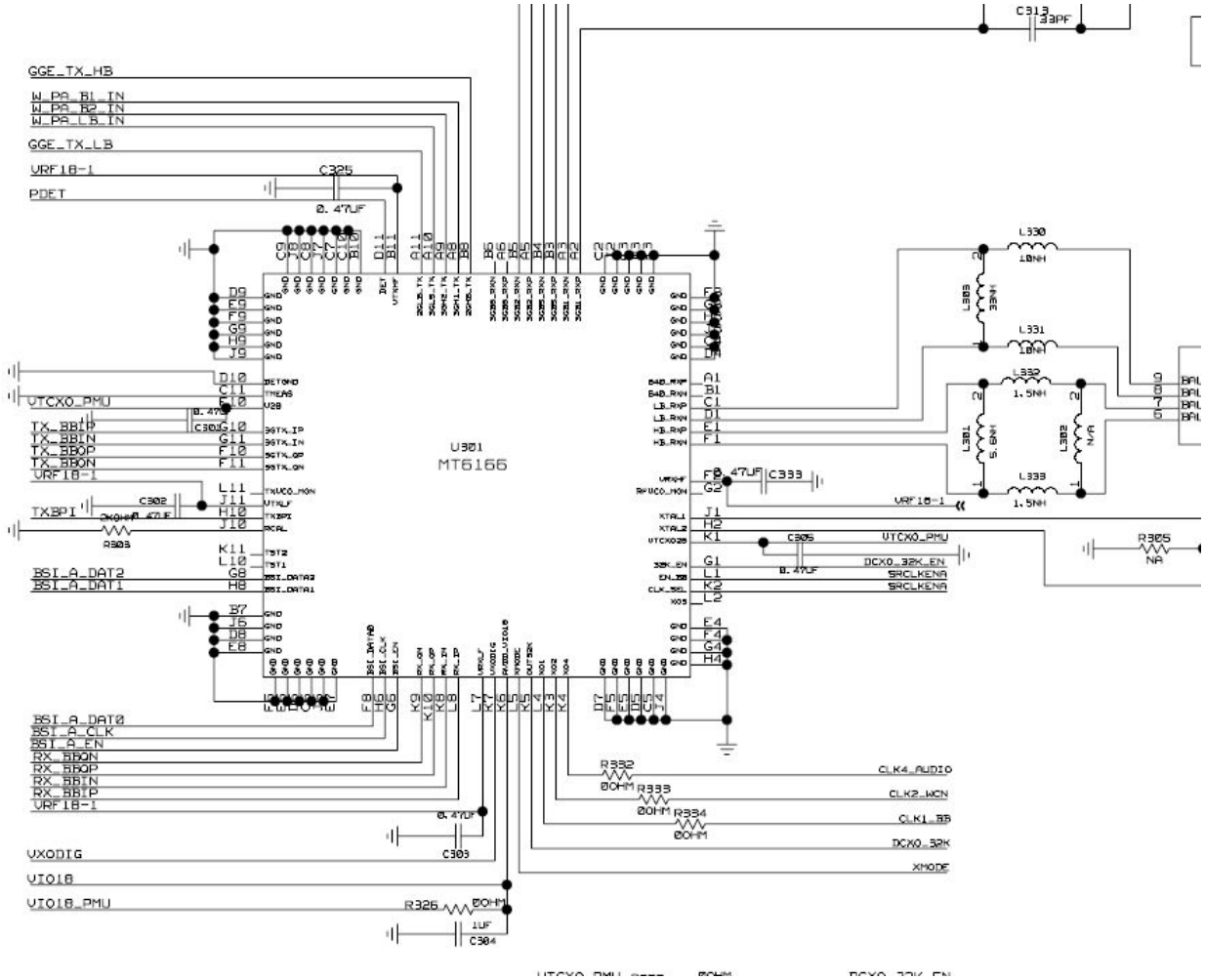


Figure 3-5: Receive Transceiver circuit

Mobile solution diagram----GGE(GSM/GPRS/EDGE)

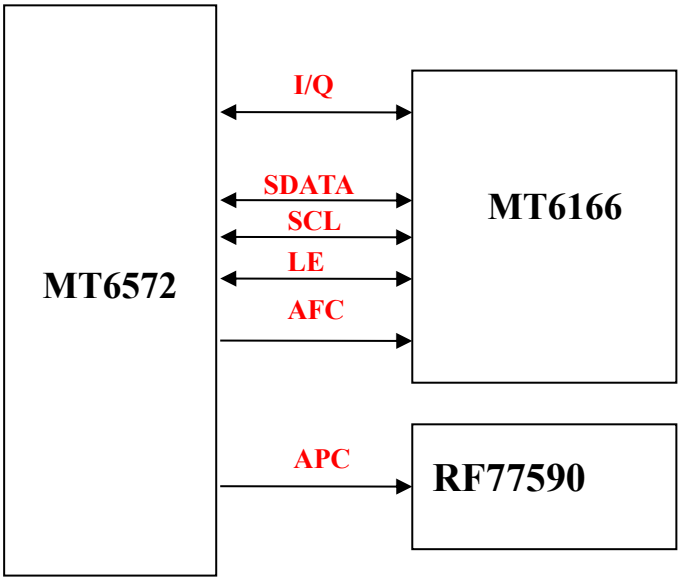


Figure 3-1: RF Interface Block Diagram

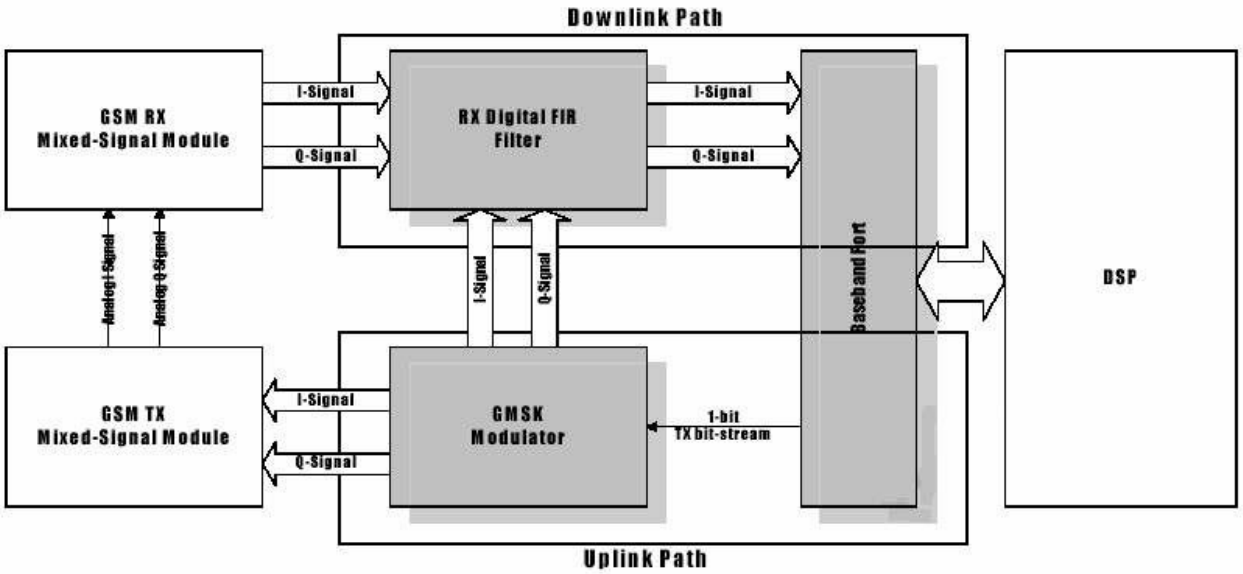
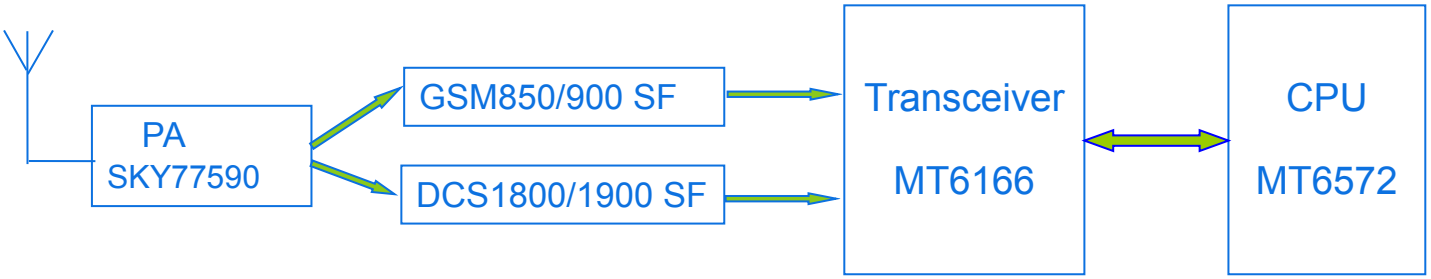


Figure 3-2: IQ Signal Process Block Diagram

RF receiver circuit description



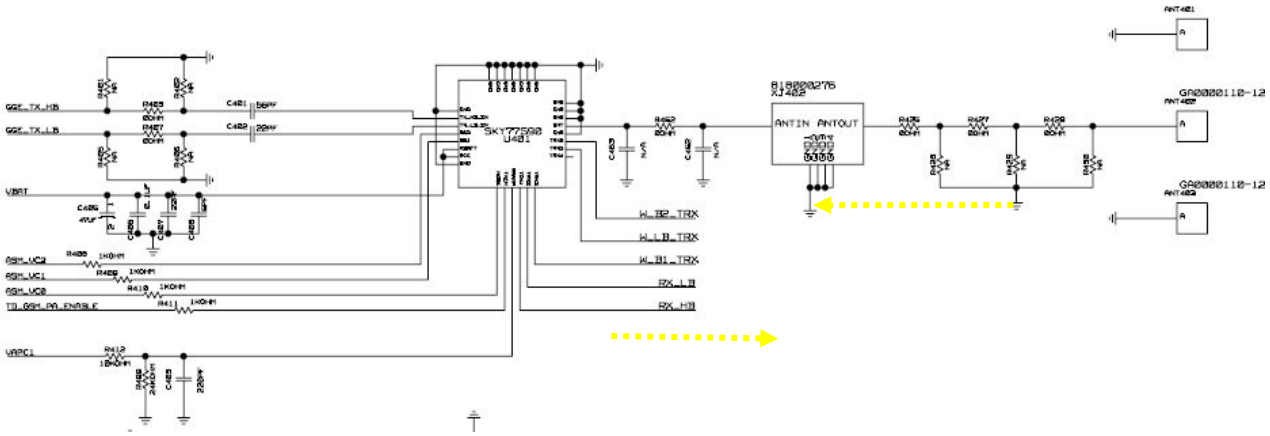


Figure 3-3: PA switcher circuit

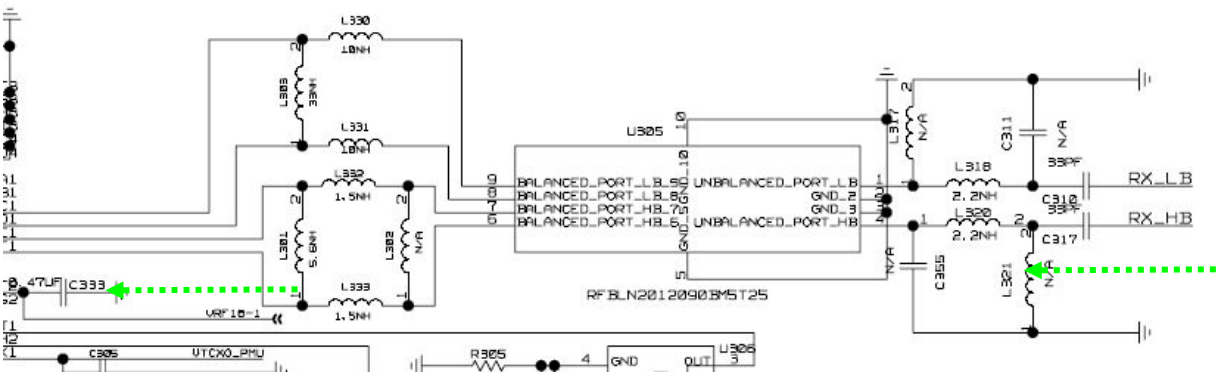
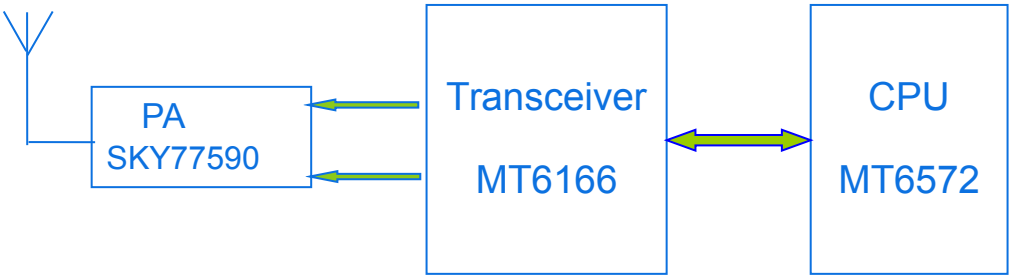


Figure 3-4: Receive saw-filter circuit

RF transit circuit description



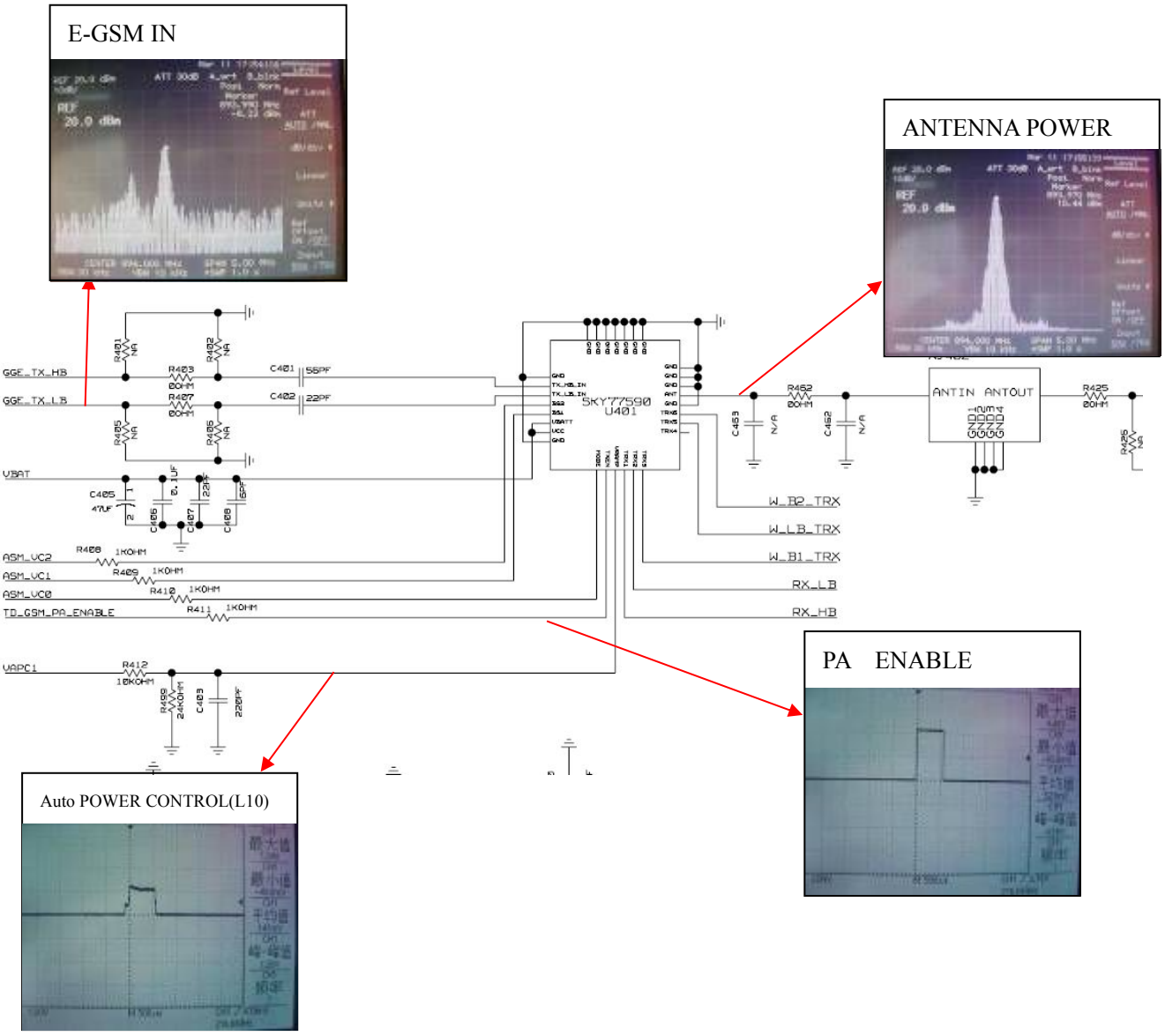


Figure 3-4: RF transit circuit

Mobile solution diagram----WCDMA

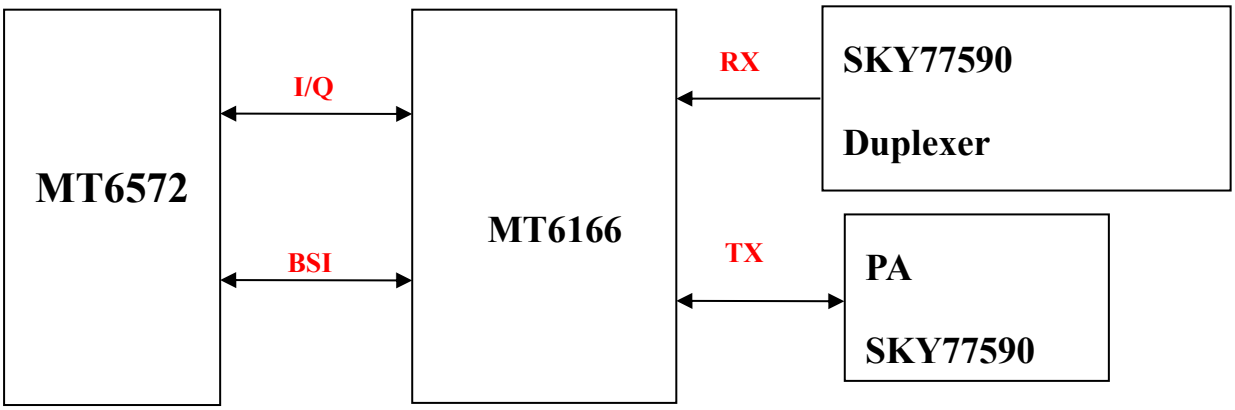


Figure 3-1: RF Interface Block Diagram

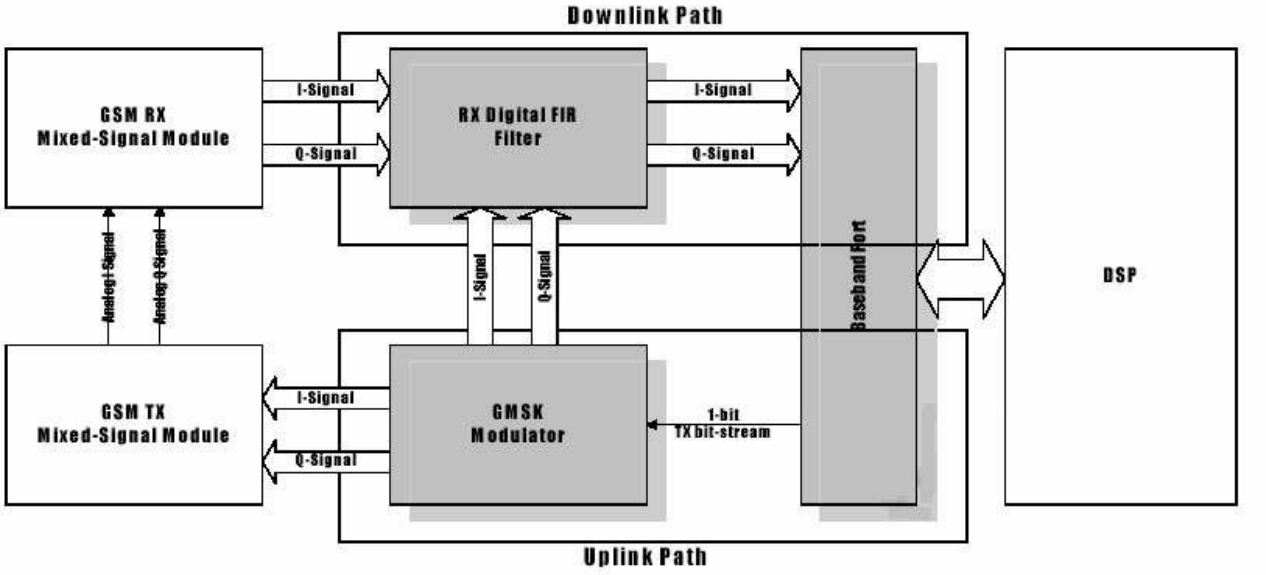
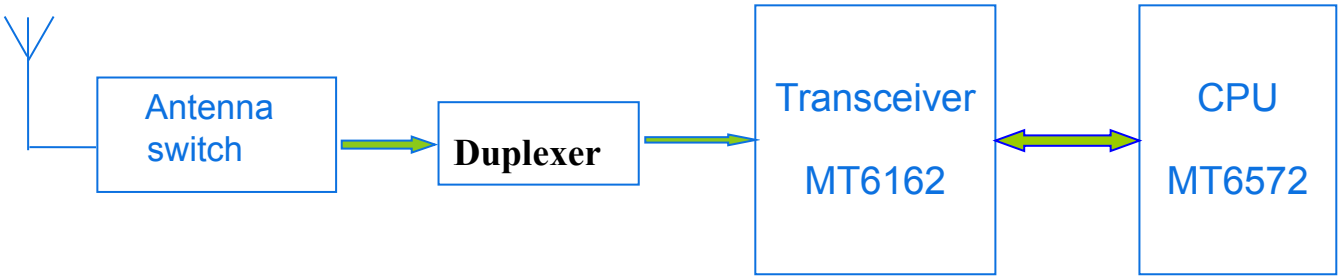


Figure 3-2: IQ Signal Process Block Diagram

RF receiver circuit description



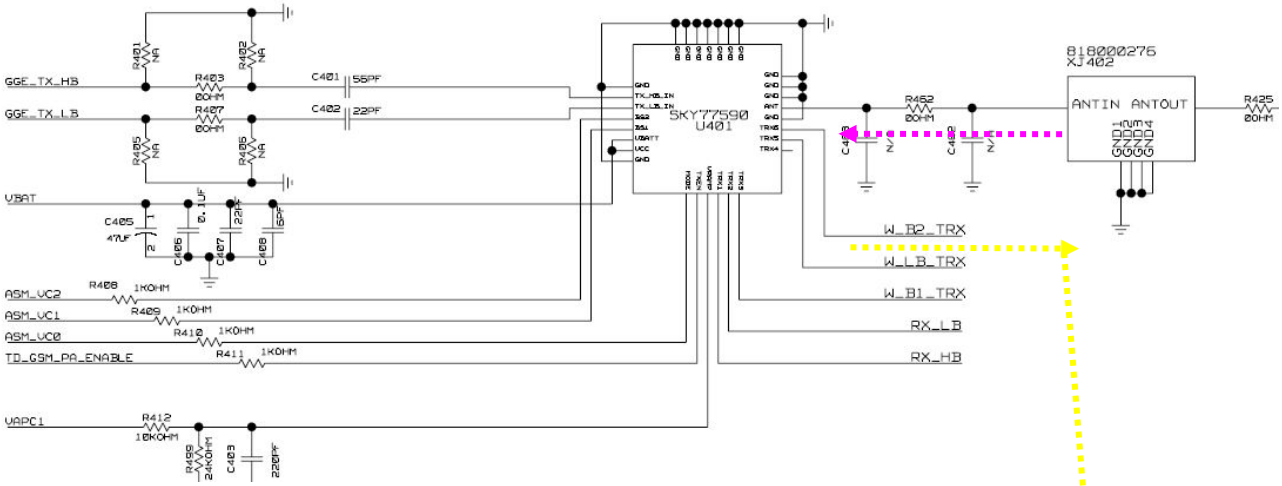


Figure 3-3: PA switcher circuit

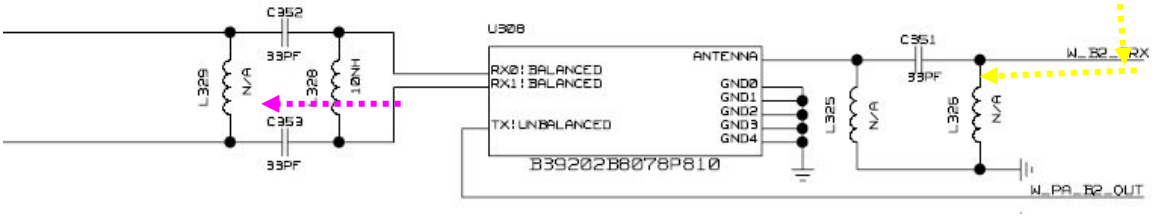


Figure 3-4: Receive saw-filter circuit

RF transit circuit description

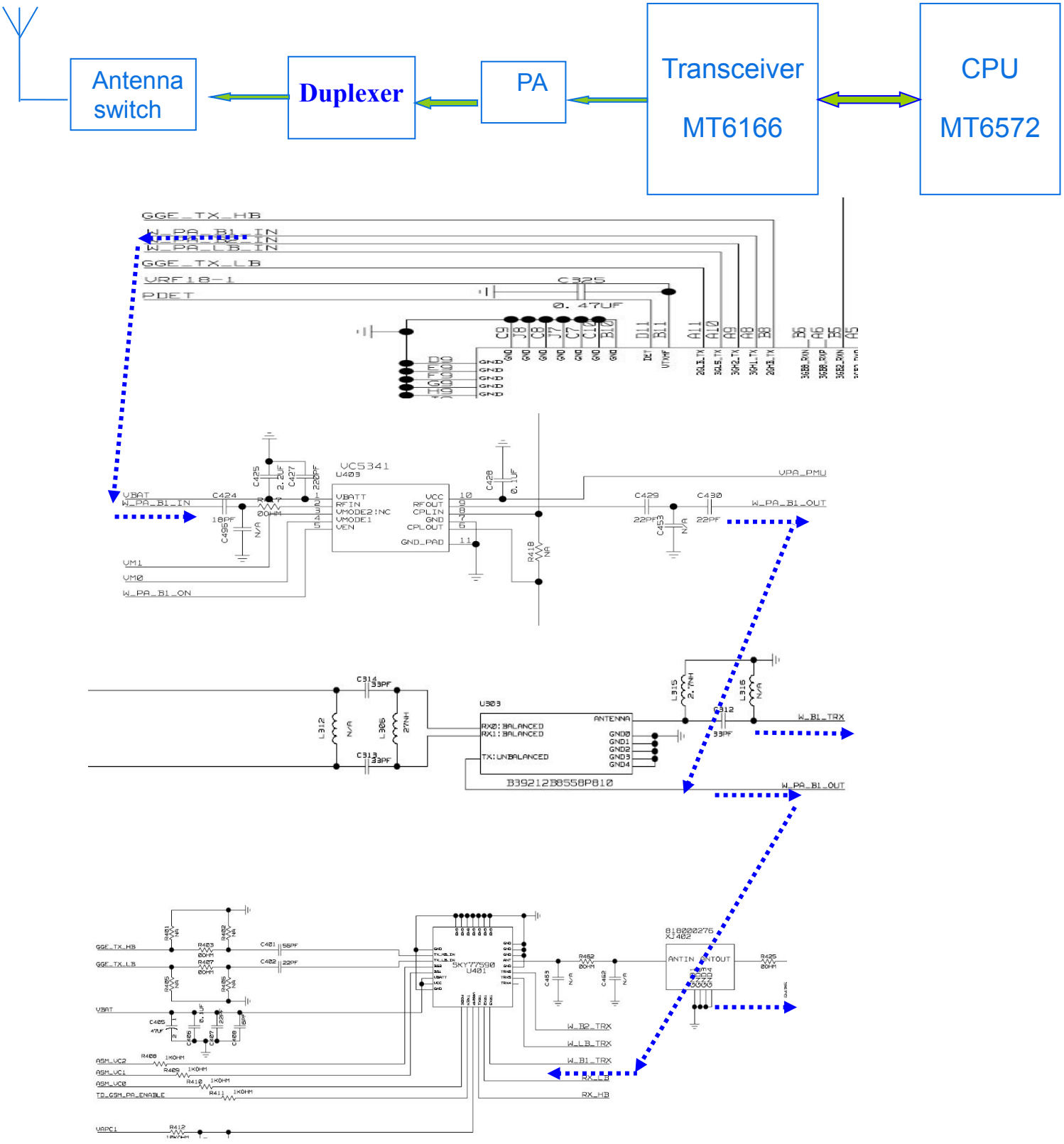


Figure 3-4: RF transit circuit

.pin outs

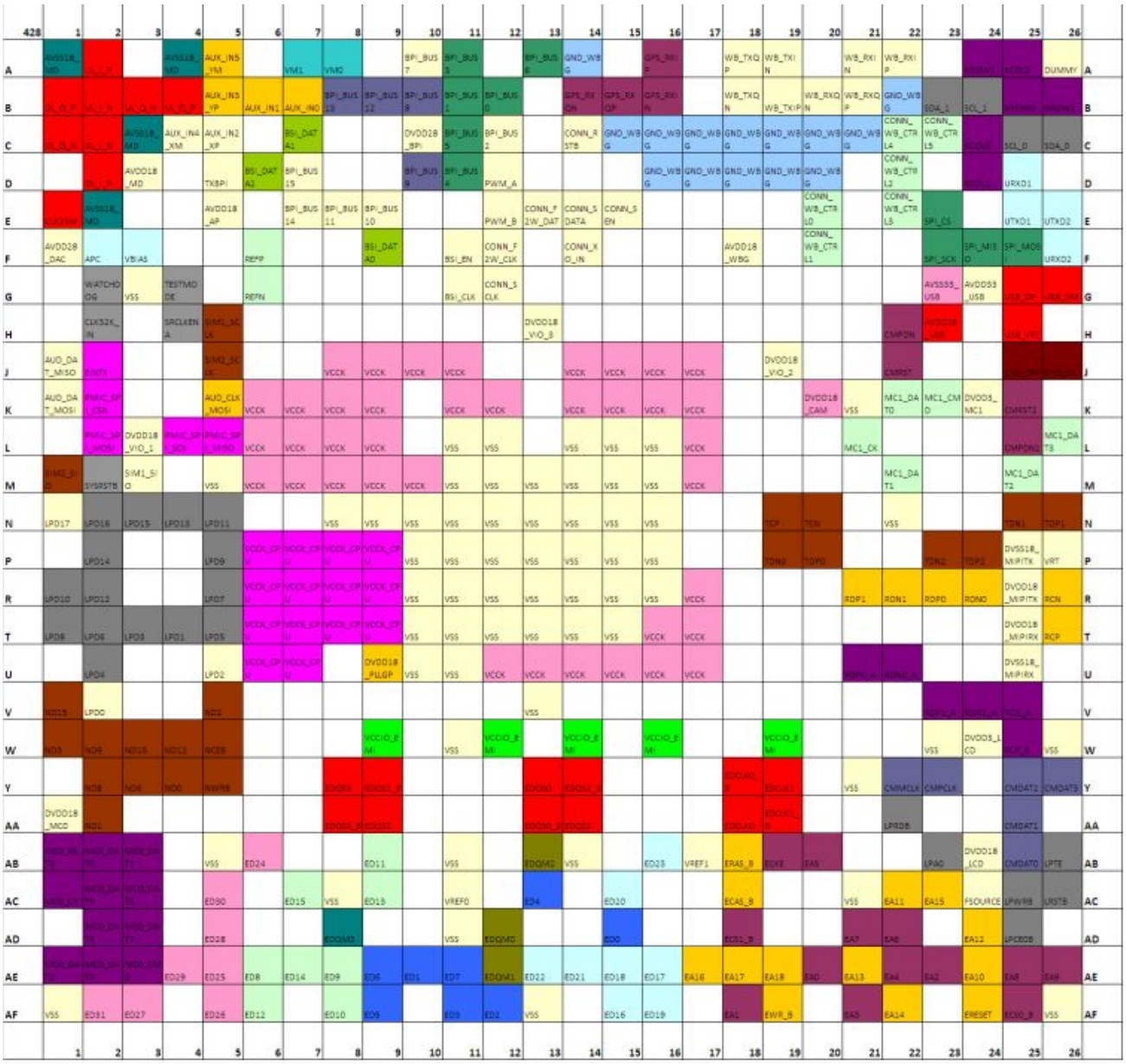
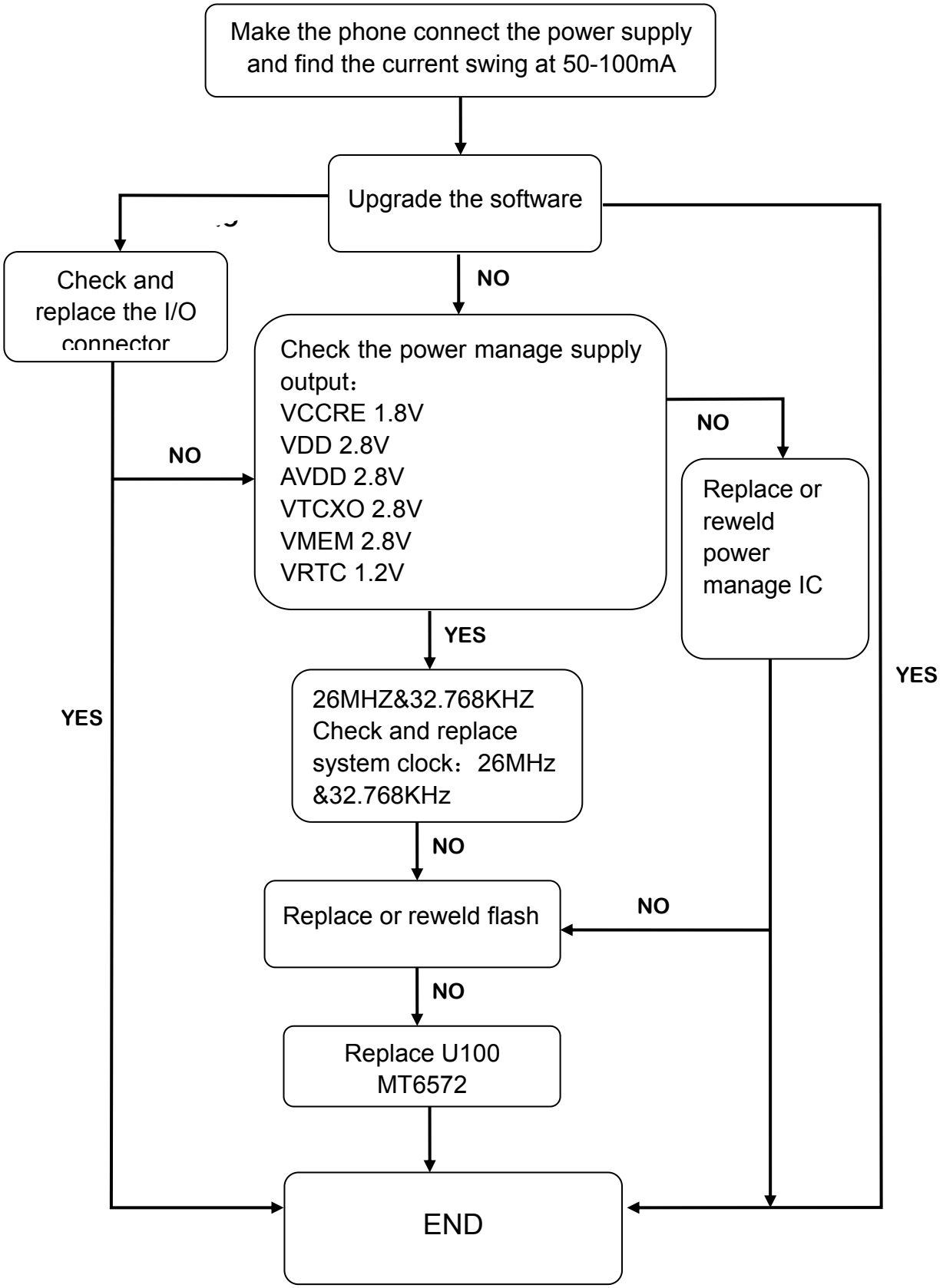
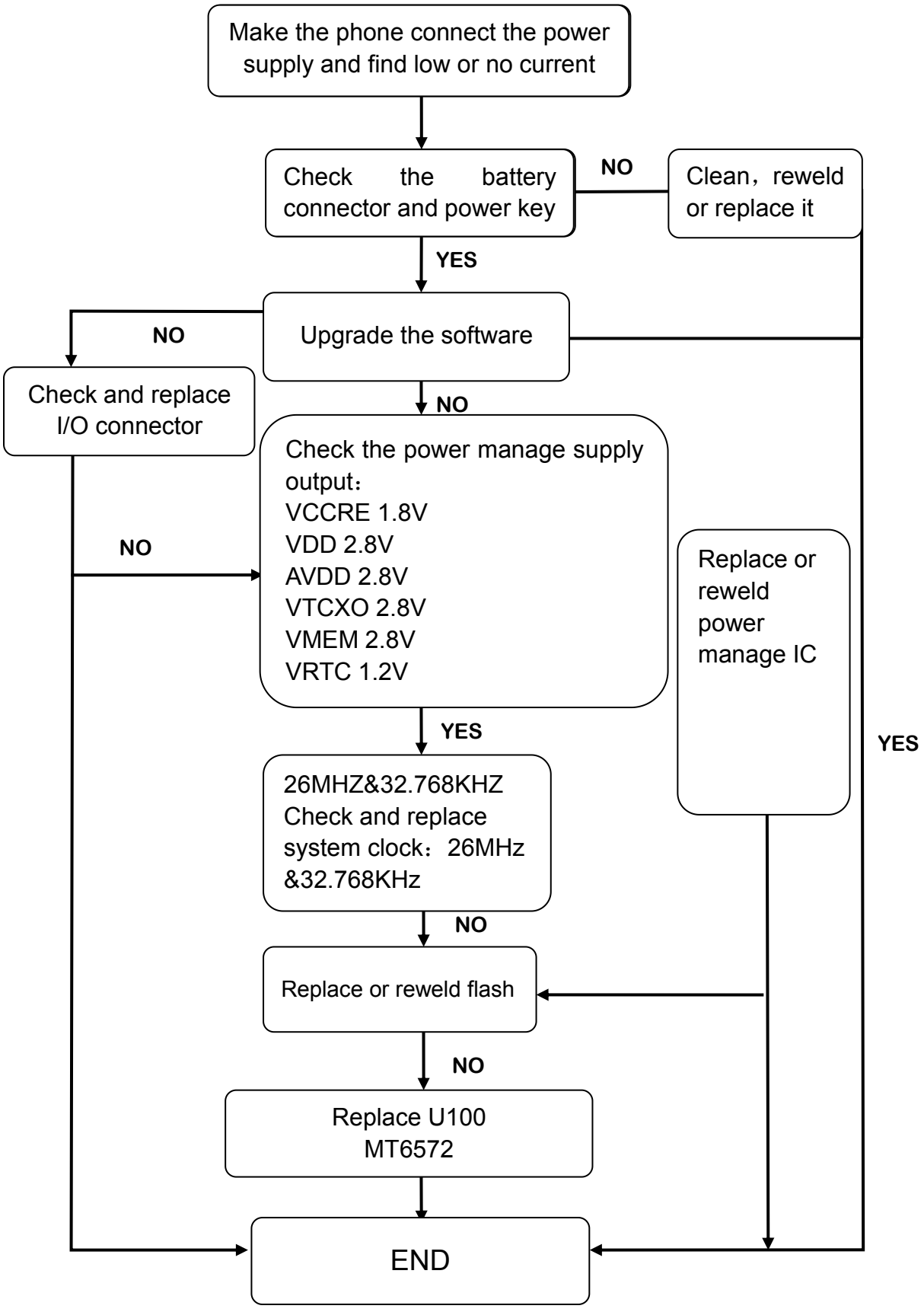


Figure 3. Ball map view for LPDDR2

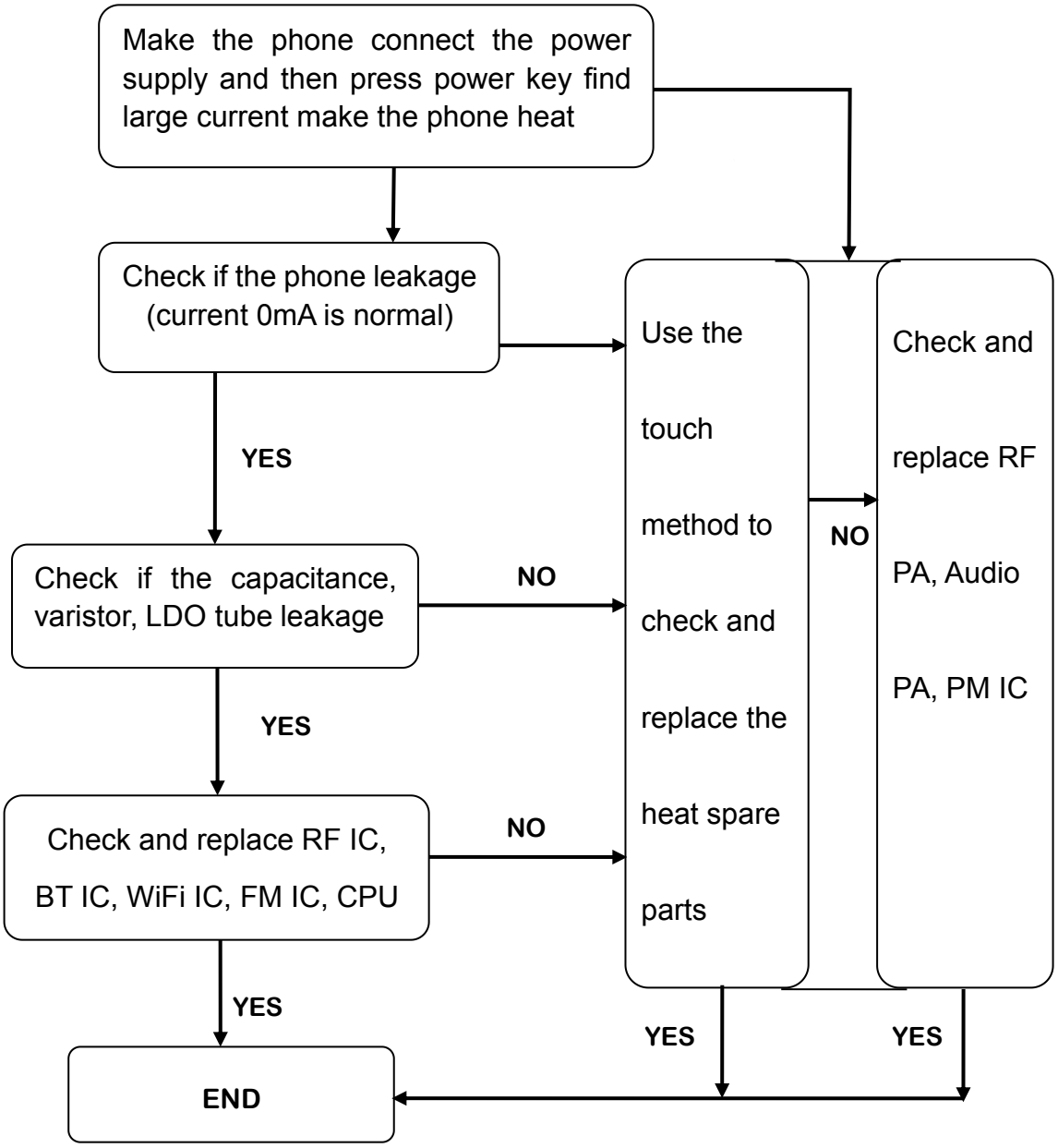
TROUBLESHOOTIng



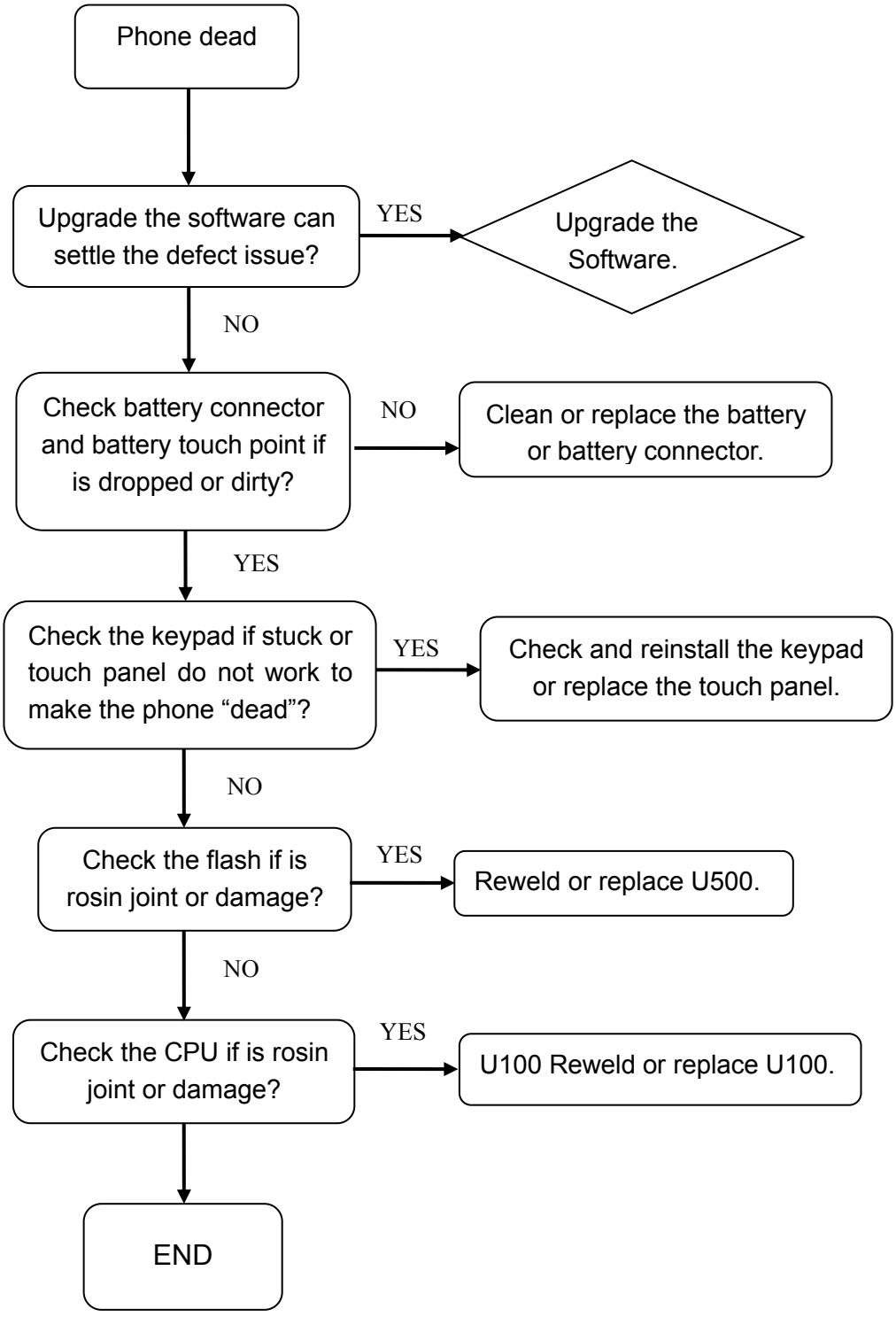
Cannot power on-low or no current



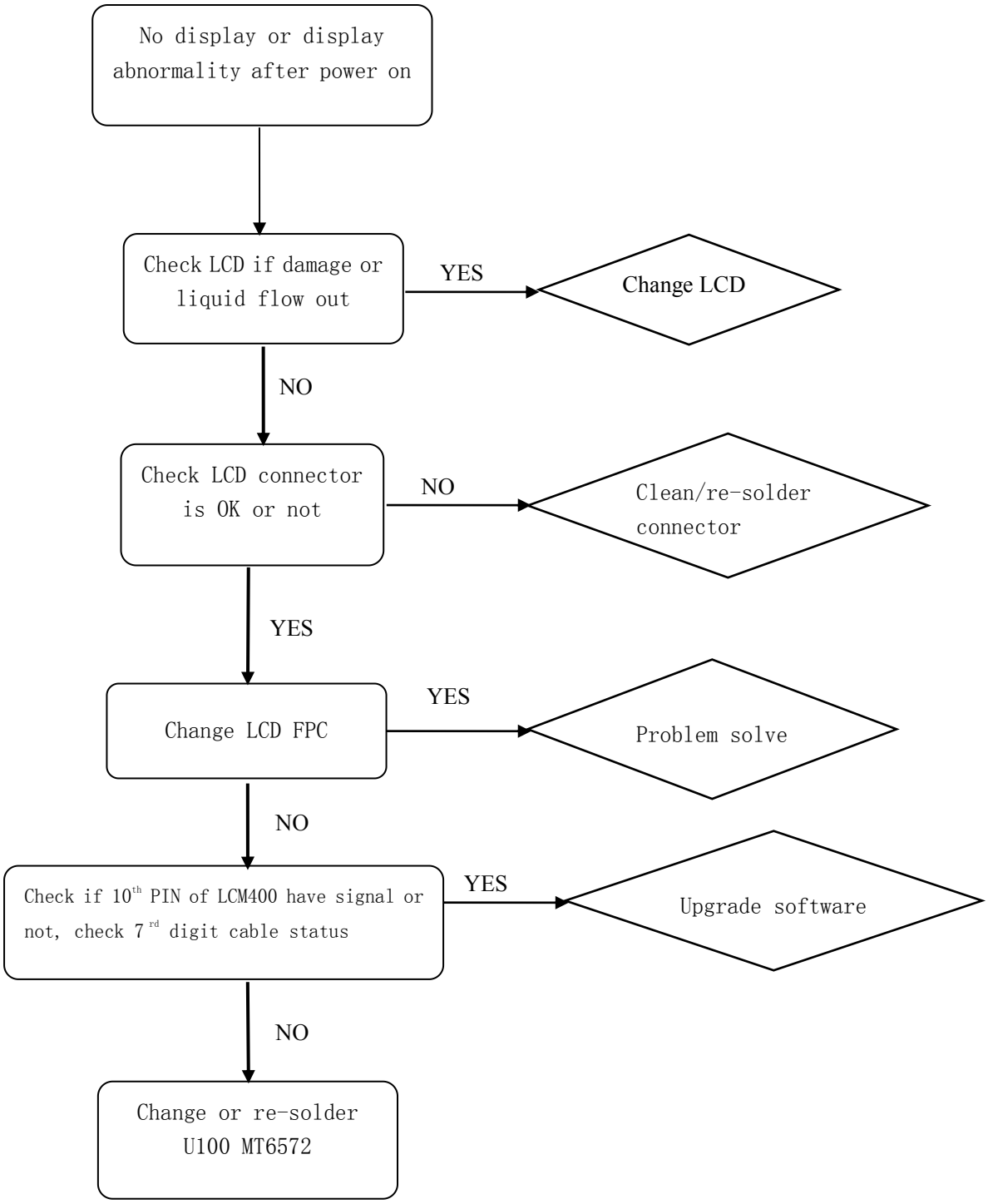
Cannot Power on-large current



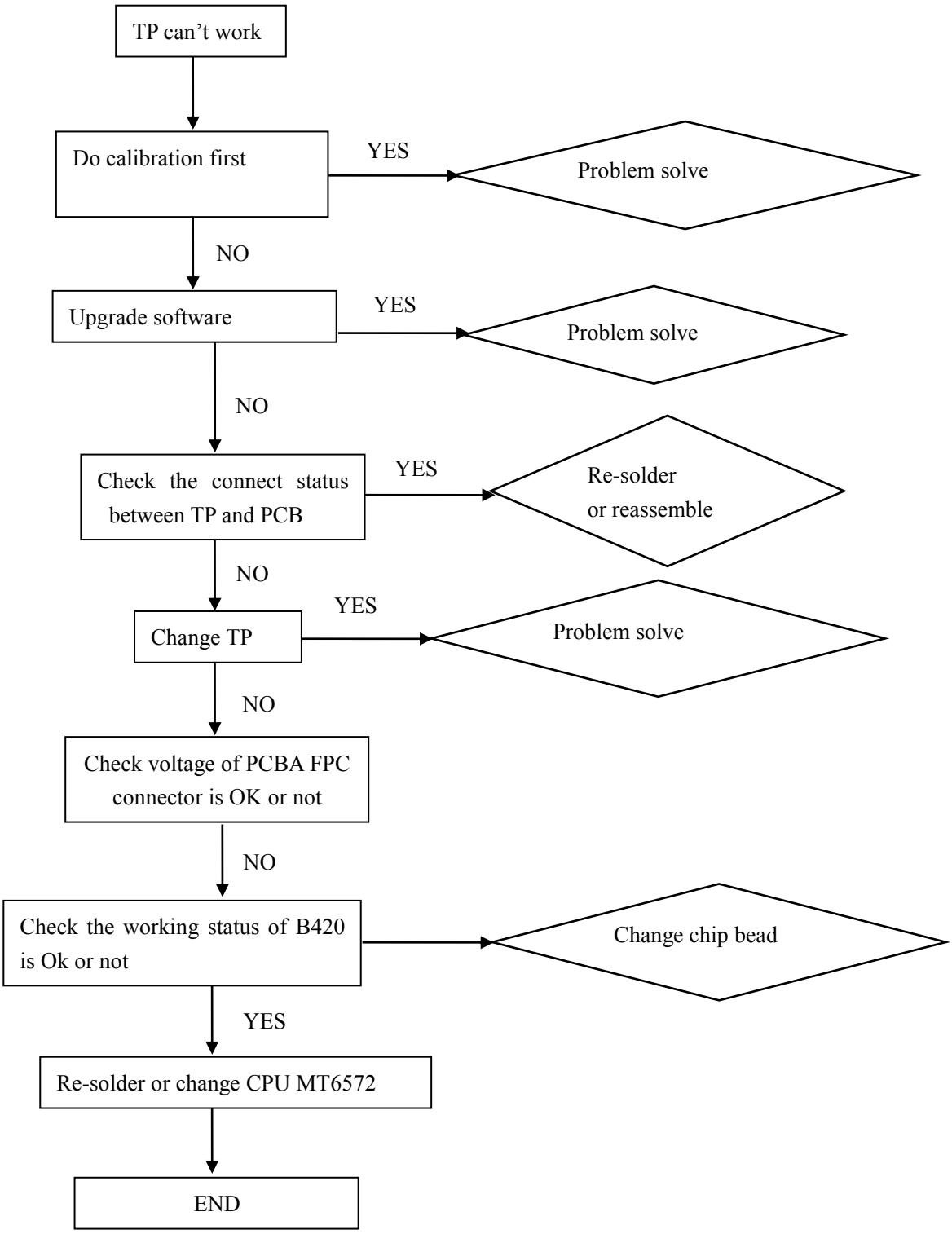
Repair flow for phone dead



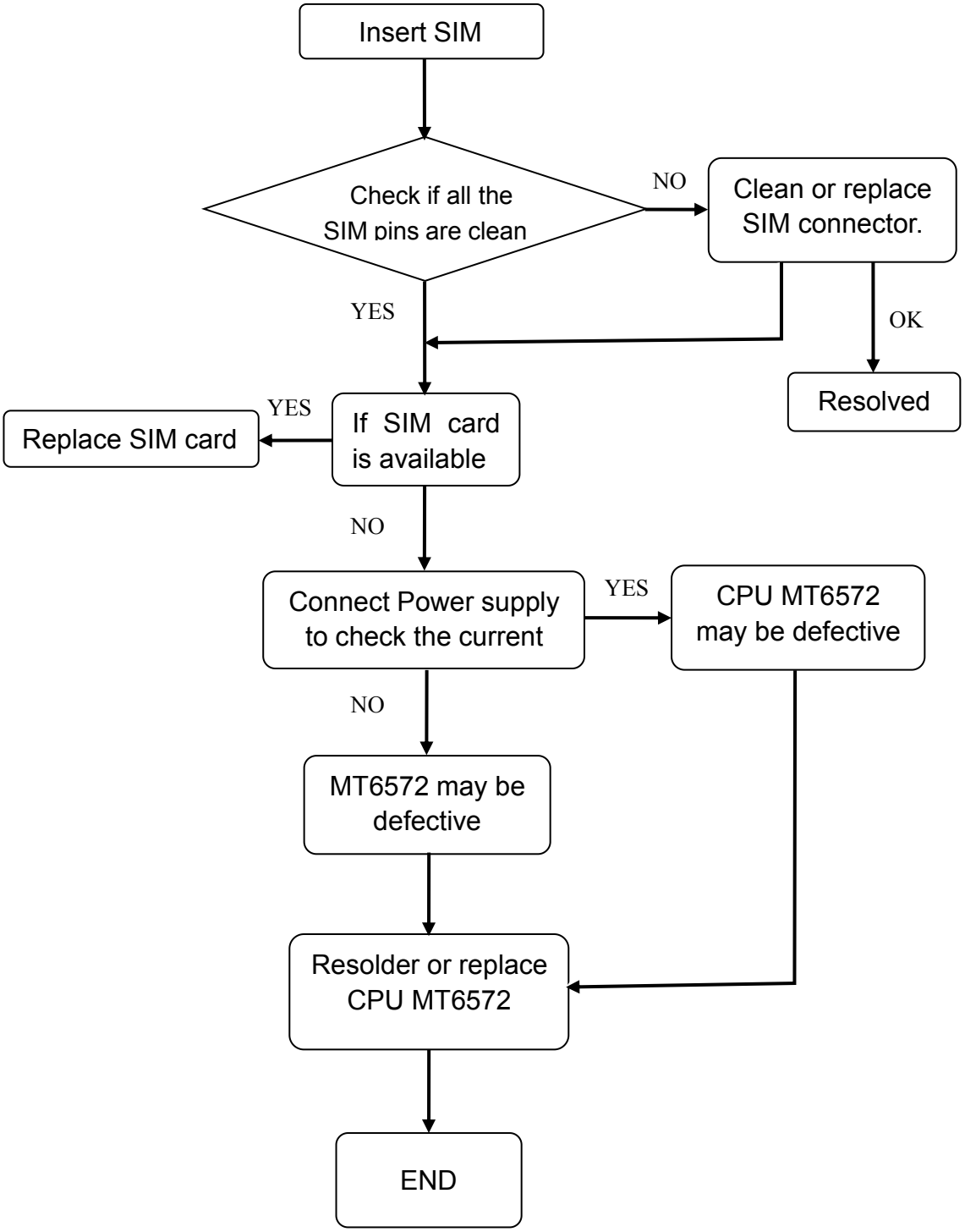
No display or display abnormality



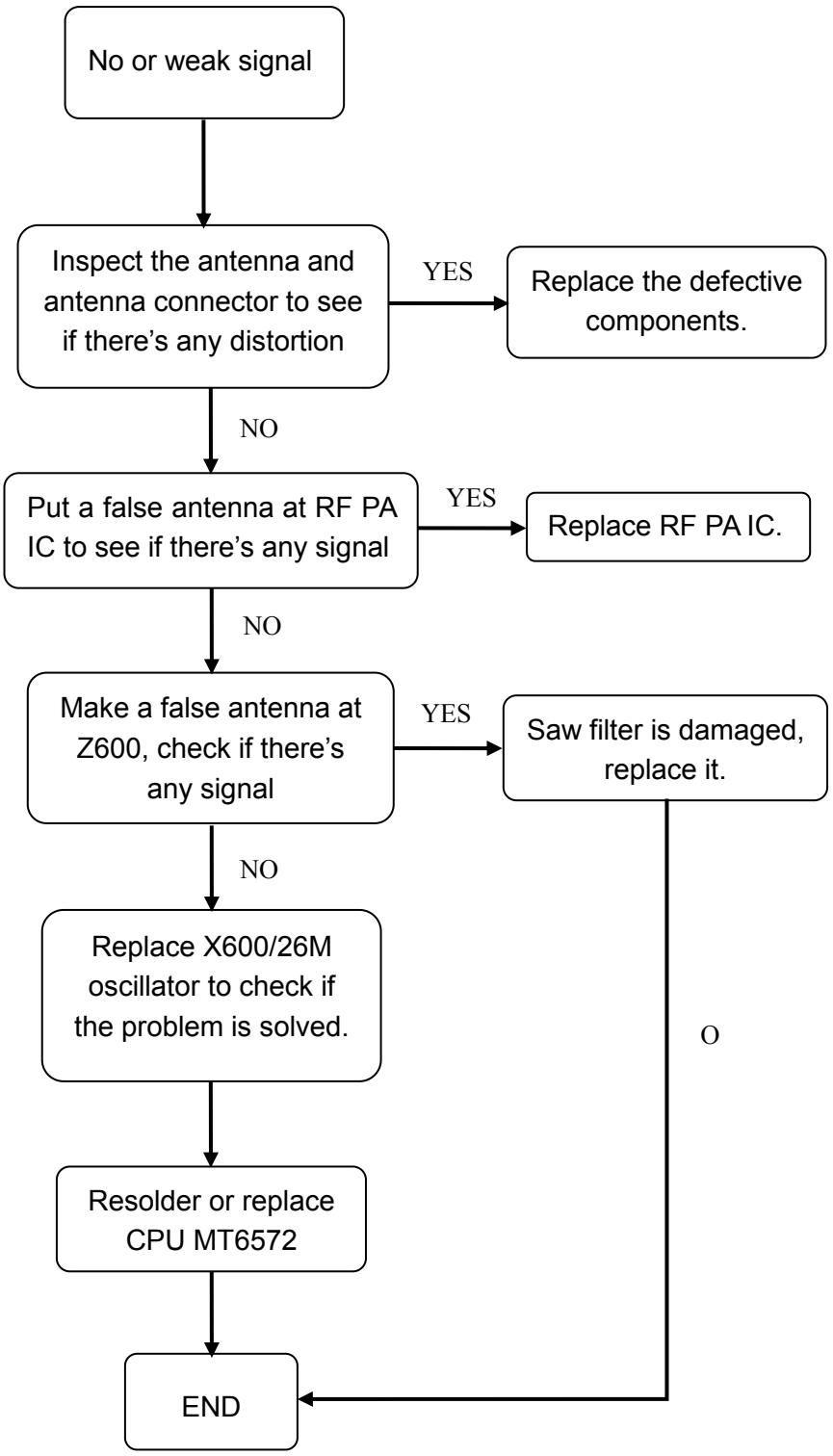
TP can’t work


TP can’t work
Do calibration first
YES
Problem solve
NO
Upgrade software
YES
Problem solve
NO
Check the connect status between TP and PCB
YES
Re-solder or reassemble
NO
Change TP
YES
Problem solve
NO
Check voltage of PCBA FPC connector is OK or not
NO
Check the working status of B420 is Ok or not
Change chip bead
YES
Re-solder or change CPU MT6572
END

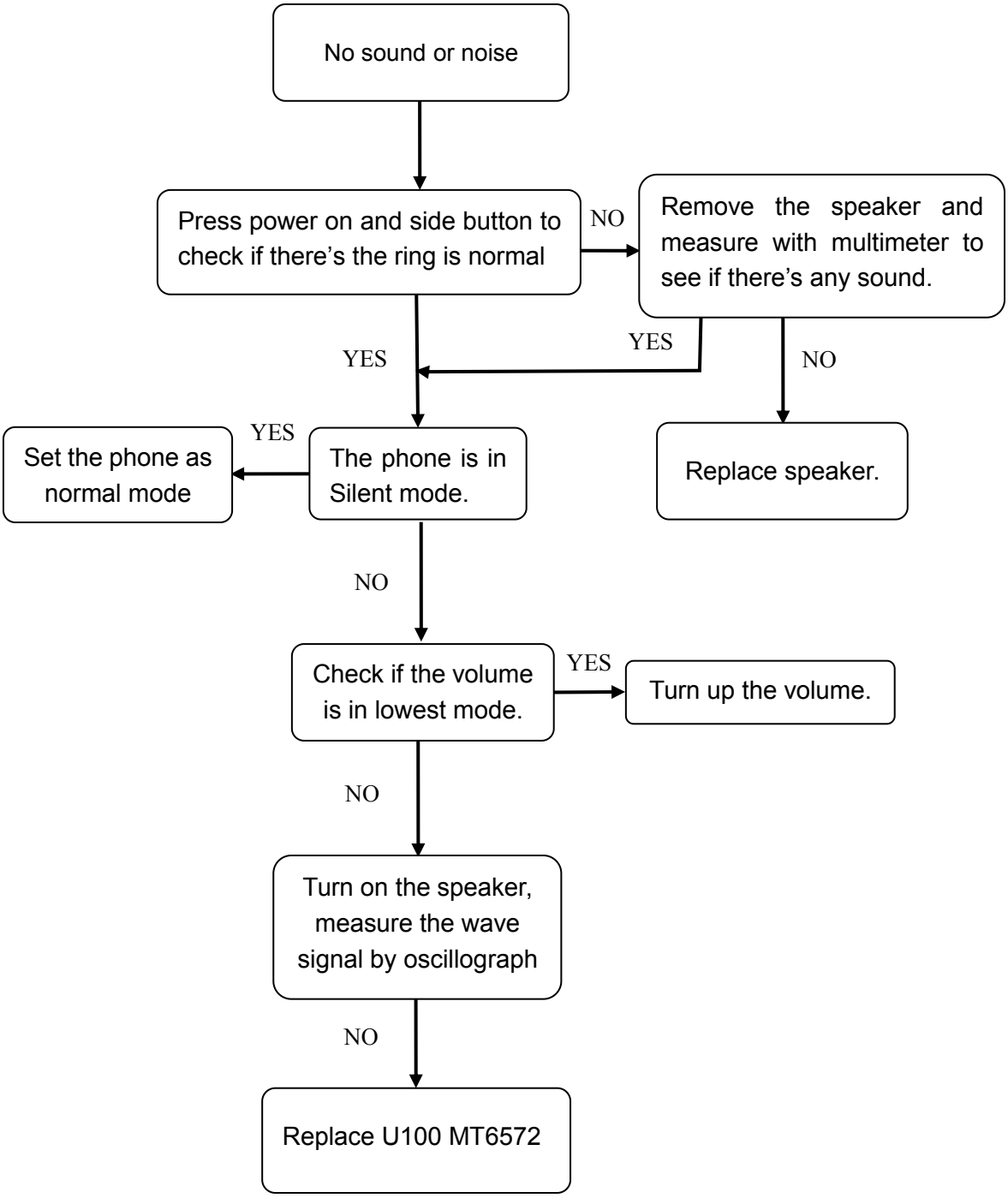
Insert SIM Repair Process



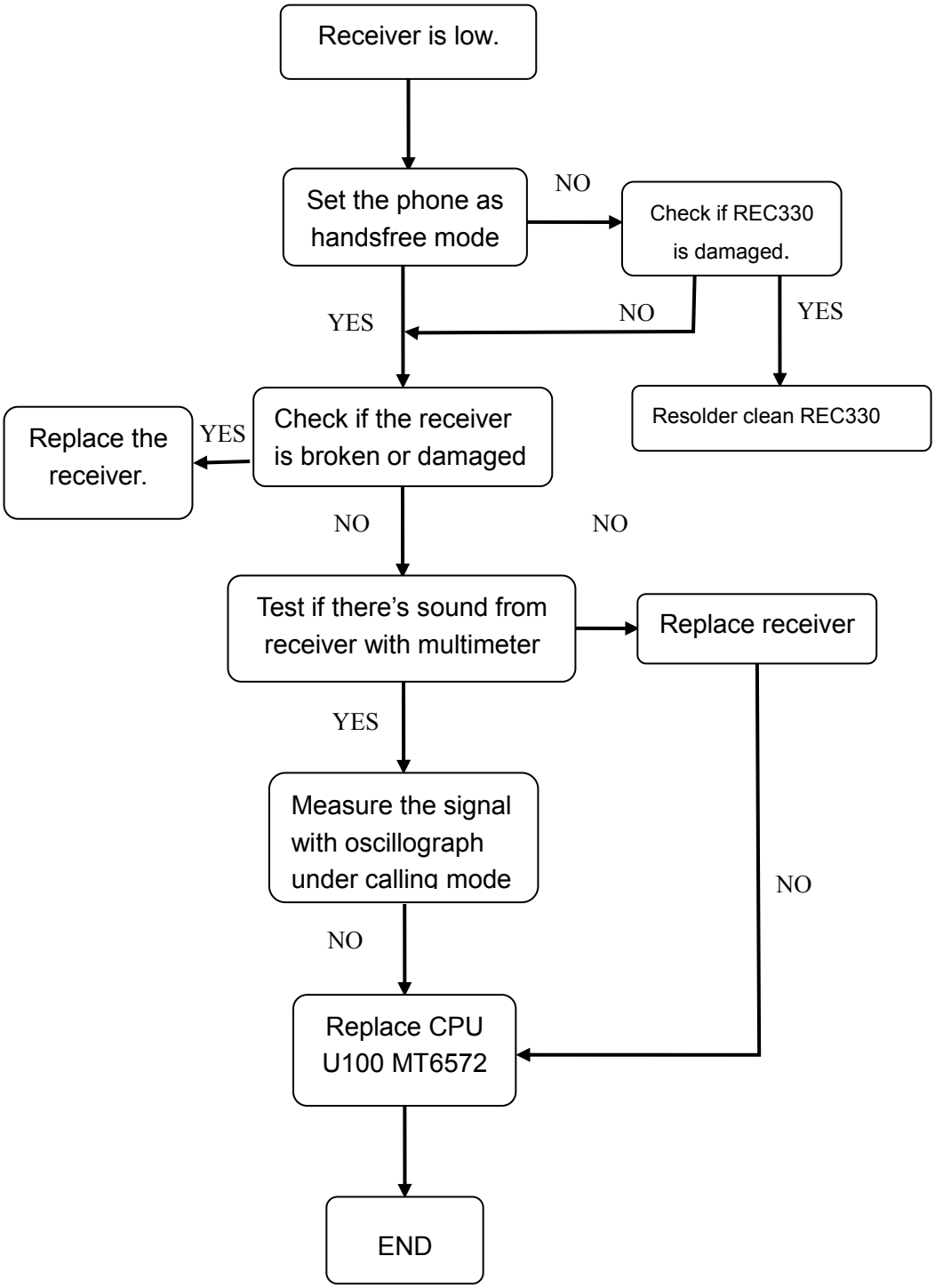
N0/weak signal trouble shooting



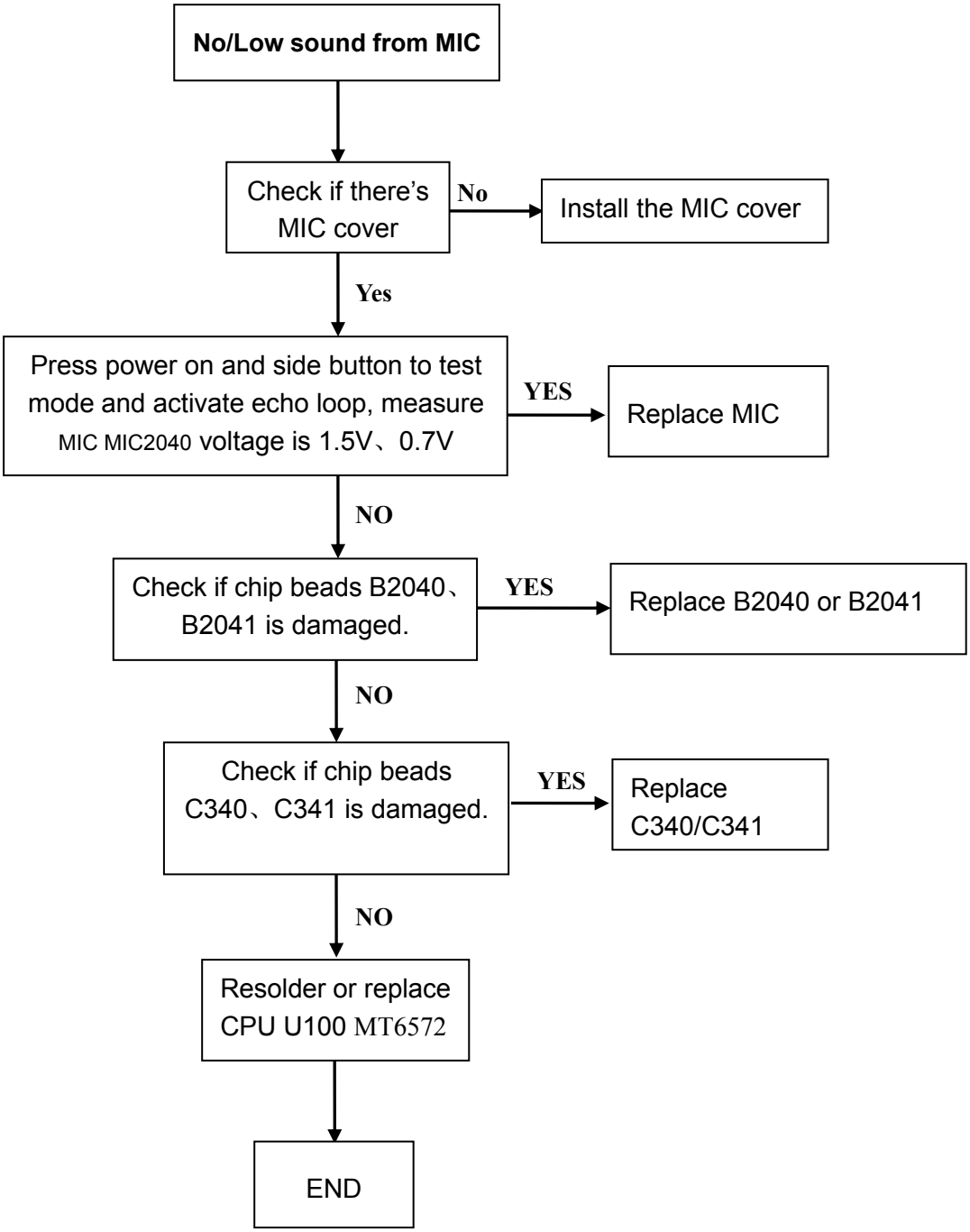
No/Low sound from Speaker



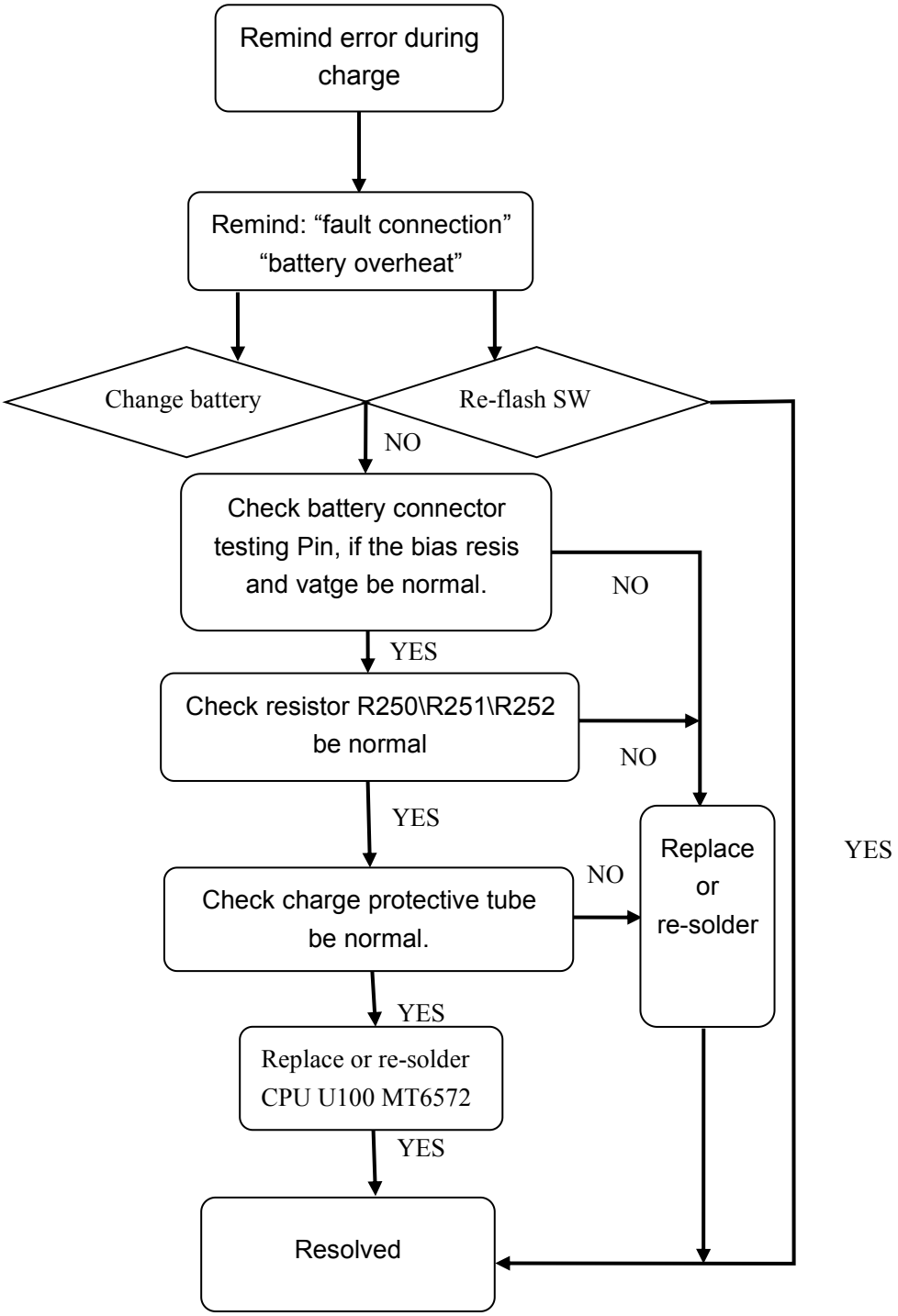
Receiver low voice or no voice



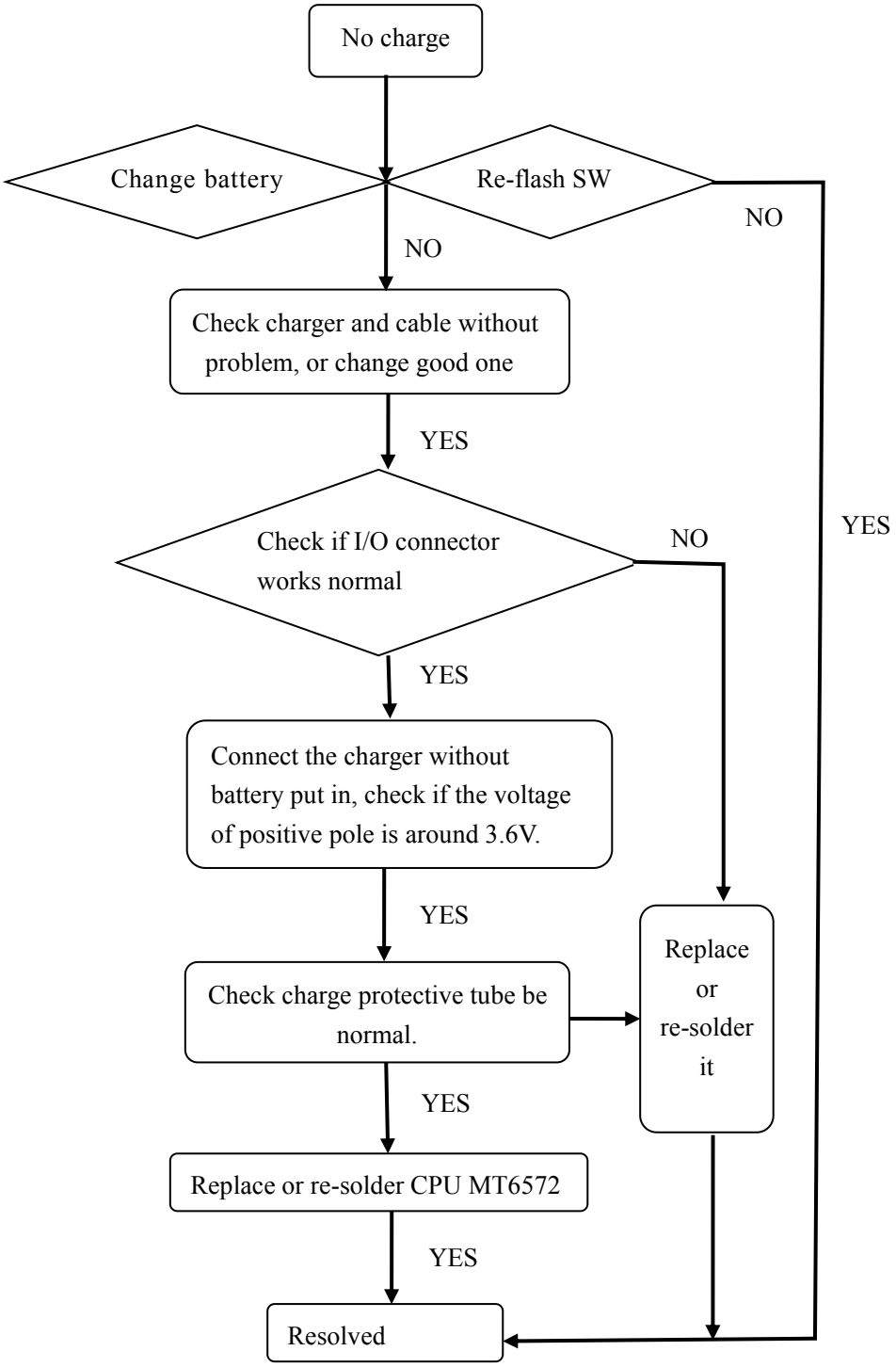
No/Low sound from MIC



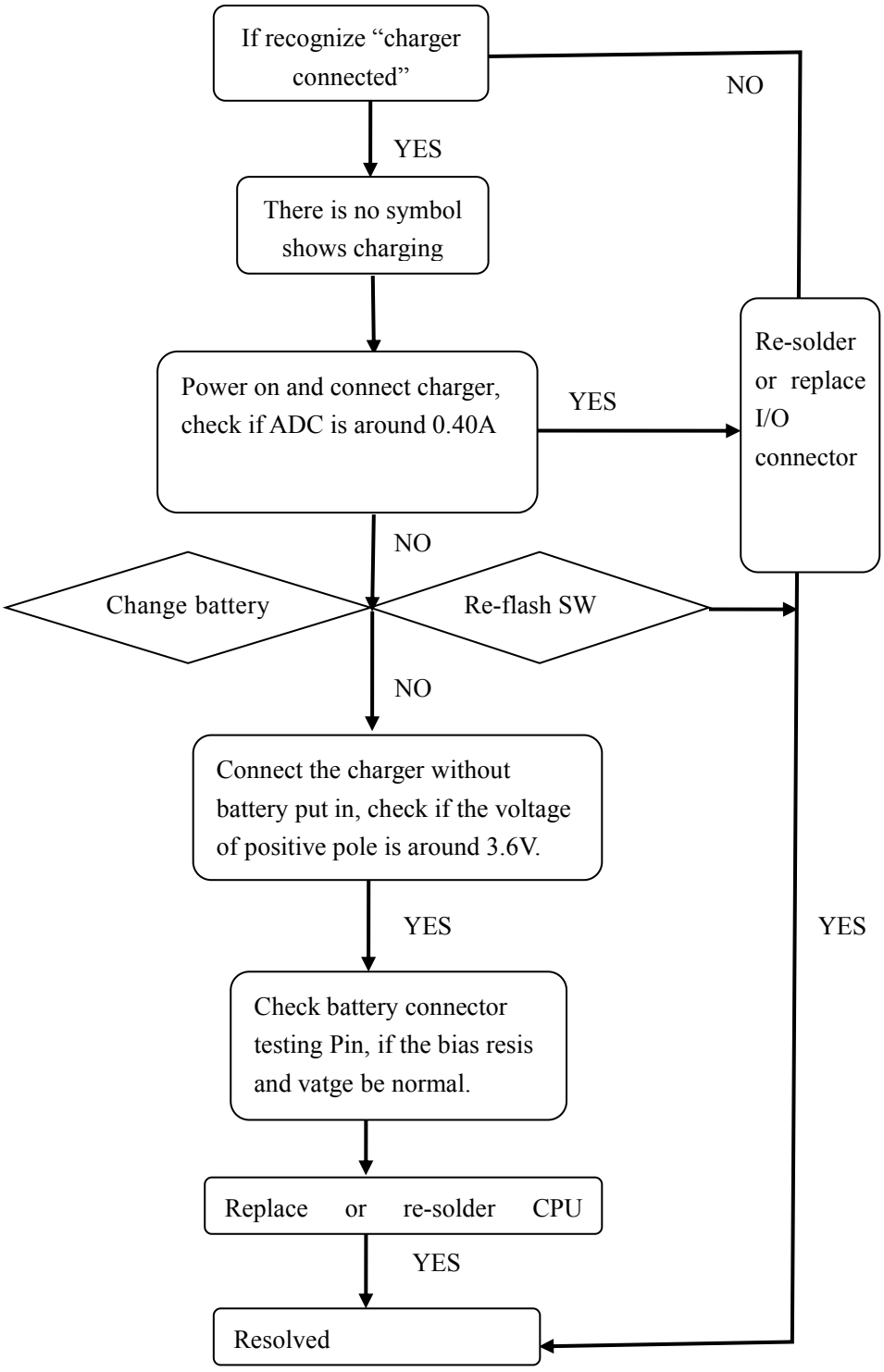
Does not charge – remind error charge



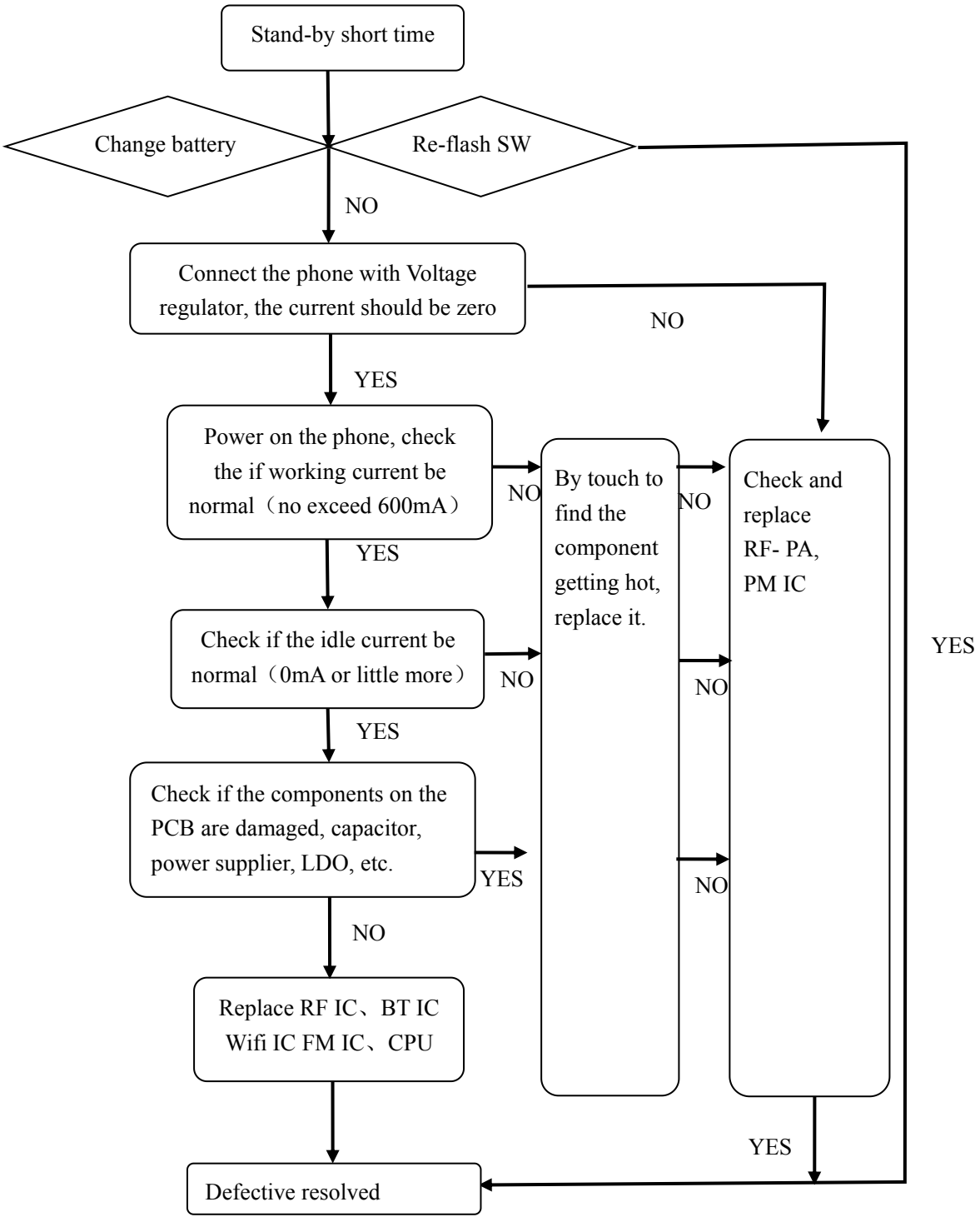
Does not charge – no charge



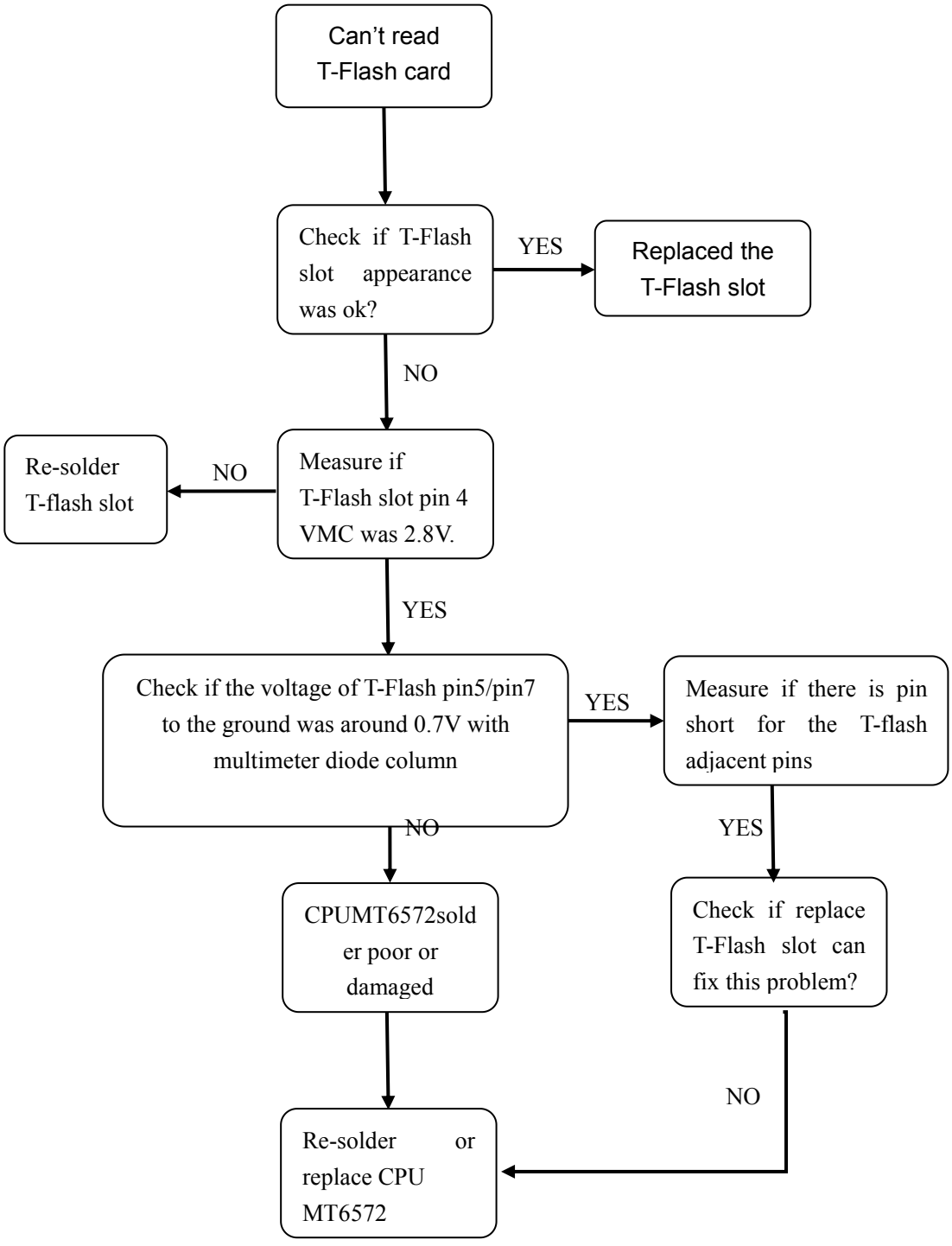
Does not charge – does not recognize charging



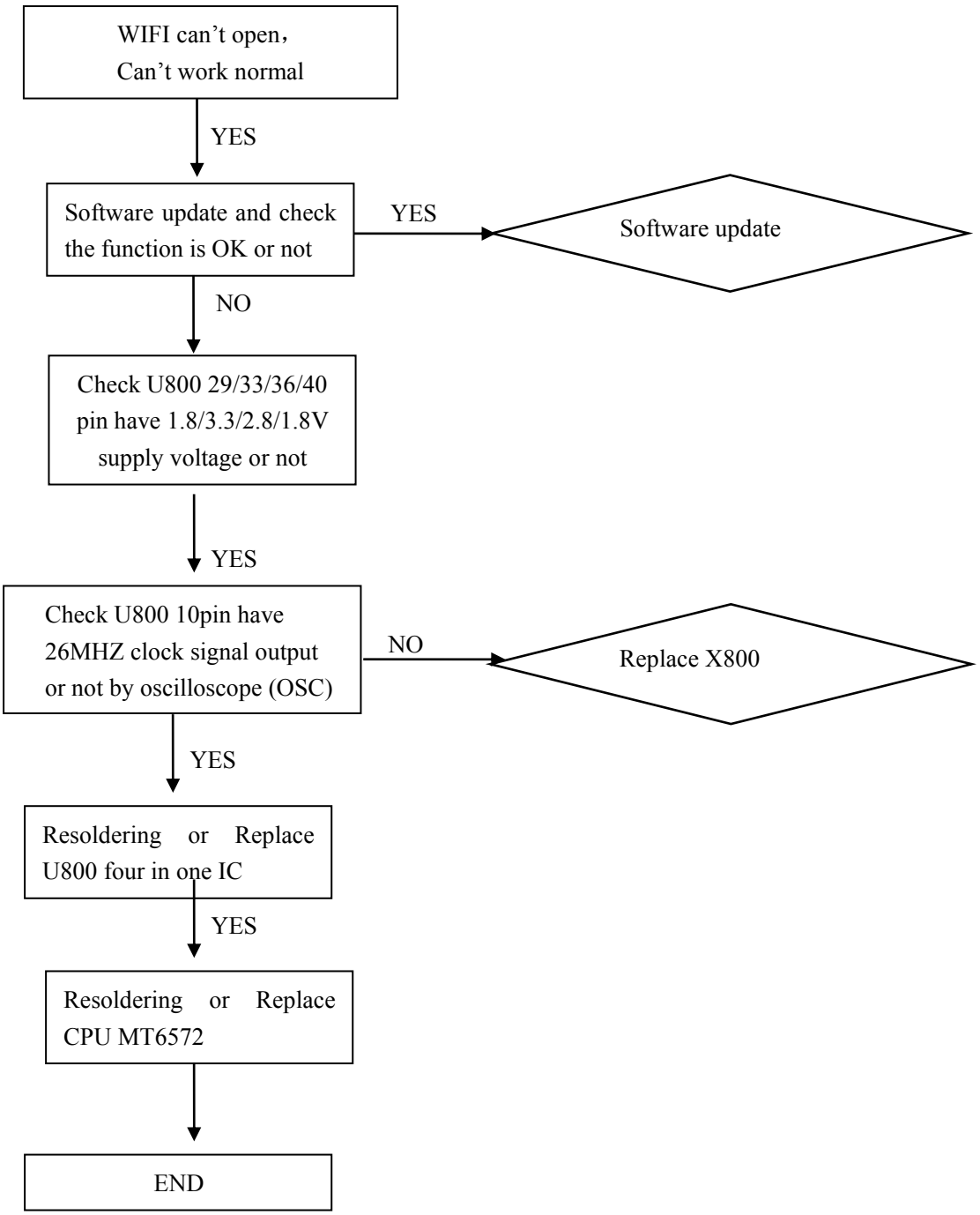
Stand-by short time



Can’t read T-Flash card



WIFI、BT、FM 、GPS defect repair flow chart



factory TEST

1.Insert T-Flash card and SIM card , Press power on and by side button at the meantime to enter factory mode for CIT test..

2. Choose Full test menu. to do full test.
3. Test relative items one by one.
4. Version check
5. LCD test
6. Vibrator:
7. LED test
8. Main loopback test..
9. Headset loopback.
10. Speaker.
11. Receiver.
12.main Camera.
13.sub camera
13: FM
14: Bluetooth.
15:Wifi.
16.sim

After finished the test, press ‘’back’’ button and return to Factory mode, and then choose ’’reboot’’ , the unit can power on at normal mode.